A Process Control Methodology Applied to Sub-micron Gate Lithography in Manufacturing GaAs MMICs

Peter W. Moran	Leaders For Manufacturing	Massachusetts Institute of Technology
Scott Elliott	Microwave Technology Division	Hewlett-Packard
Neil Wylie	Microwave Technology Division	Hewlett-Packard
Rebecca M. Henderson	Sloan School of Management	Massachusetts Institute of Technology
Jesús A. del Alamo	Electrical Engineering	Massachusetts Institute of Technology

Abstract

While many useful tools for pursuing process control exist, little has been written to guide manufacturing organizations in using these tools to realize process control on a facility wide basis; Consequently, many organizations fail to realize significant process improvement despite repeated attempts. To fill this gap, a methodology for guiding process driven manufacturing organizations in instituting process control is proposed. The methodology begins with definition of the customer's expectations and of the manufacturing process used to meet these expectations. The output of a given process or sub-process must reach four progressive levels of control. When the output can be reliably measured, it is considered Measurable. The second level is reached when this output, viewed in aggregate and over time, is found to be Predictable. When the distribution of outputs is centered within the spec limits and a 'sufficient' fraction of the output lies within the spec limits, the process is considered Acceptable. Finally, when the process, as it is currently operated, is fully documented and operator technique is passed on through training, the process reaches the fourth and final level of control, Recoverable. An application of this methodology to the control of sub-micron gate lithography on a GaAs MMIC process at Hewlett-Packard's Microwave Technology Division is discussed. Finally, the unexpectedly broad organizational implications of developing and instituting this methodology at MWTD over the past two years are briefly described

1) Introduction

Well controlled processes have been shown to be economically and strategically beneficial to the long term competitive abilities of a firm, yet many firms - particularly American ones - have made little progress in improving the level of control of their manufacturing processes.[1] While process control is a primary goal in some of these organizations and many useful tools are available to assist in accomplishing process control, many organizations still fail to realize substantive improvement. Experience at Hewlett-Packard (HP) suggests that at least one barrier to further progress is the lack of a clear pattern for managing the introduction and integration of process control techniques to an organization. The many false starts in pursuing process control that organizations make suggests that the need for a clearer pattern for managing this organizational change is needed.

Prior work on the control of manufacturing processes is quite extensive. Most of this work has focused on tools, such as the control charts, histograms and pareto charts, that play a specific, but limited, role in achieving process control. More recently, researchers such as Taguchi have added new tools to the field with improved experimental techniques and more explicit evaluations of "quality loss".[2] While many such tools are useful, if not invaluable, in achieving process control, they emphasize localized optimization of some aspect of a single process, to the possible detriment of an organization wide process control optimum. Furthermore, none of them consider the broader question of how a manufacturing organization, set in a pattern of operation that has not aimed for process control in the past, goes about defining what it means by process control and incorporating available tools into their daily operations to achieve such control. Meanwhile, a few management researchers, most notably Bohn, have better explained the value of process control by demonstrating the link between environmental noise (which is at least partially a function of the degree of process control) and the speed of organizational learning.[3] Still, little has been written on how to guide an organization in adopting available tools and pursuing process control, yet this may be one of the most critical aspects to successfully attaining process control.

At Hewlett-Packard's Microwave Technology Division (MWTD), which supplies a wide variety of leading edge, solid state components operating in the RF, Microwave, and Lightwave frequency ranges to HP's instrument divisions, the growing number of processes supported and increasing volume of devices produced has placed an increasing emphasis on process control as a necessary element in providing these devices reliably and at costs competitive with external sources of supply. From MWTD's attempts to improve process control has grown the MPAR methodology (M.P.A.R. is an acronym for the four levels of process control: Measurable, Predictable, Acceptable, and Recoverable) that now guides the division's efforts to define, institute, and continually improve its level of process control.

This paper describes the M.P.A.R. methodology. On the surface, MPAR seems straightforward, yet its application to the control of sub-micron gate lithography for the production of GaAs MMICs (Monolithic Microwave Integrated Circuits) reveals some subtle complexities. The paper includes a discussion of the impacts to the organization of using the MPAR process.

2) The M.P.A.R. Methodology

Experiences at MWTD suggested that efforts to utilize existing statistical and experimental tools to improve process control often suffer on three fronts:

* Mr. Moran is currently with McKinsey & Company, Inc.

- Control of complex, multi-step processes, well beyond the scope of a single individual, cannot be readily broken down into discrete pieces such that realistic responsibility for a process unit can be assigned to a single engineer.
- While most engineers and operators are at least exposed to current statistical and experimental techniques, such techniques are used only sporadically and acceptance is slow to increase.
- Management, faced with an extremely broad array of processes, each in different stages of a life-cycle, cannot easily and with confidence manage process improvement.

The MPAR methodology addresses these three problems by providing, on a consistent basis throughout the organization:

- a definition of "process" and "process control"
- a pattern to assure that process improvement followed an orderly procedure
- a simple, clear means to measure the level of control on several processes

3) Customer Expectations

The M.P.A.R. methodology[4], shown schematically in Figure 1, begins with a definition of who the "customer" is and definition of the customer's expectations. "Customer" is a figurative term that can represent the actual person receiving the finished product or, more often, the downstream process or co-worker that is affected by the output of the process under consideration.

One new and important fabrication process at MWTD is the MMIC-A process used to fabricate a variety of GaAs MMICs. While MPAR is being gradually applied throughout the MWTD facility, an in-depth application was undertaken by examining the production of a primary electrical parameter of one part produced on the MMIC-A process[5].

Among the circuits produced on the MMIC-A process is a 2-26.5 GHz traveling-wave amplifier. Gain Slope, defined as

$$\text{Gain Slope} = \frac{\text{Gain(max)} - \text{Gain(min)}}{\text{frequency range}} = \frac{\text{Gain(max)} - \text{Gain(min)}}{24.5\ \text{GHz}} \quad (1)$$

is a parameter of critical interest to HP's microwave instrument designers interested in supplying microwave amplifiers with constant gain over a broad frequency range. Thus, an essential customer expectation of the traveling wave amplifier is a small gain slope.

While this expectation represents a suitable output of the MMIC-A process it has the distinct disadvantage that it can only be measured when the multi-step fabrication process is completed. Study of the circuit physics of this traveling wave amplifier suggests that gain slope is largely determined by the input capacitance of the MESFETs used to construct the amplifier circuit.[6] In turn, device physics suggest that input capacitance is a strong function of gate length.[7] Using these relationships, the customer expectation for gain slope can be translated to a comparable expectation for a physical feature of the MESFET devices created, gate length (L_g).

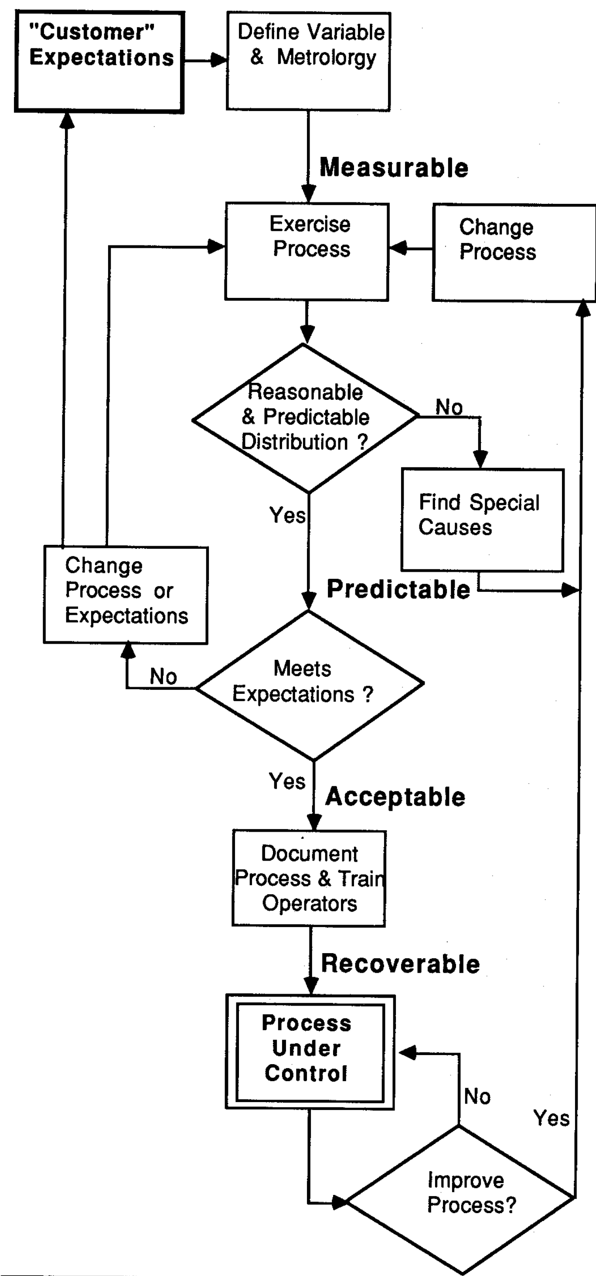

Figure 1: Schematic Overview of M.P.A.R. Methodology

4) The Process

A "process" for these purposes is 'a series of (repeated) actions used in manufacturing something'. Processes are hierarchical in nature in that they can be divided into a series of sub-processes, each of which can be considered a process unto itself. The methodology considers three types of processes that most directly affect the manufacture of saleable items:

1) Processes which add value to materials by either altering them, sorting them, or moving them closer to the customer application.
2) Processes which verify the product materials, processing equipment, or construction of the product; e.g., setting up a stepper for even field exposure.
3) Processes which alter data about the product materials; e.g., metrology, or data storage and manipulation.

This application has focused mainly on the first two types of processes.

The MMIC-A process[8] requires the eleven masking levels outlined in Figure 2. The critical gate region (which will be shown to be of particular interest in this application), however, is fully formed after the fourth masking layer and changes little during subsequent processing. Initial processing begins by growing a doped GaAs active region on a semi-insulating GaAs substrate. Oxide is deposited by a CVD process to provide field passivation. Initial masking steps pattern the oxide for deposition of ohmic contacts, allow for proton isolation of active devices and pattern the oxide for sputter deposition of a thin film resistor. At this point, wafers begin the critical processes that lead to gate formation.

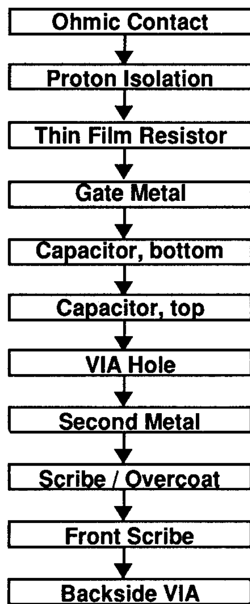

Figure 2: MMIC-A process flow

The Gate Formation Process

The MESFET gate is formed through a series of processes depicted in figure 3.1 - 3.6 and the final gate is shown in figure 4.

Gate processing begins by spinning on a 0.6 µm polyimide layer to planarize the wafer surface (other surface features are ~0.2 µm off the active layer) and to provide a lifting medium for the transfer layer after the gate metal is deposited. After the polyimide is baked to provide stabilization, a 0.5 µm PMMA layer, is spun on to act as an imaging resist (see Figure 3.1)

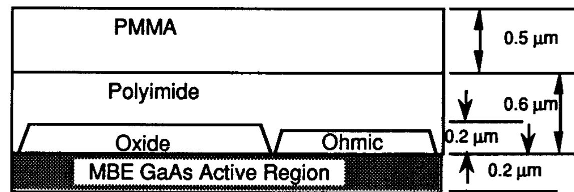

Figure 3.1: Gate region profile after spinning on Polyimide and PMMA

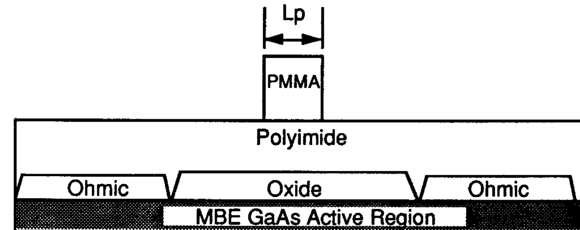

Figure 3.2: Gate region profile after developing PMMA

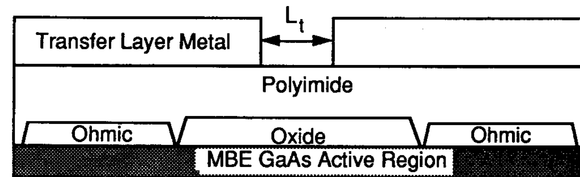

Figure 3.3: Gate region profile after evaporating transfer layer and lifting PMMA

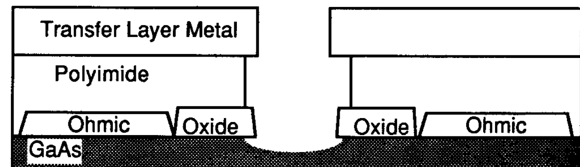

Figure 3.4: Gate region profile after etching polyimide, oxide, and active-GaAs

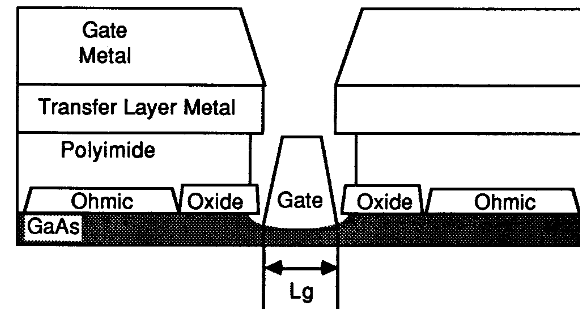

Figure 3.5: Gate region profile after evaporating gate metal

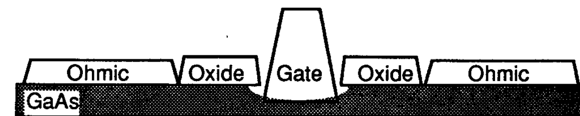

Figure 3.6: Gate region profile after lifting polyimide

After a stabilization bake, the PMMA is aligned and exposed with deep-UV illumination on a contact lithography system. The process design attempts to keep exposure dose constant by calibrating the illumination level before every batch is run. Calibration is accomplished using an exposure analyzer to measure intensity and then dividing this into the total desired dose to get the necessary time.

Developing is done in a 50:50 mixture of MIBK:Iso to remove the exposed PMMA and leave a PMMA line of length L_p. Batch-to-batch variation in developing is reduced by targeting the develop time before each new batch is processed. Targeting is done using a silicon "dummy" wafer. A single dummy is developed for a set period that approximates, but undershoots the necessary develop time. The resulting PMMA line is then examined with a SEM. Based on the line length observed and an experimentally determined function of change in L_p with increased develop time, the dummy is redeveloped. This process continues until L_p on the dummy is within the acceptable limits of 0.30 µm to 0.38 µm. Nominal L_p equals 0.35 µm. Then the total develop time, nominal develop time is 120 seconds, of the dummy is used to batch develop the actual product wafers. It is assumed that this calibration corrects all batch-to-batch variability in prior processing as well as batch-to-batch variability present in the develop process. (See Figure 3.2)

Subsequent processing seeks to transfer the current critical feature, the PMMA line, to an approximately equal line of gate metal. To accomplish this, a metal transfer layer is E-beam evaporated, which because of the PMMA thickness and sharp profile, is non-conformal. A transfer layer opening, of length L_t, is left when the PMMA is lifted off and the transfer layer now acts as a conformal mask. (See Figure 3.3). L_t, as shown in the preceding section, is the parameter selected as an in-process monitor of gate fabrication.

Reactive Ion Etching (RIE) is used to transfer this pattern anisotropically through first the polyimide and then the oxide. An isotropic wet etch process is used iteratively to etch the semiconductor and target the drain current, I_{dss}, by controlling channel depth with the etching process. (See Figure 3.4). The gate metals are sequentially evaporated into this trench with the effective gate length controlled by the location of the sidewalls, the steepness of the trench profile and the aperture in the evaporator. (See Figure 3.5). Finally, the polyimide is lifted off in NMP to remove the transfer layer and the excess gate metal. This yields the final gate profile. (See Figures 3.6 and 4).

5) The Four Levels of Process Control

When the process under study and the expectations of this process are defined, control of meeting these expectations is increased along four levels, as follows. (Follow along with figure 1)

5.1) Measurable

The output(s) of concern to the customer must be defined precisely and a means for objectively and accurately assessing this output must be developed. Once done, the process or process step has reached the first level of process control, **Measurable**.

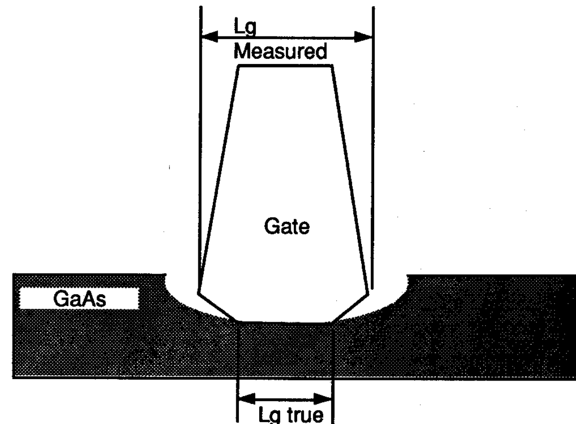

Figure 4: Mushroom structure of MMIC-A process's gate

This first level is often difficult to accomplish, particularly in semiconductor fabrication where the physics of working devices are not completely understood and the physical features of interest often range from sub-micron down to atomic scales. Measurement of relevant parameters is often difficult, inaccurate, unrepeatable and expensive.

With an expectation for the MMIC-A process comparable to the customer's, but measurable at a point in the process reasonably close to those sub-processes that actually determine the output of interest, one attempts to make these sub-processes measurable. Unfortunately, due to the mushroom shape of the gate, gate length can only be measured accurately by scribing and breaking the wafer along the gate, a difficult and destructive process that adversely affects the additional mask steps needed to create the finished circuit. Since gate length is difficult to measure, it is useful to find an alternative process output that can be measured. A detailed study of the gate metal evaporation process suggests that gate length should be closely related to transfer layer length (L_t) for this MMIC-A process, making transfer layer length a suitable output to measure to achieve control of gain slope (see figures 3.3-3.5). Current processing calls for five sites per wafer on each production wafer to be measured for transfer layer length using a SEM that provides accuracy and repeatability better than 0.015 µm, which is within the allowable variability. Consequently, we can consider the gate formation process to be "measurable". Note that the method used to make this process measurable is not unique. One could use a variety of other metrology methods, from optical microscopy of transfer layer length to electrical probing of a test cell specifically designed to approximate the gate length.[9]

5.2) Predictable

Once a particular process is Measurable, it is run over a period of time during which data is collected to study the output. This allows observation of the variation currently existing in the process.

Prior research is useful in defining a "statistically significant sample" of measures of the output[2]. When a sufficient data set has been taken, one examines the data to see if the distribution is reasonable and expected.

Here again, prior work, such as tests for normality, is available to assist in determining whether a distribution is reasonable[2]. Proper application of these tests requires the choice by the engineer or operator of a suitable physical or mathematical model of the process. Such models suggest a particular type of distribution, such as normal or bi-modal, for which a statistical test can then be applied.

When the distribution of a statistically significant sample of the measured output does not meet expectations for these types of process, further exploration and experimentation must be done to find the causes of unexpected behavior and the process must be modified to eliminate those causes. Only when the distribution of measured outputs is reasonable and expected with a high statistical confidence for the given type of process, has the process met the second level of process control, **Predictable.**

Since regular transfer layer data is available on all production wafers, it can be examined in aggregated form. Control charts and histograms are two useful representations of such aggregate data. Standard statistical tests are useful in suggesting whether such data are to be expected. Figure 5 shows a histogram of transfer layer lengths which can be tested for normality. If normality is shown to be statistically likely, other tools can be used such as control charts. When transfer layer length data is plotted on a control chart, as in figure 6, further tests of reasonableness can be made. For instance, the run of seven points on one side of the mean in the control chart is an improbable event that should be more closely investigated. Using MPAR highlighted that there are few tools to guide the engineer or operator in these investigations other than reviewing the processing of wafers that diverge from expectations in the hopes of uncovering some bias to the process. Still, only when the distribution of transfer layer lengths is well behaved is the gate formation process considered to be "Predictable".

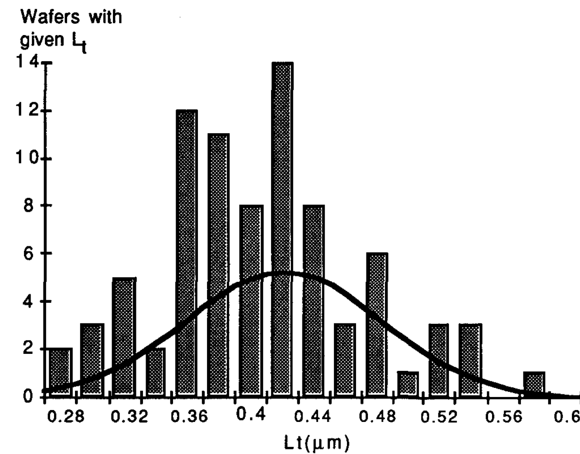

Figure 5: Histogram of wafer mean transfer layer lengths. (Solid line represents a normal distribution with the same mean and standard deviation as this data)

5.3) Acceptable

When a process is behaving in a predictable manner, one can begin to ask the question of whether the observed distribution of the output meets the expectations of the "customer". Ideally the distribution should be centered about the target output value and the entire range of the distribution contained within the spec limits. (Taguchi has argued that all divergences of an output from the target value are, by some measure, inferior goods.) Typically, however, some portion of the distribution lies beyond the spec limits. The question of how much, if any, of the distribution should be allowed to exist beyond the spec limits, requires a consideration of the economics involved. The cost of reworking or scraping out of spec parts must be traded off against the expense of improving the process to narrow the distribution of outputs. Because this economic analysis is not always easy to do, judgement and negotiation with the customer on the necessity of the spec limits may play a non-scientific, but unavoidable and important role in determining acceptability. When the distribution is centered and a 'sufficient' portion of the output distribution lies within the spec limits, the process has achieved the third level of process control, **Acceptable.**

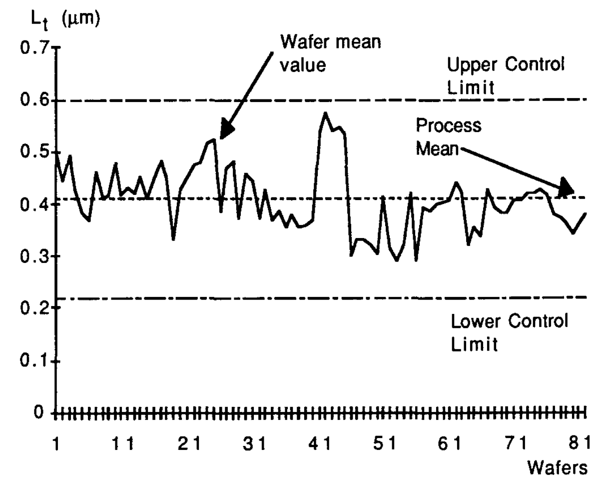

Figure 6: Control chart of wafer mean transfer layer length

Determining acceptability requires knowledge of the expectations for gate length. Orr has shown that the customer desire for gain slope requires a transfer layer length range of 0.35 μm - 0.48 μm with a target of 0.42 μm.[7] The current gate formation process can achieve this specification with a yield of only 65 %.

The acceptability of this yield must take into account two factors:

- the marginal cost of increasing yield, and
- the marginal benefit of this increase.

In practice, neither of these values are straightforward to assess. The marginal cost of increasing yield requires understanding:

- the causes of yield loss,
- how such causes can be reduced or eliminated, and
- the expense involved in undertaking such process improvement projects.

This research, to date, has spent considerable effort to obtain this first piece of information, the causes of yield loss, for one critical parameter on this MMIC-A process. It was found that variability in transfer layer length can be traced to the six process inputs listed in figure 7. Obtaining

this single piece of information required three man-months effort in designing and running experiments to trace the effects of variability in various process inputs on the gain slope parameter under study. Yet once these causes were known, it was found that coming up with ways to reduce or eliminate these sources of yield loss was a straightforward task for experienced engineers. Finally, estimating the expense involved in undertaking these process improvement projects benefited greatly from similar challenges in estimating the costs of research and development. (See figure 7)

The marginal benefit of increased yield is equally opaque. Nominally, the marginal benefit is simply the reduction of rework and scrap costs. However, in a capacity-constrained fab that expects continued growth in demand and must shorten cycle times even as they are growing longer, such an estimate definitively understates the benefit of increased yield. While estimates have been made for this application, considerable improvements can still be made in the accounting and information reporting structures and in the proper application of economic and financial models to this situation. It is clear, however, that the marginal benefit of a process improvement project is an inverse function of the change in variability from undertaking a given project. Ultimately, though, an accurate relationship between reduced variability and increased profitability must be identified.

Once known, the marginal cost can be compared against the marginal benefit to suggest which, if any, process improvement projects merit the investment of resources. One can construct a table, such as figure 7, that summarizes the central data. It is important to remember that other alternatives to these projects are equally valid, prime among these are to replace the process with a new one (e.g., use an E-beam lithography process), or take no action at all.

Cause of process variability	var. now (μm)	**Solution to reduce variability**	new var. (μm)	**Cost of solution ($)**
Develop Control Method	230	improve method	170	40,000
developer exhaustion	213	single wafer develop station	0	170,000
particles on wafer	112	auto-spin system, better mask clean	56	180,000
developer bath temperature	209	buy new bath controller	42	40,000
mask CD accuracy	214	screen masks at vendor	44	35,000
mask CD repeatability	123	screen masks at vendor	51	15,000

Figure 7: Central data needed in deciding whether to invest resources to improve the gate formation process

If resources are invested in some or all of these process improvement projects, a reduction in process variability can be expected (see Figure 8). This change to the process should move the process closer to "acceptable".

Defining what level of yield is acceptable and committing resources to meet this level was found to encompass a broad array of challenges, primarily related to acquiring and applying information that is not commonly available in many manufacturing environments, that make this step central in bringing a process under control.

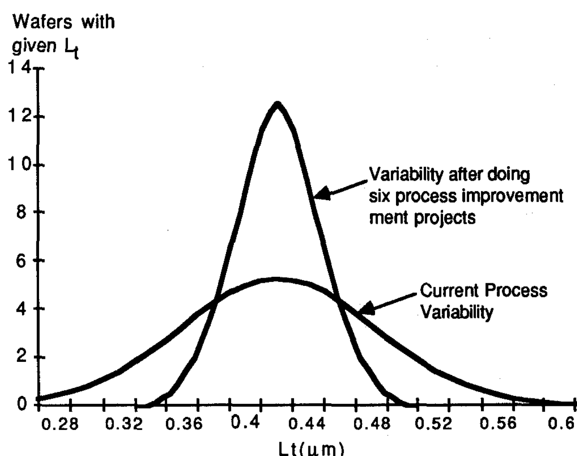

Figure 8: Process variability before and after process improvements

5.4) Recoverable

Having reached the "acceptable" stage, a process is fully under control ... for now. To provide a sense of security that this condition will remain or can be recovered if lost, the process should be fully documented to allow rebuilding the facilities, tooling, software, and operator techniques currently in use. Since many manufacturing processes, particularly semiconductor fabrication, are still dependent on operator technique, it is imperative that documentation be complete and that an active training program exists to pass on that part of technique not captured in documentation. Only when this final requirement is met has the process reached the final level of process control, **Recoverable.**

In exploring what was needed to make this process recoverable, it was found that processing technique varied over time. Consequently, "Unit Process Specifications" that define processing techniques and expected output values are being written for each sub-process involved with gate formation. This also requires writing specifications for auxiliary processes such as daily aligner calibration or aligner bulb replacement. Not surprisingly, these documents sometimes fail to capture all the details of correct processing and/or operators don't always read updated specifications . Consequently, training is used as an ongoing means of keeping processing technique uniform across operators and over time. When the process is found to be acceptable and the training and documentation are current, the gate formation process will finally be considered to have reached the final level of control, "Recoverable".

This does not imply that all die produced will meet customer expectations, but that the current yield is -for now - acceptable and can be expected to remain relatively constant. Finally, this does not excuse anyone from continuously improving the process over time as such improvement may be necessary to maintain competitive manufacturing capability in the future.

A process that has reached the fourth level of control predictably yields an acceptable number of product with an output measurement within the spec limits and can be expected to continue to do so with a low level of risk.

6) Organizational Benefits of MPAR

The MPAR methodology was initially viewed as a means of creating a unified concept among engineers and managers of how to define, pursue and measure process control in a facility with a wide variety of processes. As this methodology gains increasing acceptance and use within MWTD, the resources committed to process improvements and the potential benefits of applying MPAR have increased considerably. While the implications of using the MPAR methodology cannot be fully separated from the effects of other changes underway at MWTD, the costs and benefits discussed here appear to be significantly dependent on the increasing use of MPAR.

The MPAR methodology has been developed and gradually utilized at MWTD over the past two years. As this methodology becomes standard practice, it has sparked several changes in the way the manufacturing and, more recently, the design functions are managed. More than anything else, MPAR has helped to make the pursuit of process control a way of life at MWTD. Process control is becoming a never fully reached goal, quite in keeping with the HP corporate philosophy of Total Quality Control.

The successful use of MPAR is far from complete at MWTD. As was observed in the application of this methodology to the narrow problem of control of gain slope by control of the gate formation process, rigorous application of this process is a costly and major endeavor. The shear number of processes requiring control and the reliance on operator technique in GaAs IC fabrication necessitate that much of the burden of utilizing MPAR be shared by operators. This, however, has required MWTD to re-think what level of operator knowledge is needed in the fab. Consequently, MWTD upgraded all fab operator positions to the highest HP operator skill level and they have undertaken an exhaustive operator training program that includes both the MPAR methodology and the various tools, such as Statistical Process Control, necessary to support MPAR. Along with this skills upgrade, MWTD is empowering line operators with the responsibility to evaluate and, in many cases, fix out of control processes. Furthermore, engineers are being further educated in the use of efficient experimental design. All of this represents a large investment on the part of MWTD.

As was observed in the case of control of gate formation, it is difficult to analytically evaluate the benefits to be expected from such an investment. Current management must have the foresight to realize that high levels of process control can be a primary determinant of competitive advantage now and in the future as has been true in other industries.

While MPAR is being gradually implemented throughout the facility, few processes have yet to reach the recoverable stage; nonetheless, the implementation of MPAR is changing the way manufacturing and design engineering are practiced. Statistical Process Control is becoming a de facto part of these jobs. Manufacturing and design managers both have performance goals that include the level of control reached by their processes. MPAR has become a tool for change at this division.

7) Conclusion

A methodology for guiding the pursuit of process control at Hewlett-Packard's Microwave Technology Division has been presented. The MPAR methodology begins with defining a specific process and the customer's expectations of this process, then increases control over the process through four levels: Measurable, Predictable, Acceptable, and Recoverable. The use of this methodology to control the gate fabrication process for a GaAs traveling-wave amplifier was discussed.

Experience at MWTD suggests that the realization of process control is as much a managerial problem, as it is a technical one. This application suggests that MPAR serves as a useful conceptual guideline for operators, engineers and managers in uniformly applying a wide variety of process control tools previously in only sporadic use at MWTD. While a correct and complete use of MPAR encompasses a broad span of organizational undertakings and requires commitment of considerable resources, it appears to fill a critical gap in current efforts to realize process control.

Acknowledgement

This research was conducted with support from the Leaders For Manufacturing Program at the Massachusetts Institute of Technology (MIT). Leaders For Manufacturing is a partnership between the MIT School of Engineering, the MIT/Sloan School of Management and eleven major US manufacturing firms, among them Hewlett-Packard.

References:

1) Deurtouzos, Michale L., Richard K. Lester, and Robert M. Solow, Made In America, Cambridge, MA., MIT Press, 1989.
2) Phadke, M.S., Quality Engineering Using Robust Design, MIT Draft Copy, June 22, 1988.
3) Bohn, Roger E., Learning By Experimentation in Manufacturing, Working Paper, Harvard Business School, 1987.
4) Elliot, Scott, Designing for Manufacturability is Designing for Process Control, Hewlett Packard, 1989.
5) Moran, Peter W., Sub-Micron Gate Lithography in an MMIC Production Environment, Master's Thesis, Massachusetts Institute of Technology, Cambridge, MA, June 1990.
6) Orr, Jerry, MMIC Parameter Correlations and Process Specifications, Internal HP/MWTD Internal Memorandum, August 12, 1988.
7) Ladbrooke, P.H. MMIC Design: GaAs FETs and HEMTs, Boston: Artech House, 1989.
8) D'Avanzo, D., D.B. Estreich, T.W. Taylor, H. Kondoh, J. Orr, A. Quach, E.H. Wong, R. Yeats, V.K. Makker, and R.A. Fisher, *A Manufacturable, 26 GHz GaAs MMIC Technology*. Proceedings of the GaAs IC Symposium, November 6-9, 1988, pp.317-320.
9) Azzam, W.J. and J.A. del Alamo. *An All-Electrical Floating Gate Transmission-Line Model Technique for Measuring Source Resistance in Heterostructure Field-Effect Transistors.* to be published in IEEE Transactions on Electron Devices, 1990.