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An $In_{0.52}Al_{0.48}As/n^{+}$-$In_xGa_{1-x}As$ Heterostructure Field–Effect Transistor with an In–Enriched Channel [1]

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Abstract

$In_{0.52}Al_{0.48}As/n^{+}$-$In_xGa_{1-x}As$ HFETs have been fabricated with InAs fractions in the channel between 0.53 and 0.7. The enhancement of InAs in the channel results in a drastic improvement in transconductance and peak drain current. However, gate leakage current is increased, device pinchoff is degraded, and the breakdown voltage is reduced. Leakage at the mesa-edge gate overlap is found partially responsible for these effects.

Introduction

$In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ Heterostructure FETs (HFETs) on InP are of great interest for long-wavelength optical and microwave telecommunications. HFETs with a doped-channel and an undoped wide-bandgap insulator, also called MIDFETs (Metal-Insulator Doped-channel FETs,) have a number of benefits over conventional MODFETs [1]: reduced g_m and f_t collapse, higher current drivability, and higher breakdown voltage. These features are particularly desirable for power microwave amplification.

In this work, we investigate the effect of increasing the InAs mole fraction (x) in the $In_xGa_{1-x}As$ channel from that required to lattice match to InP (x=0.53). This work is motivated by the expected improvement in electron transport properties [2] [3] and the enhanced conduction band discontinuity between the channel and insulator [4] as the InAs composition increases

Experimental

Three wafers were grown by MBE with cross sections shown in Fig. 1. The starting material was semi-insulating Fe-doped InP. The InAs mole fractions in the $In_xGa_{1-x}As$ channel and subchannel were 0.53, 0.6, and 0.7. The 100Å subchannel is undoped and the 100Å channel is Si doped. Due to the differing growth rates of the different $In_xGa_{1-x}As$ compositions, the channel doping is slightly different as the Si cell was maintained at a constant temperature. The doping levels thus deduced for the x=0.53, 0.60 and 0.70 devices are 4.0×10^{18}, 4.5×10^{18}, and 5.3×10^{18} cm^{-3} respectively. The $In_{0.52}Al_{0.48}As$ gate insulator and buffer are undoped as is the $In_{0.53}Ga_{0.47}As$ cap. Device fabrication is similar to that used in [1].

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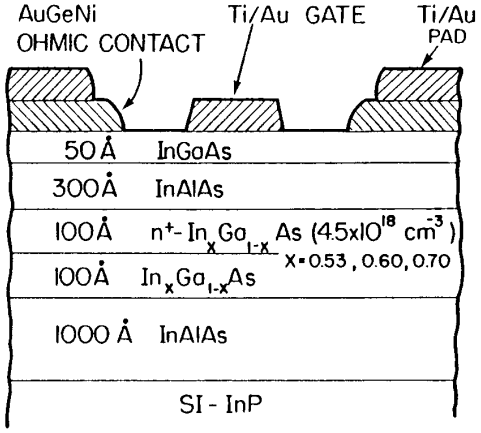

Figure 1: Cross-section of device structure.

I-V characteristics were measured for devices with a nominal gate length of 1 μm and width of 30 μm. The gate diode characteristics were measured with the drain and source shorted. TLM measurements were used to obtain the contact and sheet resistances. The MIDFET source resistance was calculated from these values and used to extract the intrinsic device transconductance. Specially designed gate-diode structures were also measured in order to investigate the gate-channel leakage paths.

Results

Fig. 2 shows the I-V characteristics of representative devices of each of three InAs fractions. The reference device has a clean pinchoff. The pinchoff characteristics degrade with x.

Fig. 3 is a plot of g_m vs. V_{gs} at V_{ds} = 3 V. For devices with x = 0.53, 0.6, and 0.7, the peak g_m's measured (averaged over 10 devices) were 200 ± 22, 250 ± 14, and 296 ± 15 mS/mm respectively. The threshold voltages are -1.04 ± 0.09, -1.28 ± 0.20 and -2.09 ± 0.24 V respectively, which are largely consistent with an increased doping.

Fig. 4 shows the I_d vs. V_{gs} at V_{ds} = 3 V. The peak I_d's measured over 10 devices were 320 ± 42, 424 ± 37 and 656 ± 69 mA/mm respectively, demonstrating the tremendous improvement in electron transport properties as the InAs mole fraction in the channel increases. How-

ever as x increases, the leakage current below threshold increases, preventing the transistor from shutting off.

Fig. 5 is a plot of the contact resistance, R_c, the sheet resistance times source-gate gap, $R_{sh} \times L_{gs}$, and the source resistance, R_s. The gate-source spacing is 2 μm. These values are averages over three TLM structures.

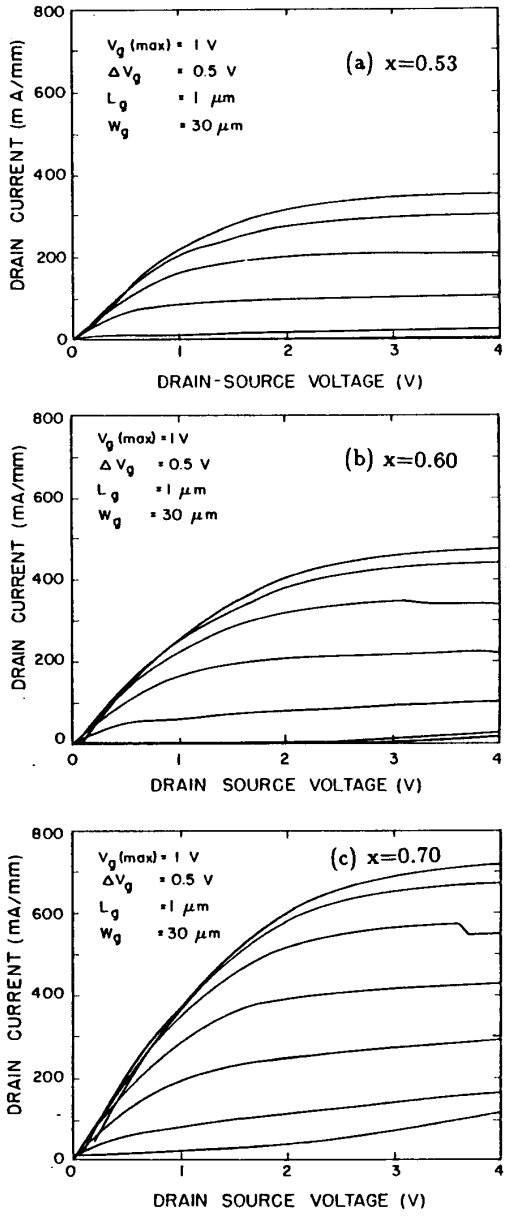

Figure 2: I-V characteristics of devices with (a) x=0.53, (b) x=0.60, and (c) x=0.70.

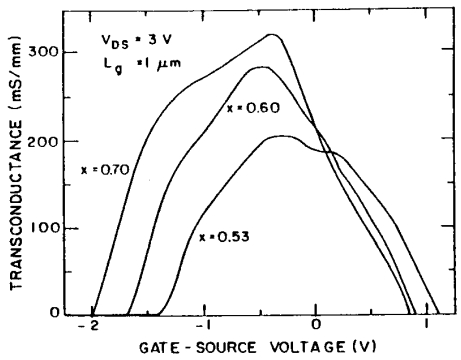

Figure 3: g_m vs. V_{gs} with V_{ds}=3 V vs. x

There is an improvement in all three resistances with x, which again reflects the merits of increased InAs in the channel. The source resistance was used to calculate the intrinsic transconductance, g_{m0}. Both g_m and g_{m0} are plotted vs. x in Fig. 6 and substantially increase with x.

Fig. 7 shows the gate diode characteristics for V_{ds}=0 V. For a clearer presentation, the forward scale has been expanded. The increased InAs fraction in the channel results in larger forward and reverse currents. In forward bias, this is contrary to what is expected from the enhanced ΔE_c between channel and insulator. The values of reverse breakdown voltage are -12.6, -6.7 and -2.6 V for x= 0.53, 0.6 and 0.7 respectively. We have defined breakdown at a reverse gate current of 1 mA, which is about 10% of the peak I_d carried by the reference (x=0.53) device. The increased gate leakage current represents a serious shortcoming of enhanced InAs channels.

Discussion

As shown above, an increase in x results in improved peak I_d, and g_m, and lower contact and sheet resistances. These gains are more than can be explained by the doping increase and are mainly due to enhanced electron transport. However, the tradeoffs are increased gate leakage

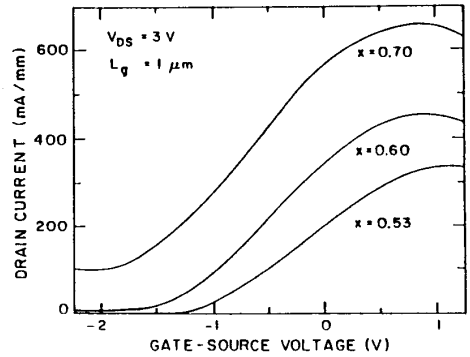

Figure 4: I_d vs. V_{gs} with V_{ds}=3 V vs. x

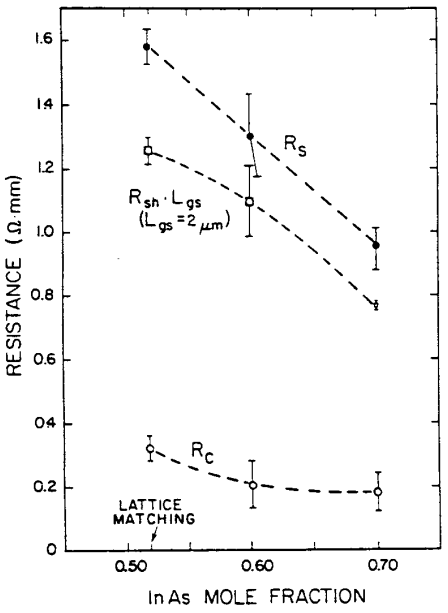

Figure 5: Contact resistance, sheet resistance times gate-source gap, and source resistance and vs. x.

current, a drastically reduced breakdown voltage, and degraded pinchoff. Particularly, as Fig. 7 shows, with increasing x, the forward current increases. As x increases, the conduction band discontinuity between the $In_xGa_{1-x}As$ and the $In_{0.52}Al_{0.48}As$ should increase, going from 0.5 eV at lattice matching to 0.58 eV at x=0.6, and 0.66 eV at x=0.7 [4]. This implies that the forward current should in fact *decrease* with increasing x. We attribute this degradation to direct leakage between the gate and the channel at the edge of the mesa.

Fig. 8 is a perspective drawing of the intrinsic device region. At the mesa edges, where the gate metal goes onto and off the mesa, there is no isolation between the edge of the channel and the gate metal. $In_{0.53}Ga_{0.47}As$ has a Schottky barrier height of 0.2 eV with the metal. As x increases, this gets smaller: $\approx$ 0.1 eV and 0.03 eV at x=0.6 and 0.7 respectively [5]. To investigate this *edge leakage* path, we have fabricated the test structures shown in Fig. 9. These are heterojunction diodes with an inner square gate with area 10,000 μm^2. In one diode there is no gate-edge overlap, i.e. the gate is entirely on the mesa. In the other diode, a 600 μm long edge overlap has been obtained by producing three cuts of the mesa structure underneath the gate. The surrounding metal is the ohmic contact to the channel.

Fig. 10 shows the forward characteristics for these two diodes. Without edge overlap, the forward current decreases with increasing x, as expected from the larger ΔE_c. With edge overlap, however, we see a marked increase in the forward current and a reversal in x dependence. This implies that edge leakage dominates the forward characteristics in the actual FETs (Fig. 7).

Fig. 11 shows the reverse charateristics of these diodes. For x=0.53, the edge overlap marginally contributes to the total reverse current. At x=0.6, the presence of three regions in the reverse characteristics becomes evident: pre-threshold, plateau, and breakdown. The edge overlap influences the reverse current in the pre-threshold region and then saturates at the threshold voltage, i.e. when the channel gets totally depleted underneath the gate. Far into the breakdown region, the reverse characteristics of both the structures with and without edge overlap at x=0.6 do not differ much either. For the x=0.7 structures, edge leakage strongly affects the entire reverse characteristics. For this device, the edge leakage definitely exacerbates the loss of pinchoff. Significant gains could be made in pinchoff quality and reverse breakdown voltage by using some form of isolation that prevents edge gate-mesa overlap

Conclusion

$In_{0.52}Al_{0.48}As$/ $n^+In_xGa_{1-x}As$ MIDFETs have shown markedly improved peak currents and transconductance as the InAs mole fraction in the channel is increased. Devices with L_g=1 μm and x=0.7 display an unprecedented I_d of 656 mA/mm and g_m of 296 mS/mm. As x is increased, however, there is an increase in the gate current, a dramatic decrease in the breakdown voltage, and a degradation of pinch-off. Leakage at the gate-mesa edge overlap is found to be partially responsible for these effects. To achieve the substantial gains in transport that higher InAs fractions offer, better isolation technology is required.

Acknowledgements

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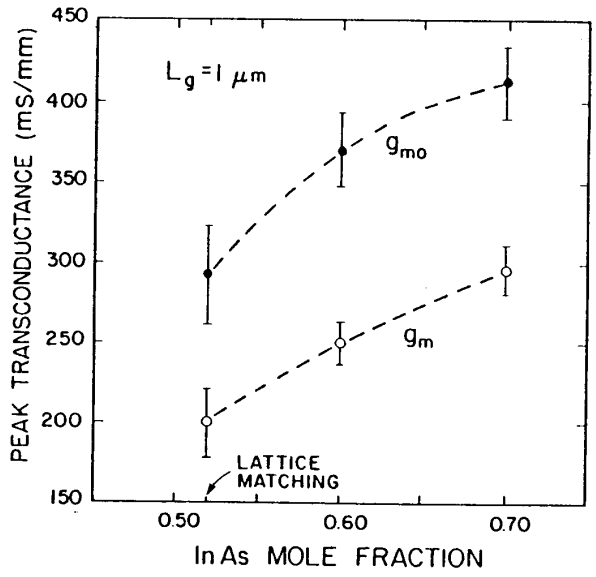

Figure 6: g_m and g_{m0} vs. x.

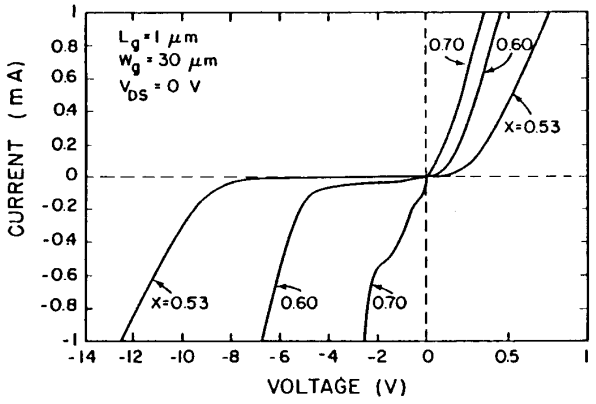

Figure 7: Forward and reverse diode characteristics of 1 μm MIDFETs vs. x.

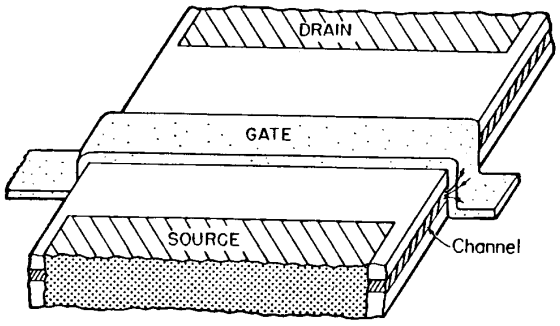

Figure 8: Perspective of the intrinsic device region.

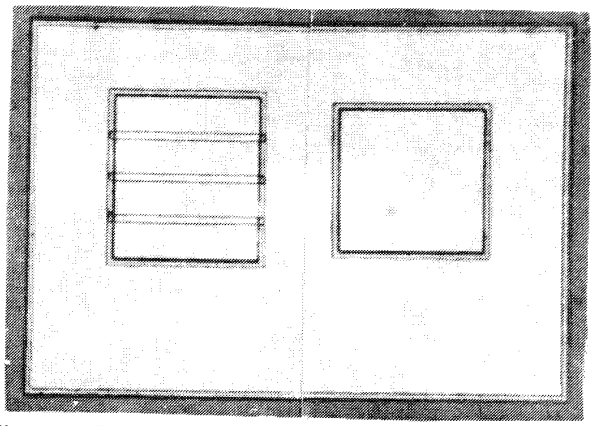

Figure 9: Edge leakage test diodes with 10,000 μm^2 area and leakage edge lengths of 0 and 600 μm.

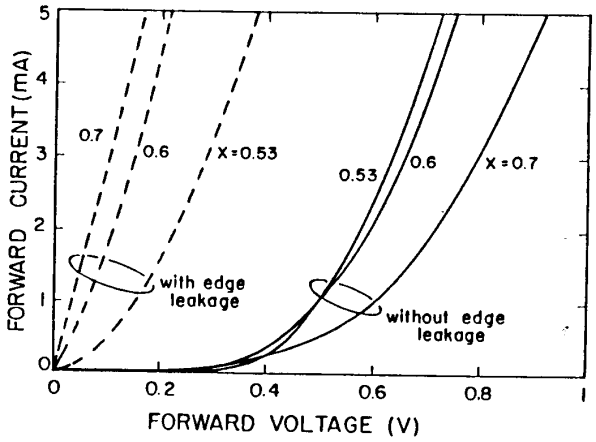

Figure 10: Forward diode characteristics with and without edge overlap.

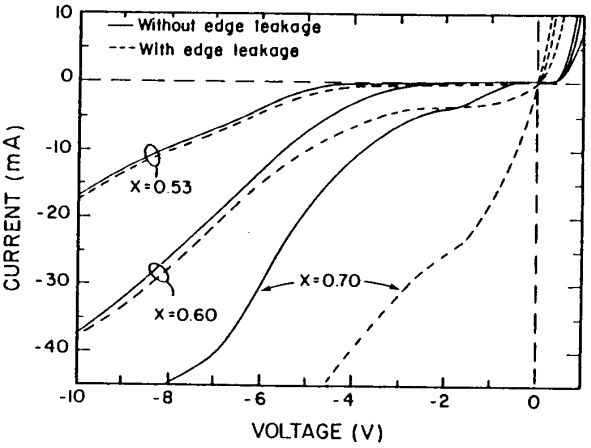

Figure 11: Reverse diode characteristics with and without edge leakage.