A Floating-Gate Transmission-Line Model Technique for Measuring Source Resistance in Heterostructure Field-Effect Transistors

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Abstract—**A new simple technique to measure the parasitic source and drain resistances in heterostructure field-effect transistors (HFET) is presented. The technique makes use of the unavoidable gate leakage current of a typical HFET under bias. Floating-gate measurements with current flowing from the source to the drain are carried out in a set of devices with different gate lengths. Extrapolation to zero gate length unequivocally and simultaneously yields both the source and drain resistances. No special test-pattern structure is required. The technique is demonstrated in $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ metal-insulator doped semiconductor field-effect transistors (MIDFET's).**

I. INTRODUCTION

THE performance of heterostructure field-effect transistors (HFET's) is severely affected by the parasitic source and drain resistances. In particular, the source resistance R_S degrades the intrinsic transconductance of HFET's g_{mo} unless $R_S < 1/g_{mo}$. Reduction of the source resistance is imperative if high-performance devices are to be obtained.

In order to optimize device design by having a low source resistance, its value must first be accurately measured. The most popular technique for the measurement of the source resistance is the transmission-line model (TLM) method [1], [2]. This technique utilizes a special test structure that consists of several metal contact pads located at various distances from each other on top of an n^+-region identical to the one utilized for the source and drain of the FET [1], [2]. This technique yields, simultaneously, the specific transfer resistance (or contact resistance per unit length, the proper figure of merit for contact resistance in lateral devices such as FET's) and the n^+-region sheet resistance. From the measurement of these two parameters and from a knowledge of the dimensions of the FET, one can estimate the source resistance of any device fabricated with the same technology.

There are several problems with this approach. First, a special test structure that consumes valuable chip area is required. Second and most important, the typical TLM test structure is very different from a field-effect transistor structure because the standard TLM does not have a "gate." As a result, the spreading resistance due to current crowding at the source end of the gate cannot be correctly measured by the TLM. In particular, the TLM test structure is very different from a typical recessed-gate HFET, in which an n^+-cap is recessed before gate metal deposition [3]. This HFET structure is under intense research because it yields devices with very small source resistance. In fact, the highest microwave performance devices to date use this recessed-gate approach [4]. For this very important class of devices, the TLM completely fails to measure the source resistance.

An improved version of the TLM recently has been proposed in an effort to eliminate this severe limitation of the conventional TLM. The gated TLM (GTLM) introduces a gate between the contact pads of the otherwise standard TLM [5]. This structure correctly takes into account the additional resistance due to current crowding that exists at the gate edge of a FET. However, because the method measures the total resistance from the source to the drain, symmetric structures in which the gate is exactly positioned in the middle of the source-to-drain gap are required. Such is seldom the result of a normal HFET fabrication process.

A number of techniques for evaluating the source resistance of metal-semiconductor field-effect transistors (MESFET's) through measurements on a single device have been proposed [6]–[14]. Unfortunately, most of these techniques require assumptions that do not apply to typical HFET's. Several authors [7]–[9] based their techniques on Hower and Bechtel's [6] in which the total source-to-drain resistance is measured. From this measurement, the sum of the source and drain resistances can be obtained if the behavior of the sheet resistance as a function of gate voltage is known. This is rarely known in the case of HFET's. Techniques based on the "end" resistance [9]–[15] require assumptions of the behavior of the gate current as a function of the gate voltage. Gate current models that are utilized in MESFET's [9]–[14] are unlikely to be correct for HFET's [15].

In this paper we propose and demonstrate a new simple measurement technique that we denote the "floating-gate transmission line model" (FGTLM) technique. The

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FGTLM utilizes actual HFET structures of various gate lengths. There is no need for a special test structure. The method is based on the fact that unavoidable gate leakage current flows in an HFET under bias. With current flowing from the source to the drain and the gate floating, the gate-to-source and the gate-to-drain voltages are measured in devices with different gate lengths. Extrapolation to zero gate length yields simultaneously and unequivocally both the source and drain resistances.

We demonstrate the method in $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ metal-insulator-doped semiconductor field-effect transistors (MIDFET's), a new device structure very promising for high-frequency large-signal microwave applications [16]–[18].

II. Theory

The theory that will be described in this paper applies to any HFET, be it a modulation-doped FET (MODFET), MIDFET, etc., and to nonheterostructure FET's with some gate leakage, such as MESFET's or junction FET's (JFET's).

The geometry of the problem is shown in Fig. 1, which represents a generic HFET with either a two-dimensional electron gas or a doped channel, biased in the linear mode of operation. The intrinsic device shows a wide-bandgap material that is intended to isolate the metal gate from the channel. In a MESFET, the gate-to-channel isolation is provided by the depletion region associated with the Schottky junction. In a JFET, on the other hand, the depletion region of the p-n junction fulfills the same role. Common to all of these devices is the fact that the isolation is not perfect and a small leakage current flows between the channel and the gate at room temperature for any significant gate bias.

In the linear mode of operation, in which a very small electric field exists along the channel, the proper equivalent circuit representation of the intrinsic HFET is a network of series resistances and parallel conductances, as schematically shown in Fig. 1. The series resistances characterize the resistance of the channel, while the parallel conductances represent the leakage between the channel and the gate. This network, which is associated with the intrinsic device, is in series with the parasitic source and drain resistances R_S and R_D that connect the intrinsic device to the outside world. These are the resistances that we wish to determine. Even though the source and drain n^+-regions are fabricated simultaneously, the respective distances between the source and gate, and the drain and gate, are in general different, and so are R_S and R_D.

The distributed resistance network associated with the intrinsic device can be analyzed using the transmission line model (TLM), as is commonly used in treating ohmic contacts [1]. In Fig. 1, R represents the resistance per unit length of the channel (in units of ohms per micrometer) and G represents the gate-to-channel conductance per unit length of channel (in units of reciprocal ohms per micrometer). In the linear regime, with small biases applied

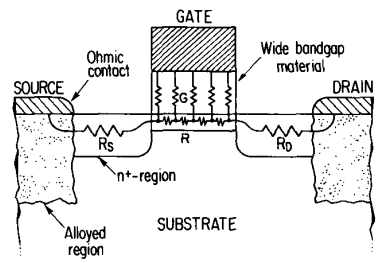

Fig. 1. Diagram of HFET showing the distributive resistance network associated with the intrinsic device.

to drain and gate, R and G can be considered independent of the x position in the channel (the discussion section explores the limits of this approximation). In this case, the complex resistive network can be represented by a simple inverted T-type resistive circuit. Symmetry implies that both wings of the inverted T must be identical. We denote this value by $\frac{1}{2}R_{ch}$, or half the "channel resistance." We also denote the column of the inverted-T resistive circuit by R_g, or "gate barrier resistance." The complete equivalent circuit model for the HFET in the linear mode of operation is shown in Fig. 2, which also includes R_S and R_D.

In order to express R_{ch} and R_g as a function of R, G, and L_G (with L_G being the FET gate length), we must solve the TLM shown in Fig. 1. This is carried out in the Appendix. R_{ch} and R_g are found to be (see (A11) and (A14) in the Appendix)

$$R_{ch} = 2Z_0 \frac{\cosh(\gamma L_G) - 1}{\sinh(\gamma L_G)} \tag{1}$$

$$R_g = \frac{Z_0}{\sinh(\gamma L_G)} \tag{2}$$

where Z_0 is the characteristic impedance (in ohms)

$$Z_0 = \sqrt{\frac{R}{G}} \tag{3}$$

and γ is the propagation constant (in reciprocal micrometers)

$$\gamma = \sqrt{RG}. \tag{4}$$

As (1) and (2) indicate, in general, R_{ch} and R_g depend on both the channel resistance R and the gate conductance G. In the case of R_{ch}, this is because the metal gate partially shorts the channel through G and, therefore, contributes to conduction between the source and the drain. In the case of R_g, this is because the channel resistance partially appears in series with the channel conductance. A plot of R_{ch} and R_g, normalized with Z_0, is shown in Fig. 3.

It is of interest to explore the limit values of R_{ch} and R_g. For short channel lengths or small gate conductance, $\gamma L_G \ll 1$ implies

$$R_{ch} \simeq RL_G, \qquad (\gamma L_G \ll 1) \tag{5}$$

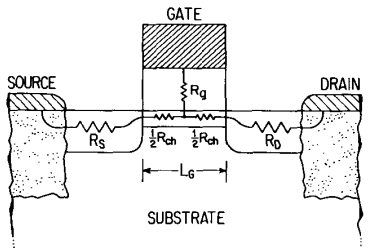

Fig. 2. Diagram of HFET showing inverted T-type resistive network equivalent to the distributive network associated with the intrinsic device, as indicated in Fig. 1.

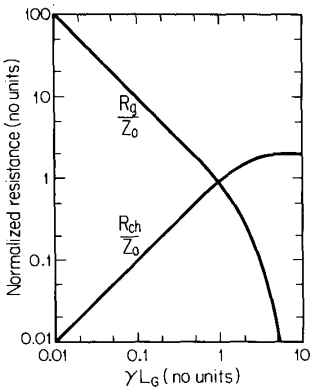

Fig. 3. Plot of gate and channel resistance, normalized by Z_0, as a function of the dimensionless parameter γL_G.

$$R_g \simeq \frac{1}{GL_G}, \qquad (\gamma L_G \ll 1). \tag{6}$$

In this situation, R_g is solely determined by the gate conductance. R_{ch}, on the other hand, is entirely given by the intrinsic resistance of the channel, i.e., the parallel conduction through the gate from the source to the drain is negligible. As a result, as $L_G \to 0$, $R_{ch} \to 0$ (see Fig. 3). This behavior of R_{ch} for very small gate lengths will be used in our measurement procedure, as described below.

For large gate barrier conductance or long gate lengths, $\gamma L_G \gg 1$ implies

$$R_{ch} \simeq 2Z_0, \qquad (\gamma L_G \gg 1) \tag{7}$$

$$R_g \simeq 2Z_0 e^{-\gamma L_G}, \qquad (\gamma L_G \gg 1). \tag{8}$$

In this case, the gate barrier resistance is made negligibly small, and the gate metal effectively shorts the channel. This results in a channel resistance of $2Z_0$, independent of gate length, where a Z_0 arises from the resistance of the channel to the gate at each of the two ends of the gate. The behavior of R_{ch} and R_g in this limit is clearly seen in Fig. 3.

Using the equivalent inverted-T model for the intrinsic HFET shown in Fig. 2, we can now have three possible measuring configurations. They are schematically summarized in Fig. 4.

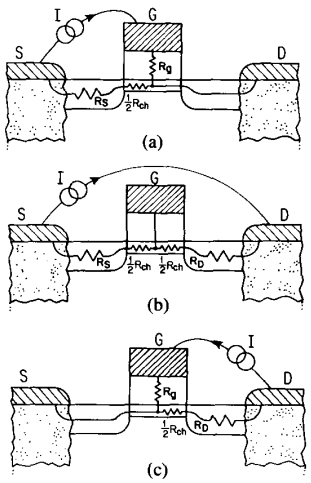

Fig. 4. Measurement configurations utilized in this work: (a) floating drain, (b) floating gate, (c) floating source.

A. Floating-Drain Configuration

As shown in Fig. 4(a), in this configuration current is injected from the gate to the source and the drain is left floating. In this case, there is no current through R_D or the $\frac{1}{2}R_{ch}$ on the drain-side half of the channel. The resistances that we measure on each pair of terminals (measured voltage divided by injected gate-to-source current) are

$$R_{gs}(fd) = R_S + \tfrac{1}{2}R_{ch} + R_g \tag{9}$$

$$R_{gd}(fd) = R_g \tag{10}$$

$$R_{ds}(fd) = R_S + \tfrac{1}{2}R_{ch} \tag{11}$$

where the fd notation in brackets indicates a floating drain.

B. Floating-Gate Configuration

As Fig. 4(b) shows, current is now injected from the drain to the source and the gate is left floating. There is no current through R_g, and, therefore, the gate samples the voltage in the middle of the intrinsic channel. The three measured resistances are

$$R_{gs}(fg) = R_S + \tfrac{1}{2}R_{ch} \tag{12}$$

$$R_{gd}(fg) = R_D + \tfrac{1}{2}R_{ch} \tag{13}$$

$$R_{ds}(fg) = R_S + R_D + R_{ch}. \tag{14}$$

C. Floating-Source Configuration

Now the situation is as shown in Fig. 4(c) in which current is injected from the gate to the drain and the source is left floating. The three measured resistances are:

$$R_{gs}(fs) = R_g \tag{15}$$

$$R_{gd}(fs) = R_D + \tfrac{1}{2}R_{ch} + R_g \tag{16}$$

$$R_{ds}(fs) = R_D + \tfrac{1}{2}R_{ch}. \tag{17}$$

The nine measurements summarized above are not all independent of each other. In fact, since this is a linear circuit with three terminals, at most three measurements can be performed in an independent manner. As a result, at most, on a given HFET, we can determine R_g, $R_s + \frac{1}{2}R_{ch}$, and $R_D + \frac{1}{2}R_{ch}$. The extraction of R_S and R_D, therefore, cannot be carried out from one single device.

An interesting situation appears when we have several devices that are identical to each other except for the gate length L_G. If γ is such that all of them are operating in the $\gamma L_G << 1$ regime, using (5) we obtain from the above equations

$$R_{gs}(fg) = R_{ds}(fd) \simeq R_S + \tfrac{1}{2}RL_G \quad (18)$$

$$R_{gd}(fg) = R_{ds}(fs) \simeq R_D + \tfrac{1}{2}RL_G \quad (19)$$

$$R_{ds}(fg) = R_S + R_D + RL_G. \quad (20)$$

Therefore, if we measure $R_{gs}(fg)$ and $R_{gd}(fg)$ for all the devices and plot the data as a function of L_G on a linear scale, the data points should fall on straight lines. The extrapolation of these straight lines to $L_G = 0$ gives, respectively, R_S and R_D. The slope of both lines is $\frac{1}{2}R$. These measurements can be confirmed by additionally measuring $R_{ds}(fd)$ and $R_{ds}(fs)$, which should yield identical results for both $R_{gs}(fg)$ and $R_{gd}(fg)$ respectively.

Furthermore, a similar measurement of $R_{ds}(fg)$ as a function of L_G yields $R_S + R_D$ from the intercept and R from the slope. This serves as a check for the internal consistency of the measurement technique. Out of all the possible measurements, those that utilize a floating gate are the more straightforward and are sufficient to obtain R_S and R_D. Because of this, we call this technique a floating-gate TLM or FGTLM.

Additionally, one must check the validity of the linear regime approximation, i.e., the measured resistance must be independent of the magnitude and sign of the injected current. This is shown in the next section to pose no problem for practical devices.

III. Experimental

The measurement technique proposed above has been demonstrated in $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ metal-insulator-doped semiconductor field-effect transistors (MIDFET's) with a thin and heavily doped channel. These devices, first reported in this semiconductor system in [16], appear very promising for ultrahigh-frequency large-signal microwave operation.

The cross section of the device used in this work is shown in Fig. 5. In summary, this device consists of an undoped $In_{0.52}Al_{0.48}As$ buffer layer, an undoped $In_{0.53}Ga_{0.47}As$ smoothing layer, a thin and heavily doped $In_{0.53}Ga_{0.47}As$ active channel, an undoped $In_{0.52}Al_{0.48}As$ gate barrier, and a thin $In_{0.53}Ga_{0.47}As$ undoped cap. All the layers are grown by molecular-beam epitaxy on a semi-insulating InP substrate. The ohmic contacts were made with alloyed AuGeNi, and the gate metal is Ti/Au

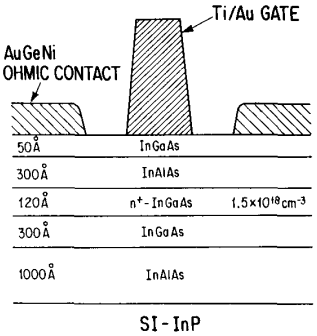

Fig. 5. Cross section of $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFET utilized in experiments.

defined by lift-off. The details of fabrication of this particular device have been reported in [18].

A 1.5 μm × 200 μm gate dimension FET displayed an extrinsic transconductance of 164 mS/mm and a current-gain cutoff frequency of 15.2 GHz. The I-V characteristics of this device are shown in Fig. 6. The threshold voltage was −1.7 V [18]. These results are very close to those obtained with conventional MODFET's of the same gate dimensions fabricated on the $In_{0.52}Al_{0.48}As/In_{0.53}Ga_{0.47}As$ system [19].

Integrated on the same wafer are test HFET's with a gate width of 28 μm and variable gate lengths of 1, 1.5, 2, 3, 5, 10, and 50 μm (as-drawn dimensions). These devices were used for the FGTLM measurements. Additionally, located next to the HFET's, there is a conventional TLM test pattern 110 μm wide with nominal contact spacings of 2, 3, 5, 10, 20, and 30 μm. All of the actual dimensions of the FET's and TLM were measured by a scanning electron microscope (SEM) with a precision of 0.1 μm.

The device studied here (see Fig. 5) is a depletion-mode device, and therefore, there is no need to fabricate additional n^+-regions for the source and the drain. This feature provides a convenient verification of the experimental procedure proposed in this paper since the sheet resistance of the source and the drain n^+-regions (measured by the TLM) should be identical to the sheet resistance of the intrinsic channel (measured by the FGTLM). This, in fact, is what is experimentally found, as described below.

Fig. 7 shows measurements of $R_{gs}(fg)$ as a function of drain-to-source voltage V_{DS} for a set of devices with varying gate lengths. The parameter on the graphs is the actual gate length measured by SEM. Around $V_{DS} = 0$, the resistance measurement becomes very inaccurate because the voltage being measured is very small. This has been indicated in Fig. 7 by a broken line. All resistances were measured using the Kelvin technique to avoid contact probe resistance. For example, for $R_{gs}(fg)$, current was injected by means of two probes from the drain to the source, and the gate-to-source voltage was measured by means of two other probes.

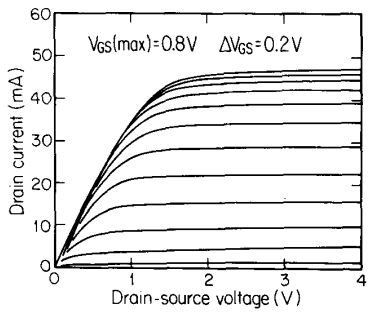

Fig. 6. I-V characteristics of 1.5 μm × 200 μm $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ MIDFET.

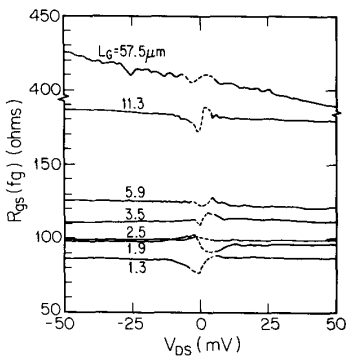

Fig. 7. Measurements of $R_{gs}(fg)$ as a function of drain-to-source voltage for FET's of various gate lengths (measured by SEM).

As Fig. 7 indicates, for short gate lengths, the measured resistance is effectively independent of the magnitude and sign of the injected current (i.e., less than 5 percent from -250 to $+250$ mV in the $L_G = 11.3$ μm device), as a correct measuring procedure requires. For the longest gate device ($L_G = 57.5$ μm), however, the resistance is found to decrease significantly with forward voltages (about 9 percent in the range indicated in Fig. 7). This is attributed to a small spacial variation of G along the channel, as discussed in Section IV of this paper.

Fig. 8 plots $R_{gs}(fg)$, $R_{ds}(fd)$, and $R_{ds}(fg)$ measured on a set of devices as a function of *actual* gate length. For the sake of clarity, we have left out the measurements of $R_{gd}(fg)$ and $R_{ds}(fs)$ that also were performed. In the range of gate lengths shown in this graph, all of the resistances are found to depend linearly on gate length, as (18)–(20) predict. The data points of the $L_G = 57.5$ μm device (not shown in Fig. 8) do not fall on this straight line, as will be discussed below. Straight lines were fitted to the data by the least squares technique. The extrapolation of these straight lines to $L_G = 0$ yields $R_S = 76.7$ Ω (from $R_{gs}(fg)$ and $R_{ds}(fd)$, $R_D = 78.0$ Ω (from $R_{gd}(fg)$ and $R_{ds}(fs)$, not shown in Fig. 8), and $R_S + R_D = 154.4$ Ω (from $R_{ds}(fg)$). Note the excellent internal consistency of these three results.

The results of Fig. 8 confirm additional predictions of the theory presented in Section II. To within experimental error, $R_{gs}(fg)$ equals $R_{ds}(fd)$ as (18) requires. The same

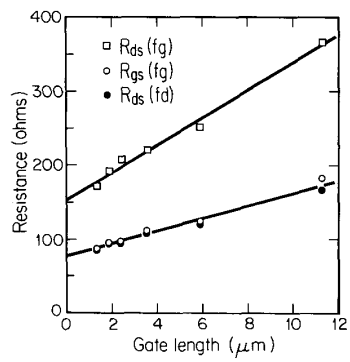

Fig. 8. Plot of $R_{ds}(fg)$, $R_{gs}(fg)$, and $R_{ds}(fd)$ as a function of device gate length. The intersection of the line fitted to the measurements of $R_{gs}(fg)$ and $R_{ds}(fd)$ to the y axis at $L_G = 0$ gives $R_S = 76.7$ Ω. Similarly, $R_S + R_D = 154.4$ Ω is extracted from the measurements of $R_{ds}(fg)$.

equality was found between $R_{gd}(fg)$ and $R_{ds}(fs)$. Additionally, the slope of $R_{ds}(fg)$ (18.5 Ω/μm) is about double the slope of $R_{gs}(fg)$ (8.6 Ω/μm) and of $R_{gd}(fg)$ (9.3 Ω/μm, not shown), as (18)–(20) predict.

For comparison, measurements on the TLM pattern adjoining the devices were carried out. As is well known, the TLM yields a value for the contact resistance (specific transfer resistance) R_c and the sheet resistance of the n^+-region. The values extracted for these two parameters from the TLM (with gap spacing measured by SEM) were, respectively, 0.99 Ω · mm and 505 Ω/□. As expected, this last value is in excellent agreement with the sheet resistance of the n^+-channel, measured underneath the gate, by the FGTLM.

Taking into consideration the gate-to-source distance (measured by SEM as 1.55 ± 0.09 μm), the TLM measurements predict a source resistance of 63 Ω. This value is 18 percent smaller than the actual source resistance measured by the FGTLM. Similarly, a discrepancy of about 11 percent is found between the value predicted by the TLM and the one actually measured by the FGTLM in the case of the drain resistance.

In many measurements that we have performed on this and on other wafers, this significant difference between the actual terminal resistance measured by the FGTLM and the calculation based on the TLM has been found to be systematic. That is, the FGTLM always measures a higher value than what the TLM predicts. This was expected because, as argued in the introduction, the TLM does not measure the resistance associated with the two-dimensional flow of electrons at the source side of the gate. This is very relevant to device design because the TLM measurements *underestimate* the intrinsic transconductance of a device.

Since R_S and R_D have already been measured, we can solve in (12)–(14) for the channel resistance R_{ch} for every device. Fig. 9 plots, as a function of L_G, the value extracted for R_{ch} from the measurements of $R_{ds}(fg)$, $R_{gd}(fg)$, and $R_{gs}(fg)$. The agreement among the three sets of data is rather good. The line drawn in Fig. 9 is a theoretical fit to the data using (1). The fitting parameters

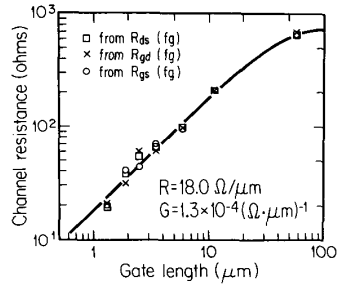

Fig. 9. Channel resistance R_{ch} extracted from the floating-gate measurements. The solid line indicates the theoretical fit obtained with $R = 18.0\ \Omega/\mu m$ and $G = 1.3 \times 10^{-4}\ (\Omega \cdot \mu m)^{-1}$.

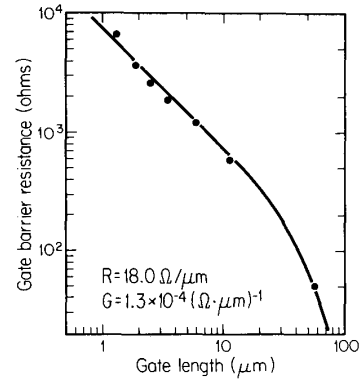

Fig. 10. Gate barrier resistance R_g extracted from the measurement of $R_{gd}(fd)$ as a function of L_G. The solid line is a fit to the data points using (2) and the parameters indicated in the graph.

that have provided such a close fit are $R = 18.0\ \Omega/\mu m$, and $G = 1.3 \times 10^{-4}\ (\Omega \cdot \mu m)^{-1}$. It is worth noting that the $L_G = 57.5\ \mu m$ sample is very close to the $\gamma L_G >> 1$ regime, while all of the other ones are in the $\gamma L_G << 1$ regime. As a result, both R and G have been accurately determined (within about 15 percent). The value of R of $18.0\ \Omega/\mu m$ translates, into a channel sheet resistance of $504\ \Omega/\square$. The corresponding values for Z_0, and γ are, respectively, $372\ \Omega$ and $0.048\ \mu m^{-1}$.

Further confirmation of the correctness and internal consistency of the FGTLM technique comes from a measurement of the gate barrier resistance R_g. As was presented in Section II, R_g can be directly measured from $R_{gd}(fd)$ (see (10)). The result is plotted as a function of L_G in Fig. 10. The solid line in Fig. 10 represents a plot of R_g from (2) using the same R and G values as in the fit shown in Fig. 9. This excellent agreement provides confidence in the soundness of the theory underlying the FGTLM.

IV. Discussion

In order for the TLM analysis of the intrinsic device to be correct, a key requirement is that the vertical resistance of the channel has to be much smaller than the contact interface resistance with the gate [1]. In other words, the inverse of the propagation constant (the characteristic length of the problem) must be much bigger than the thickness of the channel. More specifically, the calculations of Berger [1], confirmed by Woelk *et al.* [20], require that

$$\eta = \frac{1}{\gamma^2 h^2} >> 0.19$$

where h is the channel thickness. Based on the measured $\gamma = 0.048\ \mu m^{-1}$ and the designed $h = 0.012\ \mu m$, $\eta \simeq 3 \times 10^6$, which makes the TLM approximation valid [1], [20].

The TLM is used under the assumption that R and G in the intrinsic device are independent of position. As discussed above, the floating gate samples the potential at the middle of the intrinsic channel. This implies that, for positive drain–source bias, the gate is, respectively, forward and reverse biased with respect to the source and drain of the channel. As a result, the sheet resistance of the channel increases and the gate conductance decreases as one goes from the source to the drain. For short channels, only the variation of R is of relevance (see (5)). For long channels, the variation of G is also important (see (7)). If the maximum voltage across the device (V_{DS} in Fig. 7) is kept comparable to kT/q, the change of R along the channel should be negligible.

For long devices in which the value of G plays a role, an impact from the change of G along the channel cannot be avoided because of the expected exponential dependence of G on the gate-to-channel voltage. Specifically, in the measurement of $R_{gs}(fg)$ in Fig. 7, as G increases with forward voltage on the source side of the intrinsic channel, Z_0 decreases and R_{ch} also decreases (for positive V_{DS}). The opposite occurs for negative V_{DS}. This is in agreement with the experimental observations of Fig. 7 for the $L_G = 57.5\ \mu m$ device.

The FGTLM technique requires the device to be ON with the gate floating. Because of this constraint, it can only be used on *depletion-mode* FET's. Since measurements are taken directly on actual FET structures, however, this technique can be applied to recessed-gate FET's. The conventional TLM completely fails to determine R_S in such devices.

V. Conclusion

A new simple technique to measure the source resistance in HFET's, called the floating-gate transmission line model (FGTLM), has been developed. The technique is based on measurements taken on actual device structures of different gate lengths, with no need for dedicated test patterns. The technique is applied to and the predictions of the theoretical model are confirmed in $In_{0.52}Al_{0.48}As/n^+$-$In_{0.53}Ga_{0.47}As$ HFET's. For these devices, the conventional TLM systematically underestimates R_S and R_D by 10–20 percent.

Appendix

Fig. 11 represents the TLM equivalent resistive network of the intrinsic portion of an HFET. $i(x)$ and $v(x)$

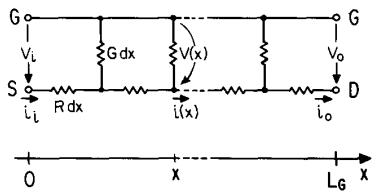

Fig. 11. Definition of variables in the TLM equivalent circuit model of the intrinsic device.

represent, respectively, the current and voltage as a function of x in the TLM. They are easily found to be [1]

$$v(x) = Ae^{\gamma x} + Be^{-\gamma x} \tag{A1}$$

$$i(x) = \frac{1}{Z_0}(Be^{-\gamma x} - Ae^{\gamma x}) \tag{A2}$$

where

$$Z_0 = \sqrt{\frac{R}{G}} \tag{A3}$$

is the *characteristic impedance* and

$$\gamma = \sqrt{RG} \tag{A4}$$

is the *propagation constant*. A and B are arbitrary constants that depend on the boundary conditions of the problem.

The expressions for the end voltages and currents are

$$v_i = v(x = 0) = A + B \tag{A5}$$

$$v_0 = v(x = L_G) = Ae^{\gamma L_G} + Be^{-\gamma L_G} \tag{A6}$$

$$i_i = i(x = 0) = \frac{1}{Z_0}(B - A) \tag{A7}$$

$$i_0 = i(x = L_G) = \frac{1}{Z_0}(Be^{-\gamma L_G} - Ae^{\gamma L_G}). \tag{A8}$$

R_{ch} can easily be determined by letting the gate float, or $i_i = i_0$

$$R_{ch} = \left.\frac{v_i - v_0}{i_i}\right|_{i_i = i_0}. \tag{A9}$$

From (A7) and (A8), this boundary condition $i_i = i_0$ implies

$$B = A\frac{1 - e^{\gamma L_G}}{1 - e^{-\gamma L_G}}. \tag{A10}$$

Inserting (A5), (A6), and (A10) into (A9) R_{ch} is easily found to be

$$R_{ch} = 2Z_0\frac{\cosh(\gamma L_G) - 1}{\sinh(\gamma L_G)}. \tag{A11}$$

The gate barrier resistance is determined as (see Fig. 11)

$$R_g = \left.\frac{v_0}{i_i}\right|_{i_0 = 0} \tag{A12}$$

because, in this case, $i_0 = 0$, and all the current is forced to go from the source to the gate. This boundary condition, from (A8), implies

$$B = Ae^{2\gamma L_G}. \tag{A13}$$

Inserting (A6), (A7), and (A13) into (A12), we obtain

$$R_g = \frac{Z_0}{\sinh(\gamma L_G)}. \tag{A14}$$

Similarly, and for completeness, it is easy to verify that

$$\left.\frac{v_i}{i_i}\right|_{i_0 = 0} = R_g + \frac{1}{2}R_{ch} \tag{A15}$$

$$\left.\frac{v_i - v_0}{i_i}\right|_{i_0 = 0} = \left.\frac{v_i}{i_i}\right|_{i_i = i_0} = \frac{1}{2}R_{ch} \tag{A16}$$

as the simple inverted-T model of Fig. 2 requires.

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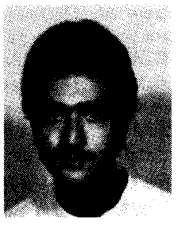

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