Wide-bandgap materials and power applications

Efforts continue to realize the potential of wide-bandgap semiconductors for power switching applications. Researchers presented a number of papers at December's International Electron Devices Meeting (IEDM) in Washington DC. Mike Cooke reports.

Materials with high critical breakdown fields and high electron saturation velocities should lead to more efficient and compact power handling systems. Wideband materials such as silicon carbide (SiC) and gallium nitride (GaN) have such properties, but moving from principles to practice is not straightforward.

For GaN-based devices, one of the leading obstacles has been the fact that characteristics achieved in direct current (DC) measurements are not maintained when switching speed increases. In particular, the current 'collapses', indicating that the dynamic resistance of the on-state has increased.

SiC material quality and more difficult processing are some of the impediments on the alternative branch towards efficient, compact power handling. Some of the materials problems such as 'micropipe' defects have been tackled in particular cases. Manufacturing difficulties include the hardness of the material and the high temperature at which processing has to be carried out – ~1600°C as opposed to ~1000°C for GaN.

Here we look at some of the presentations at IEDM that touched on these issues and others. Next issue, we will cover IEDM progress reports toward combining III-V transistors with CMOS.

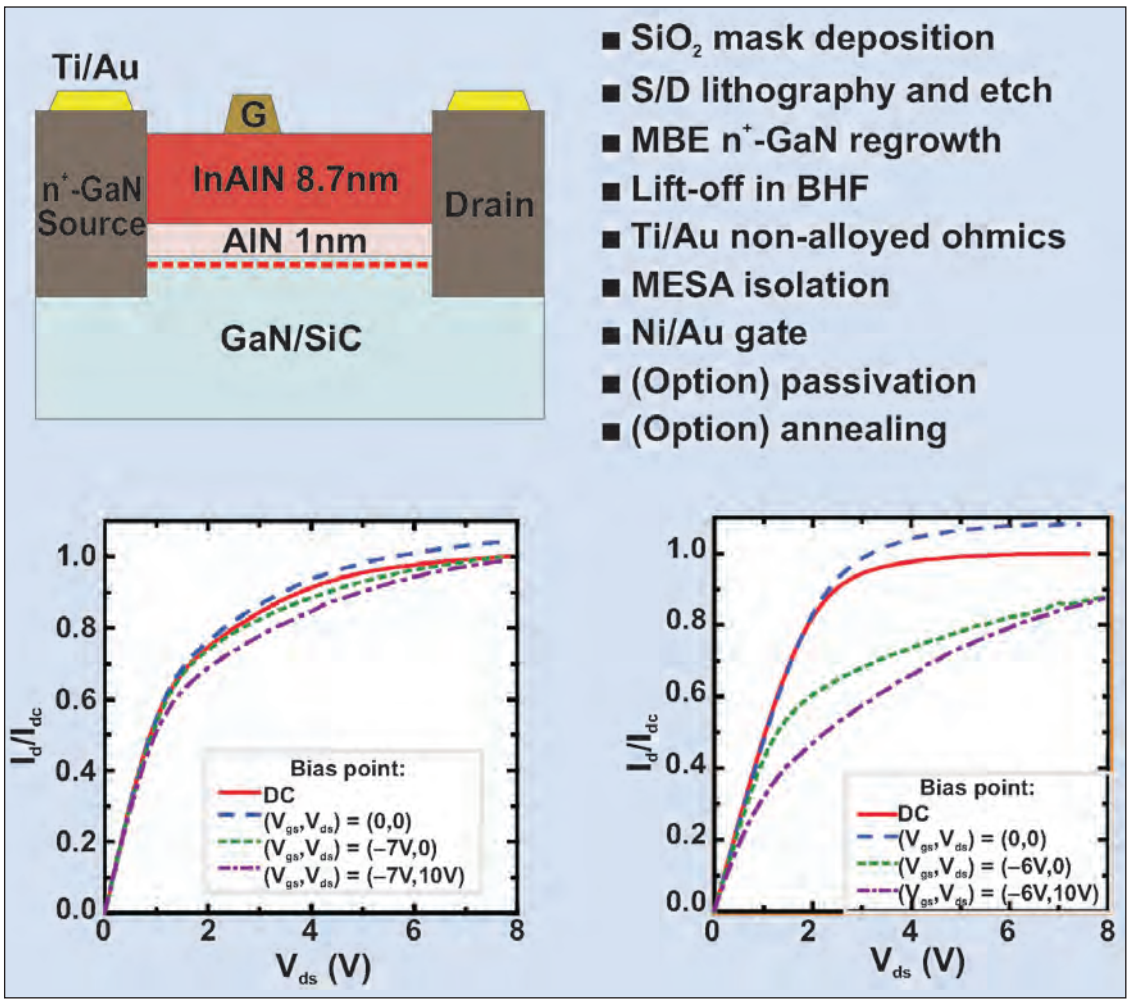

Figure 1. UND / IQE InAlN-based HEMTs with non-alloyed re-grown contacts and no passivation: Device schematics (top left) and process flow (top right). Pulsed current-voltage (I–V) characteristics using 300ns pulses and duty cycle of 0.5ms, and 0V gate potential, without annealing (bottom left) and with annealing at 650°C for 30 seconds in nitrogen (bottom right).

Dispersion / current collapse

University of Notre Dame and IQE have been studying how to obtain 'dispersion-free' operation in indium aluminium nitride (InAlN) barrier high-electron-mobility transistors (HEMTs) [Ronghua Wang et al, session 28.6]. Dispersion away from DC performance when operated in pulsed switch-mode is often attributed to surface states near the gate that trap and release elec-

trons. 'Current collapse' is another term for such behavior in gallium nitride (GaN) HEMTs.

Although passivation schemes have been developed to avoid surface states, it is important that such efforts do not negatively impact carrier densities in the channel.

Dielectric deposition is one technique to reduce the surface states that produce dispersion. However, dielectrics can also extend the effective length of the gate, creating a 'virtual gate', along with introducing parasitic capacitance that increases delays — both effects reducing performance.

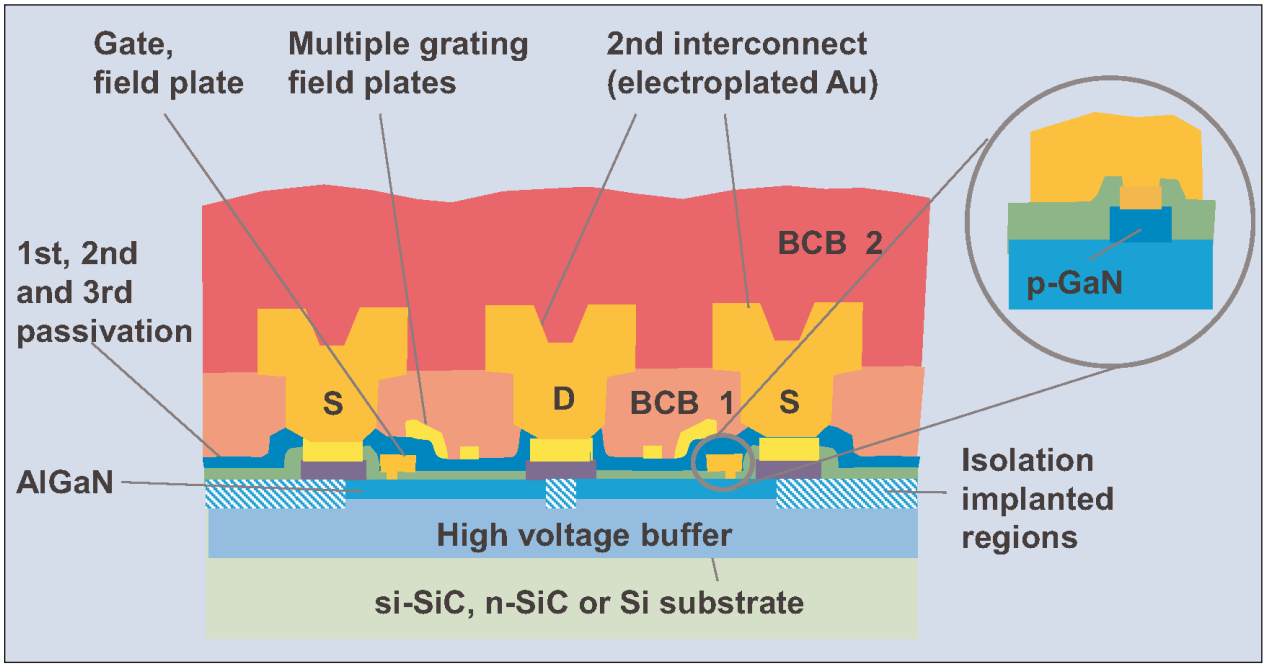

Figure 2. High-voltage switching GaN technology developed at Ferdinand-Braun-Institut: normally-on and normally-off devices are fabricated in same process with the exception of the gate module. Inset details related to p-type GaN gate which renders devices normally-off.

UND/IQE studied devices based on epitaxial layers that included near-lattice-matched ternary $In_{0.17}Al_{0.83}N$ or quaternary $In_{0.13}Al_{0.83}Ga_{0.04}N$ barriers, deposited on GaN buffers on silicon carbide (SiC) substrates. The barrier thicknesses were in the range 4–11nm.

One type of ohmic contact was based on UND's 650ºC molecular beam epitaxy (MBE) GaN re-growth process followed by non-alloyed titanium/gold metal, giving a contact resistance of 0.27Ω-mm. Devices with alloyed contacts were also produced with 0.38Ω-mm contact resistance. The alloying is achieved with a high-temperature anneal that is avoided with the MBE re-growth technique. The re-growth involves a silicon dioxide mask that protects the InAl(Ga)N barrier surface from oxidation during the 650ºC MBE.

Various passivation schemes were evaluated: plasma-enhanced chemical vapor deposition (PECVD) of silicon nitride (SiN), atomic layer deposition (ALD) of aluminium oxide (Al_2O_3), and an oxygen/argon plasma treatment of the InAl(Ga)N surface to give an oxide layer that was developed by UND as a 'dielectric-free passivation'. The researchers now designate the dielectric-free passivation as a "plasma oxide, to be more accurate".

The tested devices featured a range of gate lengths from 30nm up to 250nm. The gate width was 2x50μm. The source–drain distance was 1.6μm in devices with alloyed contacts and 1μm for non-alloyed/MBE re-grown contacts.

Devices with non-alloyed/re-grown contacts without passivation showed "essentially no dispersion" (Figure 1) and a high cut-off frequency (f_T) of 180–220GHz for gate lengths in the range 60–100nm. The use of ALD passivation reduced f_T by about 10%. The passivation also created dispersion of about 50%.

The alloyed-contact HEMTs without passivation had a low f_T of 125GHz for 60nm gates and exhibited strong dispersion. For these devices, passivation with SiN or Al_2O_3 increased f_T and reduced dispersion effects.

The UND oxide-plasma process avoids the problems of dielectric deposition techniques. The plasma treatment is thought to amorphorize the top InAlGaN barrier (~ 4nm) in the access region into an Al-rich oxide passivation layer. With alloyed contacts the process gives an f_T of 220GHz and 'negligible dispersion', similar to the HEMTs with non-alloyed ohmic contacts.

The researchers report that the characteristics "stayed largely the same over months of study". Further improvement of device stability needs "a low-permittivity moisture barrier or hermetic packaging".

Massachusetts Institute of Technology (MIT) and Texas Instruments also reported on current collapse in GaN metal-insulator-semiconductor HEMTs [D. Jin et al, 6.2]. The MIT/TI group studied operation at more than 600V, finding extreme trapping in the OFF-state, leading to total current collapse. The researchers attribute this to high-field tunneling-induced electron trapping ('Zener trapping').

"This finding gives urgency to defect control during epitaxial growth and appropriate field-plate structures for high-voltage MIS-HEMTs," the team comments.

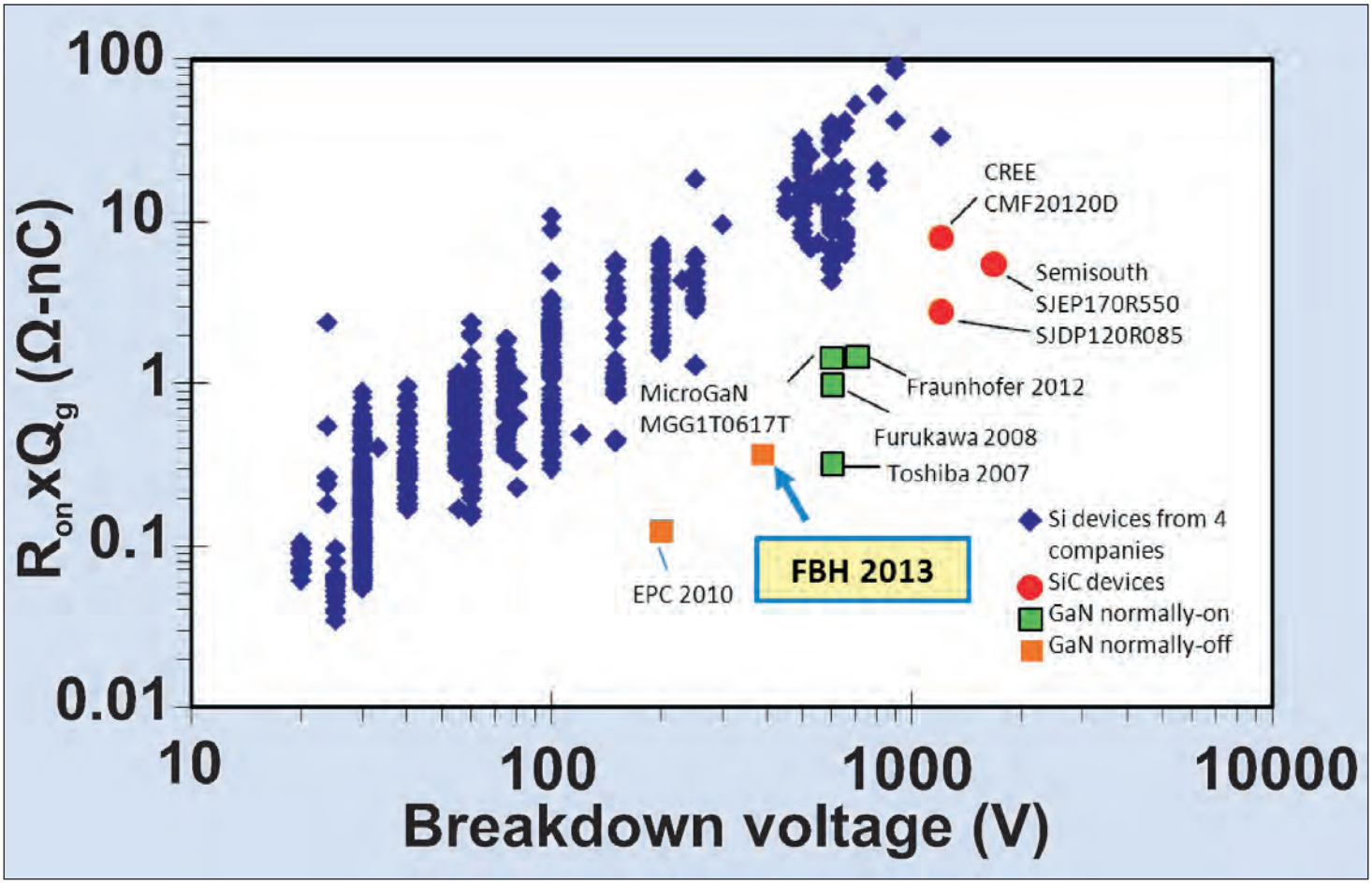

Figure 3. Comparison of product of specific on-state resistance R_{ON} and gate charge Q_g versus breakdown voltage for different device families. R_{ON} relates to on-state device losses and gate charge Q_g limits maximum obtainable switching speed.

Dynamic response

Ferdinand-Braun-Institut, Leibniz Institut für Höchstfrequenztechnik (FBH) reported on dynamic switching limitations of GaN power transistors [J. Würfl et al, 6.1]. Dynamic on-resistance is another way of expressing the problems of dispersion/current collapse.

The researchers produced both normally-on and normally-off HEMTs using different gate stack process modules (Figure 2). The normally-off HEMTs included p-GaN in the gate region. The normally-on transistor used a metal stack of iridium/titanium/gold. Benzocyclobutene (BCB) was used for passivation. Isolation was achieved with ion implantation. Although the process can be used with GaN/Si substrates, the reported work involved only n-SiC substrates.

The researchers carried out a series of process variations designed to investigate the effects of epitaxial buffer design. For power switching devices, one wants high values of breakdown strength combined with low dynamic on-resistance. Unfortunately, devices produced with buffers exhibiting 170V/μm breakdown values often have unusably high dynamic on-resistance.

One technique to increase breakdown strength is to increase carbon concentration. Alternatives include iron-doping and adding an AlGaN back-barrier beneath the channel layer. While these techniques reduce dynamic on-resistance, they also reduce the breakdown range to 40–50V/μm. The carbon-doping method introduces deep acceptor levels that charge and discharge slowly and thus affect the dynamic performance.

Finally, the researchers developed a combination of GaN:C with an AlGaN back-barrier close to the channel layer that increased the breakdown to 80V/μm and reduced the dynamic/static on-resistance ratio to 1.1 at 65V switching.

Tests with 500V drain bias showed that dynamic on-resistance increases by factors of 880 after switching and 220 after 10μs for a device with heavily doped GaN:C ($2x10^{19}/cm^3$) buffer. By contrast, the dynamic on-resistance factor was only 2.5 for a device with AlGaN back barrier on GaN:C doped at $4x10^{18}/cm^3$.

The researchers comment: "This is a breakthrough, showing that GaN devices really outperform Si-power devices in terms of the $R_{ON}xQ_g$ product and therefore in terms of potential system efficiency."

A normally-off device switching at 400V demonstrated an $R_{ON}xQ_g$ product as low as 0.4Ω-nC using an iron-doped buffer (Figure 3).

Monolithic E/D MIS-HEMTs

Hong Kong University of Science and Technology and Chinese Academy of Sciences' Institute of Microelectronics reported on a monolithic process for creating integrated 600V enhancement-mode (normally-off) and depletion-mode (E/D) MIS-HEMTs [Zhikai Tang et al, 6.4].

While power-switching GaN device research tends to focus on the difficult-to-achieve enhancement-mode behavior, the Chinese researchers see potential applications arising from the ability to produce both types of device on one chip.

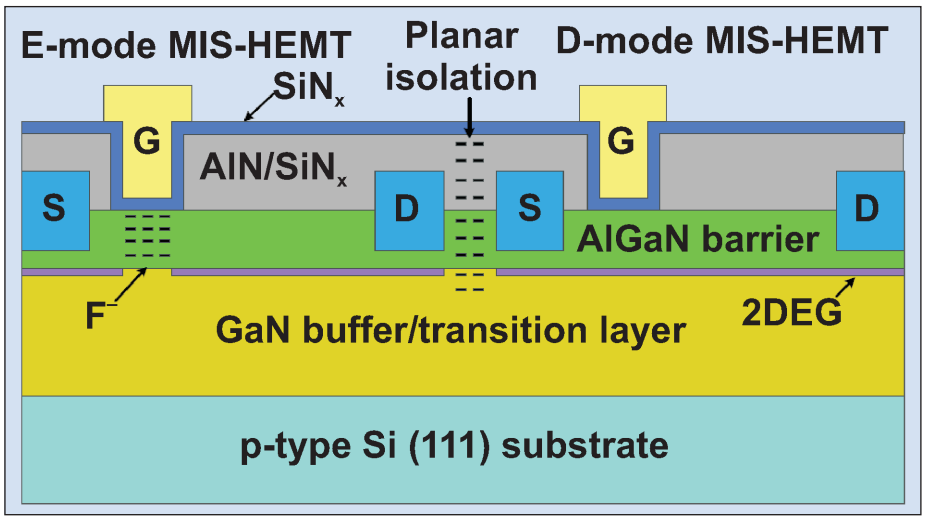

Figure 4. Schematic cross section of monolithically integrated E/D-mode SiNx/AlGaN/GaN MIS-HEMTs.

As an example, they designed and created a high-voltage start-up circuit for off-line switched-mode power supplies (SMPSs) using their integrated E/D-transistor process. Such circuits are used to charge up the capacitor in pulse-width modulation ICs in start-up mode. After start-up, this charging is supplied by the power stage. Conventional start-up circuits use silicon-based D-mode junction field-effect transistors (JFET) along with E-mode MOSFETs.

The GaN-based circuit used one D-mode and two E-mode transistors. A silicon-based op-amp was also used as hysteretic comparator with 2.8V reference voltage.

Other potential applications for integrated E/D GaN transistors include level-shifting and low-voltage control/sensing/protection functional blocks.

The devices (Figure 4) were grown on (111) Si substrates. The 21nm barrier layer consisted of GaN/$Al_{0.25}Ga_{0.75}N$/AlN. The GaN buffer/transition layer was 3.8μm thick. The ohmic contacts were achieved with titanium/aluminium/nickel/gold annealed at 850ºC for 30 seconds in nitrogen. A passivation layer of AlN/SiN was applied using plasma-enhanced atomic layer deposition (PE-ALD) and plasma-enhanced chemical vapor deposition (PE-CVD), respectively.

Multi-energy fluorine ion implantation achieved device isolation. Fluorine ion implantation of the gate region also created enhancement-mode transistors. The gate stack consisted of silicon nitride insulator and nickel/gold electrodes.

The device measurements were 1μm/10μm gate length/width, 1μm gate-source distance, and 15μm gate-drain. The 1μA/mm drain current off-state breakdown (BV) performance with grounded substrate was 604/640V, respectively, for the E-/D-mode devices (Figure 5). The corresponding specific on-resistances (R_{ON}) were 2.1mΩ-cm^2/1.5mΩ-cm^2.

Pulsed measurements showed negligible difference between the DC and pulsed I–V measurements of drain current in the linear region, "indicating effective suppression of current collapse". The dynamic on-resistance at 100mA/mm drain current was maintained at a low value after a 650V off-state stress.

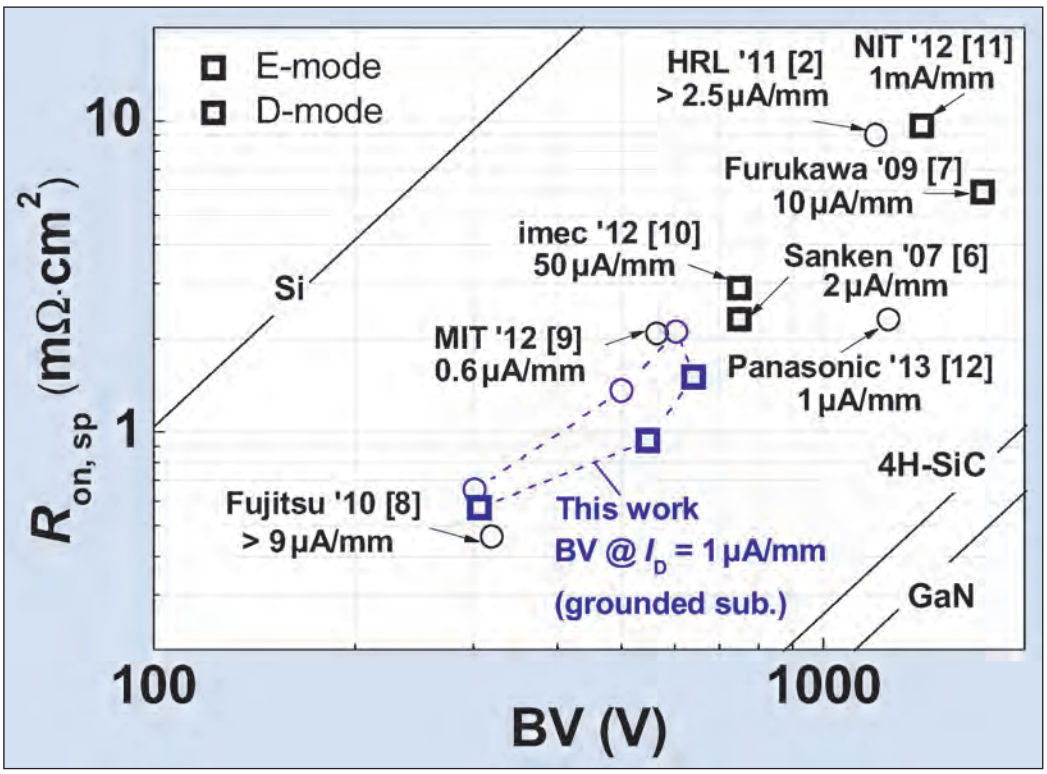

Figure 5. Specific RON versus off-state BV for a range of GaN power devices.

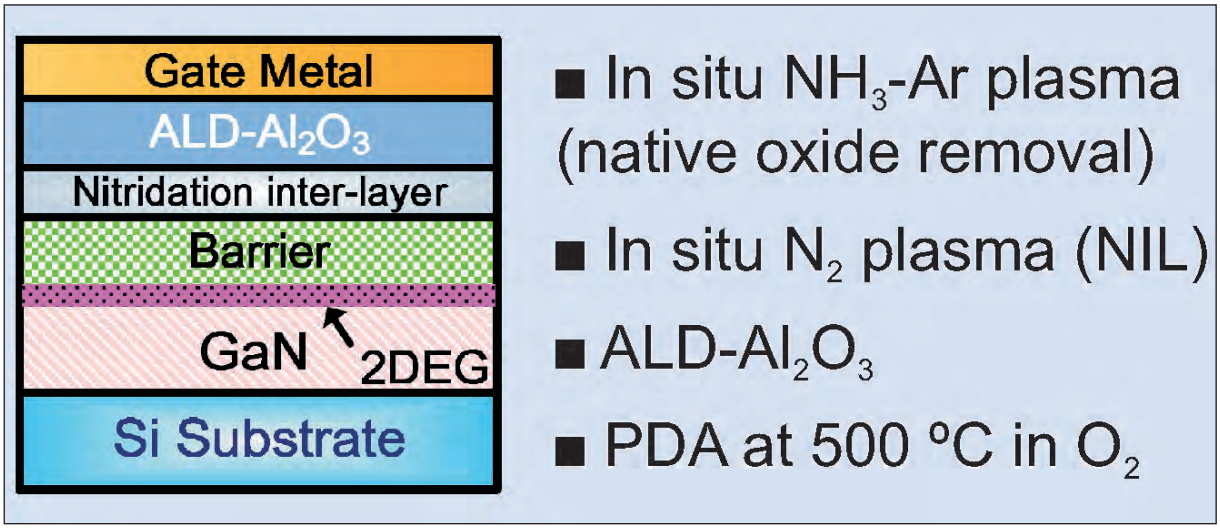

Figure 6. Schematic cross section and key process steps of Al_2O_3(NIL)/GaN/AlGaN/GaN gate dielectric stack with in-situ low-damage remote plasma pre-treatment before gate dielectric deposition.

Reducing charge trapping in metal–insulator–semiconductor structures

Hong Kong University of Science and Technology and TSMC's Analog/Power & Specialty Technology Division have developed a high-quality Al_2O_3/GaN-cap interface for Al_2O_3/GaN/AlGaN/GaN MIS-structures with low interface trap densities in the range 10^{12}–10^{13}/cm^2-eV [Shu Yang et al, 6.3]. Normally, such interfaces have trap densities in the range 10^{13}–10^{14}/cm^2-eV. Such charge trapping under the gate affects threshold voltage stability.

The process involved an in-situ low-damage NH_3-Ar-N_2 plasma pre-gate treatment in a plasma-enhanced atomic layer deposition system at 300°C (Figure 6). The researchers attribute their achievement to "effective removal of native oxide and the subsequent formation of a monocrystal-like nitridation inter-layer on the GaN surface".

The oxide removal was achieved with NH_3-Ar plasma, while the nitridation was achieved with N_2 plasma. After the process, a 25nm layer of Al_2O_3 insulation was added in the PE-ALD chamber.

X-ray photo-electron spectroscopy (XPS) and transmission electron microscopy (TEM) were used to analyze the difference between stacks with and without the plasma treatment. Without treatment, the Al_2O_3/GaN cap surface is rough and amorphous due to a high density of Ga–O bonds at the interface. These bonds are suppressed in the treated stack by the presence of the nitrided interlayer. This results in a "uniform and sharp interface".

The trap density was measured using frequency- and temperature-dependent capacitance-voltage (C–V)-based techniques to overcome the difficulty posed for traditional C–V measurements due to the relatively large separation between the dielectric/III-N interface and the conducting channel.

Silicon carbide

Researchers in Japan have achieved an ultra-high blocking of 16kV with a silicon carbide insulated-gate bipolar transistor (IGBT) [Yoshiyuki Yonezawa et al, 6.6]. At the same time, the on-state forward voltage was only 5V at 100A/cm^2 current density. The n-channel device used the flipped back-side of the n-SiC substrate to take advantage of the higher mobility of 100cm^2/V-s of the C-face $(000\bar{1})$ of the crystal structure. Si-face (0001) mobilities are typically in the range 20–30cm^2/V-s.

A further advantage of flipping the substrate and forming p^{++} regions on the back-side is that n^{++} substrates can be used. The crystal quality of p^{++} SiC substrates are very poor with high micropipe densities, leading to low conductivity. By contrast, these problems are well controlled in n^{++} SiC wafer growth.

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The researchers used a combination of implantation and epitaxial (IE) deposition to achieve selective p-wells for the emitter region. The use of epitaxy in the final stage of the p-well gives a smoother surface, enabling higher channel mobility.

The potential applications of the IGBT include smart grid and high-voltage DC, according to the team from Japan's National Institute of Advanced Industrial Science and Technology

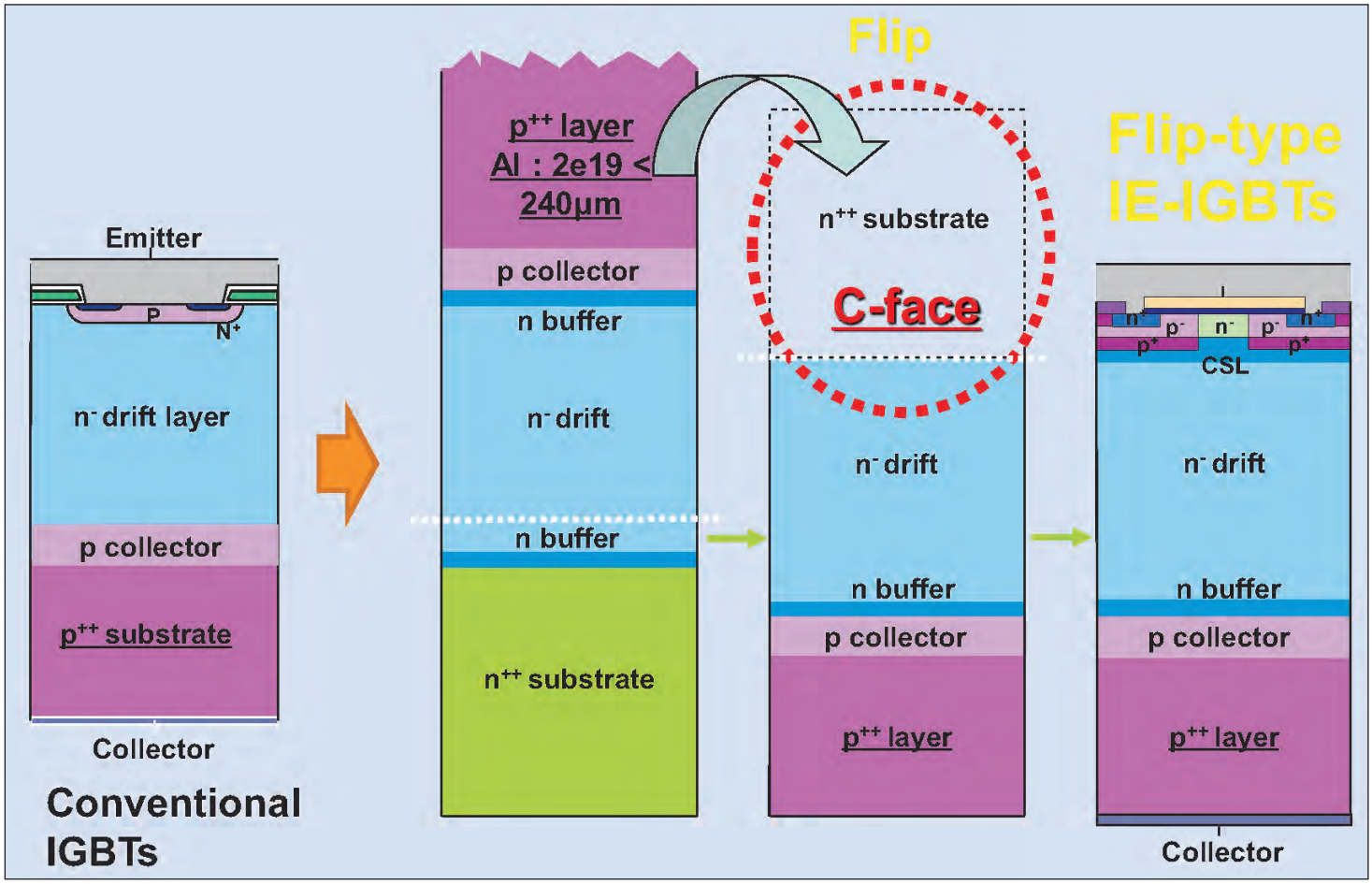

Figure 7. Fabrication process flow of flip-type IE-IGBT on 4H-SiC (000-1) carbon face.

(AIST), Fuji Electric Co Ltd, New Japan Radio Co Ltd, Tokyo Electron Yamanashi Ltd, and Kyoto University. Particular devices where SiC IGBTs could be used to increase voltage handling include static synchronous compensators (STATCOMs) and solid-state transformers (SSTs).

Epitaxial growth of the semiconductor material began with growth on the Si-face of the substrate to give the collector and drift structures (Figure 7). The n-type drift layer of more than 150μm thickness was grown on a buffer layer that converted basal plane dislocations into threading edge dislocations. A second 1–2μm buffer on top of the drift layer was grown before an aluminium-doped p-type collector. The pre-flip structure was completed with more than 100μm of p^{++} SiC as the flipped substrate layer.

After flipping, the n^{++} substrate was removed and the new surface subjected to chemical mechanical polishing (CMP). The flipped growth proceeded by first adding a 2μm charge storage layer (CSL).

The p-wells were then formed with a selective implantation of aluminium, followed by epitaxial growth of 0.5μm p^{-}-SiC. The JFET n-channel and n-extension were achieved using selective implantation of nitrogen into the p^{-}-SiC.

The gate oxide was achieved with a combination of dry and wet oxidation. The wet oxidation was carried out in a hydrogen-rich environment that suppressed threshold voltage shift to 0.1V at ±30V gate potentials. The researchers say that this could show that hydrogen atoms provide an effective termination for SiO_2/SiC interface states.

The 3mm x 3mm device consisted of a series of 14.8μm-pitch unit cells in a striped array. With a 1.6μm JFET gate length, the breakdown occurred at 16kV. The peak field-effect mobility (μ_{FE}) was 75cm^2/V-s and at 20V gate-emitter voltage it was still 60cm^2/V-s. The researchers comment: "This is considerably higher than the μ_{FE} of MOSFETs on a Si face."

The collector-emitter voltage behavior remained relatively stable, with 10V gate potential over a wide temperature range of 100–250°C.

A larger 5.3mm x 5.3mm IE-IGBT was produced on a different substrate. This second device achieved a higher 16.5kV breakdown with a forward voltage of 5.2V at 100A/cm^2. The researchers believe longer carrier lifetimes of 10μs could be achieved with carbon implantation and longer oxidation processes. Longer lifetimes are expected to improve the IE-IGBT performance. ■

The author Mike Cooke is a freelance technology journalist who has worked in the semiconductor and advanced technology sectors since 1997.