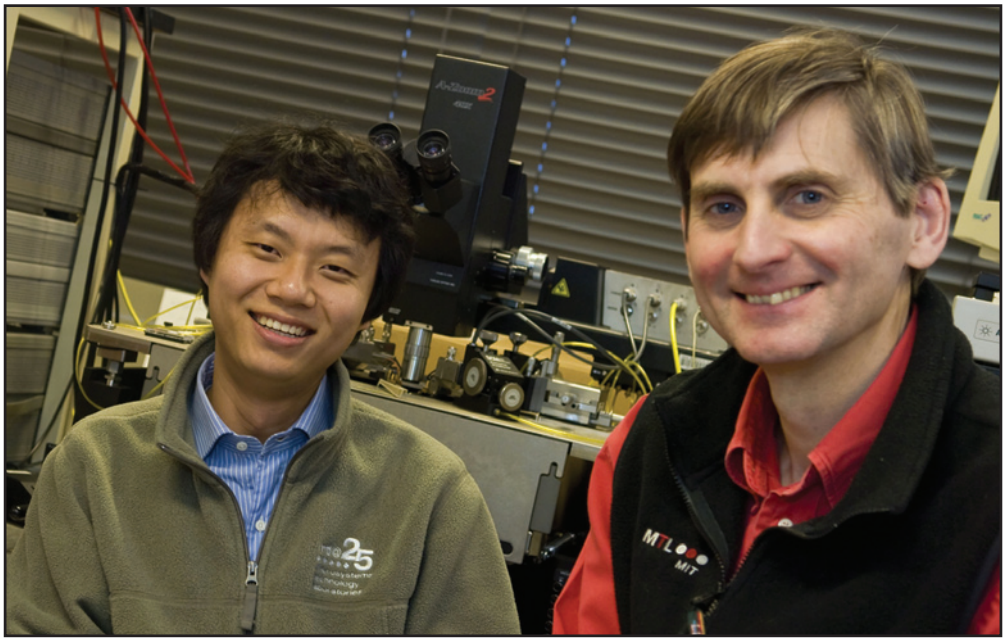
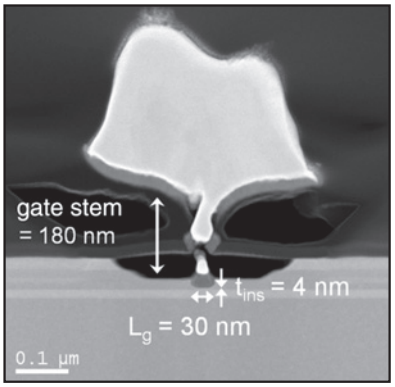
FURTHER READING

Page 406
'InGaAs HEMT with InAs-rich InAlAs barrier spacer for reduced source resistance', T.-W. Kim, D.-H. Kim and J. A. del Alamo

MIT takes another step forward in its high performance and high-frequency application HEMT technology research

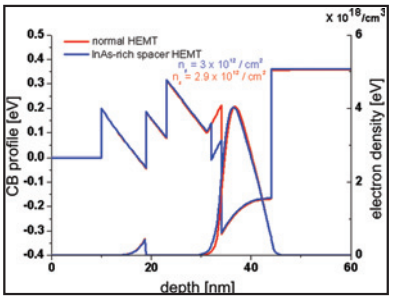
reinforcing the barrier





Researchers at Massachusetts Institute of Technology (MIT) in the US have demonstrated a new approach to improve the high-frequency characteristics of InAlAs high electron mobility transistors (HEMTs). In their Letter in this issue Taewo Kim, Dae-hyun Kim (now at Teledyne Scientific Company) and Jesús del Alamo report on how their optimised heterostructure design with an InAs-rich spacer in the InAlAs barrier increased in the current gain cut-off frequency f_T to 530 GHz from 390 GHz for a device with a gate length L_g of 40 nm.

ABOVE: MIT researchers Dr Taewoo Kim (left) and group leader Professor Jesús del Alamo (right)
ABOVE RIGHT: The state-of-the-art InP-based HEMT developed at MIT has a 30 nm gate length. A 10 nm thick channel includes a 5 nm thick InAs core, and the InAlAs barrier has an effective thickness of 4 nm [D.-H Kim and J. A. del Alamo, '30 nm InAs pseudomorphic HEMTs on an InP substrate with a current-gain cutoff frequency of 628 GHz', IEEE Electron Device Lett., Vol. 29, No. 8, pp. 830–832, 2008]
RIGHT: A 1D Poisson-Schrodinger simulation of the conduction band diagram under the source contact of normal HEMT and InAs-rich spacer HEMT shows how the increase in InAs mole fraction eliminates one energy spike in the path between the ohmic contact and the channel



A high performer

With their excellent transport properties, proven reliability, and well understood physics and technology, III-V compound semiconductors offer a practical alternative material system for CMOS, and currently the III-V community is actively looking for a technology that reaches beyond silicon CMOS. InAlAs/InGaAs HEMTs on InP have shown outstanding high-frequency performance; increasing the InAs content of InGaAs rapidly improves electron transport properties and increases conduction band discontinuity, which results in enhanced carrier confinement. As a consequence, InP-based HEMTs are uniquely suited for millimetre-wave applications in radar, radio astronomy, high resolution imaging arrays, high capacity wireless communications, high data rate optical fibre systems and sub-millimetre-wave spectroscopy.

Reduced resistance

MIT has been investigating InP-based HEMTs for several years and recently they have achieved state-of-the-art high-frequency performance including an f_T of 644 GHz and a maximum oscillation frequency (f_{max}) of over 1 THz for devices with gate lengths of 30 nm and 50 nm, respectively (see references [1] and [7] in their Letter on page 406). The current bottleneck for further improvement in the frequency response is the reduction in the parasitic elements, among which the source and drain resistance are particularly important.

In their analysis of the parasitic resistance, the MIT team found that its dominant component is the tunnelling resistance between the cap layer and the channel. To minimise this tunnelling resistance, they used the bottom 2 nm spacer of the barrier which is made from $In_{0.62}Al_{0.48}As$ while the rest of the barrier has a lattice matched composition with 48% InAs. This was found to eliminate one of the energy spikes in the conduction band under the contact regions, which resulted in a lower barrier resistance. They also ensured that their design was optimised so that the gate leakage current did not significantly increase over the useful operating range. With their enhanced design, the source resistance was reduced to R_s = 170 Ω-μm at a voltage V_{DS} of 0.5 V from the previous best value of 232 Ω-μm in a similar device with a lattice matched barrier. The reduced R_s also resulted in enhanced trans-conductance characteristics and, of course, the significant increase in f_T to 530 GHz.

Towards III-V CMOS

The MIT team are continuing to work on improving the performance of their devices, and they are actively researching the introduction of a self-aligned contact approach to reduce the source resistance. The group is also currently working on III-V CMOS for logic applications and are trying to harness the outstanding electron transport properties of InGaAs, InAs and other III-V compound semiconductors to address the scaling issues of silicon and extend Moore's Law. At 30 nm gate length, the III-V devices are already close to their scaling limit from a logic point of view, so the team is looking at the introduction of a high-k dielectric in the gate stack, and the development a self-aligned gate scheme to minimise device foot-print size and parasitic resistance. They hope in the future that their efforts will lead to the III-V transistor being widely used in millimetre-wave and other high-frequency applications, as well as in new applications such as III-V CMOS.

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