Heterostructuring for high speed, power and light

Last month we reported on developments presented at December 2008's International Electron Devices Meeting (IEDM) towards III-V MOSFETs for use in mainstream high-performance microelectronics. Here Mike Cooke looks at progress with the wider variety of heterostructure materials (III-nitride, III-arsenide, III-phosphide) for power, light and high speed applications.

Nitride semiconductors are best known for their ability to produce higher-frequency light (green to ultraviolet) both in normal LEDs and laser diodes. In recent years, the material system's ability to handle higher critical fields has spawned a new area of development — power devices. At IEDM 2008 last December, this new focus was expressed with most nitride papers being concerned with developing the new power capability. Meanwhile, the more traditional arsenide and phosphide semiconductors have been pushed in speed for microwave applications (GHz–THz), often with an eye to combination with silicon technology.

Nitride power

One group at Hong Kong University of Science and Technology (HKUST) reported on using industry-standard AlGaN/GaN-on-Si epitaxial wafers from Nitronex to develop low-cost AlGaN/GaN devices for switched-mode power supply (SMPS) converters [1]. The integrated devices consisted of high-performance lateral field-effect rectifiers (L-FER) and normally-off HEMTs (Figure 1). The rectifier had a 470V breakdown and 2.04mΩcm^2 specific on-resistance. A boost converter proof-of-concept with 1MHz switching frequency was also produced based on the integrated device.

The normally-off HEMT makes the power switch fail-safe with low circuit complexity and higher noise margin. The normally-off nature of both the L-FER and HEMT is achieved using a CF_4 plasma treatment. Fluorine atoms from the plasma deplete the two-dimensional electron gas (2DEG) channels of the HEMT and L-FER, shifting the threshold from −2.1V to +0.9V. Schottky contacts are then made for the HEMT gate and L-FER anode (shorted with an Ohmic contact).

The drift length between the anode and cathode regions of the L-FER can be varied to trade-off breakdown voltage (BV) with specific on-resistance (R_{on}). A longer drift region offers a higher BV at the cost of higher R_{on}. The researchers point out that the forward turn-on voltage at forward current densities of 100A/cm^2 for their device

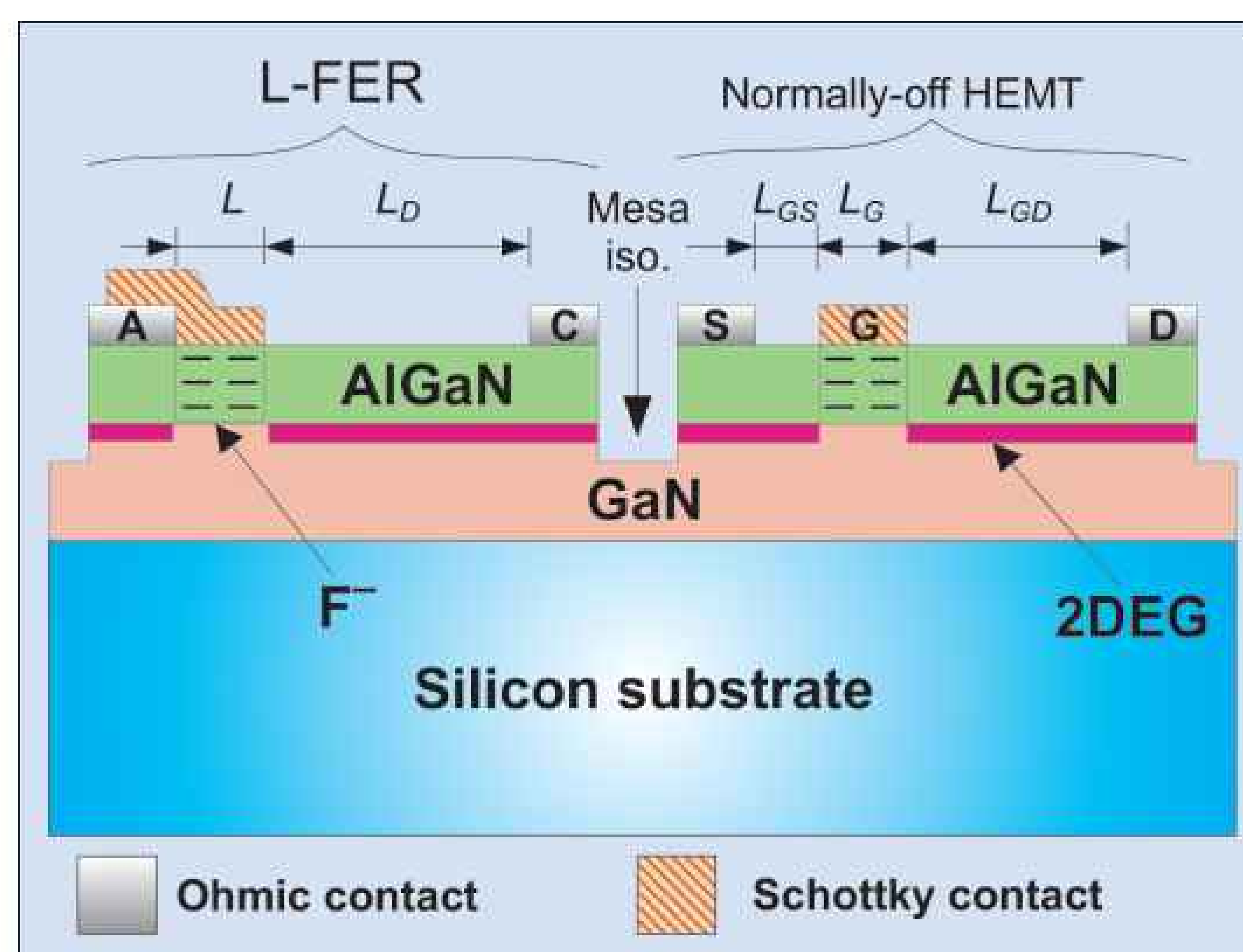

Figure 1. Schematic cross-sectional diagram of a lateral field-effect rectifier (L-FER) with normally-off HEMT. L_D is the drift length of the L-FER.

with various drift lengths is significantly lower than that achieved for silicon p-i-n and SiC Schottky barrier (SBD) diodes that are currently used for these types of application. This is attributed to the turn-on control offered by the field-effect mechanism compared with p-i-n or Schottky junctions. High 2DEG densities and mobilities also play a role. The voltage performance is little affected by temperatures up to 250°C, although the current decreases somewhat as a result of phonon scattering.

The monolithic boost converter was constructed from an L-FER with 15μm drift region and 1.5μm gate HEMT (gate–source distance 1.5μm, gate–drain distance 12μm). The width of the device was 2mm for the HEMT gate and 1mm for the anode of the L-FER. The chip area was 0.36mm^2, with the active region being 0.0625mm^2. With a 1MHz switching speed, 55% duty cycle and 10V input, an output voltage of 21V with 84% efficiency is obtained. At lower voltages the power efficiency decreases due to the increased R_{on} of the component devices. The main reason for this is given as being due

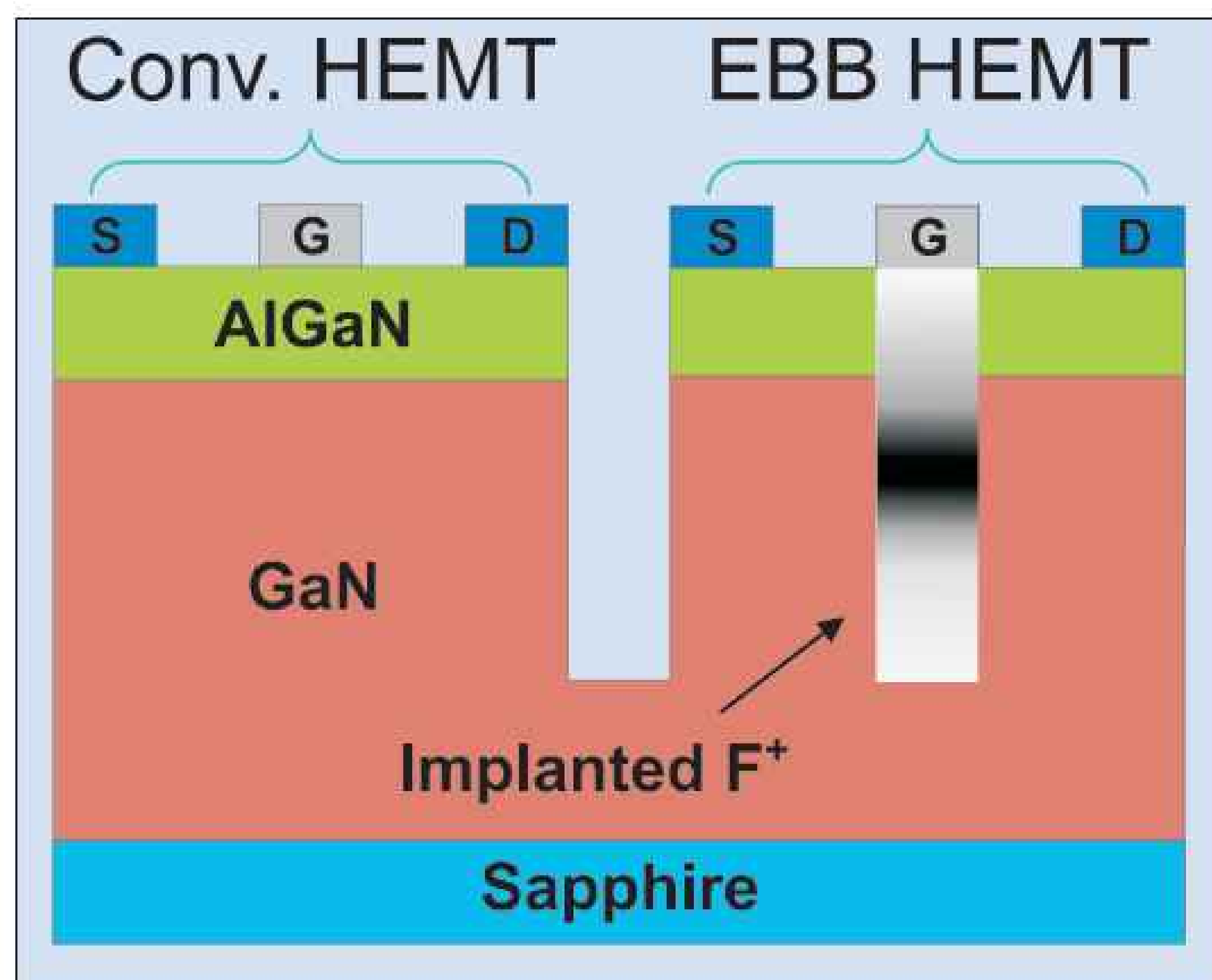

Figure 2. Schematics of conventional HEMT and HKUST's HEMT with fluorine implanted enhanced back barrier to block unwanted off-state current flow.

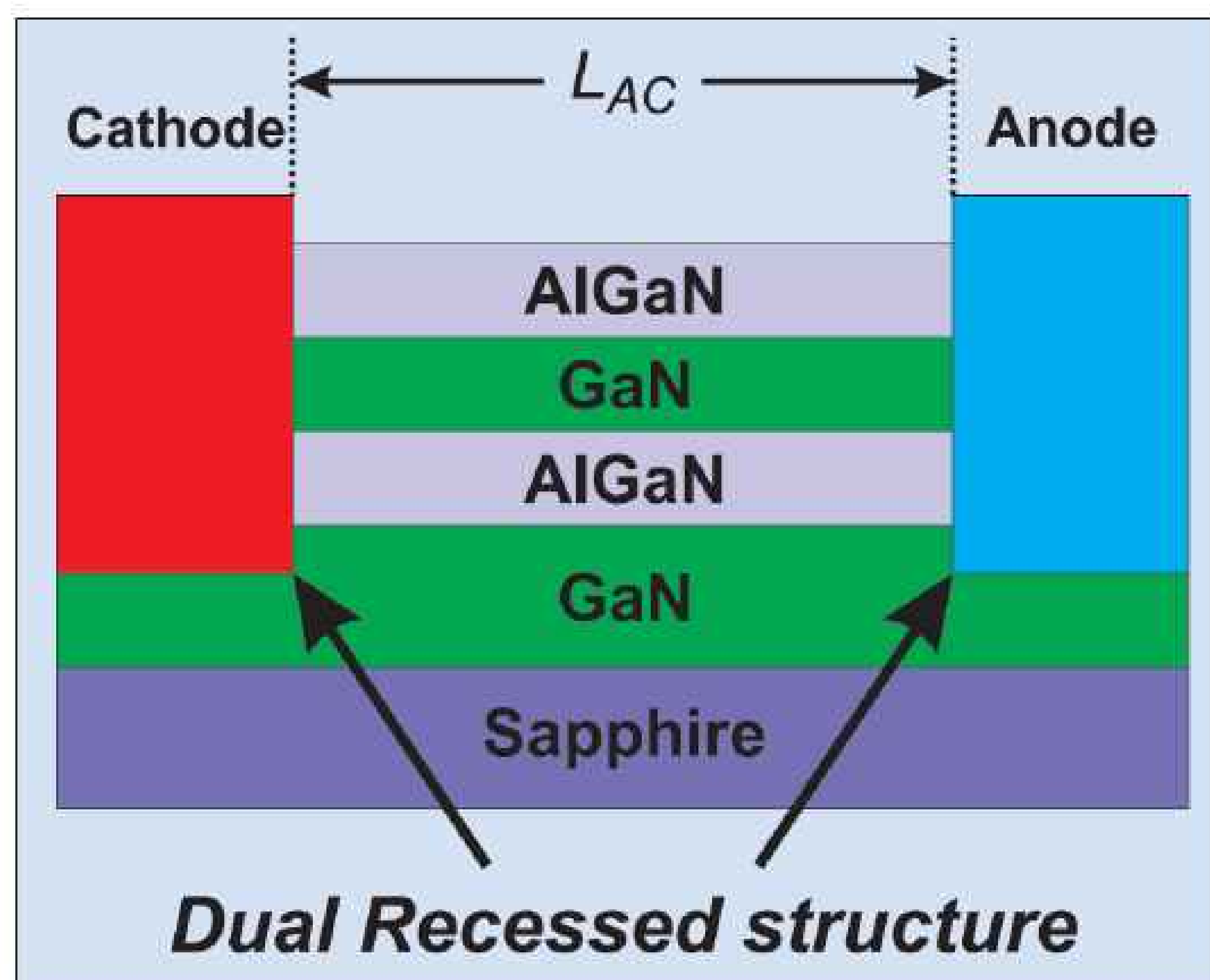

Figure 3. Schematic of Panasonic's natural superjunction diode with double channel and dual-recess structure.

to increased dynamic resistance related to current collapse at higher switching amplitudes and frequencies. Current collapse can be ameliorated using passivation and field-plates.

Further study of the use of fluorine in improving source injection induced off-state breakdown in AlGaN/GaN HEMTs was the subject of another HKUST presentation [2]. Drain-injection techniques were used to study both source and gate injection induced impact ionization. Source injection was identified as the culprit in leading to premature three-terminal breakdown of the device.

The researchers found that a 35% increase in breakdown performance could be achieved in enhanced back-barrier (EBB) HEMTs with a fluorine implant (Figure 2). Fluorine ions beneath the channel were found to be an effective blocker of source injection through the buffer layer. The effect of the negatively charged fluorine in the GaN is to modulate the band structure, raising the conduction band in the buffer by about 1eV and thus reducing the source current injected into the high-field region of the channel. The HEMTs were produced on sapphire substrates using MOCVD.

Panasonic's Semiconductor Device Research Center in Kyoto has developed what it calls 'Natural Super Junctions' (NSJ) using GaN technology [3]. Diodes produced from the structure (Figure 3) achieve extremely high breakdown voltages of 9300V, while the specific on-resistance ($R_{on}A$) remains low (176mΩcm^2). These parameters are claimed to be records over GaN-based Schottky barrier diodes (SBDs).

Traditional super junctions consist of alternating layers of p- and n-type material. This structure enables higher levels of breakdown voltage but is difficult to grow with sufficient accuracy. The voltage is applied along the layers rather than across, as is more usual in single pn-junction diodes. The structure reduces the peak field that arises for a given applied potential. This increases the breakdown voltage that is achievable. Complete balance between the n- and p-type regions is hard to achieve due to the difficulties of controlling film thicknesses and impurity concentrations.

The Panasonic team believes that junctions of undoped GaN with AlGaN can behave like a natural super-junction due to the polar nature of the material where the Ga ion in the lattice tends to have a positive charge and the N ion tends to have a negative charge. Two-dimensional numerical simulations based on charge continuity and on Poisson's equation were carried out to model an AlGaN/GaN structure with p-GaN at one end (anode) and n-GaN at the other (cathode). The AlGaN and GaN layers were both 1μm long and 50nm thick. At equilibrium, an electron gas is formed in the GaN material while a hole gas forms on the AlGaN surface opposite the AlGaN/GaN junction. At reverse bias these carriers disappear. These simulations were then confirmed by producing single- and dual-channel diodes with and without recessing. Dual-recessing increases the forward current and thus lowers the specific on-resistance.

Joh and Del Alamo of MIT have worked on charge trapping in GaN HEMT devices [4], targeting high-power RF and high-voltage applications. Excessive charge trapping and detrapping (Figure 4) in such devices degrade the performance and lead to current collapse effects.

Joh and Del Alamo have found that when GaN HEMTs are stressed beyond a critical voltage, the trapping behavior is significantly enhanced inside the AlGaN barrier layer or at the surface. The buffer layer, however, has the same trapping properties as before the degradation event.

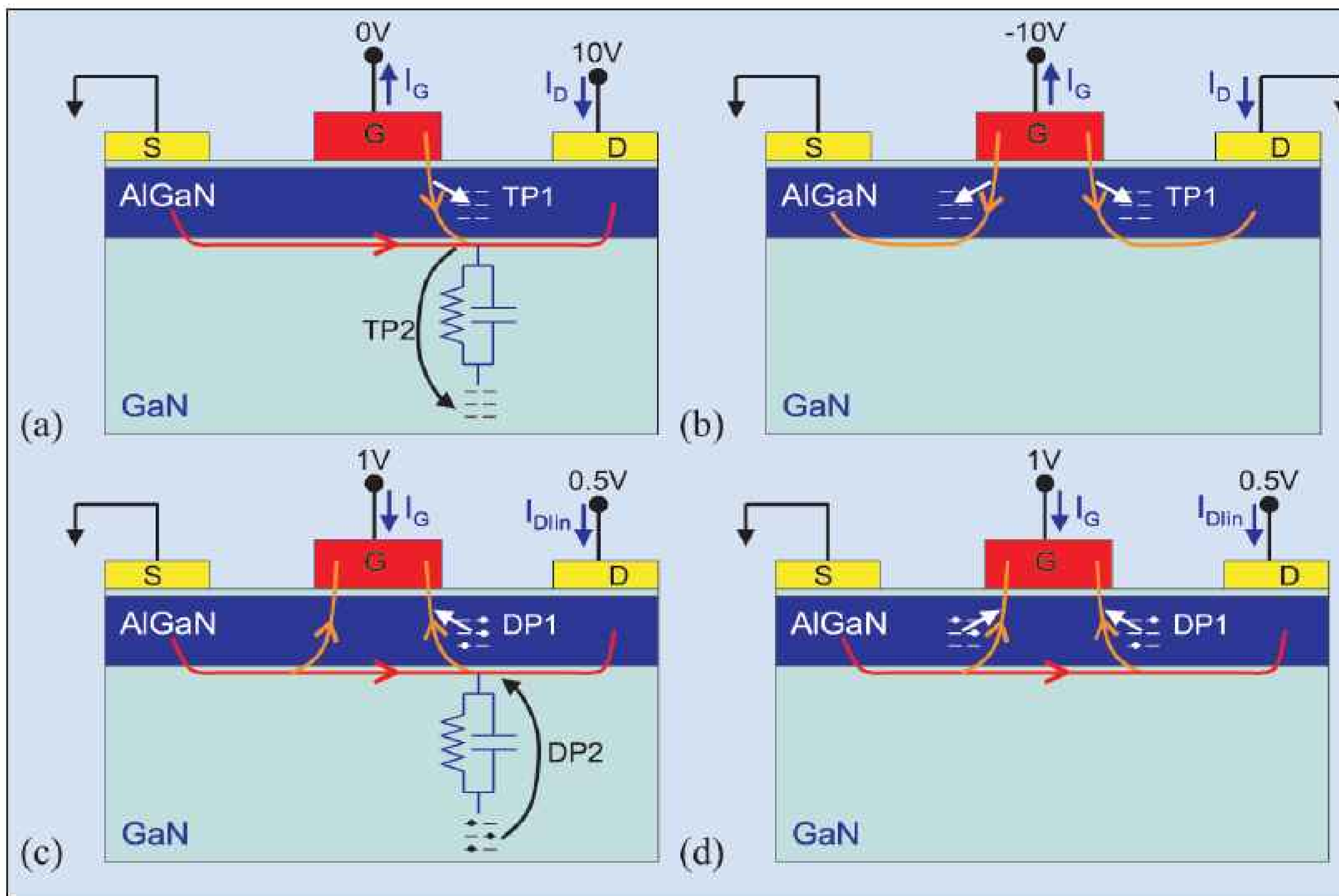

Figure 4. Different trapping and detrapping mechanisms. (a) On-state trapping. (b) Trapping with V_{DS} = 0. (c) Detrapping after on-state pulse. (c) Detrapping after V_{DS} = 0 pulse.

These insights are the result of a newly developed current transient analysis methodology. This reveals traps in the GaN buffer and also at the surface or in the AlGaN barrier in fresh devices. Degradation introduces new traps with a broad spectrum of detrapping time constants on the drain side of the device.

The technique was demonstrated on a 0.25μm-gate millimeter-wave GaN HEMT with a source field plate. The device width was 2 x 25μm. The performance could be restored from the stressed condition to the initial condition by shining a microscope light on the device for 30s.

The researchers believe that the results are consistent with their previous findings that suggest that deep trap states result from an inverse piezoelectric effect where the electric field physically stresses the material to the point where defects are introduced.

Researchers from the University of Padova and Matsushita Electric Industries (now officially Panasonic) have studied the degradation of InGaN laser diodes designed for use with BluRay optical disk storage [5]. The nature of the current through the device is found to be a major driver towards degradation of such devices.

The work was carried out on low-dislocation-density (10^6/cm^2) LDs with a threshold current density of 3.2kA/cm^2 (29mA) and a slope efficiency of 1.6W/A. The case temperature of the devices was raised to 70ºC to accelerate the degradation process. Stressing the devices at constant current levels shifts the threshold upwards. Degradation occurred at currents as low as 200μA, suggesting that the role of the optical field in the degeneration process is small. It was also found that current stress reduced the sub-threshold emission.

These facts have led the researchers to propose that the degradation is due to a shortening of the non-radiative recombination lifetime so that its importance increases relative to the radiative recombination, reducing the effectiveness of the device. This was confirmed by extracting the non-radiative recombination lifetime from plots comparing efficiency with output power. The researchers believe that the increase in non-radiative recombination is correlated with an increase in the concentration of defects in the active layer.

Arsenide speed

Another Hong Kong University of Science and Technology (HKUST) group, Lau et al [6], described the production of AlInAs/GaInAs metamorphic HEMTs (mHEMTs) on silicon wafers 'for the first time'. The researchers see this approach as being attractive to the development and integration of monolithic microwave ICs (MMICs) and high-speed logic with more mature silicon technology.

In 2007, AlInAs/GaInAs HEMTs were grown on silicon using molecular beam epitaxy (MBE). However, for integration with silicon CMOS technologies, an MOCVD approach is preferred, and this was the growth method used by HKUST. A composite series of buffer layers was grown on the silicon before the undoped $In_{0.53}Ga_{0.47}As$ channel (Figure 5, Table 1). The recessed gate consisted of a Ti/Pt/Au Schottky contact. The source/drain contacts consisted of a six-layer metal system of Ni/Ge/Au/Ge/Ni/Au.

The Hall mobility of the two-dimensional electron gas (2DEG) was measured at 4540cm^2/Vs at 300K. The sheet carrier density was 8x10^{12}/cm^2. The mobility increased to 14,000cm^2/Vs and the sheet carrier density fell to 5x10^{12}/cm^2 at 77K.

X-ray diffraction rocking curves revealed that the GaAs and InP buffer layers were fully relaxed and that the other layers were compositionally lattice-matched to the InP layers. Transmission electron micrographs (TEMs) showed misfit and threading dislocations in the compositional buffer. The final two buffer layers were

found to effectively terminate the threading dislocations, leaving the active layers with no significant threading dislocations. This is necessary for the formation of a 2DEG with high mobility.

Transistors with 1.0μm gates had cut-off frequencies of 32GHz and 44GHz for f_T and f_{max}, respectively. The peak extrinsic transconductance (G_m) was 587mS/mm. The reverse gate leakage was somewhat higher than desirable for applications, but the researchers point out that no passivation or plasma treatment had been performed. Such treatment is a normal part of commercial production to reduce gate leakage.

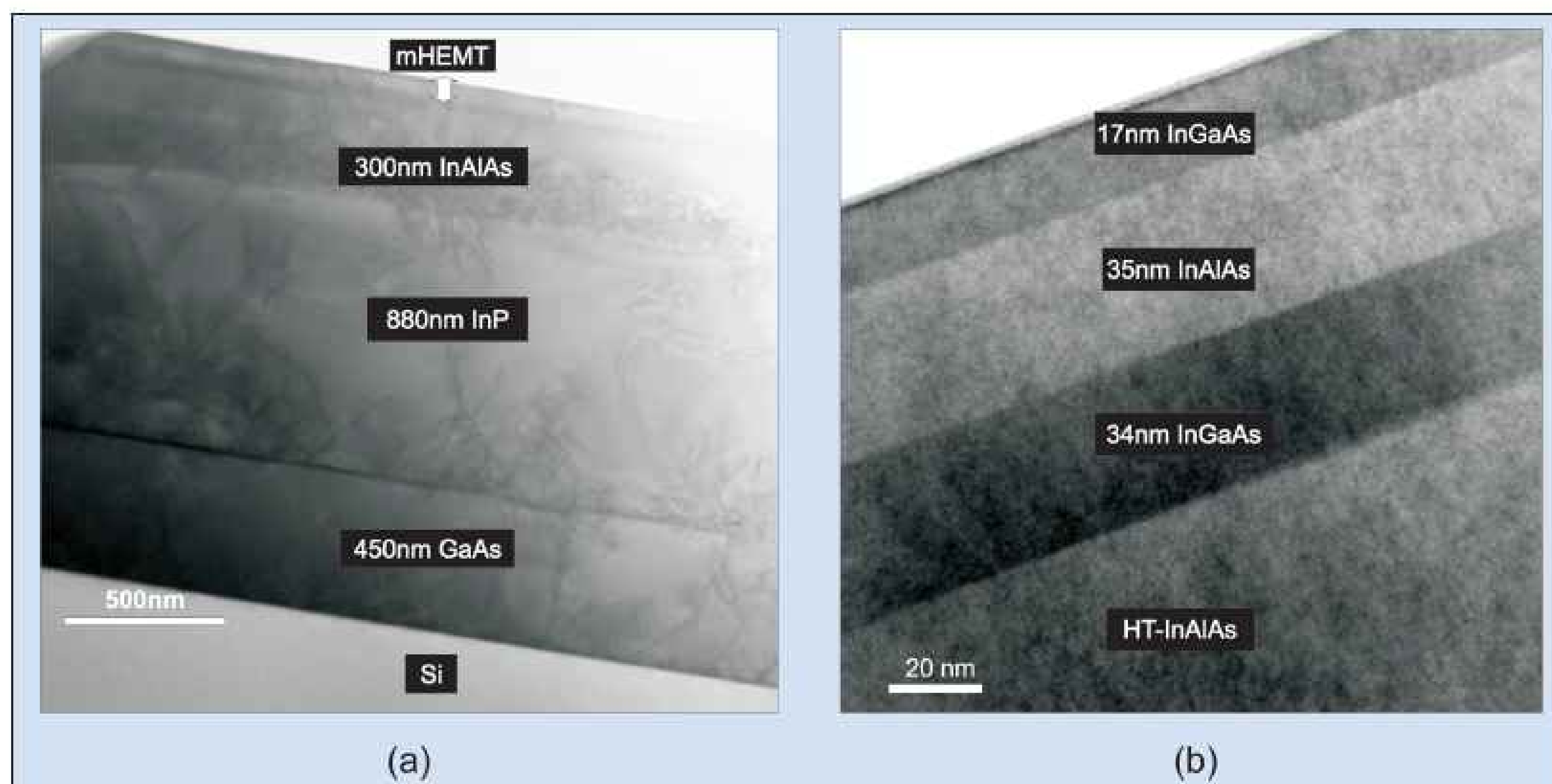

Figure 5. TEM cross-section of an mHEMT structure.

Rochester Institute of Technology, University of Notre Dame and Amberwave Systems are claiming a record peak-to-valley current ratio (PVCR) of 56 for GaAs-based Esaki inter-band tunnel diodes grown on silicon [7]. Normal GaAs tunnel diodes have PVCRs in the range 21–25, while Si-based devices have PVCRs of 6 at best. Only tunnel diodes grown on indium phosphide substrates show better performance (a PVCR of up to 144 for a resonant inter-band device, Table 2).

The researchers see their achievement of higher-performance tunnel diodes on silicon as a spur to further exploration of new tunneling-based circuit architectures to extend and enhance CMOS, such as for static random access memory and field-effect transistors.

The deposition of GaAs on silicon has to deal with the large lattice mismatch as well as coefficient of thermal expansion differences between the two materials.

Table 1. Nominal layered structure of mHEMT device grown by MOCVD.

Layer	Thickness	Function
$In_{0.53}Ga_{0.47}As$:Si	15nm	Cap layer
Undoped $In_{0.50}Al_{0.50}As$	30nm	Barrier
Si	$(4–8)\times10^{12}cm^{-2}$	δ-doping
Undoped $In_{0.50}Al_{0.50}As$	5nm	Spacer
Undoped $In_{0.53}Ga_{0.47}As$	32nm	Channel
Undoped HT-$In_{0.50}Al_{0.50}As$	180nm	Buffer 5
Undoped LT-$In_{0.53}Ga_{0.47}As$	180nm	Buffer 4
Undoped HT-InP	730nm	Buffer 3
Undoped LT-InP	150nm	Buffer 2
Undoped HT-GaAs	450nm	Buffer 1
Undoped LT-GaAs	10nm	Nucleation
n-type Silicon	(100)	Substrate

The team implemented a new technique called aspect ratio trapping (ART), which uses patterned, sub-micron-wide trench features and epitaxy of germanium, which is closer to GaAs in terms of lattice matching (Figure 6).

Table 2. Comparison of Rochester Institute of Technology's Esaki diode on silicon with similar devices.

Type	Substrate	Tunnel diode	Growth technique	J_p(A/cm^2)	PVCR	Study
RITD	Si	Si/SiGe	MBE	5000	6	Eberl, 2001
RTD	Si	AlAs/InGaAs	MBE/Wafer Bond	30000	27	Evers, 1996
Esaki	GaAs	P+/N+ GaAs	Alloy	N/A	25	Holonyak, 1960
Esaki	GaAs	GaAs/$In_{0.1}Ga_{0.9}As$	MOCVD	1500	22	Richard, 1993
RTD	InP	AlInAsSb/InGaAs	MOCVD	22000	46	Su, 2002
RTD	InP	AlAs/InGaAs/InAs	MBE	3000	51	Smet, 1993
RITD	InP	InGaAs/InAlAs	MBE	200	104	Day, 1993
RITD	InP	InGaAs/InAlAs	MBE	200	144	Tsai, 1994
Esaki	**Si**	**GaAs/P^+/N^+ $In_{0.1}Ga_{0.9}As$**	**UHVCVD/MOCVD**	**9**	**27**	**IEDM 2008 (TD 1)**
Esaki	**Si**	**GaAs/P^+/N^+ $In_{0.2}Ga_{0.9}As$**	**UHVCVD/MOCVD**	**1000**	**43**	**IEDM 2008 (TD 2)**
Esaki	**Si**	**P^+/N^+ $In_{0.1}Ga_{0.9}AsAs$**	**UHVCVD/MOCVD**	**250**	**56**	**IEDM 2008 (TD 3)**
Esaki	**Si**	**P^+/N^+ $In_{0.1}Ga_{0.9}As$ graded**	**UHVCVD/MOCVD**	**65**	**8**	**IEDM 2008 (TD 4)**

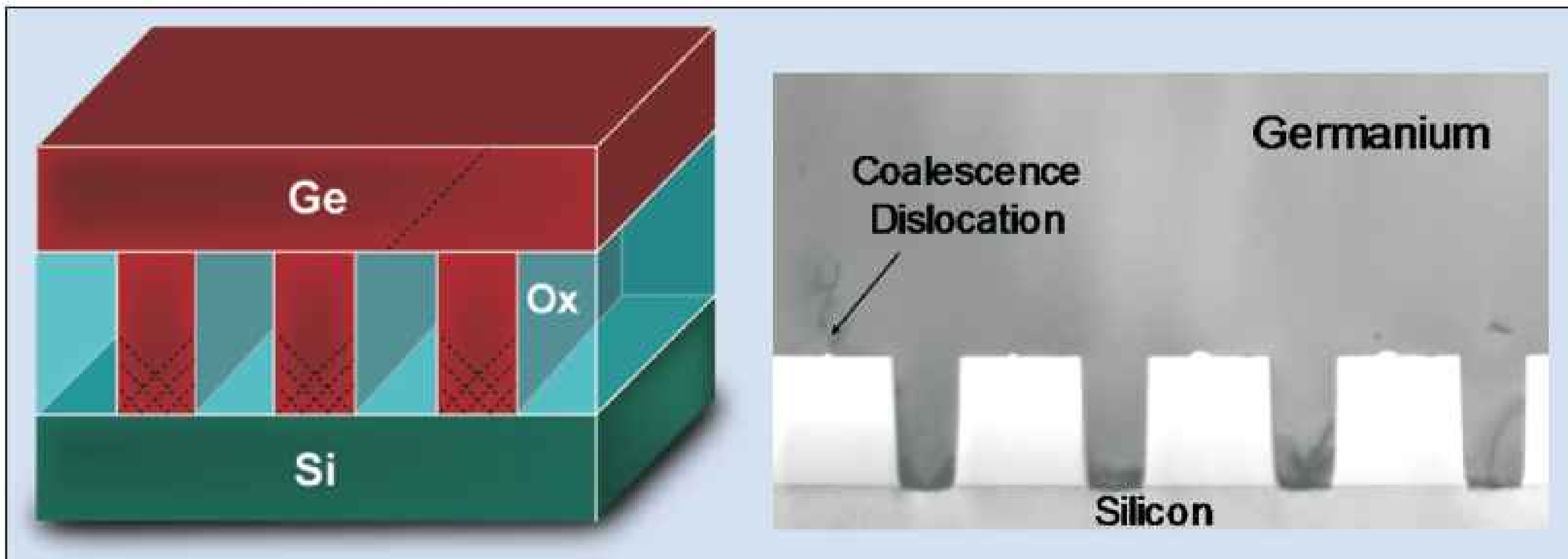

Figure 6. Aspect ratio trapping — dislocation densities in germanium on silicon can be reduced with trench structures that trap the faults.

The GaAs/InGaAs deposition used by the team was metal-organic chemical vapor deposition (MOCVD) rather than the molecular beam epitaxy (MBE) more commonly used for Esaki diodes. Unlike CVD, MBE processes are rare in mainstream CMOS production.

The trenches used were 250nm wide, made in a 490nm layer of thermal oxide grown on the silicon wafer. Reduced-pressure chemical vapor deposition (RPCVD) was then used to grow a germanium layer. Defects caused by the Si/Ge lattice mismatch are trapped by the oxide trench side walls. The final Ge layer is relatively thin (825nm) compared with the microns of Ge resulting from techniques normally used to deposit Ge on Si. The rough surface resulting from the coalescence of the Ge from the various trenches is planarized using chemical mechanical polishing (CMP), a standard technique in CMOS processing.

The layer structure of the Esaki diodes reported was n^+GaAs/n^+InGaAs/p^+GaAs with different combinations of parameters. A structure of 50nm n-GaAs (Si-doped > $9\times10^{18}/cm^3$), 10nm n-$In_{0.1}Ga_{0.9}As$ (Si $9X10^{18}/cm^3$) and, finally, 80nm of p-$In0_{.1}Ga_{0.9}As$ (carbon-doped $5X10^{18}/cm^3$) gave the 56 PVCR and a peak current of $250A/cm^2$ (Figure 7). An alternative structure — 50nm n-GaAs (Si > $9\times10^{18}/cm^3$), 10nm n-$In_{0.2}Ga_{0.8}As$ (Si $9\times10^{18}/cm^3$) and, finally, 80nm p-GaAs (C $5\times10^{18}/cm^3$) gave a higher peak current of $1000A/cm^2$ but with a lower PVCR of 43.

Kim and Del Alamo of MIT have pushed InAs pseudomorphic HEMT (pHEMT) performance to more than 600GHz, which is usually the territory of InP or SiGe HBTs [8]. The 30nm device (Figure 8) operates in enhancement mode (normally-off). A gate sinking process effectively thins the barrier layer, which consists of $In_{0.52}Al_{0.48}As$ material. The gate length is scalable from 130nm down to 30nm.

The f_T/f_{max} combination of 601/609GHz is said to be record breaking (V_{DS} = 0.5V). The source injection velocity is estimated at 2.5×10^7cm/s, a factor of two higher than state-of-the-art Si MOSFETs. This velocity

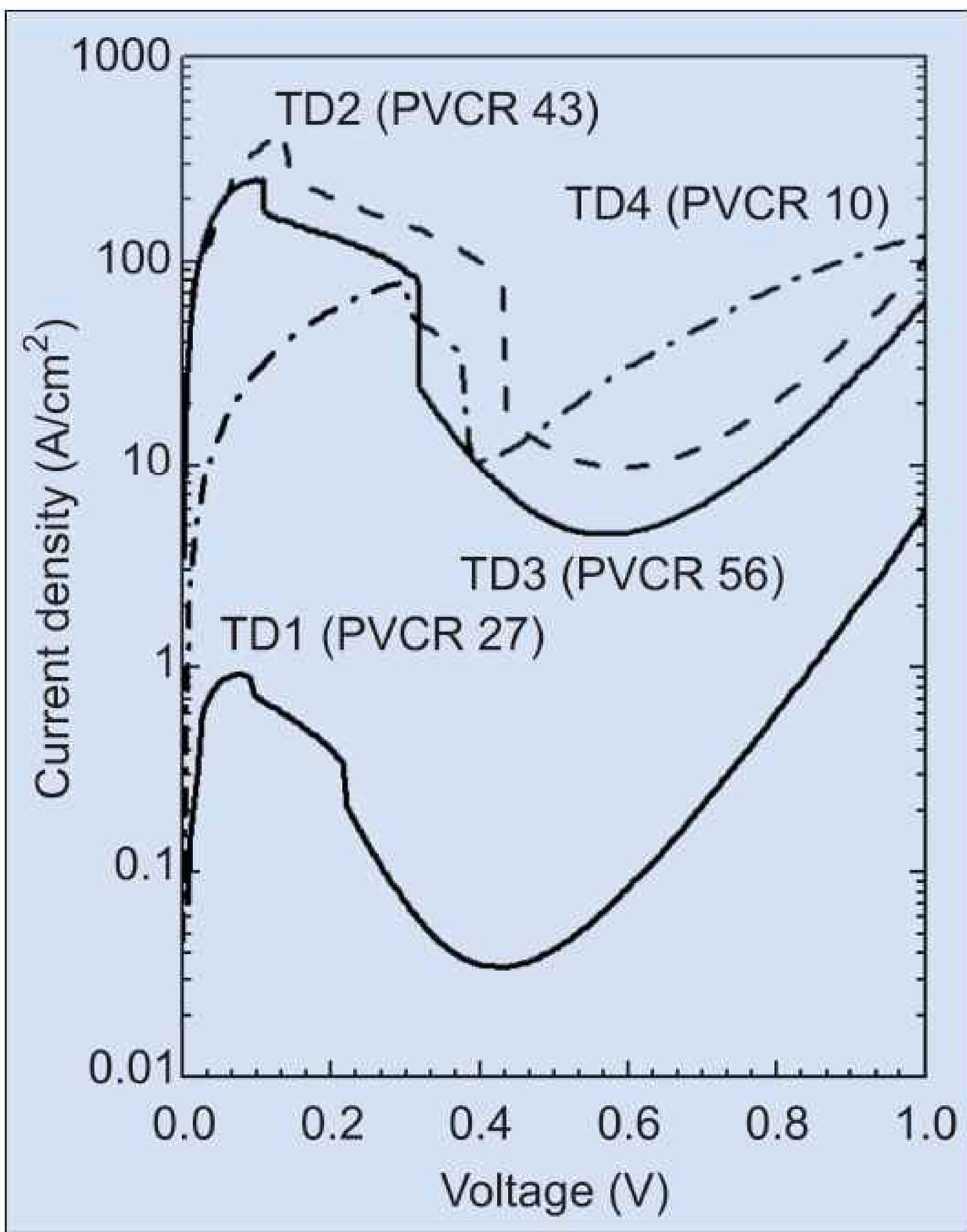

Figure 7. I-V characteristics for different InGaAs Esaki diodes built on ART germanium on silicon substrate. TD3 has the highest PVCR of 56.

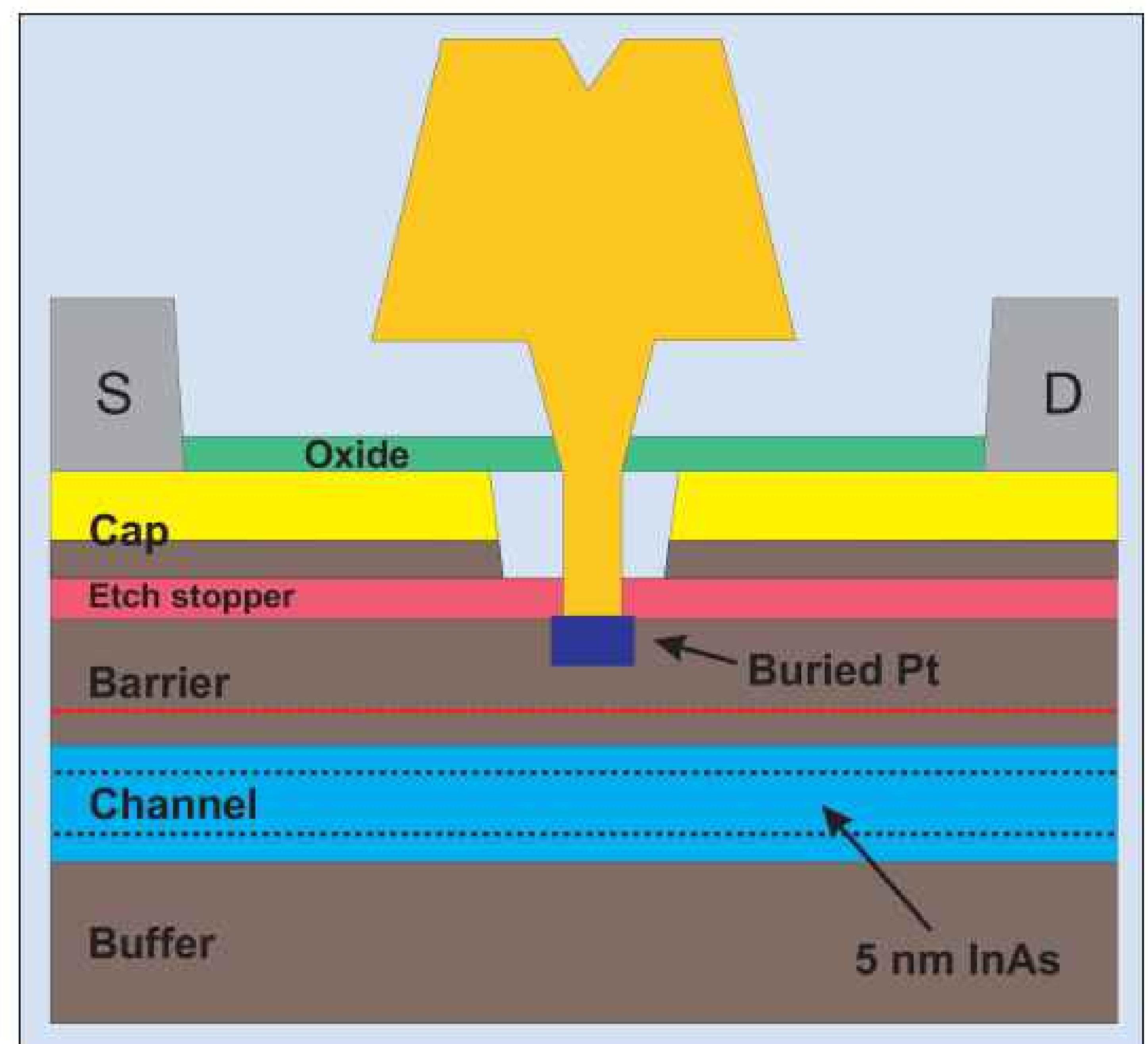

Figure 8. Schematic of MIT's InAs pHEMT.

meets the requirements of the International Technology Roadmap for Semiconductors (ITRS) for devices at 10nm. The device has been carefully designed to deliver 'outstanding' THz frequency and logic performance at short channel lengths.

InP on Si RF-CMOS fusion

Finally, researchers from HRL Laboratories have integrated entire wafers of high-performance 250nm, 300GHz f_T/f_{max} InP double-heterostructure bipolar transistors (DHBTs) with wafers from IBM's CMRF8SF 130nm RF-CMOS technology [9]. For handling purposes, the full-thickness InP 76.2mm or 100mm epitaxial wafer is first temporarily bonded to a handle wafer. This allows the InP growth substrate and etch-stop layers to be removed. An aluminum heat-spreader layer is deposited as a blanket film. The InP DHBT layers are then permanently bonded to the IBM CMOS wafer's top surface. In tests, the CMOS transistors showed no sign of degradation, while the InP transistors showed only minor performance impacts. ■

References

[1] Chen et al, IEDM 2008, Session 6.4, 'Monolithic Integration of Lateral Field-Effect Rectifier with Normally-off HEMT for GaN-on-Si Switch-mode Power Supply Converters'
[2] Wang et al, Session 6.6, 'Source Injection Induced Off-State Breakdown and Its Improvement by Enhanced Back Barrier with Fluorine Ion Implantation in AlGaN/GaN HEMTs'
[3] Ishida et al, Session 6.5, 'GaN-based Natural Super Junction Diodes'
[4] Joh and del Alamo, Session 19.3 'Impact Of Electrical Degradation On Trapping Characteristics Of GaN High Electron Mobility Transistors'
[5] Meneghini et al, Session 19.6, 'Role Of Non-Radiative Recombination In The Degradation Of InGaN-Based Laser Diodes'
[6] Lau et al, Session 30.2, 'AlInAs/GaInAs mHEMTs on Silicon Substrates by MOCVD'
[7] Rommel et al, Session 30.6, 'Record PVCR GaAs-based Tunnel Diodes Fabricated on Si Substrates using Aspect Ratio Trapping'
[8] Kim and del Alamo, Session 30.1, '30nm E-mode InAs PHEMTs for THz and Future Logic Applications'
[9] Li et al, Session 30.7, 'Heterogeneous Wafer-Scale Integration of 250nm, 300GHz InP DHBTs with a 130nm RF-CMOS Technology'

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