

Power, speed and other highlights at IEDM

Mike Cooke rounds up developments reported at December's 2010 IEEE International Electron Devices Meeting (IEDM) in San Francisco.

The past few years have seen growing interest in using nitride semiconductors as components in power systems. The wide bandgaps ($> 3.4\text{eV}$) of gallium nitride (GaN) and aluminum gallium nitride (AlGaN) mean that the breakdown electric field is large compared with more traditional semiconductors such as silicon (Si) or gallium arsenide (GaAs). The wider bandgap also allows such devices to maintain their performance characteristics to higher temperatures.

The 2010 International Electron Devices Meeting (IEDM) in early December had a special focus on power electronics, where gallium nitride technologies were to the fore. The themes of these presentations were energy efficiency and supply for green technologies.

Session 13 was titled 'Emerging Technologies — Next Generation Power Devices and Technology', while 'Advanced Power Devices and Reliability' from the perspective of quantum and compound semiconductor technology was also the topic of session 20.

The earlier of these sessions was concerned mainly with sifting through potential applications and matching them to suitable potential technologies. Applications include battery control (e.g. switching and charging), motors (e.g. in hybrid electric vehicles, industrial processes etc), renewable energy distribution into the electric grid, etc.

For many of these uses, silicon is the favored option due to its long development and low cost. However, some companies such as Toyota [session 13.5] and consultant Dr Michael A. Briere of ACOO Enterprises LLC [13.6] see potential for the application of GaN and silicon carbide (SiC) to automotive, and even voltage regulator modules for multi-processor CPU power control. Some key features of these devices are higher power efficiencies and higher power densities. High temperature operation is also a useful factor and is of much interest for aerospace applications, as well as automotive and electric grid applications.

Toyota is a leading producer of hybrid electric vehicles, known internationally for its Prius range, which the US Environmental Protection Agency has determined is the most fuel-efficient gasoline car sold in the USA (achieving 51 miles per gallon in cities, according to

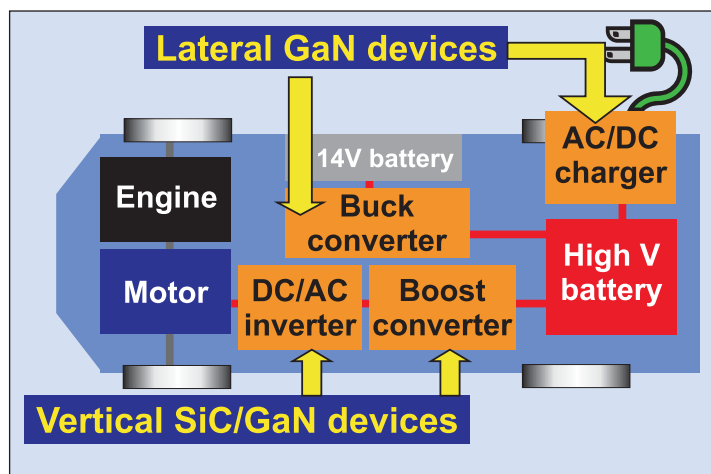


Figure 1. Prospect of SiC/GaN application in future plug-in hybrid electric vehicles, according to Toyota researchers. The lateral power switch devices may need to be bidirectional (for AC/AC matrix conversion) or high frequency (for buck).

	vertical	lateral
structure		
cost	high	low (on Si)
speed	relative high	high
main issues	quality of sub. etc.	current collapse etc.
power	high ($>10\text{kW}$)	middle ($\sim\text{kW}$)
application	inverter etc.	bi-directional sw. high-f converter.

Figure 2. Relative merits of vertical and lateral structures for GaN transistors, according to Toyota researchers.

www.fueleconomy.gov/feg/best/bestworstNF.shtml). The company sees improved economy being made available by the introduction of silicon carbide and/or gallium nitride power devices in inverters, boost and buck converters, and for AC/DC charger units (Figure 1). Vertical devices (Figure 2) are preferred for the higher-power applications (inverter, boost converter), but are

more costly to produce. Lateral devices can be manufactured on silicon, reducing costs, but are restricted to mid-range powers that are acceptable for AC/DC chargers and buck converters.

Session 20 reported actual structures and technologies for high-power/voltage operation, mainly in nitride semiconductors, but also with some silicon technology. Some of the nitride research is aimed at characterizing traps that can impact performance [Ohio State University, Wright Patterson Air Force Base, Wyle Labs, 20.1], or looking for degradation mechanisms [MIT, 20.2; IMEC, University of Padova, 20.3; Hong Kong University of Science and Technology, Nitronex, 20.4] of nitride high-electron-mobility transistors (HEMTs).

MIT found that RF stress created more degradation compared with a comparable DC voltage. IMEC and Padova applied for the first time the time-dependent dielectric breakdown (TDDB) technique that is used in CMOS reliability assessments to give lifetime extrapolations.

HKUST et al reported the on-state reliability of HEMTs that were treated with fluorine plasma to shift the threshold voltage to 'enhancement mode', i.e. normally-off operation, which is desirable for lower power consumption. A critical voltage was found that seemed to be caused by impact ionization of the fluorine ions in the barrier layer.

Also, new high-power device structures were presented such as Panasonic's new method to increase the blocking voltage of GaN power switching transistors on silicon substrates to 2200V [20.5; see Semiconductor Today news at www.semiconductor-today.com/news_items/2010/DEC/PANASONIC_081210.htm]. The method consists of putting selectively formed p-type regions on the surface of the Si substrate to block electron current flows that occur at the interface between the GaN and Si layers of the device. This allows the Si to also contribute to the blocking voltage. The 2200V blocking voltage is about five times that achieved by usual GaN power transistors grown on silicon substrates. The researchers believe that increasing the thickness of the epitaxial nitride semiconductor structures could increase blocking to 3000V.

Panasonic says that the new GaN transistor extends the operating voltages of a variety of power switching systems including inverters for industrial use and uninterruptible power supplies. The company has filed applications for 99 domestic and 64 overseas patents on the technology.

In the same section, North Carolina State University and Nitronex presented a normally-off nitride semiconductor transistor that included a silicon dioxide (SiO_2) gate tunnel dielectric and tantalum nitride (TaN) floating gate layers [20.6]. The structure (Figure 3) is described as being a metal-oxide-semiconductor-heterostructure field-effect transistor (MOS-HFET). The channel layer

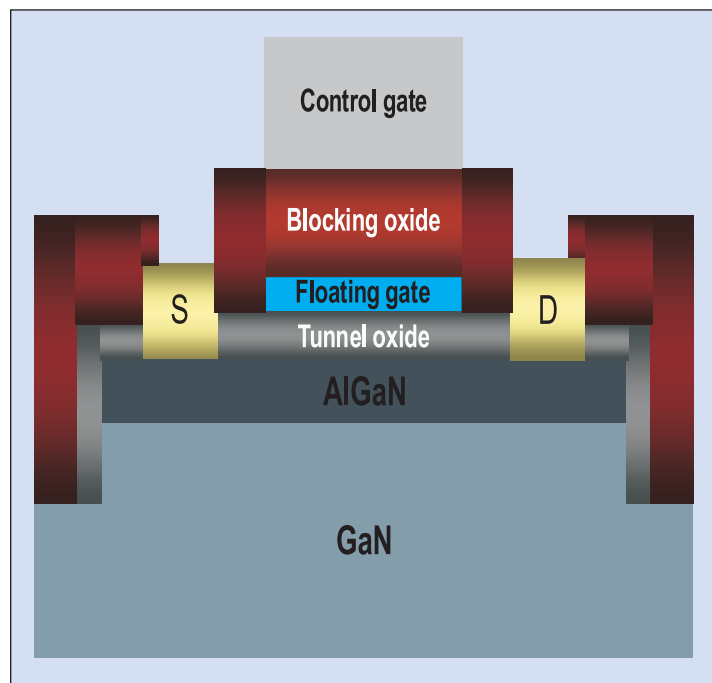


Figure 3. Schematic NCSU nitride semiconductor MOS-HFET.

was GaN and the barrier was AlGaN (26% Al).

The enhancement-mode operation is achieved by injecting charge into the floating gate (rather like in Flash memory devices), shifting the threshold voltage. In fact, a floating gate stack of SiO_2 (tunnel oxide)/TaN/HAH (blocking oxide), where $\text{HAH} = \text{HfO}_2/\text{Al}_2\text{O}_3/\text{HfO}_2$, entered enhancement mode after a 15V pulse for 500ms. The charge retention of the floating gate was such that less than 10% was lost after 10,000 seconds. Threshold voltage shifts of up to 6V were achieved, representing a charge density in the floating gate of $1.2 \times 10^{13}/\text{cm}^2$.

One would normally expect a nitride HFET/HEMT to be depletion mode (normally-on) and that adding insulation to reduce gate leakage (MOS-HFET) would shift the threshold in a negative direction, making the device harder to turn off and putting it further from enhancement behavior.

Although a floating gate structure had been suggested previously as a way to shift thresholds to enhancement mode in nitride HEMTs, this had not been experimentally demonstrated before. A combination of atomic layer deposition and RF magnetron sputtering (floating gate) was used to create the stack.

Compounding digital performance

Digital devices built in compound semiconductor material continue to be of interest, particularly as a possible means of overcoming the increasing problems of developing traditional complementary metal oxide semiconductor (CMOS) silicon technology that controls most consumer electronics today.

The main material here is indium gallium arsenide (InGaAs). For example, Intel and epitaxial wafer

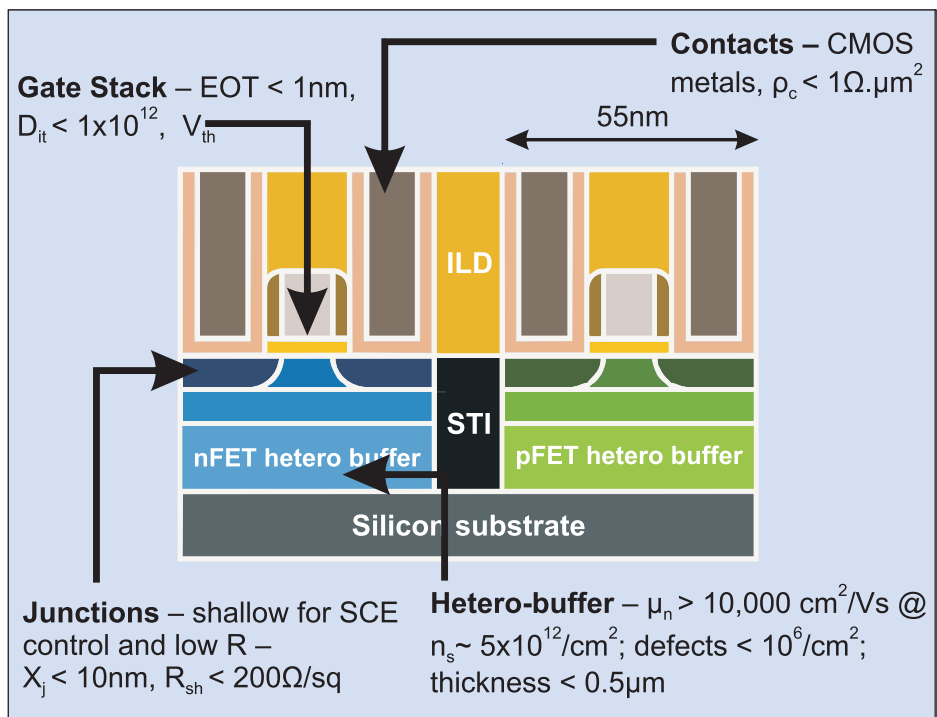


Figure 4. Module targets for III-V at 11nm and below. SEMATECH’s process meets the targets for contact (1Ω-cm²) and junction (100Ω/sq) resistance, and for junction depth (10nm). However, work is needed on interface trap density (D_{it}), nFET hetero buffer mobility (μ_{nr}, 8900cm²/V-s) and buffer thickness (1.4μm).

producer IQE last year developed an InGaAs FinFET (i.e. a long thin channel with a wrap-around gate). The advantage of InGaAs is a higher mobility than silicon. Intel/IQE research in 2010 has improved the device structure with a fin that was 35nm wide and reduced the gate-source and gate-drain distances to 5nm. The researchers claim ‘more enhancement-mode threshold voltage and significantly improved electrostatics’ from their new device.

Meanwhile [3.1], the University of Tokyo, working with Japan’s National Institute of Advanced Industrial Science and Technology (NAIST) and Sumitomo Chemical,

produced ultra-thin InGaAs-on-insulator MOSFETs using direct wafer bonding techniques (i.e. the layers are grown on another substrate and transferred to a silicon wafer for further processing such as wiring, etc.). The insulator consisted of a buried aluminum oxide layer. The thickness of the InGaAs channel was 3.5nm and that of the oxide was 9nm. Using a double gate, the on/off current ratio was 10⁷.

The US-based SEMATECH industry consortium produced self-aligned III-V MOSFETs on 200mm silicon wafers using standard silicon industry tools for the first time [6.2]. The gate length was 0.5μm (500nm, rather than the tens of nanometers used by present-day CMOS). The maximum external transconductance (g_{m,ext}) was 1005μS/μm and the on-current was 1μA/μm at 1V operating voltage. The researchers comment: ‘We present statistically significant data demonstrating that III-V on Si devices can be processed on a Si line with controlled contamination, uniformity and yield while demonstrating good device

performance.’ The team is targeting the introduction of III-V devices with critical features around 11nm (Figure 4).

III-V MOSFETs tend to be n-MOS. For CMOS circuitry, one also needs p-MOS. Generally, it is expected that these devices will be provided by germanium channels. However, Stanford University, Stanford Linear Accelerator Center, and the Naval Research Lab reported on indium gallium antimonide (InGaSb) devices that had 100% (910cm²/V-s) improved buried mobility for holes, compared with germanium, over the entire sheet charge range [6.4]. The surface mobility was 50% better

(620cm²/V-s). The researchers produced transistors with on-off current ratios of 10⁴ with a subthreshold slope (SS) of 120mV/dec. The SS is desired to be as close as possible to the 60mV/dec limit at room temperature (log(10)kT/q) for a sharp turn-on. Various devices were produced to optimize hole transport, using aluminum oxide gate insulation in a self-aligned gate-first process (Figure 5).

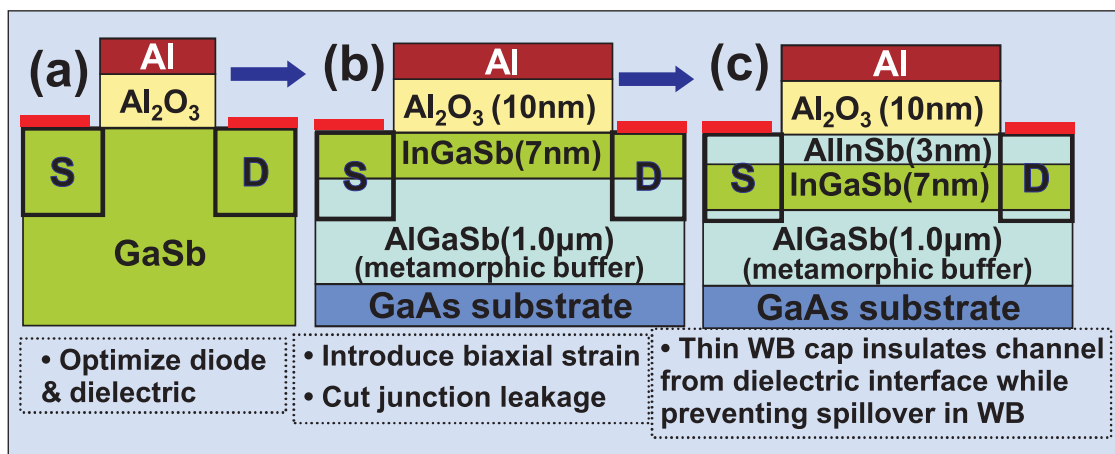


Figure 5. Different channel designs to separate the impact of different issues and enhance transistor performance. Top surface is terminated with two monolayers of GaSb in each case to maintain high-quality interface with Al₂O₃. WB = wide bandgap.

Support for the research came from Office of Naval Research and Intel.

Quantum well devices are also being developed to incorporate III-Vs into silicon. On the n-side, Pennsylvania State University, Naval Research Lab, and Israel Institute of Technology University have worked with $\text{InAs}_{0.8}\text{Sb}_{0.2}$ wells to produce a drive current of $380\mu\text{A}/\mu\text{m}$ at 0.5V [6.3]. A high-k gate stack consisted of 3.3nm of aluminum oxide and 1nm GaSb, giving an equivalent oxide thickness of 4.2nm. Intel has worked on p-type QWFETs with a strained germanium channel and an EOT (equivalent oxide thickness) of 1.5nm [6.7]. The hole mobility ($770\text{cm}^2/\text{V}\cdot\text{s}$ at sheet carrier density of $5 \times 10^{12}/\text{cm}^2$) was found to be four times that of standard strained silicon. The researchers comment: 'This suggests the Ge QWFET is a viable p-channel option for III-V CMOS.'

Speedsters

More traditional III-V transistors were also presented, targeting and achieving frequency characteristics up to 1 terahertz ($1000\text{GHz} = 1\text{THz}$). Such devices are of interest for millimeter and sub-millimeter radio wave transmissions used for defense and communications, e.g. for signal generation/detection and high-power amplification (GaN or SiC) at high frequency.

The highest characteristic of 1THz was for the maximum oscillation frequency of a 50nm gate-length enhancement-mode $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ pseudomorphic HEMT on 100mm InP substrate, produced by Teledyne Scientific (with Jesús del Alamo of MIT) [30.6]. According to the researchers, this is the first demonstration of such a performance for enhancement-mode PHEMTs. To establish this result the researchers had to understand some abnormal peaky behavior that could have led to over-estimation of f_{max} .

A platinum gate-sinking process was used to reduce the effective gate-channel distance and to shift the threshold to positive values for enhancement-mode (normally-off) behavior. The transconductance was $1.7\text{S}/\text{mm}$ at 0.75V 1THz input. The subthreshold region was 'very sharp', with a swing of $80\text{mV}/\text{dec}$ and drain-induced barrier lowering of $80\text{mV}/\text{V}$. The $1\text{mA}/\text{mm}$ current turn-on voltage was more than 0.5V.

In a related presentation, MIT separately reported on its work with 60nm self-aligned-gate InGaAs HEMTs

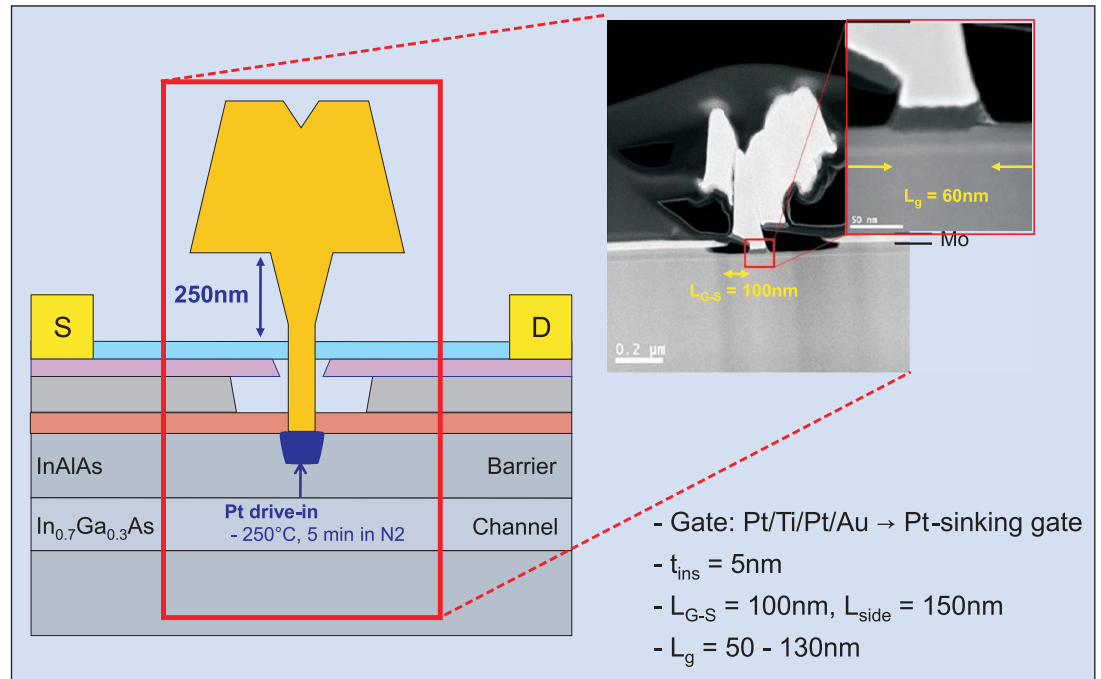


Figure 6. Cross-section of MIT device structure.

(Figure 6) with a cut-off (f_{T}) of 580GHz and maximum oscillation (f_{max}) of 675GHz [30.7]. This was achieved using a molybdenum-based self-aligned gate process (Figure 7) that 'yields outstanding contact resistance,

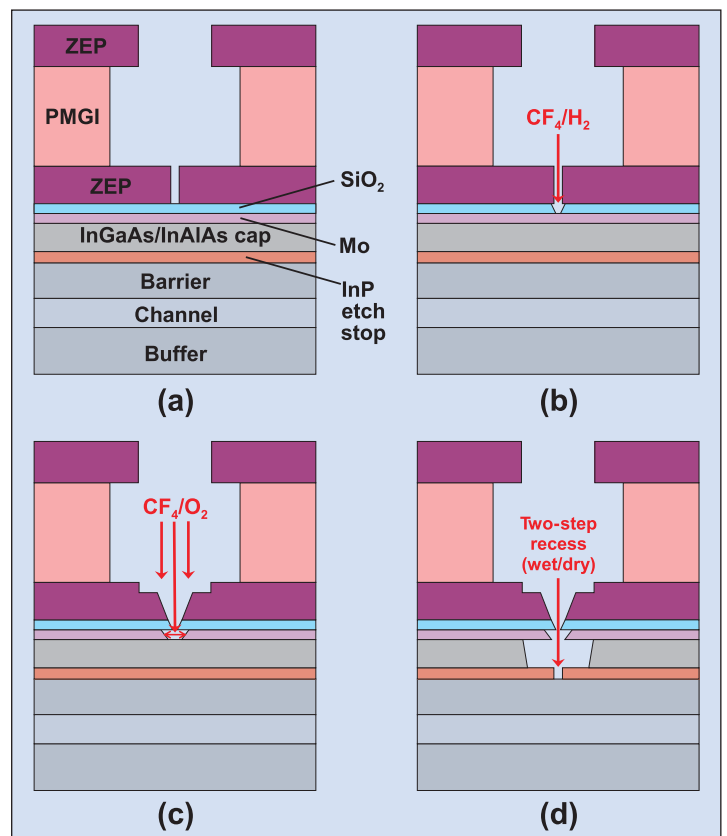


Figure 7. Process flow for self-aligned gate (SAG) structure: (a) double electron-beam exposure/development of photoresist; (b) silicon dioxide etch; (c) molybdenum lateral etch; (d) two-step citric acid solution/argon plasma etches to expose barrier.

source resistance, transconductance and high-frequency characteristics'. Many of the measured values were records, or near the record value.

The purpose of using non-alloyed molybdenum is to create ohmic source-drain contacts with low parasitic resistance and capacitance, allowing high-frequency operation. One important feature of reducing the parasitic characteristics is to shrink the footprint of InGaAs devices from the typical micron-scale needed for contacts and $\sim 100\text{nm}$ separation distance from the gate. The transconductance was $2.1\text{mS}/\mu\text{m}$ at a source-drain voltage of 0.5V . The work was part sponsored by Intel.

For GaN HEMT performance, a speed record beyond 400GHz has been achieved by HRL Laboratories with NASA's Jet Propulsion Laboratory [30.1]. A double heterostructure with barriers above and below the GaN well (AlN/GaN/AlGaIn) was used. The gate length was 40nm . The cut-off frequency was 220GHz and the maximum oscillation was 440GHz . Silicon carbide substrates were used. To improve the ohmic contact with the source and drain regions of the device, a re-growth process involving molecular beam epitaxy (MBE) was used.

Further nitride semiconductor HEMT developments were reported by MIT Microsystems Technology Laboratories [30.2], and by University of Notre Dame, TriQuint Semiconductor, and IQE RF LLC [30.4]. The MIT group has developed a gate recess/oxygen plasma treatment to reduce collapse effects in terms of transconductance, enabling an f_T of 225GHz . Notre Dame et al produced 144nm gate enhancement-mode and depletion-mode devices on the same wafer, producing ring oscillators with a $15.3\text{psec}/\text{stage}$ delay.

GaN nanowires transistors also made a showing, with National Taiwan University presenting a depletion-mode device that operated at 100GHz [30.3]. The channel consisted of the two-dimensional electron gas formed at the interface with a gallium oxide (Ga_2O_3) nanowire region.

AlGaIn/GaN MOS-HEMTs have also been produced for the first time in research in Singapore [11.3], by the University of Singapore (NUS), the Institute of Materials Research and Engineering, and the Data Storage Institute. The device used a diamond-like carbon (DLC) liner with high compressive stress to enhance the performance, increasing saturation currents by up to 30% at 10V (gate at 2V). Peak transconductance was increased by 22% at 5V by using the DLC liner. The gate lengths of the devices were less than 500nm . The researchers believe that the shift of the threshold by 1V in the positive direction suggests the potential of strain engineering for achieving enhancement-mode operation.

High-speed electronics was not exclusively the preserve of III-V devices at IEDM. IHP — Innovations for High Performance Microelectronics (Leibniz-Institut für innovative Mikroelektronik) presented a silicon germanium heterojunction bipolar transistor with f_T/f_{max} of

$300\text{GHz}/500\text{GHz}$, a breakdown voltage of 1.6V , and 2psec minimum CML ring oscillator gate delay [30.5]. The researchers attribute these improved results over previous SiGe HBTs to 'reduced specific collector-base capacitance and base resistance and scaling of device dimensions'.

Light handlers

Another area where III-Vs tend to dominate is light-emitting devices. At IEDM, Dartmouth College and MIT reported lasers created through band engineering germanium on silicon (both group IV elements). These group IV materials normally have indirect bandgaps that make light emission difficult. By compensating the energy difference between the direct and indirect bandgaps, Dartmouth-MIT created laser emission at $1590\text{--}1610\text{nm}$ wavelengths using optical pumping (i.e. energy is delivered into the device through an external light source). However, the researchers also report direct-gap electroluminescence from Ge/Si heterojunction diodes, indicating that electrical pumping is at least possible. The wavelength range was $1450\text{--}1650\text{nm}$ at room temperature. In combination with traditional CMOS, the light emitters could be a 'desirable choice for monolithic electronic-photonic integrated circuits'.

In the light-detection arena, European researcher center IMEC, France's CRHEA-CNRS, and the Royal Observatory of Belgium presented an AlGaIn-on-silicon imager to detect extreme ultraviolet radiation (EUV) [14.5]. The detectors have a wavelength cut-off of 280nm from using AlGaIn with 40% Al, giving a 4.2eV bandgap; the device is thus intrinsically blind to wavelengths longer than this. An array of such detectors was formed into a 256×256 -pixel focal plane array with a $10\mu\text{m}$ pixel-to-pixel pitch. The device also contains $0.35\mu\text{m}$ CMOS read-out circuitry to which the AlGaIn on Si detectors are flip-chip bonded. The nitride material was deposited using MBE.

The structure of the device is such that the illumination came through the 'back-side' — i.e. through the locally thinned silicon wafer. The sensitivity of the device down to a wavelength of 1nm was verified using synchrotron radiation.

Ultraviolet detection is of particular interest for solar science, EUV microscopy and advanced EUV lithography tools. In fact, the devices were produced within the framework of the BOLD project of the European Space Agency [<http://bold.sidc.be/-BOLD-GSTP-AlGaIn-.htm>]. The ultimate aim is to produce 1000×1000 -pixel arrays for use on future solar missions.

The use of the wide-bandgap nitride semiconductor AlGaIn makes the devices more rugged in terms of UV damage compared with devices using silicon. Also, such devices do not need filters to block the visible and infrared radiation that is needed for 'solar blindness'. ■

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