

A Micro-Power EEG Acquisition SoC With Integrated Feature Extraction Processor for a Chronic Seizure Detection System

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Abstract—This paper presents a low-power SoC that performs EEG acquisition and feature extraction required for continuous detection of seizure onset in epilepsy patients. The SoC corresponds to one EEG channel, and, depending on the patient, up to 18 channels may be worn to detect seizures as part of a chronic treatment system. The SoC integrates an instrumentation amplifier, ADC, and digital processor that streams features-vectors to a central device where seizure detection is performed via a machine-learning classifier. The instrumentation-amplifier uses chopper-stabilization in a topology that achieves high input-impedance and rejects large electrode-offsets while operating at 1 V; the ADC employs power-gating for low energy-per-conversion while using static-biasing for comparator precision; the EEG feature extraction processor employs low-power hardware whose parameters are determined through validation via patient data. The integration of sensing and local processing lowers system power by 14x by reducing the rate of wireless EEG data transmission. Feature vectors are derived at a rate of 0.5 Hz, and the complete one-channel SoC operates from a 1 V supply, consuming 9 μ J per feature vector.

Index Terms—1/f noise, algorithm design and analysis, amplifiers, biomedical equipment, brain, choppers, digital signal processing, electroencephalography, low-noise amplifiers, low-power electronics.

I. INTRODUCTION

RECENTLY therapeutic and prosthetic devices have begun emerging that hold great promise for the treatment of patients with neurological conditions ranging from epilepsy [1], Parkinson's disease [2], narcolepsy [3], depression [4], and motor impairments [5]. The ability to acquire targeted neurological information from the brain is an essential requirement to the advancement of these systems. This implies the need to sense neural signals but, more critically, to use these in order to establish correlation with the actual clinical states of interest.

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Brain monitoring thus introduces key challenges for electronic systems in terms of both instrumentation and information extraction.

Seizure detection in epilepsy patients is an important application that is representative of the challenges. This paper describes the details of an SoC that performs feature extraction from an analog EEG channel into the digital domain; the output is used to detect the onset of seizures by way of a machine-learning classifier that is trained to patient-specific data. EEG sensing is targeted so that the system is noninvasive. This implies that microvolt signals must be acquired from electrodes having very poor output impedance while in the presence of numerous physiological and environmental interferences (e.g., EMG, hum, etc.). Further, for reliable detection, subtle patient-specific EEG signal correlations must be determined over multiple channels (up to 18). The following sections start by describing the opportunity and algorithm approach for patient-specific seizure detection. Then, the SoC is described from both the system perspective and the IC implementation perspective. Finally, IC results are described, followed by a system demonstration and conclusions.

II. EPILEPSY AND SEIZURE DETECTION

Epilepsy is a neurological disorder that causes a recurring abnormal firing in groups of neurons. As a result patients experience seizures causing loss of coherence/cognition, loss of motor control, involuntary motion (convulsions), and possibly even death. Fig. 1 shows PET scan images highlighting a particular firing pattern that is associated with seizures (ictal period) in the considered patient. The EEG during a seizure onset is also shown. Although EEG has the benefit that it is noninvasive, its correlation with seizures is complicated by the attenuation, 1/f filtering, and spatial aliasing of the neural field potentials across the skull and skin. Nonetheless, taking the recording in Fig. 1 as an example, approximately 7.5 sec before the start of clinical symptoms, a subtle but characteristic change in the EEG can be observed. If this electrical onset can be detected, an advanced signal can be generated to warn the patient and caregivers, actuate a therapeutic stimulator (e.g., [6], [7]), or trigger EEG data storage for analysis by a neurologist.

Although the critical variances in the electrical onset are minute and variable from patient to patient, [8] shows that seizures are stereotypical for a given patient. Machine learning can thus be used to train a classifier on a patient-by-patient

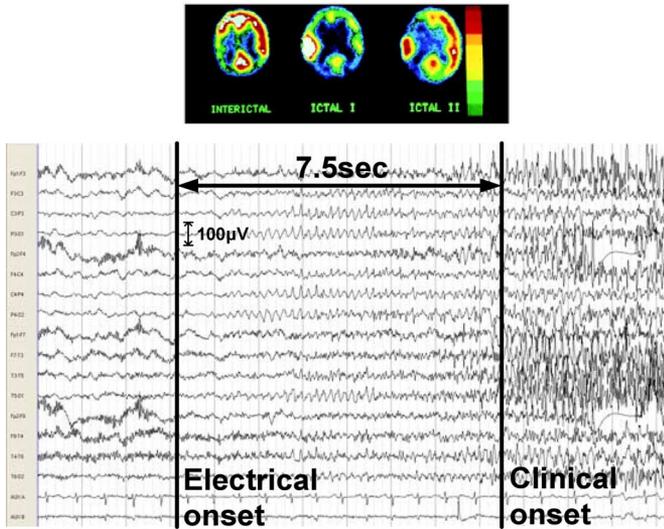


Fig. 1. 18-channel EEG showing onset of patient seizure (ictal); electrical onset occurs 7.5 sec before the clinical onset, which is characterized by muscle reflexes causing the large excursion artifacts.

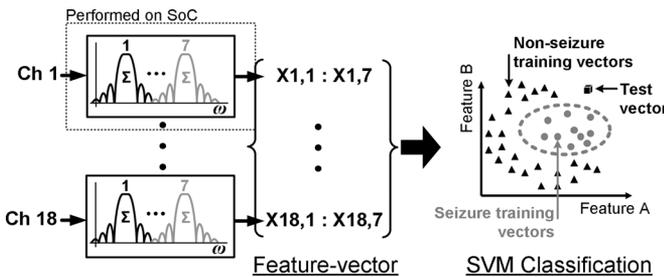


Fig. 2. Seizure detection algorithm employing spectral analysis feature extraction and SVM classification.

basis, thereby simultaneously improving sensitivity and specificity of detection. The following subsection briefly describes the approach and parameters used in this system.

A. Seizure Detection Algorithm

Fig. 2 illustrates the detection algorithm. First, the EEG channels are processed to extract specific bio-markers that are relevant for seizure detection. Clinical studies have determined that seizure onset information is contained in the spectral energy distribution of the patient’s EEG [9]. Accordingly, in this SoC the spectral energy of each channel is extracted to seven frequency bins over a two second window in order to form a feature vector. Up to 18 channels may be used, resulting in a complete feature vector of up to 126 dimensions.

In order to distinguish between seizure and non-seizure EEG, machine learning is introduced through the use of a support-vector machine (SVM) classifier. The classifier must first be trained by providing it feature vectors that are labeled as corresponding to seizure or non-seizure. These are used to establish an optimal decision boundary between the two cases. Accordingly, for real-time seizure detection, incoming test feature vectors are conceptually plotted (as illustrated in Fig. 2) to determine where they lie with respect to the decision boundary. The SVM radial-basis kernel is used for the classification computation (a description of the kernel can be found in [10]).

The algorithm was validated through tests on 536 hours of data over 16 patients. Ref. [8] shows that the approach of patient-specific learning simultaneously improves sensitivity, specificity, and latency (the values achieved are 93%, 0.3 ± 0.7 false alarms/hour, and 6.7 ± 3 seconds, respectively).

III. CONTINUOUS MONITORING AND DETECTION APPROACH

The physical partitioning and form-factor of the system have important implications to patient usability, power consumption, and robustness. For instance, EEG sensing must be distributed around the scalp in order to acquire spatial channels, but SVM classification (over the multidimensional feature vector) must be centralized. As a result, the intermediate instrumentation, computation, and communication tradeoffs determine the appropriate system topology. Further, a critical application consideration is that, for chronic seizure detection, no cables can originate from the scalp, since these pose a strangulation hazard in the case where the patient begins convulsing. Accordingly, some form of wireless transmission from the scalp is essential.

For sensing robustness, the acquisition circuitry (e.g., instrumentation amplifier and ADC) is kept as close to the electrodes as possible to mitigate EMI and mechanical disturbance on wires carrying the microvolt EEG signals. As a result, the instrumentation amplifier (and, to a lesser extent, also the ADC) must be distributed along with each electrode.

The digitized EEG recordings can be robustly transmitted (i.e., wireless EEG) for central processing. However, local processing is beneficial for minimizing communication cost. In Table I, the system power for wireless EEG (where both feature vector extraction and SVM classification are performed remotely) is compared to that with local processing (where feature vector extraction is performed locally and only SVM classification is performed remotely). The power numbers are based on actual measurements of the hardware prototype assuming 18 EEG channels. The radio used is a commercially available low-power transmitter, ChipCon CC2550 [11], and its power consumption is for duty-cycled operation at the required data-rates (including idle, start-up, and active transmission modes). By performing local processing to extract the feature vectors for transmission, the radio data-rate is reduced by a factor of over 40 compared to complete wireless EEG transmission. Through this computation-versus-communication tradeoff, local processing reduces the total system power on the scalp by a factor of 14 for the radio considered. Although other custom ultra-low-power radios have been reported [12], [13], their use in this system requires consideration of synchronization overhead, which leads to additional power consumption.

Fig. 3 shows the block diagram of the SoC. It integrates an instrumentation amplifier (I-amp), ADC, feature extraction processor, and low-power parallel–serial interface for feature vector streaming. Each SoC outputs a one-channel feature vector, and for multiple channels, all node outputs are wired to a central radio (also on the scalp) so that the feature vectors can be concatenated and transmitted.

In this system, SVM classification could also have been performed locally. However, without specialized hardware, the SVM computation significantly raises the system power

TABLE I
POWER COMPARISON BASED ON HARDWARE MEASUREMENTS OF WIRELESS EEG AND LOCAL FEATURE EXTRACTION SYSTEMS

	Wireless EEG	Local feature-extraction
I-Amp array	72 μW	72 μW
ADCs (12b, 11kS/s)	3 μW	3 μW
Digital processors	-	2.1 μW
Radio (CC2550) [11]	1733 μW	43 μW
-Active: $bit\text{-}rate * 40nJ/bit$	-Active: $43.2kpbs*40nJ/bit$	-Active: $2kpbs/2sec*40nJ/bit$
-Start-up: $4.8\mu W$	-Start-up: $4.8\mu W$	-Start-up: $4.8\mu W/2sec$
-Idle mode: $0.46\mu W$	-Idle mode: $0.46\mu W$	-Idle mode: $0.46\mu W/2sec$
Total	1808 μW	120 μW

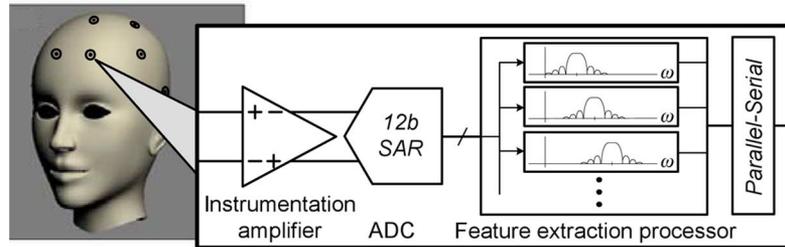


Fig. 3. SoC block diagram. Each chip corresponds to one EEG channel and is placed near the associated electrode.

consumption on the scalp, where battery size and weight limitations are the most severe. Although this further reduces the communication load to a single classification result, additional data-rate reduction is not essential since the radio power no longer dominates.

Promising computational approximations for low-power SVM classification are currently being investigated [14]. Such approximations can also be leveraged in this system, since they can be applied to the spectral feature vectors.

IV. FEATURE-EXTRACTION SOC

The circuit and architecture details of the major SoC components are described in the following sections.

A. Instrumentation Amplifier

The I-amp must amplify $10\text{--}50\ \mu\text{V}$ EEG signals from the passive scalp electrodes, and in doing so, faces the instrumentation challenges summarized in Fig. 4. First among these is electrode interfacing; Ag/AgCl electrodes and electrolyte gels are commonly used to contact the scalp since these are inexpensive and commercially available. The typical circuit model used for such electrodes is shown. The electrode offset voltage (EOV) can be large (i.e., $10\text{--}100\ \text{mV}$), and it arises from charge accumulation due to chemical interaction between the metal and gel. R_S , which comes about from conduction through the electrolyte, may be on the order of $2\ \text{k}\Omega$, while R_P and C_P , which come about from the skin, can be on the order of $2\ \text{M}\Omega$ and $50\ \text{nF}$, respectively [15]. To avoid severe signal attenuation, the input impedance of the I-amp must have much larger resistive component and much smaller capacitive component than this. Second, common-mode rejection is critical to 1) avoid coupling to environmental EMI and 2) avoid interference from extraneous electrical activity on the skin (e.g., EMG, baseline EEG, etc.). Third, $1/f$ noise falls within the EEG signal band, and it must be avoided through chopper stabilization.

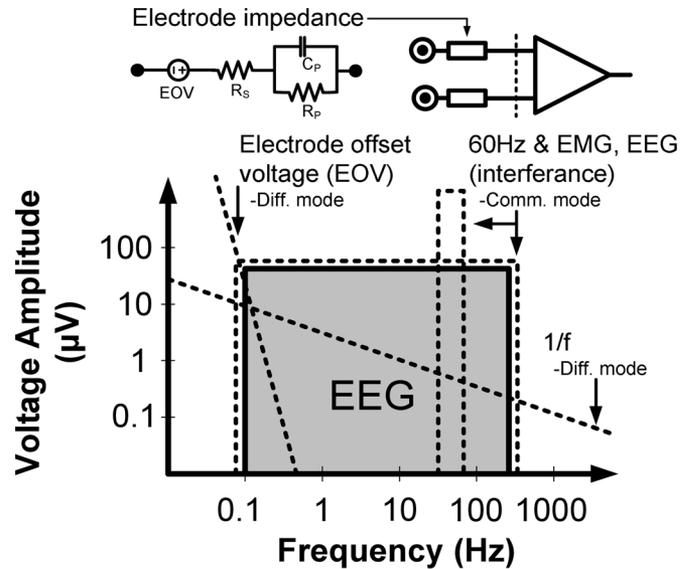


Fig. 4. Instrumentation challenges with EEG sensing.

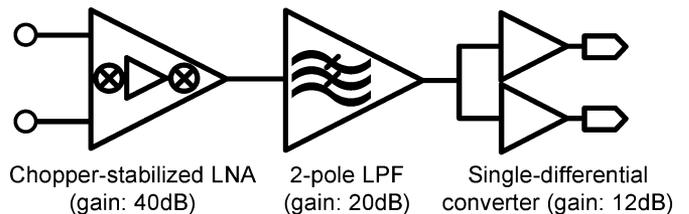


Fig. 5. Instrumentation amplifier block diagram.

The architecture of the I-amp is shown in Fig. 5. Its stages include a chopper-stabilized low-noise amplifier (CS-LNA), a low-pass filter, and a single-differential (S-D) converter to drive the ADC. These provide a total gain of approximately 4000.

1) *Chopper-Stabilized LNA*: Having stringent noise and electrode interfacing requirements, the CS-LNA is the most

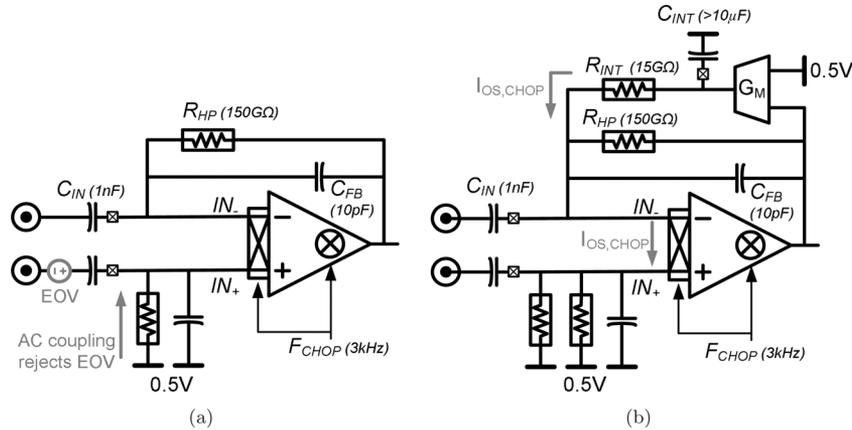


Fig. 6. Chopper stabilized LNA (a) core topology and (b) complete topology with $I_{OS,CHOP}$ cancelling servo-loop (C_{IN} and C_{INT} are off-chip).

critical stage of the I-amp. Chopper stabilization is a popular and important approach for mitigating $1/f$ noise, and several topologies employing it effectively towards low-power bio-potential sensing have recently been reported [16], [17]. A summary of these is provided below, followed by discussion of the motivation, circuit design, and analysis for the topology used in this I-amp.

State-of-the-Art Bio-Sensing Amplifiers: The amplifier in [16] uses a topology where the electrode signal is sensed through input capacitors. The use of input capacitors allows EOV cancellation through a servo-loop that integrates the low-frequency error at the amplifier output and feeds-back a corrective charge following the input capacitors. In the resulting topology, very few active devices strongly impact the amplifier noise, which is thus set primarily by the input pair of the core op-amp. In this topology, however, the amplifier performs chopper modulation before the large input capacitors. This leads to a switch-capacitor conductance that reduces the amplifier's input resistance beyond the level desired for scalp electrodes.

To achieve very high input impedance, the amplifier in [17] uses a current-feedback topology. Here, EOV is cancelled through a servo-loop that feeds-back a corrective current using transconductors. The noise of the transconductors, however, contributes to the overall amplifier noise, thus affecting the noise efficiency somewhat.

An additional consideration is that in applications where large EOV (e.g., 100 mV) must be tolerated, the approach of active cancellation through servo-loops limits the minimum supply voltage of the amplifier. As a result, power reduction through V_{DD} scaling is restricted.

Finally, alternate topologies that do not rely on chopper stabilization have also been effective for bio-sensing applications [18], [19]. These designs, however, are susceptible to $1/f$ and popcorn noise sources [16].

Proposed CS-LNA Topology: In order to achieve high input impedance, minimum noise, and low-voltage operation, the CS-LNA topology shown in Fig. 6(a) is used. The gain is set by the ratio of the input capacitors C_{IN} and the feedback capacitors C_{FB} . The high-pass cutoff, which is designed to be

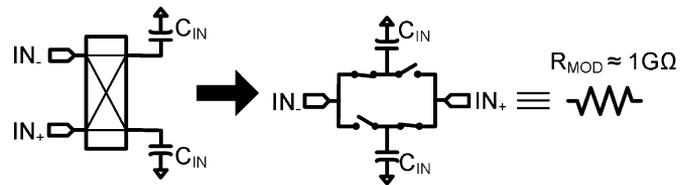


Fig. 7. Parasitic switched-capacitor resistance (R_{MOD}) introduced by chopper modulator.

less than 1 Hz in order to reject EOV while passing low-frequency EEG, is set by the large feedback resistor R_{HP} (along with C_{FB}).

An important choice is to perform input chopper-modulation at the op-amp virtual ground node. The first benefit of this is that it allows the DC offset of the electrodes to be truly decoupled by way of the biasing resistors (R_{HP}). As a result, very large EOV can be rejected passively and does not have to be processed by the amplifier. Accordingly, EOV imposes no limitation on the amplifier supply voltage, which can thus be reduced to 1 V to improve power efficiency and has been tested down to 750 mV. The second benefit is that the input modulator does not load the input electrodes. The input modulator does combine with the op-amp capacitance to introduce a parasitic switched-capacitor resistance (R_{MOD}), as shown in Fig. 7; however, at virtual ground the electrode signal does not appear as a voltage swing across the modulator. Hence, the amplifier has very large input-resistance from the perspective of the input electrodes.

One issue with input modulation at the virtual ground node is that the parasitic switched-capacitor resistance of the modulator R_{MOD} introduces a current path between the IN_+ and IN_- nodes in Fig. 6(a). Any offset at the op-amp input passes through this, giving rise to an offset current $I_{OS,CHOP}$ that can saturate the amplifier through the large feedback resistor R_{HP} . In particular, for the op-amp device sizes used, the effective value of R_{MOD} is only 1 G Ω (which is much less than R_{HP}). Accordingly, to cancel the offset-current, a G_M - C servo-loop is used as shown in Fig. 6(b) in order to integrate the amplifier's output error and provide the offset current to the input modulator. It is

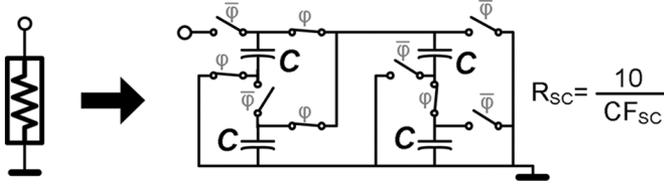


Fig. 8. Switched-capacitor resistors for implementation of large resistances using manufacturable capacitors.

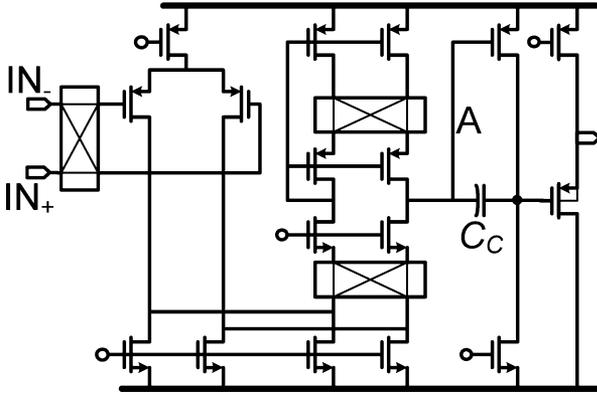


Fig. 9. Two-stage op-amp with embedded chopper-modulators used in CS-LNA.

worth noting that although the servo-loop provides a high-pass characteristic, R_{HP} is still required in order to cancel a zero in the feedback path which is introduced as a result of the parallel G_M - C and C_{FB} feedback branches.

An important drawback to performing input modulation at the op-amp virtual ground node is degraded common-mode rejection ratio (CMRR). Mismatch in the input capacitors can convert common-mode input signals to differential-mode noise. Chopping before the input capacitors (as in [16]) mitigates the effect of their mismatch [20]. Hence, in this design CMRR is compromised in favor of higher input-impedance and low-voltage operation. As described in Section IV-C, 60 Hz interference, which is the greatest concern with regards to CMRR, falls outside the band required for seizure detection. In this application 60 dB of CMRR is targeted, and Section V-A shows that EEG signals are reliably acquired.

The resistors in the CS-LNA are implemented using a modified switched-capacitor topology shown in Fig. 8. Through the use of series-to-parallel charge sharing between the internal stages, the charge transfer per cycle is reduced by a factor of ten. As a result, large resistances can be realized while ensuring high switching frequency (F_{SC}) and sufficiently large capacitors, which are required for improved manufacturability. SpectreRF is used to verify that noise from the switched-capacitor circuits is acceptable (see analysis below).

The op-amp used in the CS-LNA is shown in Fig. 9. It is composed of two gain stages with Miller compensation, and similar to the design in [16], output demodulation is performed before the dominant pole (at node A). As a result, chopper stabilization does not limit the required bandwidth. A third current-buffer stage is also included to reliably drive resistive loads.

Fig. 6(b) shows that the CS-LNA virtual ground node is biased to midrail at 0.5 V; this helps achieve the biasing required in the op-amp devices. Although V_{DD} is low, the transistor threshold voltages are such that all switches in the stage (implemented as CMOS transmission gates) can be minimum sized and still reliably pass their required signals levels at the switching speeds of interest.

CS-LNA Analysis: To simplify the analysis of the CS-LNA, Fig. 10(a) shows a single-ended representation where noise sources from each major element have been included. Based on this, an equivalent block diagram can be derived as shown in frame (A) of Fig. 10(b). In order to simplify this block diagram, note that

$$Z_a = \frac{1}{G_{MOD} + G_{INT} + G_{HP} + sC_{IN} + sC_{FB}}. \quad (1)$$

In the CS-LNA implementation, however, $G_{INT}, G_{HP} \ll G_{MOD}$ (where G_{MOD} is the parasitic modulator conductance) and $C_{FB} \ll C_{IN}$. Hence, Z_a can be approximated as

$$Z_a \approx \frac{1}{G_{MOD} + sC_{IN}} = \frac{1}{C_{IN}(s + \omega_{mod})} \quad (2)$$

where

$$\omega_{mod} = \frac{1}{R_{MOD}C_{IN}}. \quad (3)$$

The chopping waveform x_{ch} is not given the designation of a voltage to highlight the fact that switch-based choppers do not perform analog multiplication, but rather commutation (i.e., they reverse the polarity of the input signal periodically). Equivalently, x_{ch} is a square-wave signal with values of +1 or -1 and a mean value of zero. As a result, $x_{ch}^2 = 1$. We can exploit this characteristic to dispose of the choppers in frame (A) of Fig. 10(b), thereby simplifying the analysis. First note that

$$v_c = v_a x_{ch} + v_{na} = v_a x_{ch} + v_{na} x_{ch}^2 \quad (4)$$

which can be rewritten as

$$v_c = x_{ch}(v_a + v_{na} x_{ch}). \quad (5)$$

This means that the block diagram in frame (B) can be replaced with that in frame (C). The two choppers in (C) can then be eliminated since their product is unity. To further simplify the diagram, the $v_{na} x_{ch}$ summer is moved to the left of Z_a . To maintain equivalence, $v_{na} x_{ch}$ is multiplied by $1/Z_a$. Finally, the two summers are merged and the final block diagram for the CS-LNA is shown in frame (D). The transfer function of the operational amplifier, $A(s)$, is modeled as having large DC gain A_0 and a single, dominant pole at ω_0 . Some of the admittances are rewritten as poles and zeros with the relevant frequencies (i.e., ω_{mod} , ω_{hp} , and ω_{eff}) defined in frame (D).

Now, to analyze the CS-LNA, the loop gain is readily determined to be

$$LG(s) = \frac{\omega_0 A_0 C_{FB} (s + \omega_{hp}) (s + \omega_{eff})}{s C_{IN} (s + \omega_0) (s + \omega_{mod})}. \quad (6)$$

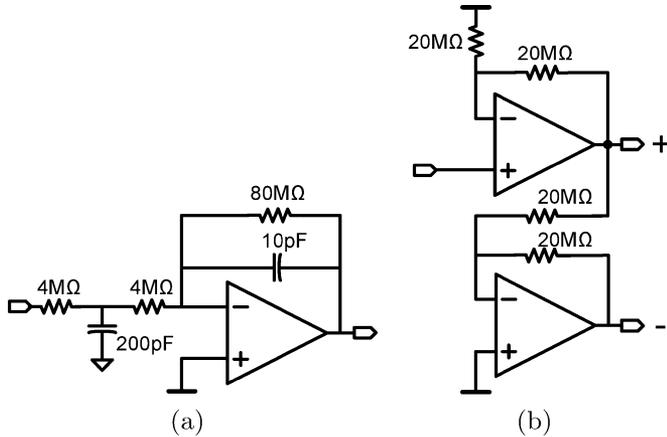


Fig. 11. Implementations for (a) low-pass filter and (b) single-differential converter.

(13), however, amplifies the noise for frequencies below ω_{mod} and shapes it as $1/f^2$. To minimize this effect, component values are chosen such that ω_{mod} is smaller than most of the frequency band of interest.

Using similar noise analysis, the input-referred noise transfer function for v_{ngm} is given by

$$H_{ngm,i}(s) = \frac{G_{\text{INT}}G_M}{s^2C_{\text{INT}}C_{\text{IN}}} = \frac{\omega_{\text{eff}} \cdot \omega_{\text{hp}}}{s^2} \cdot \frac{C_{\text{FB}}}{C_{\text{IN}}}. \quad (14)$$

The noise contribution from G_M is small since both ω_{eff} and ω_{hp} are below the band of interest, and since $C_{\text{FB}} \ll C_{\text{IN}}$.

2) *Low-Pass Filter and Single-Differential Converter*: The low-pass filter and S-D converter have a much smaller impact than the CS-LNA on the noise and instrumentation issues. Together, their power is approximately 20% of the total I-amp power. The low-pass filter provides two-pole roll-off near 200 Hz and a gain of 20 dB. Its implementation is shown in Fig. 11(a), where the OTA uses a standard two-stage topology.

The S-D converter provides a total differential gain of approximately 12 dB, and it has been designed to drive the capacitive sample-and-hold of the ADC. Its implementation is shown in Fig. 11(b), where the OTAs use a differential input stage and a current-buffer output stage to drive the resistors shown.

B. ADC

Based on simulation experiments of the detection system (see Section IV-C), it is determined that detection improves as the resolution of EEG samples is increased up to at least 10 bits. The ADC used in the system is thus a 12-bit successive approximation register converter with an ENOB of 10.55 bits. It uses the 6-bit main-DAC and 6-bit sub-DAC architecture shown in Fig. 12. Detailed design and analysis of the ADC is presented in [22]. Although the maximum conversion rate is 100 kS/s, it operates at only 600 S/s in this system. An important feature of the ADC for this application is that it maintains its energy per conversion down to very low speeds (i.e., < 100 S/s). Although static biasing is required in the comparator pre-amplifiers (to limit device hysteresis from large bias swings [23]), controlled power-gating (through the *SLEEP* signal) ensures that the static biasing remains on for only the minimum time required by the conversion.

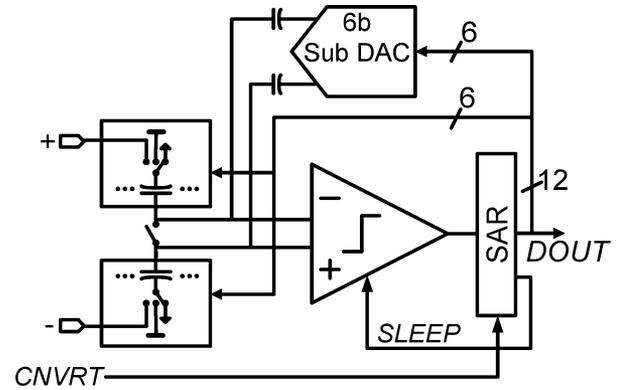


Fig. 12. 12-bit SAR ADC block diagram.

Like the I-amp, the ADC operates at 1 V. It is fully differential, which helps achieve 12-bit dynamic range for the given noise floor and also provides power-supply noise rejection, since supply noise originating from capacitor array switching is an important concern.

C. Feature Extraction Processor

The feature extraction processor derives the spectral energy distribution of the input EEG channel. Due to the wide range of approaches and parameters associated with spectral analysis, it is important to understand the key tradeoffs affecting seizure detection. Clinical work in [9] has shown that the EEG band from 0–20 Hz is relevant for seizure detection. Since implementation and computation complexity are also important concerns in this low-power integrated system, the precise manner in which the band should be analyzed depends on how the detector performs as the processor's implementation parameters are eased.

The critical detector metrics are sensitivity, specificity, and latency. With seizure detection performed via learning-based SVM classification, it is difficult to analytically determine the precise effect on these metrics that the feature extraction implementation parameters have. Accordingly, in order to ascertain how the processor complexity can be minimized, experiments were performed to evaluate detector performance with respect to the processor parameters. As an example, Fig. 13 shows how the sensitivity, specificity, and latency are affected when the resolution of the spectral energy distribution is scaled from two bins to eight bins (experiments are based on 1117 hours of data from 30 patients). For instance, to achieve a sensitivity of 90%, at least seven bins are required. Fig. 13 also shows a plot of how the number of support vectors is affected; the number of support vectors represents the SVM classification complexity and linearly scales the energy of the radial-basis kernel computation; therefore, in the complete detection system, it affects the energy of the device used to perform classification. The final processor parameter values that are targeted based on this experimentation are specified in Table II, and they pertain to the modulated filter bank implementation described below.

1) *Spectral Analysis Implementation*: Fig. 14 shows the block diagram of the signal processor used to perform spectral analysis and feature vector extraction. It consists of a bank of seven modulated bandpass filters (BPF1-7) that analyze the band from 0–20 Hz. Each of the modulated filters is followed

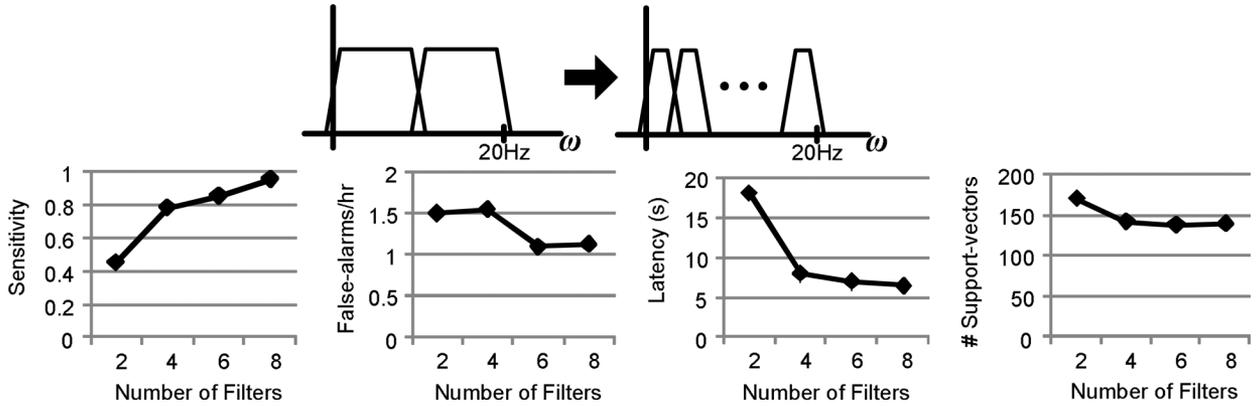


Fig. 13. Experimentation of detector performance while scaling feature extractor spectral bin resolution (each point is based on 1117 hours of data across 30 patients).

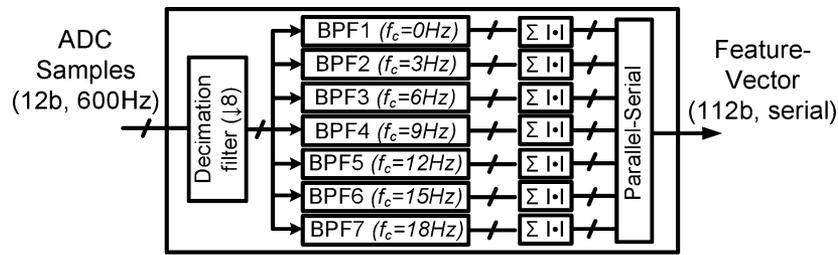


Fig. 14. Block diagram of feature extraction processor.

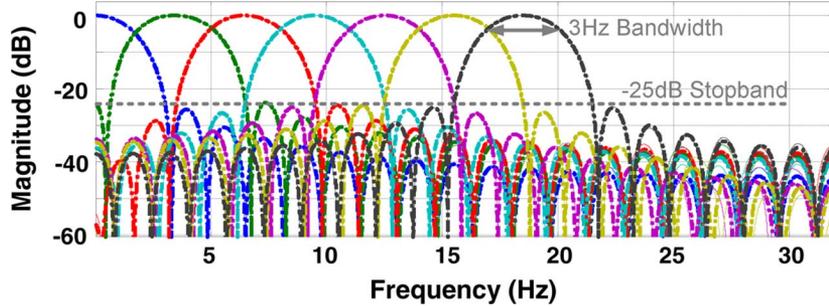


Fig. 15. Specifications of modulated bandpass filters.

TABLE II
SPECIFICATIONS FOR FEATURE EXTRACTOR FILTER BANK

# of filters	7
-3dB bandwidth	3Hz
Stop-band gain	-25dB
Transition band	1.5Hz
Resolution (input/coefficient)	12 bits

by a magnitude summation, whose output is used to represent the spectral energy of the bin. The spectral energies for each bin are represented by a 16-bit number, and they are computed over a two-second window. The seven bin energies are then provided to an output interface which is responsible for serially outputting the resulting 112-bit feature vector for the one-channel SoC.

As mentioned, the ADC samples the EEG at a rate of 600 S/s, providing some oversampling in order to tolerate aliasing in the seizure band due to non-idealities in the anti-aliasing filtering

of the I-amp. Since the analysis bandwidth of interest is much smaller, a decimation filter provides down-sampling by 8 preceding the filter bank in order to ease the specifications of the modulated filters. Using this approach, the final filter orders are 48, for the decimation filter, and 46 for the modulated filters, which have the specifications illustrated in Fig. 15. Both the decimation and modulated filters are Type-I FIR. The resulting impulse responses are symmetric, allowing the coefficient multiplications to be shared [24]. As a result, only 24 and 23 multiply-accumulate operations are required for the respective filters. Finally, during typical system operation the modulated filters need to operate at a frequency of only 75 Hz in order to process input samples to the decimation filter at the rate of 600 Hz. At a supply voltage of 1 V, the modulated filters can, however, operate up to a frequency of 50 kHz.

As an alternative to the modulated filter-bank, FFT is also a possible implementation for spectral analysis. However, for modest decimation filter complexity, the analysis bandwidth is

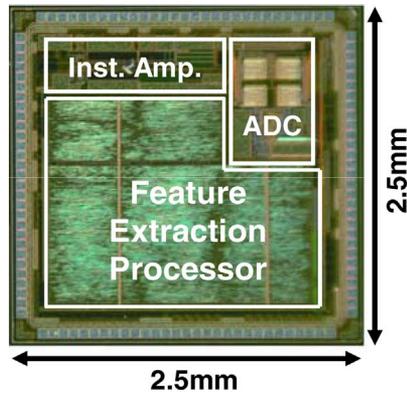


Fig. 16. Die photograph of prototype SoC.

TABLE III
SOC PERFORMANCE SUMMARY

Supply voltage	1V
I-amp LNA power	3.5 μ W
I-amp input impedance	>700M Ω
I-amp noise (input referred, 0.5Hz-100Hz)	1.3 μ V _{rms}
I-amp electrode offset tolerance	>1V
I-amp CMRR	>60dB
ADC resolution	12b
ADC energy per conversion	250pJ
ADC max. sampling rate	100kS/s
ADC INL/DNL	0.68/0.66LSB
ADC SNDR	65dB
Digital energy per feature-vector	234nJ
Feature vector computation rate	0.5Hz
Total energy per feature-vector	9μJ

still considerably wider than the seizure band, and modulated filters allow selective analysis in the low-frequency band of interest.

V. SOC TEST RESULTS

The EEG acquisition and seizure detection SoC is implemented in a 0.18 μ m CMOS process with five-metal-two-poly (5M2P) layers [25]. The choice of technology among the options available was driven primarily by the need for low leakage and the need for poly-poly capacitors, which are required by the ADC and I-amp. A die photograph of the prototype IC is shown in Fig. 16. The entire device operates from a single 1 V supply. A performance summary of the SoC is provided in Table III.

The I-amp has an effective area of approximately 0.30 mm². The power consumption of the CS-LNA, which is the most critical stage is, 3.5 μ W. Its CMRR is > 60 dB, and its integrated noise over a 100 Hz bandwidth is 1.3 μ V_{RMS}. Fig. 17(a) shows the I-amp transfer-function measured at the output of the low-pass filter stage, where a gain of 60 dB is observed. Fig. 17(b) shows the input-referred noise measured at the output of the low-pass filter stage, where an input-referred noise power

spectral density (PSD) of approximately 130 nV/ $\sqrt{\text{Hz}}$ is observed in the EEG signal band. Fig. 17(c) shows a comparison of the I-amp with previously reported designs.

Although the ADC samples at 600 S/s in this system, it achieves a maximum sampling rate of 100 kS/s at a power consumption of 25 μ W. The resulting energy/conversion is 250 pJ (maintained down to very low sampling rates due to power-gated duty cycling), and the SNDR (with a 50 kHz input) is 65.3 dB (10.55 ENOB). Detailed performance measurements are provided in [22] along with the FOM comparison.

The energy per output vector of the feature extraction processor is 234 nJ and it derives 112-bit output vectors at a rate of 0.5 Hz. The overall energy of the one-channel SoC is approximately 9 μ J per output vector.

A. EEG Acquisition

Fig. 18(a) shows actual EEG recorded using the on-chip I-amp and ADC without any post-processing. For sensing, Ag/AgCl electrodes are used along with electrolyte gel. A ground connection is provided between the SoC and the depicted ground location on the scalp. Differential sensing is performed through a recording electrode and a reference electrode, which is located on the scalp midline. The first waveform corresponds to recordings from the frontal position location (FP1-REF). The large periodic excursions correspond to eye-blinks by the subject. The second two waveforms correspond to recordings from the occipital location (O1-REF). In the first case, the subject closes his eyes to enter a relaxed state, evoking the alpha wave with a characteristic 10 Hz rhythm. In the second case, the subject opens his eyes, and is restimulated by the environment, abolishing the alpha wave. Fig. 18(b) shows an FFT of the occipital recordings, highlighting the 8–12 Hz activity of the alpha wave during the relaxed, eyes-closed state.

VI. EEG CLASSIFICATION SYSTEM DEMONSTRATION

Plans exist to employ the SoC in patient tests both for patient monitoring/alert-generation and for closed-loop actuation of a therapeutic vagus nerve stimulator [6]. Before patient testing, however, system demonstration of the SoC is performed through real-time EEG sensing, digitization, feature vector extraction, and feature vector classification.

For the demonstration, a one-channel system is used to sense EEG from the occipital electrode location, and the SVM is trained to detect the relaxed eyes-closed state characterized by the presence of the alpha wave. Fig. 19(a) shows a block diagram of the setup. The SVM classification computation has been implemented on several processor platforms including low-power DSP (e.g., MSP430) and mobile laptop device (for the purposes of benchtop testing and demonstration). Detection latency is an important metric that is primarily limited by feature extraction; the importance of low-frequency (e.g., 1 Hz) EEG content in seizure detection implies the need for long window times for spectral analysis. For instance, in this system a window length of 2 seconds is used.

For the demonstration, training is first performed by providing the SVM with ten feature vectors (i.e., five eyes-closed

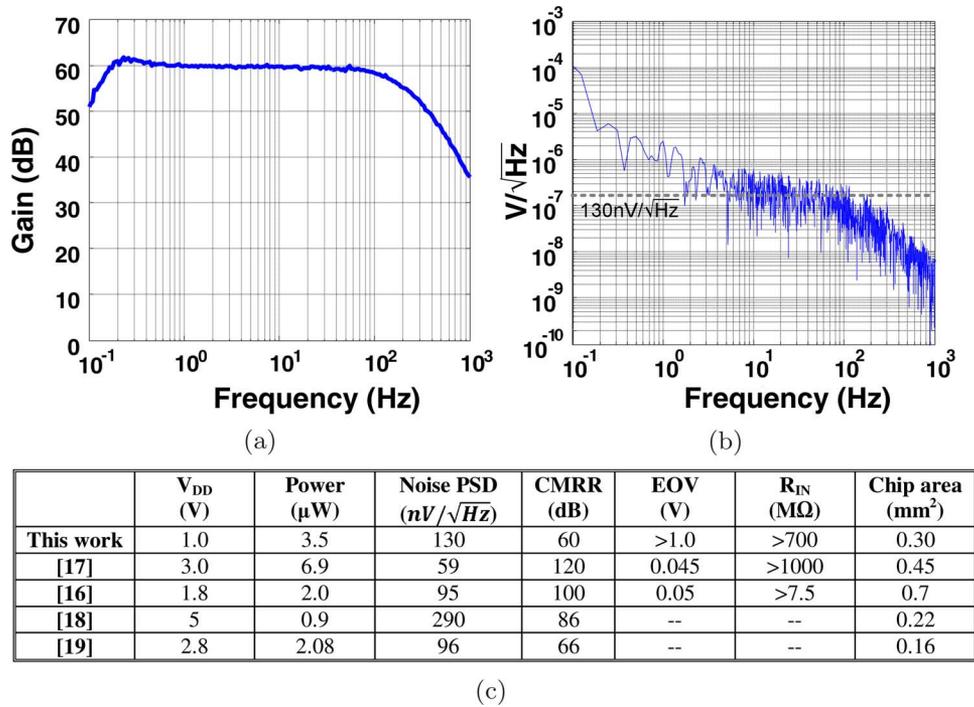


Fig. 17. Instrumentation amplifier measurement results: (a) gain transfer function (at low-pass filter output), (b) input-referred noise PSD, and (3) comparison with reported designs.

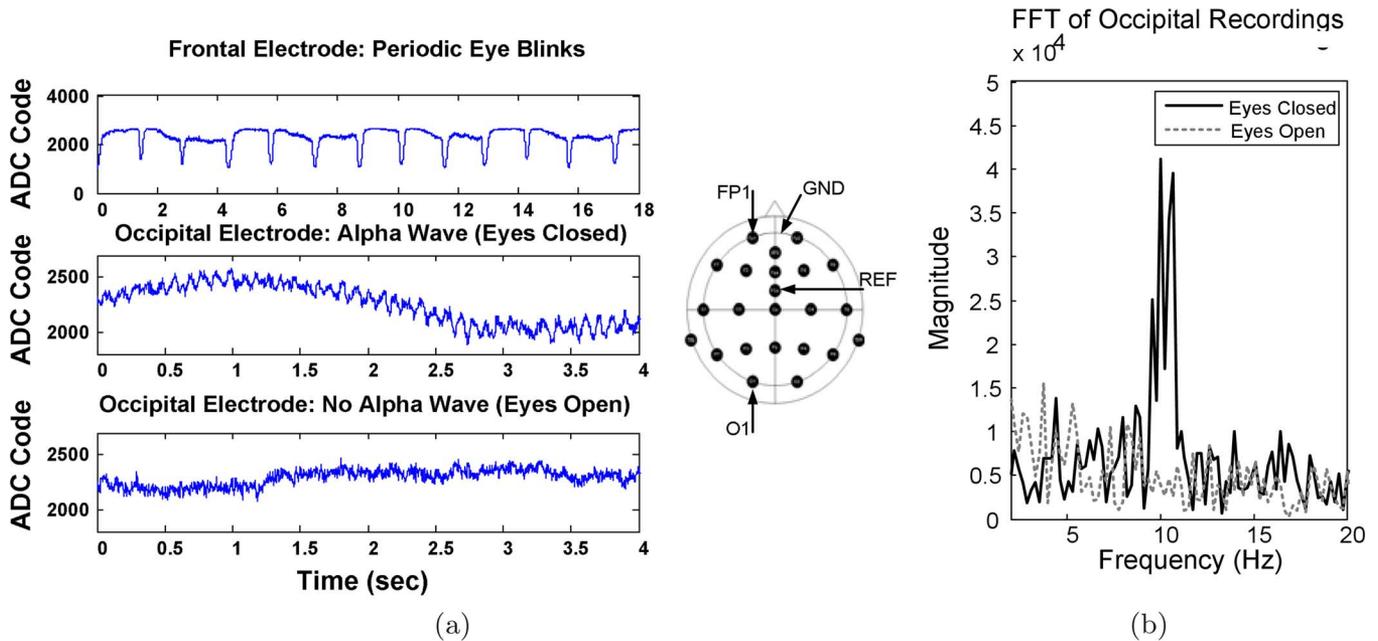


Fig. 18. Frontal-position and occipital EEG recordings using on-chip I-amp and ADC in (a) time-domain and (b) frequency domain (occipital recordings).

and five eyes-opened), requiring 20 sec of subject monitoring. During real-time detection, the subject periodically opens and closes his eyes to enter and exit the relaxed state, and the SoC continuously senses the EEG and generates test feature vectors that are transmitted to an SVM for alpha classification.

Fig. 19(b) shows a segment of the demonstration. The first waveform corresponds to the ADC output, showing the EEG annotated with the relaxed eyes-closed and eyes-opened states. The second waveform corresponds to the output of the SVM

classification. All relaxed eyes-closed states are correctly detected with less than 2.5 sec latency during a five-minute test run.

VII. CONCLUSION

This paper discusses the rationale, design, and results for an SoC performing continuous EEG acquisition and feature extraction which is required for a chronic seizure detection system for epilepsy patients. An important focus of this work is processing

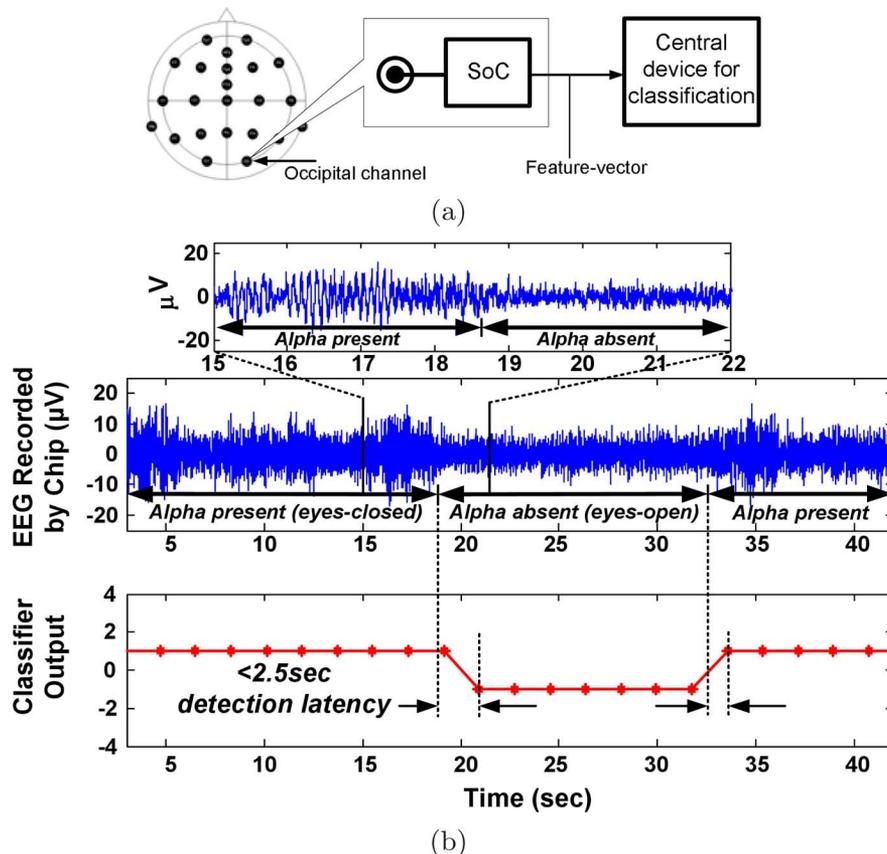


Fig. 19. One-channel system demonstration of EEG acquisition, digitization, feature vector extraction, and classification: (a) setup block-diagram and (b) measured detection waveforms.

of the raw bio-potentials to extract physiologically important information and represent this as a concise feature vector. Patient idiosyncrasies and the presence of numerous complex background processes motivates the need to apply machine learning on the feature vectors on a patient-by-patient basis in order to achieve high sensitivity, specificity, and latency of the detection.

The need to process a large amount of highly distributed data in order to extract specific subtle variances applies generally in brain monitoring applications. Since processing and communication of the entire data through the system imposes excessive power cost, ultra-low-power local processing is critical to make the overall system viable.

Finally, the instrumentation needs for low-power EEG acquisition strongly affect the total power. As a result, it is important to use targeted analog processing where possible to avoid the limitations imposed by electrode, environment, and physiological disturbances.

The presented SoC performs EEG acquisition, digitization, and feature vector extraction. Each SoC corresponds to one electrode channel, and up to 18 channels may be required depending on the patient. Each SoC operates from a 1 V supply and consumes $9 \mu\text{J}$ to derive a feature vector. Feature vectors are derived at a rate of 0.5 Hz.

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