A 2.5 nJ/bit 0.65 V Pulsed UWB Receiver in 90 nm CMOS

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***Abstract*—A noncoherent 0–16.7 Mb/s ultra-wideband (UWB) receiver using 3–5 GHz subbanded pulse-position modulation (PPM) signaling is implemented in a 90 nm CMOS process. The RF and mixed-signal baseband circuits operate at 0.65 V and 0.5 V, respectively. Using duty-cycling, adjustable bandpass filters, and a relative-compare baseband, the receiver achieves 2.5 nJ/bit at 10^{-3} BER with -99 dBm best case sensitivity at 100 kb/s. The energy efficiency is maintained across three orders of magnitude in data rate. For data rates less than 10 kb/s, leakage power dominates energy/bit.**

***Index Terms*—Adjustable bandpass filter, energy/bit, interference mitigation, low-noise amplifier (LNA), low voltage, mixed-signal, passive mixer, phase-splitter, receiver, relative-compare baseband demodulator, sensitivity, system, ultra-wideband (UWB).**

I. Introduction

With the proliferation of portable electronics and wireless sensor networks, energy-efficient radios have become an active area of research [1]–[3]. Though sub-nJ/bit data reception is achievable for data rates $\geq$100 Mb/s using optimized coherent architectures [4], there is a need for simple, low-power radios as specified in the IEEE 802.15.4a task group [5]. This work explores the unique properties of FCC-compliant pulsed ultra-wideband (UWB) signals and scaled CMOS devices to improve the energy/bit of existing low data-rate GHz-range integrated radios for use in wireless sensor network applications.

Fig. 1 is a block diagram of a typical sensor node. For a node to become energy autonomous and rely solely upon energy scavenging, energy efficiency is a key parameter. Many techniques have been demonstrated to reduce radio power consumption, namely through circuit innovations [6]–[9], process technology advancements [10]–[13], and high-Q off-chip resonators [1], [14]. However, even with these techniques, energy efficiency is still difficult to achieve at low data rates (Fig. 2).

Fig. 2 plots the energy/bit of recently published receivers and shows the dependency between energy/bit and data rate. At the extremes of data rate, a 480 Mb/s WiMedia [15] compliant UWB receiver achieves 0.68 nJ/bit [4], and at 5 kb/s a super-regenerative receiver [1] achieves 80 nJ/bit. Because the fixed cost of analog/RF bias currents in the receiver are amortized over more bits/second as data rate increases, a tradeoff between energy efficiency and data rate is observed. Although coherent signaling schemes utilize bandwidth more efficiently and achieve better sensitivity than noncoherent schemes, these benefits come at the cost of degraded energy efficiency when normalized by data rate. This is due to the power cost of phase tracking hardware for coherent architectures. Three prominent phase-independent signaling schemes utilized by the receivers in Fig. 2 are on–off-keying (OOK), frequency-shift-keying (FSK), and pulse-position modulation (PPM). Receivers [1], [16], [17], and [18] are super-regenerative architectures utilizing OOK signaling. They do not require a phase-locked loop (PLL), thereby saving power. The work outlined in [19] affords similar energy savings as the super-regenerative architecture by operating with a 20 dB noise figure (NF) system specification, allowing the low-noise amplifier (LNA) to operate in sub-threshold. Analog correlation and UWB PPM signaling is used in [3] to achieve low energy/bit, but only at a moderately high, fixed data rate. The receiver in [2], similar to [19], increases the modulation index of the FSK receiver to relax the PLL and demodulation requirements. It also achieves voltage amplification through a passive resonance, thereby demonstrating an optimal energy/bit measurement at 300 kb/s. In this work, by using a noncoherent UWB PPM signaling scheme, duty-cycling, and a relative-compare noncoherent demodulator, a 2.5 nJ/bit receiver is realized across three orders of magnitude in data rate.

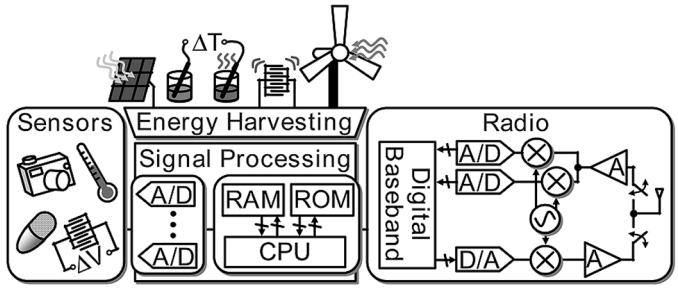

Fig. 1. Wireless sensor node.

II. Signaling and System Architecture

To maximize energy efficiency, a binary noncoherent PPM signal scheme using UWB pulses is chosen [Fig. 3(a)]. In this signaling scheme, the 2 ns UWB pulse (corresponding to a 500 MHz signal bandwidth) can be placed in one of two time slots: T_{int1} or T_{int2}. If the pulse arrives in T_{int1}, then a 1 is declared by the receiver. If the pulse arrives in T_{int2}, then a 0 is declared. Though the UWB pulse is only 2 ns wide, T_{int} is set

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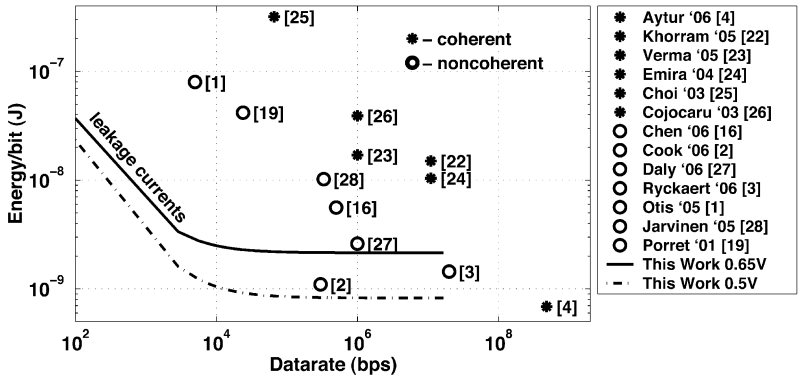


Fig. 2. Energy/bit plot of recent radio receivers.

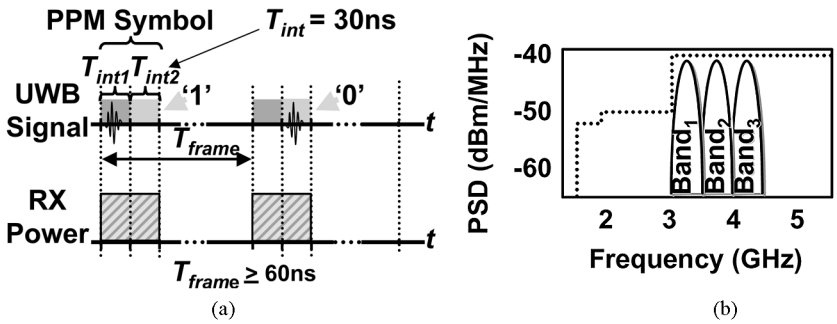


Fig. 3. (a) Binary UWB PPM signal and (b) band plan.

to 30 ns such that the worst-case multi-path channel and crystal frequency offset can be tolerated. The data rate is scaled simply by changing the receiver off period between each PPM symbol. The receiver is designed so that it can be quickly turned on/off to minimize power consumption during the time between symbols, thereby exploiting the energy saving opportunities inherent in this signaling scheme [Fig. 3(b)]. The maximum data rate of this architecture is 16.7 Mb/s when $T_{\rm frame} = 60$ ns and one bit is encoded in each frame. In determining the band plan, this architecture adopts three 500 MHz subbands [Fig. 3(b)], and trades transmission distance for improved interference robustness.

Fig. 4 shows a simplified block diagram of the noncoherent receiver. It is comprised of a 3–5 GHz subbanded RF front-end, a passive self-mixer, and a low-power relative-compare baseband [20]. An RF PLL is not required. Only a 33 MHz crystal is needed to operate the relative-compare baseband. For out-of-band noise/interference robustness, the RF front-end performs channel selection in the 3.4, 3.9, and 4.4 GHz bands. More than 99% of the total receiver power consumption is in the front-end gain stages. By switching on the receiver only during the 60 ns PPM symbol, energy savings are realized by duty-cycling the receiver. The noncoherent receiver utilizes mixed-signal techniques to realize a relative-compare baseband that determines the bit. For bit-slicing, a low-power sample-and-hold (S/H) capacitor network stores analog integration results during $T_{\rm int1}$ and $T_{\rm int2}$ onto separate capacitors C_1 and C_2, respectively. Thereafter, two cascaded offset-compensated preamplifiers and a latch perform a relative-compare on the two capacitor voltages to evaluate the received bit. This scheme inherently performs compensation of DC-offsets from down conversion and pre-integrator signal-path normalization in each bit decision. In this way, PPM signals are easily and reliably demodulated for high-speed demodulation up to $1/(2 \cdot T_{\rm int}) = 16.7$ Mb/s. The entire receiver can operate at 0.65 V or 0.5 V, and is implemented in a 90 nm CMOS process.

A. RF Front-End

The RF front-end consists of an LNA, six RF gain stages, and a passive self-mixer (Fig. 4). Each of the six amplifiers contain a second order bandpass filter for channel selection. The front-end also provides 40 dB of gain to overcome the $V_{\rm out} = k \cdot V_{\rm in}^2$ transfer characteristic of the self-mixer for small inputs. The single-to-differential conversion is done in the first stage so that the remaining amplifiers with high common-mode rejection ratio (CMRR) equalize and condition the differential signal. The amplifiers and passive mixer are DC-coupled and chain-biased so that duty-cycling does not cause long-settling transients.

B. High-Speed Baseband

To achieve rapid coarse acquisition during the preamble search, uninterrupted time-adjacent integration windows for continuous bit decisions are needed [21]. Fig. 5 shows the implemented baseband block diagram and the corresponding operation schedule. Four capacitors are rotated among three states—*reset*, *integrate*, and *evaluate bit*—to achieve integrations every $T_{\rm int}$. Two offset-compensated relative-compare paths ($\rm Decision_1$ and $\rm Decision_2$) swap between *evaluate* and *reset* modes to provide a continuous stream of bit decisions

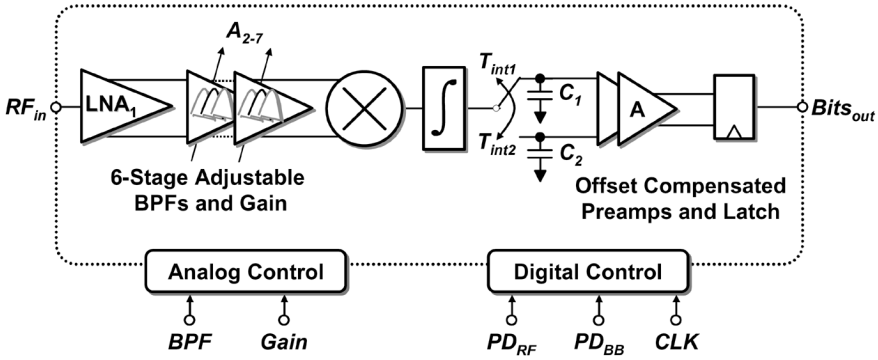


Fig. 4. Self-mixing receiver architecture.

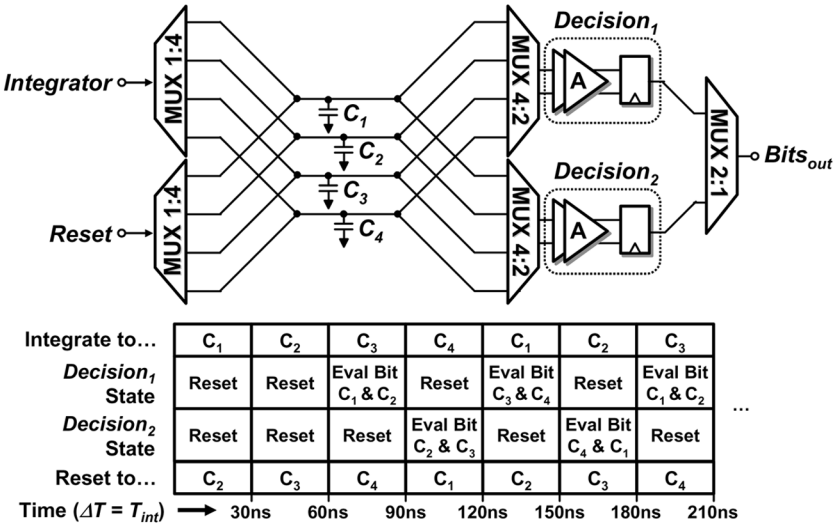


Fig. 5. High-speed baseband.

every $T_{\rm int} = 30$ ns. The pipeline delay for a bit decision to appear at the output from the end of a PPM symbol integration time is 45 ns. The fastest clock required to operate the entire receiver is $1/T_{\rm int}$, or 33.3 MHz.

III. Circuits

A. LNA and Gain Stages

The circuit schematic for the LNA is shown in Fig. 6(a). This block operates at 0.65 V or 0.5 V, depending on the required sensitivity. This circuit is based upon a common-gate single-to-differential conversion architecture (with core transistors M_2 and M_3) to provide differential signals required by the self-mixer. Performing this operation in the first stage impacts the NF significantly. However, if conversion is done in the last stage, the signal no longer qualifies as "small-signal," and requires a highly linear, high dynamic range converter, which is unrealistic for low-voltage circuits. Furthermore, power supply and substrate noise directly couple and appear inline with the signal for single-ended circuits. Therefore, to improve signal fidelity and reduce the number of sensitive nodes to power supply and substrate noise, the single-to-differential conversion is completed in the first stage and the effect on NF is accounted for in the link budget.T he following six gain stages with high CMRR equalize the conversion. A differential amplifier with one input grounded could suffice as a converter, but since this is the first stage, additional reactive elements for matching and diodes for ESD protection would be required, thereby increasing circuit complexity. Thus, a back-to-back common-gate architecture is used to meet the converter requirements by floating the common gate connection during small-signal amplification and allowing the series capacitive divider to invert the signal across $C_{\rm gs}$ of M_2 and M_3. The circuit also provides ESD protection from the inherent source-bulk diode in M_2.

The input match is primarily set by the feedback mechanism through the gain and $1/g_{\rm ds}$ of M_2, as the 0 V RF choke formed by the $L_S C_S$ parallel resonance forces most of the RF current into the source of M_2. In addition, a 0 V load formed by $L_L C_L$ allows the LNA to operate at 0.65 V or 0.5 V while keeping M_2 and M_3 saturated. The LNA is designed to have a 1.5 GHz bandwidth by damping the load with R_L, so that the desired S_{11} is achieved all at once without requiring channel-to-channel tuning to support the subbanded architecture. Subbanded channel selection is thereby delegated to the following six gain stages. For process variations, the DC bias for the transistors and load varactors are tunable through $V_{\rm gate}$ and $\rm BPF_1$.

The energy savings during the data payload are realized with aggressive duty-cycling between pulses. The LNA is

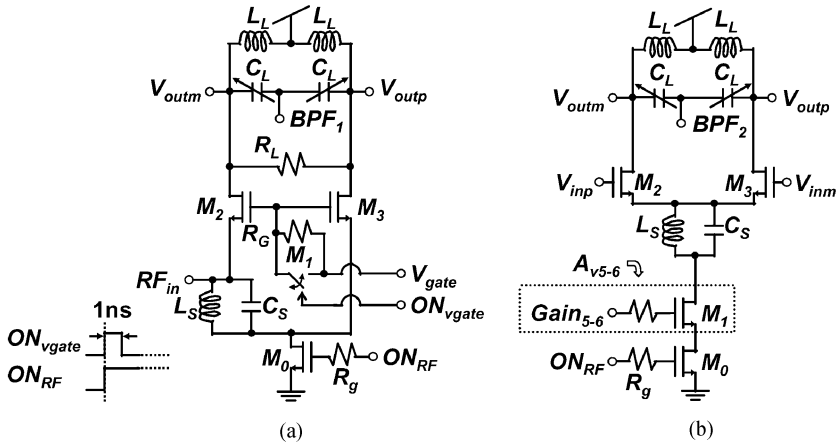


Fig. 6. (a) LNA and (b) A_{v1-6}.

dynamically biased and switched on within 2 ns. When $\mathrm{ON_{RF}}$ is switched on to power up the amplifier, $\mathrm{ON}_{v\mathrm{gate}}$ is also pulsed for 1 ns to relay V_{gate} to the gate with low impedance. Thereafter, $\mathrm{ON}_{v\mathrm{gate}}$ is switched off, and the amplifier has reached its operating point and ready to amplify RF signals. R_g provides the necessary damping so that the signal driving $\mathrm{ON_{RF}}$ does not appear under-damped. Because the LNA is virtually symmetric, switching M_0 does not cause significant differential mode excitation. For any differential perturbations, the settling time is dictated by the effective time constant seen at the load. For a 1.5 GHz bandwidth, the time constant is approximately 100 ps. To minimize leakage currents when the amplifier is off, the length of M_0 is sized $2\times$ minimum length.

Fig. 6(b) shows the schematic for A_{v1-6}. Each of these amplifiers acquire their biasing from the preceding amplifier's DC output voltage. All of the resonant loads are identical; thus, the control voltage to the varactors, BPF_2, can be routed with one external analog voltage. Each stage provides an identical 6 dB of gain and can be tuned to any one of three subband channels at 3.4 GHz, 3.9 GHz, and 4.4 GHz. The tunable bandpass filter load is formed by a differential inductor L_L and varactor C_L, and has a tuning range of over 1 GHz. Gain stages A_{v5-6} have power scaleable, bandwidth-independent gain control with the inclusion of M_1. Because the input gate voltage of each amplifier is DC biased to the power supply through the load inductor of the prior stage, large capacitances are not charged/discharged during power on/off—only the parasitic capacitance at the drain of M_0 is charged/discharged.

Monte Carlo simulations of the differential output gain from a small-signal input at the power supply show a 10 dB improvement with the inclusion of the parallel $L_S C_S$ resonance. Like the LNA, these amplifiers can be switched on and settle at their operating points within a few nanoseconds.

B. Self-Mixer

In the passive self-mixer shown in Fig. 7, M_1, and M_2 are used as voltage-controlled resistors. The biasing for the source and drain of these transistors are derived from the DC output voltage of the previous amplifier stage (a short to power through the load inductor and through the transistors of the mixers themselves). The maximum gain through the mixer occurs when V_{GS} of the transistors is biased close to the threshold voltage. This passive self-mixer requires zero voltage headroom for operation. The single-ended output of the mixer also lends itself to the baseband circuitry that follows.

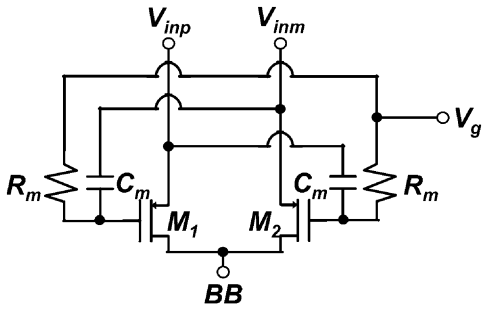


Fig. 7. Self-mixer.

C. Baseband Integrator

At baseband, the integrator, S/H capacitor bank (C_1, C_2, C_3, and C_4), offset-compensated preamplifier stages, and latch are all designed for 0.5 V operation and work together to perform signal demodulation. The integrator, shown in Fig. 8, is an inverter externally biased at the switching threshold for 38 dB of DC gain. The DC gain and the output impedance must be maximized so that the integrator can hold the final integrated voltage for the targeted time. Because a voltage shift is necessary from the mixer to the integrator, an AC coupling capacitor interfaces them together. However, because the integrator must be duty-cycled along with the rest of the system, it is DC-biased with a high impedance connection at the gate (because the gate voltage and mixer output do not change when the system is switched on/off), and dynamically biased at the output (the S/H capacitors are also pre-charged to V_{reset} before they are presented to the integrator to capture an integration). Thus, the integrator is always set to the switching threshold at the beginning of each integration and integrates in the same direction from the self-mixer rectified output. Fig. 9 shows the integrator performing a new integration every 30 ns when a stream of pulses is present at the input. These integrations are stored onto one of four capacitors that are rotated through at each integration time

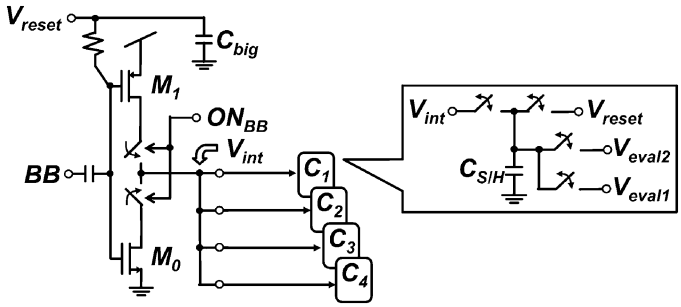


Fig. 8. Integrator and S/H capacitors.

according to the operation schedule in Fig. 5. Although the integrator integrates in increments of 30 ns, the capacitors hold the final integration value for an additional 60 ns so that adjacent bit decisions can be made. For each capacitor, the 30 ns integration time, two consecutive 30 ns hold times, and 30 ns reset time are staggered relative to each other. M_0 and M_1 are nonminimum length transistors to achieve the maximum DC gain, and their widths are sized such that a pole at 250 MHz is formed at the output of the mixer. The S/H capacitors are integrated using high Q MIM capacitors for high linearity, and sized such that the inverter and capacitor combination approximates an integrator over the 250 MHz bandwidth. Two minimum length complementary switches are used at the drain nodes for fast switching of the integrator, and allow for symmetric convergence from the power and ground supplies to the operating point voltage. The length of the switching transistors are set such that $R_{\rm off}/R_{\rm on}$ is sufficiently large for isolation between input/outputs of the switches. $V_{\rm eval1}$ and $V_{\rm eval2}$ connect the S/H capacitors to the appropriate offset-compensated preamplifiers for downstream bit evaluation.

D. Offset-Compensated Preamplifiers and Latch

Offset-compensated preamplifiers reduce the offset voltage of the regenerative bit decision latch. The offset voltage contributes significantly to bottom-line receiver sensitivity. If there is ideally zero offset, the latch will declare ones and zeros with equal probability in the presence of two noise integrations. However, for nonzero offset, the offset voltage undesirably skews the bit decisions. Monte Carlo simulations of the latch offset voltage show that the maximum offset can be as much as ± 100 mV. A schematic of the offset-compensated preamplifier and its associated timing diagram is shown in Fig. 10. In reset, all of the switches are closed to allow for fast turn-on time and S_4 presents a 0 V input to the amplifier. Only one negative edge to S_1 is sent to the amplifier to initiate the sequence from compensation to amplification. S_2 through S_4 are asynchronously generated with three series buffers starting from S_1. Initially, when S_1 is opened, the output offset of the amplifier is presented to C_C. S_2 and S_3 successively open thereafter, and store the offset onto C_C. Finally, S_4 releases the input from the 0 V input state, and another signal that is triggered from the falling edge of S_4 latches the appropriate $V_{\rm eval}$ voltages (from Fig. 8 to $V_{\rm in}$ of the preamplifier for amplification. The total gain for the cascaded stages is 20 dB, which reduces the latch offset voltage by an order of magnitude.

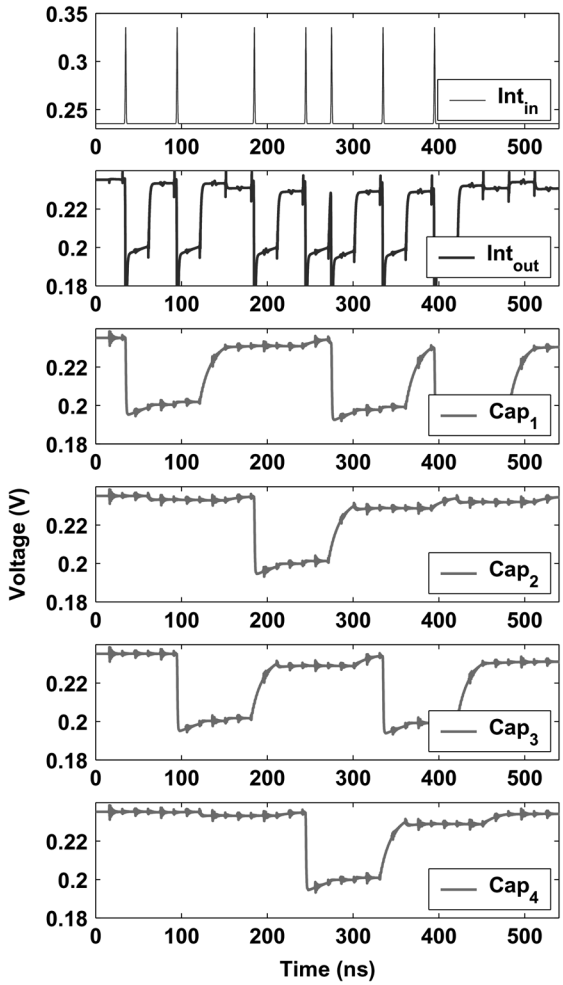


Fig. 9. Simulated baseband capacitor bank transient response.

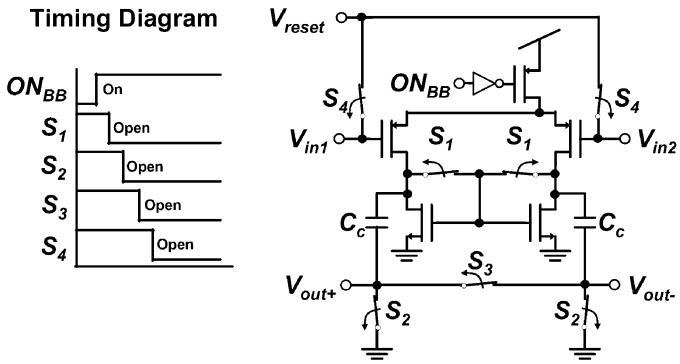


Fig. 10. Timing diagram and initialized offset-compensated preamplifier.

Receiver sensitivity could be improved by adding an offset voltage control to the latch, and wrapping the backend in a feedback loop. A simple, low power calibration can be performed by disabling the front-end to generate noise inputs to the baseband and running the backend. The offset knob can be tuned until equal percentages of ones and zeros are observed at the bit decision output. Because the RF front-end—which consumes 99% of the total receiver power—is turned off, this calibration method requires marginal power overhead while affording improvements in receiver sensitivity and architectural simplicity.

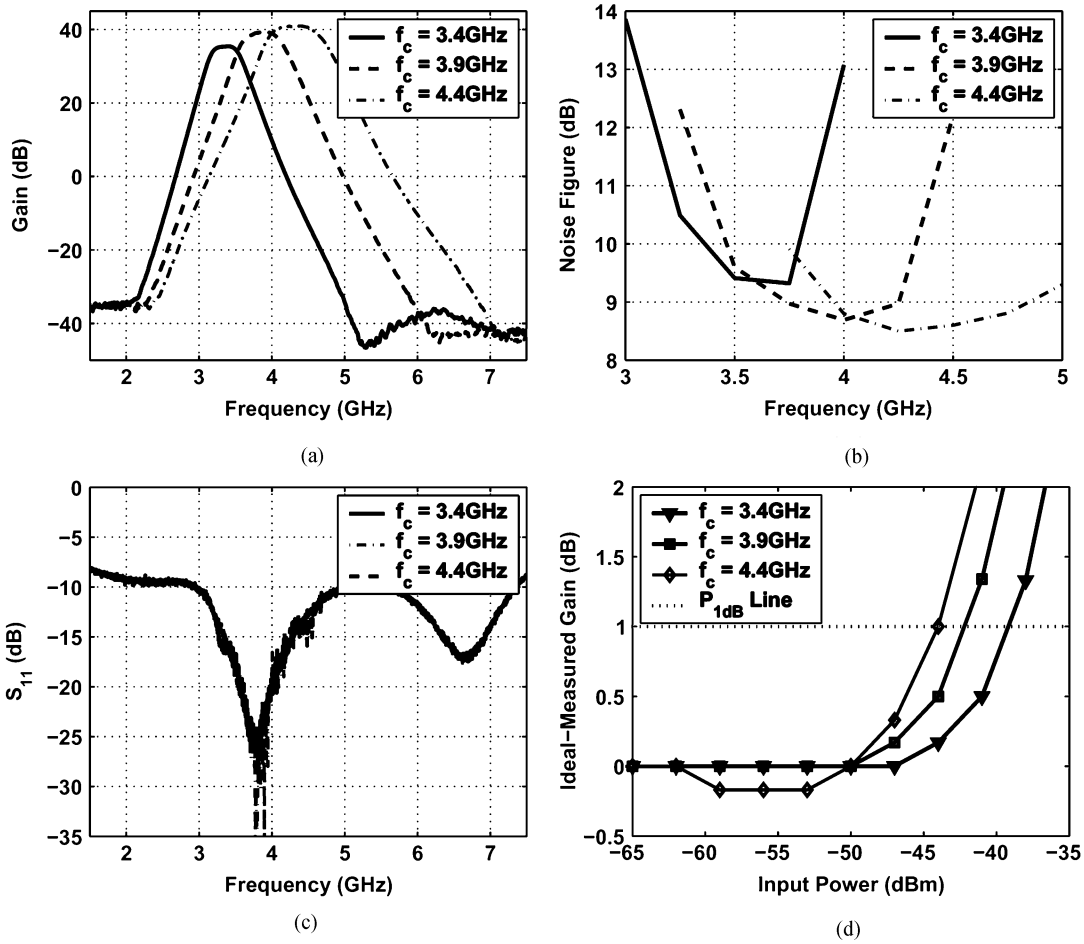


Fig. 11. (a) Gain. (b) NF. (c) S_{11}. (d) $\mathrm{P}_{1\mathrm{dB}}$ in RF front-end.

IV. Measurements

The RFIC is bonded into a QFN 28 leadless package and mounted on an FR4 PCB with one RF input and two differential RF output test ports. The two-layer PCB has a continuous ground plane on the back and the RF traces are 50 Ω coplanar microstrip lines that have ground vias for reliable coplanar grounds. A commercial FPGA to USB2.0 interface board provides digital I/O control to the chip and is where a backend timing acquisition algorithm is implemented [21].

Fig. 11(a) shows the measured transfer response of the RF front-end in each of the three bands. The RF front-end provides up to 40 dB of gain. In the 3.4, 3.9, and 4.4 GHz bands, the -3 dB bandwidth varies from 430 to 715 MHz. The filters roll off rapidly and offer channel selection for out-of-band noise and interference suppression. Fig. 11(b) shows the measured NF of the front-end. In the 4.4 GHz band, 8.6 dB of NF is achievable. Without external matching networks, the packaged chip exhibits -10 dB of matching across the entire 3–5 GHz channel, regardless of subband configuration [Fig. 11(c)]. When the receiver gain is maximized, the input $P_{1\mathrm{dB}}$ compression point is measured to be -39.2 dBm, -42.2 dBm, and -44.2 dBm in the 3.4 GHz, 3.9 GHz, and 4.4 GHz channels, respectively [Fig. 11(d)]. The 40 dB of built-in gain control allows these to be scaled.

To measure BER, the test setup in Fig. 12 is constructed. It is comprised of an arbitrary waveform generator (AWG) that supplies the pulse waveform template generated by Matlab to the vector signal generator (VSG). The VSG up-converts the baseband signal to RF, where the center frequency and power level are easily adjusted. The FPGA board manually synchronizes the received pulse and the relative-compare baseband. Fig. 13(a) shows -99 dBm of sensitivity is achievable for a BER of 10^{-3} at 100 kb/s in the 4.4 GHz band. The sensitivity shifts laterally according to the gain differences achievable in each band. The BER waterfall curves have a more dramatic roll-off for this PPM signal than for a raw coherent signal, because the gain path contains a squared term, which links signal amplitude to achievable gain.

To measure the impact of interferers on BER, the interference generator in Fig. 12 is enabled. The receiver is initially configured such that the BER is at 10^{-5}. Then, the in-band/out-of-band interference tone is activated and increases in amplitude while the BER is recorded. The in-band test reveals demodulator robustness to interference, and the out-of-band interference test reveals channel select filter effectiveness to known out-of-band interferers.

Fig. 13(b) shows how the receiver degrades with an in-band sinusoidal interferer. To achieve 10^{-5} BER, the received power

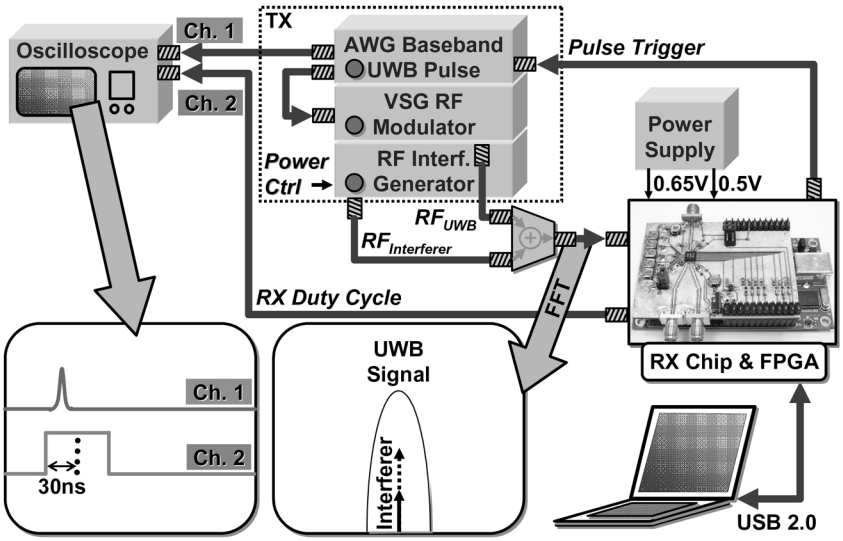
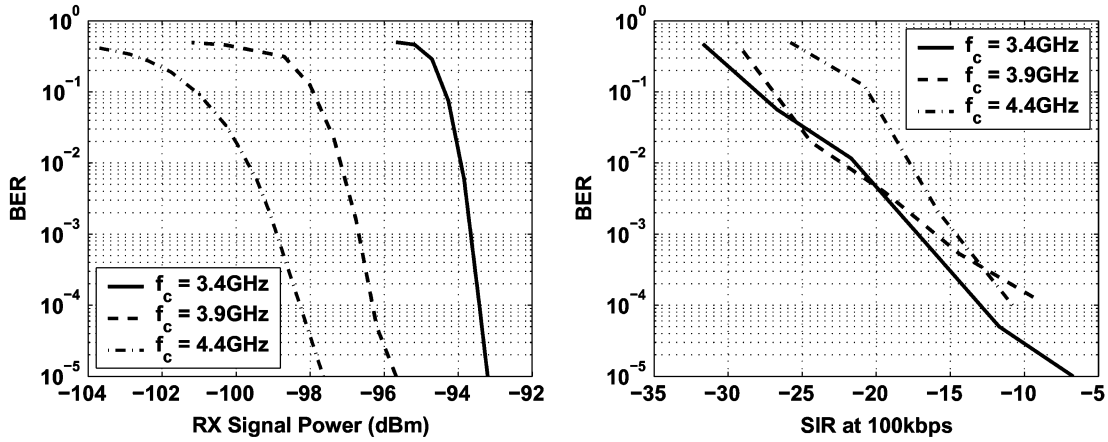


Fig. 12. BER test setup.



(a) (b)

Fig. 13. (a) Sensitivity vs. BER and (b) in-band interferer vs. BER at 100 kb/s.

is set to −98 dBm in the 4.4 GHz band at a data rate of 100 kb/s, translating to a UWB pulse amplitude of 282 μV. For a −15 dB SIR, the −83 dBm interference power translates to a sinusoidal amplitude of 22.3 μV. An explanation for this low tolerance could be attributed to the integration window time. Since the integration window is 15× larger than the pulse width, any noise/interference terms that are sustained through the window period are integrated as undesired energy.

Fig. 14 shows the tests performed for out-of-band interferers at the known 802.11 frequencies and the corresponding results. Again, the received signal power is −98 dBm. In most cases, the receiver can tolerate up to −15 and −20 dBm of interferer power, corresponding to 56 mV and 32 mV sinusoidal amplitudes, respectively. In the 4.4 GHz band, when the interference is set at 5.25 GHz, the tolerable interference power is at −47 dBm, which corresponds to 1.4 mV amplitude. This is due to the relaxed bandpass filter roll-off in the 4.4 GHz band.

A summary of measurements is shown in Table II. Fig. 2 reveals the energy/bit performance of the entire receiver. For a 0.65 V supply, 2.5 nJ/bit is achieved for data rates above 10 kb/s. For rates below 10 kb/s, energy/bit increases as data rate decreases, as the fixed leakage power becomes a more significant portion of the energy consumed per bit. Data is also taken at 0.5 V, and sub-nJ/bit of operation is achievable; however, sensitivity degrades by 15 dB due to reduced front-end gain at the lower supply voltage. To prove the feasibility of the receiver architecture and relative-compare PPM demodulation scheme, a full synchronization algorithm is implemented and verified in an FPGA that interfaces to the receiver [21].

The chip area (Fig. 15) is 1 mm × 2.2 mm. Three separate power/ground supply pairs are on the chip: one for the power-gating buffers when duty-cycling the front-end, another for the RF front-end, and another for the relative-compare baseband. Isolation is accomplished through thick p+ substrate guard rings and separate downbonds for the substrate isolation.

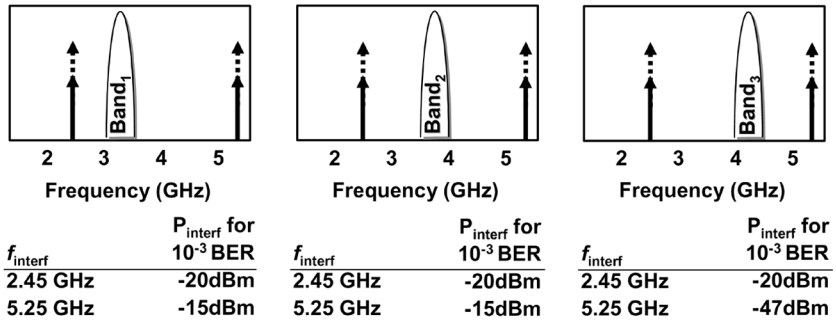


Fig. 14. Out-of-band interference test.

TABLE I
RECENTLY PUBLISHED RECEIVER DETAILS

Paper	Mod.	Sens.	Rate	Power	nJ/bit
Aytur '06 [4]	MB-OFDM	-71 dBm	480 Mbps	330 mW	0.68
Khorram '05 [22]	802.11b	-88 dBm	11 Mbps	165 mW	15
Verma '05 [23]	DBPSK	-75 dBm	1 Mbps	17 mW	17
Emira '04 [24]	802.11b	-86 dBm	11 Mbps	114 mW	10.4
Choi '03 [25]	GMSK	-82 dBm	66 kbps	21 mW	318
Cojocaru '03 [26]	2-GFSK	-91 dBm	1 Mbps	39 mW	39
Chen '06 [16]	OOK, AM	-80 dBm	500 kbps	2.8 mW	5.6
Cook '06 [2]	2-FSK	-98 dBm	300 kbps	330 μW	1.1
Daly '06 [27]	OOK	-65 dBm	1 Mbps	2.6 mW	2.6
Ryckaert '06 [3]	PPM	N/A	20 Mbps	29 mW	1.44
Otis '05 [1]	OOK	-100 dBm	5 kbps	40 mW	80
Jarvinen '05 [28]	2-GFSK	N/A	333 kbps	3.4 mW	10.2
Porret '01 [19]	FSK	-95 dBm	24 kbps	1 mW	41.7

TABLE II
SUMMARY OF MEASURED RESULTS FOR 90 nm CMOS CHIP

UWBRX Chip Info	
Technology	90nm CMOS
Supply	0.65V
Die size	1mm x 2.2mm
Modulation	PPM
Data rate	0-16.7Mbps
Pulse BW	500MHz
f_c subbands	3.4GHz, 3.9GHz, and 4.4GHz
Measured Results	**f_c=4.4GHz, T_{int}=30ns, 100kbps**
Front-end gain	40dB
Front-end NF	8.6dB
Sensitivity (10^{-3} BER, 0.65 V)	-99dBm
Sensitivity (10^{-3} BER, 0.5 V)	-84dBm
In-band SIR for 10^{-3} BER	-15dB
Instantaneous power	35.8mW
Leakage power	3.5μW
Turn-on time	$\sim$2ns
Energy/bit (0.65 V)	2.5nJ/bit
Energy/bit (0.5 V)	0.85nJ/bit
P_{interf} at 2.4GHz for 10^{-3} BER	-20dBm

V. CONCLUSION

A self-mixing, duty-cycled UWB receiver using UWB PPM signaling enables energy-efficient operation at 2.5 nJ/bit for over three orders of magnitude in data rate, ultimately limited by fixed leakage currents at low data rates. A new, low-power, relative-compare demodulator is introduced and achieves -99 dBm of best-case sensitivity for 10^{-3} BER at 100 kb/s. The entire receiver operates from a 0.65 V or 0.5 V supply, and is implemented in a 90 nm CMOS process.

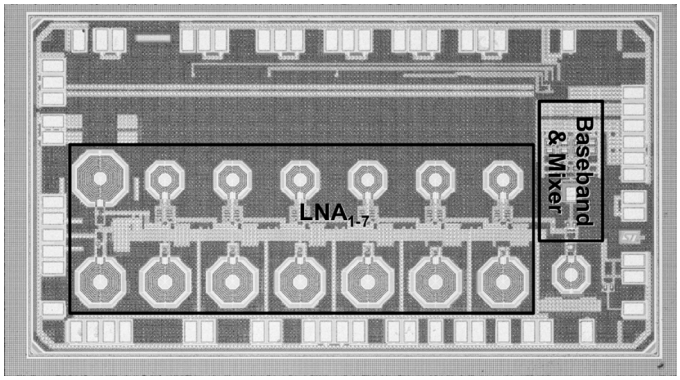


Fig. 15. Die photo.

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