Vibration-to-Electric Energy Conversion

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***Abstract*—A system is proposed to convert ambient mechanical vibration into electrical energy for use in powering autonomous low power electronic systems. The energy is transduced through the use of a variable capacitor. Using microelectromechanical systems (MEMS) technology, such a device has been designed for the system. A low-power controller IC has been fabricated in a 0.6-μm CMOS process and has been tested and measured for losses. Based on the tests, the system is expected to produce 8 μW of usable power. In addition to the fabricated programmable controller, an ultra low-power delay locked loop (DLL)-based system capable of autonomously achieving a steady-state lock to the vibration frequency is described.**

***Index Terms*—Delay-locked-loop, low-power design, low-power dissipation, mixed signal, performance tradeoffs.**

I. Introduction

THE trend in modern VLSI design toward low-power DSP and remote sensing applications creates an opportunity for the exploitation of novel energy sources. The extremely low duty cycle of such systems pushes power requirements of a source into the μW range [1]–[3]. Self-powered systems based on harvesting ambient energy become viable alternatives, eliminating the need for batteries and creating low-maintenance, autonomous systems. Several different ambient sources have already been exploited. These include solar, electromagnetic, RF [4], and mechanical vibration [5]–[7] sources. With advances in microelectromechanical (MEMS) technology, it is possible to implement a self-powered system with the MEMS device acting as an electromechanical transducer in the form of a variable capacitor, with conversion governed by employing low power digital control techniques. This paper presents the design of such a system, with emphasis on the controller IC.

The energy conversion process will be derived in Section II from a generic model of a variable capacitor. Section III will offer backround information into the MEMS transducer. Sections IV and V describe the power and digital electronics that make up the fabricated controller IC. Measured data from this chip in an emulated physical MEMS environment are presented in Section VI. Based on this intial success, a more robust controller is proposed and described in Section VII. Finally, overall conclusions are drawn in Section VIII.

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II. Energy Conversion

The method proposed to convert ambient mechanical vibration into electrical energy is to use a MEMS variable capacitor. By placing charge on the capacitor plates and then moving the plates apart, mechanical energy can be converted into electrical energy which can then be stored and utilized by a load. The system is depicted in Fig. 1. The mechanical system is modeled as a vibration source which couples into the electrical system through the MEMS transducer. A low-power controller directs energy conversion and supplies power to the load. The controller consists of a power electronics subsystem which is responsible for exciting the transducer through its energy conversion cycle, and has been optimized to minimize losses, and a digital control core which generates the timing pulses which drive the gates of the power FETS in the power electronics subsystem.

There are two possible energy conversion cycles in the charge-voltage plane for the MEMS transducer as shown in Fig. 2. Path A-B-D-A depicts charge constrained conversion, while path A-C-D-A depicts voltage constrained conversion. The name of the path depicts which property is held constant during the conversion process while the other changes in response to a varying capacitance. One basic constraint for both cycles is that there is some maximum allowable voltage, $V_{\max}$, which is set by some process or system requirement. For example, the power switches which are employed in the converter will have some oxide or channel breakdown limit which must be considered. Also, the MEMS device itself will have a maximum field limit which it can withstand when its plates are closest together.

For the voltage constrained case, the cycle starts when the capacitor is charged up to $V_{\max}$ from a reservoir. This is done when the capacitance of the MEMS transducer is at a maximum $(C_{\max})$. During this time, the value of C_{MEMS} is taken to be constant, and so segment A-C is a straight line. This is a valid assumption since the charge-up time to traverse path A-C (and discharge path D-A) is an electrical time near 600 ns, while path segment C-D, which corresponds to the plates moving, is traversed over a mechanical time near 400 μs. It is evident from the figure that during this step in the conversion process, the voltage is held constant. (Hence the name voltage constained conversion.) As the plates move and the capacitance decreases, path segment C-D is traversed, where the capacitance is at a minimum. The mechanical force does work by causing charge to move from the capacitor back into the reservoir. The charge remaining on the plates is then recovered while $C_{\mathrm{MEMS}} = C_{\min}$ following path D-A. The net energy gained, E_{voltcons}, is the shaded area ACD in Fig. 2 [8]

$$E_{\mathrm{voltcons}} = \tfrac{1}{2}(C_{\max} - C_{\min})V_{\max}^2. \tag{1}$$

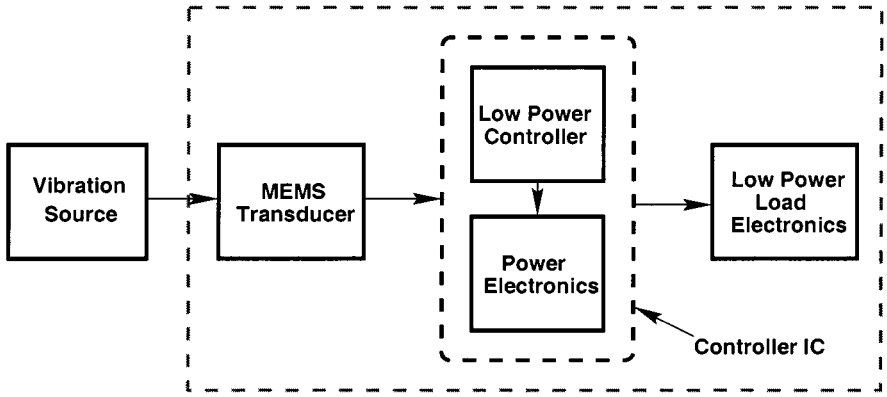

Fig. 1. System block diagram.

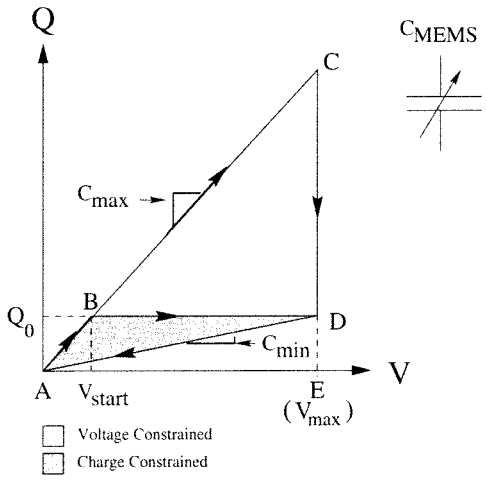

Fig. 2. Conversion cycles.

This method sets a maximum limit on the conversion process. The major obstacle for this approach is that some method must be employed to hold the voltage across the MEMS device constant during the conversion process, which would require another source of value $V_{\max}$. This is an additional source to that of the conversion charge reservoir, which is of a lower voltage and is also used to power the control electronics. It is desirable to perform the conversion with a single source. This means that there are two relevant voltage rails in the system. The first is V_{dd}, which supplies the control electronics with power and is a constant rail at 1.5 V in this application. It is represented in the circuit diagram of Fig. 6 by C_{res}, the charge reservior. The second rail is equal to $V_C = V_{dd} + V_{\text{MEMS}}$, where V_{MEMS} is the voltage across the MEMS capacitor and changes during a conversion cycle. This voltage is also depicted in Fig. 6.

In the charge constrained case, C_{MEMS} is charged to some initial voltage while its capacitance is at a maximum, which corresponds to path segment A-B in Fig. 2. As the capacitor separates, the voltage increases as capacitance decreases until the plate displacement is at a maximum ($C_{\text{MEMS}} = C_{\min}$) at point D. The amount of charge initially placed on the plates was precalculated such that when C_{MEMS} reaches its minimum, the value of the voltage across the capacitor is $V_{\max}$. During the transition from point B to D, the MEMS device is isolated (open-circuited) with respect to the rest of the system so that no current path exists. It is forced to hold its charge, and as C decreases, V must increase to satisfy $Q = CV$. The charge is then returned to the reservoir along path D-A. The net energy out is the shaded area ABD. It is immediately obvious that this energy is less than what is possible with the voltage constrained conversion cycle. This energy may be expressed as

$$E_{\text{chrgcons}} = \tfrac{1}{2}(C_{\max} - C_{\min})V_{\max}V_{\text{start}}. \tag{2}$$

Comparing (1) to (2), it is clear that the energy available from the charge constrained case is less than that available from the voltage constrained case by a factor of $V_{\text{start}}/V_{\max}$. The advantage of this approach is that now only a single charge source is needed to begin the process, and its value can be much less than $V_{\max}$.

Fig. 3 depicts a hybrid alternative. Here, a second capacitor of constant value, C_{par}, has been added in parallel to the MEMS device. Path a-b-d-a represents conversion without C_{par} and path a-b'-d'-a includes C_{par}. The energy converted in shaded area acda, E'_{voltcons} equals the converted energy of shaded area ac'd'a, so no benefit for the voltage constrained cycle has been gained by incorporating C_{par}. However, if the energy converted for charge constrained cycles abda and ab'd'a are compared, it is evident that more energy, E'_{chrgcons} is converted in area ab'd'a. Comparing charge and voltage constrained energies with C_{par} present, we find

$$E'_{\text{chrgcons}} = E'_{\text{voltcons}} - \frac{(\Delta Q)^2}{2(C_{\text{par}} + C_{\max})}. \tag{3}$$

Equation (3) shows that in the limit as C_{par} approaches infinity, the charge constrained energy approaches that available through voltage constraint. Therefore, it is desirable to have a parallel capacitor to, in effect, "hold" the voltage across the MEMS device constant, mimicking the behavior of the voltage constrained condition. The disadvantage to adding C_{par} is that now more initial charge is required for the conversion process. This means that the losses associated with the reactive energy flow in the system will be increased. The tradeoff between increasing the capacitance of C_{par} and the increase in losses will be discussed in detail in Section IV. An added benefit of this

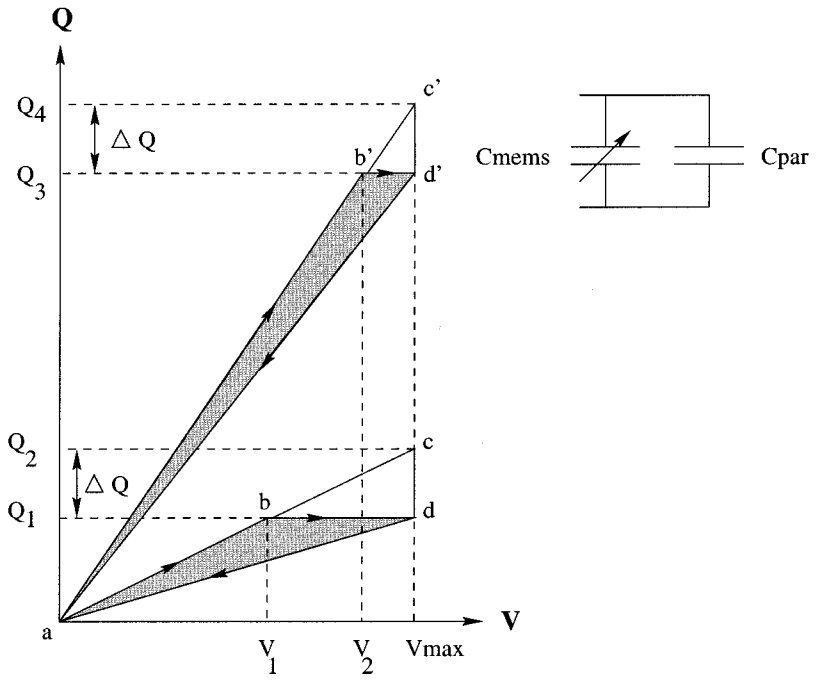

Fig. 3. Modified energy conversion with $C_{\rm par}$.

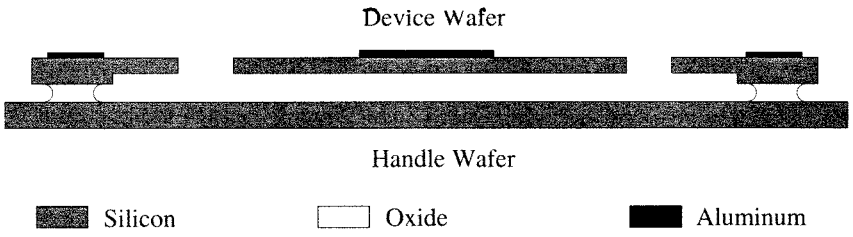

Fig. 4. MEMS device side view (not to scale).

final analysis is that the parallel capacitor may be included in the design essentially for free by exploiting the parastics that will exist between the MEMS device and its substrate. By tailoring the bonding oxide thickness between the two wafers making up the MEMS device, as will be dscribed in Section III, $C_{\rm par}$ can be set to the desired value.

III. MEMS Device

The variable capacitor will be implemented using MEMS technology, as shown in Figs. 4 and 5. The capacitor has been analyzed and designed, and is now in fabrication. It will consist of a 1.5 cm-by-0.5 cm silicon structure etched in a wafer of 500 μm thickness through a deep-reactive-ion etching process [9], as shown in Fig. 4. The device wafer will be supported by an identical silicon handle wafer. The two wafers will be separated by a thin layer of silicon dioxide. The silicon will be heavily doped so that it acts as a very good conductor. The silicon dioxide acts as an insulator, thus forming a parasitic capacitor between the device and the handle wafer. The width of the silicon dioxide layer can be controlled to set the value of this parasitic capacitance as desired. The advantages of this parasitic capacitance were explained in Section II.

A plan view of the MEMS capacitor is shown in Fig. 5. It consists of three basic parts: a floating mass, a folded spring (one per side), and two sets of interdigitated combs, one per side. Each spring consists of four spring bars, a free rigid beam, and a rigid anchor. The spring bars are connected to both the anchor and the free beam, limiting the motion of the mass to one dimension, as indicated in the figure.

The interdigitated combs form two variable capacitors by connecting one terminal to the moving mass at the anchors and the others to each of the stationary combs. Since the characteristics of the variable capacitors are identical, the analysis in this paper will focus on one of the variable capacitors and only one set of interdigitated combs. Note that the output power for one device can be doubled by taking into account the power obtained from the two variable capacitors.

The spring-mass system is designed to resonate with a mechanical vibration source applied to the casing to whom the anchors are attached. The converter described here is designed for a mechanical vibration of 2520 Hz. The source is the well-established harmonic of an engine's vibration spectra. The transfer of energy from the source to the spring-mass system is maximized by tuning the resonant frequency of the spring-mass system to that of the vibration source. This can be achieved by varying the

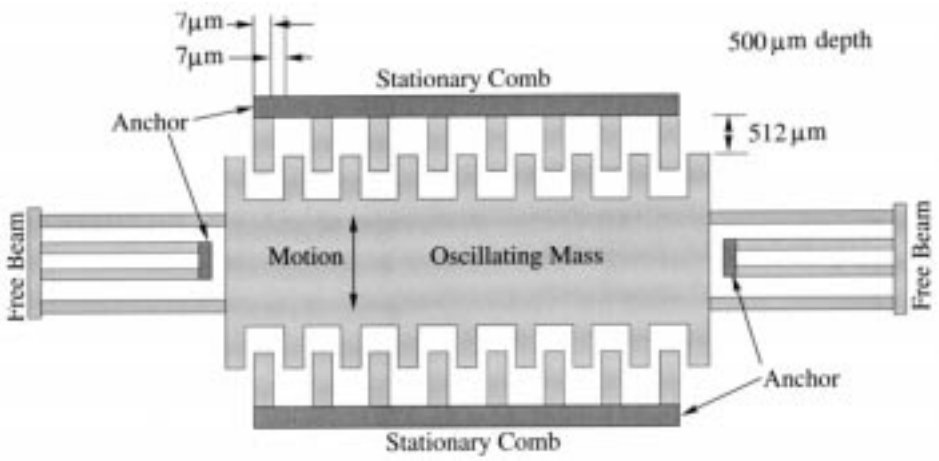

Fig. 5. MEMS device plan view (not to scale).

dimensions of the spring in order to change its effective spring constant, or by changing the mass of the moving element.

As the mass oscillates, the interdigitated combs move together and apart, effectively varying the area of the variable capacitor, and, thus, its capacitance. The transfer of energy from the spring-mass system to the electrical circuit is governed by the change in capacitance of the interdigitated combs, as viewed from their electric terminals. In order to maximize this energy transfer, the change of capacitance must be maximized given constraints of space and structural soundness. In fact, one of the fundamental challenges in the design of the MEMS device is to provide a large enough change of capacitance given the design constraints. A large change of capacitance can be obtained by: 1) reducing the gap between the opposing elements of the comb structure; 2) increasing the height of the device; 3) elongating the fingers of the comb structure; and 4) increasing the length of the comb structure.

The minimal gap is limited by device fabrication technology. The current state-of-the-art sets this limit at around 7 μm. This minimal gap limits the height of the device. As the height of the device increases, the minimal gap increases. It is expected that a 7-μm gap may be etched as deep as 500 μm. Spring travel and structural resonance limit the length of the fingers in the comb structure. Note that as the length of the combs is increased, the travel of the spring must also increase. Also, the combs' natural resonant frequency decreases as they become longer. Given a minimal width for each comb finger of 7 μm, a length of 512 μm is required in order to keep the combs' natural frequency ten times larger than the mechanical vibration frequency to ensure the physical integrity and proper operation of the device. A spring with a peak-to-peak travel of 512 μm appears feasible. The length of the comb structure is constrained by the dimensions of the spring and the overall device. As the length of the comb structure is increased, so does the moving mass. In order to keep the spring-mass system tuned to the desired frequency, the spring must be stiffened accordingly. However, the stiffness of the spring is limited by the length of the spring. As the spring gets longer, other undesirable modes of vibration are introduced. Furthermore, the dimensions of the device are specified to fit inside a 1.5 cm-by-1.5 cm square, including the springs. After an optimization is performed, the optimal size for the mass is found to be 1cm by 0.3 cm. Given the previous constraints of gap size and comb finger width, each comb structure can have about 400 individual comb fingers.

An analysis of the capacitance with the comb structure fully closed yields a value of 260 pF. Similarly, the value of the capacitance with the comb structure fully open is approximately 2 pF. The analysis and design of the control and power electronics is based in these two values with a maximum gap voltage of 8 V.

IV. Power Electronics

Fig. 6 shows the implementation of the converter and accompanying waveforms associated with timing and system state variables. This represents one phase of the conversion process, as described in Section III. The complete circuit would simply be Fig. 6, with a counterpart mirrored about the load and control electronics. For all discussions of its operation, we will recall that the resonant LC time constant is much shorter than the vibration period. This is represented by the break on the time axis.

At startup, the capacitor combination of $C_{\rm par}$ and $C_{\rm MEMS}$ has no voltage across it, so $V_C = V_{DD}$. (Note that all voltages in Fig. 6 are referred to ground.) At this point, the power electronics are waiting for the controller to determine when $C = C_{\max}$ to begin the conversion process. Currently, this is an external signal input to the controller. This trigger occurs at the beginning of t_1. During t_1, SW2 is on, SW1 is off, and the inductor current increases. At t_2, SW2 is off, SW1 is on, and the inductor transfers energy to the capacitor. During t_3, both switches are off and the variable capacitor plates move. This time constant is near 400 μs while the resonant on time of the switches is approximately 600 nS. It is therefore a reasonable approximation to say that the MEMS capacitor value is constant during t_1, t_2, t_4, and t_5. During t_3 the plates move from their minimum separation $(C_{\max} + C_{\rm par})$ to their maximum separation $(C_{\min} + C_{\rm par})$. The mechanical energy has moved the plates apart and caused the voltage across the capacitor combination to reach a maximum, and the energy harvesting is performed. During t_4 SW1 is on, SW2 is off, and the capacitor combination transfers energy to the inductor. Note that this LC time constant is smaller than t_2 because the overall capacitor value has decreased. Once the capacitor voltage reaches zero, corresponding to one-quarter of the

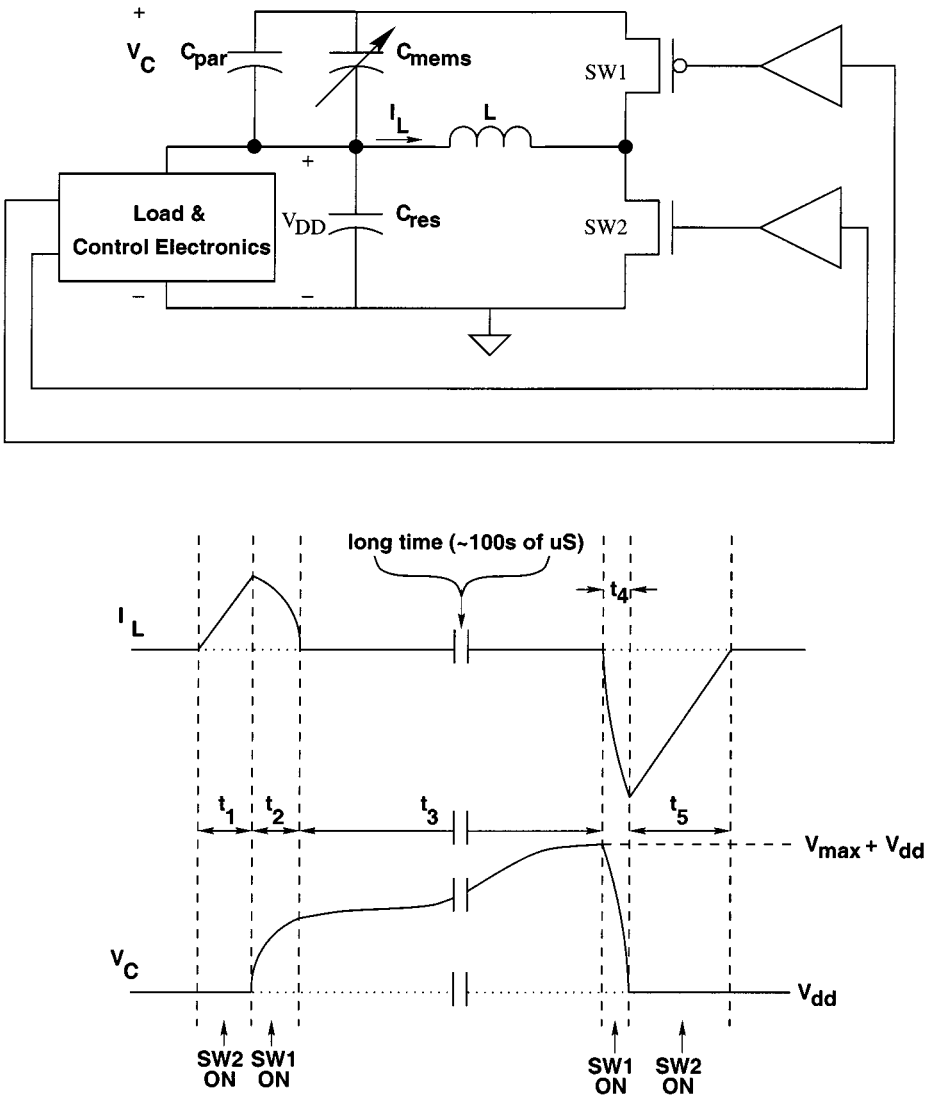

Fig. 6. System implementation and timing waveforms.

resonant period of the LC, SW1 is turned off, SW2 is turned on, and the energy put into the inductor is transferred to the reservoir during t_5. This process repeats at the frequency of the mechanical vibration, which corresponds to variations in $C_{\rm MEMS}$. The overall system gains energy when the losses associated with the conversion process are less than the harvested energy. Because the values of $L, C_{\rm min}, C_{\rm max}$, and $C_{\rm par}$ are known, the timing pulses can be set such that synchronous rectification may be used, eliminating the need for diodes across SW1 and SW2. The main loss mechanisms in the conversion are switching and conduction losses associated with the power FETs and conduction losses in the inductor.

As stated in Section II, it is desirable to have a large valued capacitor in parallel with the MEMS device to improve energy conversion. This requires that more charge be initially placed on the capacitor plates, as shown in Fig. 3. There is a practical limit to this charge due to the losses that occur in the inductor and SW2. They will have some series resistances, R_L and R_{DS}, respectively, and this will limit the maximum value of current that the inductor will ramp to, and therefore the initial energy that can be placed into the system. This maximum current will be $I_{L\,\max} = V_{DD}/(R_L + R_{DS})$, where V_{DD} is the supply voltage. Since the main job of the inductor is to act as an energy source for the capacitor combination, $(C_{\rm MEMS} + C_{\rm par})$ this is taken into account when sizing L. The limits on the MEMS capacitor, $C_{\rm min}$ and $C_{\rm max}$ are fixed, so what really needs to be looked at is the relationship between L and $C_{\rm par}$. To do this, a mathematical model of the system was used along with real inductor specifications. This is depicted in Fig. 7. L was modeled as the nominal values from the specifications, and $C_{\rm par}$ was varied to observe performance. Fig. 8 shows optimization curves for $C_{\rm par}$ for three values of L, as well as the case where L and SW2 are lossless.

The peaking in the curves show that after some optimal value of $C_{\rm par}$ the system gains less energy. This is due to the increased conduction losses in the inductor and power FETs (which are

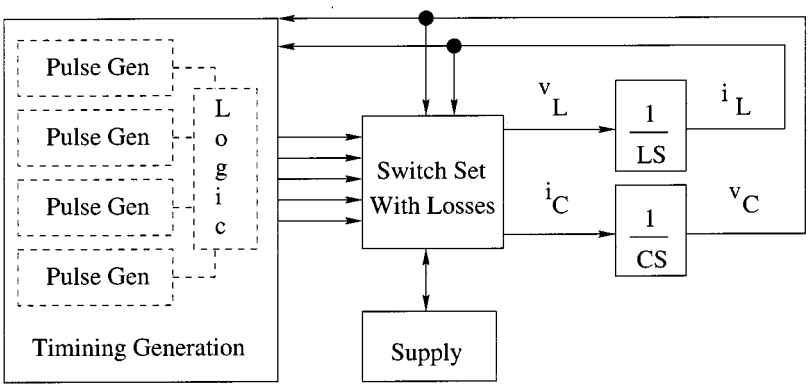

Fig. 7. Model used for analysis.

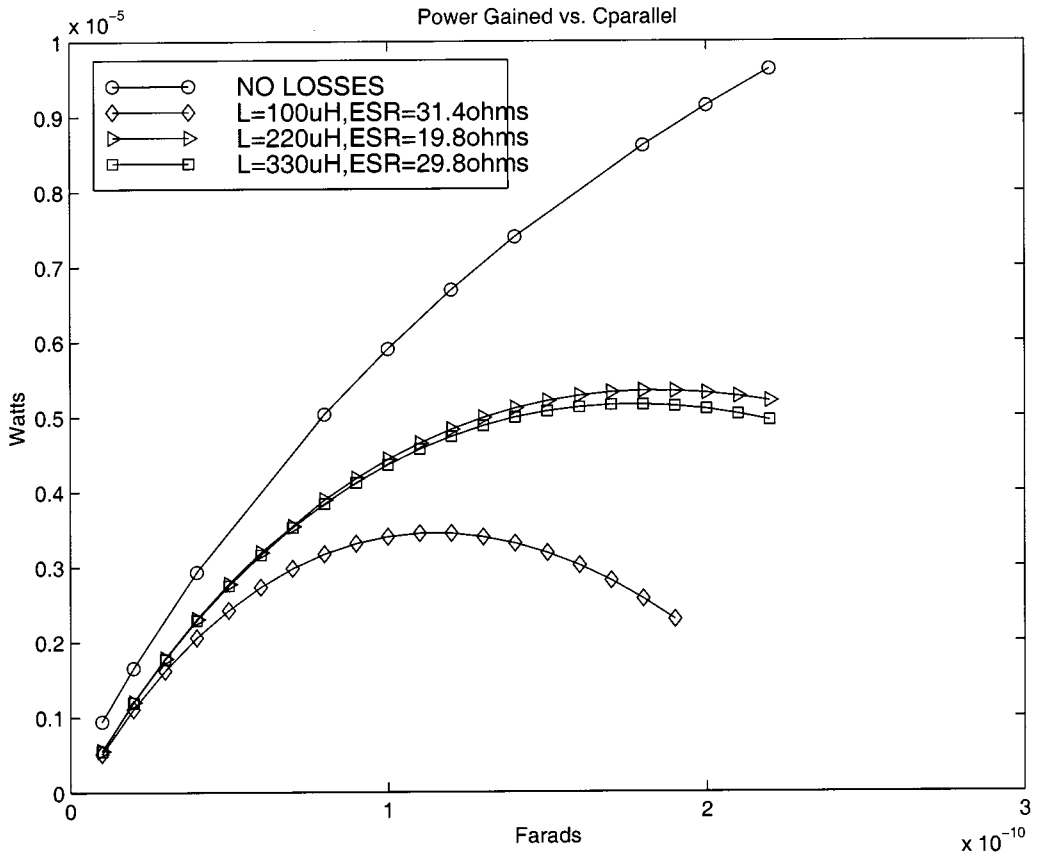

Fig. 8. $C_{\rm par}$ optimization curves.

also included in the model). We arrive, therefore, at $C_{\rm par} = 180$ pF and $L = 220$ μH. The lossless case was included to verify that as $C_{\rm par}$ was allowed to go to infinity, the energy out equaled that possible with a voltage constrained approach as discussed in Section II. This was used to validate the model.

A straightforward approach to optimizing transistor width has been developed [10]. (In general it is assumed that the FETs will be sized to minimum or near minimum lengths and appropriate widths. The choice between minimum or nonminimum gate length depends on the voltages in the system and whether or not short channel effects are a concern.) This approach models the FETs as being in the linear region during operation with some constant gate drive V_{GS}. This model forms a useful basis for analysis of our converter but will offer better results if the assumptions are modified to provide for a gate drive that varies over the course of one conversion period. This modified model more accurately reflects our converter as shown in Fig. 6, where the PFET gate drive is given by $-V_C$. The power, $P_{\rm tot}$, dissipated by a FET over the course of one switching period is given by

$$P_{\rm tot} = I_{\rm rms}^2 R_{DS} + f_{sw}\left(C_{GS}V_{GS}^2 + C_{\rm dyn}V_{\rm dyn}^2\right) \qquad (4)$$

where the first term represents conduction losses (P_{cl}) and the second, lumped, term represents switching losses (P_{sw}). $I_{\rm rms}$ is the rms current through the device, R_{DS} is the on resistance

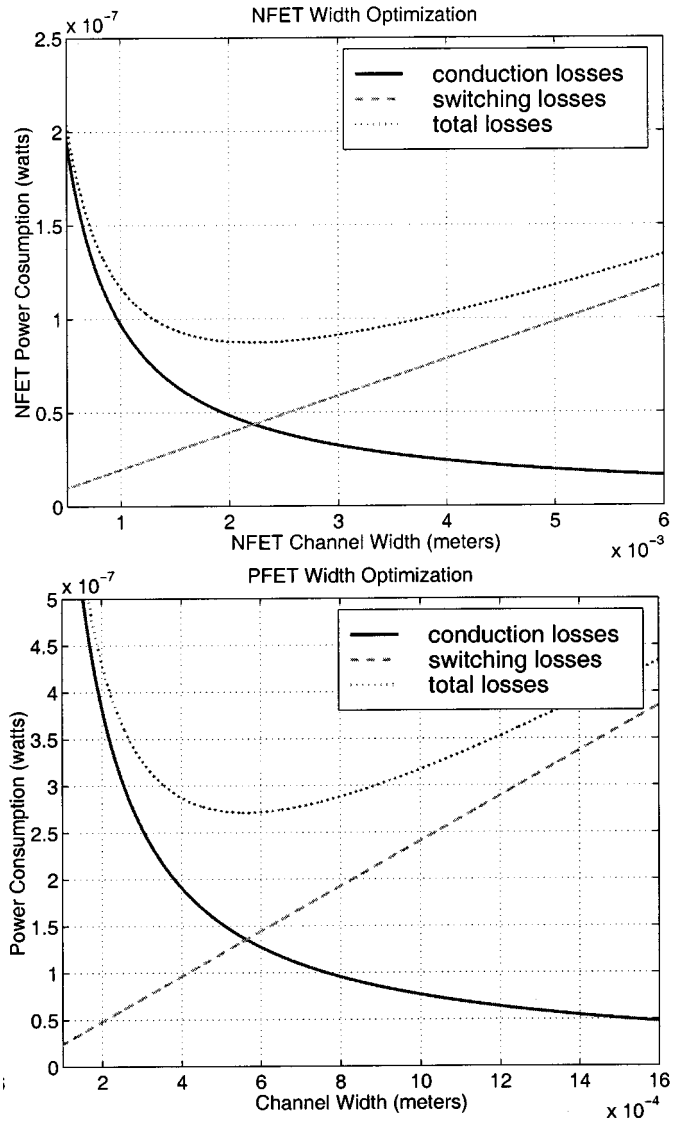

Fig. 9. Switch optimization curves.

of the FET, f_{sw} is the switching frequency, C_{GS} is the gate capacitance, V_{GS} is the gate drive voltage, $C_{\rm dyn}$ is the capacitance of the switched dynamic drain or source node, and $V_{\rm dyn}$ is the voltage the dynamic node is switched at. It is possible as in [10] to make some simplifications to the power loss optimization problem. The first is to combine the gate and drain or source capacitances if the drain and source extensions are roughly equivalent to the gate area. Also, if a further restriction on the system is that the gate drive voltage is always the same and is roughly equal to the switched voltage at the dynamic node, then the two lumped switching terms in (4) may be linearly combined to produce a simpler equation. For our system, this is not true. If we refer again to Fig. 6, we see that the PFET causes special conditions to occur. For proper operation, it must be ensured that during t_3 the PFET is off. This requires that there be a level converter driving its gate since the dynamic capacitor voltage V_C will start off at V_{DD} and increase to some $V_{\rm max}$. This means that the PFET has a much higher gate drive during t_4 than during t_2. Fig. 9 shows optimization curves for the power switches with the difference in gate drive accounted for.

The values obtained from Fig. 9 are $W_P = 538\ \mu$m and $W_N = 1399\ \mu$m. Unlike previous complementary switcher designs [1], [10] the PFET is actually smaller than the NFET for minimal power losses. This is due not only to the fact that the PFET experiences higher gate drive for half of its switching duties, but also because of the fact that the NFET passes higher rms currents. One characteristic to note is that the curves, especially for the NFET, exhibit shallow troughs. This means that a value off of the optimum can be taken to save area at a very low power cost. Also, some of the power that appears to be lost by going to a shorter width is actually saved because the buffers needed to drive the power FETs' gates, as depicted in Fig. 6 can become smaller. (The buffer losses were not included in the optimization algorithm because their sizing is dependent on the power FETs' width.)

V. Controller Architecture

In order to experimentally verify the validity of the proposed method, a programmable controller was developed based on the mathematical model of Fig. 7. Because the important system parameters $L, C_{\rm par}, C_{\rm max}, C_{\rm min}$, and f_{sw} are known, the timing pulses can be realized through the use of a programmable delay line. The block diagram for a single pulse generator is shown in Fig. 10. This is a hybrid delay line design which combines the area savings of a fast clocked counter approach with the resolution flexibility of a tapped delay line. The counter acts as a coarse adjust while the tapped delay line is used to fine tune the pulsewidth. The delay time for the counter block is set by comparing the count to some reference value. Once this has occurred, a pulse is sent down the tapped delay line and is picked off by a multiplexer. This sets the overall delay time. A simple power saving technique is to use an AND gate tied to the MSB of the multiplexer selects and placed in the middle of the delay line to decide whether the pulse propagates to the second half of the line. In cases where the MSB is not selected, this prevents half of the delay line buffers from needlessly switching. It would be possible to gate all of the buffers in the delay line, but the additional overhead associated with decoding the multiplexer selects to vary the delay line length may make this approach undesirable.

VI. Experimental Data

The programmable controller and associated power electronics have been implemented in a 0.6-μm CMOS process. Fig. 11 shows a photograph of the controller IC. This represents one-half of the total circuit. As stated in Section III there are two phases of conversion; the controller IC was designed for a single phase. In order to extend the design for both phases, the present layout may simply be duplicated and will fit in the same area since the IC was pad, not area, limited. The system has been tested for functionality and the controller measured for losses. At the time of this writing the MEMS device is not available in the system, so a constant value capacitor was used in its place to verify correct operation. To verify nonbreakdown of the power switches, a dc source was switched in during t_3 of Fig. 6 to emulate the MEMS device's behavior.

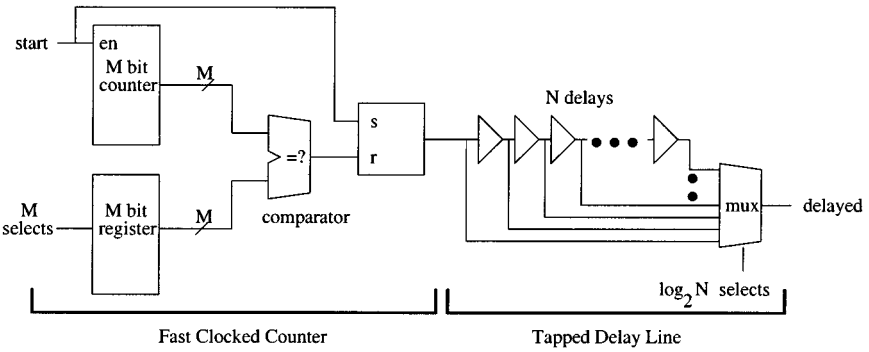

Fig. 10. Controller block diagram.

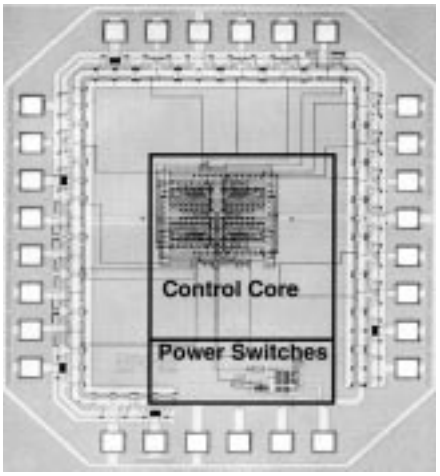

Fig. 11. Controller block diagram.

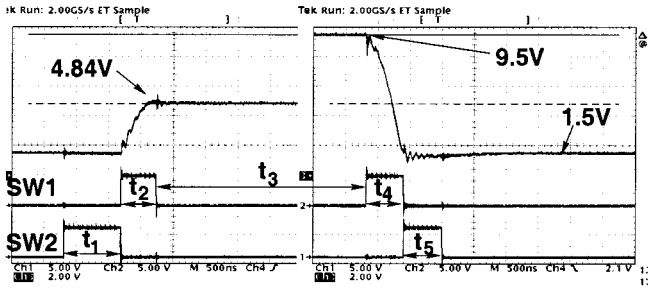

Fig. 12. Experimental waveforms.

Fig. 12 depicts the correct operation of the controller. Using this switched-supply test methodology allows for full characterization of the controller under circumstances equivalent to the MEMS being present in the system and represents a more valid excercising of the controller than simulations alone would allow. Table I presents the relevant data taken during controller testing. All power values in the table may be doubled to account for both phases of the conversion period. Therefore, we may expect approximately 8.6 μW out of the system at a $\Delta V_{\mathrm{MEMS}} = 8.0$ V.

TABLE I
CONTROLLER SPECIFICATIONS (HALF CIRCUIT)

Area	2163μm x 2554μm
Transistor Count	2661
Process	0.6μm CMOS
Predicted Converted Energy	8.66μW
Core Power	500nW ($f_{vib} = 2.5$kHz, $V_{dd} = 1.5$V)
Switch Loss Power	3.87μW ($\Delta V_{MEMS} = 8.0$V)
Predicted Power Out	4.29μW ($\Delta V_{MEMS} = 8.0$V)

VII. ENERGY FEEDBACK CONTROL

The fabricated controller does not have the ability to lock to the capacitor motion automatically. While this could be a requirement placed on the load electronics, it is desirable to give the controller the ability to determine when to initiate conversion. This implies some method of feedback which the controller can use to lock its conversion process to the phase of the plate motion.

Since the energy available for conversion in the system is limited to an ideal maximum value of $(1/2)(C_{\max} - C_{\min})V_{\max}^2 = 42\ \mu$W, the overhead associated with the controller feedback must be minimized. In fact, as we have seen from Section VI, even with the system optimized to provide for maximal energy output, the converted mechanical power is only on the order of 10 μW, so the restrictions on controller consumption are very strict.

The architecture for generating timing pulses used to drive the power FETs has been discussed in Section V. It is now desired to generate conversion initialization pulses which correspond to C_{mems} being at a maximum and at a minimum. The method chosen to do this is to use a modified form of a delay locked loop (DLL), where a reference clock with a period equal to the desired mechanical vibration frequency, T_{vib}, is phase-locked to the capacitor plate motion. A DLL architecture was chosen because of its amenability to ultralow power implementation through the use of appropriate delay line architecture. A block diagram of the loop is shown in Fig. 13.

A tapped delay line delays the reference clock by an amount set by the feedback mechanism. The feedback employed is to measure the energy converted in a given period at a given delay and compare it to the energy converted over a period at a different delay. By using the delay value which corresponds to the global maximum value of energy converted over a period, the system can attain phase lock.

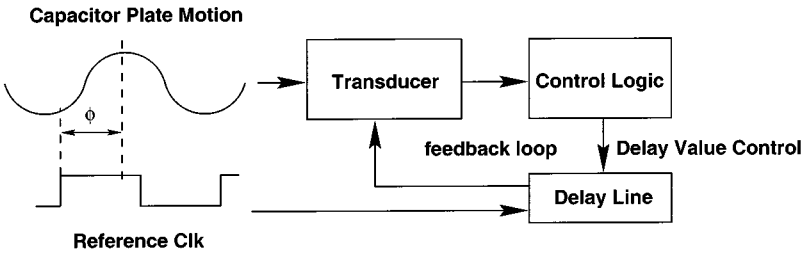

Fig. 13. DLL block diagram.

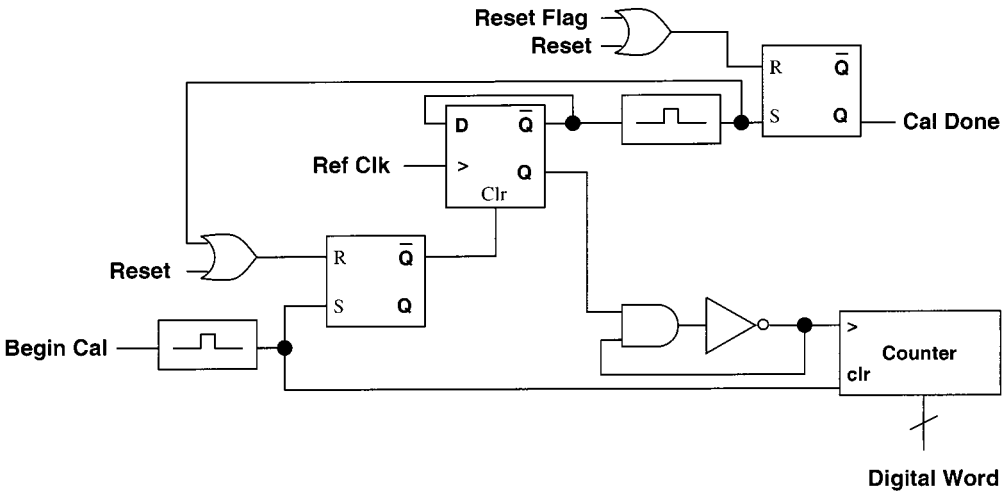

Fig. 14. Single period calibration circuit.

The length of the line is variable in two respects. First, the total number of taps in the line is calibrated at startup to just equal a reference clock period (or, in actual implementation, half-period), and second, once lock is attained, unused taps are prevented from toggling. This is in order to save power during both locking of the loop and steady-state operation.

Since the power budget for the system is low, analog techniques are not used to calibrate the total delay of the line to the reference clock period. Fig. 14 shows a circuit that allows the calibration of the delay line length to occur in one reference period. The flip–flop combination creates a pulse of a duration equal to one clock period (note that both flops must be cleared prior to calibration) which enables a ring oscillator. This oscillator consists of a ring of inverters whose period equals one tap of the delay line. The counter then tracks how many taps are required to equal one reference clock period. There will be steady state error, but since the oscillator is enabled by the reference clk, it is assured that the error will be some fraction of a single delay tap. The calibration code word is stored in a register, to be used by the phase locking algorithm. The major benefit from (periodic) calibration is that the effects of process, supply and temperature variations may be eliminated. In addition, calibration assures that when phase locking is performed, only a single reference clock period is sampled over, saving power.

A. Delay Line Architecture

A binarily weighted delay line was ultimately chosen for reasons discussed in [11] and is depicted in Fig. 15. In this instance, binarily weighted delays are used to vary the line length, where the weighting is achieved by replicating unit delays. The decode logic is simple here, and in steady state no extra transitions will occur. A simple circuit trick to decrease the required delay line length is to use an XOR gate in series with the reference clock. The XOR allows a modification to the lock algorithm. Now, a half-period of the reference period is sampled over with the clock simply buffered by the XOR gate. After this half-period window is over, the clock polarity is flipped by asserting an InvPol signal, which gives a half period phase shift "for free." A second half-period is sampled with this negative clock phase. After this window is over, a comparison is performed between the maximum counts of each clock polarity, and the overall maximum is chosen. This halves the required length of the delay line.

B. Energy-Based Feedback

In order to attain phase lock between the reference clock and capacitor motion, energy feedback is utilized. For the lossless case, the relationship between energy out and phase delay between the reference clock and vibration is

$$E_{\text{out}} = \frac{1}{2}\,\frac{C_1(t_d) - C_2(t_d)}{C_{\text{par}} + C_2(t_d)}\,Li_{\max}^2 \tag{5}$$

where $C_1(t_d)$ and $C_2(t_d)$ are the values of the MEMS capacitance when the conversion process is started and completed as functions of delay time, t_d, and ideally $C_1(t_{\text{nom}}) = C_{\max}$ and $C_2(t_{\text{nom}}) = C_{\min}$ where t_{nom} is the optimal value. This relationship is depicted in Fig. 16. The rule here is that the values

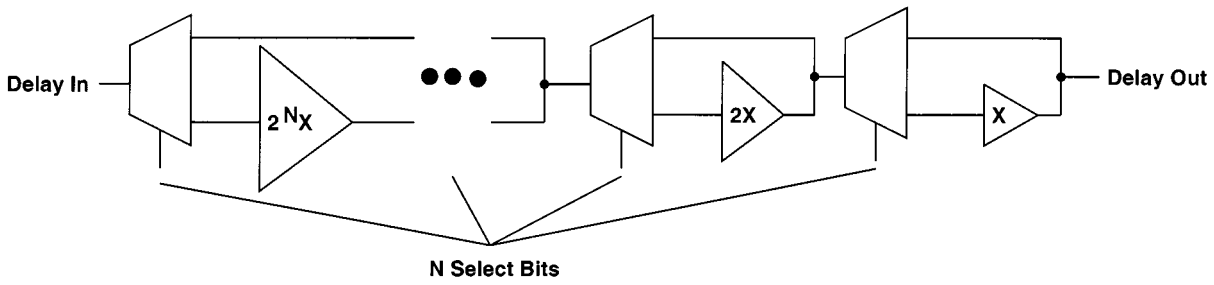

Fig. 15. Binary weighted delay line.

for t_1, t_2, t_3, t_4, and t_5 are constant. These timing pulsewidths are dependent on the values of the inductor, external capacitor, $C_{\rm par}$, and vibration frequency and are independent of phase. By moving this window of pulses in phase, different output energies are obtained. In order to give a qualitative description as to how the energy output varies with delay, the value of capacitance of the MEMS device has also been plotted. As expected, at integer multiples of delay equal to the vibration period, $T_{\rm vib}$, energy output is at a maximum, and at integer multiples of $T_{\rm vib}/2$, energy output at a minimum. Fig. 16 shows that there is a window W of delay values about the optimum value for which the energy out is still relatively large. This suggests that if the system is initially locked to the maximum value, phase and/or frequency drift can be tolerated in the reference clock. Once the energy converted drifts out of the acceptable window area, the system should be relocked. This eliminates the need for continuous feedback. Ideally, if the reference clock matches the vibration frequency exactly, the delay value will never need to be updated and feedback control is only implemented once, since storage of the lock control code for the delay line is done digitally. In a practical system, the feedback update time will be dependent on the frequency difference and phase drift between the reference clock and mechanical vibration. The requirements on the controller for re-lock are discussed in greater detail in [11].

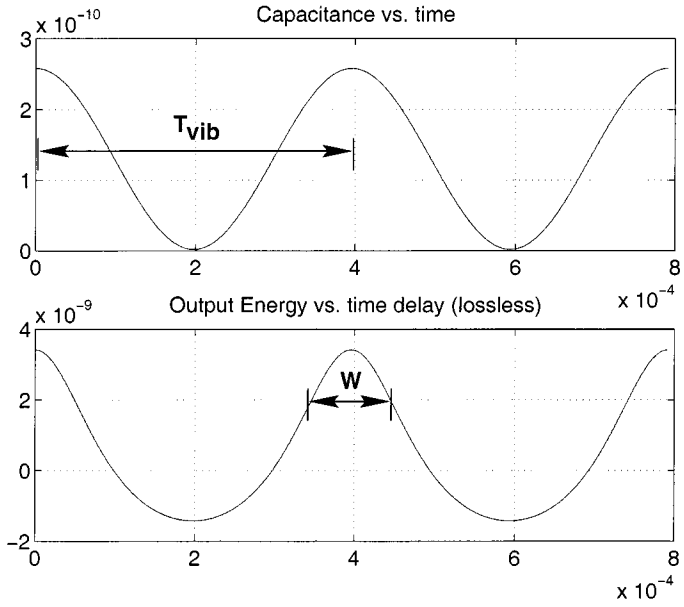

Fig. 16. Energy out versus delay.

C. Energy Measurement

The feedback variable used is the energy converted during a period. The method proposed to measure this energy is depicted in Fig. 17. During t_5 of the energy conversion cycle as described in Section II, the inductor would normally return the converted energy to the source. During the phase lock sequence, the converted energy is instead integrated onto a measurement capacitor, $C_{\rm meas}$. After t_5 is over, $C_{\rm meas}$ is used to power a ring oscillator which in turn clocks a counter. The final value of the count over a sampling window gives a measure of the energy converted. This can then be used to lock to some maximum value of energy converted, corresponding to the reference clock being in phase with the mechanical vibration.

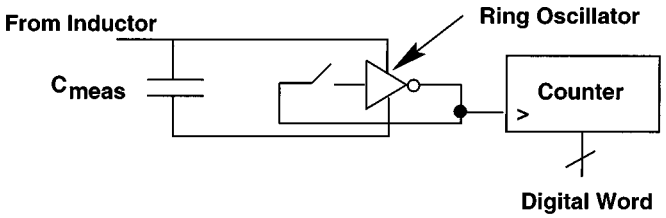

Fig. 17. Energy measurement circuit.

D. Feedback Algorithms

Once the measurement technique has been established, it is necessary to evaluate different methods for utilizing this information to achieve phase lock. Closed-loop response analysis was done by using the previously developed models for the power electronics portion of the converter and including models for the energy feedback using the MATLab Simulink package. Fig. 18 shows one possible approach. The top trace represents the total value of the delay, the sinusoidal wave is the capacitor value, and the square wave is the reference clock. Here, a counter is used to keep track of the desired delay. The amount by which the delay is increased is dependent on the count output from the counter. When the count is below a certain threshold value, a large increment is used. This is equivalent to a proportional (the gain control) plus integral (the delay counter) control method. Once the count is past the lower threshold, the gain is decreased until the count passes an upper threshold value, above which the system is determined to be locked. The delay increment was made large enough so that phase capture occurs over few enough periods so as to be discernible. This approach is sensitive to the value of the upper threshold. If it is chosen too low,

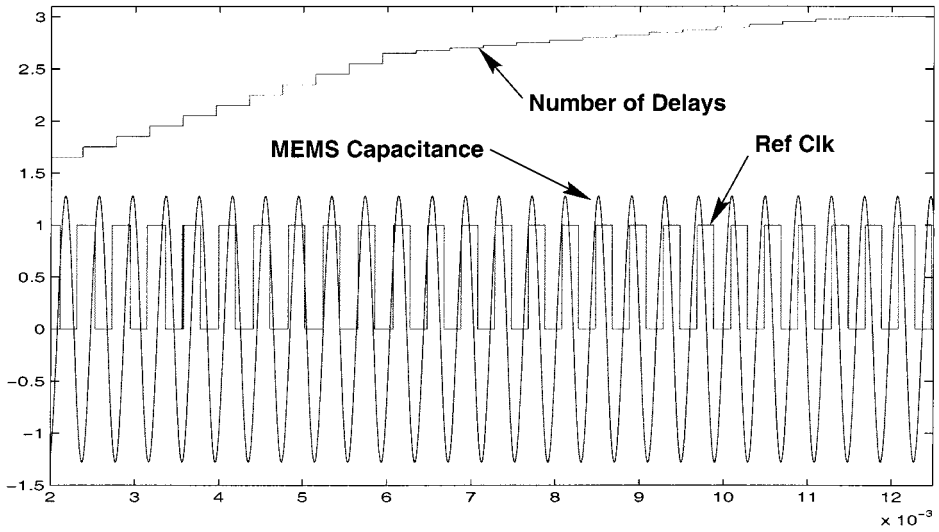

Fig. 18. Locking based on a count threshold.

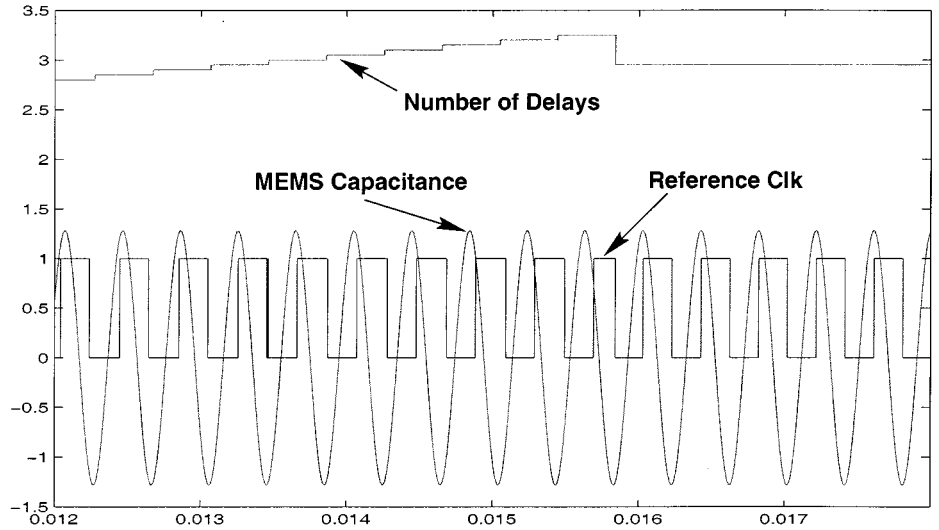

Fig. 19. Locking based on a examining a full period.

the system will have to relock sooner for a given phase drift, because it will be just on the edge of acceptable energy conversion. If the upper threshold is set too high, the system will never lock and the delay line length will saturate.

Another approach is to measure the values of energy converted at each possible delay and, after a period is over, choose the value of delay corresponding to the maximum energy converted. This is shown in Fig. 19. The step down in the delay value trace denotes that the controller has sensed that a complete period has been sampled, so it switches to the stored value of delay matching to the maximum energy converted. Once again, the delay step size has been exaggerated to make the plot more readable. This approach has several advantages. It is not dependent on *a priori* knowledge of the count that will be produced under optimal lock, in order to obtain optimal lock, as the previous approach is. Also, because the entire period of the reference clock is sampled over, some distortion in the capacitor plate motion can be filtered out. This is true because the controller looks for a *global* maximum over a period and so will filter out local maxima as the period is sampled. Of course, the degree to which the distortion filtering is effective (and therefore the amount of distortion allowed) is dependent on the resolution of the sampling process, which is determined by the delay line length and single delay duration.

The best solution is to use a combination of the two approaches. In order to allow for distortion in the plate motion and to attain optimal phase lock, the entire reference period is sampled over. In order to decrease the number of cycles to accomplish this, a lower threshold of count is set. When the feedback counter output is below this value, the delay increment is made large. In this way, regions of low output energy may be rapidly stepped through, reducing lock time and saving power. Finally, after the system has captured phase lock, the output energy is subsampled at a lower frequency and compared to a lower bound of acceptable feedback count. The value of the lower bound is based on the stored value of maximum count when phase lock was previously achieved. If it is above this minimum upper bound, the system is allowed to

continue at the set delay. If the value is below this threshold, the system undergoes the phase lock process again. In this way, phase drift and frequency differences between the reference clock and the mechanical vibration can be compensated for.

Hspice simulations of worst case operation of the delay line (all nodes transitioning in steady state), and block level simulations of the control logic necessary to implement the feedback algorithm suggest that closed loop control could be performed at a worst case power cost of approximately 2–3 μW. Given the performance of the fabricated controller, this would leave 5.6 μW available for the load. Despite the need to generate long delay times of hundreds of microseconds, this ultralow overhead power cost is achieved through the extensive use of digital calibration and all digital control techniques.

VIII. Conclusion

A system has been presented to convert ambient mechanical vibration into electric energy. The conversion process has been modified through the use of $C_{\rm par}$ to provide for maximal energy transfer. Several controller IC optimizations for low power, including power switch sizing and $C_{\rm par}$ capacitance, have been performed. The controller has been verified to operate correctly and its losses have been measured. Based on predicted values of capacitance from the MEMS transducer, 8.6 μW of power is expected to be available for use by a load, resulting in a self-powered electronic system. An architecture for closing a loop around the system by means of energy feedback which offers more robust operation has been proposed. Under this new control scheme, it is estimated that the same system would produce approximately 5.6 μW of useable power. The maximum energy producible can easily be increased by moving to processes designed for higher voltage operation.

References

[1] R. Amirtharajah and A. P. Chandrakasan, "Self-powered signal processing using vibration-based power generation," *IEEE J. Solid-State Circuits*, vol. 33, May 1998.

[2] K. Bult *et al.*, "Low power systems for wireless microsensors," in *Proc. IEEE/ACM Int. Symp. Low-Power Electronic Design*, Aug. 1996.

[3] G. Asada, M. Dong, T. S. Lin, F. Newberg, G. Pottie, W. J. Kaiser, and H. O. Marcy, "Wireless integrated network sensors: Low power systems on a chip," *IEEE ESSIRC*, 1998.

[4] S. M. Wu, J. R. Yang, and T. Y. Liu, "An ASIC transponder for radio frequency identification system," in *Proc. 9th Annual IEEE Int. ASIC Conf. Exhibit*, 1996.

[5] A. P. Chandrakasan, R. Amirtharajah, J. Goodman, and W. Rabiner, "Trends in low power digital signal processing," in *1998 IEEE Int. Symp. Circuits Syst.*, vol. 4, 1998.

[6] M. J. Konak, I. G. Powlesland, S. P. van der Velden, and S. C. Galea, "A self-powered discrete time piezoelectric vibration damper," in *Proc. SPIE—Int. Soc. Optical Eng.*, vol. 3241, 1997.

[7] C. B. Williams and R. B. Yates, "Ananlysis of a micro-electric generator for microsystems," *Transducers'95/Eurosensors IX*, 1995.

[8] H. H. Woodson and J. R. Melcher, *Electromechanical Dynamics*. New York: Wiley, 1968, vol. 1.

[9] A. A. Ayon, C. C. Lin, R. A. Braff, M. A. Schmidt, and H. H. Sawin, "Etching characteristics and profile control of a time multiplexed inductively-coupled plasma etching system," in *Proc. Solid-State Sensor Actuator Workshop*, 1998.

[10] A. Dancy, "Power supplies for ultra low-power applications," Masters thesis, Massachusetts Inst. Technol., 1996.

[11] S. Meninger, "A low power controller for a MEMS based energy converter," Masters dissertation, Massachusetts Inst. Technol., 1999.

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