High-Efficiency Multiple-Output DC–DC Conversion for Low-Voltage Systems

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***Abstract*—This versatile power converter controller provides dual outputs at a fixed switching frequency and can regulate either output voltage or target system delay (using an external L–C filter). In the voltage regulation mode, the output voltage is monitored with an analog–digital (A/D) converter, and the feedback compensation network is implemented digitally. The generation of the pulsewidth modulation (PWM) signal is done with a hybrid delay line/counter approach, which saves power and area relative to previous implementations. Power devices are included on chip to create the two independently regulated output PWM signals. The key features of this design are its low-power dissipation, reconfigurability, use of either delay or voltage feedback, and multiple outputs.**

***Index Terms*—Dc/dc conversion, low power.**

I. Introduction

In PORTABLE systems, electronic circuits can be designed to operate over the range of the voltages supplied by the battery over its discharge cycle. However, adding some form of power regulation can significantly increase battery life, since it allows circuitry to operate at the "optimal" supply voltage from a power perspective. Given the advances in power management techniques (e.g., low-voltage operation [1]), there is a need for efficient dc–dc converters at output power and voltage levels previously uncommon for such circuits. A high-efficiency low-voltage dc–dc converter has been reported that delivers 750 mW [2], and several commercial controllers are currently available for the 100-mW to 1-W range. However, the challenge is to deliver high efficiencies at low currents since in these regimes the control overhead power becomes a significant relative to the delivered power. The chief contribution of this work is to demonstrate control techniques which can deliver low currents to the load efficiently for use in low-power applications. This paper describes techniques for high-efficiency low-voltage regulation for power levels down to tens of milliwatts.

Many portable systems such as cellular phones and PDA's work in an event-driven fashion and have a low duty cycle. In such systems, only a small section of the chip will be turned on during the standby mode and the power dissipation of this circuitry can have a significant impact on the battery life of the system. In order to maintain efficient operation at very low output powers, the power dissipation of the control circuitry, as well as that of the power conversion circuit must be minimized. The converter must be designed to operate efficiently over wide variations in output load power. Low-power systems are being designed with multiple power supply voltages [3]–[6]. The basic approach to reduce power dissipation is to use reduced power supply voltages for modules not in the critical path of the computation. This technique requires the generation of multiple power supply voltages efficiently. A brute force approach is to use separate controllers for each output. In this paper, we describe techniques to reuse portions of the controller for multiple outputs. As an example, a dual-output supply is demonstrated. Finally, there are many systems where the amount of processing per input sample (i.e., the computational workload) varies with time [7]–[10]. For such systems, one approach to save power is to dynamically vary the power supply voltage as the load varies. From a power supply perspective, this translates to a need to design the regulator control for a quick transient response. Even if the workload does not vary, the power supply should be dynamically adjusted to compensate for temperature and process variations [11].

This paper describes techniques for efficient dc–dc converter design for low-power supply voltage digital systems. Section II describes the overall architecture of the multiple-output converter. Section III outlines some of the issues in feedback control for these converters and describes the motivation for moving from a previous one bit feedback scheme to the scheme shown in Fig. 1. Section IV discusses several techiques for pulsewidth modulation (PWM) that can be used in these converters. The implementation and test results are shown in Section V. Conclusions from this research are drawn in Section VI.

II. Dual-Output DC–DC Converter Architecture

Fig. 1 shows a block diagram of the dual-output dc–dc converter. The converter operates by creating a PWM signal of some duty cycle at node V_A (and similarly at node V_B), whose average value is the desired output voltage. External passive filtering is used to filter the PWM signal, creating a dc voltage with some tolerable value of ripple.

In order to provide reasonable efficiencies for the low-supply voltages present in low-power digital systems, power converters must incorporate synchronous rectification (i.e., active power devices are used to replace diodes) [2]. A drawback of synchronous rectification is that without explicit monitoring of the output current and control of the synchronous rectifier,

Manuscript received July 28, 1999; revised September 21, 1999. This work was supported by DARPA Contract DAAL-01-95-K3526 and the U.S. Army Research Laboratory Advanced Sensors Consortium under Cooperative Agreement DAAL-01-96-2-0001. A. Dancy was supported by an NSF Graduate Research Fellowship.

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Publisher Item Identifier S 1063-8210(00)04351-1.

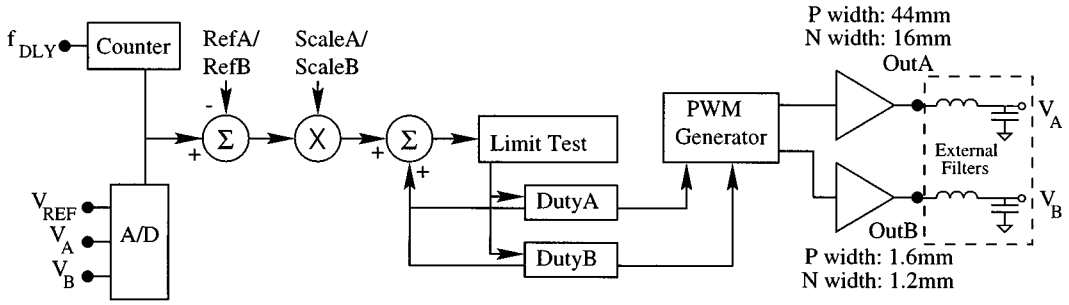

Fig. 1. Block diagram of the dual-output dc–dc converter.

the circuit will not enter discontinuous mode at light loads. The resulting ripple current in the inductor will cause resistive losses that will reduce efficiency at light loads.

This converter has the ability to regulate either an output voltage or target system delay. That is, the input feedback signal is taken either from the analog–digital (A/D) converter or the delay feedback input. The delay feedback input allows the controller to measure the speed of operation of a load circuit. The input is a signal from a ring oscillator formed from the critical path of the circuit to be controlled. This enables the operation of the controller in a variable supply voltage system, where the supply voltage is minimized dynamically over variations in process, temperature, and workload [7], [12].

The compensation network for the output of the power converter is a variable gain integral controller. A reference value (in a digital form) is subtracted from the A/D or delay measurement, and the difference is scaled in an array multiplier stage. The product is then subtracted from the previous duty cycle command to produce the next duty cycle command. The internal representation of the duty cycle is 12 b, and the ten MSB's are passed to the PWM stage to create the output. The compensation sample rate is programmable; the sample rate is primarily limited by the A/D conversion time. The compensation network elements (adders and multiplier) are time multiplexed to derive duty cycle commands for both of the outputs. This multiplexing allows the control overhead to be amortized over both dc–dc converter outputs. The reference value and gain for each of the two outputs and other configuration registers are fully programmable through a bidirectional two-wire serial interface.

The first of the two outputs is optimized for a 20-mA 2-V load, and the second is optimized for a 1-mA 1-V load. Guard rings help to isolate the power output stages from the core digital logic. Additional guard rings separate the A/D capacitor array and low-current bias reference from the power stages and digital core.

The switching frequency of the converter, the physical size of the output filter, and the efficiency of the converter are inextricably linked. The volume of the output filter is roughly proportional to the energy which it must store over a single cycle, which in turn is proportional to the power being processed times the period of a single cycle. Thus the volume is inversely proportional to the switching frequency. The relationship between the cutoff frequency of the output filter and the switching frequency determines the size of the ripple on the output voltage. The power dissipation in a switching converter will always increase with increasing switching frequency. Choosing the switching frequency requires making tradeoffs between efficiency, power density, and transient performance. Low frequencies yield larger filters, higher efficiency, and low-output voltage ripple, while higher operating frequencies allow the use of smaller filters at the expense of a lower efficiency and increased ripple. In the case of portable electronic applications, filter volume and cost are at a premium and thus drive the design toward higher switching frequencies and less efficient operation. Therefore, this technology driver makes reducing the control power consumption even more important. A small area inductor is chosen for this application and its implications for efficiency are described below.

III. Control Strategies for Low-Power Converters

A. Current Techniques

The most common power converter controller consists of an amplifier which creates a voltage proportional to the desired duty cycle, by comparing the output voltage to a reference, and perhaps adding some dynamics such as an integrator. Some problems with this technique for low-power integrated applications are sensitivity to noise (when integrated with a digital load circuit), difficulty interfacing to a digital frequency feedback signal (for variable voltage operation), and challenges achieving low-power (microwatt level) operation.

Another control technique employed in low-power dc–dc converters is pulse frequency modulation (PFM) [13]. With PFM, pulses of current are output to the load filter, and voltage regulation is achieved by varying the time delay between pulses (the power circuit is always operating in discontinuous mode). The control can be implemented without a feedback amplifier, by simply comparing the output voltage to a reference, and initiating current pulses when the output voltage is low. A slight variant of this method is a burst-mode controller (e.g., [14]), where a fixed frequency train of current pulses is applied when the output voltage is below the reference. Drawbacks of PFM operation (as described) are the use of discontinuous mode at all loads and variable frequency switching. These characteristics increase the radiated output noise (EMI), and using discontinuous operation for all loads requires oversizing the output filter inductor to accommodate the inherently large peak inductor current.

A fully digital controller can also be used to control a dc–dc power converter. A digital proportional integral derivative (PID)

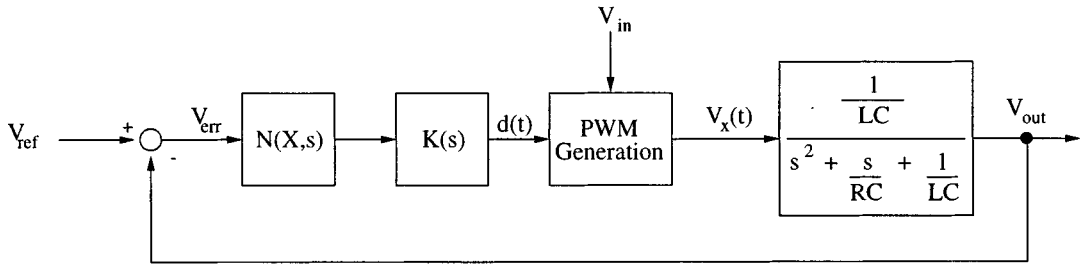

Fig. 2. Block diagram of buck converter system.

controller has been presented [12], which is suited for situations where the feedback signal is available in digital form. This type of controller has the potential to have very low power consumption, and its digital nature makes it a good choice to be integrated with other systems.

B. Low-Resolution Digital Feedback

In order to achieve the low-power operation of the commercial PFM controllers, while retaining fixed frequency continuous mode operation, a very simple A/D conversion with some digital processing can accomplish the voltage feedback function. This entails far less power dissipation than that required by even the simplest analog feedback circuits, due to the static current draw of the analog circuits. Minimally, the A/D conversion can be accomplished by a comparator, which decides whether the sensed output voltage is above or below a reference voltage. If the comparator is implemented as a dynamic comparator, which evaluates only upon command, it will not dissipate any power outside of the brief evaluation period. In this single bit feedback case, a digital word representing the duty cycle is created by a counter which counts up when the output is lower than the reference and counts down when the output is higher than the reference. This digital counter accomplishes the functionality of an integrator.

Fig. 2 is a block diagram of the buck converter under feedback control. The transfer function of the output low-pass filter is a typical second-order system. The square wave signal $V_x(t)$ that is filtered is generated by the PWM generation block. This block takes a commanded duty cycle $d(t)$ which in steady state should be the ratio between the unregulated input voltage V_{in} and the desired output voltage V_{ref}. The compensation network consists of a linear block $K(s)$ and a nonlinear block $N(X, s)$.

Consider the fully linear system $(N(X, s) = 1)$. To eliminate steady-state error, we will use an integral compensator with gain K

$$K(s) = \frac{K}{s}. \tag{1}$$

This leads to the following open-loop transfer function:

$$L(s) = \frac{\frac{K}{LC}}{s\left(s^2 + \frac{s}{RC} + \frac{1}{LC}\right)}. \tag{2}$$

Equation (2) indicates that there are three poles, one at the origin and two more in the left-half plane, so the system is open loop stable. Fig. 3 shows the root locus as the feedback gain

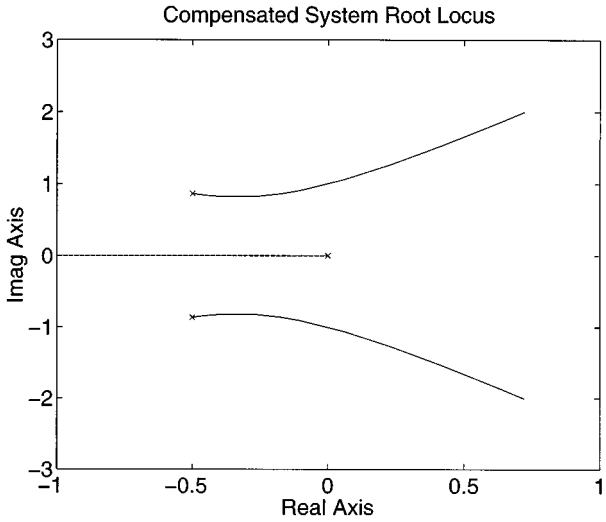

Fig. 3. Integrator compensation system root locus.

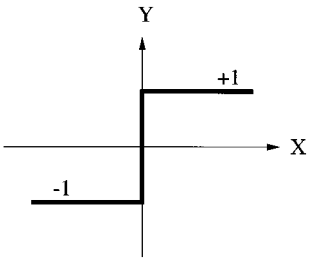

Fig. 4. One bit error constitutive relation.

K is varied. As K increases, two of the poles move toward the $j\omega$-axis and the system responds more quickly to step changes at the input at the expense of greater ringing. For some value of K, the poles move into the right-half plane and the system is unstable. To compensate the system, simply choose a gain that achieves the desired transient performance, making sure that it is not so large that it destabilizes the converter.

A single bit feedback scheme can be implemented by using a comparator to sample the error V_{err}. The comparator then outputs a $+1$ if V_{err} is positive and a -1 if it is negative. Fig. 4 shows the nonlinear constitutive relation of the comparator. To analyze the feedback system with this nonlinearity, we apply the theory of describing functions to determine the transfer function $N(X, j\omega)$ [15]

$$N(X, j\omega) = \frac{4}{\pi X} \tag{3}$$

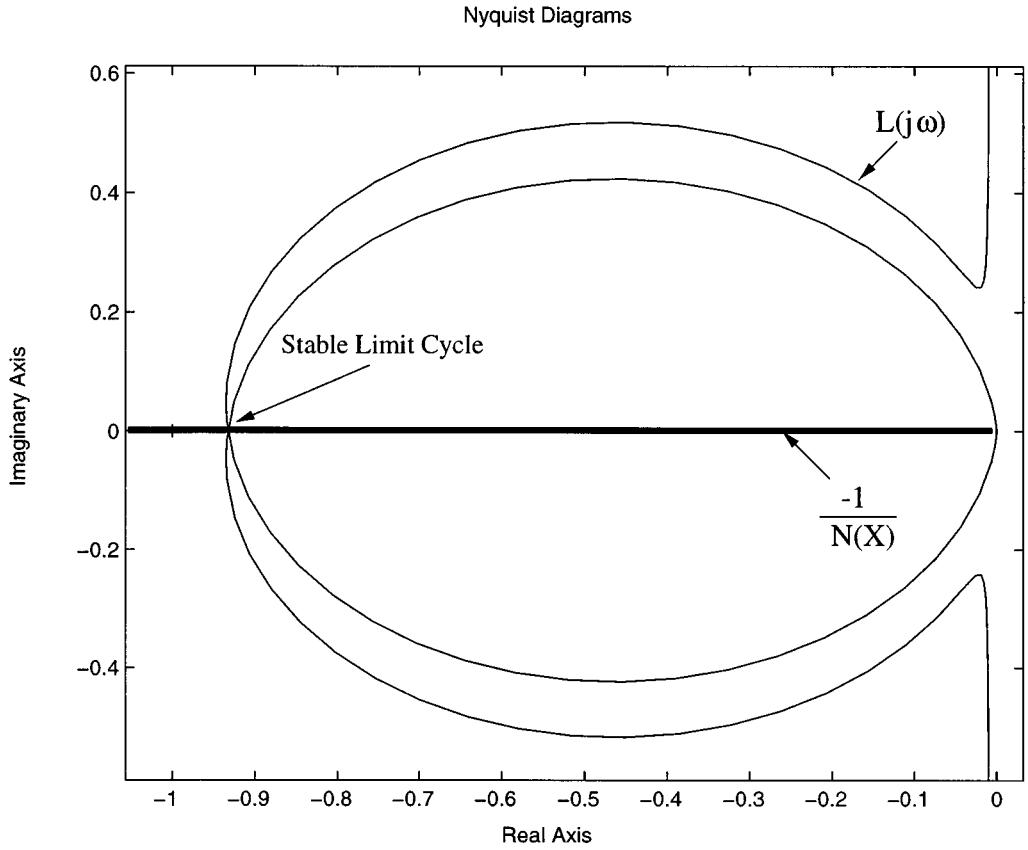

Fig. 5. Nyquist plot with describing function for 1-b error feedback.

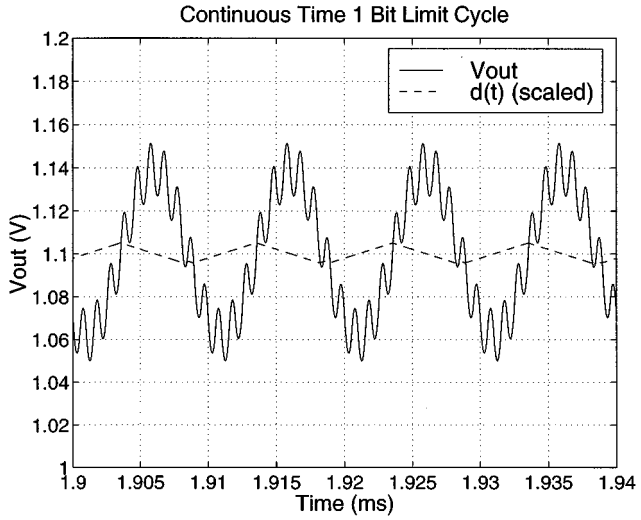

Fig. 6. CT limit cycle for 1-b feedback.

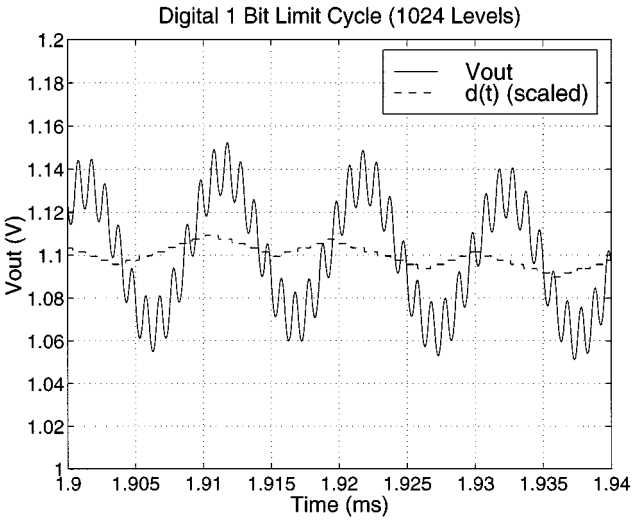

Fig. 7. Digital limit cycle for 1-b feedback (10-b quantization).

where $X \geq 0$ is the amplitude of the exciting sinusoidal function. Note that this describing function does not depend on frequency, which simplifies its use in stability analysis. It also has zero phase, so we can think of it as a variable gain in our open-loop transfer function. Fig. 8 shows the transient response of an earlier power supply that used single bit feedback control [16]. The output limit cycle can clearly be seen. Also, the response is slew limited to about 10 ms by the clock rate. Though slow, the response is certainly not unstable.

The locus of points traced out for different values of X is shown in Fig. 5, along with the Nyquist plot of the linear transfer function of the integral compensated system [$L(j\omega)$ from (2)]. This locus is simply the negative real axis. To analyze the stability, consider what happens to a small oscillation at the input of the closed-loop system. For X small, $-1/N$ is also small, and our operating point is inside the encirclements of $L(j\omega)$. This means that the operating point is unstable and small amplitude oscillations will grow, moving the operating point to the left

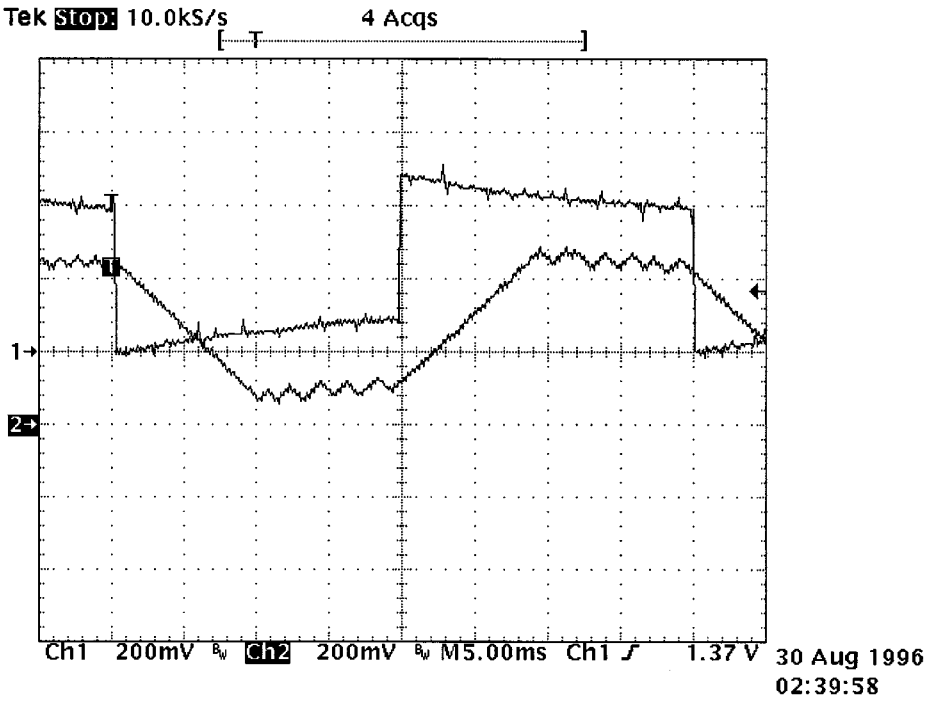

Fig. 8. Transient response of closed-loop power supply using single bit feedback. Upper trace is the reference voltage and the lower trace is the power supply output. Traces have been separated vertically by 200 mV as a visual aid. Arrow markers on left side correspond to a voltage of 1.2 V.

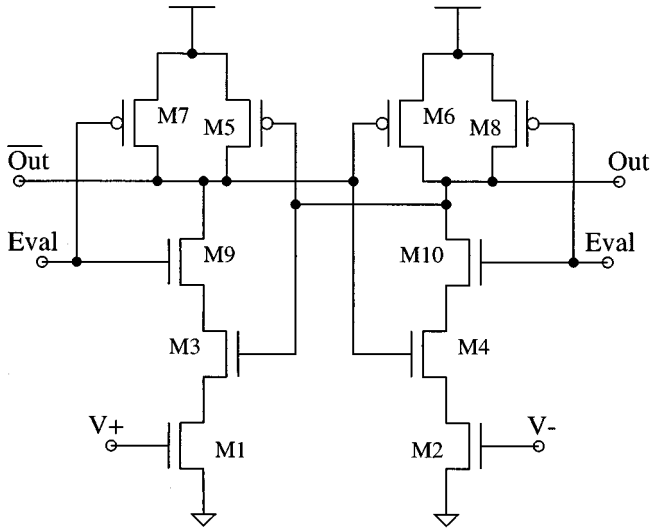

Fig. 9. A CMOS dynamic comparator. $V+$ and $V-$ are the inputs, Out and $\overline{Out}$ are the outputs. Outputs are valid some time after *Eval* has gone high.

along the $-1/N$ curve. If X is large, we start outside the encirclements and the operating point is stable, meaning the amplitude of the oscillation decreases with time. This in turn moves us to the right on the $-1/N$ curve. The intersection of $L(j\omega)$ and $-1/N$ is therefore a stable operating point, and we expect the closed-loop system to have a limit cycle (steady-state oscillation). The frequency of the oscillation is the frequency ω_0 at which $\angle L(j\omega) = 180°$. Its amplitude is obtained by setting $-1/N = L(j\omega)$ and solving for X. For our system

$$X = \frac{-4L(j\omega_0)}{\pi} = \frac{4KRC}{\pi}. \tag{4}$$

To verify this continuous time analysis, the buck converter system was simulated using MATLAB. The resonant frequency of the converter was chosen to be 100 kHz and the load resistance $R = 10\ \Omega$. The compensator gain $K = 1000$ and the switching frequency of the PWM generation was 1 MHz. From these numbers, we expect the limit cycle frequency to be 100 kHz and the amplitude $X = 20.3$ mV. Fig. 6 shows the V_{out} limit cycle caused by having one bit error feedback and confirms the theoretically predicted frequency and amplitude. $V_{\text{ref}} = 1.1$ V for this simulation. Sumperimposed on the plot is the commanded output voltage $d(t)V_{\text{in}}$ which can be seen as a triangle wave. Since the cutoff frequency of the output filter is only a decade above the switching frequency of the PWM generation, there is substantial 1-MHz ripple on the output.

Implementing the control using a digital system requires quantizing the duty cycle command $d(t)$ and discretizing the time axis. A typical implementation is to use an up/down counter as the integrator and a comparator to generate the 1-b error signal. One can think of the "gain" of such a system as

$$K_{DT} = \frac{\Delta d}{T_{\text{cnt}}} \tag{5}$$

where Δd is the duty cycle resolution of the PWM generation and T_{cnt} is the period of the counter clock. Since the input to the counter tells it to add or subtract one from its state every cycle and a one corresponds to a minimum change in the duty cycle, this equation is intuitively clear. For example, if the error is one for T s, the counter output value should be T/T_{cnt}.

Equation (5) therefore yields a notion of how to understand the performance of the digital control system. For a given duty cycle quantization interval Δd, increasing the clock frequency results in a higher digital "gain" and can destabilize the system

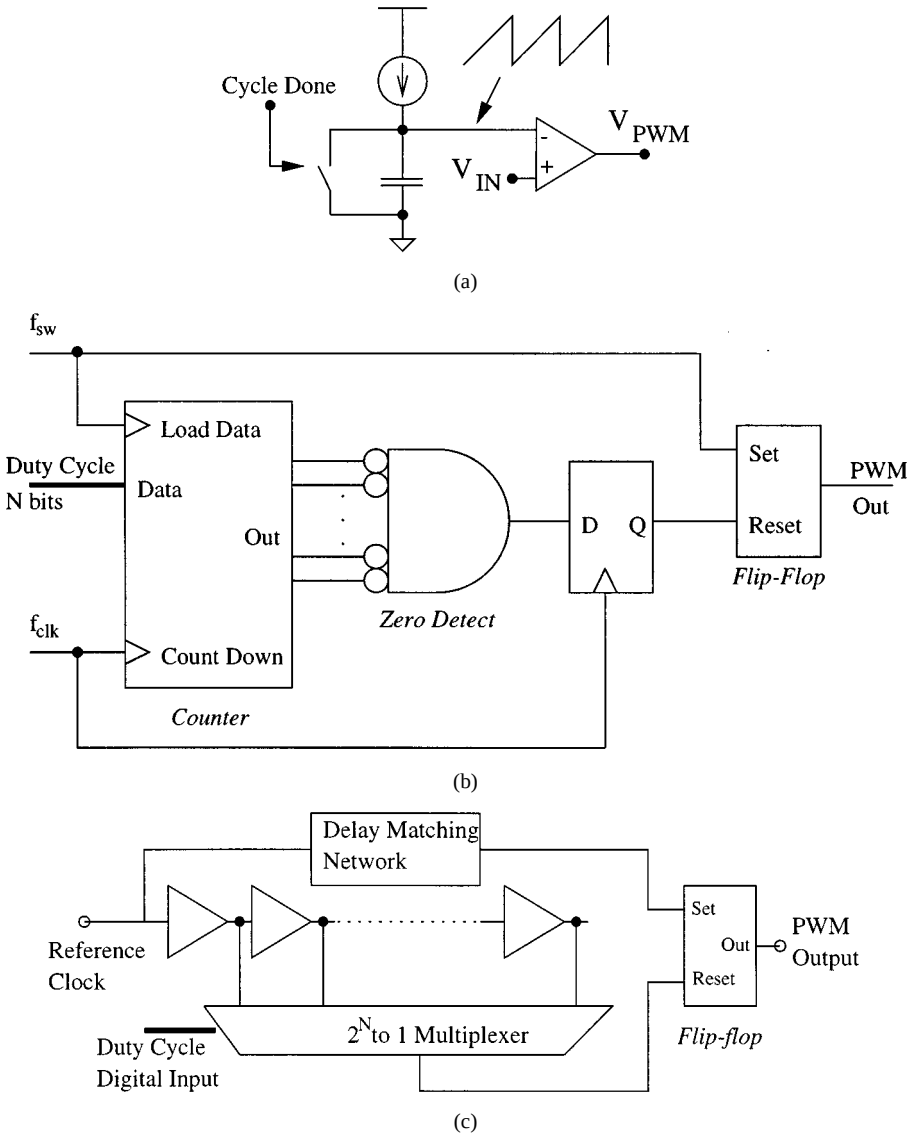

Fig. 10. Analog and digital PWM signal generation techniques. In (a), $V_{\rm IN}$ is the analog duty cycle command, and *Cycle Done* is a narrow-pulse clock signal.

as the root locus diagram showed. Equation (5) can also be used as a design tool. If we have a continuous time compensator gain K that produces a desired performance, we can simply solve for the ratio of Δd and $T_{\rm cnt}$ using five. Δd is usually a more constrained design variable than the counter clock rate, so this should be chosen first. This does not guarantee that the performance of the digital system approximates the continuous time one, but decreasing Δd and choosing the appropriate $T_{\rm cnt}$ will eventually satisfy the preformance requirements. This must be verified using simulation.

Fig. 7 shows a simulation of the steady-state limit cycle of the digital controller using 1-b error feedback for a 10-b quantization of the duty cycle. The sample rate $T_{\rm cnt}$ was set such that the digital gain was equal to the analog gain of Fig. 6. The performance is similar to the analog compensator although the effect of the quantization can be seen in the commanded output voltage signal (dashed line). There is also a lower frequency small amplitude oscillation superimposed on the output. As the quantization is increased to 12 b, the digital controller becomes almost indistinguishable from the analog implementation.

C. High-Resolution Digital Feedback

A previous chip which used low-resolution feedback techniques is described in [17]. However, the transient performance of that converter was limited by the slew rate of the counter, i.e., for the given duty cycle quantization Δd of the previous chip, it was impossible to choose $T_{\rm cnt}$ small enough to give fast transient performance without destabilizing the feedback loop. As more bits of resolution are added to the error sample, the digital system starts to approach a linear analog controller. Describing function analysis is unecessary once the resolution is high enough. For power converters where the overhead of good A/D resolution and wide digital data is insignificant, the high-resolution approach is best since there are no steady-state limit cycles or steady-state errors. That is the approach taken in the current work.

The A/D converter is a 7-b standard charge redistribution converter. The resolution is based on quantizing the input voltage range (3 V for the assumed lithium battery power source) to the 25-mV level. The advantage of a charge redistribution converter for low-power applications is that it can be implemented without

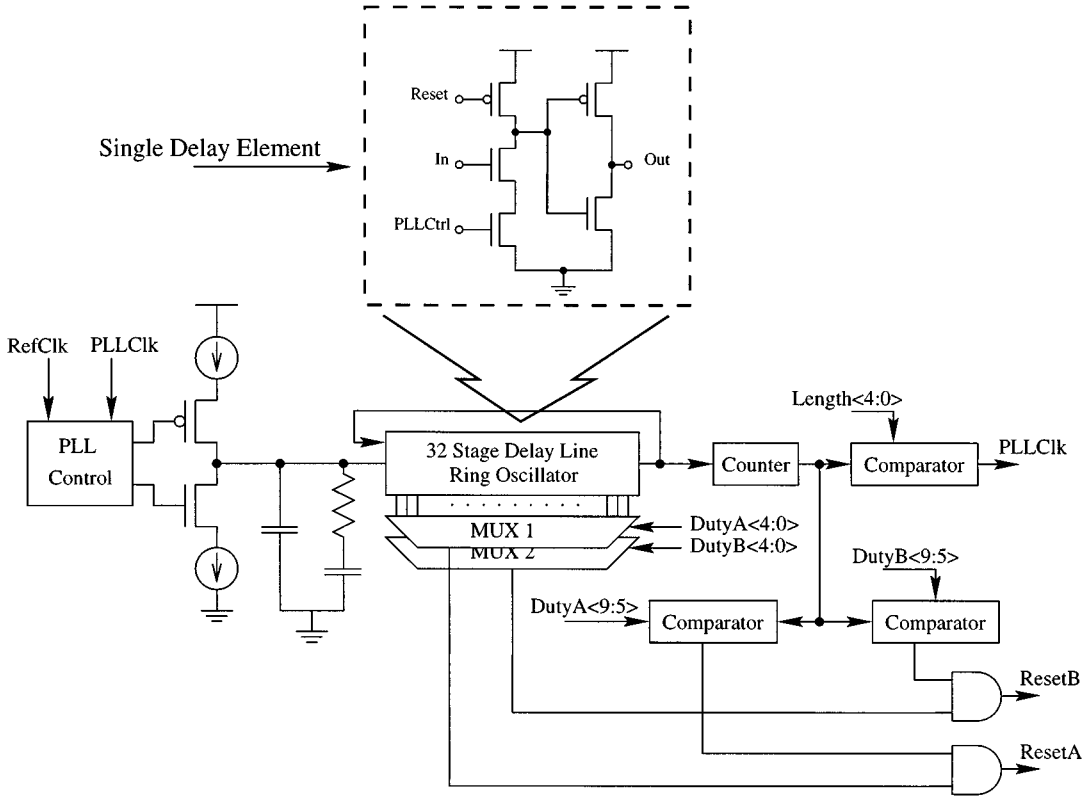

Fig. 11. PWM generation block, showing PLL charge pump and dual-output hybrid delay line/counter PWM approach.

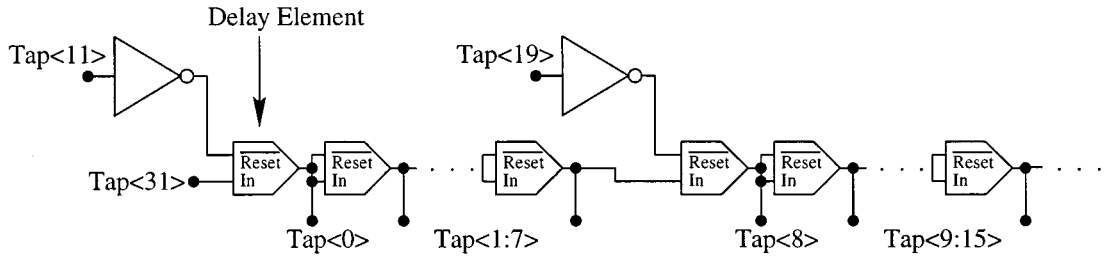

Fig. 12. Postcharge logic in delay line matches leading edge and falling edge propagation times and allows a ring oscillator to be created with an even number of stages.

amplifiers, which would typically cause significant static currents to be dissipated. A dynamic comparator was utilized to compare the capacitor array voltage to an external analog reference at each stage of the conversion. The capacitor array utilizes common centroid layout, and there are two rows and columns of dummy devices on the perimeter of the array to enhance matching. Due to the relatively low resolution of the converter, unit capacitor sizing was rather aggressive; a 10 μm $\times$ 10-μm poly–poly capacitor giving 47 fF of capacitance. A schematic of the dynamic comparator used is shown in Fig. 9. This design is relatively common [18]. In this comparator, the offset voltage is a function of the parameter matching (dimensions and thresholds) between the pairs of devices M1, M2; M3, M4; and M5, M6. When a comparison is initiated by a rising Eval signal, M1 and M2 begin discharging the nodes Out and $\overline{Out}$. The cross-coupled feedback causes whichever node is falling more slowly to become latched high.

IV. Pulsewidth Modulation

A. PWM Generation Alternatives

After a digital word representing the desired duty cycle has been created, the actual switching waveform must be generated. When using analog circuits, a PWM signal is typically created by comparing a ramp signal to a reference value with a static comparator as shown in Fig. 10(a). This requires dc current flow to generate the voltage ramp. Digital PWM circuits can avoid the problem of static power dissipation.

In digital systems, PWM signals are typically created by using a clock at some multiple of the switching frequency with a counter. The PWM signal is set high at the beginning of a switching period and then reset after the counter detects that some number of cycles of the faster clock have passed. Fig. 10(b) shows a block diagram of the counter-based PWM approach. Unfortunately, ultrafast-clocked counters are not

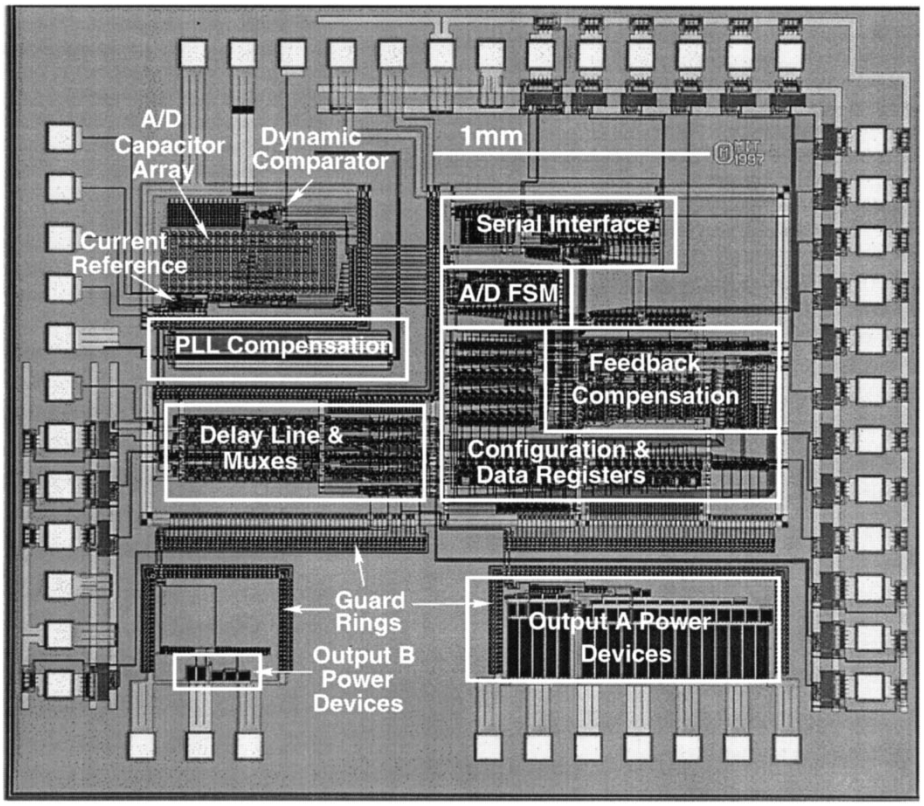

Fig. 13. Die photo of dual-output dc–dc converter.

particularly well suited for low-power operation. The counter clock frequency is chosen to be 2^N times the switching frequency of the converter, where N is the number of bits in the digital command word. The clock is used to divide the switching period into 2^N increments. For example, a 1-MHz switching waveform with 256 discrete levels of duty cycle requires a 256-MHz clock! As a result of the short delay requirement, such a circuit does not lend itself to voltage scaling. A digital controller has been reported that uses the counter-based approach, but the power of the controller alone is on the order of 30 mW [12]. This is acceptable for dc–dc converters that deliver power in the watt range, but not for systems in the milliwatt range.

Another way to create a PWM signal from an N-bit digital value is to use a tapped delay line [17]. Since this approach uses the switching frequency clock, the power is significantly reduced relative to the fast-clocked counter approach. Fig. 10(c) shows a schematic for the delay line-based digital word-to-PWM circuit. The essential components of a tapped delay line PWM circuit are the delay line and a multiplexer. A pulse from a reference clock starts a cycle, and sets the PWM output to go high (after a delay designed to match the propagation delay experienced through the multiplexer). The reference pulse propagates down the delay line, and when it reaches the output selected by the multiplexer, it is used to set the PWM output low. The total delay of the delay line is adjusted so that the total delay is equal to the reference clock period. That is, feedback is used to turn the delay line into a delay-locked loop (DLL), which locks to the period of the input clock. This approach is very power efficient, however, can require significant implementation area. If multiple PWM signals are needed, it requires the addition of multiplexers to a single delay line.

TABLE I
DC–DC CONVERTER CHIP SUMMARY

A/D INL	± 0.5 LSB
A/D DNL	$+0.3, -0.4$ LSB
Inductor Value	440μH
Capacitor Value	0.22μF
Filter Area	0.024in^2
Output Ripple ($f_{switch} \geq 500kHz$)	$40mV$
Operating Frequency	< 2.5MHz

B. Hybrid PWM Generation Architecture

A hybrid scheme (Fig. 11) is described here that provides considerable advantages over both the fast-clocked counter and delay line approaches. A 32-stage delay line forms the basis for the PWM stage. The delay line is configured as a ring oscillator, which is phase locked to a reference clock. A divider allows the ring oscillator frequency to be set between 2–32 times faster than the reference frequency. The taps of the delay line then divide the input clock period into between 64 to 1024 equal increments. The taps of the delay line are sensed by two 32-to-1 multiplexers, one for each of the output PWM signals. The rising edge of the reference clock sets the PWM signals high. A PWM signal is set low when a pulse arrives at the tap of the delay line selected by its multiplexer for the Nth time, where N represents the five MSB's of the 10-b duty cycle command.

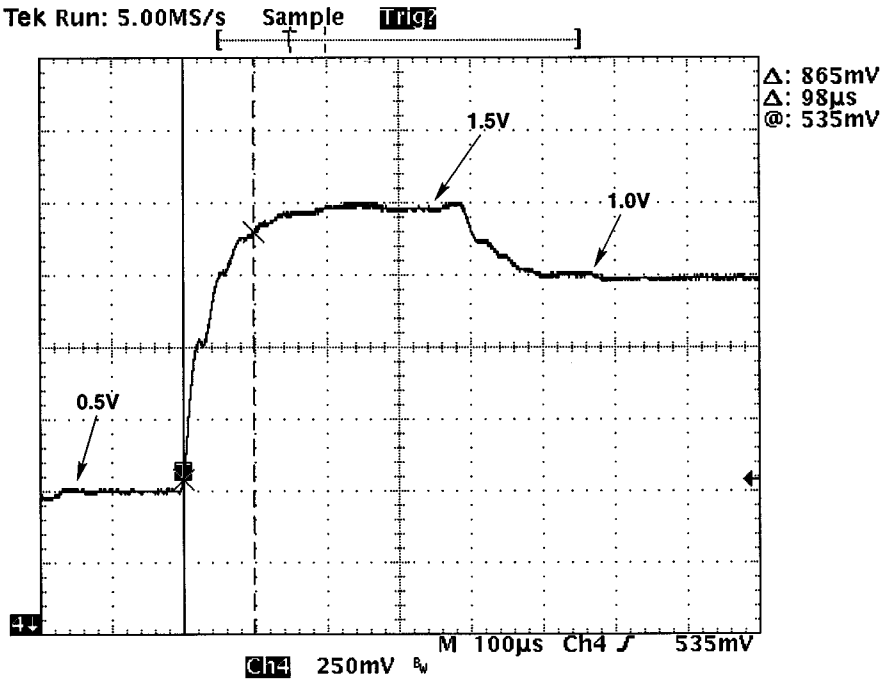

Fig. 14. Transient response of filtered output voltage to changing digital reference commands ($f_{sw} = 1$ MHz).

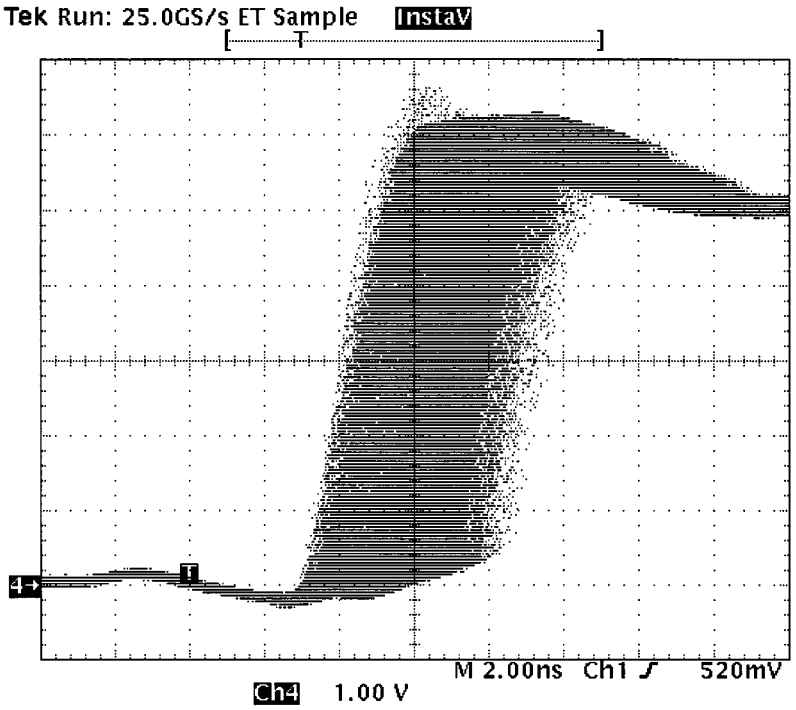

Fig. 15. PLL jitter at last tap of delay line.

The delay of the delay line is controlled by adjusting the gate signals on starvation-type NMOS devices. The gate control signal controls the speed of the positive going edge at the output of each buffer. Fig. 12 shows how postcharge logic is used to ensure that the negative edge of the outputs travel at the same speed as the positive edge [19]. Each delay element consists of a starved inverter inverter followed by a regular CMOS inverter. If the input node were connected to both the PMOS and the starved NMOS, the falling transition would be much slower than the rising transition. This would lead to a mismatch in propagation delays for the rising and falling edges through each delay stage. By making the circuit dynamic and using the later delay stages to time the precharge for the preceding stages, the falling edge propagation delay through the entire delay line

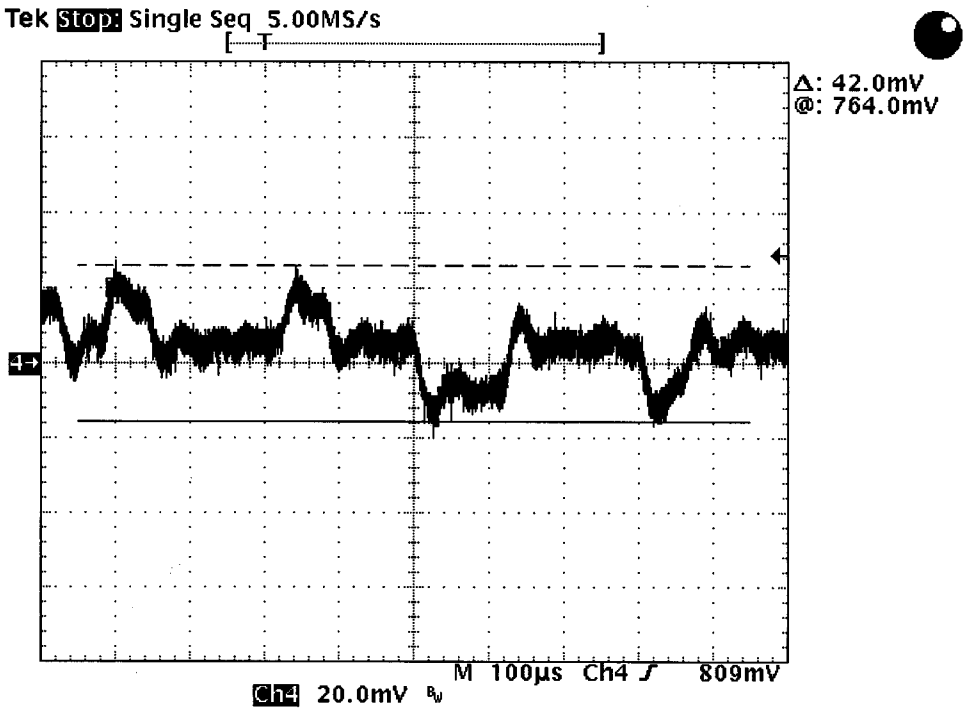

Fig. 16. Regulated output voltage and ripple.

is dependent on the delay of the rising edge and the delays are made more equal. In addition, putting the inversion in parallel with the delay line enables the ring oscillator to have an even number of stages. The starvation control node is charged up and down using a current source. The biasing for the current source is generated on chip with a MOS Widlar current source. The compensation network for the PLL control node is implemented on chip with poly–poly capacitors and a poly-2 resistor.

The hybrid delay line/counter circuit reduces power dissipation relative to the fast-counter approach, by a 32X reduction in counter clock frequency (in this implementation). Compared to the delay line-based PWM circuit, the hybrid approach gives a nine times reduction in area; when leveraged to provide multiple outputs as done here, the effective area reduction is a factor of 12.

V. Implementation and Results

Fig. 13 shows a die photo of the dual-output dc–dc converter. The A/D, control circuitry, and power switches are integrated on the same die. The power switches are sized to trade off the switching and conduction losses. Table I gives the details of the power converter chip including the chosen filter values.

Fig. 14 shows the transient response of the output voltage to step changes in commanded output. The switching frequency is 1 MHz, and the feedback sampling period is 25 μs. The output settles to 90% of the desired value in 100 μs. The switching speed is limited by the conversion time of the A/D converter (since the A/D takes multiple switching periods for data conversion). The ability the supply voltage on demand allows the minimization of energy dissipation in variable load systems. The dc–dc converter, as mentioned earlier, can also be configured in a performance feedback mode. The performance feedback has been tested and is functional. The performance feedback requires the DSP load circuit to provide a clock signal derived from a ring oscillator matched to the critical path circuitry.

TABLE II
Output Efficiency Using a Low-Cost Inductor with a Series Resistance of 9.5 Ω and a Low-Loss Inductor at High-Output Power Levels

Output (f_{sw} = 500kHz)	Efficiency	
	low cost inductor	low loss inductor
Output A		
V_{out} = 2V		
I_{out} = 10mA	89%	89%
I_{out} = 45mA	80%	95%
Output B		
V_{out} = 1V		
I_{out} = 750μA	89%	
I_{out} = 10mA	80%	

The jitter of the PLL is 5.5 ns (Fig. 15). The effect of this jitter on the output voltage is a slight broadening of the spectrum of the switching frequency ripple. Fig. 16 shows the regulated output voltage and the ripple.

Measured output efficiencies were between 89% and 80% over a range of output currents, for the particular output filter selected. There is a tradeoff between the size and cost of the output filter and the achievable efficiency. The filter selected here represents a low-cost small area selection. The losses are dominated by a 9.5-Ω resistance in the output inductor at high-output powers. The first column of Table II shows the output efficiency for this low-cost small-sized inductor. The basic tradeoff in inductor design is between cost and area versus resistive loss. To achieve a particular inductance value, a certain number of turns of wire must be created in the winding. The desire for low area and cost demands that the wires in the winding have a small cross-sectional area and thus a significant resistance as

TABLE III
POWER DISSIPATION FOR 1024 AND 256 LEVELS OF THE PWM

Parameter	Value
# of taps	1024
Switching Frequency	500kHz
Min. Supply Voltage	2.05V
PLL & Logic Current	199.3μA
Analog Circuits Current	1.5μA
# of taps	256
Switching Frequency	500kHz
Min. Supply Voltage	1.35V
PLL & Logic Current	42.8μA
Analog Circuits Current	1.5μA

the number of turns increases. Using a low-loss inductor with low-series resistance for the high-power output A, we were able to achieve a total efficiency of 95% for the 2-V output at a load of 45 mA, as shown in the second column of Table II. At low-output power levels (output B), the losses are not dominated by the inductor so there is no reason to use the less resistive inductor. In comparison to a recently reported embedded converter [20], the implementation described here achieves higher efficiencies at all delivered power levels of interest (e.g., 95% versus around 80% at 90 mW and 80% versus around 40% at 10 mW).

At 500 kHz, with 256 levels of duty cycle resolution, the control circuit draws less than 45 μA. Table III shows the power dissipation for two different configurations of the power converter (with 8- and 10-b resolutions on the PWM). The power overhead of this hybrid controller is much lower than previously reported work [12] using a fast-clocked counter architecture (61 μW versus 32 mW).

VI. CONCLUSION

We have shown that it is possible to achieve stable operation with only a single bit of feedback regarding the output voltage, albeit with degradation of output response time. A circuit was presented which creates a PWM signal from digital inputs at frequencies appropriate for very small low-power voltage converters, with a power dissipation on the order of 100 μW.

A digital PWM power supply converter has been described here that produces dual-output voltages efficiently. This converter can be configured to regulate a fixed supply voltage or a processing speed. The ability to adapt supply voltage quickly can be exploited to minimize power dissipation in applications where the workload varies rapidly. Minimizing the fixed overhead loss of the converter is the key to achieving high efficiency at light load conditions. The power supply converter features a hybrid delay line and counter-based PWM generator that is area and power efficient for generating multiple outputs.

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