Back-Gated CMOS on SOIAS For Dynamic Threshold Voltage Control

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***Abstract*— The simultaneous reduction of power supply and threshold voltages for low-power design without suffering performance losses will eventually reach the limit of diminishing returns as static leakage power dissipation becomes a significant portion of the total power consumption. This is especially acute in systems that are idling most of the time. In order to meet the opposing requirements of high performance at reduced power supply voltage and low-static leakage power during idle periods, a dynamic threshold voltage control scheme is proposed. A novel Silicon-On-Insulator (SOI)-based technology called Silicon-On-Insulator-with-Active-Substrate (SOIAS) was developed whereby a back-gate is used to control the threshold voltage of the front-gate; this concept was demonstrated on a selectively scaled CMOS process implementing discrete devices and ring oscillators. For a 250 mV switch in threshold voltage, a reduction of 3–4 decades in subthreshold leakage current was measured.**

I. The SOIAS Concept

THE CONCEPT of the Silicon-On-Insulator-with-Active-Substrate (SOIAS) technology can be taken to many levels of complexity. The fundamental idea behind this technology is to add one or more conductive under layers beneath the buried oxide of a Silicon-On-Insulator (SOI) structure. Such layers can serve as buried interconnects, gates or both. To take this idea even further, one can imagine stacked SOI structures with embedded interconnects and gates in between them. The fabrication of SOIAS structures leverages off from many of the technologies developed for bulk and SOI CMOS processes (e.g., CMP and wafer bonding). There are several options and various degrees in which the buried layer or layers can be rendered conductive. On one extreme, the buried layer can be a refractory metal such as tungsten, or silicides of such metals which can withstand subsequent high-temperature processing. In this case, the buried conductive layer must be pre-patterned prior to bonding which can make the bonding process more challenging. On the other extreme, a blanket insulating/semi-insulating layer (e.g., intrinsic amorphous/polycrystalline silicon) can be used, and selective areas of the buried layer can be made conductive by ion implantation with dopants. This work focuses on the development of the latter approach with one buried layer of intrinsic polysilicon for the purpose of dynamic threshold voltage control in low-power applications.

Manuscript received June 3, 1996; revised January 6, 1997. The review of this paper was arranged by Editor G. W. Neudeck. This work was supported by the MIT Lincoln Laboratory. The work of I. Yang was supported by AT&T through a graduate fellowship.

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Publisher Item Identifier S 0018-9383(97)03008-6.

II. Dynamic Threshold Voltage Control Concept

Many system computations are either temporally or spatially localized. Systems that are frequently idle, i.e., doing computation only for a small fraction of the time, operate in burst-mode, and hence exhibit temporal locality. On the other side of the spectrum are systems that operate in continuous mode (e.g., active all of the time), and hence do not exhibit temporal locality. At the same time, a system may only have a fraction of its functional modules active all of the time; such systems exhibit spatial locality. This idea can be applied to lower levels of the hierarchy such as at the logic gate level or the transistor level. A global strategy for achieving high performance and low power in continuously computing systems (e.g., modules of a video compression system) has been the simultaneous reduction of supply voltage V_{DD} and threshold voltage V_T where the optimal V_{DD} and V_T are found for minimum total system energy by trading off dynamic energy for static leakage energy [1]–[3]. CMOS-based high-performance burst-mode computation systems (e.g., a microprocessor running an X-server or cellular phone which is idling more than 90% of the time) will suffer high-static leakage energy dissipation operating at low V_{DD} with constant low V_T even with clocks stopped. For example, even when a user is continuously entering data at the keyboard, the X-server is active, (i.e., doing computation), only 2–3% of the time [4]. In order to simultaneously achieve high performance during active periods and low leakage power during idle periods for burst-mode computational systems, several schemes of reducing the leakage current have been proposed. The multiple V_T CMOS design involves using high V_T transistors to gate the low V_T blocks [5], [6]. Both NMOS and PMOS transistors are needed in order to preserve state. These devices must be made large due to the finite resistance of these transistors. This will incur additional switching energy to switch these devices. Therefore, appropriate sizing of the high V_T transistors is crucial. Another approach is the dynamic control of V_T by biasing the bulk-CMOS wells [7]. A triple well technology is required for this scheme. Furthermore, well biasing is complicated by the N-well to P-well junction leakage current as well as source/drain to well junction leakage currents. Both of the above schemes are implemented at the functional module level; for example, in the well biasing scheme, all the transistors in the functional module have the same variable V_T which is dependent on the well bias.

The aforementioned technologies have been mainly proposed for implementation in bulk silicon CMOS. However, the maturity of the SOI technology in the past few years cannot be

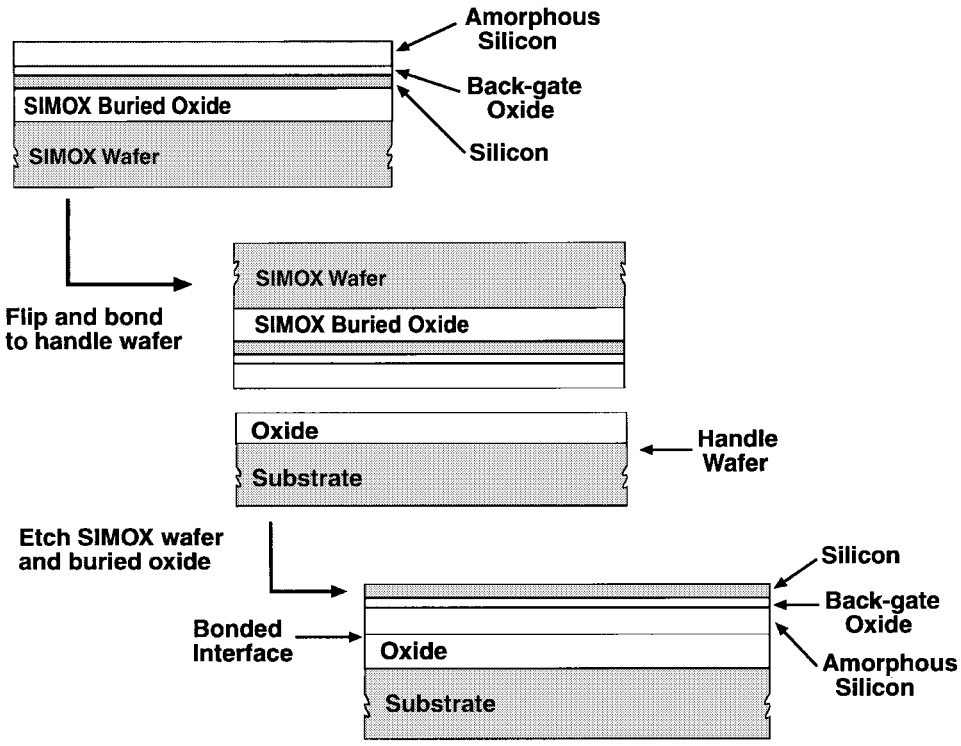


Fig. 1. SOIAS preparation using bonded SIMOX process.

ignored, especially with the dramatic improvements in material quality. There are two modes of operation for SOI MOSFET's: 1) fully depleted (FD) and 2) partially depleted (PD) channel region (body). In the conventional strongly FD SOI device, the silicon film thickness is usually less than or equal to half of the depletion width of the bulk device. The surface potentials at the front and back interfaces are strongly coupled to each other and capacitively coupled to the front-gate and the substrate through the front-gate oxide and buried oxide, respectively. Therefore, the potential throughout the silicon film, and hence the charge, is determined by the bias conditions on both the front-gate and the substrate. By replacing the substrate with a back-gate, the device becomes a dual-gated device. The FD design is unique to SOI because the front-gate and back-gate both have control of the charge in the silicon film. In the strongly PD SOI, the back-gate or substrate has no influence on the front surface potential. In the middle regime, the device is nominally PD and can become FD by applying a back-gate bias, thus, coupling of the front and back surface potentials still occurs. There have been numerous studies on the merits of fully depleted SOI CMOS and its implications for low-power electronics. Various researchers have exploited the use of FD SOI in dual-gated devices in which the top and bottom gates are tied and switched together, resulting in enhanced transconductance [8]–[11]. The SOIAS technology was developed to fabricate back-gated FD CMOS devices by capitalizing on existing SIMOX, wafer bonding, and thinning technologies [12]. The back-gate controls the (V_T) of the front-gate device, and the NMOS and PMOS back-gates are switched independently from each other and the front-gates. For burst-mode high-performance and low-power applications, the threshold voltage would be raised during idle periods to reduce the static leakage current, and lowered during active periods to achieve high performance. Similar to the well biasing scheme, the SOIAS technology is proposed to be implemented at the functional module level. This paper describes the development of the SOIAS technology with implementation in a selectively scaled CMOS SOI baseline process, and a theoretical evaluation for low-power logic applications.

III. SOIAS Preparation and Material Characterization

The SOIAS substrate is a multilayered blanket film stack consisting of the silicon wafer, insulating oxide, intrinsic polysilicon, back-gate oxide, and silicon film. Two different approaches have been taken for preparing the SOIAS wafers. The first is the more traditional route of the BESOI process. In this case, the device wafer includes the back-gate oxide (to be) which is obtained by dry thermal oxidation, and the back-gate material to be which is amorphous silicon (as deposited). This device wafer was then bonded to the handle wafer which was also oxidized to form approximately 1 μm of silicon dioxide. Therefore, the bonding interface is between the amorphous silicon and the thick insulating oxide. After bonding, the wafers were annealed in N_2 at 1000 °C for 1 h. The device wafer was then thinned back by chemical and mechanical polishing. Finally, localized plasma thinning (Accu-Thin)[1] was used to improve silicon film uniformity. The second approach involves the bonding of a SIMOX wafer. The buried oxide, in this case, served as an etch-stop using wet chemistry wafer etching. The same layers as described above were grown on the SIMOX and the handle wafers. The bonding interface was still between the amorphous silicon and

[1] Accu-Thin is a trademark technology of Hughes.

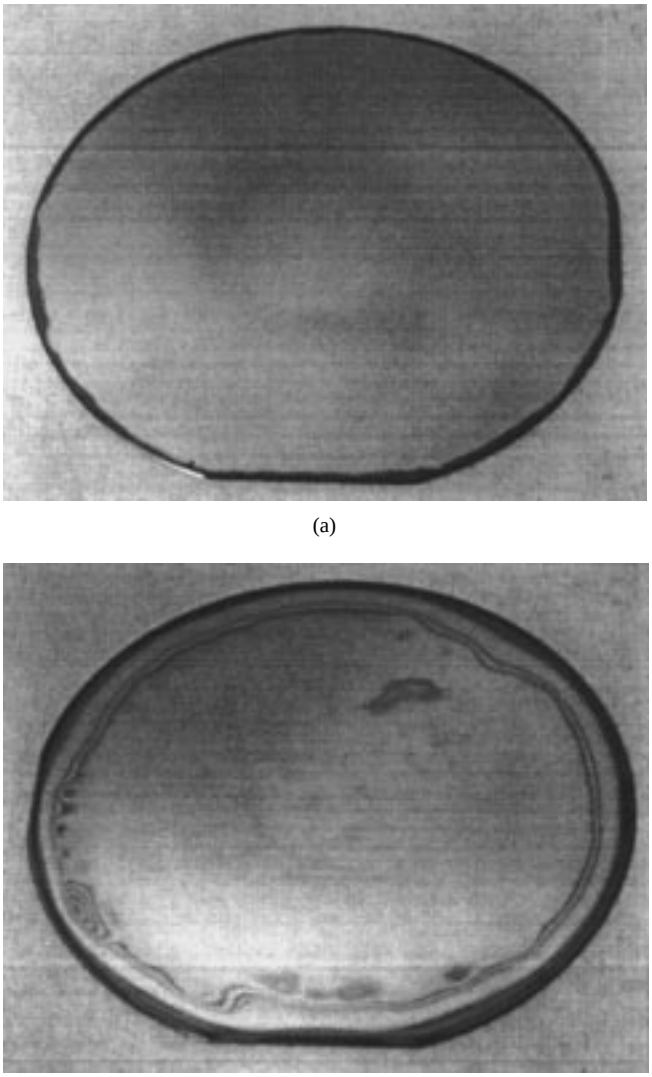


Fig. 2. SOIAS wafers prepared by bonded SIMOX (top), and BESOI processes (bottom).

the insulating oxide. Fig. 1 depicts the SOIAS preparation for the bonded SIMOX process. The bonded SIMOX wafers were etched in 25 wt% Tetramethyl Ammonia Hydroxide (TMAH), commonly known as photo resist developer, to remove the bulk of the SIMOX wafer, stopping on the buried oxide. The selectivity of silicon to oxide in TMAH is about 5000 to 1 at 80 °C [13]. Therefore, the resulting silicon film thickness is as uniform as that of the original SIMOX wafer. Final thinning of the silicon film was accomplished with thermal oxidation and wet oxide strip. Amorphous silicon was used as the back-gate material (to be) because as-deposited amorphous silicon is very smooth which facilitates direct bonding to the oxidized handle wafer. Fig. 2 shows the SOIAS wafers prepared by the bonded SIMOX and BESOI processes. The integrity of the SOIAS substrates is compared with the conventional SIMOX wafers through measurements of the effective electron mobility and Time Zero Dielectric Breakdown (TZDB) tests for intrinsic oxide quality. Fig. 3 shows the effective electron mobility versus effective transverse electric field of the front-gate device for conventional SIMOX and SOIAS. The universality of the curves indicates no apparent difference between the SOIAS and SIMOX substrates from a device operation point of view. Fig. 4 shows the cumulative percentage failure comparison of SOIAS with bulk and SIMOX substrates in the TZDB test. The bonded SIMOX SOIAS is slightly worse than the bond and etch-back SOIAS as well as the bulk and SIMOX. Overall, the intrinsic oxide breakdown of the SOIAS is comparable to those of bulk and SIMOX.

IV. Device Fabrication

The device fabrication on SOIAS follows the conventional CMOS SOI process with two additional steps. The back-gates were formed first by ion implantation through the silicon film in two masking steps, resulting in islands of p and n polysilicon insulated by intrinsic polysilicon after thermal anneal. Using the same type of doping in the back-gate polysilicon and silicon film resulted in near-zero flatband voltage at the back-gate. By properly tailoring the energy and dose of the implant, the back-gate and the V_T-adjust implants for setting quiescent V_T value (i.e., V_T at zero back-gate bias) can be done in one step. The peak of the back-gate implant is placed deep in the back-gate polysilicon, and the leading edge of the implant is used to dope the silicon film. Fig. 5 shows examples of the as-implanted and final boron and phosphorus concentrations in the silicon and back-gate from Suprem3 simulations. Typical sheet resistance of the back-gate poly is in the 1–5 KΩ/square range for the shown dopant concentrations in the back-gate. The front-gate device is then built as in a conventional SOI CMOS process using LOCOS isolation with an additional step of cutting the back-gate contacts. The back-gates were contacted through the top by cutting through the field oxide. Fig. 6(a) illustrates the final device schematic, and Fig. 6(b) is a SEM micrograph of the SOIAS device. The coupling between the front and back-gates depends on the ratio of the critical film thicknesses: front-gate oxide thickness $(t_{\rm fox})$, silicon film thickness $(t_{\rm si})$, and back-gate oxide thickness $(t_{\rm box})$. We have demonstrated SOIAS with 9-nm $t_{\rm fox}$, 40-nm $t_{\rm si}$, and 100-nm $t_{\rm box}$ nominal design parameters in a selectively scaled 1-μm baseline CMOS technology.

V. Device Results

Figs. 7 and 8 show the I–V and subthreshold device characteristics for NMOS and PMOS at two different threshold voltages tuned by biasing the back-gate; $L_{\rm eff}$ is 0.44 μm and 0.35 μm, respectively. A 250 mV change in threshold voltage results in a 3.5–4 decade reduction in off current and a 50–80% increase in on current at 1 V operation for PMOS and NMOS respectively. Fig. 9 shows the maximum and minimum tunable V_T limits for the above nominal design parameters. The x-axis is the designed quiescent V_T (V_T at $V_{gb} = 0$ V). The quiescent V_T was obtained either by varying the doping or the silicon film thickness. Therefore, for low quiescent V_T devices, the film is strongly fully depleted, i.e., either the doping level is low or the silicon film is thin. Similarly, for the high quiescent V_T devices, either the doping level is high or the silicon film is thick. The y-axis, tunable V_T, was obtained by applying various back-gate biases. The tunable V_T range is quite large

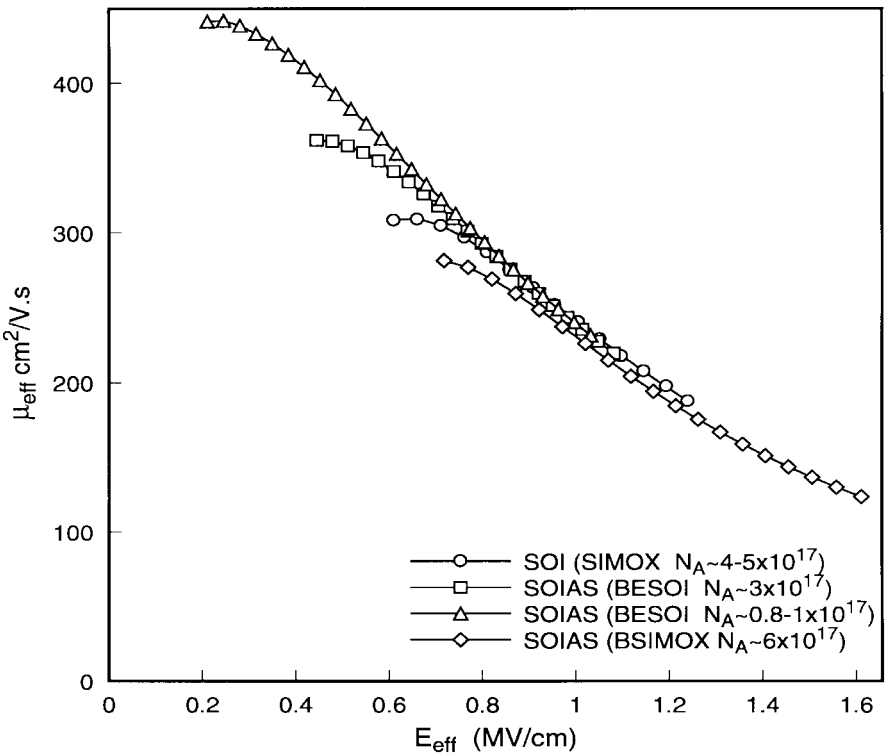


Fig. 3. Measured effective electron mobility for SIMOX and SOIAS.

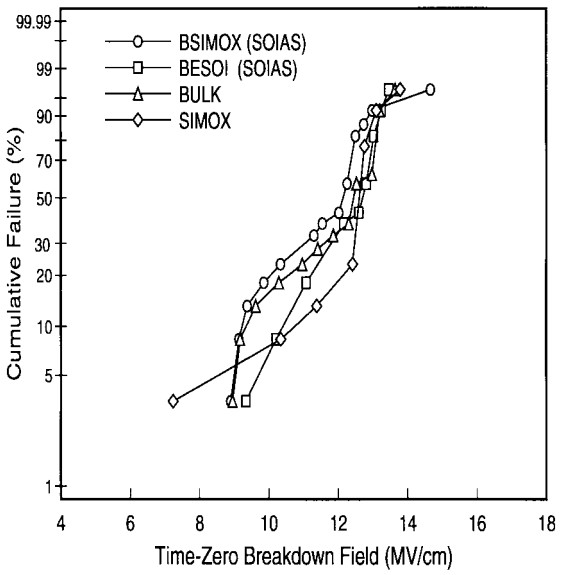


Fig. 4. Cumulative percentage failure of 1×10^{-6} cm^2 transistors.

(approximately 1 V) for fully depleted back interface as can be seen for the lowest quiescent V_T case ($V_T = -0.2$ V). The limits of the upper and lower tunable V_T range are determined by the back interface becoming either accumulated or inverted, in which case the back-gate becomes decoupled from the front-gate. Even for the partially depleted highest quiescent V_T case ($V_T = 1.0$ V), there is still a reasonable tuning range (approximately 0.5 V). This has implications for making FD SOI a viable technology since the threshold voltage and the device operating mode can be controlled precisely by the back-gate. Fig. 9 demonstrates that V_T can be fine tuned over a wide range despite variations in t_{si}(average thickness = 48.4 nm, maximum thickness = 69.9 nm and minimum thickness = 37.6 nm) and L_{eff}. For example, a nominal V_T of 500 mV can be reached even for a $\pm$400 mV deviation by using a $\pm$5–6 V back-gate bias. Typically, only a 200 mV switch in the V_T is sufficient to achieve approximately three decades reduction in the subthreshold leakage current. This design range fits well-within the limits of the tunable V_T band for the given films thicknesses and doping levels as shown in Fig. 9.

VI. Dynamic Operation

Fig. 10 shows the frequency of a 101-stage ring oscillator as a function of varying the back-gate-controlled V_T for either the NMOS or PMOS only; hence, complete independent control of the NMOS and PMOS device threshold voltages. Fig. 11 shows the actual output of the ring oscillator. For a 200 mV change in V_T for both the NMOS and PMOS, the result is a 36% change in the speed at V_{DD} of 1 V. In order for this scheme of dynamic threshold control to work properly, the V_T must change quasi-statically with back-gate switching. This is of concern because of the relatively high back-gate sheet resistance. The verification of this quasi-static control of the V_T was carried out with an experiment depicted in Fig. 12. An NMOS transistor's gate was tied to V_{DD} of 0.5 V which is close to the threshold voltage of this device at zero back-gate bias, and a 50 ohm resistor was placed between V_{DD} and the drain. The back-gate was pulsed at various frequencies and pulse heights while the output at the drain, V_{out} was monitored. The device under test has an annular gate with a large 23 $\times$ 25 μm back-gate with one contact off to the side. When the back-gate input pulse is high, V_{out} is low because more current

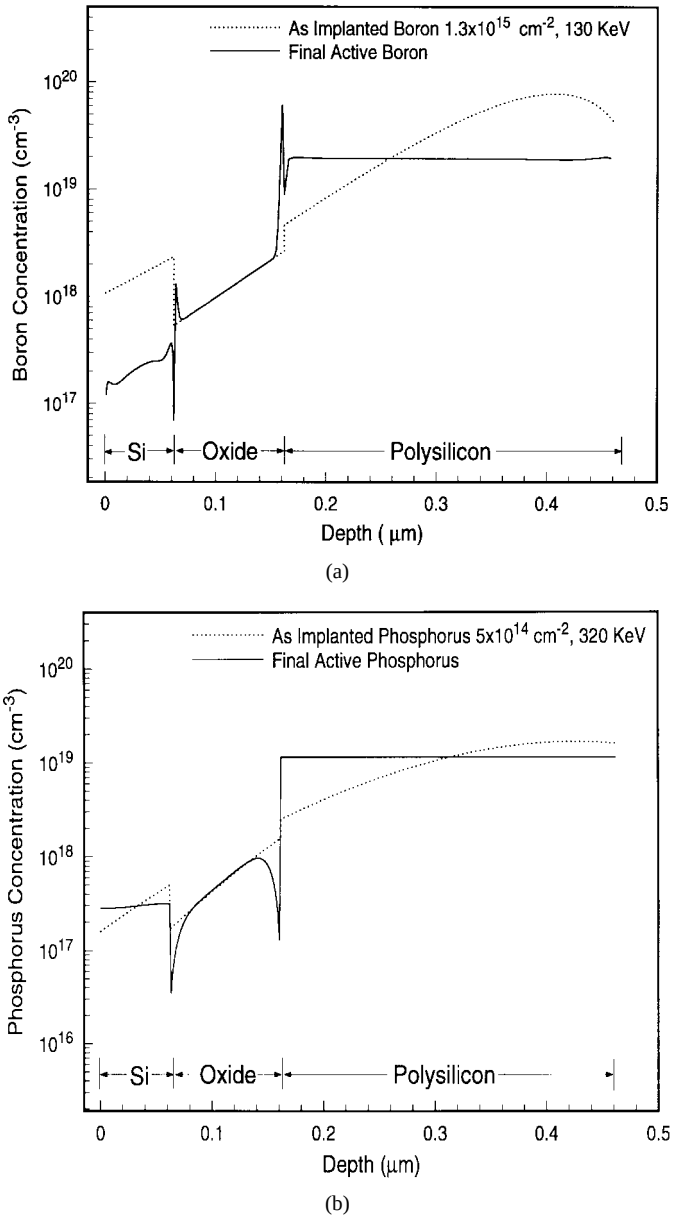


Fig. 5. Suprem3 simulated boron and phosphorus concentrations in SOIAS devices.

is pulled through the resistor due to a lowered V_T. Fig. 12 shows the V_{out} at 5, 10, and 20 MHz pulses on the back-gate. Even at 20 MHz, the V_{out} is still following the input pulse for this fairly large back-gate. Knowing the V_{out} value, the dynamic current due to lowering of the V_T, i.e., switching of the back-gate, can be overlayed onto the dc measured currents for various back-gate biases, i.e., pulse heights. The dynamic current was simply calculated as $(V_{DD} - V_{\text{out}})/R$, where R is the resistor value. Fig. 13 shows the composite of these two measurements. The x-points lying precisely on the dc measured current curves is indicative of the quasi-static control of the device V_T through dynamic back-gate biasing.

VII. Application to Low-Power Systems

Having demonstrated the technology, a theoretical model was developed to evaluate and compare the total energy

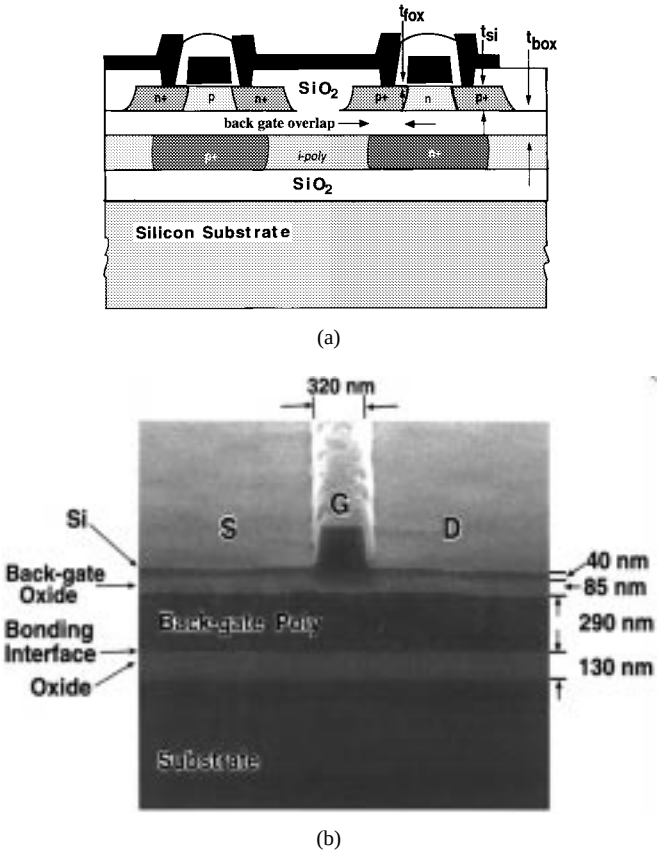


Fig. 6. (a) SOIAS back-gated CMOS device schematic. (b) SEM micrograph of SOIAS device cross section.

dissipation for the SOIAS technology versus an optimized low-power SOI CMOS technology. We have chosen to assume a model of operation in which "functional units," or modules, share a common V_T, i.e., all same polarity transistors in such modules have the same V_T. This implies, in addition to the module's conventional gated clock in the SOI implementation, another gated clock would be needed for the back-gate control. Under this model, an active module's idle devices are left in a low-leakage state. In the modeling of a microprocessor's energy dissipation, various modules were considered such as the ALU adder unit, the shifter, and the integer multiplier. In order to analyze the applicability of the SOIAS technology to low-power static CMOS logic, we have developed total energy equations including switching and static energies for a SOIAS and the benchmark SOI technology:

$$\begin{aligned} E_{\text{SOIAS}} = {} & \chi A_{fg}\gamma C_1 V_{dd}^2 \quad \text{Dynamic Energy} \\ & + \chi A_{fg} I_{\text{off(low)}} V_{dd} t_c \quad \text{Static Leakage Energy} \\ & + (1 - \chi A_{fg}) I_{\text{off(high)}} V_{dd} t_c \\ & + \chi A_{bg} C_{\text{box}} V_{gb}^2 \quad \text{Back}-\text{gate Switching Energy} \\ E_{\text{SOI}} = {} & \chi A_{fg}(\gamma C_2 V_{dd}^2) \quad \text{Dynamic Energy} \\ & + I_{\text{off(low)}} V_{dd} t_c \quad \text{Static Leakage Energy.} \end{aligned}$$

These equations include:

(a) *Algorithm and architecture parameters:*

A_{fg} module activity factor

A_{bg} back-gate activity factor

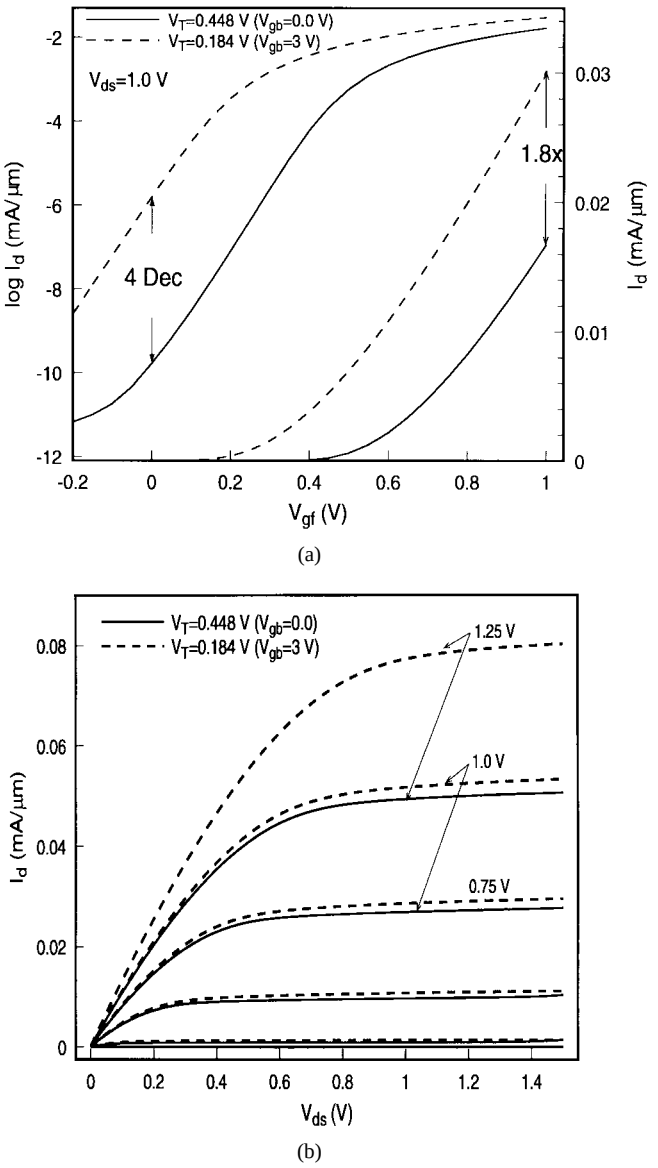


Fig. 7. Measured NMOSFET $I-V$ and subthreshold characteristics tuned at different V_T's, $L_{\text{eff}} = 0.44\ \mu$m.

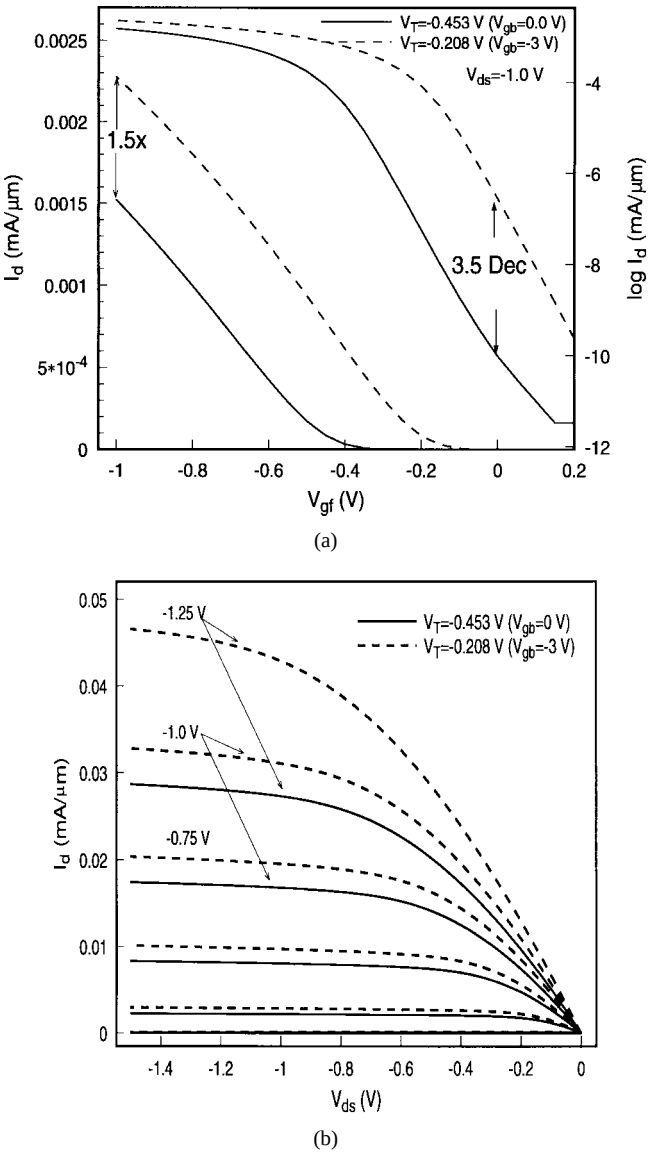


Fig. 8. Measured PMOSFET $I-V$ and subthreshold characteristics tuned at different V_T's, $L_{\text{eff}} = 0.35\ \mu$m.

γ node switching probability during active period

χ system activity of processor during interactive computation

(b) *Technology and circuit parameter:*

t_c $1/f_{\text{clock}}$

(c) *Technology parameters:*

C_1, C_2 total physical capacitance (gate capacitance + front-gate overlap capacitance + fringing capacitance + back-gate overlap capacitance)

$I_{\text{off(low)}}$ low V_T off current

$I_{\text{off(high)}}$ high V_T off current

C_{box} back-gate oxide capacitance

V_{gb} back-gate bias

The total energy equation for the SOIAS is composed of three components, the dynamic switching energy, the static leakage energy, and the overhead energy required to switch the back-gate. For the SOI technology, the total energy is composed of the dynamic switching energy and the static leakage energy. The applicability of SOIAS technology is a strong function of system, functional block and transistor usage, i.e., the parameters χ, A_{fg}, A_{bg}, and γ. A_{fg} is the module activity factor which is the fraction of time a module (e.g., an adder) is "on," i.e., doing computation. A_{bg} is the back-gate activity factor which is dependent on how frequently the module is "on". One important point to note here is that the back-gate activity factor (A_{bg}) is always less than or equal to the module activity factor (A_{fg}). For example, an adder can be active several cycles in a row, and hence the V_T for this module is then left in the low V_T state during those cycles. Therefore the back-gate only needs to be switched once for all the consecutive cycles that the module is active. The dynamic switching energies for the SOIAS and SOI technologies are approximately the same for burst-mode as well as continuously computing systems. Therefore, the sum of the static leakage energy and the back-gate switching energy for the SOIAS technology must be less than the static leakage energy of the

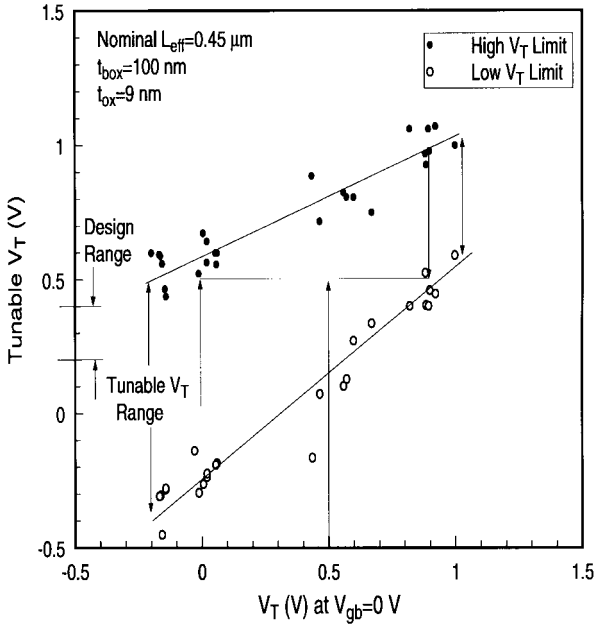


Fig. 9. Measured tunable V_T range by back-gate biasing. The upper and lower limits of the tunable V_T range was determined by the back interface becoming either inverted or accumulated. The variation in the quiescent V_T (i.e., $V_{gb} = 0$ V) was determined by doping in the channel, silicon film thickness, and $L_{\rm eff}$ variations. The typical design range of 200 mV switch in V_T (as indicated by the two bars on the y-axis) fits well within the tunable V_T band. $\Delta V_T/\Delta V_{gb} \simeq 80$ mV/V.

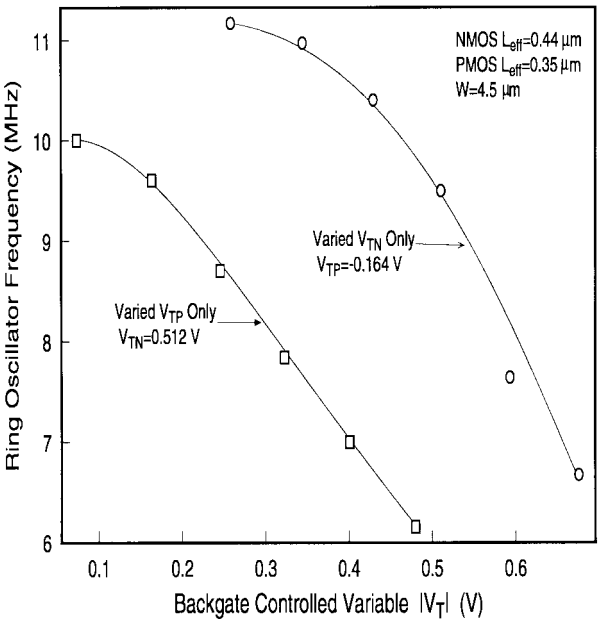


Fig. 10. Measured 101 stage ring oscillator output frequency as varied by changing V_T.

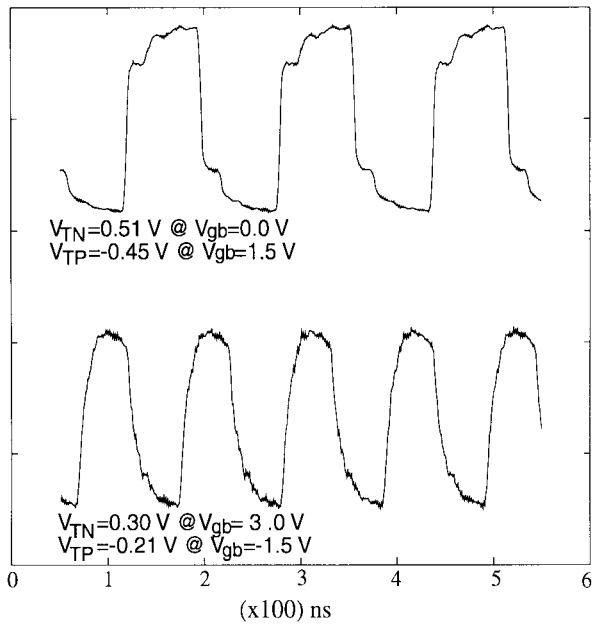


Fig. 11. Measured ring oscillator output at different V_T's tuned by back-gate bias, for V_T change of 200 mV, 36% change in the speed was observed at $V_{DD} = 1$ V.

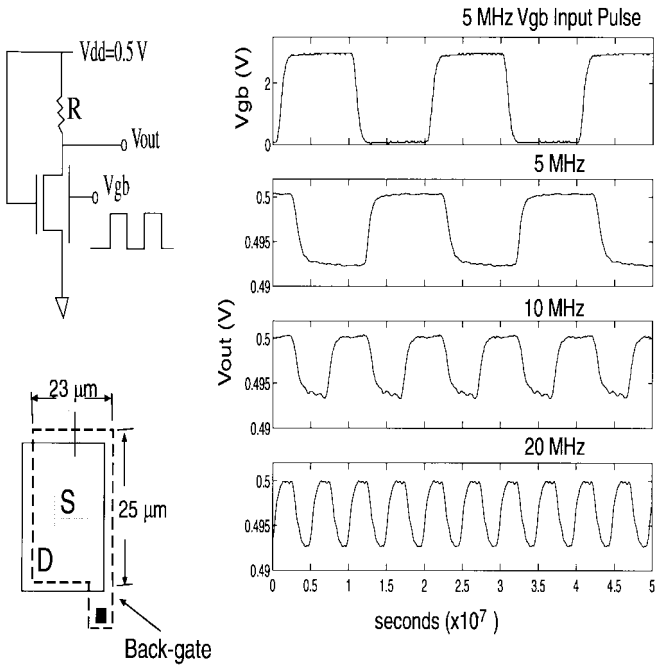


Fig. 12. Schematic illustration of dynamic back-gate switching device and measurement setup. Measured output of device ($V_{\rm out}$) is also shown for various frequencies of the back-gate pulse.

constant low V_T SOI technology for low-power applications. For burst-mode computational systems ($\chi \sim$1–2%), the χA_{fg} and χA_{bg}, are numbers much smaller than one. Therefore, the back-gate switching overhead energy is small due to χA_{bg} being a small number. The static energy for the SOIAS technology would also be much less than that of the SOI technology because the low V_T leakage energy is weighted by a very small number χA_{fg} and the high V_T leakage energy is low due to low subthreshold leakage.

In order to determine functional block usage patterns (A_{fg} and A_{bg}), a series of program profiling experiments were performed using the ATOM code instrumentation interface [14] for a particular microprocessor implementation, compiler technology, and various algorithms. The ratio of the total energy dissipation for SOIAS and SOI was analyzed as a function of algorithm and architecture dependent parameters (A_{fg} and A_{bg}, see Fig. 14). The simulation parameters are: $t_{\rm si} = 40$ nm for the practical limit of thinning the silicon

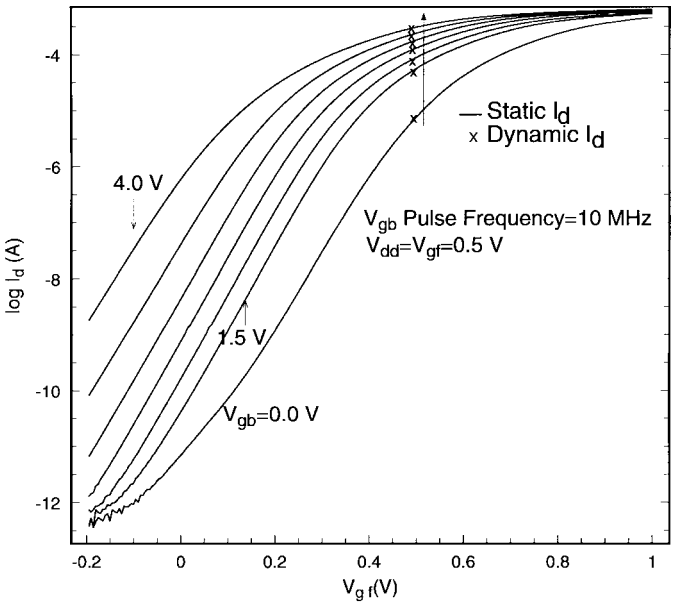


Fig. 13. Overlay of measured dynamic currents (extracted from the device and setup as shown in Fig. 12) due to switching of back-gate at 10 MHz on the measured dc currents at various back-gate voltages. The quasi-static switching of the V_T was verified by the precise overlay of the dynamic and dc currents.

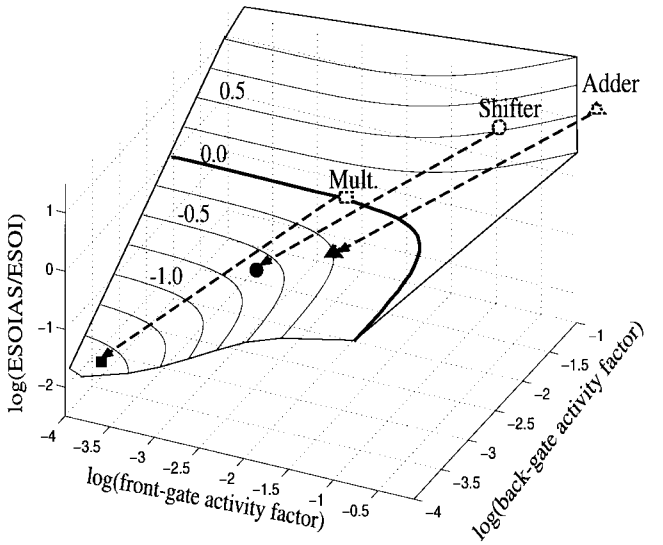
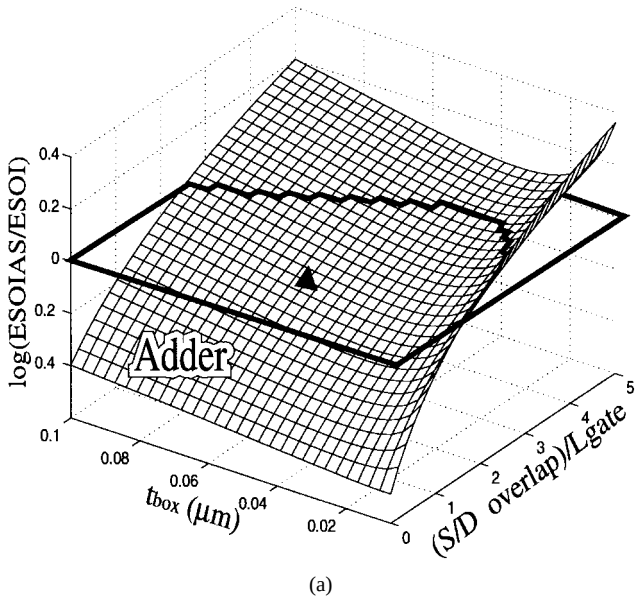
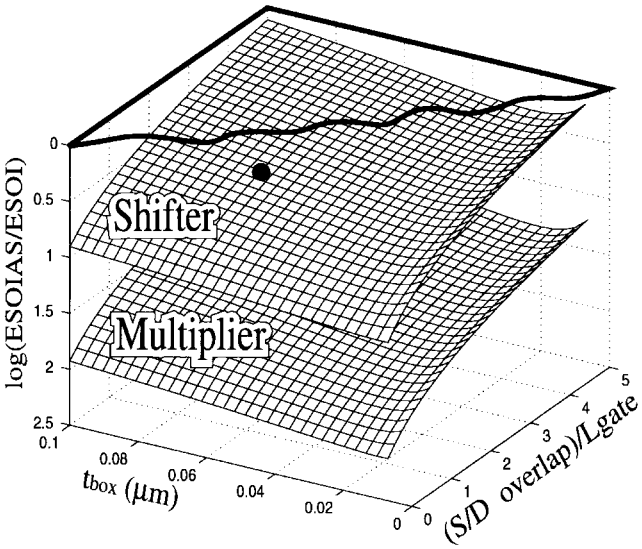


Fig. 14. Energy ratio of SOI and SOIAS technologies for systems that are frequently in use (open symbols $\chi = 100\%$) and those that are mostly idle (filled symbols $\chi = 2\%$) as a function of front-gate (module) and back-gate activities. Switching of the back-gate in low-activity modules provides significant static leakage energy saving with minimal additional back-gate switching energy. For high-activity modules, the back-gate would not be switched.



(a)



(b)

Fig. 15. Energy ratio of SOI and SOIAS in the technology design space for the adder, shifter, and multiplier functional modules operating in burst mode ($\chi = 2\%$). The dark line demarcates the break-even plane. In order to minimize the cost of switching the back-gate, the source/drain overlap must be minimized and $t_{\rm box}$ must be optimized. For the low-activity modules, the shifter and multiplier, SOIAS with any $t_{\rm box}$ and S/D overlap value in this space will provide energy savings. The higher activity adder module design space is shrunken due to the higher cost of switching the back-gate. The filled triangle and circle symbols correspond to the same points in Fig. 14.

film, $t_{\rm fox} = 7$ nm for a 0.25-μm $L_{\rm eff}$ technology; γ, the probability of a gate switching in one active cycle, is assumed to be 40% and is obtained by estimating a ripple carry adder under random input pattern (γ in general is a strong function of bit transition probabilities), 100 MHz clock frequency, $V_{T,\rm SOIAS}(\rm low) = V_{T,\rm SOI} = 200$ mV, $V_{T,\rm SOIAS}(\rm high) = 400$ mV, and $V_{DD} = 1.0$ V.

Fig. 14 shows the ratio of total energy dissipation for the SOIAS and SOI technologies. The dark line demarcates the break-even contour. For near continuous functional block usage which does not exhibit strong temporal locality (e.g., adder and shifter in a continuously computing system, χ =100%), the back-gates would not be switched, and hence $E_{\rm SOIAS}$ would be equal to $E_{\rm SOI}$ at constant low V_T. However, if the back-gate were to be switched in such systems, the cost in energy for switching the back-gate is high, and therefore, the $E_{\rm SOIAS}$ would be greater than $E_{\rm SOI}$. This is indicated in Fig. 14 by the dotted open symbols. In a system which is frequently idle while awaiting I/O, such as an X-server with $\chi = 2\%$, the SOIAS technology dissipates much less energy than conventional SOI: 43% less for the adder ($A_{fg} = 70\%, A_{bg} = 21\%$), 80% less for the shifter ($A_{fg} = 11\%, A_{bg} = 9\%$), and

97% less for the multiplier ($A_{fg} = 0.8\%, A_{bg} = 0.8\%$). This is indicated by the filled symbols in Fig. 14. In this case, the savings in static leakage energy due to changing of the V_T is much greater than the overhead energy due to switching of the back-gate. As the system and module activities become lower, the energy savings is even greater.

For the given burst-mode algorithmic parameters, the latitude in the technology design can be shown in technology parameter space, in this case, $t_{\rm box}$ and source/drain overlap with the back-gate are the parameters of choice because they reflect the energy cost of switching the back-gate. Fig. 15 shows the ratio of total energy dissipation in the technology design space for the three modules. The plane outlined in dark is the break-even plane for SOIAS and conventional SOI technology. The S/D overlap with the back-gate is normalized to gate length. For low-activity modules (the multiplier and shifter), the design space in favor of the SOIAS technology spans the entire parameter range under study for both $t_{\rm box}$ and S/D overlap, Fig. 15(b). This implies that for any design value of $t_{\rm box}$ and S/D overlap in this space, the back-gate switching energy is significantly less than the static leakage energy saved by dynamically controlling the V_T. For high-activity modules (the adder), the design space in favor of SOIAS technology is smaller because higher module activity implies higher switching frequency of the back-gate, and hence higher energy cost, see Fig. 15(a). There is, however, an optimal range of $t_{\rm box}$ which allows the most S/D overlap, i.e., the most process latitude, where the energy is minimized for the adder module.

VIII. Conclusions

Successful preparation of SOIAS substrates is a crucial part of this technology, and we have shown the preparation of substrates using two different approaches. The dynamic control of threshold voltage has been successfully demonstrated in a baseline CMOS process. Furthermore, the dynamic operation of these devices was shown to be robust and the quasi-static control of the V_T was verified. The flexibility in threshold voltage control through back-gate biasing from partially depleted to fully depleted devices provides a viable option for FD SOI. Finally, the theoretical energy evaluation of the SOIAS technology for low-power design of burst-mode computational systems showed significant energy savings.

Acknowledgment

The authors gratefully acknowledge the help of C. Goodwin of AT&T, Reading, PA, and D. P. Mathur of Hughes, Danbury, CT, in wafer thinning. The authors also would like to thank IBIS Corporation for providing all the SIMOX material, and A. Lochtefeld for helping with the TZDB measurements.

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