Non-linear Operating Point Statistical Analysis for Local Variations in Logic Timing at Low Voltage

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***Abstract*—For CMOS feature size of 65 nm and below, local (or intra-die or within-die) variations in transistor Vt contribute stochastic variation in logic delay that is a large percentage of the nominal delay. Moreover, when circuits are operated at low voltage (Vdd ≤ 0.5V), the standard deviation of gate delay becomes comparable to nominal delay, and the Probability Density Function (PDF) of the gate delay is highly non-Gaussian. This paper presents a computationally efficient algorithm for computing the PDF of logic Timing Path (TP) delay, which results from local variations. This approach is called Non-linear Operating Point Analysis for Local Variations (NLOPALV). The approach is implemented using commercial STA tools and integrated into the standard CAD flow using custom scripts. Timing paths from a 28nm commercial DSP are analyzed using the proposed technique and the performance is observed to be within 5% accuracy compared to SPICE based Monte-Carlo analysis.**

Keywords- SSTA, Local Variations, Low-voltage, Statistical Design

I. INTRODUCTION

There are three categories of process variations that are important in design of modern CMOS logic [1].

1. Global random variation in gate length, gate width, flatband voltage, oxide thickness and channel doping.
2. Systematic or predictable variations, such as variations in litho or etch or CMP.
3. Local random variations in transistor parameters. Local random variations are assumed to be random from one transistor to another within a die.

This paper deals with the effect that local variations in CMOS transistor parameters have on logic timing at low voltage (Vdd ≤ 0.5V). Local variations are primarily the result of variations in the number of dopant atoms in the channel of CMOS transistors [2, 3]. Local variations have long been known in analog design and in SRAM design. In analog design, local variations are called "mismatch" because of the mismatch in the V_t of adjacent transistors. But they have not generally been a problem for logic. However, shrinking of transistor geometries and low voltage design, for ultra-low power applications, make local variations increasingly important for logic.

Some approaches for handling local or intra-die variations have been proposed [4-8]. However this paper extends previous work in several important ways. It describes an approach to calculate the PDF of logic TP delay which results from local transistor variation. We call this approach the Non-linear Operating Point Analysis for Local Variations (NLOPALV). At Vdd ≤ 0.5V, circuit delay is highly non-linear in V_t variation. The result is that the PDF of the delay is highly non-Gaussian. As shown later in this paper, the Gaussian assumption results in substantial error at Vdd = 0.5V. This approach deals only with local variations and needs to be used in conjunction with conventional approaches to generate global fast and slow corners.

The effect of local variations is very different from the effect of Global variations. Whereas global variations in delay add linearly, local variations do not. Let us assume, for a moment that the PDF of each cell is Gaussian. If we have a number of such cells having local stochastic delay characterized by standard deviation of σ_i, the delays add in "quadrature", meaning that the variance of the TP delay is given by $\sigma_{TP}^2 = \sum \sigma_i^2$. If we add the σ_i linearly, we would get an overly pessimistic result. In this paper, we employ the concept of "operating point", which has the advantage that the stochastic delay of a TP can be computed by **linearly adding** the operating point delays of the respective cells.

The first step in calculating the effect of local variations on logic timing is the characterization of standard logic cells for local variation. Characterization needs to be done for each arc for each cell. An arc is defined by 1) input rise or fall, 2) output load capacitance and 3) input slew. Characterization needs to be done for each global corner of importance.

The analysis of this paper starts with pre-characterized logic cells. For every arc of every cell (every arc-cell) there exists a PDF of the delay. Referring to Fig. 1, it is clear that any arbitrary (in general non-Gaussian) PDF can be mapped onto a unit variance Gaussian through the Cell-Arc Delay Function (CADF) $D(\xi)$. Note, for a Gaussian PDF, $D(\xi)$ is a straight line: $D(\xi)= \sigma_i\xi$. Characterization also provides the Cell-Arc Slew Function (CASF) $S(\xi)$, which is the most probable output slew for each value of ξ. The computational efficiency of the NLOPALV approach results from the fact that the entire PDF of the TP is not usually required. In TP analysis, we are usually interested in the f-sigma delay where f ~ +3 for setup time and f ~ -3 for hold time.

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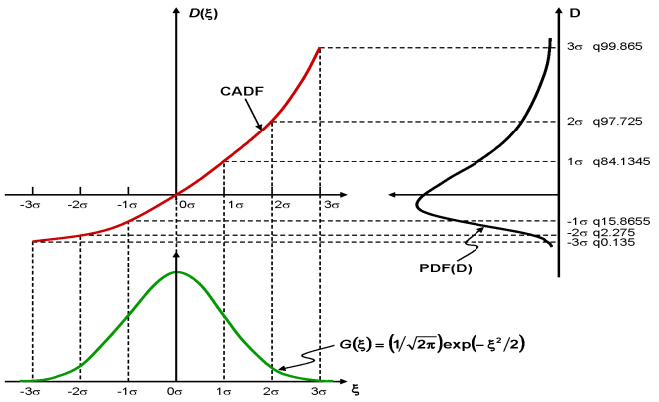

Figure 1. Gaussian mapping of non-Gaussian PDF through CADF

In the space allowed for this paper, the complete theory underlying the NLOPALV approach can not be presented. In section II, the NLOPALV approach will be presented without derivation. The validity of the approach will be demonstrated by the accuracy of the results on actual circuits presented in section II and III. The theoretical justification will be presented in a future publication.

II. MULTI-STAGE LOGIC PATH SSTA ANALYSIS

The goal of multi-stage SSTA is to determine the *3-sigma* TP delay (or in general the *f-sigma* TP delay) without incurring the computational expense of computing the entire PDF of the TP delay. In general, the PDFs of the logic cell delays are highly non-Gaussian. However, even in the non-Gaussian case, the concept of *f-sigma* delay has meaning. As shown in Fig 1, the *1-sigma* point is the 84.1345% quartile, the *3-sigma* point is the 99.8650% quartile etc. However, in the non-Gaussian case, the σ defined by quartile is unrelated to the standard deviation of the non-Gaussian variable. Using the NLOPALV approach, the TP operating point is determined, and the *f-sigma* operating point delay is approximated by a linear combination of operating point delays for the individual logic cells. This is done without the need for Monte-Carlo simulations or additional SPICE simulations.

A. Single Logic Path

We start with a timing path of N logic cells, each of which is characterized by $D_i(\xi_i)$, and we want to determine the f-sigma TP delay. For simplicity, we assume that the stochastic delays D_i are statistically independent. (We will see below that this simplifying assumption is not true, and we will address this complication.) We define the f-sigma operating point as:

$$\xi_i^{op} = \frac{f\alpha_i^{op}}{\sqrt{\sum_{j=1}^{N}(\alpha_j^{op})^2}} \text{ ; where } \alpha_i^{op} = \left(\frac{dD_i}{d\xi_i}\right)_{op} \quad (1)$$

Equation (1) needs to be solved iteratively, but once the operating point of the TP is determined, we can approximate the f-sigma timing path delay as a linear sum of operating point delays of the constituent logic cells:

$$D_{f\sigma}^{TP} \approx \sum_i D(\xi_i^{op}) \quad (2)$$

To graphically illustrate this concept, consider the following. At the operating point, $D_{TP}(f) = D_{f\sigma}$. Furthermore, the operating point lies on the hyper-sphere $\sum_i \xi_i^2 = f^2$. From this, it follows that the operating point results from the simultaneous solution of the above equations.

Considering $D_{f\sigma}^{est}$ as initial estimates of $D_{f\sigma}$ we get a family of curves. The Operating Point is the point of tangency of the curve $D_{TP}(f) = D_{f\sigma}^{est}$ with the hyper-sphere $\sum_i \xi_i^2 = f^2$ and the value of $D_{f\sigma}^{est}$ that defines the curve is the desired value of $D_{f\sigma}$ Fig 2 illustrates this idea.

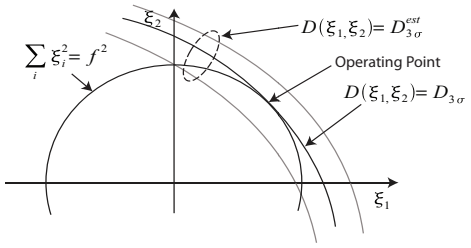

Figure 2. Multi-stage Operating Point

In the 2-stage case, making linear approximation in the region near the operating point, we can determine the operating point as the point of tangency of the line $\alpha_1\xi_1 + \alpha_2\xi_2 = D_{f\sigma}$ with the circle $\xi_1^2 + \xi_2^2 = f^2$. The operating point can thus be given as: $\xi_1^{op} = \frac{f\alpha_1}{\sqrt{\alpha_1^2+\alpha_2^2}}$ and $\xi_2^{op} = \frac{f\alpha_2}{\sqrt{\alpha_1^2+\alpha_2^2}}$ (3)

This analysis can be easily extended to N stage timing path where the operating point is given by equation (1).

However, in real timing paths, the stage delays D_i are not statistically independent. The stochastic delays of adjacent stages are correlated since the output slew of one stage is the input slew of the next. This correlation can be incorporated into the timing path analysis by modifying the operating point as:

$$\xi_i^{op} = \frac{f(\alpha_i + \eta_{i,i+1} + \lambda_{i,i+2})}{\sqrt{\sum_{i=1}^{N-2}(\alpha_i + \eta_{i,i+1} + \lambda_{i,i+2})^2}} \quad (4)$$

Where, $\alpha_i = \frac{dD_i}{d\xi_i}$, $\eta_{i,i+1} = \frac{dD_{i+1}}{d\xi_i} = \left(\frac{dD_{i+1}}{dS_{i,i+1}}\right)_{op}\left(\frac{dS_{i,i+1}}{d\xi_i}\right)_{op}$

$$\lambda_{i,i+2} = \frac{dD_{i+2}}{d\xi_i} = \left(\frac{dD_{i+2}}{dS_{i+1,i+2}}\right)_{op}\left(\frac{dS_{i+1,i+2}}{dS_{i,i+1}}\right)_{op}\left(\frac{dS_{i,i+1}}{d\xi_i}\right)_{op} \quad (5)$$

1) Algorithm for Non-linear Operating Point Analysis for Local Variations (NLOPALV)

This approach leads us to an iterative algorithm for determining the operating point and thereon computing $D_{f\sigma}$ that can be summarized as follows:

1. Determine the nominal delays D_i^{nom} for each stage in the timing path.
2. Make the initial estimate of the operating point as: $$\xi_i^{op} = \frac{fD_i^{nom}}{\sqrt{\sum_i (D_i^{nom})^2}}$$
3. At the estimated operating point, calculate α_i, $\eta_{i,i+1}$ and $\lambda_{i,i+2}$ for $1 \le i \le N$ as defined by (5).
4. Compute new estimate of the operating point using the expressions given by (4).
5. Repeat steps 3 and 4 until the operating point converges to a constant value.
6. The TP delay can then be obtained as:

$$D_{TP}(f) = \sum_{i=1}^{N} D_i(\xi_i^{op}) + \sum_{i=1}^{N-1} D_{i+1,i}(\xi_i^{op}) + \sum_{i=1}^{N-2} D_{i+2,i}(\xi_i^{op}) \quad (6)$$

where, $D_i(\xi_i^{op})$ is directly obtained from the cell characterization data and:

$$D_{i+1,i}(\xi_i^{op}) = \left(\frac{dD_{i+1}}{dS_{i,i+1}}\right)_{op} S_i^{op}(\xi_i^{op}) \quad (7)$$

$$D_{i+2,i}(\xi_i^{op}) = \left(\frac{dD_{i+2}}{dS_{i+1,i+2}}\right)_{op} \left(\frac{dS_{i+1,i+2}}{dS_{i,i+1}}\right)_{op} S_i^{op}(\xi_i^{op}) \quad (8)$$

B. Integration with the CAD flow

In order to effectively use SSTA in the design process, it is important to integrate the NLOPALV algorithm with existing CAD flow. The NLOPALV algorithm presented above is integrated with a commercial STA Timer. Fig 3 describes the process in the form of a flow-chart.

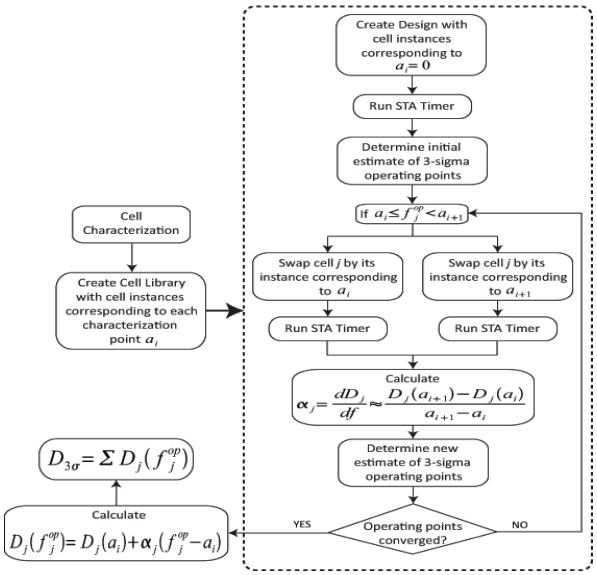

Figure 3. CAD flow for Logic Path NLOPALV analysis

C. Results

To validate the NLOPALV approach developed here, we tested it on logic paths taken from a commercial Digital Signal Processor implemented in 28nm technology, operating at 0.5V. We used the NLOPALV algorithm and the corresponding CAD flow to determine 3-sigma delay for the logic timing path and compared the results with those obtained from SPICE based Monte-Carlo analysis. Fig. 4 shows the comparison results for different timing paths.

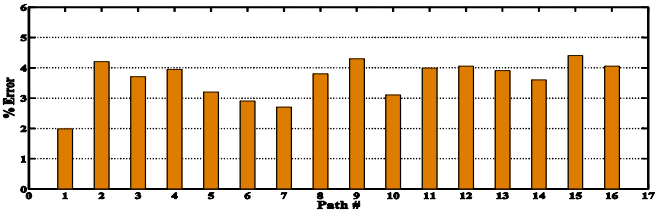

Figure 4. Performance comparison for NLOPALV vs. Monte-Carlo

The 3-sigma delay obtained from NLOPALV analysis is within 5% accuracy compared to 10,000 points SPICE based Monte-Carlo analysis. Theoretical analysis shows that the NLOPALV approach always underestimates the stochastic delay compared to Monte-Carlo analysis and this is validated by Fig. 4.

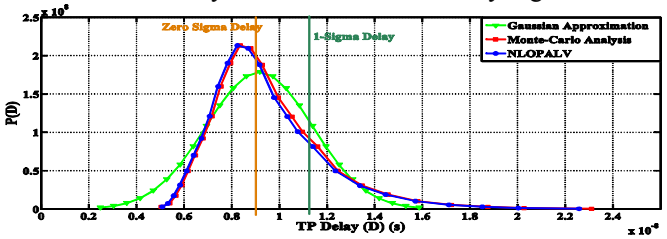

Figure 5. TP delay PDF: The zero-sigma delay is the nominal delay. The Gaussian approximation is chosen such that the standard deviation for the Gaussian is same as the 1σ delay for NLOPALV

Fig 5 shows comparison between the NLOPALV approach and Monte-Carlo for a typical timing path at 0.5V. It shows excellent agreement between the NLOPALV approach and Monte Carlo and also illustrates the inadequacy of the Gaussian approximation at low voltage. It is informative to note that:

1. The PDF of the TP delay peaks at a point in time that is less than the nominal delay (zero-sigma delay)
2. The mean of the non-Gaussian PDF lies 1.6ns to the right of the nominal delay, whereas in the Gaussian approximation, the stochastic delay has zero mean.
3. The 3σ stochastic delay is delay is 13.41ns, compared to a nominal delay of 9.17ns. This shows that the variation at 0.5V can be much higher than the nominal delay itself.
4. The 3-sigma stochastic delay calculated using the Gaussian approximation is 8.53ns compared to the actual 3-sigma stochastic delay of 13.41ns. This shows that the Gaussian approximation is highly optimistic.

The NLOPALV analysis was performed on different paths of different lengths, taken from the 28nm Digital Signal Processor. Table 1 summarizes additional results for a few of these paths. The 3-sigma delay (nominal + 3σ stochastic delay) computed using NLOPALV shows excellent agreement with Monte-Carlo. This contrasts with the large errors that result when the delay is assumed to be Gaussian.

TABLE I. PERFORMANCE COMPARISON OF NLOPALV VS. MONTE-CARLO AND GAUSSIAN APPROX.

TP #	Nominal Delay (ns)	3-Sigma Stochastic Delay (ns)				
		NLOPALV	*Monte-Carlo*	*% Error*	*Gaussian Approx.*	*% Error*
1	2.81	4.38	4.61	4.98%	2.38	45.6%
2	4.07	4.31	4.59	6.10%	2.68	37.8%
3	6.88	7.89	8.33	5.28%	4.19	45.5%
4	9.76	13.15	13.86	5.12%	6.22	52.7%
5	14.33	16.30	17.34	5.99%	7.88	50.7%
6	22.59	25.95	27.55	5.80%	13.27	48.9%
7	27.12	30.16	32.18	6.21%	14.80	50.9%
8	32.71	29.85	31.75	5.98%	14.00	53.1%

III. TIMING PATH SETUP AND HOLD ANALYSIS

After verifying the approach on single logic paths, we now extend it to perform setup and hold time analysis on timing paths including clock paths. Fig 6 shows a typical timing path for setup/hold analysis.

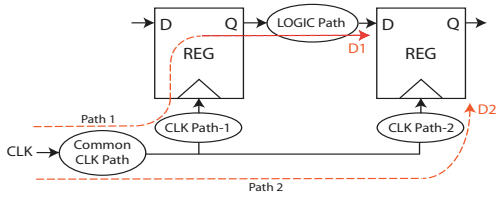

Figure 6. Typical timing path for setup/hold analysis

Consider the hold constraint: $D_1 > D_2 + T_{hold}$

In presence of statistical variations, we need to make sure that:

$$(D_1 - D_2)_{-3\sigma} - T_{hold}^{3\sigma} > 0 \quad (9)$$

Similarly, we can get the setup constraint as:

$$(D_1 - D_2)_{3\sigma} + T_{setup}^{3\sigma} < T_{CLK} \quad (10)$$

Where, T_{CLK} is the clock period for the design. The PDFs for setup/hold time for the registers are obtained from cell characterization. The NLOPALV approach described in section II can be used to compute $(D_1 - D_2)_{-/+3\sigma}$ by considering the paths D1 and D2 together and computing the +/-3σ operating point for the cells in both these paths taken together.

This approach is verified by considering timing paths along with the corresponding clock paths from a Digital Signal Processor. The 3σ setup/hold slack is computed using the NLOPALV approach described above and the results are compared with those obtained from SPICE based Monte-Carlo simulations. Timing paths taken from the same DSP are used and the results are summarized in Fig. 7 in the form of % error compared to Monte-Carlo analysis.

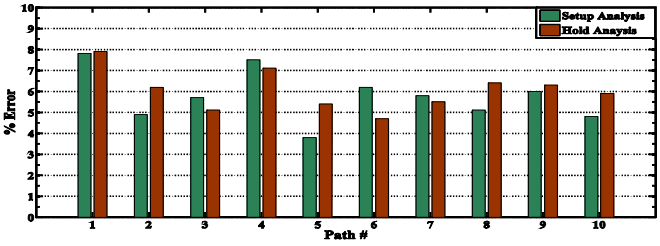

Figure 7. Setup/hold analysis: NLOPALV vs. Monte-Carlo

IV. CONCLUSIONS

This paper presents a computationally efficient approach to calculating the stochastic delay in logic at low voltage. The approach has been implemented using commercial STA tools and integrated into the existing standard CAD flow. The approach is verified by performing 3-Sigma delay computations for critical paths taken from a commercial Digital Signal Processor. Comparison of the results with those obtained from detailed SPICE based Monte-Carlo analysis demonstrates the high accuracy of the approach.

The NLOPALV computation runs in linear time with respect to number of stages, whereas the Monte-Carlo analysis has exponential run time. In this approach, no expensive Monte-Carlo simulations are required during timing closure. Our approach does not assume delay PDF to be Gaussian and can handle the case where delay is highly non-linear function of random variables with non-Gaussian PDF. The concept of operating point greatly simplifies computations despite non-linearities without sacrificing accuracy. Furthermore, this approach could be extended for optimizing the designs to reduce the stochastic delays.

The NLOPALV approach has proved very useful for performing cell characterization as well as timing closure. Future publications will cover:

1. Details of NLOPALV theory.
2. Cell characterization using NLOPALV.
3. MAX operation for convergent paths.
4. Application of NLOPALV to timing closure of a complete chip and run-time analysis.

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