A Digitally-Assisted Sensor Interface for Biomedical Applications

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Abstract

A compact, low-power, digitally-assisted sensor interface for biomedical applications is presented. It exploits oversampling and digital design to reduce system area and power, while making the system more robust to interferers. Anti-aliasing is achieved using a charge-sampling filter with a *sinc* frequency response and programmable gain. A mixed-signal feedback loop creates a sharp, programmable notch for interference cancelation. A prototype was implemented in 0.18 μm CMOS and the on-chip blocks consume a total of 255 nW – 2.5 μW from a 1.5 V supply depending on noise and bandwidth requirements.

Introduction

Electrocardiograms (ECG), electroencephalograms (EEG), and electromyograms (EMG) are common bio-potential signals measured non-invasively. Neural field potentials, in contrast, are measured using medical implants [1, 2]. In most cases, an analog front-end (AFE) comprising an instrumentation amplifier (IAMP) and an anti-aliasing filter is used to process these signals. They can be as small as a few μV's and typically reside somewhere between 1 Hz to 1 kHz.

Minimizing power consumption in implants is critical since batteries must be small and last 5–10 years. This is particularly important for applications that use multi-electrode arrays with tens or hundreds of sensors, such as brain-machine interfaces. Since the electrode pitch can be as small as 400 μm, each AFE must also be very small [1]. For non-invasive devices that use hundreds of sensors, such as modern EEG systems, there is a financial incentive to minimize area and power, particularly if consumer products are targeted.

There are four main types of aggressors that corrupt bio-potential signals: electrode DC offset (EDO), IAMP flicker noise, IAMP thermal noise, and 50/60 Hz power line interference (PLI). AFEs presented in recent literature achieve very low thermal noise and minimize the effects of EDO while consuming minimal power [1, 2]. Further, the effects of flicker noise are minimized in [2] by using chopping. Most AFE implementations try to mitigate the effects of common-mode PLI by using an IAMP with a high input impedance. This is often insufficient, however, since some PLI is converted to differential-mode interference as displacement currents flow through finite impedances in the body [3].

System Architecture

We propose the architecture shown in Fig. 1 for canceling interference in an area efficient way. It exploits oversampling to reduce the size of the anti-aliasing filter and mixed-signal feedback to create a sharp, programmable notch. By using feedback, interferers are eliminated at the front end, relaxing the dynamic range requirements of the forward path components and enabling the use of a lower supply voltage. The motivation for exploiting oversampling arises from recent advances in ADC design that have led to ultra-low energy/conversion-step figures of merit [4]. This enables the use of oversampling without a significant power penalty. Using the 4.4 fJ/step FOM cited in [4], an 8-bit ADC sampling at 10 kS/s would only consume 11 nW; at least an order of magnitude less than a typical IAMP. For a bio-potential signal with a 100 Hz bandwidth, the oversampling ratio (OSR) of 50 results in a dynamic range of more than 65 dB which is better than typically required (DR = 1.76 dB + 6.02 dB × ENOB + 10log(OSR)).

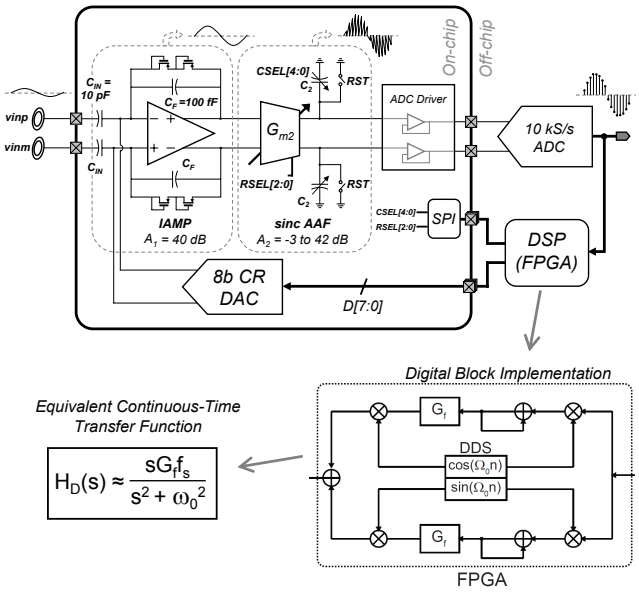

Fig. 1. System architecture including: on-chip instrumentation amplifier, charge-sampling sinc filter, and charge redistribution feedback DAC; and off-chip ADC and digital signal processor.

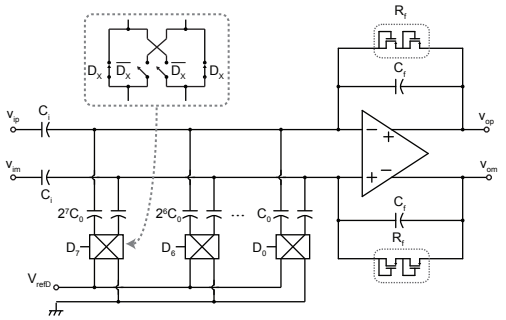

Fig. 2. Combined IAMP and charge redistribution feedback DAC.

The IAMP in Fig. 1 is similar to [1], but fully differential to reduce the supply voltage requirements. A charge-sampling anti-aliasing filter with a *sinc* frequency response is used to accurately place notches at the aliasing frequencies while providing programmable gain [5]. Its transconductor's output current is integrated onto capacitors C_2 for period T_s, and at the end of each period, the resulting voltage is digitized by the ADC. The capacitors are then reset using the switches labeled *RST* and a new cycle begins. The resulting *charge sampling* yields a *sinc* frequency response with notches at integer multiples of $f_s = 1/T_s$. Since these are precisely the frequencies that would be aliased onto the discrete-time baseband, the filter inherently provides anti-aliasing. The transconductor is similar to [6]. The filter's gain is $A_2 = 2G_{m2}T_s/C_2$ and is digitally configured using switched resistors and capacitors.

Mixed-Signal Feedback Loop

The mixed-signal feedback loop used to cancel out PLI includes a forward path comprising: the IAMP, filter, ADC

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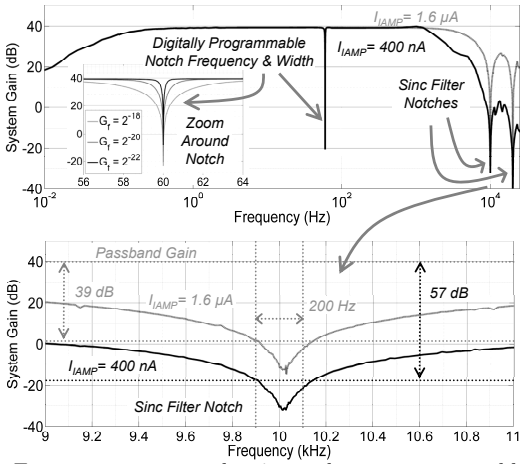

Fig. 3. Frequency response showing a sharp, programmable notch for interference cancelation and sinc filter notches for anti-aliasing.

driver, and ADC; and a feedback path comprising a digital block implemented on an FPGA and an 8-bit charge-redistribution DAC. The DAC, shown in Fig. 2, shares the IAMP's opamp, and therefore consumes only incremental fCV^2 power that is very small. The digital block uses a 32-bit direct digital synthesizer (DDS) to create digital sine and cosine signals with discrete-time frequency Ω_0. The notch frequency of the closed-loop system is $\omega_0 = f_s\Omega_0$ and can be set to any value between zero and $f_s/2$ with steps as small as 3 μHz (for f_s = 10 kHz). The equivalent continuous-time transfer function of the ADC, digital block, and DAC combination, $H_D(s)$, is shown on the bottom left of Fig. 1. It has the form of an integrator, up-converted to ω_0. The closed-loop response, therefore, has two sharp notches at $\pm\omega_0$. The notch width is set by G_f and is also programmable using a digital register. Values of G_f between 2^{-22} and 2^{-18} can be used to select notch widths between 0.5 Hz and 8 Hz, respectively.

The system architecture in Fig. 1 is conceptually similar to [7], but by implementing the integrator digitally, the area and power are reduced many orders of magnitude. In [7], 10 MΩ resistors and 100 μF capacitors are used to create the long time constants necessary to achieve a sharp notch frequency. Our implementation achieves the required long time constants using digital registers that are area and power efficient.

Measurements and Conclusion

The top plot in Fig. 3 shows the full frequency response of the system. The IAMP has a 120 mHz high pass corner frequency to filter out EDO. The gray trace shows the frequency response when the IAMP is biased with 1.6 μA of current. This relatively high bias current extends the closed-loop bandwidth of the opamp beyond 25 kHz such that the filter dominates the magnitude response. The *sinc* response notches are clearly seen at 10 kHz and 20 kHz. For a lower bias setting of 400 nA, the IAMP provides some additional low-pass filtering. The bottom plot in Fig. 3 zooms in to the notch at 10 kHz and shows that the filter provides more than 39 dB of anti-aliasing over 200 Hz of bandwidth and the IAMP provides an additional 18 dB when its bias current is set to 400 nA. The plot insert in Fig. 3 zooms in to the digitally programmable notch which was set to 60 Hz for this measurement. As shown, its bandwidth can be digitally set via G_f.

Depending on the thermal noise requirements, the IAMP bias current can be set anywhere between 100 nA and 1.6 μA. The filter's bias current is typically set to 50 nA. Since a 1.5 V supply was used, the combined power consumption of these two blocks is typically between 225 nW and 2.5 μW. The

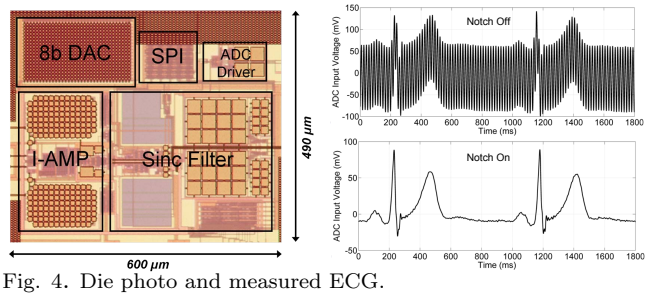

Fig. 4. Die photo and measured ECG.

feedback DAC consumes less than 30 nW.

Fig. 4 shows a die photograph of the chip and an ECG measurement performed with our system with and without using the notch. The combined area of the IAMP, DAC and filter is less than 0.225 mm^2. The filter was made significantly larger than is necessary to allow for maximum flexibility. For f_s = 10 kHz, its gain, which is inversely proportional R_s and C_2, can be tuned from -3 dB to 42 dB. For typical applications where the minimum gain can be set to 10 dB or more, the size of the filter can be reduced considerably.

For the ECG measurement, the input impedance of the IAMP was artificially degraded to exacerbate the effect of PLI and emulate a worst case scenario. As shown in the figure, when the notch filter is turned on, the 60Hz interference is completely eliminated.

	This Work	[1]	[2]	[7]
V_{supply}	1.5 V	±2.5 V	1.8 V	±5 V
I_{supply}	370 nA*	180 nA	1 μA	Not Avail.
P_{supply}	555 nW*	900 nW	1.8 μW	Not Avail.
Passband	0.12–100 Hz*	0.01–30 Hz	0.05–180 Hz	0.05–150 Hz
Noise	3.4 μV_{rms}*	1.6 μV_{rms}	1.0 μV_{rms}	Not Avail.
Gain	37–82 dB	39.8 dB	41, 50.5 dB	55 dB
Filter	*sinc*	N/A	2-pole LPF	Discrete
Notch	Mixed-Sig.	N/A	N/A	Analog
Area	0.225 mm^2	0.220 mm^2	1.7 mm^2	N/A

* Typical setting. Reconfigurable.

TABLE I. Comparison with recent publications.

In conclusion, we present a fully differential biomedical sensor interface with a low-power IAMP, *sinc* anti-aliasing filter, and mixed-signal feedback for interference cancelation. The novel use of charge-sampling for anti-aliasing yields the added benefit of 45 dB of gain programmability without consuming excessive area. The digital implementation of the feedback path in the interference cancelation loop yields a flexible, area-efficient solution. Finally, by canceling interferers at the front end of the system, the dynamic range requirements of the forward path blocks are relaxed.

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