Ultra-Low-Power UWB for Sensor Network Applications

Patrick P. Mercier*, Denis C. Daly*, Manish Bhardwaj*, David D. Wentzloff†,
Fred S. Lee‡, and Anantha P. Chandrakasan*
*Massachusetts Institute of Technology, Cambridge, MA, 01239, USA
†University of Michigan, Ann Arbor, MI, 48109, USA
‡Rambus Inc., Los Altos, CA, 94022, USA

***Abstract*— Long distance, low data-rate UWB communication for sensor network applications requires a highly energy efficient transceiver combined with circuit and system-level optimizations to maximize range. A custom pulsed-UWB transceiver chipset in 90nm CMOS is presented that targets these aggressive specifications. The transceiver efficiently communicates at data rates from 0-to-16.7Mbps in three 550MHz-wide channels in the 3.1 to 5GHz band by using pulse position modulation (PPM). The transmitter uses an all-digital architecture and calibration technique to synthesize pulses with programmable width and center frequency. The non-coherent receiver operates at 0.65V and performs channel selection filtering, energy detection, and bit-slicing. As FCC regulations limit the maximum transmit power of UWB communication, a run-length limiting technique is presented to reduce energy requirements when maximizing range at low data rates.**

I. Introduction

Wireless microsensor networks, which consist of a group of sensor nodes that are deployed remotely and used to relay sensing data to the end-user, are highly energy constrained systems. This energy constraint necessitates the realization of a highly energy efficient wireless transceiver, as the radio often dominates the power budget of a microsensor node. Pulsed ultra-wideband (UWB) communication is an active field of research and offers much promise for meeting this stringent constraint while simultaneous allowing for a highly integrated, high performance implementation.

Due to the wide signal bandwidths associated with UWB pulses compared to the relatively low data rates required by microsensor nodes, UWB radios are uniquely positioned to exploit the available bandwidth by trading off spectral precision and efficiency for other system specifications such as energy/bit and power consumption. For example, non-coherent signaling combined with relaxed frequency tolerances allows both transmitter and receiver to significantly reduce power consumption at the cost of a slight degradation in link margin [1], [2].

This paper presents a custom pulsed-UWB chipset implemented in 90nm CMOS that achieves high performance and energy efficient operation at data rates from 0-to-16.7Mbps. The chipset includes features to reduce power consumption such as an all-digital transmitter architecture, low-voltage RF and analog circuits in the receiver, and no RF local oscillators allowing the chipset to power on in 2ns for duty-cycled operation. The architecture and design of the custom chipset is described in Section II. To increase the range of the chipset, the transmitter must be able to support bursts of back-to-back pulses. Section III presents a suitable architecture for generating these pulse bursts and introduces a modulation technique to decrease the peak power while maximizing communication distance under receiver energy constraints.

II. Custom Low-Power UWB Chipset

The architecture of the transceiver chipset presented in this paper is shown in Fig. 1 [3]. Binary pulse-position modulation (PPM) is used to encode the transmitted data, where a 2ns wide UWB pulse can arrive in one of two 30ns adjacent time slots per symbol. The data rate is scaled by changing the time period between bit symbols. The PPM symbol is transmitted in one of three 550MHz channels in the 3.1 to 5GHz band. Three channels are used to avoid potential in-band interferers and to add frequency diversity for multiple users.

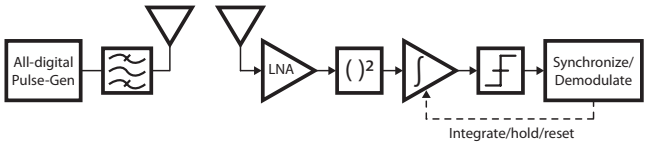

Fig. 1. Custom pulsed-UWB chipset architecture.

A. All-Digital Transmitter

A block diagram of the proposed transmitter is shown in Fig. 2 [4]. The transmitter consists of a programmable delay line, an edge combiner, and a pad driver. The use of highly digital architectures realized in deep submicron CMOS processes allows for significant savings in energy while also requiring minimal die area [5], [6], [7], [8]. All of the proposed transmitter circuits are fully digital, and thus no analog bias currents are required and power is only consumed through digital switching events (CV^2) and subthreshold leakage current. This architecture is made practical by relaxing frequency tolerances through the use of a wide bandwidth non-coherent receiver.

The transmitter generates a pulse at each rising edge of the *start pulse* input. This edge propagates through a 32-stage delay line with an 8-bit digitally controlled delay. UWB pulses

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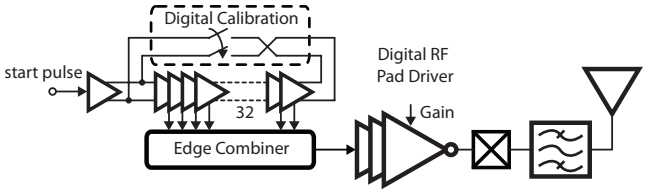


Fig. 2. Transmitter block diagram.

are generated by selectively combining the equally-delayed edges to form a single RF pulse. The center frequency and bandwidth of the pulse are adjusted by controlling the delay of each stage as well as which output edges to combine. By making both the delay and number of combined edges programmable, the pulse spectrum may be controlled with 6000ppm accuracy without requiring an RF local oscillator.

The generated pulse is buffered by a digital pad driver, which requires no static bias currents and achieves high energy efficiency. To meet the FCC spectral mask, the pad driver output is filtered by an off-chip UWB band-select filter that directly drives a 50Ω antenna. As subthreshold leakage currents can significantly degrade energy efficiency at low data rates, a standby mode is implemented in the pad driver to reduce leakage during the interval between packets.

B. Receiver

Fig. 3 shows a simplified block diagram of the non-coherent receiver. It is comprised of a 3-5GHz subbanded RF frontend, a passive self-mixer, and a low power mixed-signal baseband [9]. No RF PLL or oscillator is required; only a 33MHz crystal is needed to operate the mixed-signal baseband. Channel selection is performed in the RF front-end for out-of-band noise/interference robustness. The RF and mixed-signal baseband operate at 0.65V and 0.5V, respectively, for low power operation. The receiver is designed so that it can disable all bias currents during the time between symbols, thereby exploiting the duty-cycling inherent in pulsed-UWB low data rate signaling.

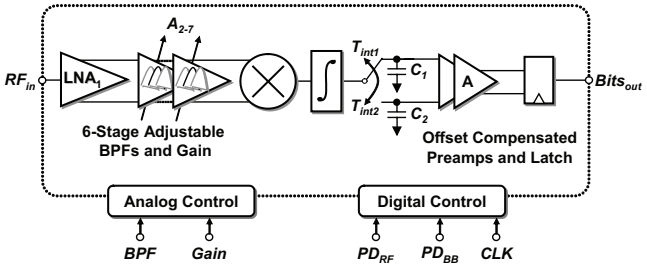


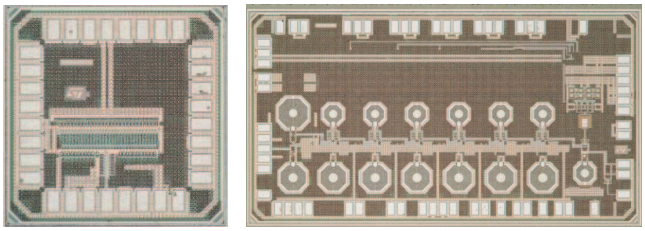
Fig. 3. Receiver block diagram.

The non-coherent receiver uses a mixed-signal relative compare baseband to determine the transmit bit by measuring and comparing the energy received in two adjacent integration periods. For bit-slicing, a sample-and-hold capacitor network stores analog integration results during T_{int1} and T_{int2} onto separate capacitors C_1 and C_2, respectively. Thereafter, two cascaded offset-compensated preamplifiers and a latch perform a relative-compare on the two capacitor voltages to evaluate the received bit. This scheme inherently performs pre-integrator signal-path normalization in each bit decision.

C. Experimental Results

The transmitter and receiver were fabricated in 90nm CMOS, and die photos are shown in Fig. 4. Measured transmitter RF spectra of all three channels are superimposed over the FCC spectral mask in Fig. 5. The standby power consumption due to subthreshold leakage current is 96μW. The power consumption while generating pulses at a data rate of 16.7Mbps is 718μW, corresponding to an energy efficiency of 43pJ/pulse. The resulting energy/pulse across a range of data rates is compared to previously published works in Fig. 7(a).

The receiver RF front-end provides 40dB of gain and high-order roll-off for channel selectivity in each of the 3 bands, as shown in Fig. 6. A noise figure of 8.5-9.5dB is achieved, and better than -10dB S11 is achieved for all three bands. The worst-case measured input P1dB is -45dBm. At 100kb/s, the receiver achieves -99dBm sensitivity at a BER of 10^{-3}. Due to the fast turn-on and turn-off time, the receiver achieves 2.5nJ/bit across three orders of magnitude in data rate, as shown in Fig. 7(b).



(a) TX area: 0.2x0.4mm^2 (b) RX area: 1x2.2mm^2

Fig. 4. Custom pulsed-UWB chipset die photographs (not to scale).

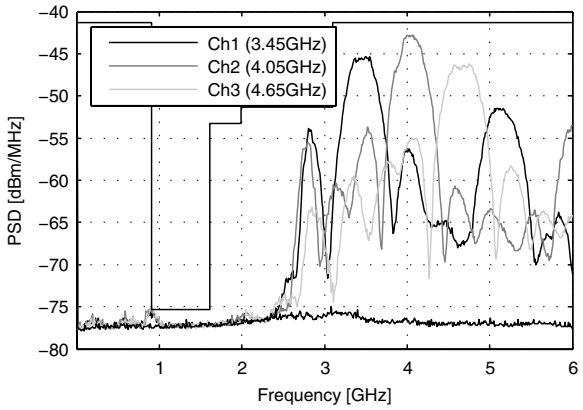


Fig. 5. Measured transmitter power spectral densities of all three channels superimposed over the FCC spectral mask.

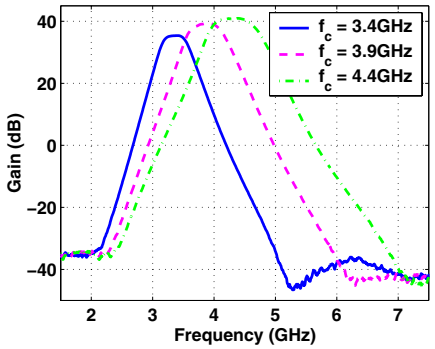
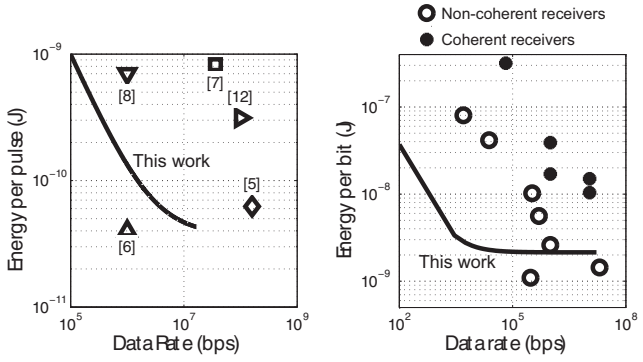


Fig. 6. Receiver front-end gain measurements.



(a) Transmitter (b) Receiver

Fig. 7. Transmitter energy/pulse and receiver energy/bit compared to previously published works (see [9] for receiver reference points).

III. Extending Communication Distance for Low Data Rate Systems

A. Physical Limits

Communication distance in a non-coherent energy-detecting UWB system is maximized when the SNR seen at the receiver during the integration period is maximized. This occurs when the transmitter generates maximum total output power under regulatory limits. Since sensor networks typically communicate at low data rates, large amplitude pulses transmitted at the data rate are required to maximize power under FCC spectral masks. For example, a peak-to-peak voltage swing of 19.3V is required to maximally satisfy FCC spectral masks at a PRF of 10kHz. This is clearly impractical in deep sub-micron CMOS where supply voltages are on the order of 1V.

An alternative approach to generating large-swing pulses while maximizing total power under FCC masks is to reduce output voltage swings and increase the PRF (i.e. multiple pulses transmitted per bit). The presented chipset can support this approach, however, the number of receiver integration periods increases directly with the number of pulse repetitions. Since receiver costs dominate the system energy budget, this is highly undesirable for energy-constrained sensor networks. Instead, a modified transmitter architecture supporting *bursts* of multiple back-to-back pulses can be used, as shown in Fig. 8. Bursts can be transmitted at the *burst repetition frequency* (BRF) while maintaining constant total power (i.e. the effective PRF remains the same). With an integration window of 30ns, the proposed receiver is capable of integrating up to fifteen 2ns pulses without suffering any energy/bit overhead. The IEEE 802.15.4a standardization committee incorporates pulse bursting into the UWB PHY [10]. Illustrative transient waveforms are shown in Fig. 8.

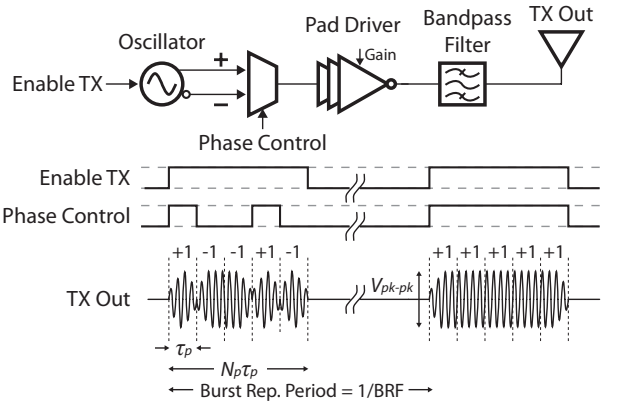


Fig. 8. Transmitter architecture incorporating pulse bursting techniques. N_p is the number of pulses per burst and $\text{PRF}_{avg} = N_p\text{BRF}$.

B. Regulatory Limits

The FCC limits output power in the 3.1-to-10.6GHz UWB band in two ways [11]:

1) The *average* power spectral density (PSD) must be less than or equal to -41.3dBm. This corresponds to a theoretical maximum total power of -13.9dBm for a 550MHz bandwidth signal. In practice this number is reduced by 2-4dB via pulse generation constraints.
2) The *peak* power may not exceed 0dBm at the UWB signal's center frequency in a 50MHz resolution bandwidth (RBW). Since most spectrum analyzers are not equipped with a 50MHz IF filter, the peak power measurement is typically performed at a lower RBW and the limit is conservatively set to be $P_{pk} \leq 20log_{10}(\text{RBW/50MHz})$.

High data rate pulsed-UWB transmitters are typically average power limited, while low data rate transmitters are typically peak power limited [12]. Sensor networks, which often operate at low data rates, can thus forsake a considerable amount of total power in order to remain peak power compliant. In other words, the peak-to-average power ratio (PAPR) of low pulse rate transmitters is generally large and thus violates the FCC peak power limit well before the average power limit.

Since the average power of low-BRF transmitters has a $10log()$ dependence on BRF while the peak power does not depend on BRF [13], the PAPR can be reduced by decreasing the peak-to-peak voltage swing and increasing the BRF. This increases the number of receiver integrations required per bit as a trade-off for enhanced communication distance.

An additional method to reduce PAPR is by introducing run-length limits (RLLs) in the transmitter phase modulator to prohibit long bursts of pulses with no phase inversions. For

example, an LFSR-based scrambler may output a run of 8 '+1' phase bits at some point in its sequence. An RLL of 3 would ensure that the fourth and eighth phase bits are inverted, as illustrated in Fig. 9. This technique spreads peak power away from the carrier frequency while leaving the average PSD undisturbed for reasonable RLLs. However, small-valued RLLs (such as run-length limits of 3 when a burst contains 15 pulses) can distort the average PSD by spreading a significant amount of energy away from the carrier frequency.

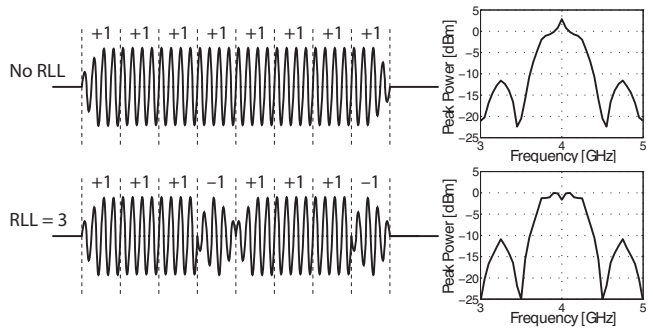


Fig. 9. Example of run-length limiting. The simulated peak peak PSDs emulate the results of a spectrum analyzer operating in peak-hold mode.

Fig. 10 illustrates the reduction of peak power by decreasing voltage swings, increasing BRF, and applying run-length limiting. The maximum average PSD is fixed at -41.3dBm/MHz across all voltages and BRFs. In the case for a data rate of 10kbps, the communication distance is maximized under FCC constraints without RLL at V_{pk-pk} = 0.26V and BRF = 3.3MHz. Sixteen pulses are generated per burst and 330 burst-repetitions are required per bit. Applying an RLL of 4 reduces peak power by 3dB, giving V_{pk-pk} = 0.37V, BRF = 1.7MHz, and 170 burst-repetitions per bit. This represents a 1.9x improvement in receiver energy efficiency.

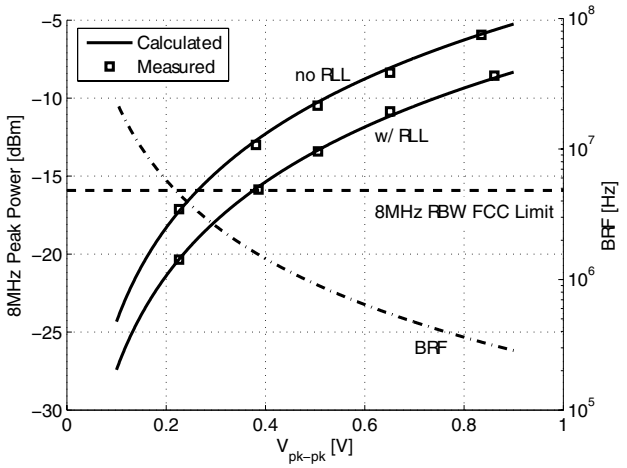


Fig. 10. Peak power versus V_{pk-pk} with $P_{avg} = -41.3$dBm/MHz fixed. Here, R_{nom} = 10kbps, RBW = 8MHz, τ_p = 2ns, N_p = 16, and RLL = 4 (when used). Measured results are from a custom pulse generator.

IV. Conclusion

Non coherent pulsed-UWB systems are proposed for use in energy-constrained sensor network applications due to their relaxed frequency tolerances, wide available bandwidth and inherently duty-cycled nature. The transmitter and receiver presented in this paper consume 43pJ/pulse and 2.5nJ/bit respectively at data rates up to 16.7Mbps. To extend range under FCC peak and average power constraints, a run-length limiting technique is introduced which spreads peak power away from the carrier frequency when bursting multiple pulses sequentially. This technique reduces peak power by up to 3dB, thereby increasing low data-rate receiver energy efficiency by up to 1.9x while maximizing communication distance.

Acknowledgments

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