30.8 A 6b 0.2-to-0.9V Highly Digital Flash ADC with Comparator Redundancy

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Microsensor wireless networks and implanted biomedical devices have emerged as exciting new application domains. These applications are highly energy constrained and require flexible, integrated, energy-efficient ADC modules that can ideally operate at the same supply voltage as digital circuits. In many applications, the performance requirements are quite modest (100s kS/s). This paper presents a highly digital ADC architecture compatible with advanced CMOS processes, capable of operating down to a supply voltage of 200mV (i.e., subthreshold regime) and up to 900mV. However, leakage and device variation must be addressed, particularly at low supply voltages.

Figure 30.8.1 shows a block diagram of the ADC. The highly digital flash ADC has no bias currents and thus energy is only dissipated through switching events (CV^2) and by leakage currents. By minimizing the use of analog circuits, the architecture is compatible with digital CMOS processes. As true differential architectures are not amenable to low-voltage integration, the ADC attempts to mimic the advantages of differential circuits through digital signal processing. The ADC can be configured in either a single-ended or pseudo-differential configuration. It consists of a sampling network, two arrays of 127 dynamic digital comparators and a digital backend. Instead of a traditional reference ladder that draws static current, the ADC uses dynamic comparators with static voltage offsets to generate comparator thresholds. As these thresholds vary die-to-die and with supply voltage, redundancy is exploited to improve linearity [1]. The ADC is calibrated with an off-chip ramp and an estimate of the cumulative distribution function (CDF) of comparator thresholds is generated in on-chip memory. This data is then processed off-chip to determine which subset of the 254 comparators to enable.

The digital dynamic comparators are based on a sense-amplifier flip-flop and their schematic is shown in Fig. 30.8.2. For flash ADCs, comparator offsets must be compensated for, either in the analog or the digital domain. As it is difficult to realize analog offset compensation at voltages below 500mV, the ADC architecture leverages digital calibration combined with redundancy. Many redundant digital regenerative comparators with large offsets are used in place of a small number of precise comparators and reference voltages. Comparator thresholds are varied by placing minimum sized PMOS input devices in parallel and series. By using a single device of minimum size rather than varying its width or length, the comparator thresholds can be estimated by only characterizing a single device. Stacking devices in series is preferred to linear width scaling as the device strength decreases quadratically in proportion to the number of stacked devices in series. This allows for a smaller implementation and consumes less power than setting comparator thresholds by scaling device widths or by adding capacitors at the drain or source nodes of transistors M1 and M3 [2].

At low supply voltages, the degraded ratio of 'on' conductance to 'off' current of the sampling switch can limit dynamic performance of the ADC. To increase the 'on' conductance, voltage boosting is used as shown in Fig. 30.8.3. Two methods employed to reduce the 'off' current are stacking 2 NMOS sampling switches in series and using a feedback amplifier to set the middle node of the stacked sampling switch. The feedback amplifier consists of self-biased NMOS and PMOS source followers and consumes only leakage current. The transient plot in Fig. 30.8.3 shows how these three techniques reduce the leakage on the sampling capacitor when the sampling switch is open.

As differential analog circuits cannot be easily realized in standard CMOS processes at voltages below 0.5V, the ADC processes the differential analog input with a single-ended analog architecture and moves differential signal processing to the digital domain [3]. When the ADC is configured in pseudo-differential mode, the outputs of the two single-ended ADCs are subtracted digitally. To increase the common-mode voltage range and decrease clipping, common-mode rejection is implemented digitally via a programmable PID IIR filter driving a 5b capacitive DAC. The two single-ended ADC outputs are averaged and compared to the desired mid-scale code. To raise or lower the input common-mode, an extra clock phase is enabled for the capacitive feedback DAC. When a full-scale input sinusoid is in the presence of a -12dBFS common-mode signal at $0.005F_S$, the ENOB degrades by 0.5b compared to a 1.3b degradation when the common-mode rejection is disabled.

The 127b thermometer output of each comparator array must be decoded to a 7b binary value to generate the digital output code. The decoder is realized with a Wallace tree adder, that allows any combination of comparators to be enabled and guarantees ADC monotonicity. Comparators are not assigned to any specific code and can be reassigned arbitrarily. The Wallace tree adder implements an energy efficient decoder; however, it is not suitable for generating an estimated CDF as it breaks the link between comparators and their associated thresholds. To generate the estimated CDF, the comparator outputs are directly fed in parallel into a 127×9b memory. 9b of memory are associated with each comparator to allow sufficient threshold accuracy. Each block of memory has an associated counter that is used for CDF generation. The memory is realized with CMOS latches to enable operation down to 0.2V and operates off an independent power supply so that it can be power gated when calibration is complete.

The comparators have a measured offset standard-deviation of 8.1mV at a 200mV supply and 7.1mV at a 400mV supply, respectively. Figure 30.8.4 presents statistical measurements of the ENOB for the ADC, before and after redundancy calibration. In pseudo-differential mode with a total of 126 comparators enabled, the ADC nominally achieves an average ENOB of 5.56 at 400kS/s. If redundancy calibration is not used, the average ENOB reduces to 3.84. The comparator thresholds vary with temperature and ADC recalibration is required to maintain linearity. In single-ended 6b mode, the ADC ENOB degrades from 5.05 at 25°C to 4.28 at 75°C without recalibration. After recalibration the ENOB returns to 5.08.

The ADC is fabricated in a 0.18μm 5M2P CMOS process and occupies 2mm² (Fig. 30.8.7). It operates from 2kS/s at 0.2V to 17.5MS/s at 0.9V, as shown in Fig. 30.8.5. Also shown in Fig. 30.8.5 is the FOM of the ADC in single-ended mode versus supply voltage. At low voltages, the leakage current degrades the FOM due to low sampling rates, whereas at high voltages, CV^2 losses degrade the FOM, leading to the emergence of a minimum FOM supply voltage of 0.4V [4]. At this voltage, the ADC achieves a FOM of 125fJ/conversion-step in single-ended mode (5.05 ENOB) and 150fJ/conversion-step in pseudo-differential mode (5.56 ENOB). The measured DNL and INL are +1.23/-0.91LSB and +0.72/-0.90LSB, respectively (Fig. 30.8.6). The total power consumption of the ADC at 0.4V, 400kS/s is 2.84μW and 1.66μW in pseudo-differential and single-ended mode, respectively, of which 135nW is leakage power.

References:
[1] M. P. Flynn, C. Donovan, and L. Sattler, "Digital Calibration Incorporating Redundancy of Flash ADCs," *IEEE Trans. Circuits & Systems II*, vol. 50, no. 5, pp. 205-213, May, 2003.
[2] G. Van der Plas, S. Decoutere, and S. Donnay, "A 0.16pJ/conversion-step 2.5mW 1.25GS/s 4b ADC in a 90nm digital CMOS process," *ISSCC Dig. Tech. Papers*, pp. 566–567, Feb., 2006.
[3] K. Pun, S. Chatterjee, and P. Kinget, "A 0.5V 74dB SNDR 25kHz CT ΔΣ Modulator with Return-to-Open DAC," *ISSCC Dig. Tech. Papers*, pp. 181-182, Feb., 2006.
[4] A. Wang and A. P. Chandrakasan, "A 180-mV Subthreshold FFT Processor Using a Minimum Energy Design Methodology," *IEEE J. Solid-State Circuits,* vol. 40, no. 1, pp. 310-319, Jan., 2005.
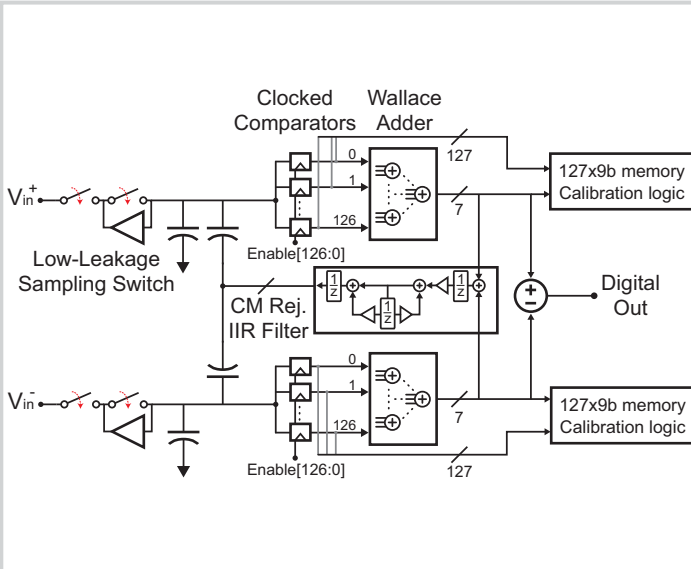
Figure 30.8.1: Block diagram of the flash ADC.

Figure 30.8.2: Comparator schematic. The comparator consists of K stacked devices, each of which is N_i minimum-sized PMOS devices in parallel.

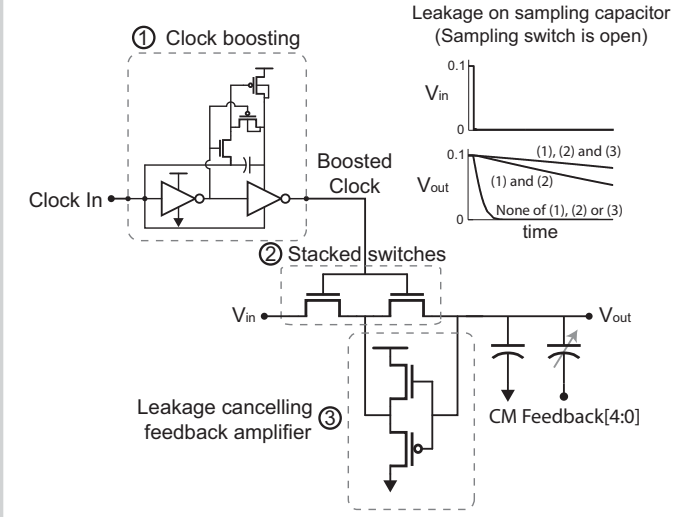Comparator Threshold = $f(K, N_1, N_2, N_3, ..., N_K)$

Figure 30.8.3: Sampling network schematic highlighting the 3 methods implemented to improve performance. The transient leakage plot is normalized for equal 'on' conductance.
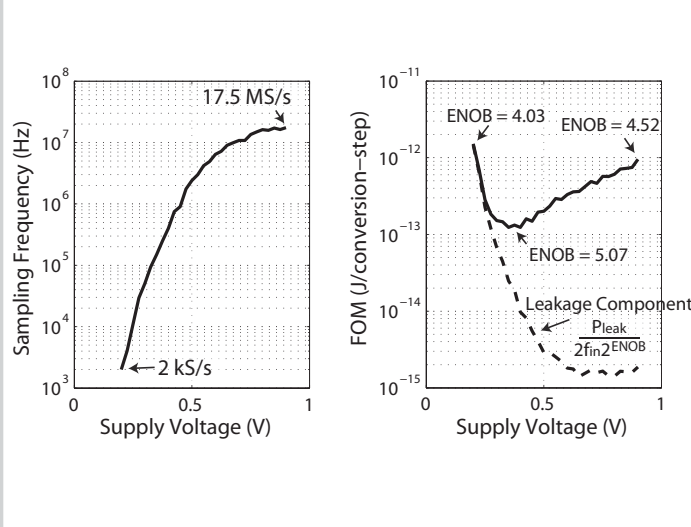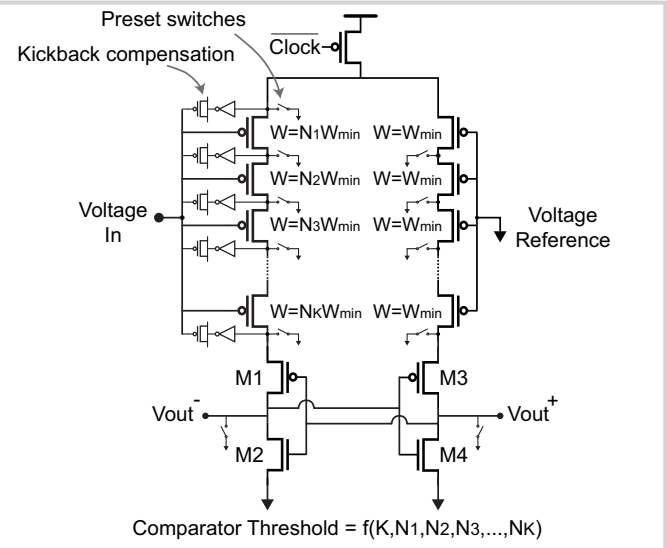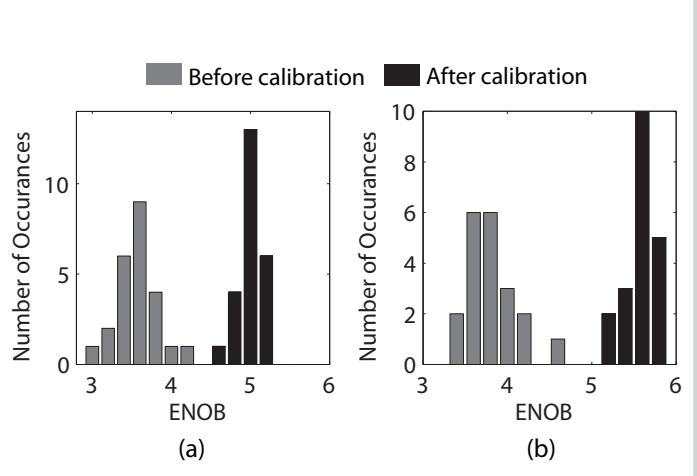
Figure 30.8.4: Statistical variation of ENOB in (a) single-ended and (b) pseudo-differential mode at V_{DD}=0.4V before and after calibration.
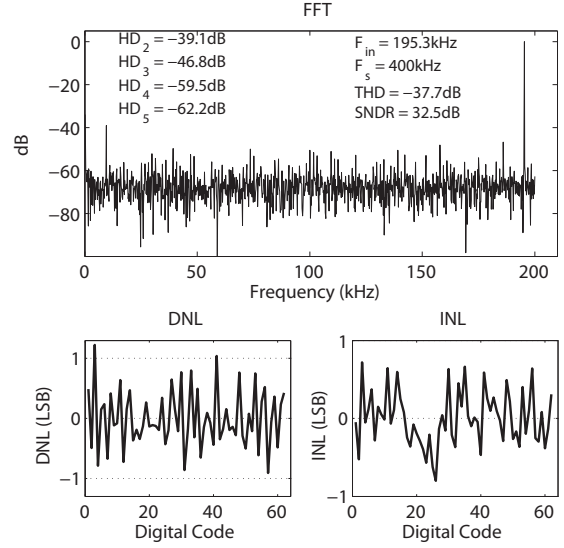
Figure 30.8.5: Maximum sampling frequency and FOM versus supply voltage, indicating presence of minimum FOM at V_{DD}=0.4V.

Figure 30.8.6: FFT and DNL/INL of ADC in single-ended 6b mode at VDD=0.4V.

$FOM = \dfrac{P_{leak}}{2f_{in}2^{ENOB}}$

$HD_2 = -39.1dB$
$HD_3 = -46.8dB$
$HD_4 = -59.5dB$
$HD_5 = -62.2dB$
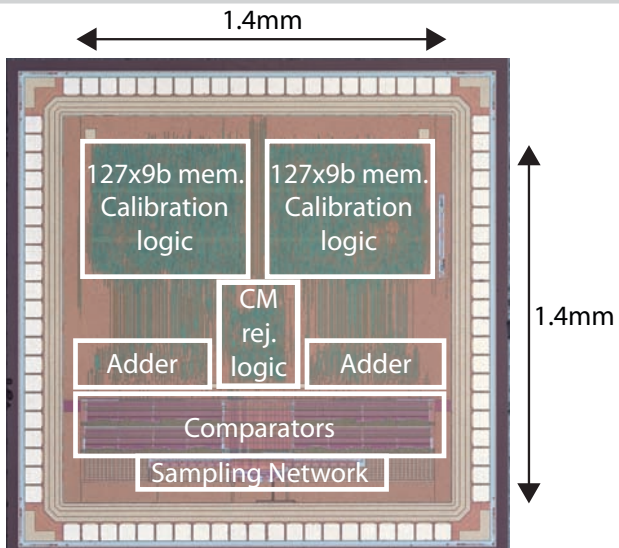$F_{in} = 195.3kHz$
$F_s = 400kHz$
$THD = -37.7dB$
$SNDR = 32.5dB$

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Figure 30.8.7: Die micrograph of the ADC in 0.18µm CMOS.