12.2 Highly Interleaved 5b 250MS/s ADC with Redundant Channels in 65nm CMOS

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Time-interleaving is a well established technique that has led to the highest combination of resolution and speed in pipelined ADCs [1,2] and has made the sampling rate of SAR ADCs competitive with flash ADCs [3,4], but several challenges exist. As every sample must be accurate, performance is limited by the worst channel; thus, local variation degrades yield. Timing skew between channels introduces distortion and is difficult to correct digitally. Finally, clock distribution is a significant overhead.

The 250MS/s ADC has 36 time-interleaved 5b SAR ADC channels operating at 800mV. Parallelism is used specifically to improve energy efficiency, and architectural solutions address the limitations of interleaving. Redundancy is used as an efficient technique to counteract the yield loss from local variation. A hierarchical top-plate sampling network reduces timing skew with extended sampling times and permits a partitioned clock network for minimum distribution requirements.

The architectural block diagram of the ADC is shown in Fig. 12.2.1. There are three blocks, each of which contains twelve nominal and two redundant channels, along with a clock-generation unit, a sampling network, and an output MUX. A precise clock at the sampling frequency f_S is distributed to the block sampling network and defines all critical sampling instants. All channels within a block share a non-critical $f_S/6$ clock. Half of the channels align to the positive edge of this clock, and half align to the negative edge. This structure reduces clock generation and distribution power.

With increased parallelism and longer available settling times, analog energy decreases as current densities move from strong to moderate inversion for improved transconductance efficiency (g_m/I_D). Also, parallelism allows the supply voltage to be reduced for V_{DD}^2 digital energy savings. These savings are modeled along with overheads of increased parallelism (e.g., clock distribution) in the plot at the top of Fig. 12.2.2. 36 channels are chosen to operate beyond the knee of this curve.

In most ADCs, static performance degradations, such as matching-dominated linearity errors, are primarily limited by local variations. Parallel systems, however, suffer from additional yield loss due to local variation, a problem only exacerbated in deep submicron CMOS. Figure 12.2.2 (bottom) shows the drop in yield (for a fixed capacitor size) as the number of channels increases from 1 to 36. Previous highly interleaved ADCs used extensive calibration to improve channel performance and matching [1]. While successful, additional complexity per channel is required. This ADC uses redundant channels to counteract the yield loss due to parallelism. Unlike the previous use of redundancy in ADCs to relax comparator offset requirements in a flash ADC [5], in this interleaved converter, a smaller number of redundant elements are required and the number of metrics that can be simultaneously improved (e.g., INL, timing skew, offset, SNDR) is increased. Two redundant channels are allocated to each block, and any 12 of the 14 channels within a block can be selected for active operation. For a 95% target yield for the 36 time-interleaved channels, this redundancy implementation reduces the required channel yield from 99.86% to 96%; this benefit can be seen in the 36+6 channels curve in Fig. 12.2.2.

Of the mismatch-related distortions in interleaved converters, gain mismatch has not been significant for SAR ADCs [3,4]. Offset is corrected digitally with an embedded adder per channel. Timing skew, however, is expensive to correct digitally, and the sufficient matching of timing paths across the large number of channels is nearly infeasible. Instead, a hierarchical global sampling network [6] is used, as shown in Fig. 12.2.3. Connected in series to the top-plate of sampling capacitor C_{Si} are a per-channel switch S_{TMi} and a global switch S_G. S_G, aligned to the precise sampling clock, opens first, defining the sampling instant. Unlike the hierarchical bottom-plate switch proposed in [2], placing the global switch on the top-plate reduces the overall switch size because the ground-referenced top-plate switch is smaller than the floating bottom-plate switch; however, skew between the different channels' S_{TMi} switches causes a residual voltage error because of charge sharing between the sampling capacitor C_{Si} and the parasitic capacitance C_{par} [6]. Each block has its own master switch, which reduces the wiring and diffusion capacitance contributing to C_{par} and minimizes the residual timing skew.

The sampling network is extended to allow overlapping sampling periods across channels with minimal crosstalk through the sampling networks. An additional top-plate switch S_{TPi} directly connects the top-plate of the sampling capacitor to ground during a pre-sampling period, avoiding multiple nodes connected to V_{sgnd} concurrently. The bottom plate switch is slowly turned on with a ramp driven to a boosted supply voltage V_{DDS}. When the switch is turned on, the slow ramp reduces the kickback noise by more than 8× compared with a step drive. The resultant crosstalk, when the ADC is driven by a 50Ω source, is sufficiently small that no further effort is made to locate the start of one channel's sampling window away from the critical sampling instant of another channel. The 1.2V sampling voltage V_{DDS} is within the process limits and is used to accurately track high-frequency inputs.

The channel structure is similar to [4], but it is extended with digital offset correction and uses a half-rate clock for driving its internal state machine. The split capacitor array [4] is used, and, to reduce its sensitivity to systematic mismatch, the main and MSB subarrays are swapped between the two differential arrays within a channel.

The 36+6-way interleaved ADC is fabricated in a 65nm CMOS process and occupies a $5mm^2$ die (Fig. 12.2.7). At 250MS/s, the ADC operates at 800mV and consumes a total of 1.20mW, including analog, digital, sampling, clock, and reference-voltage power. The current drawn from the 1.2V sampling voltage is 200µA. The dynamic performance is plotted in Fig. 12.2.4. With a 117MHz input, the ADC achieves an ENOB of 4.42, corresponding to an FOM ($P/2^{ENOB}2f_{in}$) of 240fJ/conversion-step.

Measurements are performed on 24 chips to test channel variation and redundancy. Channel selection is performed off-chip at test time by evaluating all 42 channels for INL, SNDR, THD, offset, and timing skew, and then programming the chip with the best 36 enabled channels. A typical variation across a single chip of 3 of these metrics is shown in Fig. 12.2.5. When the 4 circled channels are replaced by redundant ones, all 3 metrics improve. Figure 12.2.6 shows a histogram of the worst-channel THD on a chip with and without redundancy. By eliminating the worst channels, the distribution is tightened. Redundancy improves the yield of chips that meet all of the specifications for 5b performance from 42% to 88% (Fig. 12.2.6).

Acknowledgments:
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References:
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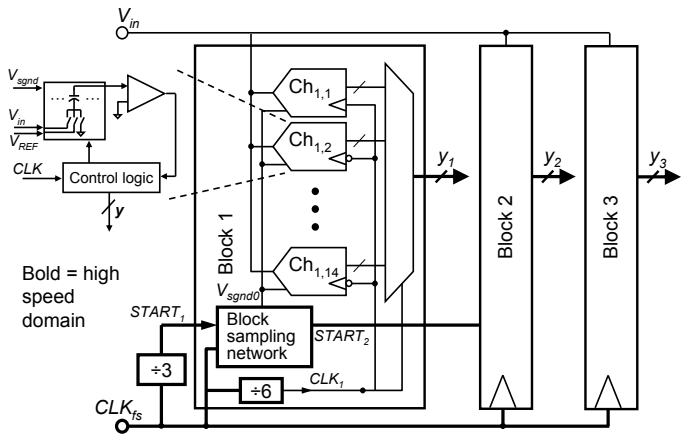


Figure 12.2.1: Architectural block diagram of ADC and (inset) SAR channel.

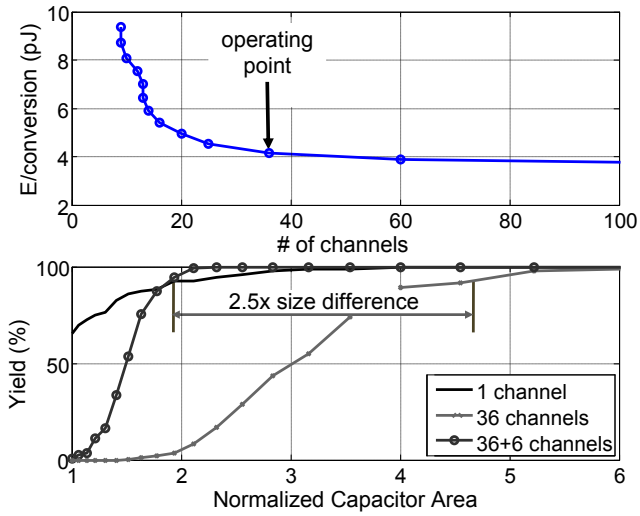


Figure 12.2.2: Modeled energy versus level of parallelism (top), and yield versus capacitor size for interleaved ADC.

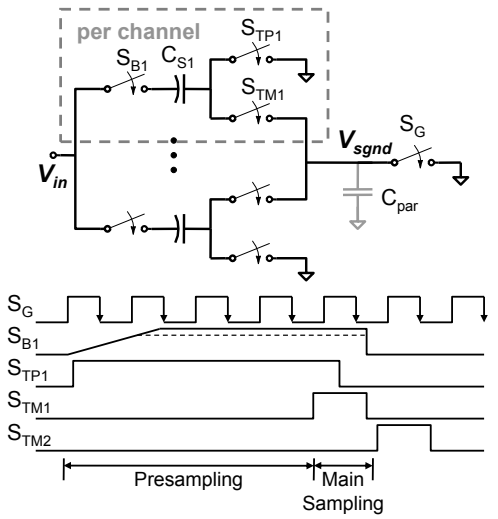


Figure 12.2.3: Hierarchical global top-plate sampling network with overlapped sampling windows.

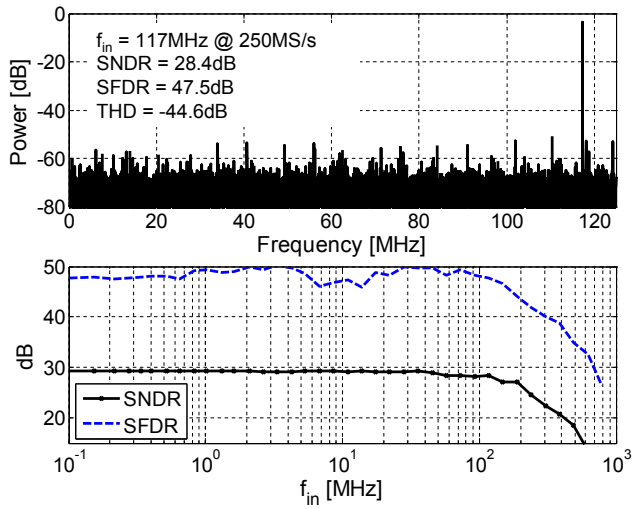


Figure 12.2.4: Measured FFT and dynamic performance.

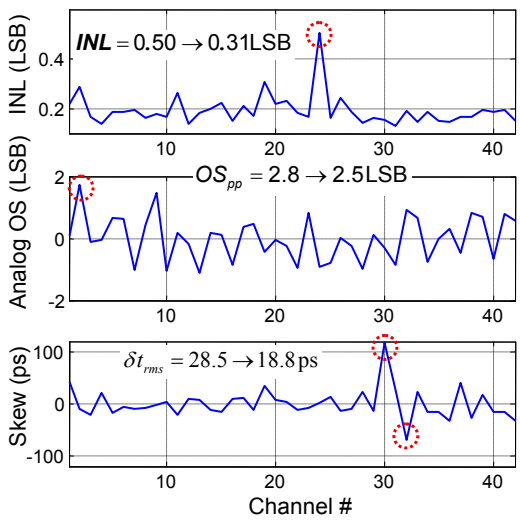
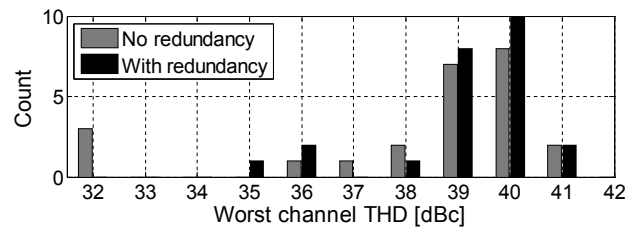


Figure 12.2.5: Measured variation across a single chip and metric improvements after eliminating circled channels.



Metric	Specification (for all channels)	Yielding Chips out of 24	
		No Redundancy	With Redundancy
INL	≤ 0.6LSB	14	21
Offset	≤ 2LSB	19	24
Channel SNDR	≥ 27dB	19	22
THD	≥ 33dB	21	24
t_{skew}	≤ 15ps	24	24
Overall SNDR	≥ 27dB	17	23
All Specifications		10	21

Figure 12.2.6: Histogram showing improvement of THD with redundancy and summary of yield data at 250MS/s.

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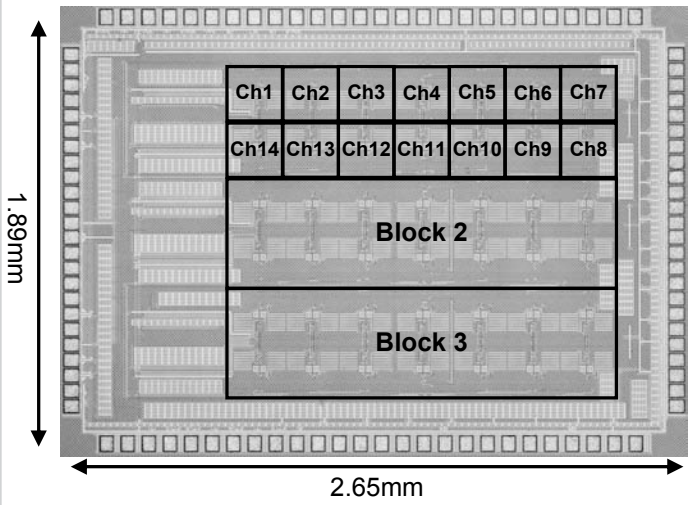

Figure 12.2.7: Die micrograph of 36+6-way interleaved ADC.

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