Voltage Scalable Switched Capacitor DC-DC Converter for Ultra-Low-Power On-Chip Applications

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***Abstract*- This paper presents a voltage scalable switched capacitor (SC) DC-DC converter which employs on-chip charge-transfer capacitors. The DC-DC converter makes use of multiple topologies to achieve scalable voltage generation while minimizing conduction loss and a technique called divide-by-3 switching to minimize the loss due to bottom-plate parasitics. It also uses automatic frequency scaling to reduce switching losses. The converter employs an all digital control which consumes no static power. The voltage scalable SC DC-DC converter with integrated on-chip charge-transfer capacitors was implemented in a 0.18µm CMOS process and achieves above 70% efficiency over a wide range of load powers from 5µW to 1mW, while delivering load voltages from 300mV to 1.1V. The active area consumed by the converter is 0.57mm^2.**

I. Introduction

Minimizing the energy consumption of battery powered systems is a key focus in integrated circuit design. Dynamic voltage scaling (DVS) [1] is a popular method to achieve energy efficiency in systems that have widely variant performance demands. As V_{DD} decreases, transistor drive currents decrease, bringing down the speed of operation of a circuit. A DVS system operates the circuit at just enough voltage to meet performance, thereby achieving overall savings in total power consumed. By introducing the capability of subthreshold operation these same systems can operate at their minimum energy operating voltage [2] in periods of very little activity, leading to further savings in total energy consumed. This way ultra-dynamic voltage scaling (U-DVS) can be achieved. U-DVS systems require a variable voltage supply that can deliver sub-threshold voltages (~300mV) at low load powers (1µW) when idling, and close to the battery voltage (~ 1.1V) at high load powers (1 - 2mW) when performing active operation. Supply voltage dithering, which uses discrete voltage and frequency pairs, was proposed as a solution to achieve U-DVS [1]. However, dithering requires an efficient system controller that can time share between the different voltage levels adding to the overall complexity of the system. This is of specific concern in ultra-low-power applications. Also, voltage dithered systems that achieve U-DVS require at least 2 voltage levels different from the battery voltage to achieve the stated power savings. This increases the number of DC-DC converters to supply these voltage levels.

This paper focuses on a voltage scalable DC-DC converter that can deliver a continuous voltage supply quantized to 10mV. U-DVS systems often require multiple on-chip voltage domains with each domain having specific power requirements. A switched capacitor (SC) DC-DC converter is a good choice for such battery operated systems because it can minimize the number of off-chip components and does not require any inductors. Previous implementations of SC converters have commonly used off-chip charge-transfer capacitors [3] to output high load power levels. A SC DC-DC converter which integrates the charge-transfer capacitors was described in [4]. In this work, we describe a 0.18µm CMOS voltage scalable SC DC-DC converter with integrated on-chip charge-transfer capacitors that achieves >70% efficiency at a wide range of load powers from 5µW to 1mW and can deliver load voltages ranging from 0.3V to 1.1V.

II. Scalable Voltage Generation

This section describes how scalable load voltages are generated from a 1.2V off-chip battery. Consider the T6 topology in Figure 1. It shows a simple switched capacitor voltage divide-by-two circuit. The charge-transfer capacitors are equal in value and help in transferring charge from the battery to the load. During phase Φ_1, the charge-transfer capacitors get charged from the battery (V_{BAT}). In the Φ_2 phase of the clock, they dump the charge gained onto the load (L). The reason behind the switches marked Φ_{1by3} or Φ_{2by3} is explained in section V (ii). Throughout this section assume that all switches shown in Figure 1 turn ON either in Φ_1 or Φ_2 (i.e. $\Phi_{1by3} = \Phi_1$; $\Phi_{2by3} = \Phi_2$). At no load, the T6 topology circuit tries to maintain the output voltage V_O at $V_{BAT}/2$ (0.6V), where V_{BAT} is the battery voltage. The actual value of V_O that the circuit settles down to is dependent on the load current I_O, the switching frequency and C_B. Let the T6 topology deliver a load voltage $V_O = V_{NL} - \Delta V$, where V_{NL} is the no-load voltage for this topology. The SC converter limits the maximum efficiency that can be achieved in this case to $\eta_{lin} = (1 - \Delta V/V_{NL})$. Thus, the farther away V_O is from V_{NL} (i.e. higher ΔV), the smaller the maximum efficiency that can be achieved by this topology. This is a fundamental problem with charge transfer using only capacitors and switches. Thus, to improve efficiency, it is necessary to switch in different topologies whose no-load

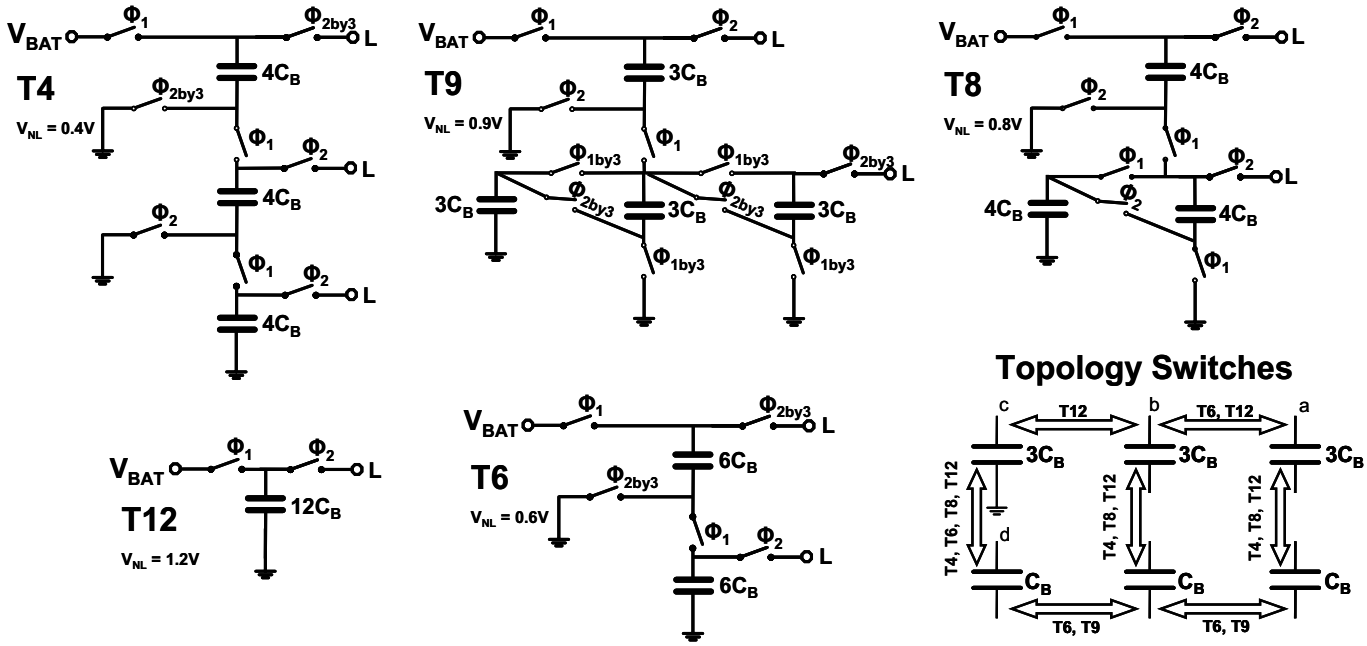

Figure 1. Topologies used to generate efficiently a wide range of load voltages from a 1.2V supply. The topology switches help form the topologies.

output voltage is closer to the load voltage desired. Fig. 1 shows the different topologies that were employed in the SC DC-DC converter. The output load voltage is scalable between 0.3V to 1.1V. The topologies are named based on the no-load voltage they deliver. For example, the T9 topology delivers a no-load voltage of 0.9V and T4, a no-load voltage of 0.4V. Each topology is clocked by two non-overlapping phases Φ_1 and Φ_2 of a system clock. In the first phase Φ_1, the charge-transfer capacitors are charged from the battery. In Φ_2, this charge gained is passed on to the load.

The T12 topology provides 1.2V at no-load. This topology behaves essentially like a linear regulator and it is used to provide load voltages between 0.9V and 1.2V. The T6 topology is a simple voltage divide-by-2 circuit, where 2 capacitors of equal value $6C_B$ are charged in series and discharge to the load in parallel. This topology caters to load voltages below 0.6V. The T4 topology is a divide-by-3 circuit and it caters to load voltages of 0.4V and below. The T8 topology shown on the top-right in Figure 1 has a no-load voltage of 0.8V and it provides a 2/3 voltage ratio output. The T8 topology functions as follows: During Φ_1, two capacitors of value $4C_B$ and $8C_B$ are charged in series from the battery. In steady state, the top capacitor of value $4C_B$ gets charged to 800mV or 2/3 of the battery voltage and the bottom capacitor of $8C_B$ to 400mV or 1/3 of the battery voltage. During Φ_2, the top $4C_B$ capacitor is connected directly to the load while the bottom $8C_B$ capacitor is split into two and connected in series with the load. This way the total voltage across the series combination is 800mV. The T8 topology is used to deliver load voltages below 800mV. The T9 topology is a ratio $3/4^{ths}$ circuit and has a no-load voltage of 0.9V. Its operation is similar to the T8 topology, except that the charge-transfer capacitors are broken down into $3C_B$ and $9C_B$ during Φ_1.

The specific topology to be used is determined based on the load voltage desired. Let the total capacitor budget for charge-transfer capacitors given a chip area constraint be $12C_B$. The individual capacitors used in the different topologies are obtained by joining fragments of the $12C_B$ capacitor using topology switches as shown on the right hand corner of Fig. 1. A topology switch represented by a two-headed arrow joins two capacitors. It consists of 2 switches, one to connect the top plates and one for the bottom plates. The topology switch is turned ON for the topologies marked on top of the arrow.

Apart from the topology switches, charge-transfer switches are employed within each topology as shown in Fig. 1. These switches are driven by either Φ_1 or Φ_2 or one of their divided versions Φ_{1by3} or Φ_{2by3}. All the charge-transfer switches used in the individual topologies are realized from a total of only 13 switches as can be seen from the switch array in Fig. 2. Each box in the array is representative of a switch which is turned ON depending on the topology in use and the phase of the

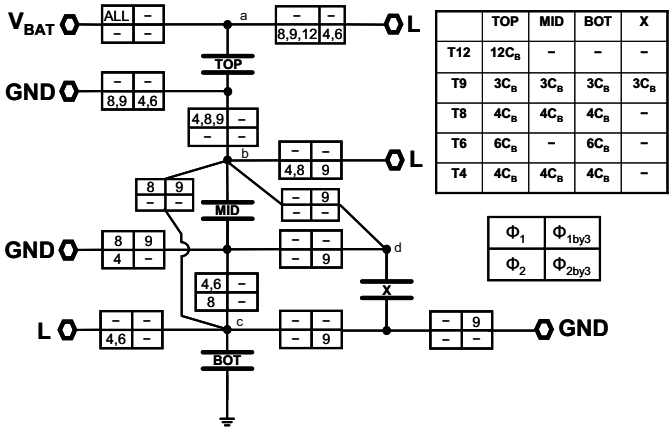

Figure 2. Charge-transfer switch array (each box represents a switch)

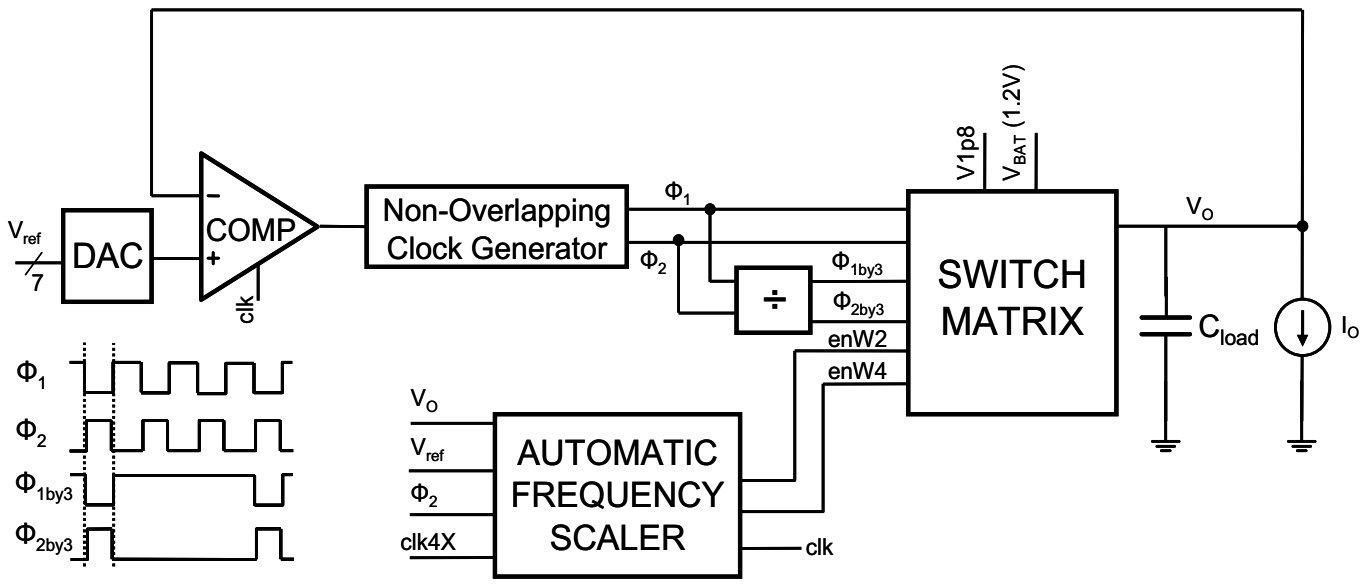

Figure 3. Architecture of the switched capacitor DC-DC converter system

clock. For instance, the switch which connects the top plate of capacitor TOP to the battery is turned ON in phase Φ_1 for all topologies while the switch that connects the bottom plate of capacitor TOP to ground (GND) turns ON during Φ_2 for topologies T8, T9 and during Φ_{2by3} for topologies T4, T6. The table inside Fig. 2 shows the value of the individual capacitors used in the different topologies. The nodes marked *a*, *b*, *c* and *d* correspond to the similarly named nodes in the right hand corner of Fig. 1. The charge-transfer switches are realized using PMOS or NMOS transistors or a combination of them depending on the location of the switch in the array (see section V (iii)). A very simple digital control is utilized to turn ON the switches depending on the topology in use. This arrangement of the switch array enables efficient sharing of charge-transfer switches between multiple topologies.

III. Switched Capacitor DC-DC Converter System Architecture

Figure 3 shows the architecture of the SC DC-DC converter. At the core of the system is the switch matrix which contains the charge-transfer capacitors, and the topology, charge-transfer switches. A suitable topology is chosen depending on the reference voltage V_{ref}, which is set digitally. The digital reference is converted to an analog value using an on-chip charge redistribution digital-to-analog converter. The entire circuit except for the topology switches operates from a 1.2V voltage supply. A 1.8V supply (V1p8) is used only for the topology switches. In steady state, as there is no switching involved in the topology switches, negligible power is consumed from the 1.8V supply. A pulse frequency modulation (PFM) mode control is used to regulate the output voltage to the desired value. A dynamic comparator clocked by the signal *clk* is used for this purpose. When the output voltage V_O is above V_{ref}, the switches are all set to the Φ_1 mode. When V_O falls below V_{ref}, the comparator triggers a Φ_2 pulse, which charges up the output load capacitor C_{load}. The non-overlapping clock generator block prevents any overlap between the Φ_1 and Φ_2 ON phases. A clock divider is used to generate Φ_{1by3} and Φ_{2by3} phases. Typical waveforms of these phases are shown in the inset in Fig. 3.

To minimize gate-switching losses, the circuit automatically adjusts the switching frequency depending on the load power demand. The automatic frequency scaling (AFS) block that performs the frequency selection is shown in Figure 4. An additional comparator called the overload comparator is used in the AFS block. The reference voltage of the overload comparator is set to V_{ref} - V_{off}, where V_{off} is an offset voltage (~20mV) which again is set digitally. When the DC-DC converter, operating in steady state, cannot supply the desired load power at a given switching frequency, V_O begins to fall below V_{ref} (see equation 3). As V_O falls below $V_{ref} - V_{off}$, the overload comparator triggers the *go_up* signal. This signal is used to double the switching frequency which in turn doubles the width of the charge-transfer switches. At low load powers, the switching frequency is brought down using a counter mechanism. If the number of Φ_2 pulses for every 4 *clk* cycles is found to be less than 3, the *go_down* signal is triggered which halves the switching frequency and the width of the charge-transfer switches. The signals *enW2* and *enW4* determine the switching frequency. When only *enW2* is high, 2X the minimum clock frequency is used and when *enW4* is high, 4X the minimum clock frequency is used. The signals *enW2* and *enW4* are fed into the switch matrix to suitably size the charge-transfer switches. While the PFM mode control effectively reduces the frequency of Φ_2 pulses as load power decreases, the AFS block helps in bringing down the overall system switching frequency together with the width of the charge-transfer switches, thereby reducing the switching losses in the gate-drive and the control circuitry. The entire control circuitry is digital and consumes no static power, which is a critical

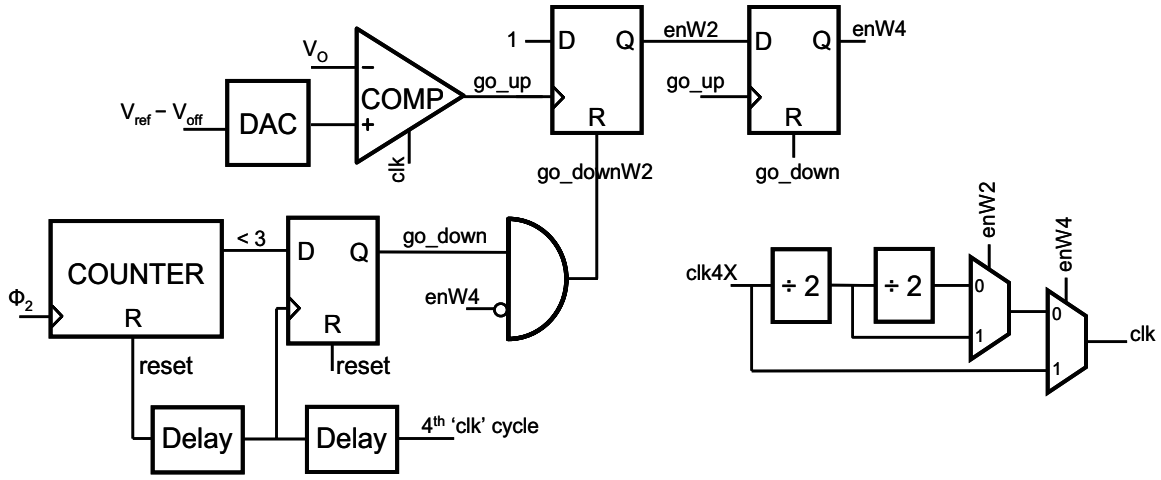

Figure 4. Automatic Frequency Scaling block

feature to achieve good efficiency at ultra-low load power levels. It is extremely scalable in terms of complexity to suit the load power and voltage demands of the target application.

IV. Power Delivery

This section presents an analysis of the power delivered to the load by the DC-DC converter. Consider the T6 topology shown in Fig. 1. Let the T6 topology deliver a load voltage $V_O = V_{NL} - \Delta V$, where $V_{NL} = V_{BAT}/2$ (0.6V) for this topology. Assume again that all the switches turn on in Φ_1 or Φ_2. While operating in steady-state, during phase Φ_2, both the $6C_B$ charge-transfer capacitors discharge down to V_O when the load capacitor is much larger than $6C_B$. When they are connected back in series again during phase Φ_1, both these capacitors get charged back to $V_{BAT}/2$. The energy extracted from the battery during this process is given by

$$E_B = 6C_B V_{BAT} \Delta V \tag{1}$$

During Φ_2, this excess charge is transferred to the load capacitor. The charge-transfer capacitors transfer twice the charge gained from the battery during Φ_1. However, this charge is delivered at a voltage V_O and hence the energy delivered to the load every cycle is a linear scaled version of the energy extracted from the battery and is given by

$$E_L = E_B \frac{V_{NL} - \Delta V}{V_{NL}} = 12C_B V_O \Delta V \tag{2}$$

The maximum power that can be delivered to the load by this topology when switching at a frequency f_s is then given by

TABLE I
Power Delivered To Load

Topology	E_B	η_{lin}
T12	$12C_BV_{BAT}\Delta V$	$V_O/1.2$
T9	$3C_BV_{BAT}\Delta V$	$V_O/0.9$
T8	$4C_BV_{BAT}\Delta V$	$V_O/0.8$
T6	$6C_BV_{BAT}\Delta V$	$V_O/0.6$
T4	$4C_BV_{BAT}\Delta V$	$V_O/0.4$

$$P_L = E_L f_s = 12C_B V_O \Delta V f_s = E_B f_s \eta_{lin} \tag{3}$$

where η_{lin} is the linear efficiency loss. From this expression it can be seen that to deliver more load power at a given load voltage, C_B or f_s need to be increased. Increasing C_B increases the energy extracted from the battery every switching cycle, whereas increasing f_s increases the rate of delivery of the charge packets. The power delivered to the load also depends on the topology being used. Table I gives a breakdown of E_B and η_{lin} for the various topologies.

It can also be noted that the larger ΔV is, i.e. the farther V_O is from the no-load voltage, the more power that the converter can deliver. This again is due to increased E_B. Thus, if a given topology is unable to meet the load power requirement even at the highest switching frequency, the next higher topology is used. This is the reason that even at moderate load power levels of 100µW, the T8 topology delivers a load voltage of 590mV and not the T6 topology. This leads to a drop in the linear efficiency than that could have otherwise been achieved had the load power requirement been low.

V. Efficiency Analysis

Efficiency of a power converter is a key metric for battery operated electronics and energy starved systems. The principal contributors to efficiency loss in the SC DC-DC converter are:

i) Conduction Loss in transferring charge from battery to load – This is a fundamental loss mechanism which arises from charging a capacitor through a switch. To minimize conduction loss, different topologies (Fig. 1) are switched in to reduce the difference between the no-load voltage (V_{NL}) of a topology and V_O. Assuming that a load voltage less than 600mV is being supplied by the T8 topology, conduction loss imposes a limit on the maximum efficiency that can be achieved to $\eta_{lin} = V_O / 0.8$. By switching to the T6 topology, this efficiency limit can be improved to $\eta_{lin} = V_O / 0.6$.

ii) Loss due to bottom-plate parasitic capacitors – The second main contributor to efficiency loss after the linear conduction loss is that due to parasitic bottom-plate capacitors.

This arises due to charging the bottom-plate parasitic capacitance [5] of the charge-transfer capacitors every charge cycle. This is of specific concern for on-chip capacitors in digital CMOS processes. The bottom-plate capacitance C_{BP}, scales with the capacitor area and can be expressed as $C_{BP} = \alpha C$, where α can be as high as 5% for the capacitors used. Consider the T6 topology. During the phase Φ_1 when the 2 charge-transfer capacitors are charged to one-half the battery voltage, the bottom-plate parasitic capacitance of the top capacitor also gets charged to $V_{BAT}/2$. In phase Φ_2 when these capacitors are connected in parallel to charge the load, the energy stored in the bottom-plate parasitic capacitance is lost by connecting it to ground. Assuming that normal switching is employed (i.e. all the switches are driven by Φ_1 or Φ_2), the energy lost per cycle in steady-state due to C_{BP} of the top capacitor is

$$E_{BP} = 1.5\alpha C_B V_{BAT}^{\ 2} \tag{4}$$

while the energy extracted from the battery per cycle, E_B is given by equation (1).

Let the ratio of E_{BP} to E_B be given by the following equation:

$$\frac{E_{BP}}{E_B} = K_p \frac{V_{BAT}}{\Delta V} = 0.25\alpha \frac{V_{BAT}}{\Delta V} \tag{5}$$

where K_p is a parasitic-loss parameter. For normal switching the factor K_p is 0.25α. The factor 0.25 in K_P is a topology-dependent parameter (Table II) while α is a technology-dependent parameter which depends on process parameters and the type of capacitor being used. Our proposed scheme to address the bottom-plate parasitic loss is to use divide-by-3 switching. For every topology (see Fig. 1) the capacitance that leads to significant bottom-plate parasitic loss is identified and it is switched once every 3 cycles. This way, the fraction of the energy lost due to bottom-plate parasitics is decreased. For the T6 topology, the top capacitor $6C_B$ is switched on to the load only once every 3 cycles. The switching waveforms are shown in the inset in Fig. 3. The energy extracted from the battery over 3 cycles is

$$E_{B,3} = 6C_B \times 1.75 V_{BAT} \Delta V = 10.5 C_B V_{BAT} \Delta V \tag{6}$$

while the energy lost due to C_{BP} remains approximately the same as given by equation (4). Thus, there is a 1.75X improvement in K_p when divide-by-3 switching is employed. A similar strategy is employed for the other topologies and the improvements obtained in K_p can be seen from Table II.

TABLE II

IMPROVEMENT IN K_P BY DIVIDE-BY-3 SWITCHING

Topology	K_p	$K_{p,\ divby3}$
T12	0	n/a
T9	0.375α	0.216α
T8	0.222α	n/a
T6	0.25α	0.141α
T4	0.555α	0.368α

For the T4 topology, the top capacitor contributes the most to bottom-plate loss and is switched only once in 3 charge transfer cycles. Since no marked improvement was observed in the T8 topology, the divide-by-3 switching scheme wasn't employed. For the T9 topology, the bottom capacitors are switched once in every 3 cycles. This is different from the other topologies because in T9 topology the top capacitor contributes $3/4^{th}$ to the energy transfer per cycle but the bottom capacitors contribute more to the parasitic loss. Thus by switching the bottom capacitors once in 3 cycles, a significant fraction of the energy can still be transferred per cycle while reducing the bottom-plate parasitic loss. While divide-by-3 switching improves efficiency by reducing the contribution of bottom-plate losses, it requires a higher switching frequency for a given load power level due to decreased energy transfer per cycle. While this increases gate switching losses in topologies T4 and T6, the divide-by-3 switching scheme decreases switching losses in T9 because of the reduction in the number of switches being switched every cycle (see Table III).

iii) Gate-drive Loss – The energy expended in switching the gate capacitances of the charge-transfer switches every cycle can be approximately given by

$$E_{SW} = nC_{ox}WLV_{BAT}^{\ 2} \tag{7}$$

where n is the number of switches used, C_{ox} is the gate-oxide capacitance per unit area, W and L are the width and length of the charge-transfer switches. The width of each switch is however proportional to the charge-transfer capacitance and the frequency of switching. This is because the resistance of the switches needs to be low enough to allow settling of the charge-transfer capacitors within the time period of switching. E_{SW} can then be expressed as

$$E_{SW} = n\gamma C_B f_s V_{BAT}^{\ 2} \tag{8}$$

where the constant γ depends on C_{ox}, L, the mobility μ and the threshold voltage of the devices. The ratio of E_{SW} to E_B can be expressed by equation (9), where K_s is a switching-loss parameter. Here again n is topology-dependent while γ is technology-dependent.

$$\frac{E_{SW}}{E_B} = K_s f_s \frac{V_{BAT}}{\Delta V} = n\gamma f_s \frac{V_{BAT}}{\Delta V} \tag{9}$$

To minimize the gate-switching loss, depending on the location of the charge-transfer switch and the topology in use, either only a PMOS or an NMOS switch is used instead of a transmission gate comprising both PMOS and NMOS devices. For example, the switch connecting the battery to the top plate of capacitor TOP in Fig. 2 is a PMOS-only switch, while all the switches connecting the bottom-plates of the capacitors to GND were NMOS-only. Also, while the switch connecting the top-plate of capacitor TOP to the load (L) comprises of both PMOS and NMOS devices, only the PMOS part of the switch is activated for T12 topology, while only the NMOS part of the same switch is activated for the T4 topology. The automatic

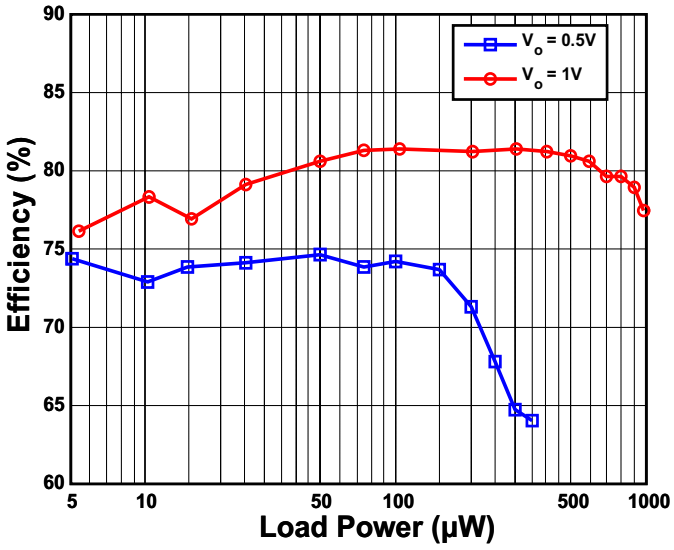

Figure 6(a). Efficiency plot with change in load power

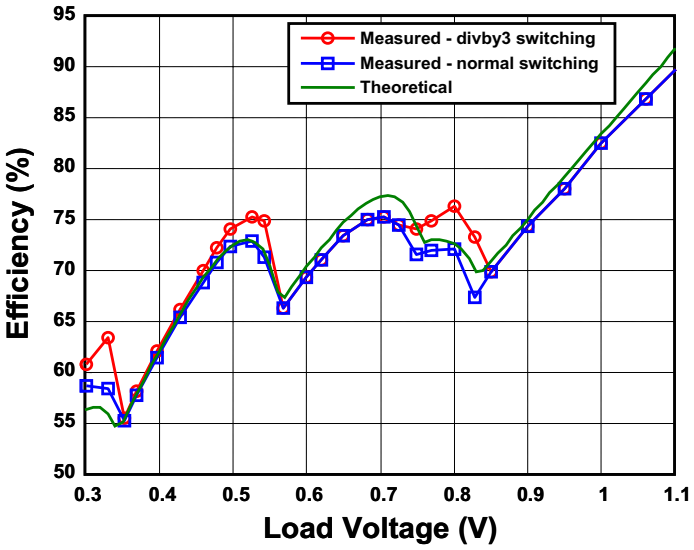

Figure 6(b). Efficiency plot with change in load voltage

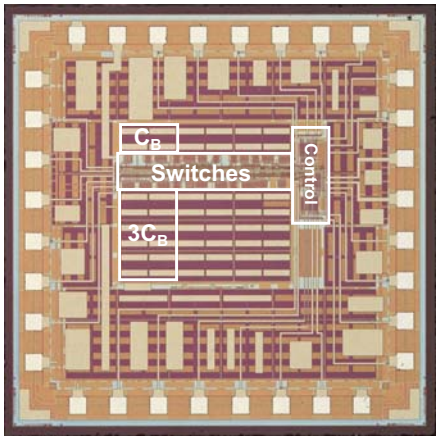

Figure 5. Die Photo of the switched capacitor DC-DC converter

frequency scaling technique described in section III scales the width of the charge-transfer switches as the switching frequency changes. This way, if the load power decreases by half, the AFS block halves both the switching frequency and the width of the charge-transfer switches, thereby effectively halving the ratio of E_{SW} to E_B.

iv) Power loss in the control circuitry – The power lost in the control circuitry is of specific concern while delivering ultra-low load power levels. The energy lost in the control circuitry every switching cycle can be broken into a switching and a leakage component and is given by

$$E_{CONT} = K_c V_{BAT}^{\ 2} + I_{leak} V_{BAT} T_{SW} \qquad (10)$$

where K_c is the average capacitance switched in the control circuitry every charge cycle, I_{leak} is the total leakage current consumed by the control circuitry and T_{SW} is the average time-period of a charge cycle. The control circuitry does not consume any static power (no analog bias currents) other than the subthreshold leakage currents in the digital circuitry.

The overall efficiency taking into account all the above mentioned losses can be expressed as the ratio between the total energy delivered to the load per cycle to the sum of the energy extracted from the battery and the energy losses / cycle.

$$\eta = \frac{E_L}{E_B + E_{BP} + E_{SW} + E_{CONT}} = \left(1 - \frac{\Delta V}{V_{NL}}\right)\left(\frac{1}{1 + K_p \frac{V_{BAT}}{\Delta V} + K_s f_s \frac{V_{BAT}}{\Delta V} + K_c \frac{V_{BAT}}{C_B \Delta V} + \frac{I_{leak} T_{SW}}{C_B \Delta V}}\right) \qquad (11)$$

On dividing the numerator and denominator by E_B, the overall efficiency can be expressed in a more compact form where the pre-factor is due to the linear efficiency. The 2nd term in the denominator is due to the bottom-plate parasitic loss. The next term is due to gate-drive switching loss, and the 4th and 5th terms are due to switching and leakage loss in the control circuitry. We see that while the linear conduction loss increases as ΔV increases, the other losses decrease with ΔV. Thus, for

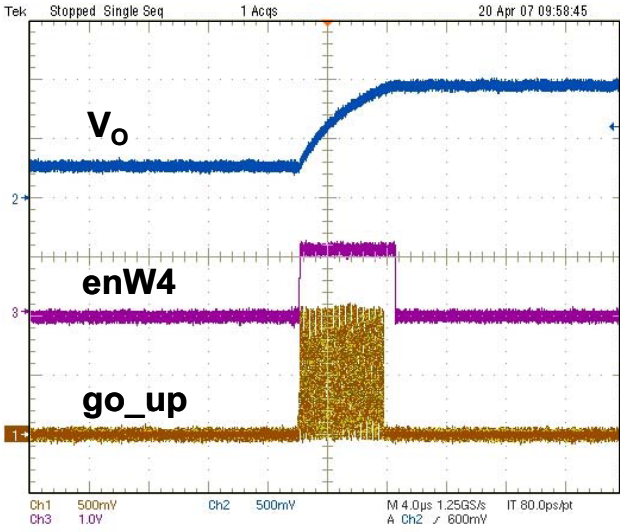

Figure 7. Waveform showing transient response

any given topology there is an optimum ΔV where the efficiency is maximized. The contribution of the switching losses in the control circuitry and the gate-drive can be minimized by increasing C_B. The leakage loss however is independent of C_B for a given load power because as C_B increases, the switching period T_{SW} also increases. In ultra-low load power levels, this leakage power component can be significant as the last term in the efficiency equation is just a ratio of the leakage power to load power.

VI. Measured Results

A switched capacitor DC-DC converter test-chip, incorporating all the features explained in the sections above, was fabricated in National Semiconductor's 0.18μm CMOS process. Fig. 5 shows a die-photo of the implemented chip. The die area occupied was 1.6 x 1.6mm^2 with the active circuitry consuming just 0.57mm^2, bulk of which was occupied by the charge-transfer capacitors. Gate-oxide capacitors were used for charge-transfer because of their high density and low bottom-plate parasitics. A total of 2.4nF of charge-transfer capacitance was used. The maximum clock frequency (*clk4X* in Fig. 4) employed was 15MHz. The DC-DC converter was able to deliver load voltages from 300mV to 1.1V. The efficiency of the SC converter with change in load power is shown in Figure 6a. The T12 topology was used to deliver 1V and T6 topology was used to deliver 0.5V. At 0.5V, the DC-DC converter was able to achieve close to 74% efficiency over a wide range of load powers. The effect of switching losses in bringing down the efficiency can be seen at load power levels above 150μW. The efficiency of the SC converter with change in load voltage while delivering 100μW to the load from a 1.2V supply is shown in Fig. 6b. The converter was able to achieve >70% efficiency over a wide range of load voltages. An increase in efficiency of close of 5% due to the divide-by-3 switching scheme can be seen at voltages delivered by the topologies T9 and T4. The measured efficiency plot closely matches the theoretical efficiency values as obtained by using equation 11.

The topology switch into the T9, T8, T6 and T4 topologies was made at 850mV, 750mV, 570mV and 350mV respectively, when divide-by-3 switching was employed. When normal switching was employed, the switch into the T9 topology was made at 825mV. The switching between topologies does not occur at the no-load voltages of the individual topologies. This is because at very low ΔV's the efficiency is low due to the bottom-plate and switching losses. Also, the load power delivered is very low at low ΔV's. The optimum load voltage where efficiency is maximized for each topology can also be seen from the peaks in Figure 6(b). The reason for this was explained in the previous section. Table III shows a breakdown of the power lost in the different loss mechanisms while delivering 100μW at 0.8V through the T9 topology. A quantitative estimate of the reduction in bottom-plate losses due to divide-by-3 switching can be seen.

Figure 7 shows a measured plot of the transient in load voltage when the reference voltage is raised from 0.3V (T4) to 1V (T12). The SC DC-DC converter takes close to 6μs to raise the output voltage to 1V when 100μA is being delivered to the load. The waveforms corresponding to the *enW4* and *go_up* signals show the operation of the automatic frequency scaling block explained in section 3. The *enW4* signal remains high till the desired load voltage is reached, thereby enabling a fast transient response. Once, the converter settles close to 1V, the *enW4* signal goes low to reduce the switching losses.

TABLE III

BREAKDOWN OF THE DIFFERENT LOSS MECHANISMS WHILE DELIVERING 100μW AT 0.8V (T9) (η_{normal} = 0.717, η_{divby3} = 0.763)

Loss Mechanism	Power Loss	
	Normal	Div-by-3
Conduction	12.45μW	12.45μW
Bottom-plate	14.68μW	7.47μW
Gate-drive	8.32μW	6.38μW
Control	4μW	4.69μW

VII. Conclusion

This paper has presented a switched capacitor DC-DC converter with on-chip charge-transfer capacitors that can deliver scalable load voltages from 300mV to 1.1V. Multiple topologies were employed in the SC DC-DC converter to minimize conduction losses. These topologies were obtained by suitably combining fragments of the charge-transfer capacitors. A divide-by-3 switching scheme was employed to minimize losses due to parasitic bottom-plate capacitors. This scheme was able to provide close to 5% improvement in efficiency. An automatic frequency scaling scheme was utilized to minimize switching losses. The converter employs completely digital control with no static power losses. The switched capacitor DC-DC converter test-chip was fabricated in a 0.18μm digital CMOS process and was able to achieve >70% efficiency over a wide range of load voltages.

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