

### 3.2 Minimum Energy Tracking Loop with Embedded DC-DC Converter Delivering Voltages down to 250mV in 65nm CMOS

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Minimizing the energy consumption of battery powered systems is a key focus in integrated circuit design. Switching energy of digital circuits reduces quadratically as  $V_{DD}$  is decreased below  $V_T$  (i.e. sub-threshold operation), while the leakage energy increases exponentially. These opposing trends result in a minimum energy point (MEP), defined as the operating voltage at which the total energy consumed per operation ( $E_{op}$ ) is minimized [1]. Operating circuits at their MEP [1, 2] has been proposed as a solution for energy critical applications and the analytical solution of the MEP has been derived in [3]. The MEP can vary widely for a given circuit depending on its workload and environmental conditions (e.g., temperature). By tracking the MEP as it varies, energy savings of 50 - 100% are demonstrated and even greater savings can be achieved in circuits dominated by leakage. In this paper, a 65nm CMOS circuit that can dynamically track the MEP of a digital circuit with varying operating conditions is presented. Embedded within the tracking loop is an ultra-low-power switching DC-DC converter that can efficiently deliver supply voltages down to 250mV, enabling minimum energy operation.

Figure 3.2.1 shows the architecture of the MEP tracking loop, which adjusts the output  $V_{DD}$ , to the minimum energy operating voltage of the digital circuit (FIR filter). An energy sensor circuit, together with an energy minimization algorithm, is used to set the reference voltage of the DC-DC converter. The DC-DC converter maintains  $V_{DD}$  close to the reference voltage. The key element in the loop is the energy sensor circuit which computes the  $E_{op}$  of the digital circuit at a given reference voltage. The DC-DC converter is disabled during energy sensing. Assuming that the voltage across the storage capacitor  $C_{load}$  falls from the reference voltage  $V_1$  to  $V_2$  in the course of  $N$  operations of the digital circuit,  $E_{op}$  at the voltage  $V_1$  is equal to  $C_{load} \times (V_1^2 - V_2^2)/2N$ . To measure  $E_{op}$  accurately,  $V_2$  should be close in value (within 20 - 30mV) to  $V_1$ . Methods to measure  $E_{op}$ , by digitizing  $V_1$  and  $V_2$  using conventional ADC's, or by sensing the inductor current, dissipate a significant amount of overhead power. Our proposed energy efficient approach to obtain  $E_{op}$  is to observe that, by design,  $V_1$  is very close to  $V_2$ . Thus,  $V_1^2 - V_2^2$  can be simplified to  $2V_1 \times (V_1 - V_2)$  within an acceptable error. Since, the digital representation of  $V_1$ , which is the reference voltage to the DC-DC converter, is already known, only the digital value for  $V_1 - V_2$  is required to estimate  $E_{op}$ .

Figure 3.2.2 shows the voltage difference measuring circuitry. Before starting an  $N$  operation energy sense cycle, the voltage  $V_1$  across  $C_{load}$  is sampled on  $C_1$  and the DC-DC converter is disabled. The digital circuit runs for  $N$  operations using the energy stored in  $C_{load}$ , and the voltage across  $C_{load}$  droops to some value  $V_2$  ( $< V_1$ ), which is then sampled across  $C_2$ . Subsequently, the DC-DC converter is enabled and normal operation of the digital circuit continues. At this point, a current sink ( $M_1$ ,  $M_2$ ) connected across  $C_1$  turns ON and a fixed frequency clock drives a counter. The fixed frequency clock, together with the constant current sink that drains  $C_1$ , quantizes voltage into time steps, as in an integrating ADC. The number of fixed frequency clock cycles required for  $C_1$  to droop down to  $V_2$  is directly proportional to  $V_1 - V_2$ . Once the value of  $V_1 - V_2$  is obtained digitally, it is multiplied with  $V_1$  to get an estimate of  $E_{op}$ .

The digital representation of  $E_{op}$  is then used by a slope descent algorithm to arrive at the MEP. Based on the value of  $E_{op}$  obtained, the algorithm suitably changes the reference voltage to the DC-DC converter. Once the converter settles at this new voltage, the energy sensing operation is performed again and the

cycle repeats until the minimum is achieved. At this point the loop shuts down. Figure 3.2.3 shows measured waveform of the tracking loop in operation. The MEP tracking loop can be enabled by a system controller as needed depending on the application.

Figure 3.2.4 shows the DC-DC converter embedded within the minimum energy tracking loop. The converter is a synchronous rectifier buck converter [4] with off-chip filter elements. It is designed to deliver load voltages from  $V_{DD} = 250mV$  to as high as  $V_{DD} = 700mV$  at ultra-low load power levels from  $1\mu W$  to  $100\mu W$ . This precludes the usage of high gain amplifiers for zero voltage and current switching. The converter implemented uses an open loop control for zero current switching. Depending on the load voltage being delivered, an appropriate delay is multiplexed in, turning the NMOS off when the inductor current approaches zero (see Fig. 3.2.4). A Pulse Frequency Modulation (PFM) control scheme is used to improve efficiency as the load power levels are low. The clock for the reference voltage comparator is derived from the critical path replica ring oscillator which feeds the digital circuit. This allows the comparator clock to scale automatically with  $V_{DD}$  and hence the load power, eliminating unnecessary comparisons. The simplicity of open-loop PFM mode control helps in decreasing the power consumption of the control circuitry, thereby improving the low load efficiency. The converter efficiency, plotted from measured results in Fig. 3.2.5, is  $>80\%$  while delivering load powers of  $1\mu W$  and higher and  $86\%$  at  $100\mu W$  ( $V_{DD}=0.5V$ ).

Figure 3.2.6 shows how the MEP varies with workload for a 7-tap FIR filter implemented in 65nm CMOS. Workload is changed by varying the number of taps of the FIR filter. The MEP decreases with increasing workload because the ratio of the active energy to total energy per operation increases. It can be deduced from curves 1, 2 in Fig. 3.2.6 that 110% energy is saved by moving  $V_{DD}$  to the new MEP value instead of staying at the original MEP value of 320mV. The MEP increases with temperature as the ratio of leakage energy to total energy per operation increases. Energy savings of the order of 50% is achieved as the MEP is tracked when the temperature changes from 0 to  $85^\circ C$ . The energy savings obtained are highly circuit dependent and can be much larger in modern digital IC's, which dissipate a significant portion of power in leakage.

The energy overhead associated with obtaining the MEP is equivalent to the energy consumed by 50 operations at the MEP in the minimum workload scenario (WL1). The proposed minimum energy tracking loop is *non-intrusive*, thereby allowing the load circuit to operate without being shut down. The tracking methodology is independent of the size and type of digital circuit being driven and the topology of the DC-DC converter.

Figure 3.2.7 shows the micrograph of the test chip fabricated in a 65nm CMOS process. The active area of the chip, which includes the digital test circuitry, occupies  $0.23mm^2$  with the minimum energy tracking circuitry occupying  $0.05mm^2$ . The small area and energy overhead of the tracking loop facilitates the use of multiple such loops for each distinct voltage domain in a complex digital system.

#### Acknowledgements:

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#### References:

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- [4] J. Xiao, et al., "A 4 $\mu A$ -Quiescent-Current Dual-Mode Buck Converter IC for Cellular Phone Applications," *ISSCC Dig. Tech. Papers*, pp. 280-281, Feb., 2004.

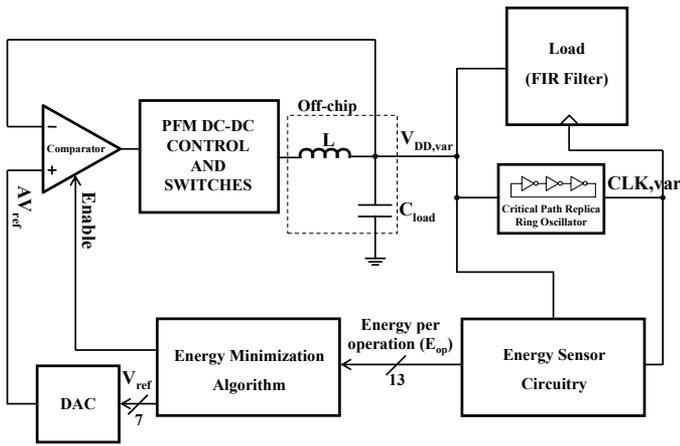


Figure 3.2.1: Block diagram of the minimum energy tracking loop and embedded DC-DC converter.

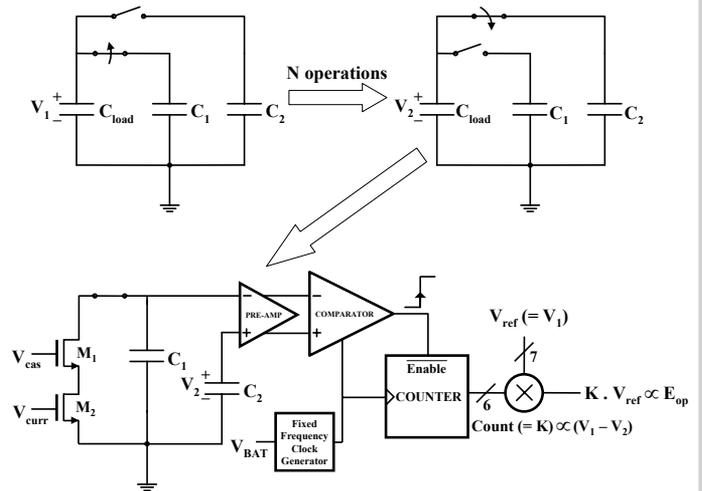


Figure 3.2.2: Circuitry to compute Energy/operation ( $E_{op}$ ) at a given operating voltage.

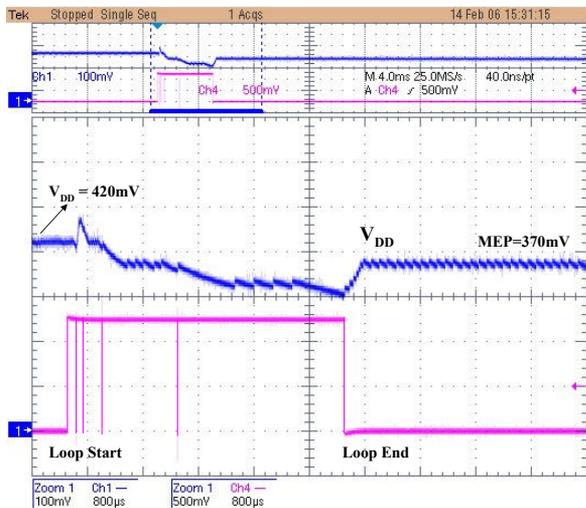


Figure 3.2.3: Measured waveform showing the minimum energy tracking loop in operation.  $V_{DD}$  starts at 420mV and is then increased to 470mV. The loop then changes direction and reduces  $V_{DD}$  to 370mV and 320mV before settling at the MEP of 370mV.

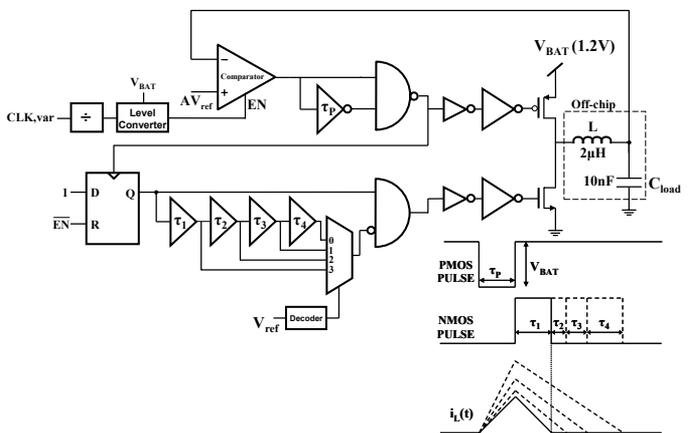


Figure 3.2.4: Pulse Frequency Modulation control of the DC-DC converter showing open-loop NMOS pulse width determining circuitry. The time delays are chosen to turn the NMOS off as the inductor current approaches zero.

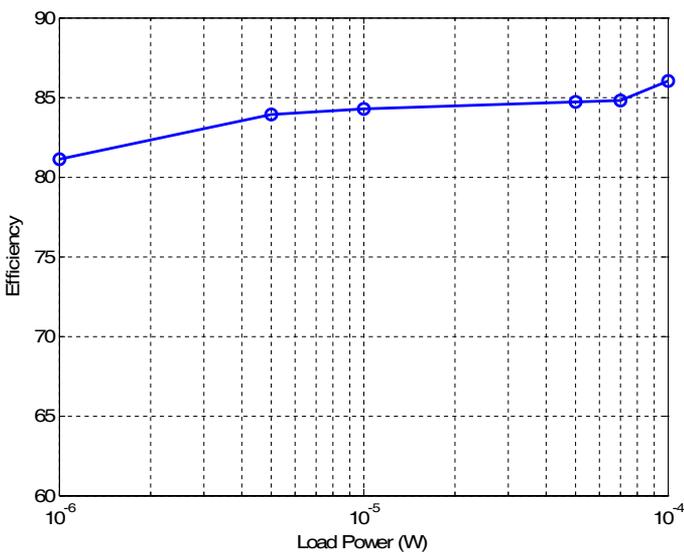


Figure 3.2.5: Measured efficiency plot of the DC-DC converter.

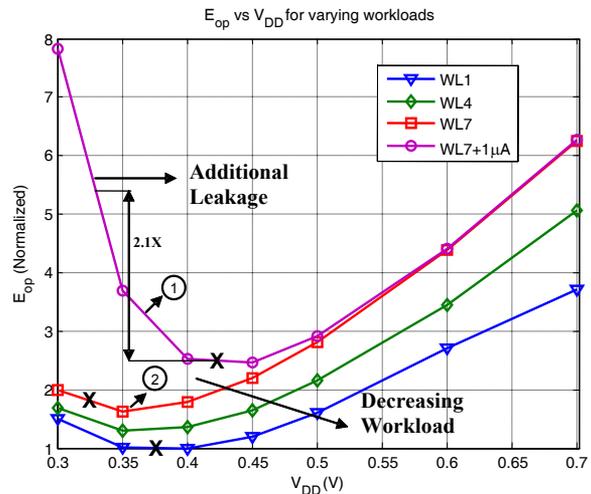


Figure 3.2.6: Measured  $E_{op}$  curves with change in workload for a 7-tap FIR filter. Curve 1 has an intentional 1 $\mu$ A leakage current added to the maximum workload scenario (curve 2). 'X' denotes the measured voltage at which the minimum energy loop settles.

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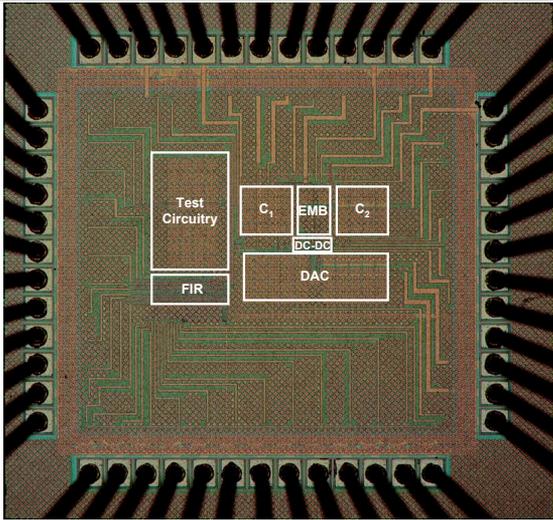


Figure 3.2.7: Micrograph of the test chip in 65nm CMOS. EMB is the energy minimizing block which comprises the energy sensor circuitry and the energy minimization algorithm.