

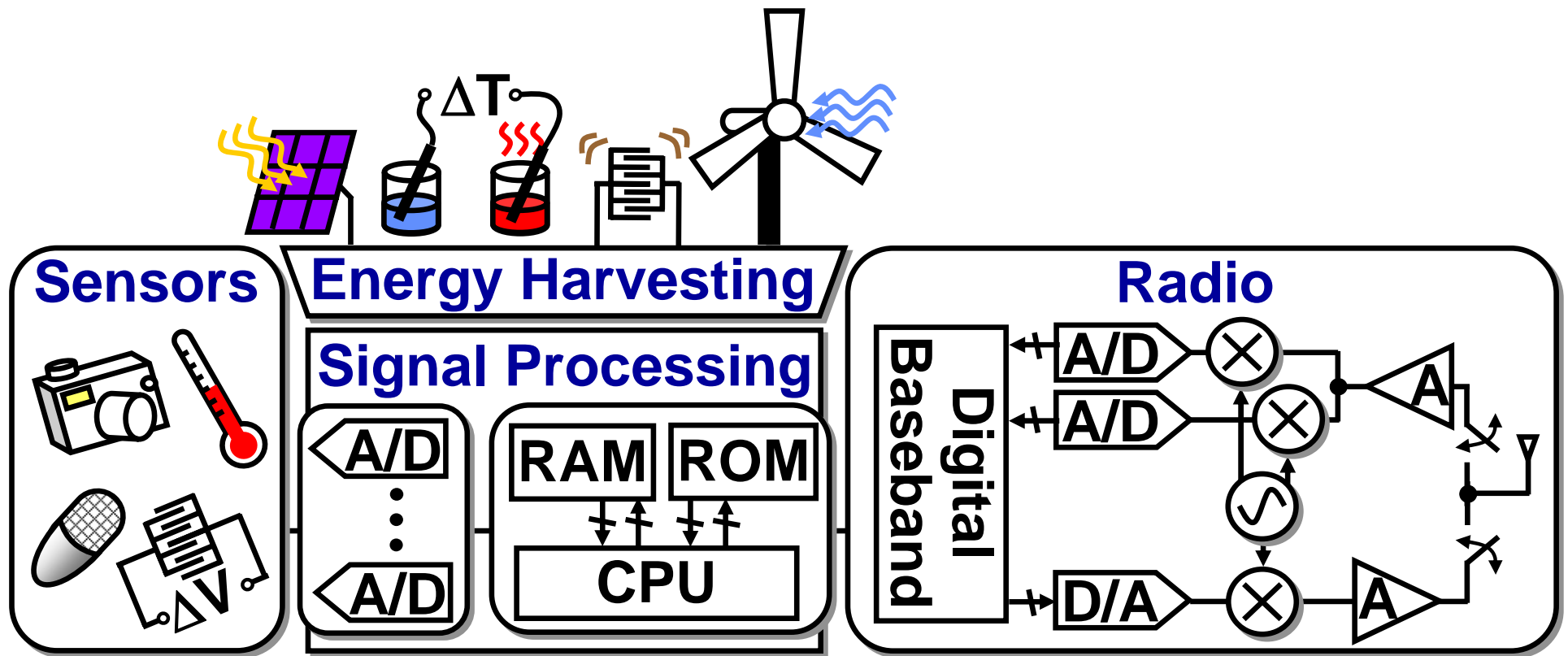
**A 2.5nJ/b 0.65V 3-to-5GHz  
Subbanded UWB Receiver in  
90nm CMOS**

**Fred S. Lee and Anantha P. Chandrakasan**

***Massachusetts Institute of Technology  
Cambridge, MA***

***ISSCC 2007***

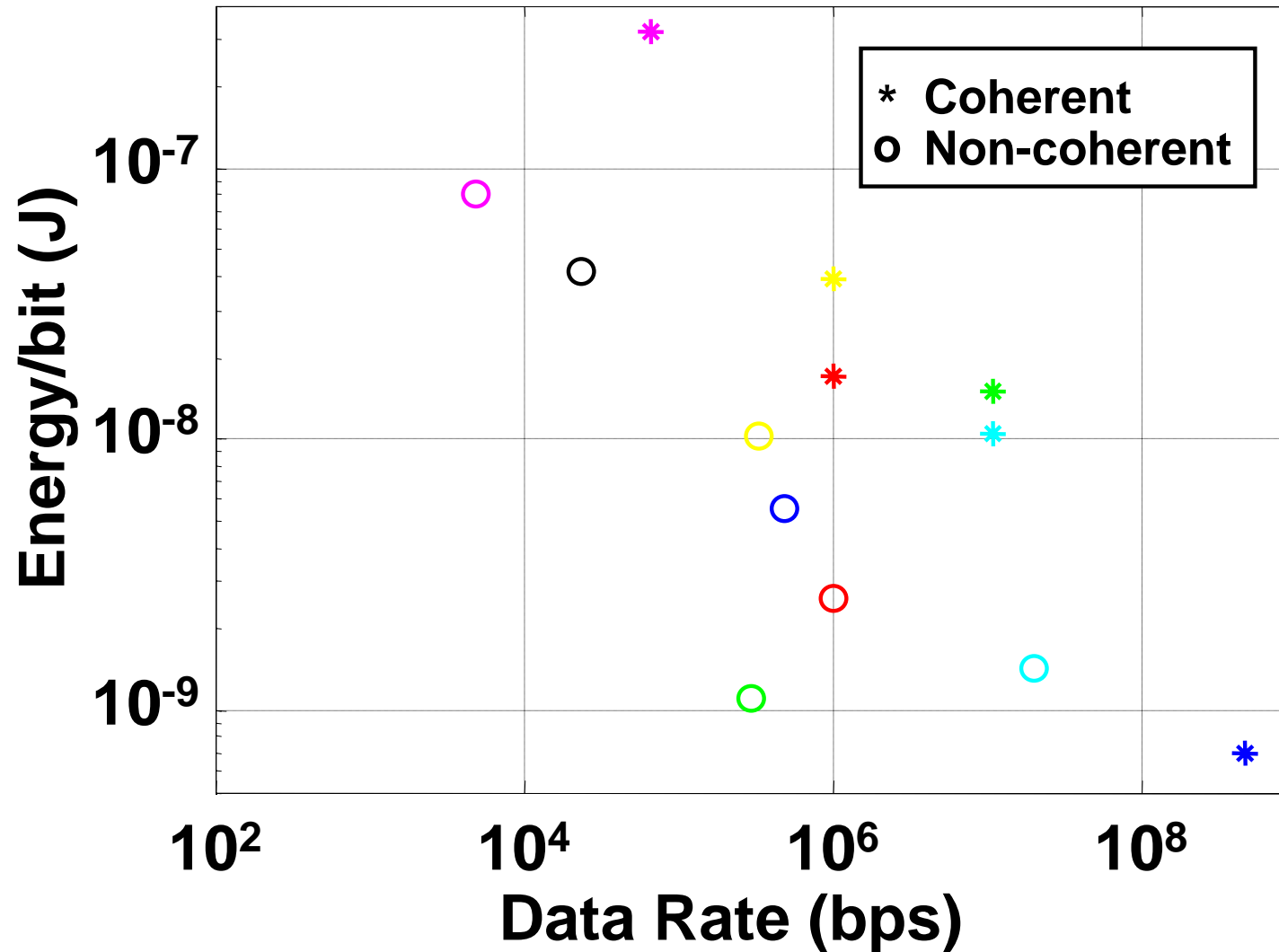
# Wireless Sensor Networks



**Simple Architecture**  
**Low Data Rate**  
**Low Power Radio**

# Radio Challenges

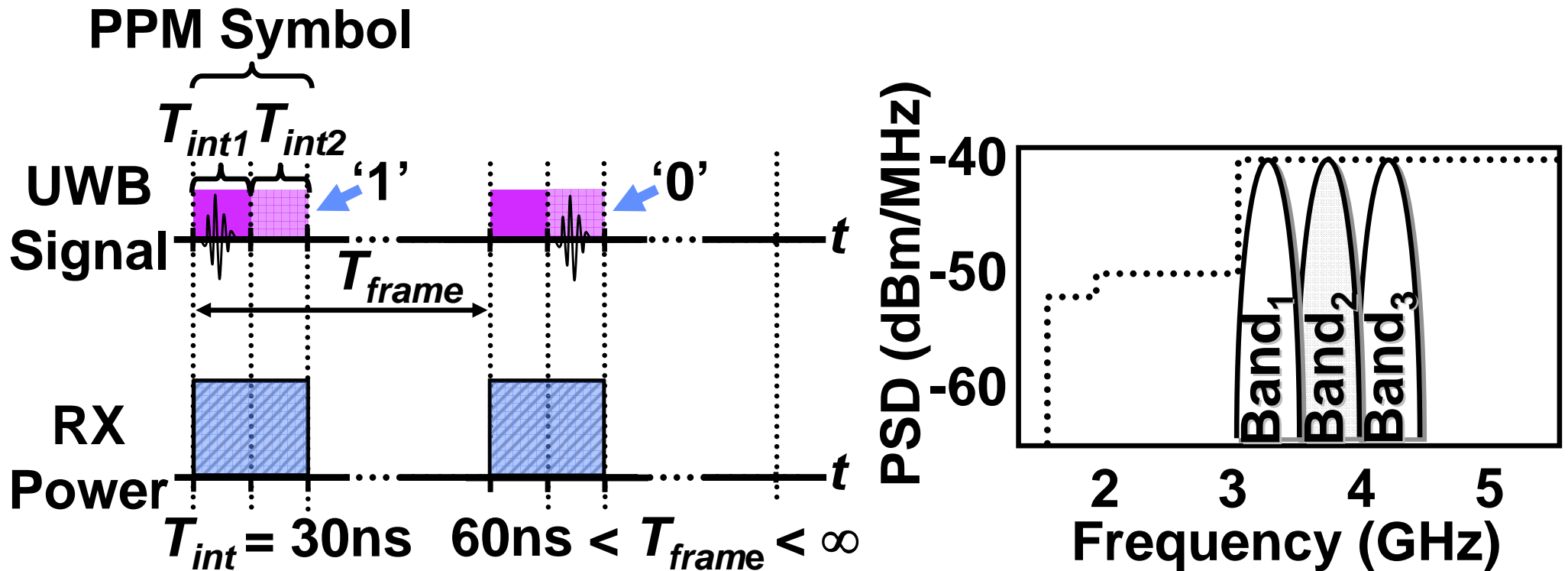
## *Recent ISSCC Receivers*



**Data Rate Independent, Low Energy/bit Radio**

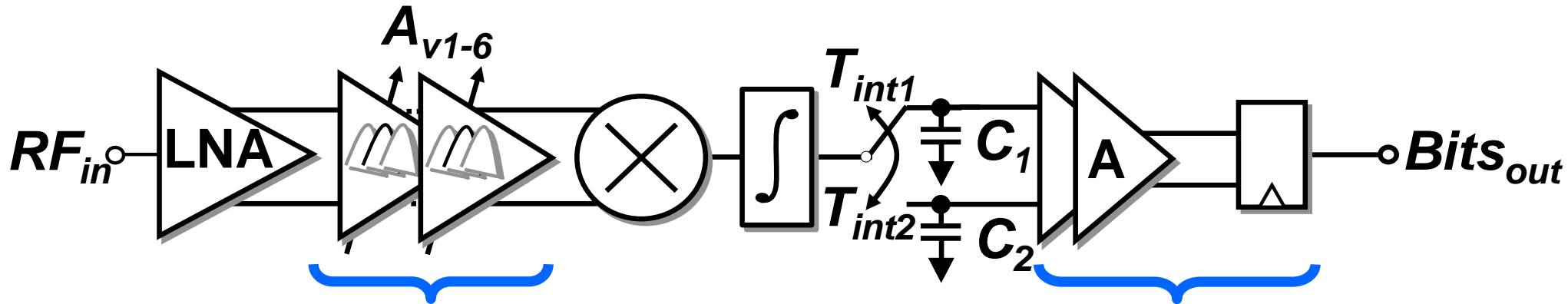
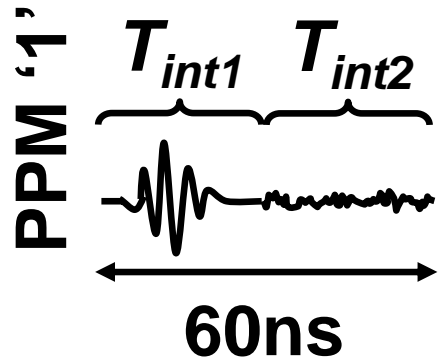
# Signaling and Frequency Plan

**Signaling Method: 2-PPM    3 Band Frequency Plan**



- $T_{int}$  set for worst channel
- Increased diversity
- Allows for duty-cycled RX
- Interference robustness

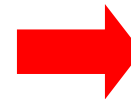
# Receiver Architecture



6-Stage Adjustable  
BPFs and Gain

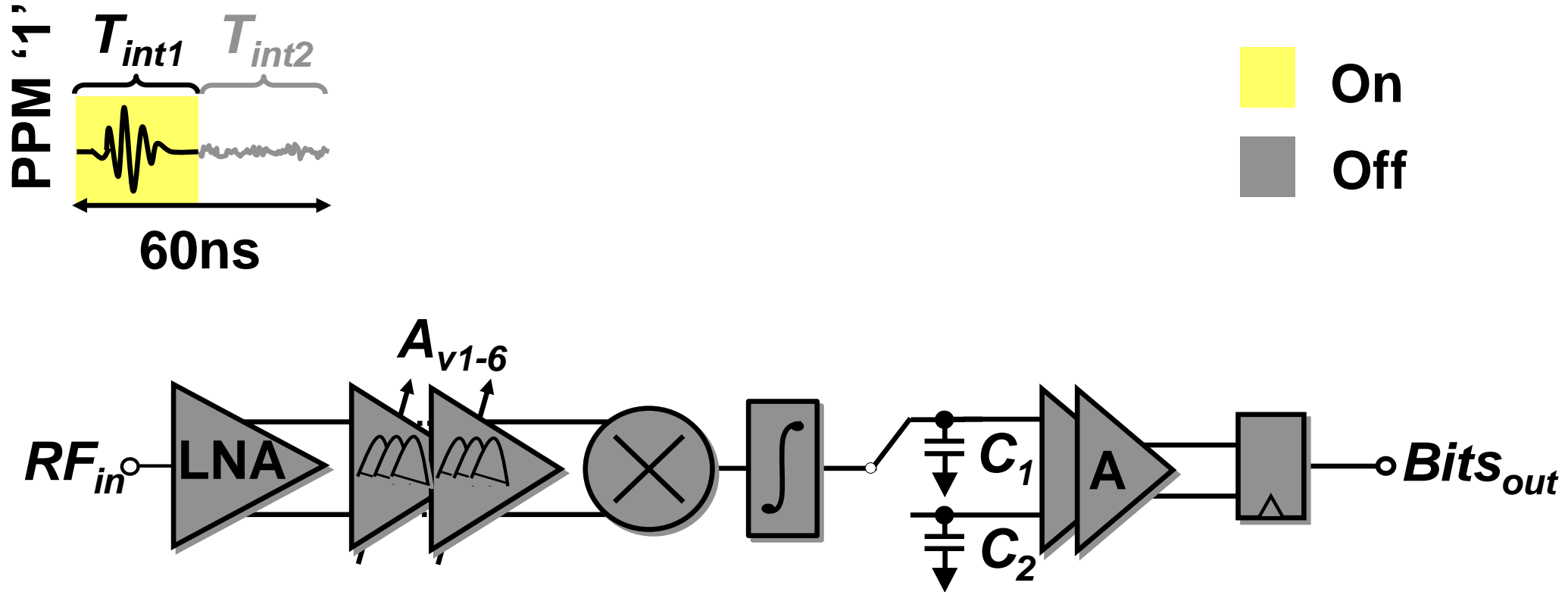
Offset Compensated  
Preamplifiers and Latch

- Energy detection receiver
- All circuits on/off time  $\sim 2\text{ns}$
- No RF PLL; only 30MHz clock



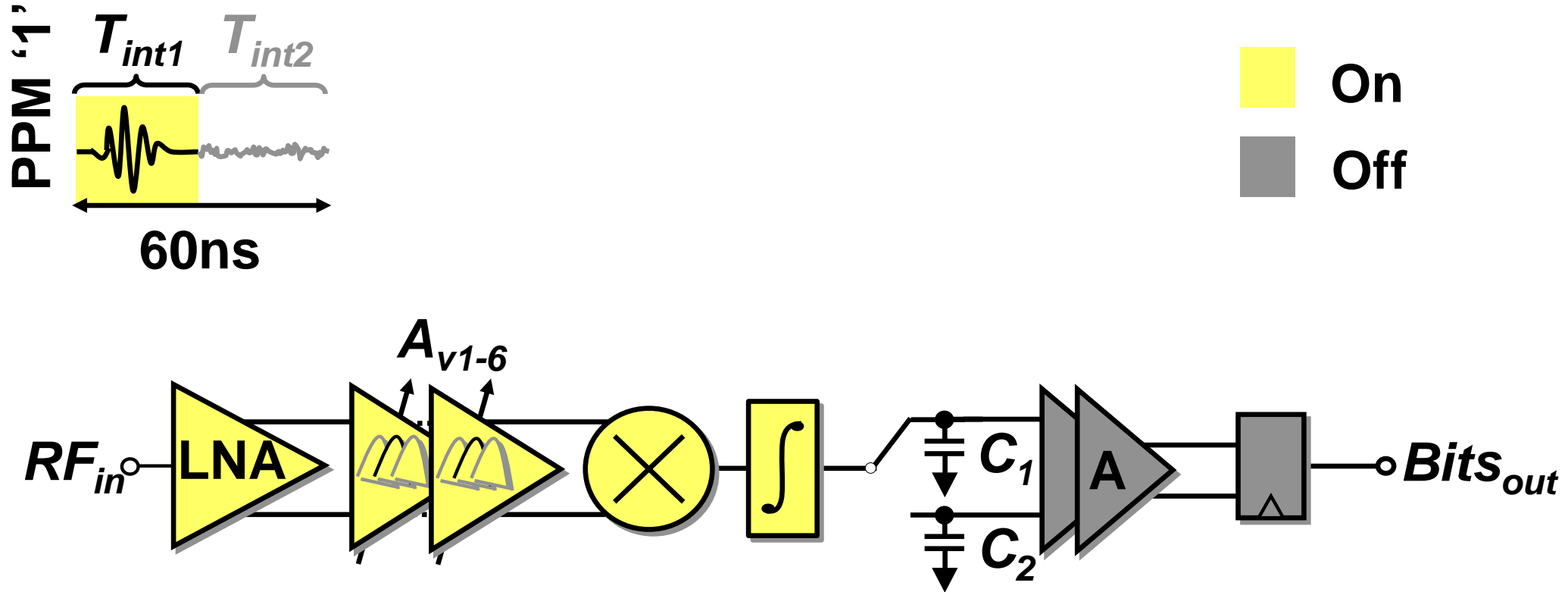
Low  
Complexity  
Receiver

# System Functionality

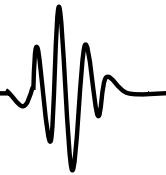


Receiving a '1'

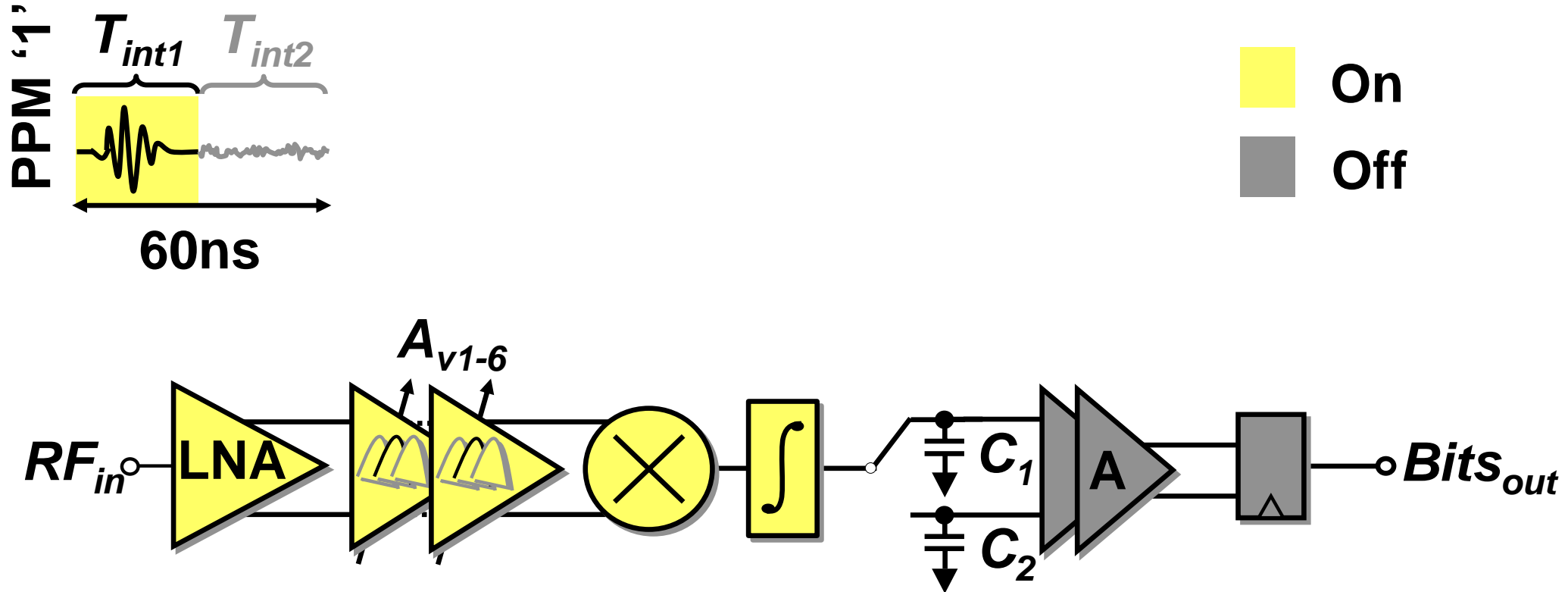
# System Functionality



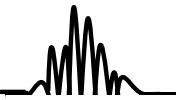
Pulse Reception



# System Functionality

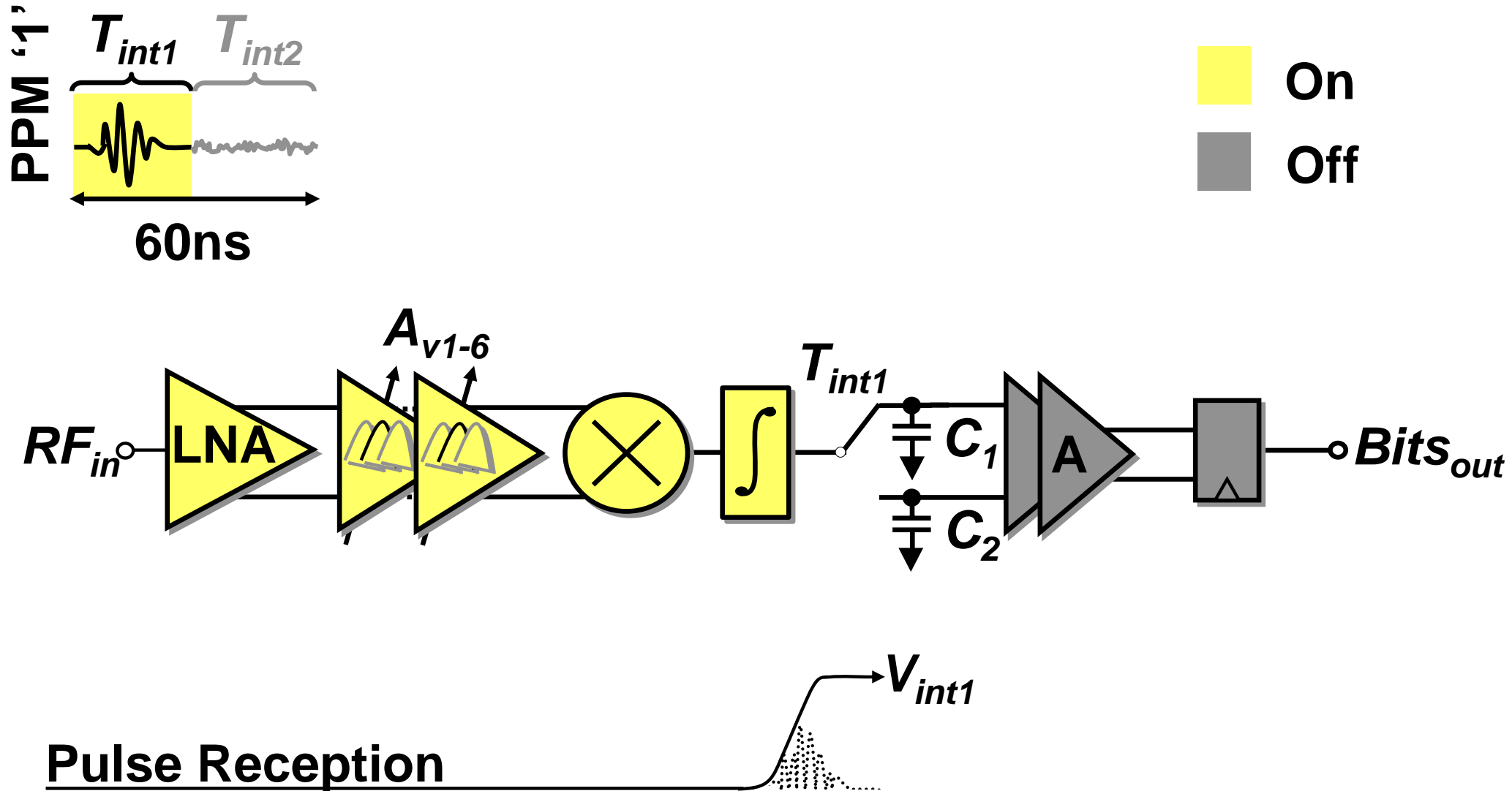


Pulse Reception

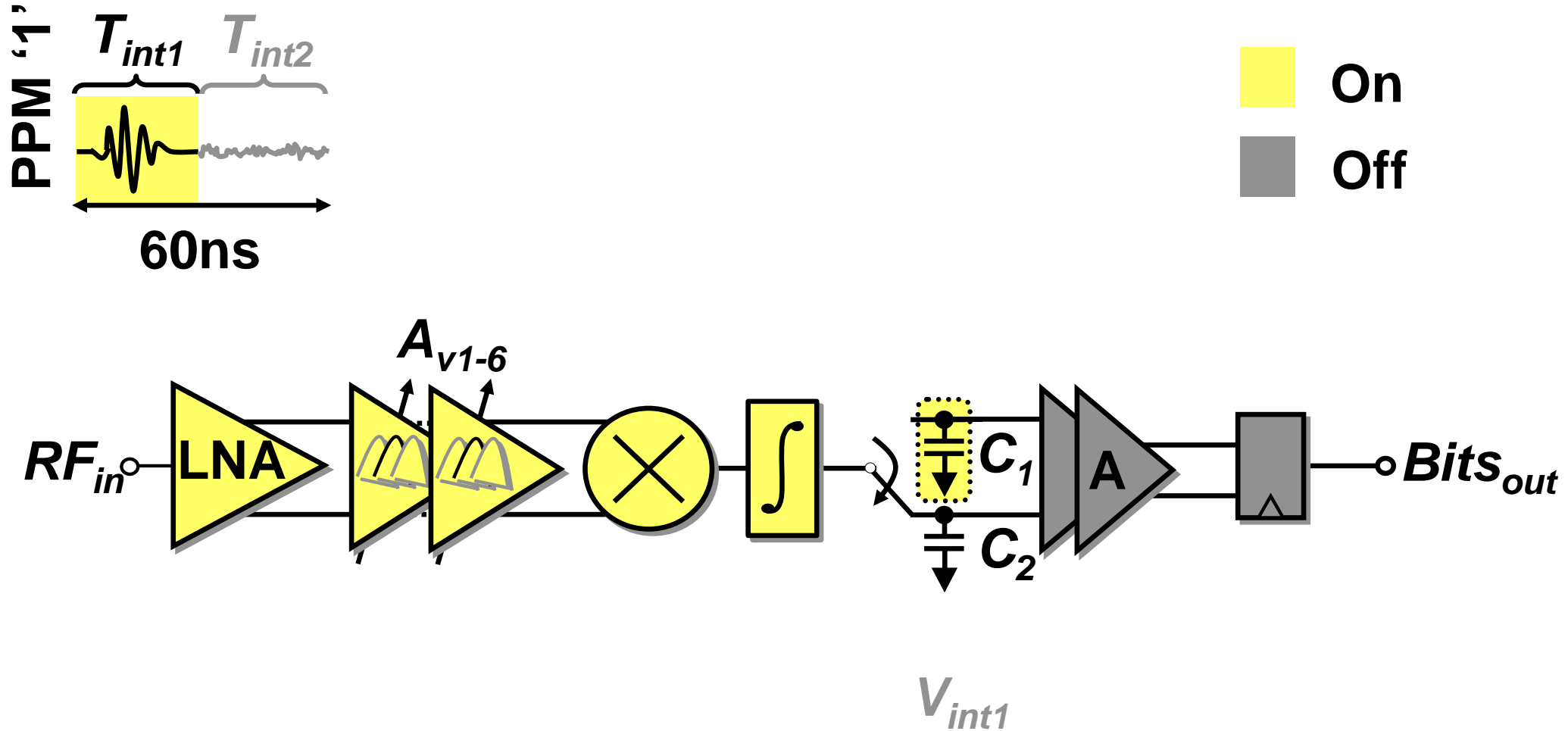




# System Functionality

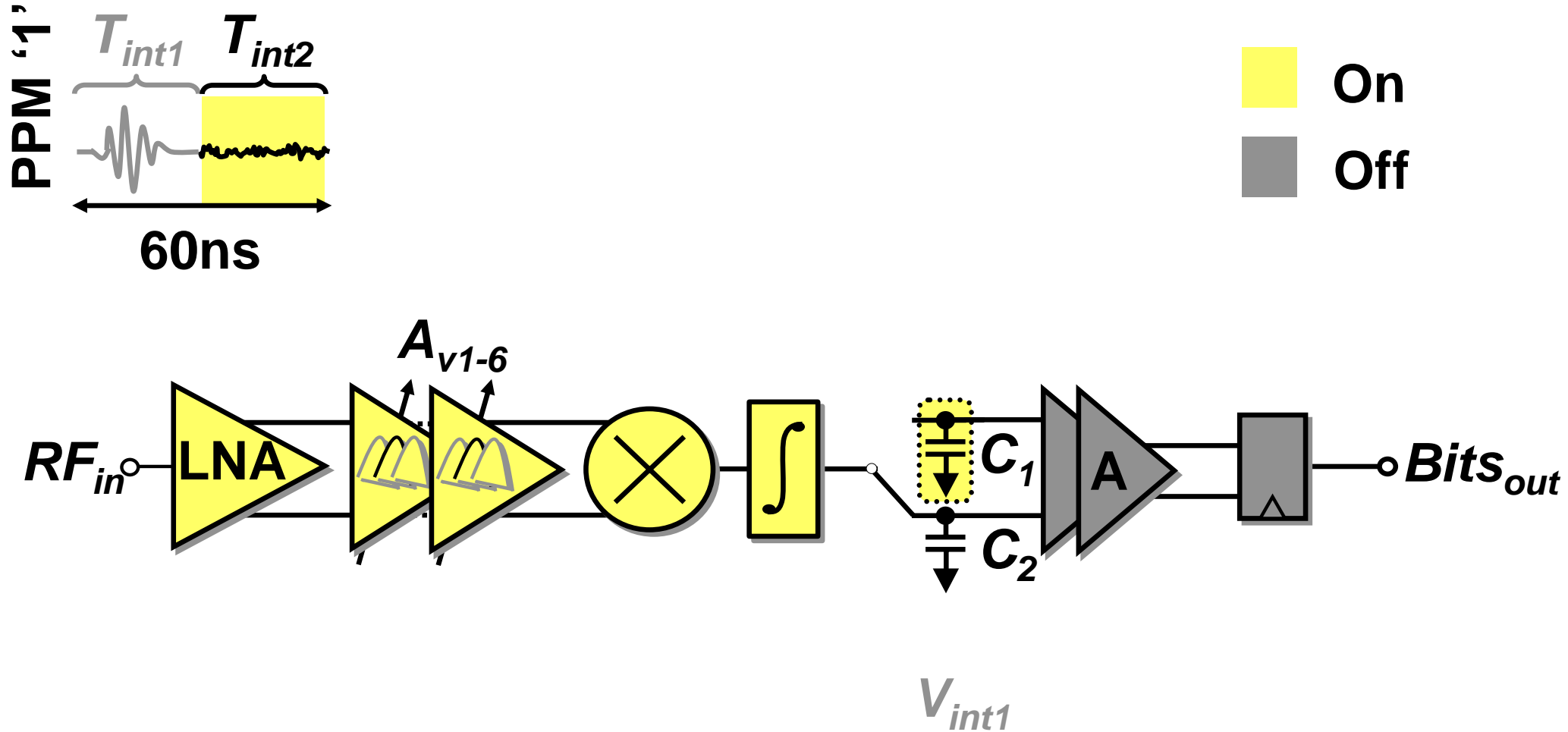


# System Functionality



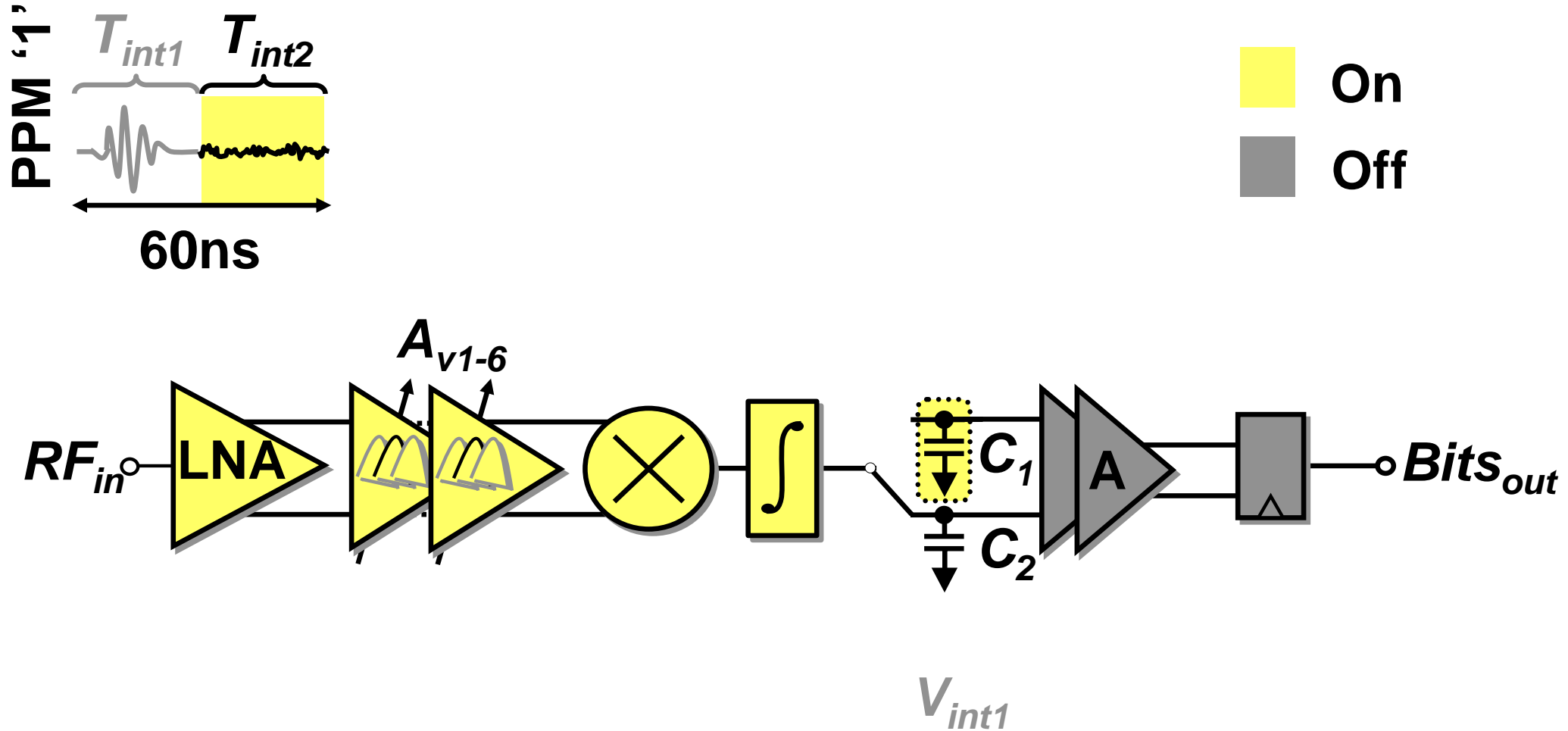
Pulse Storage

# System Functionality



Noise Reception 

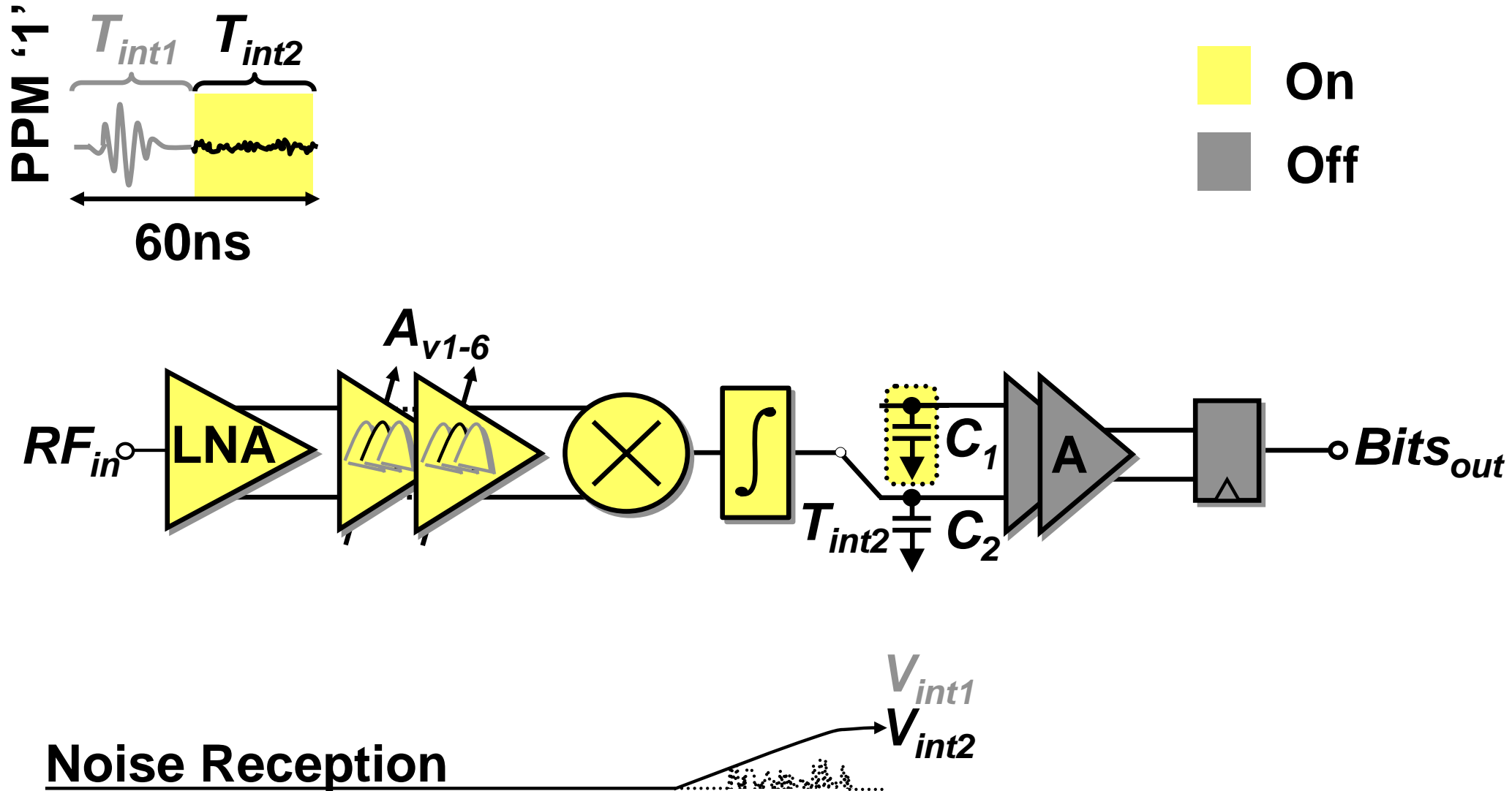
# System Functionality



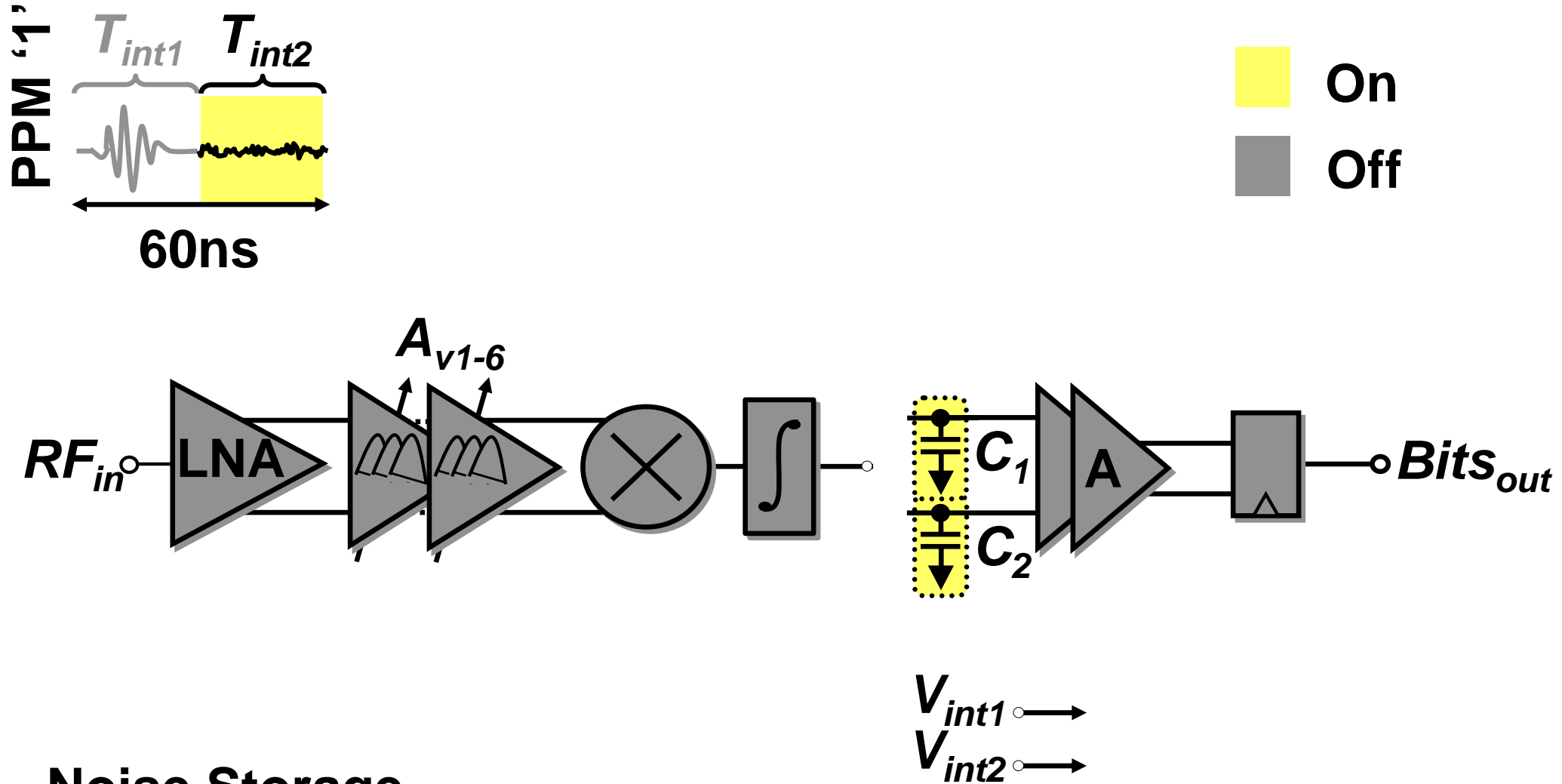
Noise Reception



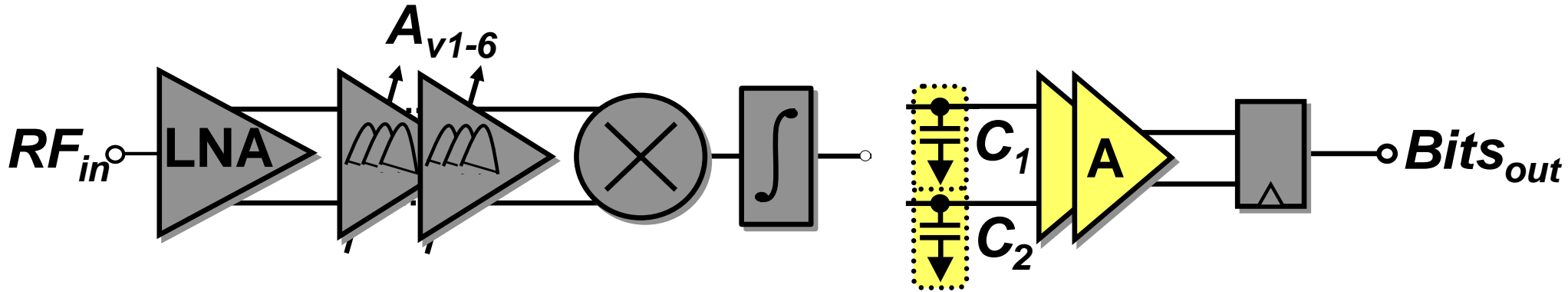
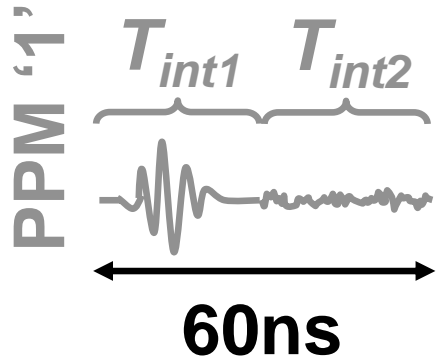
# System Functionality



# System Functionality

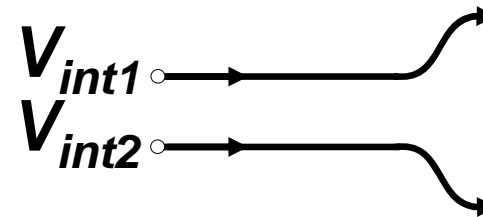


# System Functionality

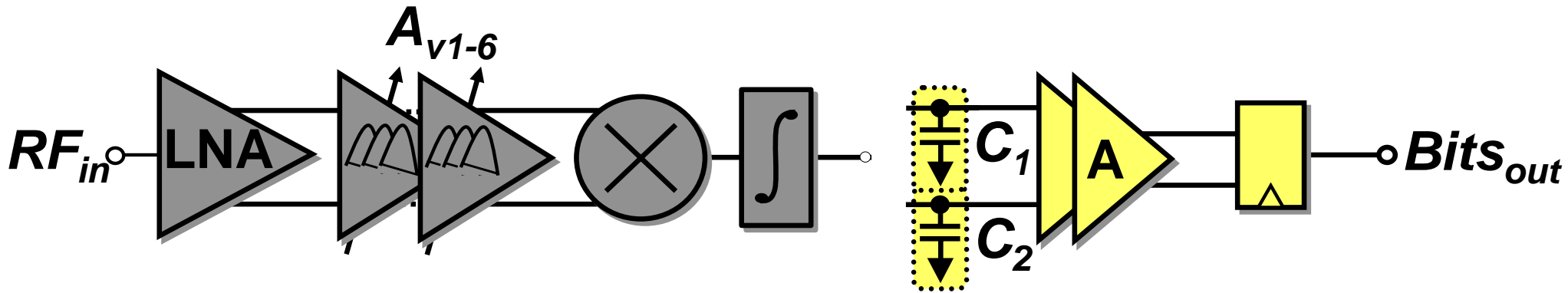
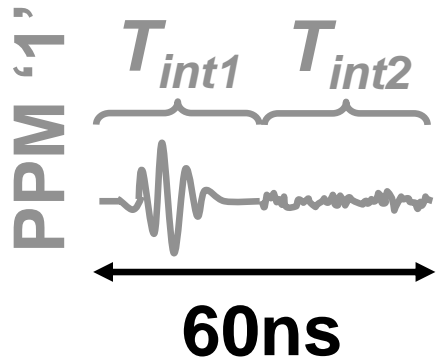


## Relative Compare

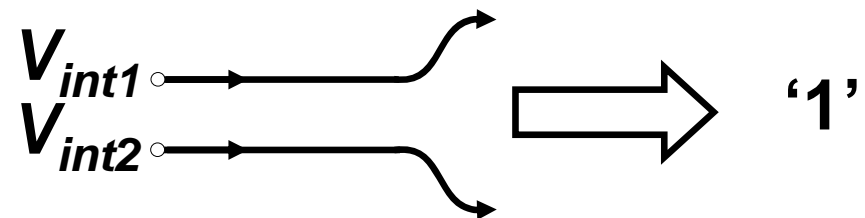
(DC offsets and path non-idealities automatically normalized)



# System Functionality



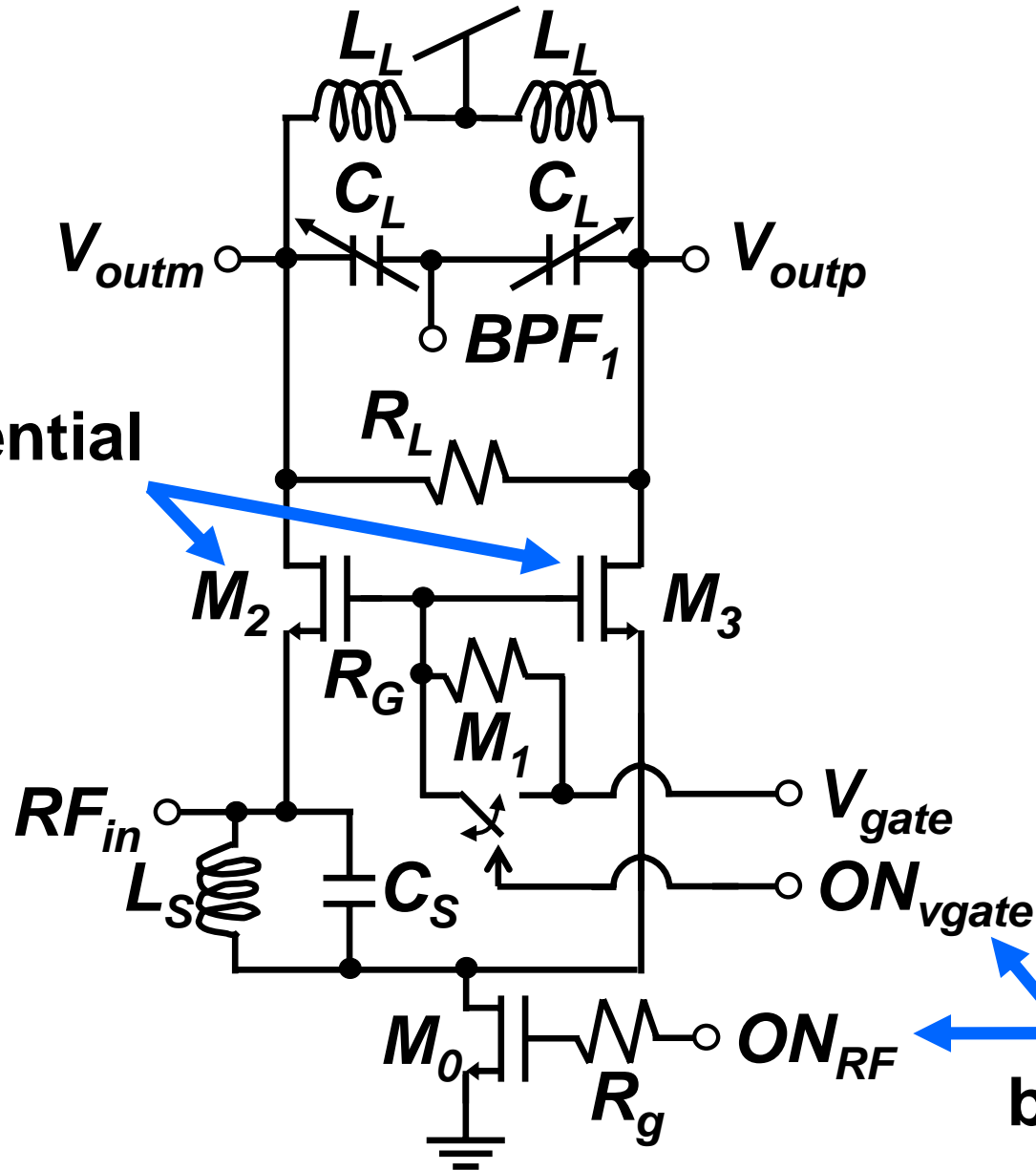
Bit Evaluation





# 0.5V-0.65V LNA

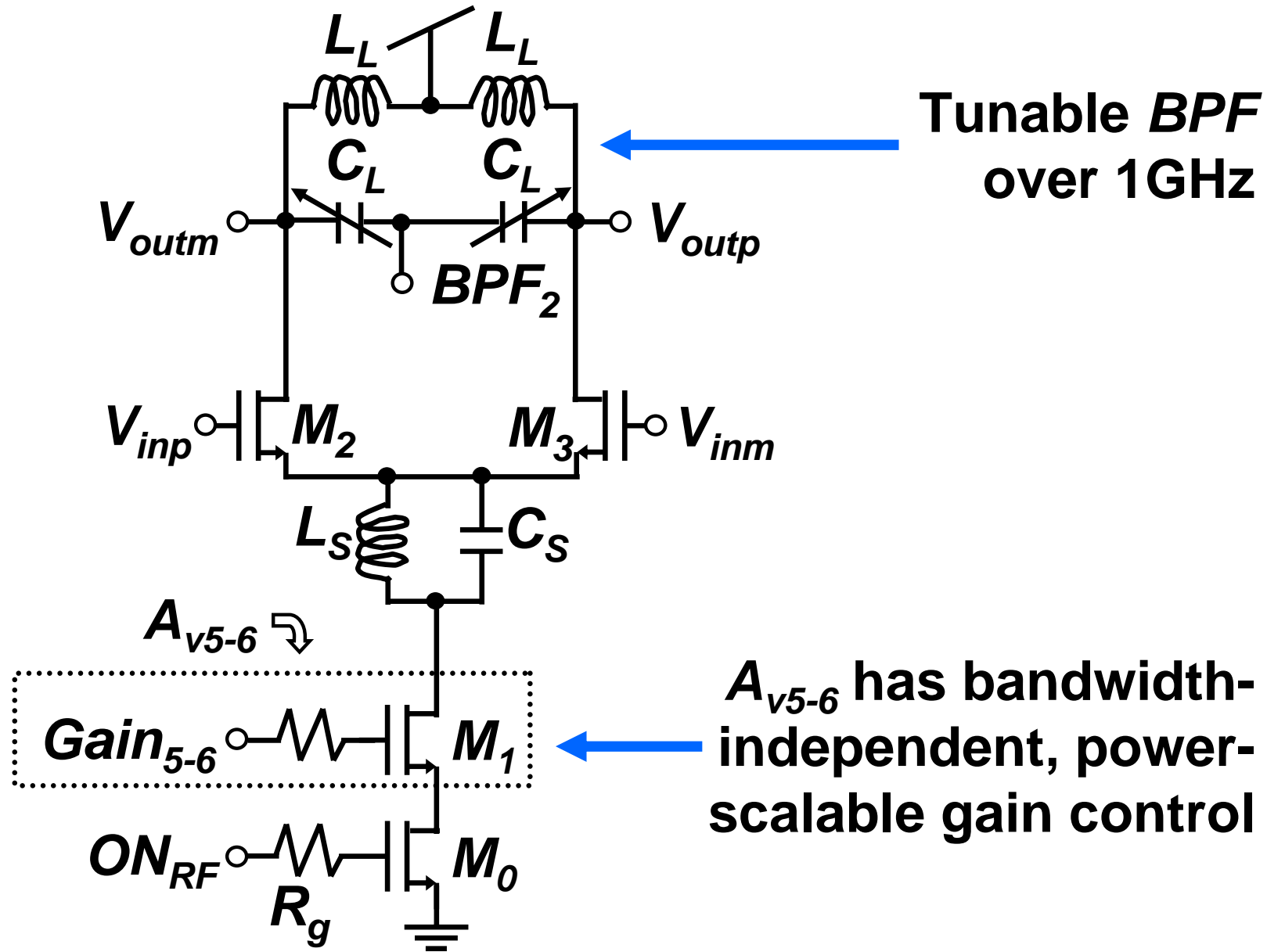
Common-gate  
single-to-differential  
conversion



Dynamically  
biased in ~2ns

# 0.5V-0.65V $A_{V1-6}$

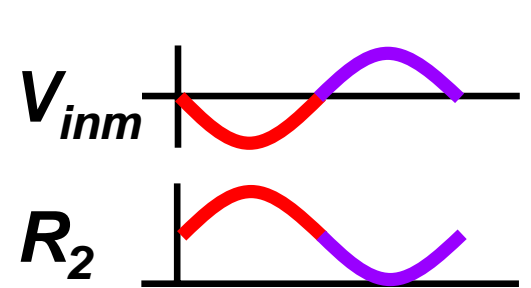
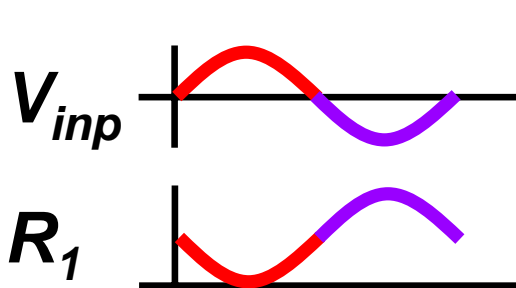
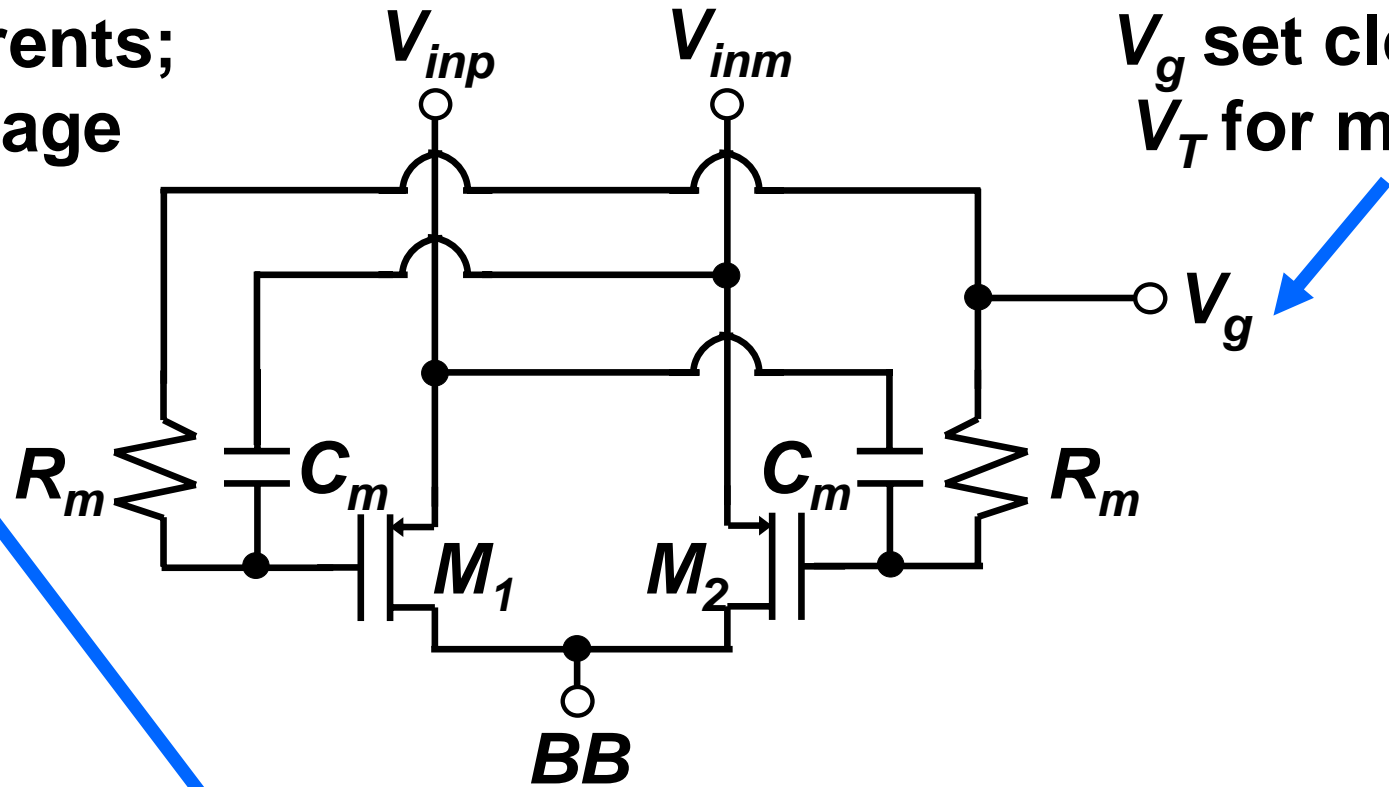
1 of the 6 cascaded  
gain stages



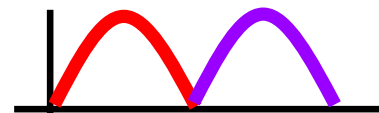
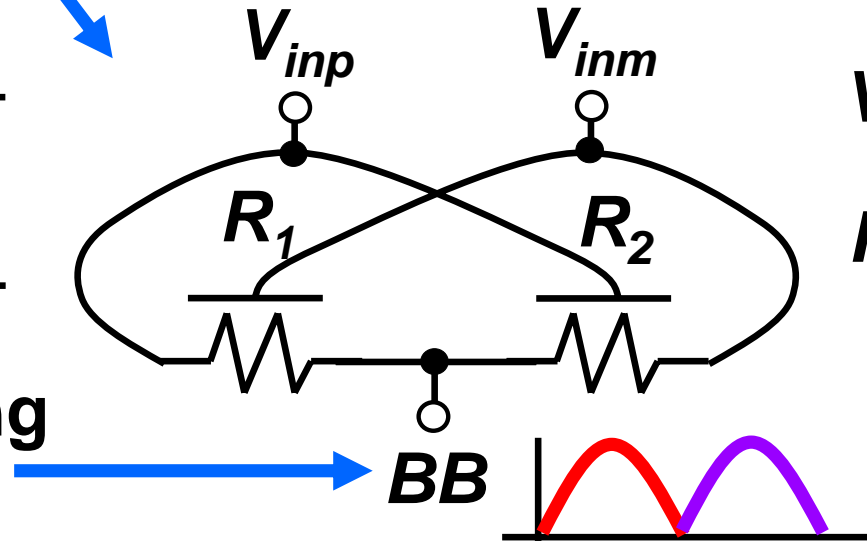
# Passive Self-Mixer

No static currents;  
works as voltage  
divider

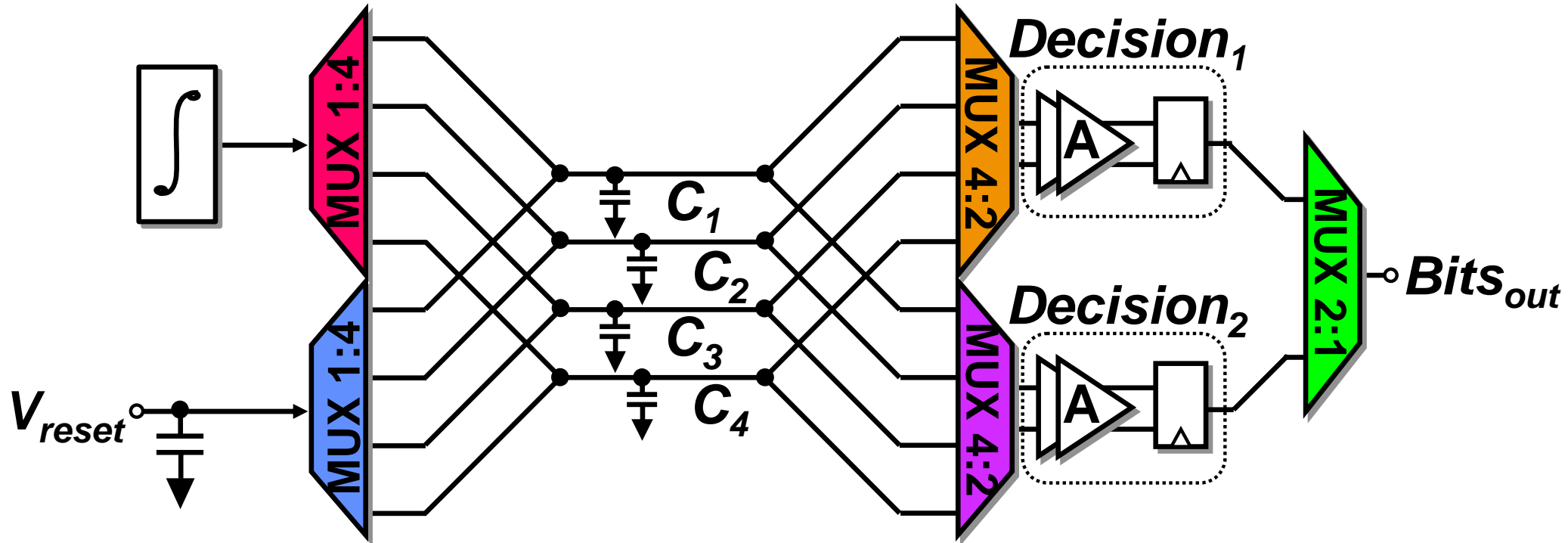
$V_g$  set close to  
 $V_T$  for max  $\Delta R$



Rectified incoming  
RF signal



# High Speed Baseband Demodulator



Integrate to...

Reset to...

*Decision<sub>1</sub>*  
State

*Decision<sub>2</sub>*  
State

$C_1$	$C_2$	$C_3$	$C_4$	$C_1$
$C_2$	$C_3$	$C_4$	$C_1$	$C_2$
$V_{reset}$	$V_{reset}$	Eval Bit $C_1$ & $C_2$	$V_{reset}$	Eval Bit $C_3$ & $C_4$
$V_{reset}$	$V_{reset}$	$V_{reset}$	Eval Bit $C_2$ & $C_3$	$V_{reset}$

...

Time ( $\Delta T = T_{int}$ )

30ns

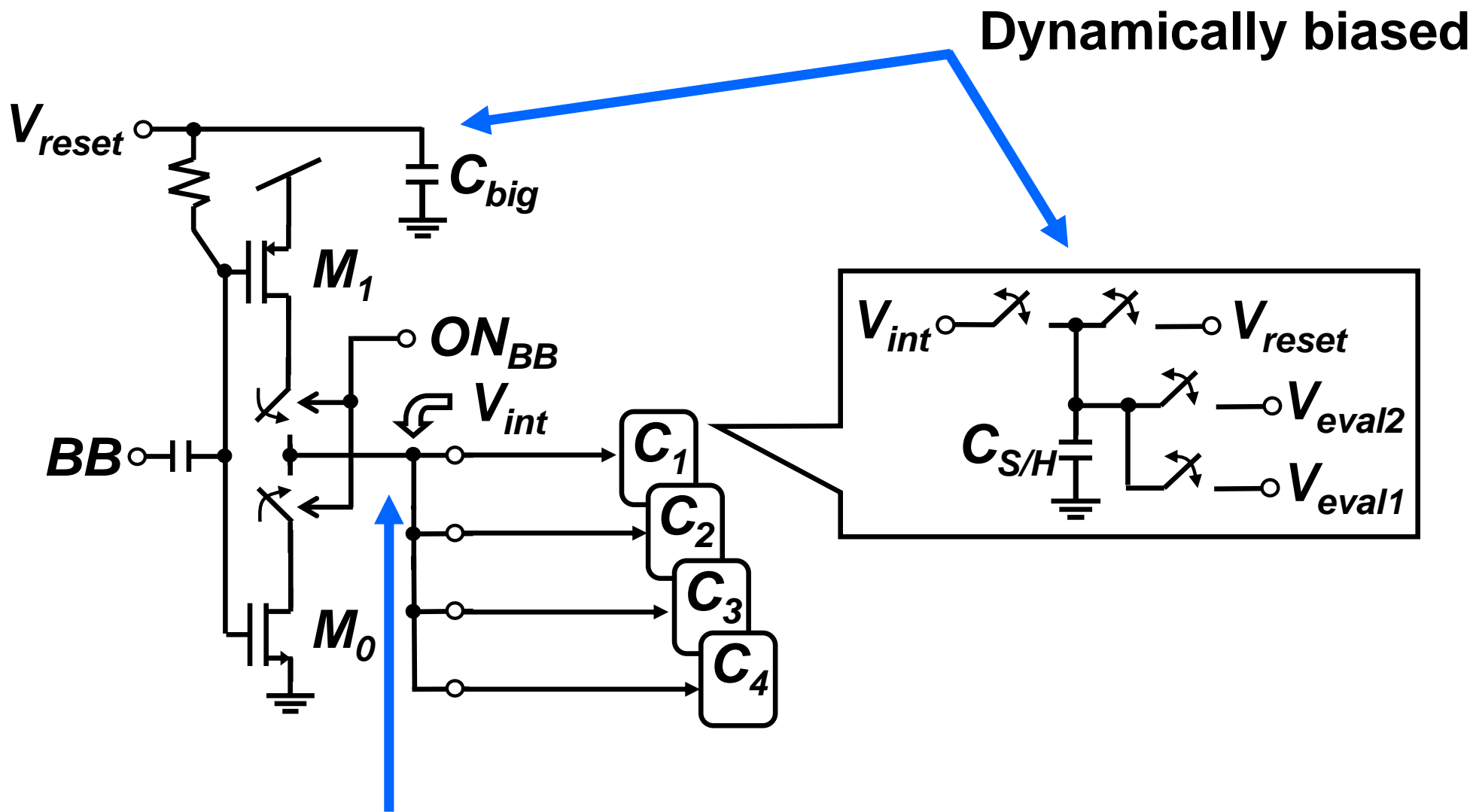
60ns

90ns

120ns

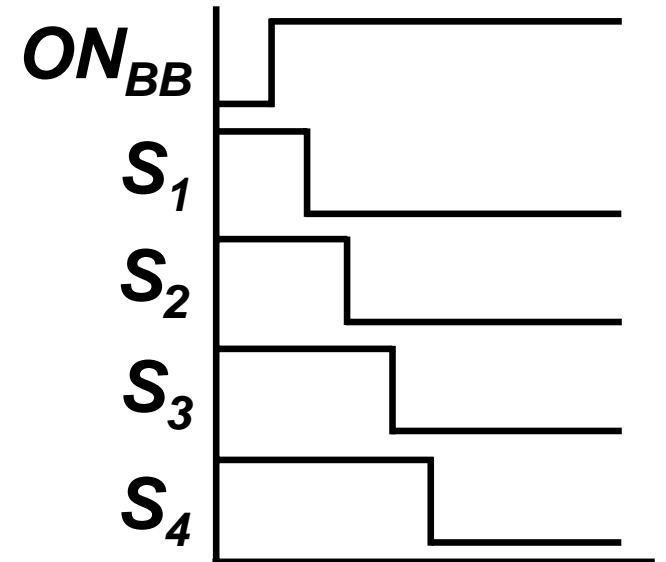
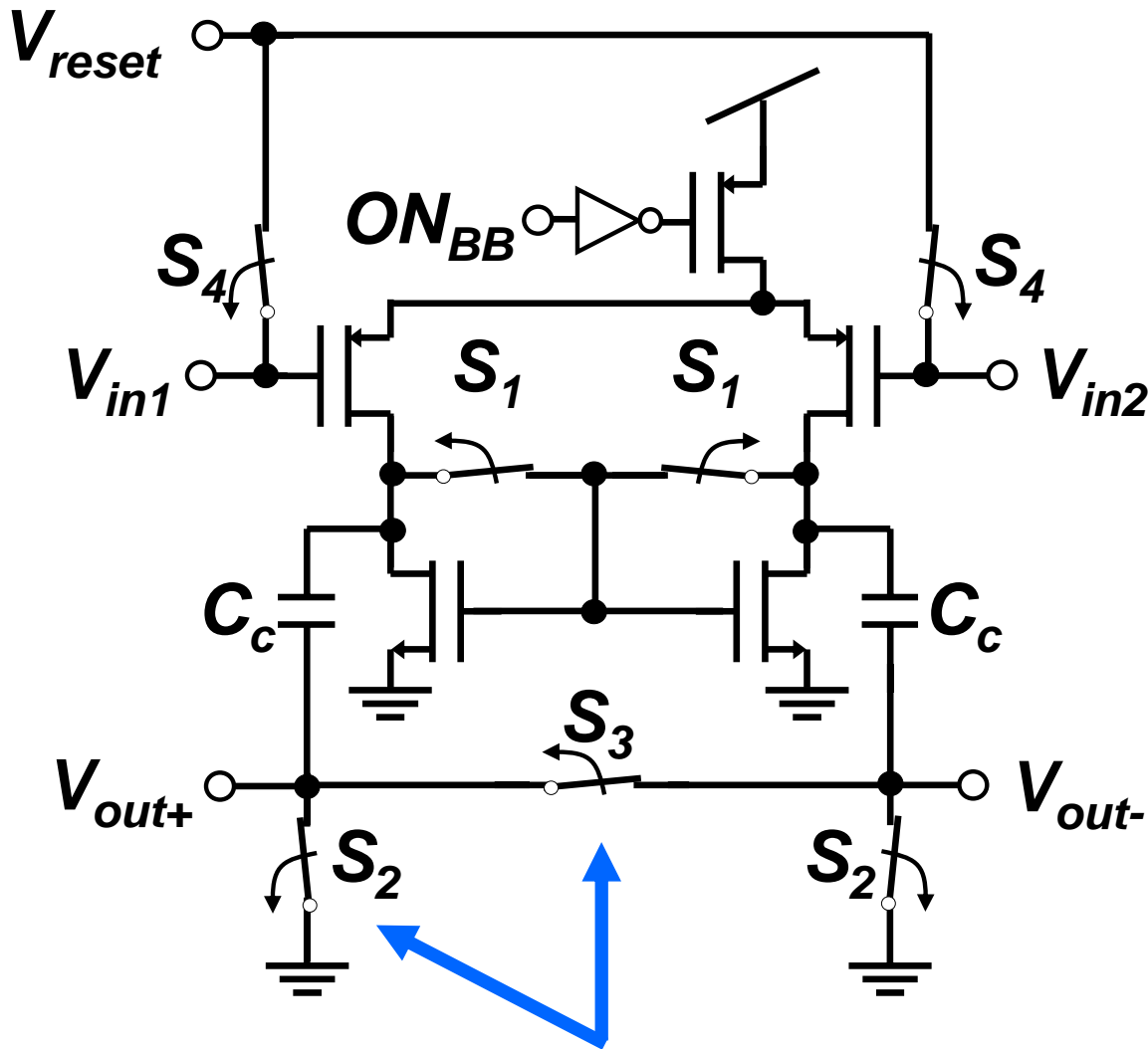
150ns

# 0.5V Integrator



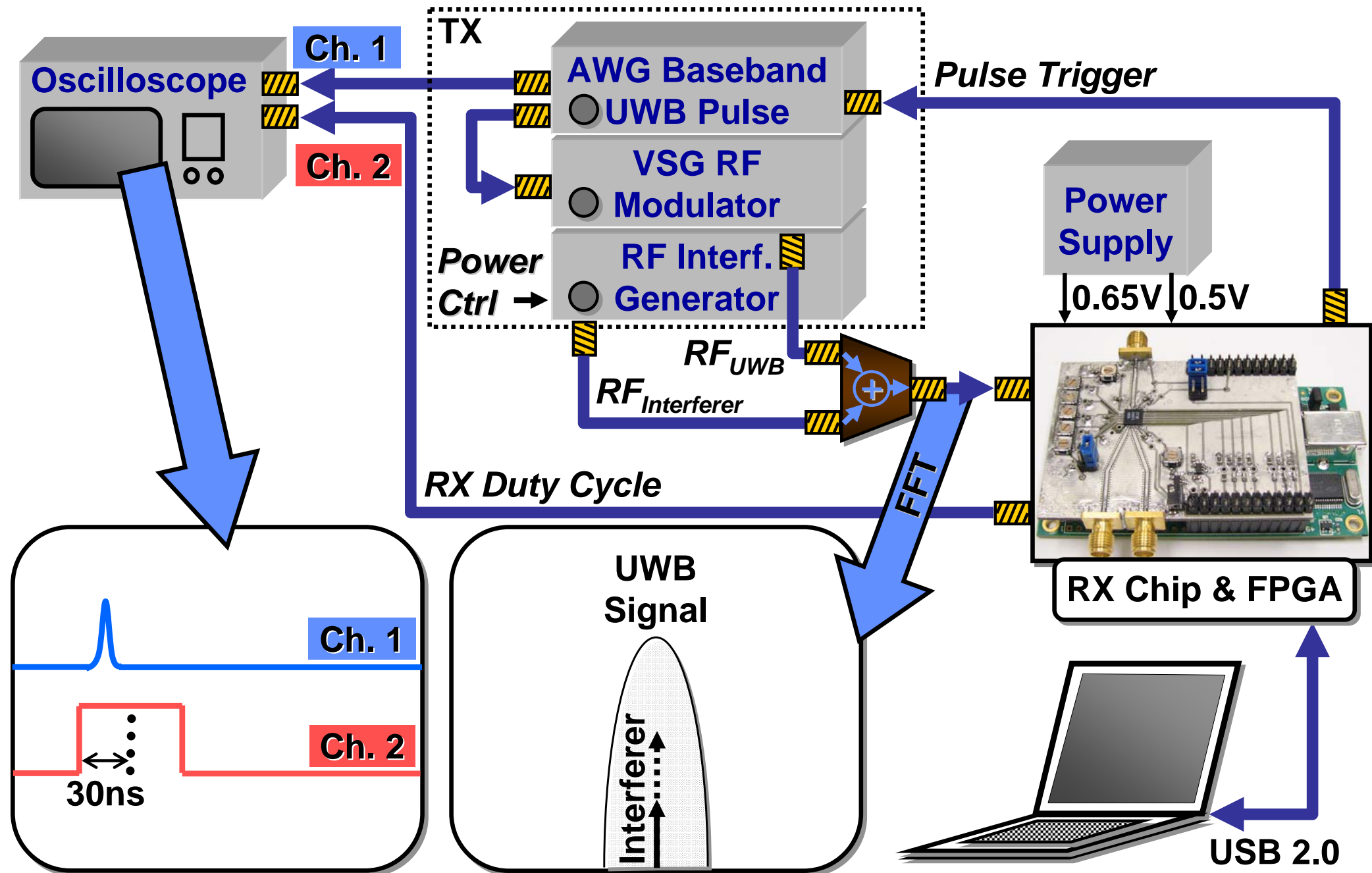
Symmetrically engaged  
for equalized settling

# 0.5V Offset Compensated Preamp

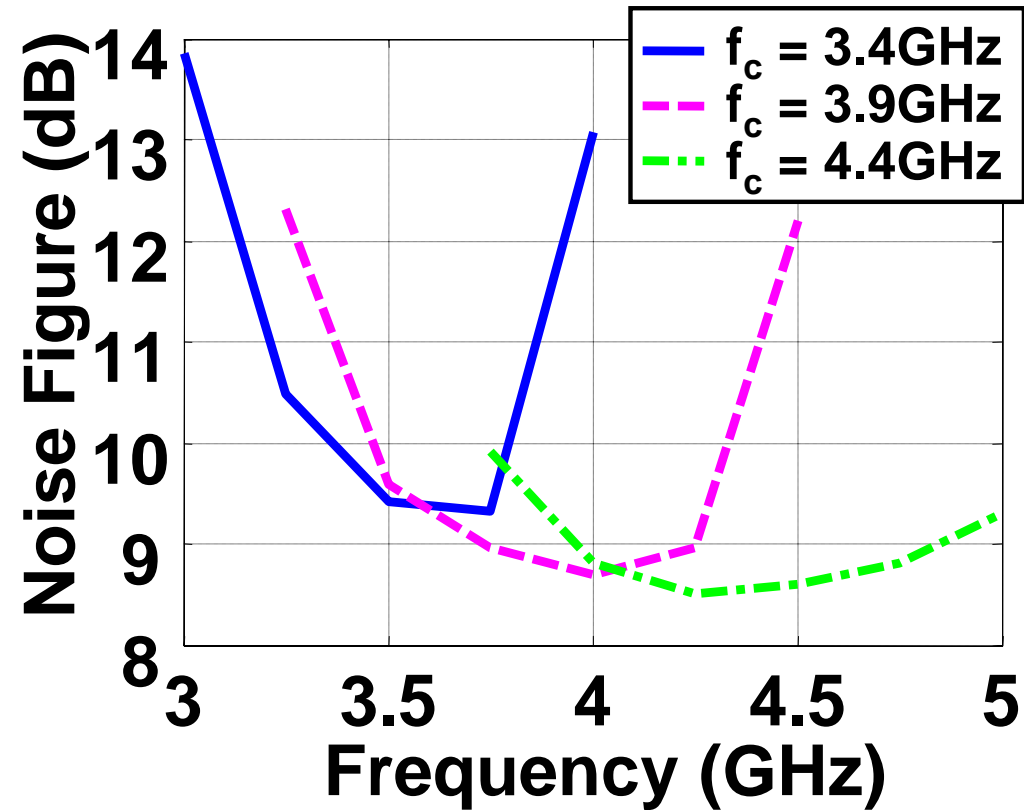
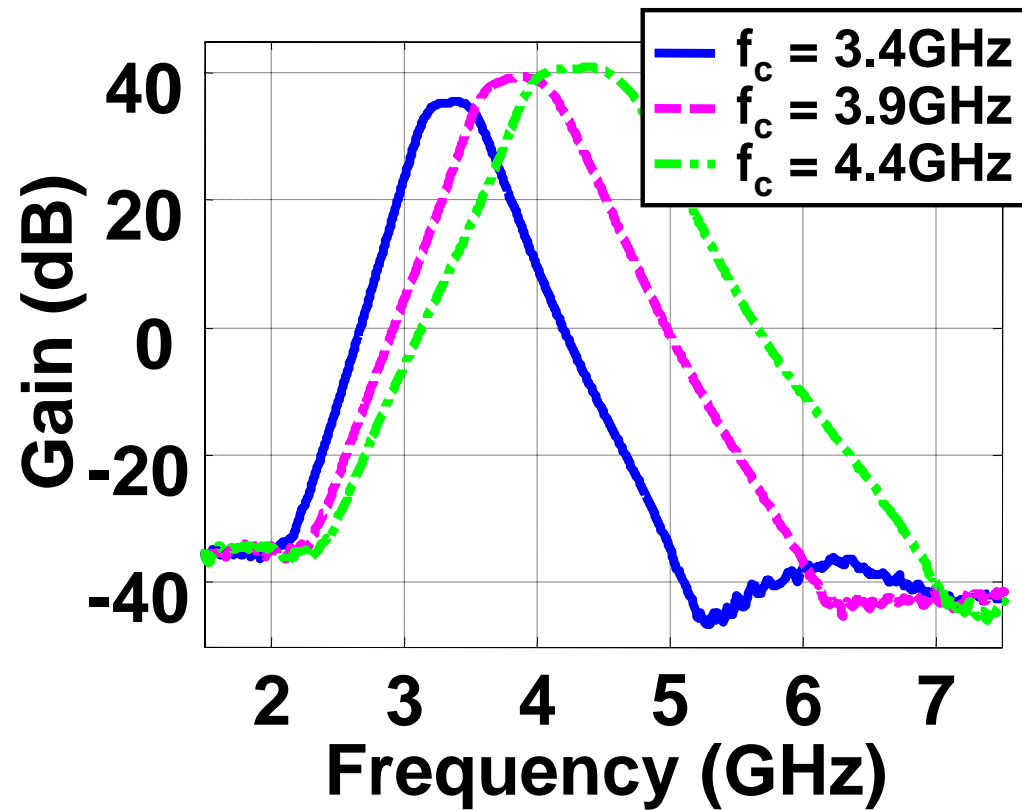


Offset stored on  $C_c$  when switches open

# Measurement Setup



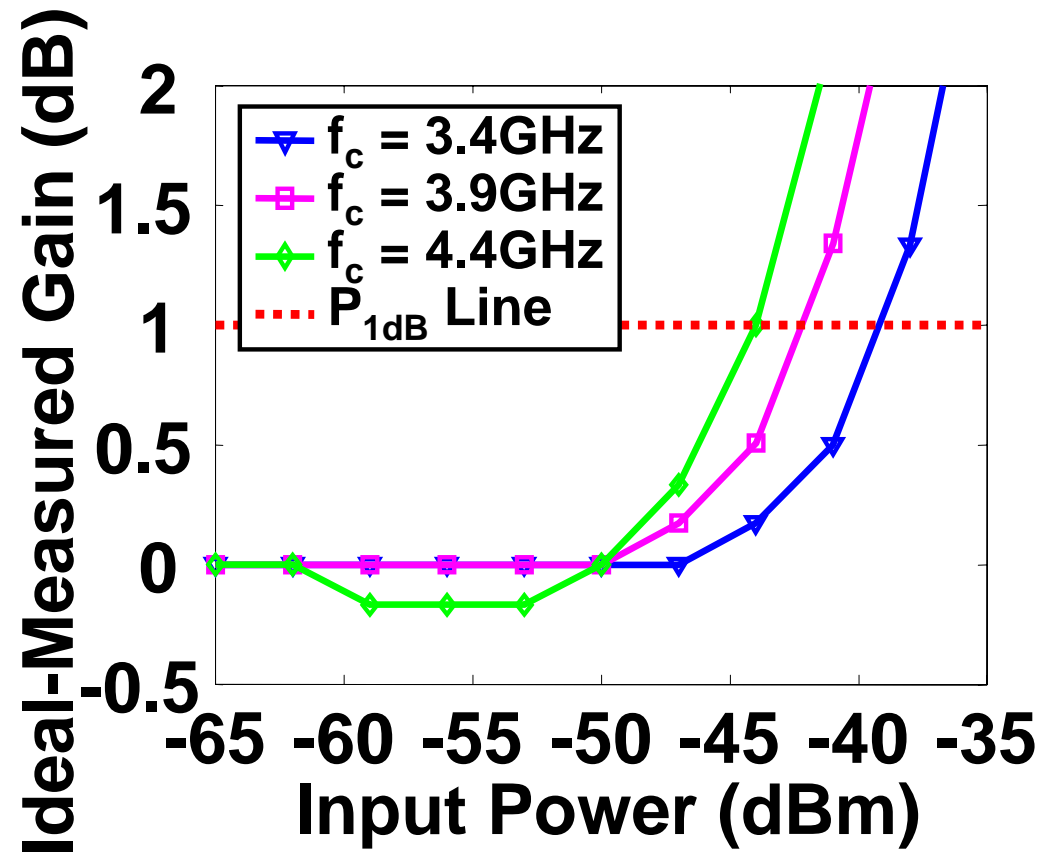
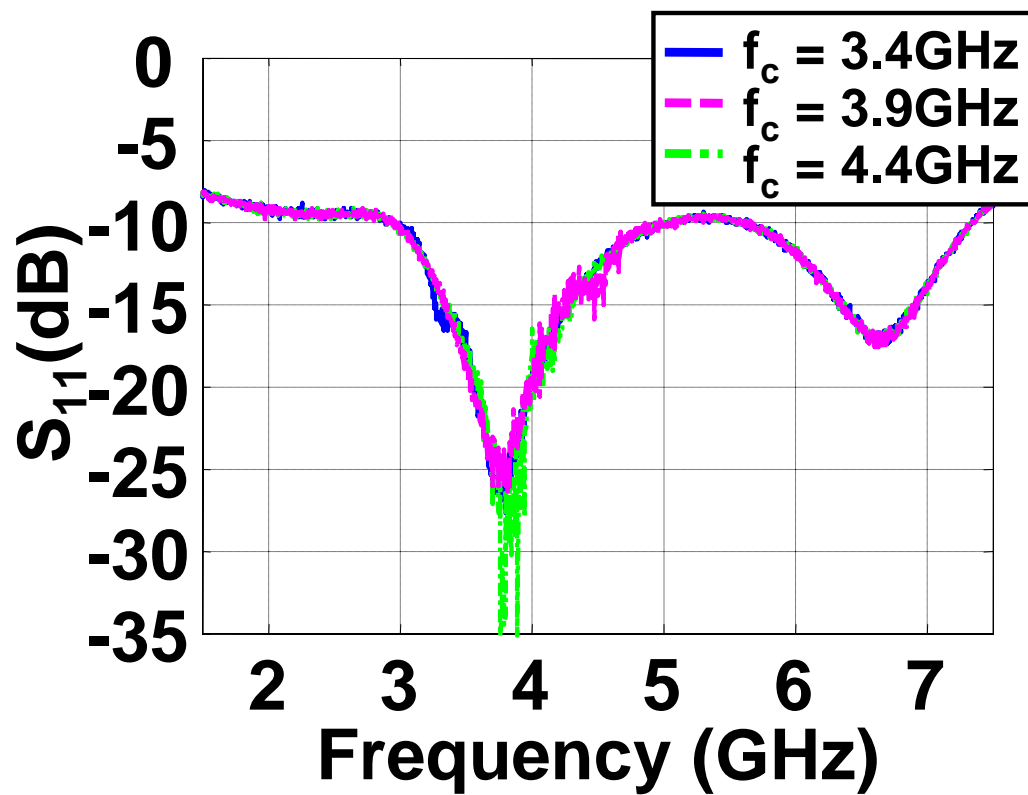
# RF Front-end Measurements



**40dB Gain, 8.6dB NF at 4.4GHz Band**

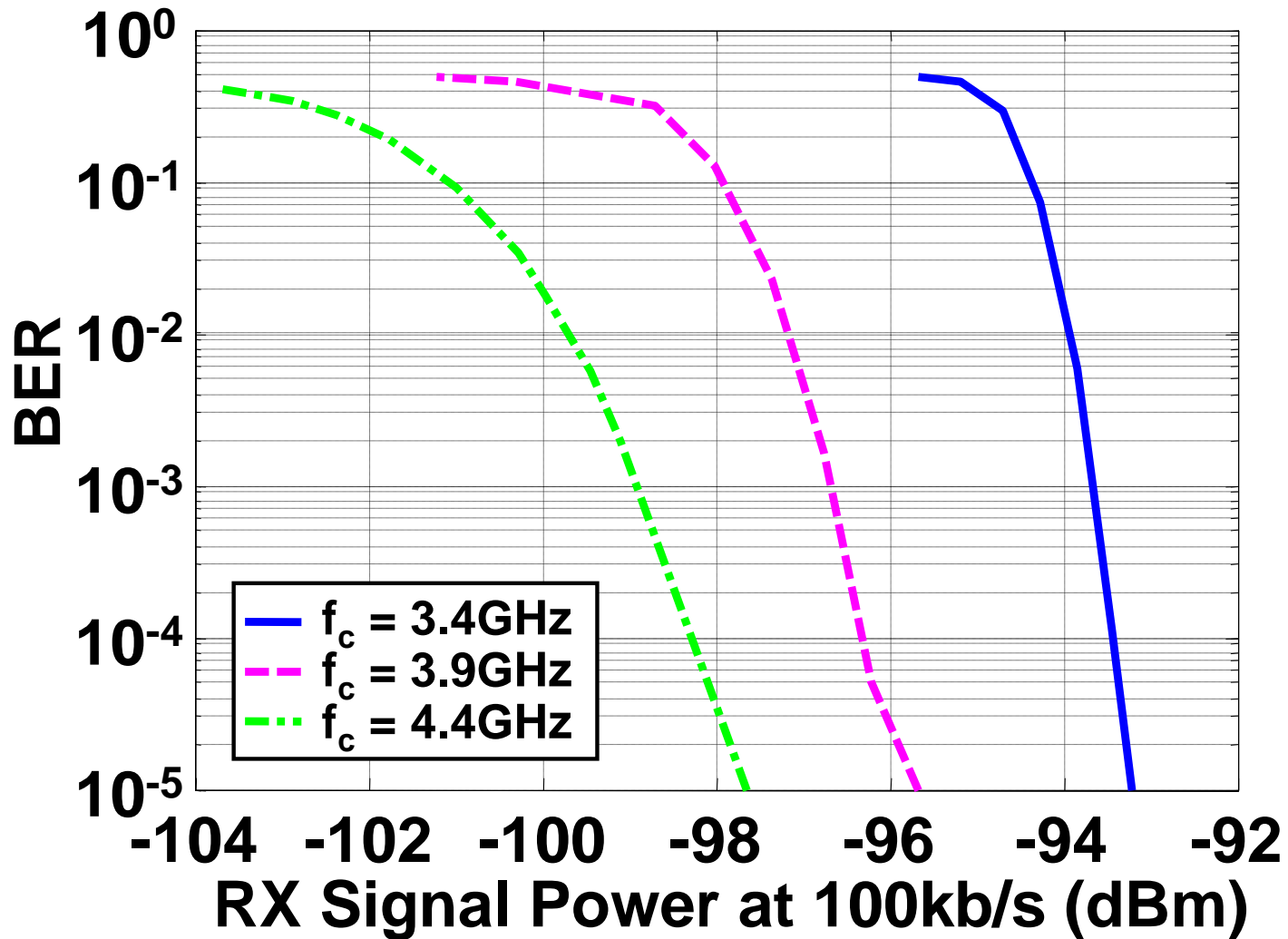


# RF Front-end Measurements



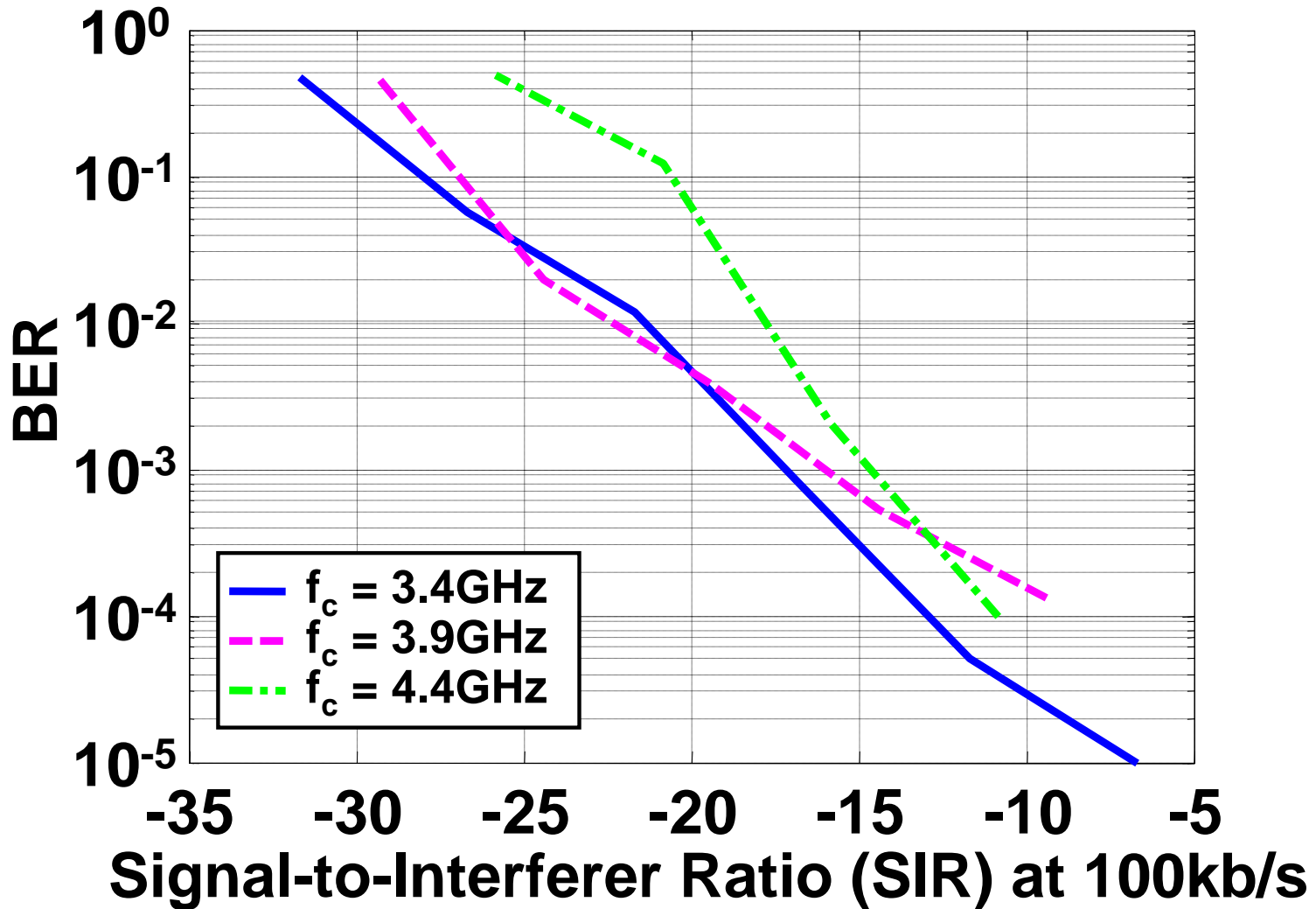
**-10dB  $S_{11}$  in All Bands, -45dBm  $P_{1\text{dB}}$  at Highest Gain**

# Bit Error Rate



**-99dBm Sensitivity for  $10^{-3}$  BER in 4.4GHz Band**

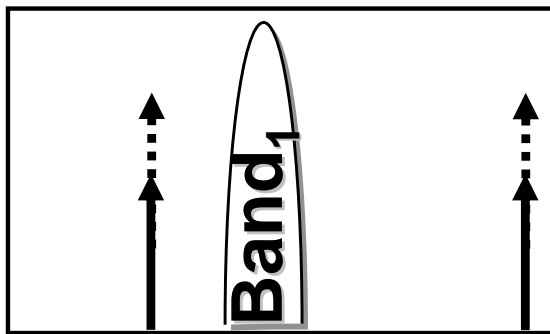
# In-band Interference



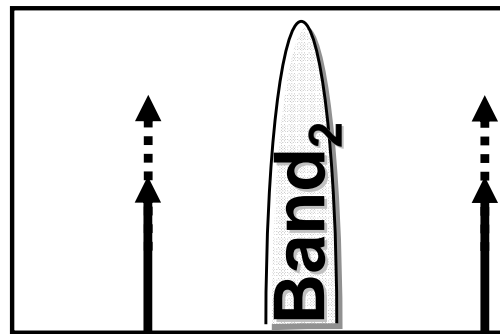
**-15dB SIR for  $10^{-3}$  BER in 4.4GHz Band**

# Out-of-band Interference

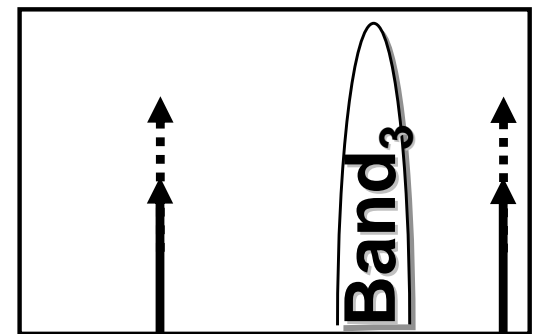
$P_{UWB}$  at  $10^{-5}$  BER Sensitivity



2 3 4 5  
Frequency (GHz)



2 3 4 5  
Frequency (GHz)



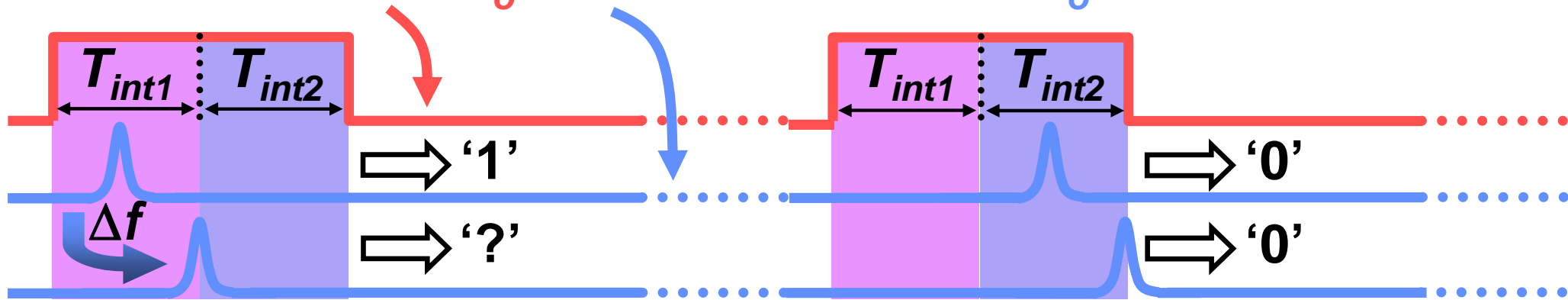
2 3 4 5  
Frequency (GHz)

$f_{interf}$	$P_{interf}$	$10^{-3}$ BER	$f_{interf}$	$P_{interf}$	$10^{-3}$ BER	$f_{interf}$	$P_{interf}$	$10^{-3}$ BER
2.45GHz	-20dBm		2.45GHz	-20dBm		2.45GHz	-20dBm	
5.25GHz	-15dBm		5.25GHz	-15dBm		5.25GHz	-47dBm	

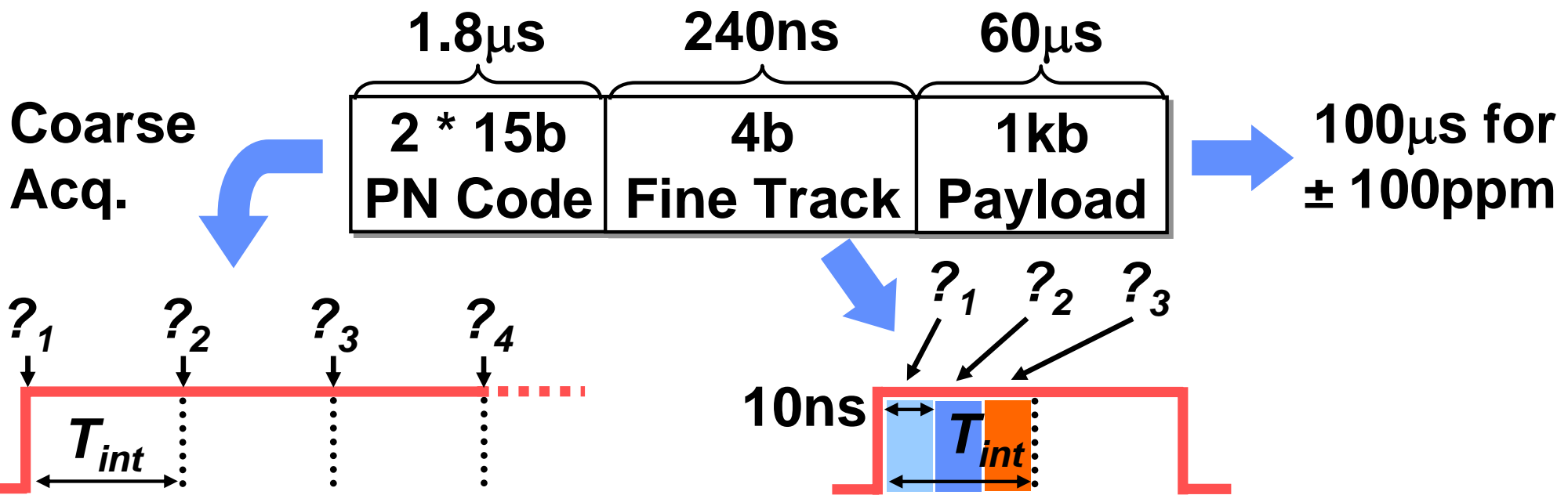
Due to slow  
BPF roll-off

# Acquisition Algorithm (FPGA)

Receiver Clock =  $f_o$  Transmitter Clock =  $f_o + \Delta f$



## Packet Structure



w/ TX in paper 6.4, we achieved 10m wireless demo

# Chip Measurements

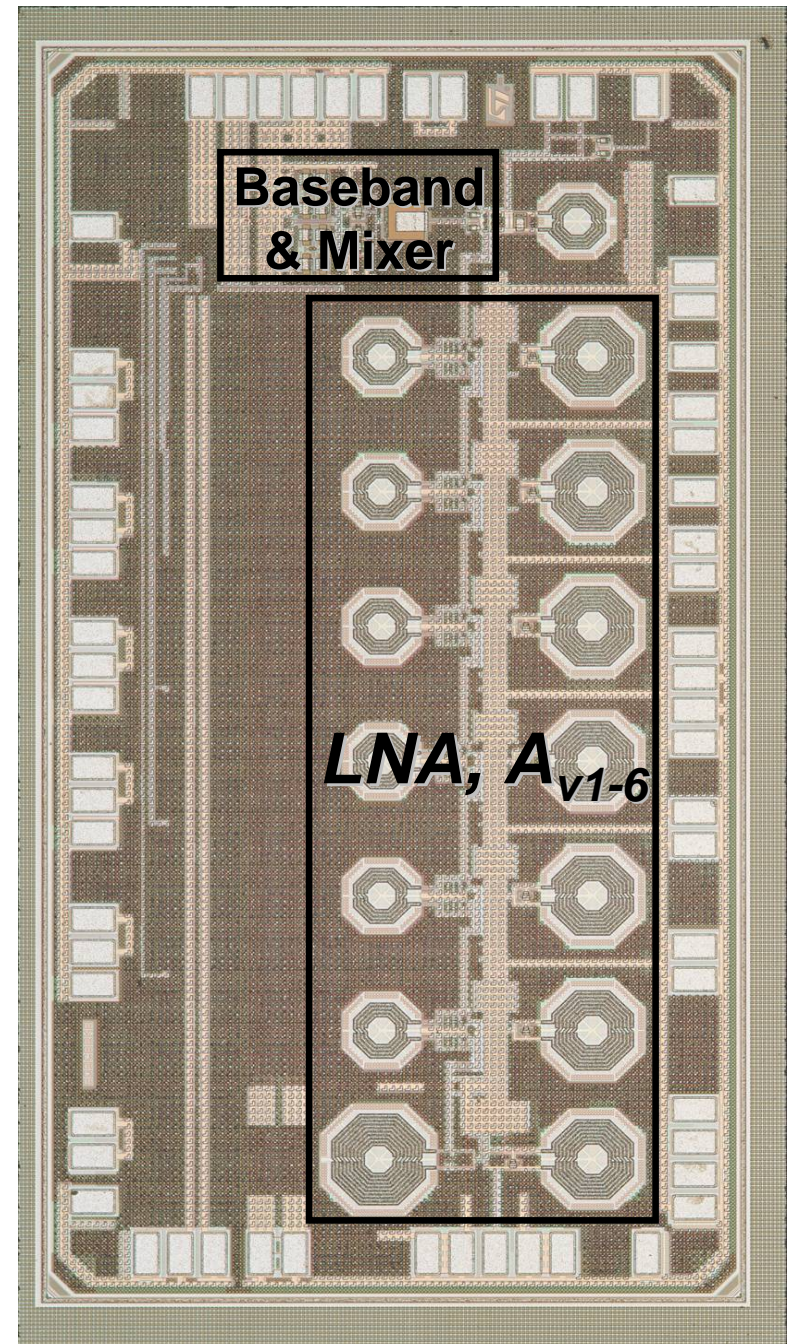
## UWBRX Chip Info

Technology	90nm CMOS
Supply	0.65V
Die size	1mm x 2.2mm
Modulation	PPM
Data Rate	0-16.7Mb/s
Pulse BW	500MHz
$f_c$ subbands	3.4, 3.9, 4.4GHz

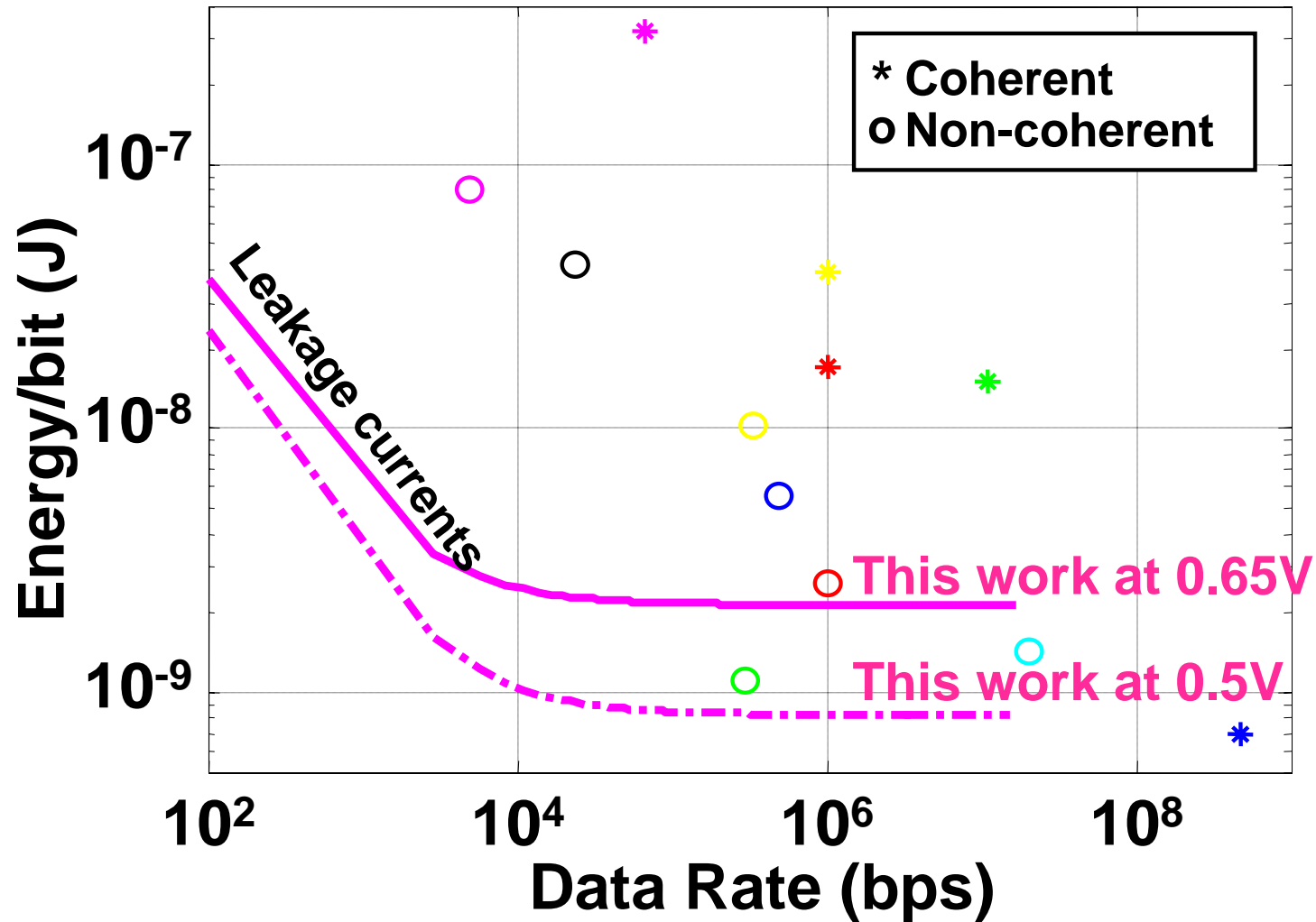
## Measured Results

( $f_c=4.4\text{GHz}$ ,  $T_{int}=30\text{ns}$ , 100kb/s)

Front-end gain	40dB
Front-end NF	8.6dB
Sensitivity ( $10^{-3}$ BER)	-99dBm
In-band SIR for $10^{-3}$ BER	-15dBm
➔ On power (99% in front-end)	35.8mW
Off power (leakage)	$3.5\mu\text{W}$
➔ Turn-on time	$\sim 2\text{ns}$
➔ Energy/bit	2.5nJ/b
$P_{interf}$ at 2.4GHz for $10^{-3}$ BER	-20dBm



# Figure of Merit



**Data Rate Independent  
Low Energy/b Radio**



# Conclusions

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- **Realized a data rate independent 2.5nJ/bit radio. (over 3 orders of magnitude in data rate)**
- **At low data rates, leakage power dominates energy efficiency.**
- **Relative compare backend is a simple demodulator and also normalizes DC offsets and pre-integrator path non-idealities.**
- **-99dBm of sensitivity for  $10^{-3}$  BER at 100kb/s is achieved with this receiver.**

Acknowledgements – MARCO/DARPA Focus Center for Circuits and Systems Solutions (C2S2), National Science Foundation (NSF), and STMicroelectronics for chip fabrication.