6.3 A 2.5nJ/b 0.65V 3-to-5GHz Subbanded UWB Receiver in 90nm CMOS

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With portable electronics and wireless sensor networks becoming increasingly pervasive, energy efficient radios have become an active area of research [1-3]. A critical figure of merit (FOM) for measuring radio efficiency in such applications is energy per bit. Though sub-nJ/b data reception is achievable for data rates >100Mb/s using optimized coherent architectures [4], there is a need for simple, low-cost, low-power, and scalable radios as specified in the IEEE 802.15.4a standard [5]. This work explores the unique properties of FCC-compliant pulsed UWB signals and scaled CMOS devices to improve energy per bit of existing low-data-rate GHz-range integrated radios.

Pulse-position modulation (PPM) signaling is shown in Fig. 6.3.1. For a maximum data rate of 16.7Mb/s, T_{frame} = 60ns and 1 bit is encoded in each frame. A '1' is received if a pulse appears during T_{int1}, and a '0' is received if a pulse appears during T_{int2}. Thus, the receiver needs to be on only during the two time windows in which a pulse may appear. Although the 500MHz pulses are only 2ns wide, T_{int} is set to 30ns for the receiver to have greater robustness to crystal frequency offset and varying channel impulse responses.

Figure 6.3.1 also shows a simplified block diagram of the proposed non-coherent receiver architecture that is comprised of a 3-to-5GHz subbanded RF front-end, a passive self-mixer, and a low-power mixed-signal baseband. The non-coherent architecture does not require a PLL. For out-of-band noise/interference robustness, the RF front-end performs channel selection in the 3.4, 3.9, and 4.4GHz bands. For bit-slicing, a low-power sample-and-hold capacitor network stores analog integration results during T_{int1} and T_{int2} onto separate capacitors C_1 and C_2, respectively. Thereafter, two offset-compensated preamps and a latch perform a relative comparison on the two capacitor voltages to evaluate the received bit. To achieve rapid coarse acquisition in the preamble, adjacent integrations for continuous bit decisions are needed. The four capacitors used in this implementation are rotated among three states – *reset, integrate,* and *evaluate bit* – to achieve integrations every T_{int}. Figure 6.3.2 shows the baseband block diagram and the corresponding operation schedule. Two offset-compensated relative-compare paths ($Decision_1$ and $Decision_2$) swap between *evaluate* and *reset* modes to provide a continuous stream of bit decisions. Because the baseband can resolve a bit 45ns after integration and the receiver can power on/off in 2ns, the RF front-end and baseband circuits are aggressively duty cycled between PPM symbols with PD_{RF} and PD_{BB} (Fig. 6.3.1) to achieve 2.5nJ/b. The fastest clock required to operate the entire receiver is $1/T_{int}$, or 33.3MHz.

For low power operation, the supply voltage is set to 0.65V. Low-voltage circuit techniques are employed in the receiver to meet performance requirements. Seven cascaded LNA stages provide sufficient gain to overcome the $V_{out} = kV^2_{in}$ transfer characteristic of the self-mixer for small inputs (Fig. 6.3.3). The cascaded LNAs and passive mixer are DC coupled and chain-biased so that switching M_0 for duty-cycling does not cause long-settling transients. M_0 is sized 2× the minimum length to improve $I_{on}/I_{leakage}$. MOS varactor C_L and differential inductor L_L form a tunable 0V BPF load. LNA_1 is inherently ESD robust, and converts its single-ended input to differential signal using back-to-back common-gate differential amplifiers. The high CMRRs of LNA_2 to LNA_7 equalize the conversion. A passive 2-transistor mixer with gate and drain inputs is chosen so that the nonlinearity in MOS transistors is exploited at the common source node to minimize mixer losses for small-signal RF and LO inputs in a low voltage environment.

At baseband, the integrator, sample-and-hold capacitor banks, and offset-compensated preamplifier stages are all designed for 0.65V operation. The integrator is an inverter that is DC biased at the switching threshold. The integration transistors are non-minimum length to achieve greater DC gain. Since prior to integration, all signals pass through the same RF front-end, mixer, and integrator, the relative-compare paths (for bit decisions) effectively normalize DC offsets, slow-varying interference and other pre-integrator path non-idealities that are common to both time integrations. The offset voltage of the final latch in each decision path affects BER of this demodulation scheme dramatically, and is mitigated by cascading two offset-compensated preamplifiers.

Figure 6.3.4 shows the measured RF gain response of the RF front-end in each of the three bands. The RF front-end provides up to 40dB of gain. In the 3.4, 3.9, and 4.4GHz bands the –3dB bandwidth varies from 430 to 715MHz. BER measurements are taken when the system is manually synchronized. When the receiver is nominally at 10^{-5} BER sensitivity, the BER in all bands is degraded to 10^{-3} in the presence of an out-of-band –20dBm 2.4GHz ISM band interferer. The same BER degradation occurs in the lower two bands when a –15dBm 5.25GHz ISM signal is present. The 4.4GHz band suffers the same BER loss with a –47dBm 5.25GHz signal, since the BPF is still rolling off at 5.25GHz.

Figure 6.3.5 shows measured sensitivity at 100kb/s. For this data rate, the sensitivity for 10^{-3} BER is -99dBm at the 4.4GHz band. Because the three bands have different gains, the curves are each shifted corresponding to those gain differences. Since downconversion is done through a self-mixer whose conversion gain is proportional to the input signal amplitude, the BER waterfall curves have a steep roll-off. The SIR performance of the receiver is measured when a worst-case in-band interference tone is placed at the center of each band. The interference power is then swept to measure the effect on BER when the receiver is nominally at a 100kb/s, 10^{-5} BER sensitivity. A –15dB SIR requirement to maintain a 10^{-3} BER for all bands is observed. To prove that this receiver architecture and relative-compare PPM demodulation scheme is viable, a full synchronization algorithm is implemented and verified in an FPGA that interfaces to the receiver.

A table summarizing the performance of the 0.65V non-coherent radio receiver fabricated in a 90nm CMOS process is shown in Fig. 6.3.6. The FCC-compliant receiver achieves –99dBm sensitivity with 10^{-3} BER at 100kb/s. Energy per bit is 2.5nJ/b for 0.01-to-16.7Mb/s data rates, and is limited only by leakage power as data rate decreases. The chip area is 1×2.2mm^2 (Fig. 6.3.7).

Acknowledgements:
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References:
[1] B. Otis and J. Rabaey, "A 400μW-RX 1.6mW-TX Super-Regenerative Receiver at 1GHz," *ISSCC Dig. Tech. Papers*, pp. 396-397, Feb., 2005.
[2] B. Cook, A. Berny, A. Molnar, et al., "An Ultra-Low Power 2.4GHz RF Transceiver for Wireless Sensor Networks in 0.13μm CMOS with 400mV Supply and an Integrated Passive RX Front-End," *ISSCC Dig. Tech. Papers,* pp. 370-371, Feb. 2006.
[3] J. Ryckaert, M. Badaroglu, V. De Heyn, et al., "A 16mA UWB 3-to-5 GHz 20Mpulses/s Quadrature Analog Correlation Receiver in 0.18μm CMOS," *ISSCC Dig. Tech. Papers,* pp 114-115, Feb., 2006.
[4] T. Aytur, H-C. Kang, R. Mahadevappa, et al., "A Fully Integrated UWB PHY in 0.13μm CMOS," *ISSCC Dig. Tech. Papers,* pp. 124-125, Feb., 2006.
[5] http://www.ieee802.org/15/pub/TG4a.html.

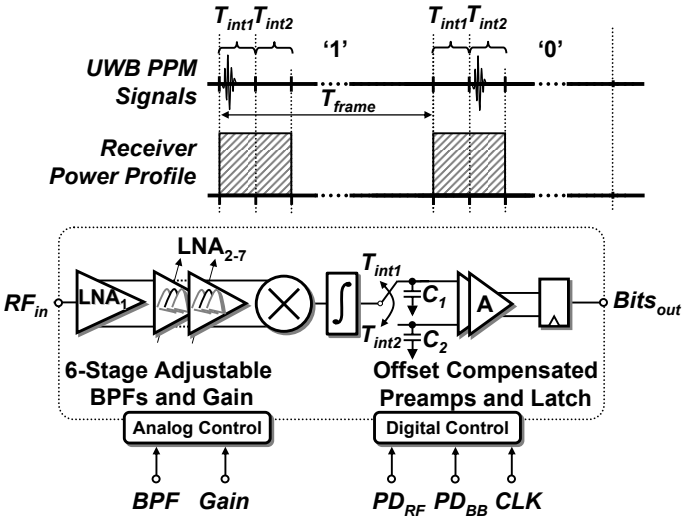

Figure 6.3.1: UWB PPM signaling and simplified receiver block diagram.

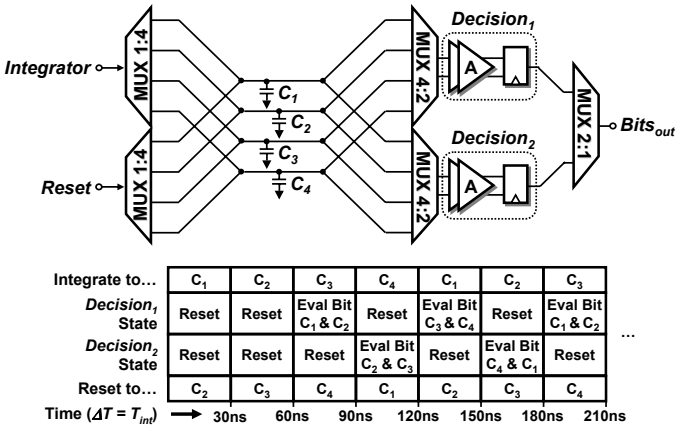

Figure 6.3.2: Implemented baseband for rapid coarse acquisition and the corresponding operation schedule.

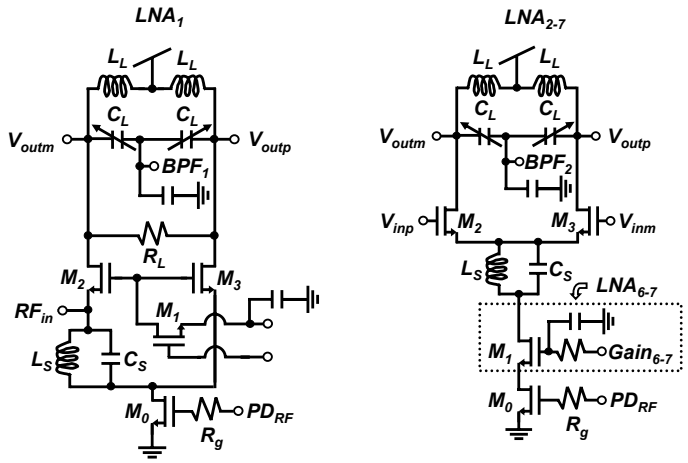

Figure 6.3.3: LNA schematics.

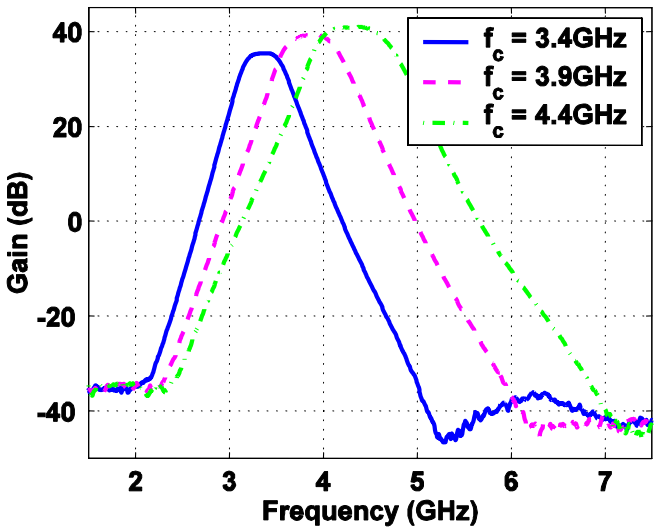

Figure 6.3.4: RF front-end transfer functions for the three UWB bands.

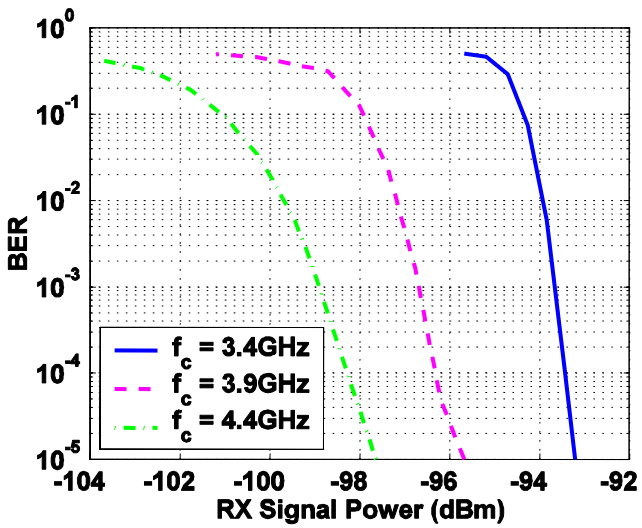

Figure 6.3.5: BER versus RX signal power at 100kb/s.

UWBRX Chip Info

Technology	90nm CMOS
Supply	0.65V
Die size	1mm x 2.2mm
Modulation	PPM
Datarate	0–16.7Mb/s
Pulse BW	500MHz
f_c subbands	3.4GHz, 3.9GHz, 4.4GHz

Measured Results (f_c=4.4GHz, T_{int}=30ns, 100kb/s)

Front-end gain	40dB
Front-end NF	8.6dB
Sensitivity (10^{-3} BER)	-99dBm
In-band SIR for 10^{-3} BER	-15dB
Instantaneous power	35.8mW
Leakage power	3.5μW
Turn-on time	~2ns
Energy/bit	2.5nJ/b
P_{interf} at 2.4GHz for 10^{-3} BER	-20dBm

Figure 6.3.6: Chip performance summary.

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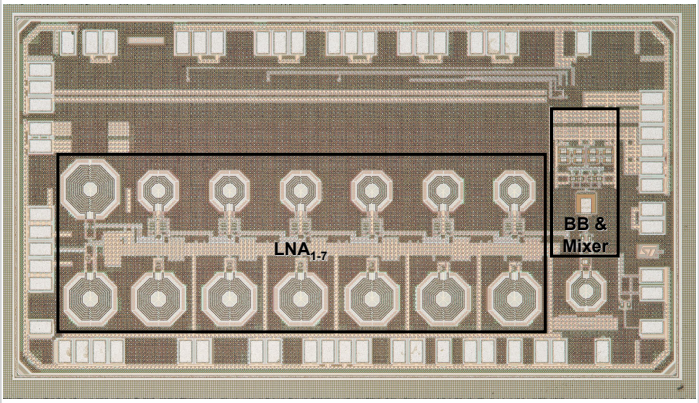

Figure 6.3.7: Chip micrograph.

