

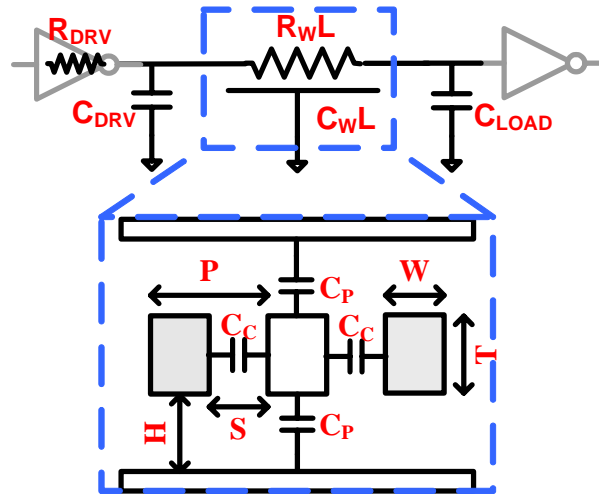
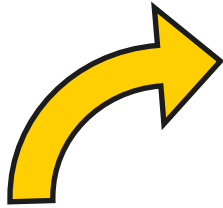
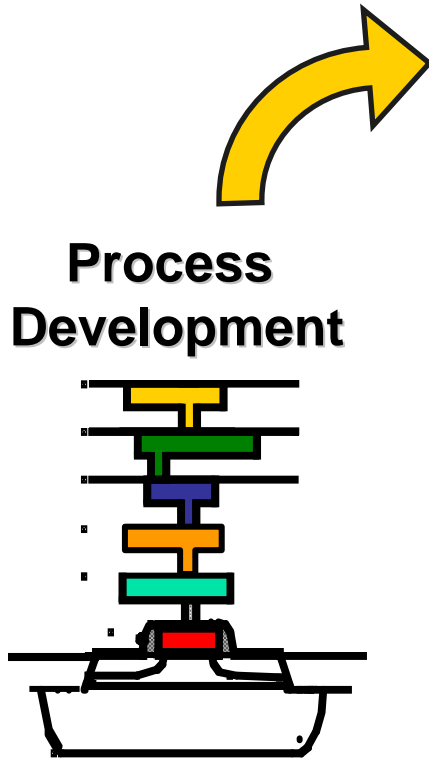
Scaling and Evaluation of Carbon Nanotube Interconnects for VLSI Applications

Fred Chen, Ajay Joshi,
Vladimir Stojanović, Anantha Chandrakasan

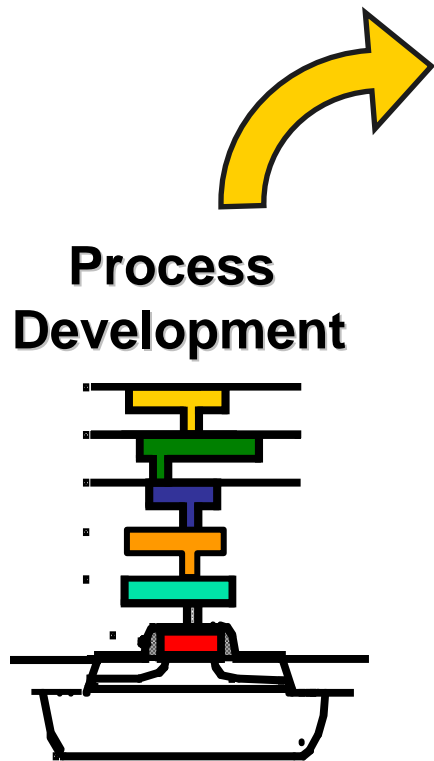
Massachusetts Institute of Technology
Department of Electrical Engineering & Computer Science

Technology Design Flow

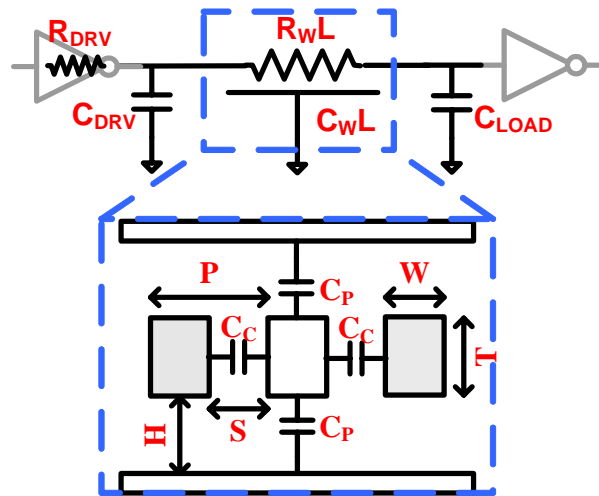
Create Models for Circuits



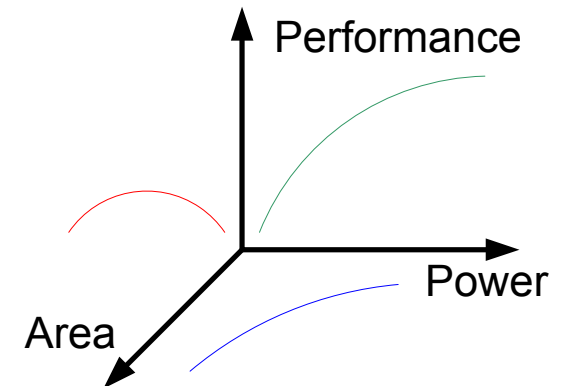
Technology Design Flow



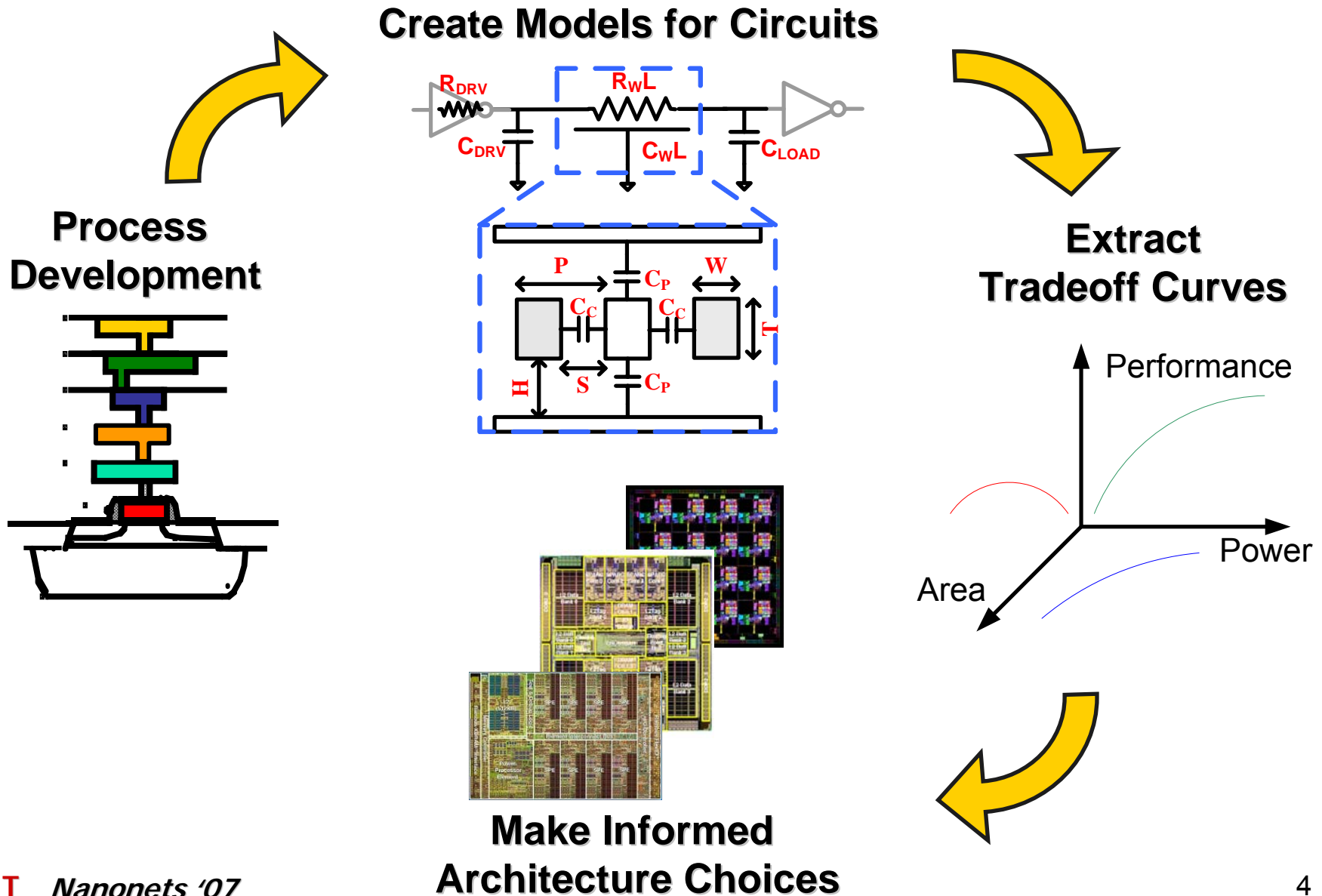
Create Models for Circuits



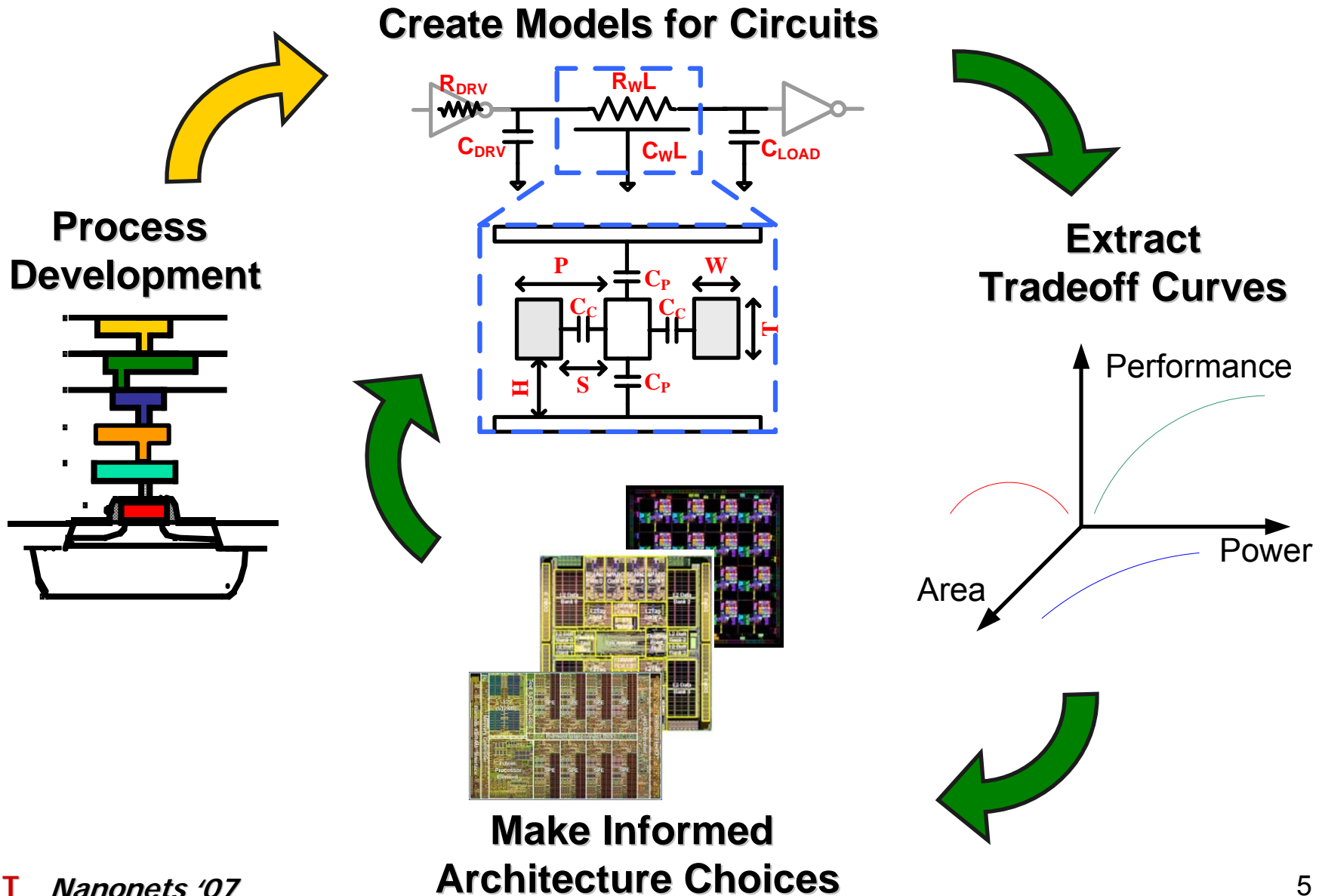
Extract Tradeoff Curves



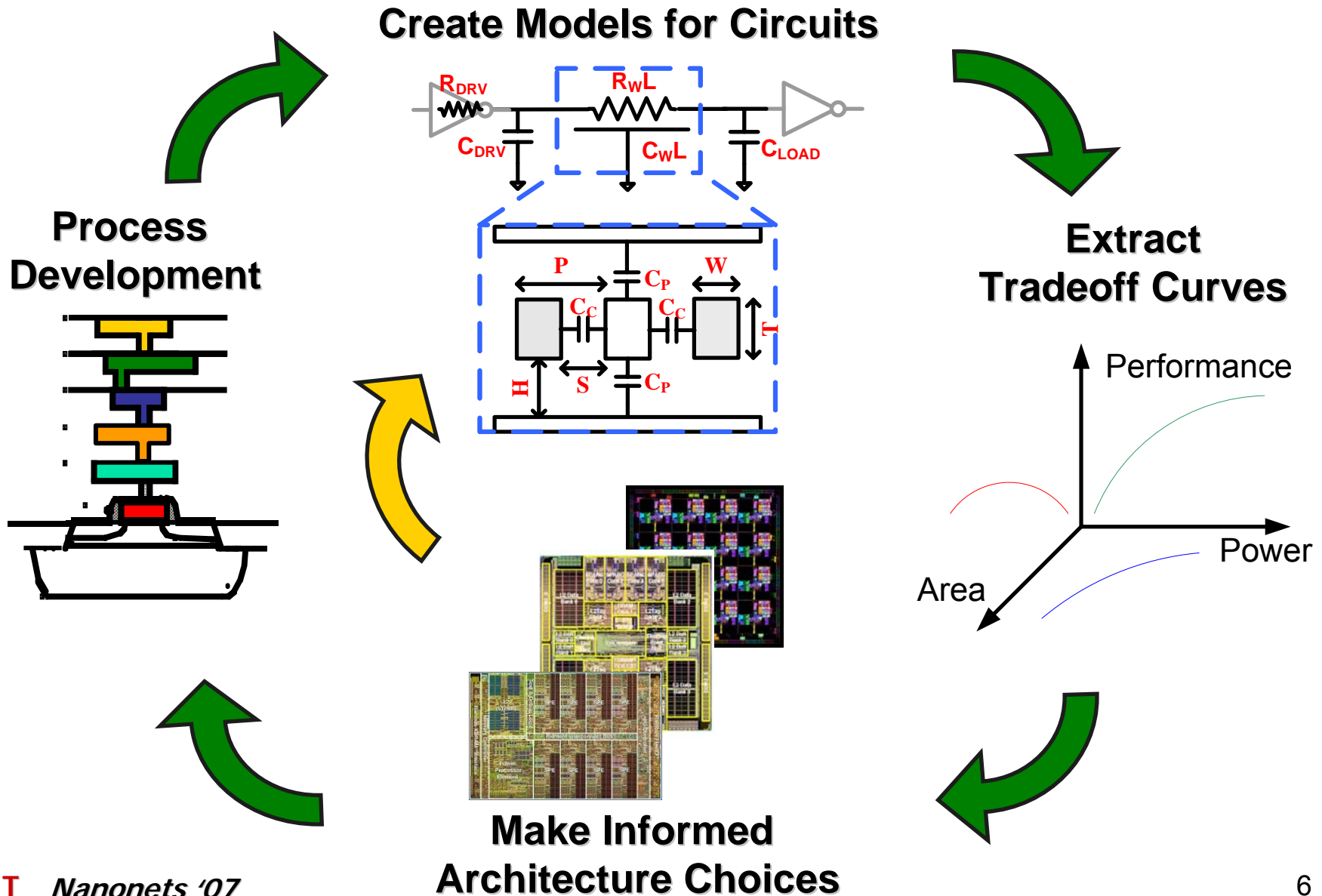
Technology Design Flow



Technology Design Flow

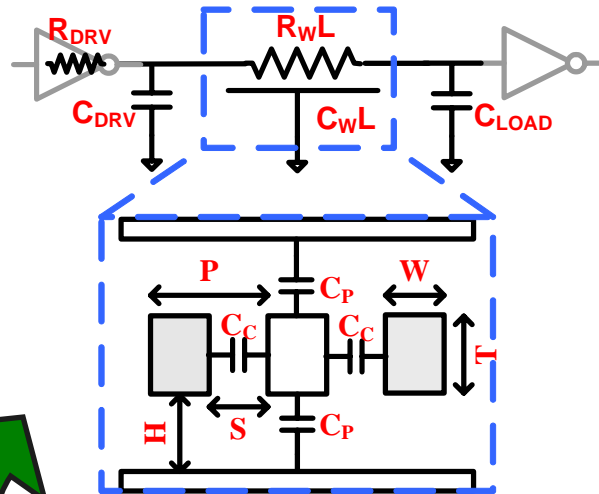


Technology Design Flow

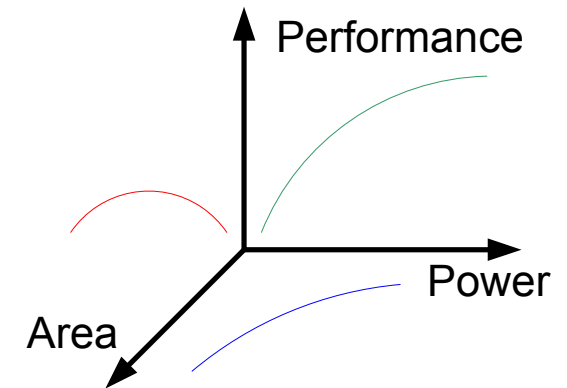


Technology Design Flow

Create Models for Circuits

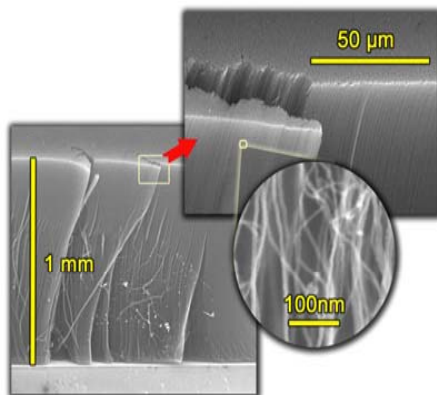


Extract Tradeoff Curves

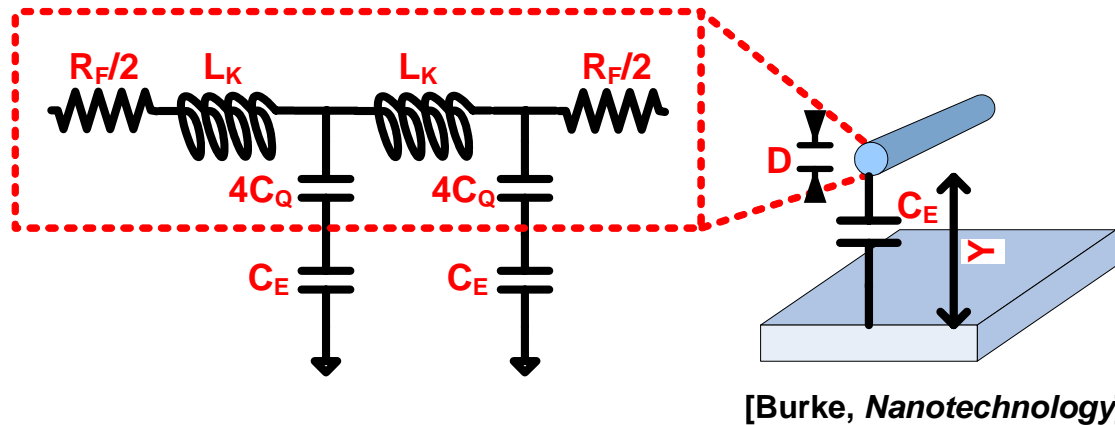


Make Informed Architecture Choices

CNT Process Development



Ideal Isolated SWCNT Model



$$R_F = \begin{cases} h/4e^2 \sim 6.5k\Omega, & L \leq L_0 \\ (h/4e^2)(L/L_0), & L > L_0 \end{cases}$$

$$L_K = h/2e^2 v_F \sim 16 \text{ nH} / \mu\text{m}$$

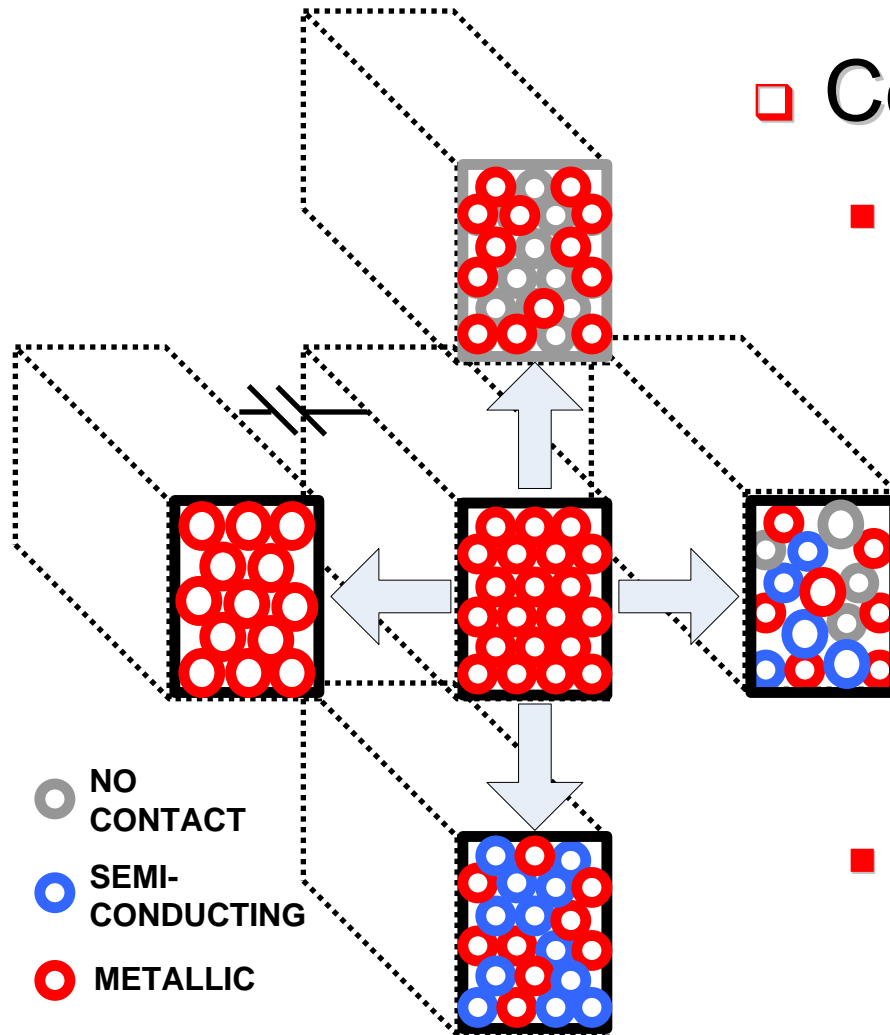
$$C_Q = 2e^2 / hv_F \sim 100 \text{ aF} / \mu\text{m}$$

$$C_E = 2\pi\epsilon / \ln(y/d) \sim 34 \text{ aF} / \mu\text{m},$$

$$\epsilon = 2.8\epsilon_0, y = 97 \text{ nm}, d = 1 \text{ nm}$$

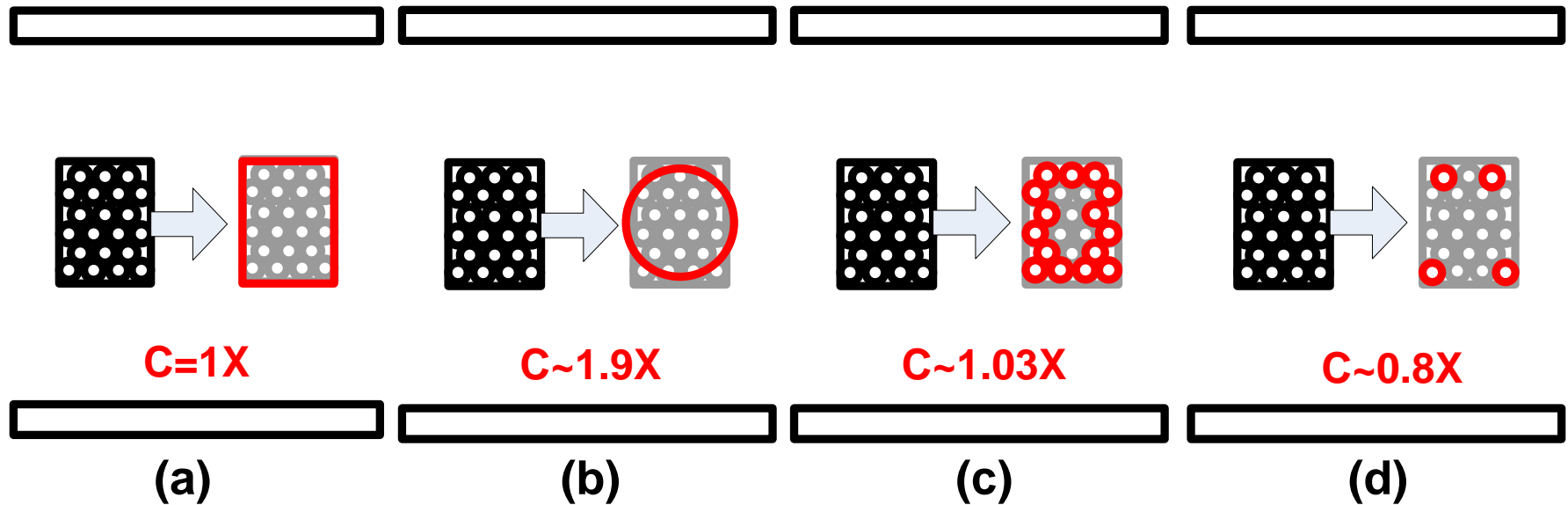
- Each parameter scales with length
 - Resistance – linear function of length beyond mean free path (L_0)
 - Capacitance – dominated by electrostatic cap (C_E)
 - Kinetic Inductance – significant only at very high frequencies ($> 7\text{GHz}$), unobserved thus far*.

Modeling CNT Bundles



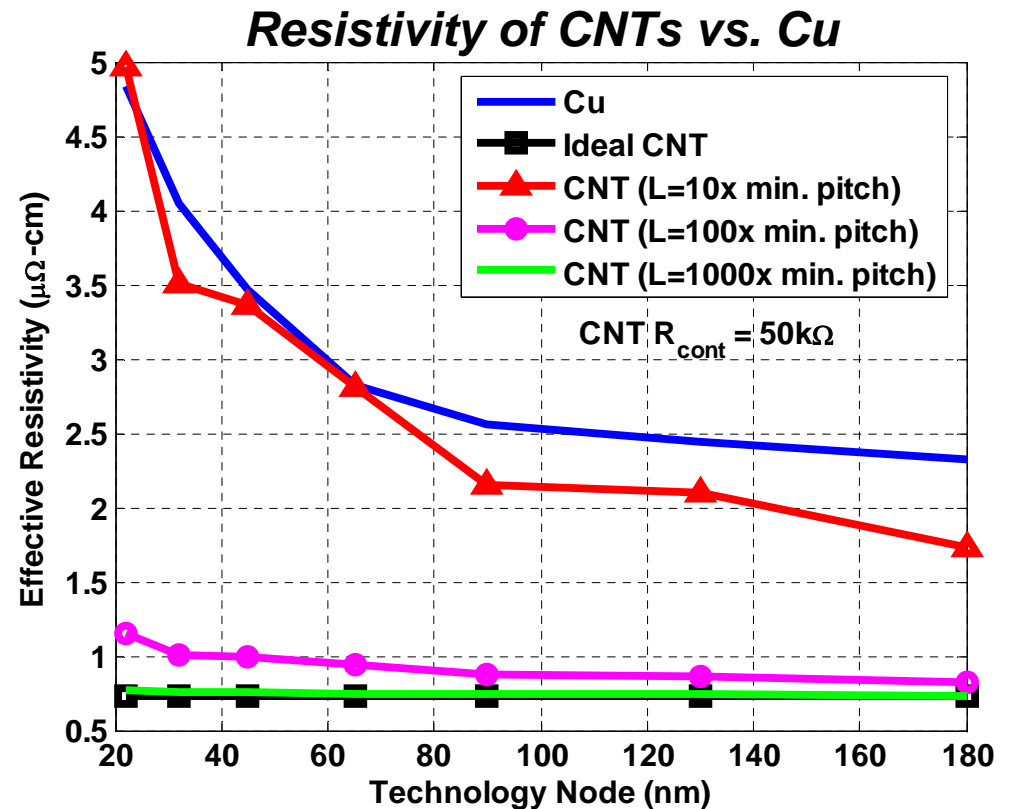
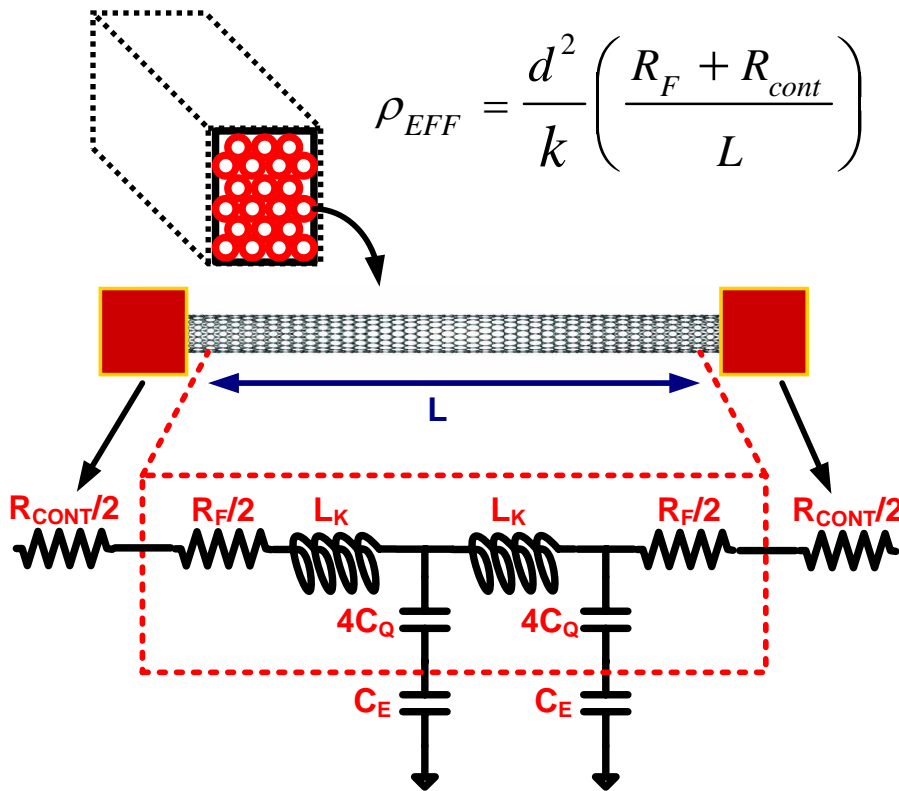
- Consider CNTs a material:
 - ‘Resistivity’ dependent on:
 - Tube diameter
 - Contact resistance
 - Mean-free path
 - Fraction of contacted metallic CNTs
 - Capacitance dependent on:
 - Bundle dimensions

Capacitance of CNT Bundles



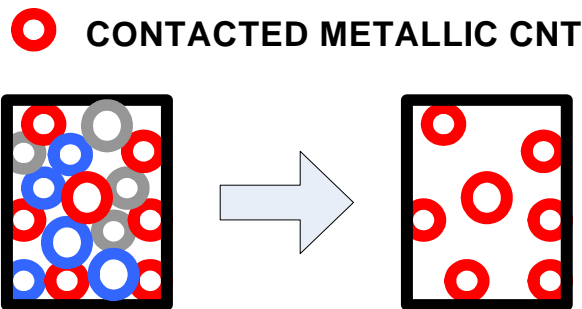
- For the same cross-section, electrostatic capacitance for all materials is the same.
 - Prior approaches use same 3D solvers as used for Cu*
- Assume similar surface roughness between Cu wires and CNT bundles

Effective Resistivity of CNTs



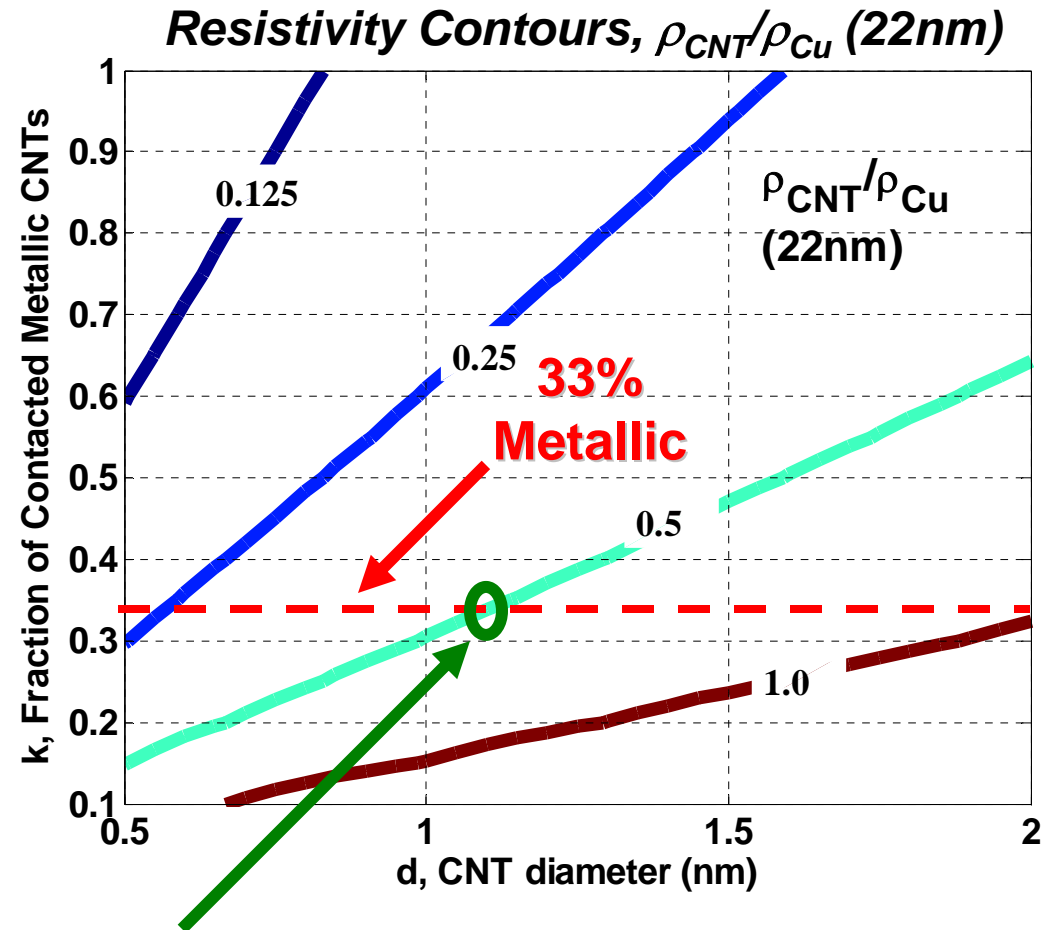
- For interconnect lengths $> \sim 1000$ gate pitches, contact resistance is insignificant
- Resistivity of ideal CNTs $\sim 7\times$ lower than Cu at 22nm

Effective Resistivity: Non-idealities



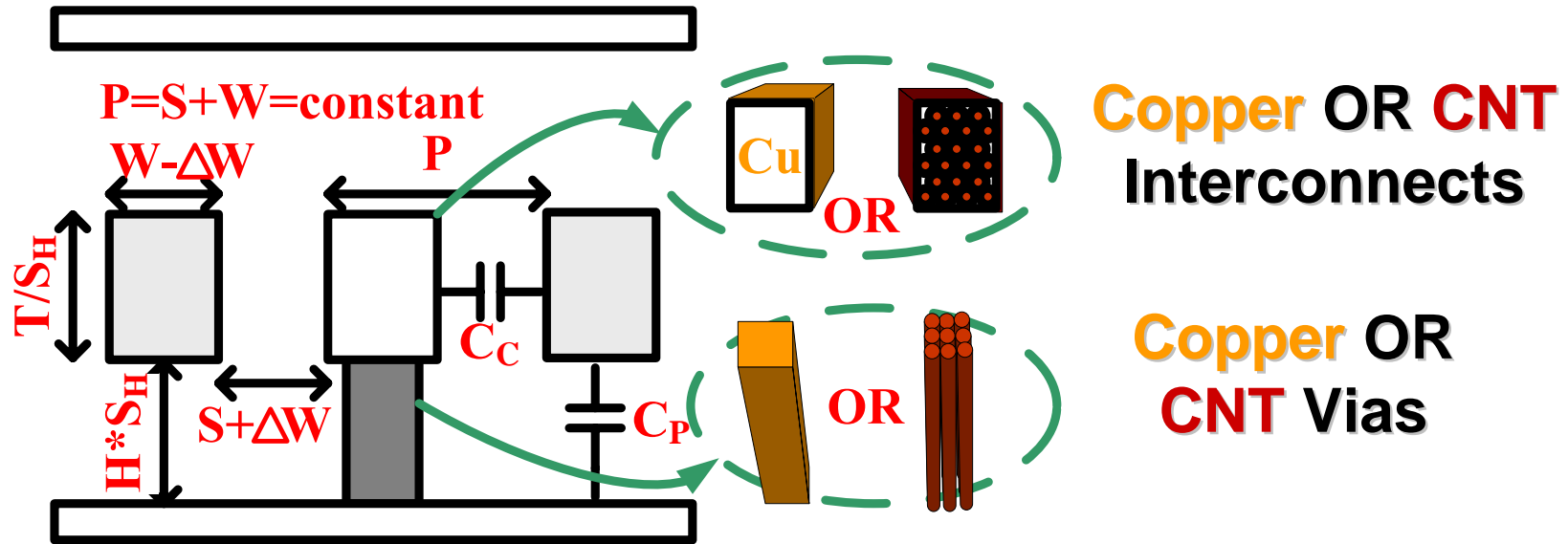
$$\rho_{EFF} = \frac{d^2}{k} \left(\frac{h}{4e^2 L_0} + \frac{R_{cont}}{L} \right),$$

$$L > L_0 \text{ where } L_0 = C_\lambda d$$



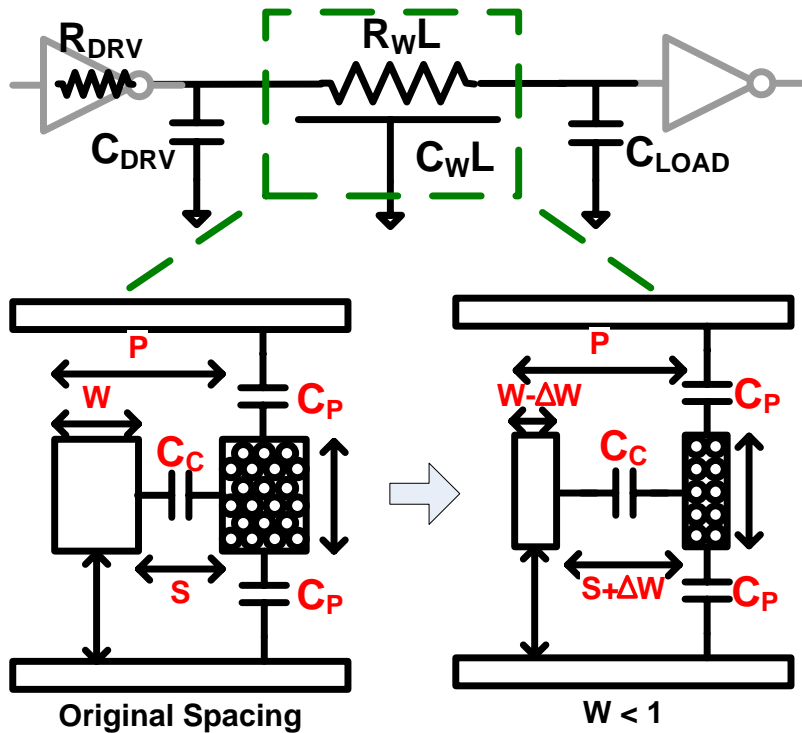
- Current growth limitations can achieve ~2x lower resistivity than copper

Scaling Interconnect: Design Space

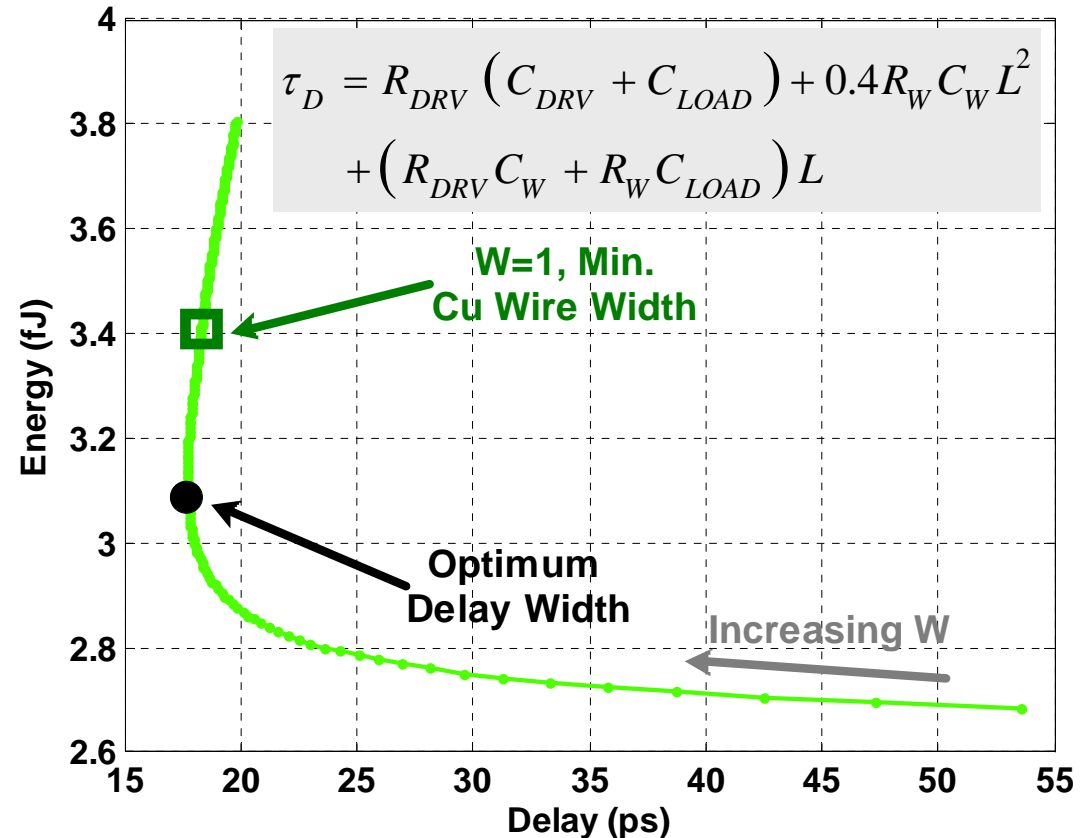


- Consider rescaling the interlayer dielectric (ILD) stackup
 - Scale width: Allow CNT bundles to be grown & assembled at finer widths
 - Increase ILD height (H): CNT vias enable higher aspect ratios, thicker ILD

Scaling Wire Width

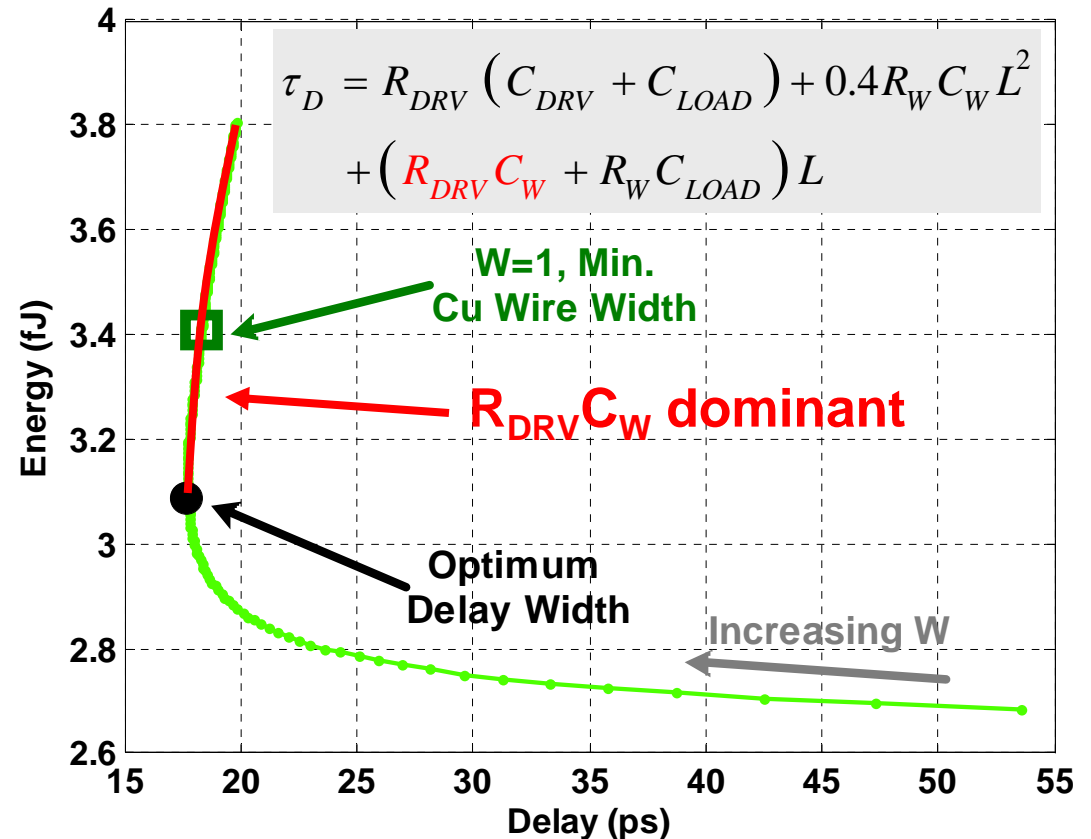
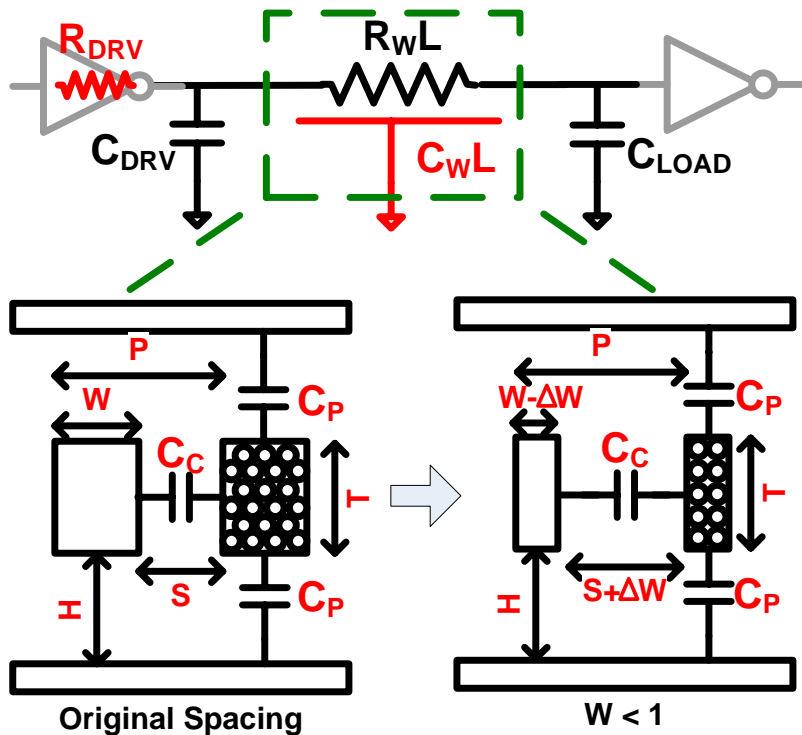


As $W \downarrow \rightarrow R_W \uparrow \rightarrow C_W \downarrow$



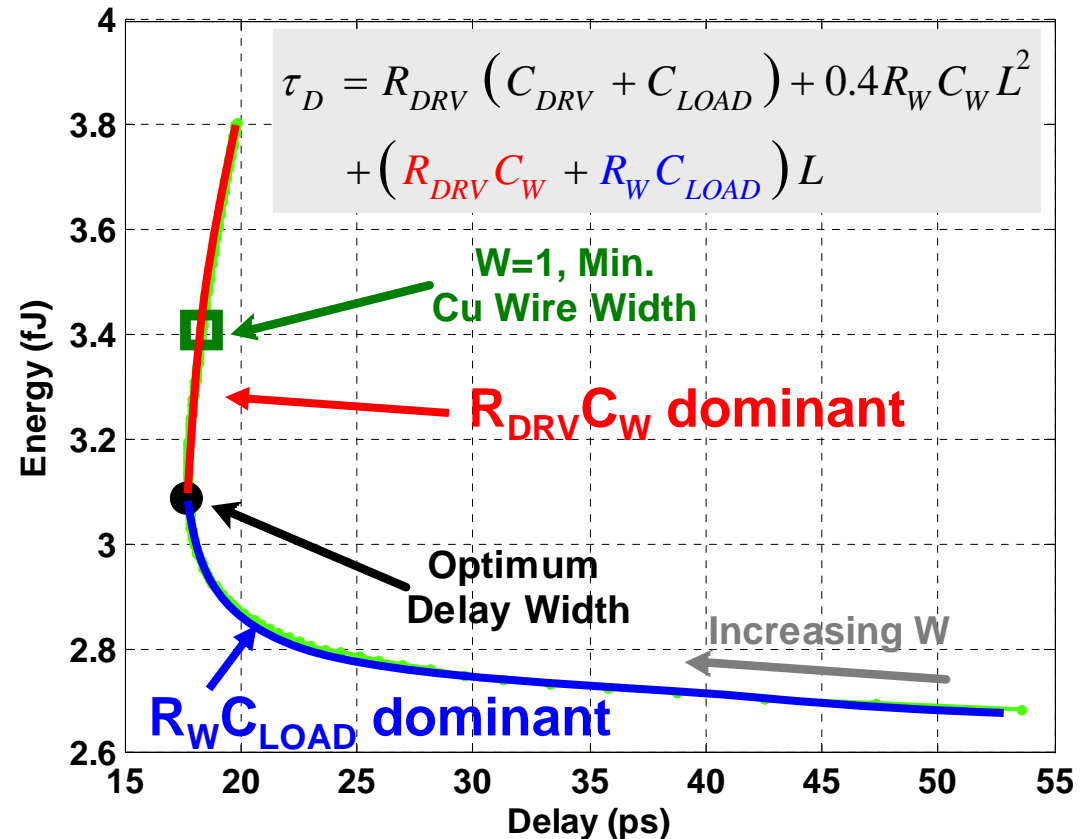
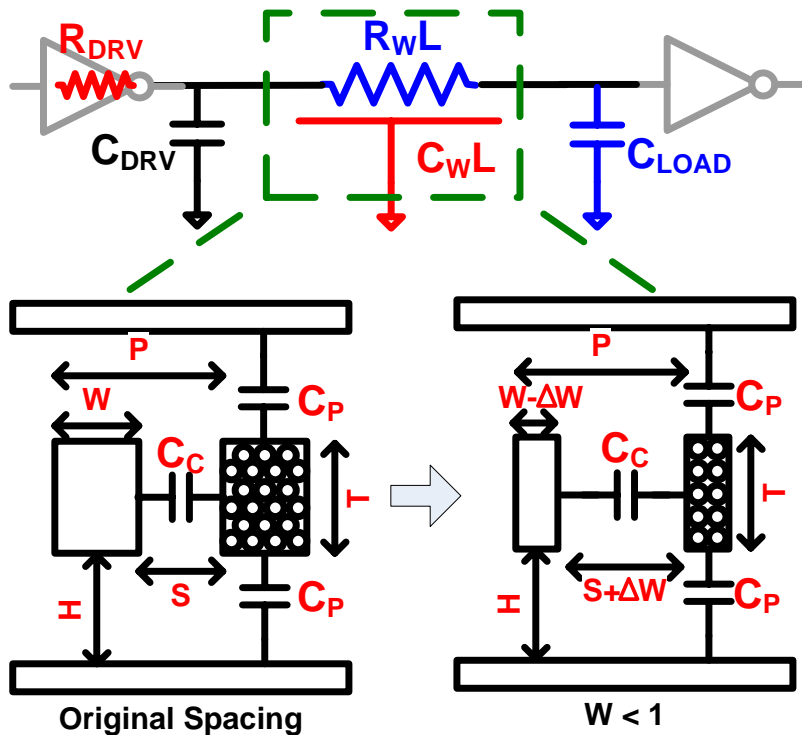
- ❑ Scale W , fixed wire pitch (P) \rightarrow constant area
- ❑ There is an optimal delay width

Scaling Wire Width



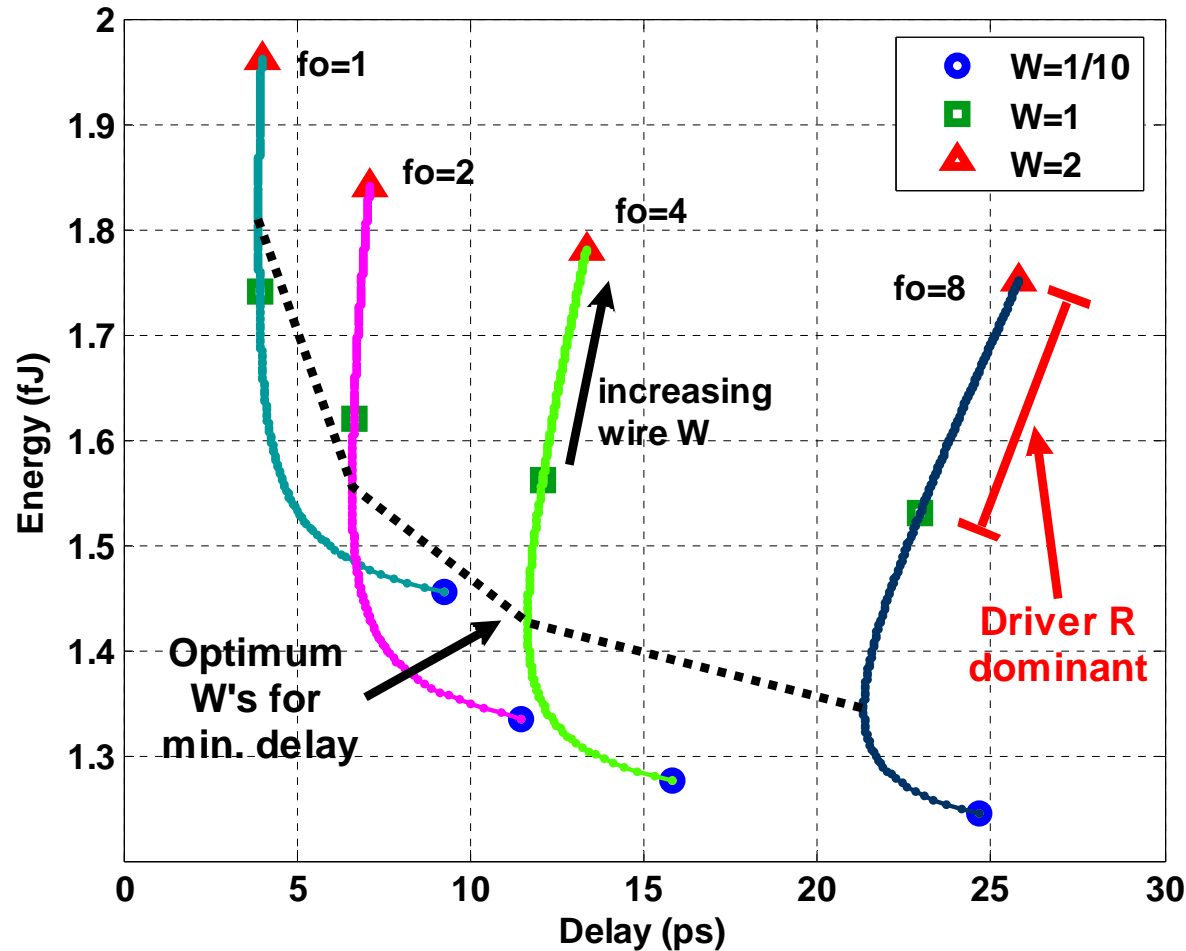
- When delay is dominated by driver resistance, decreasing wire W improves BOTH delay & energy

Scaling Wire Width



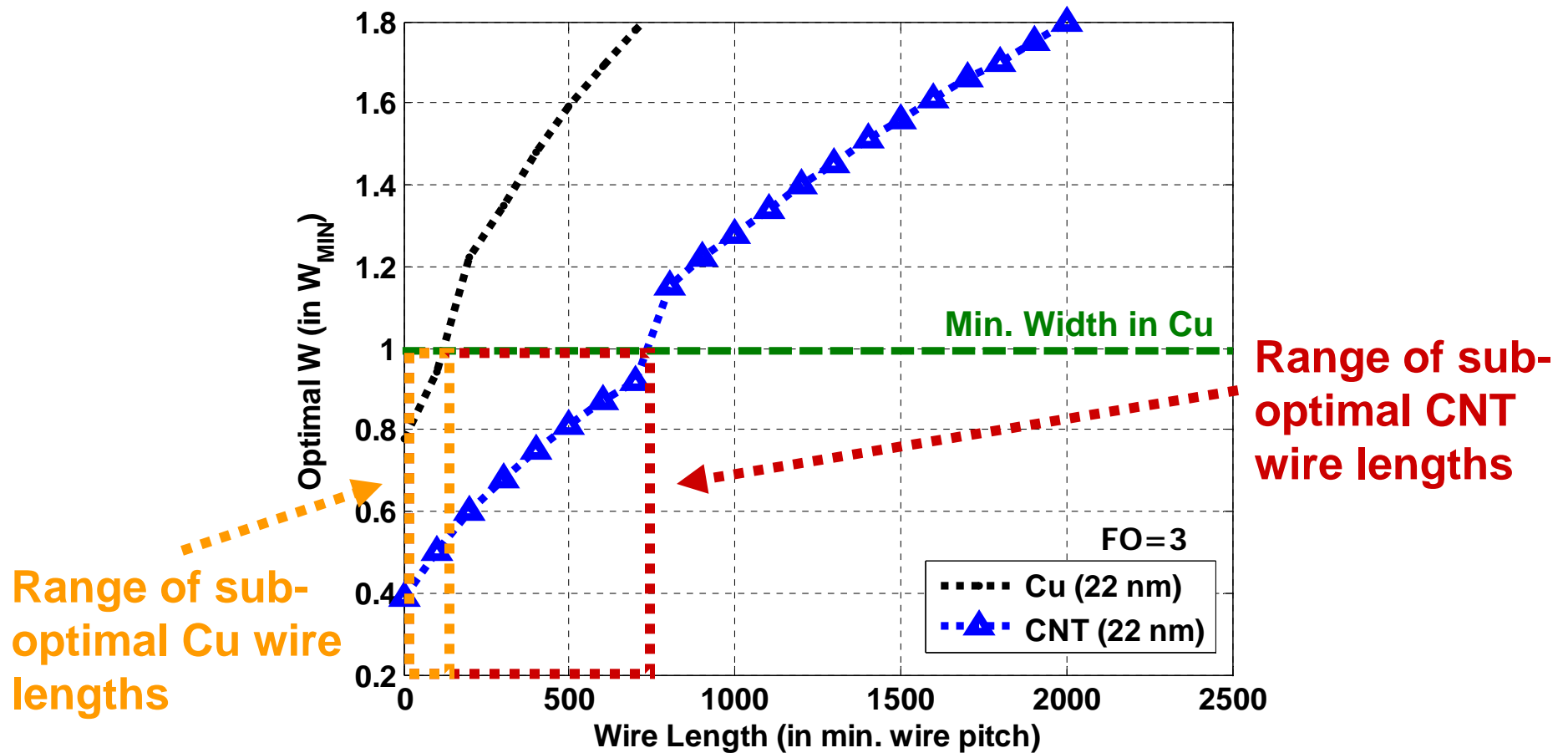
- When delay is dominated by wire resistance, scaling W trades off delay for energy
- Optimum delay width separates the two regions

Optimum Delay Wire Width (CNT, 22nm)



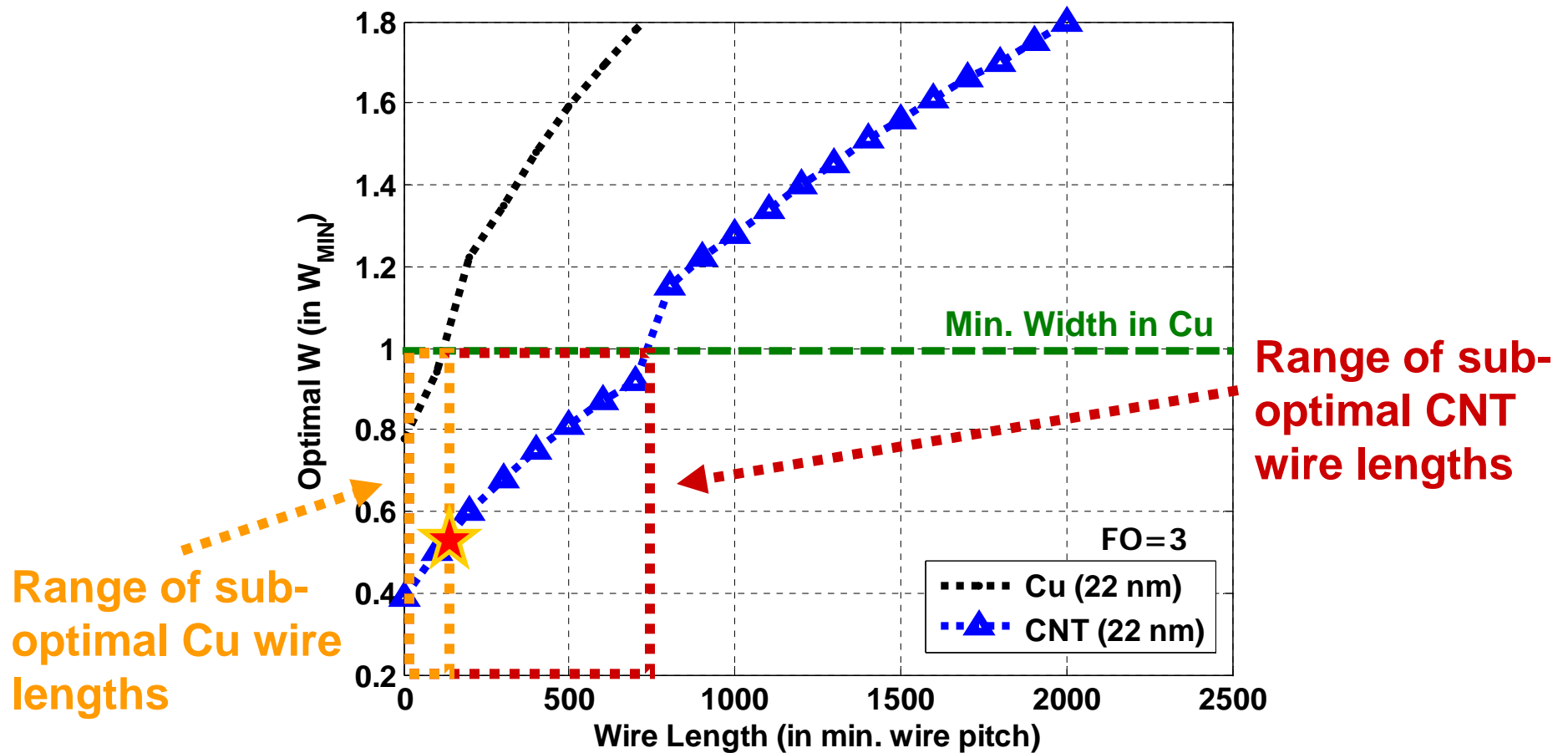
- When optimum delay wire width < 1 , wires narrower than the min Cu width result in energy AND delay improvement

Underutilizing CNTs



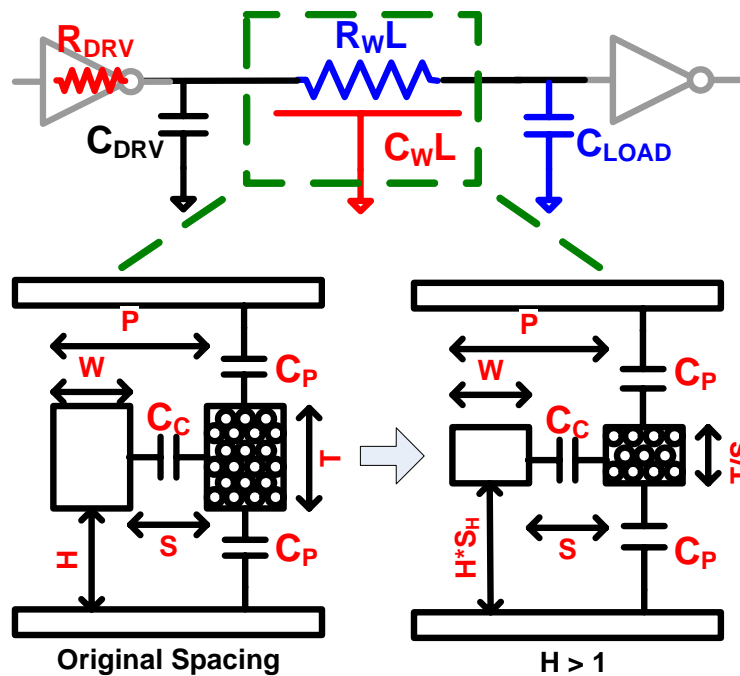
- Range of sub-optimally sized wires is greater if CNTs are used with the same cross-section as copper.

Underutilizing CNTs

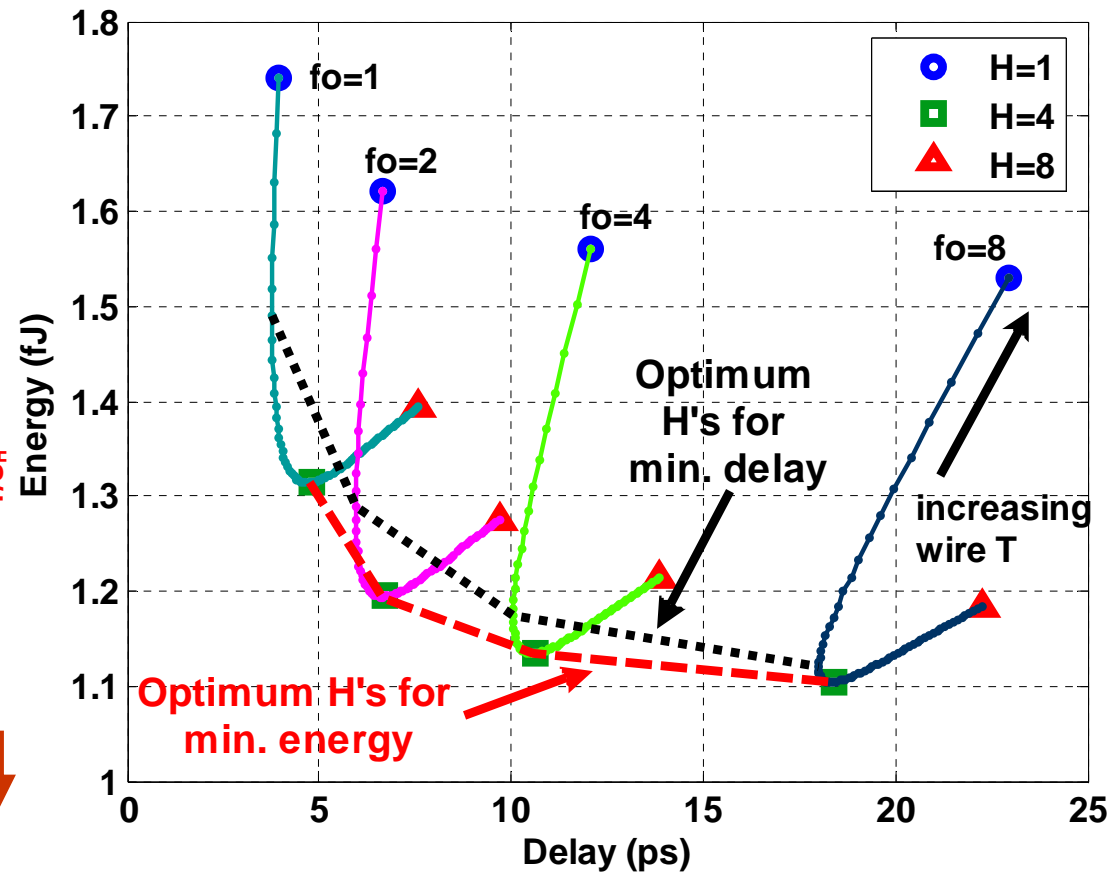


- Range of sub-optimally sized wires is greater if CNTs are used with the same cross-section as copper.

Scaling ILD Height

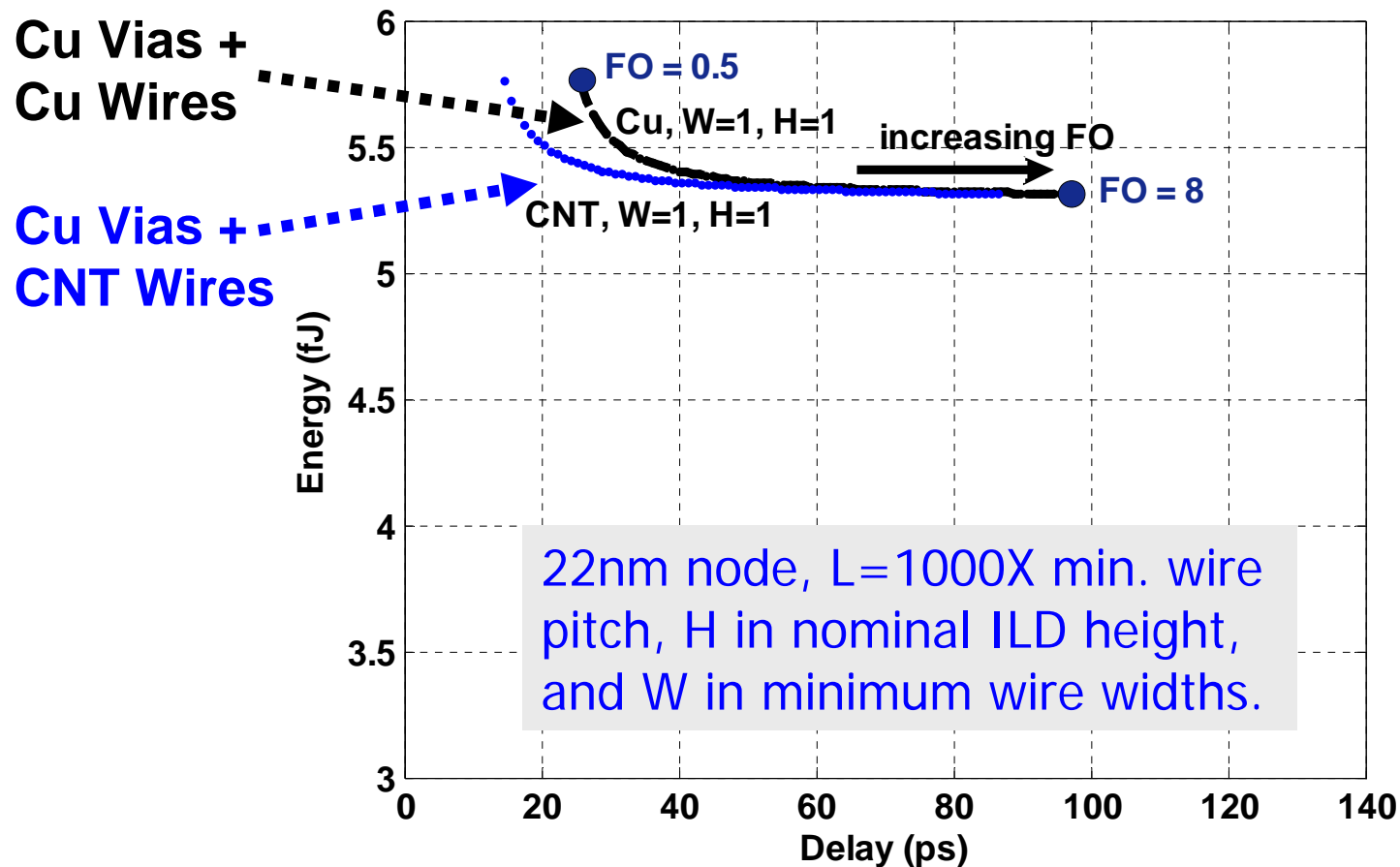


As $H \uparrow \rightarrow R_W \uparrow \rightarrow C_W \downarrow$



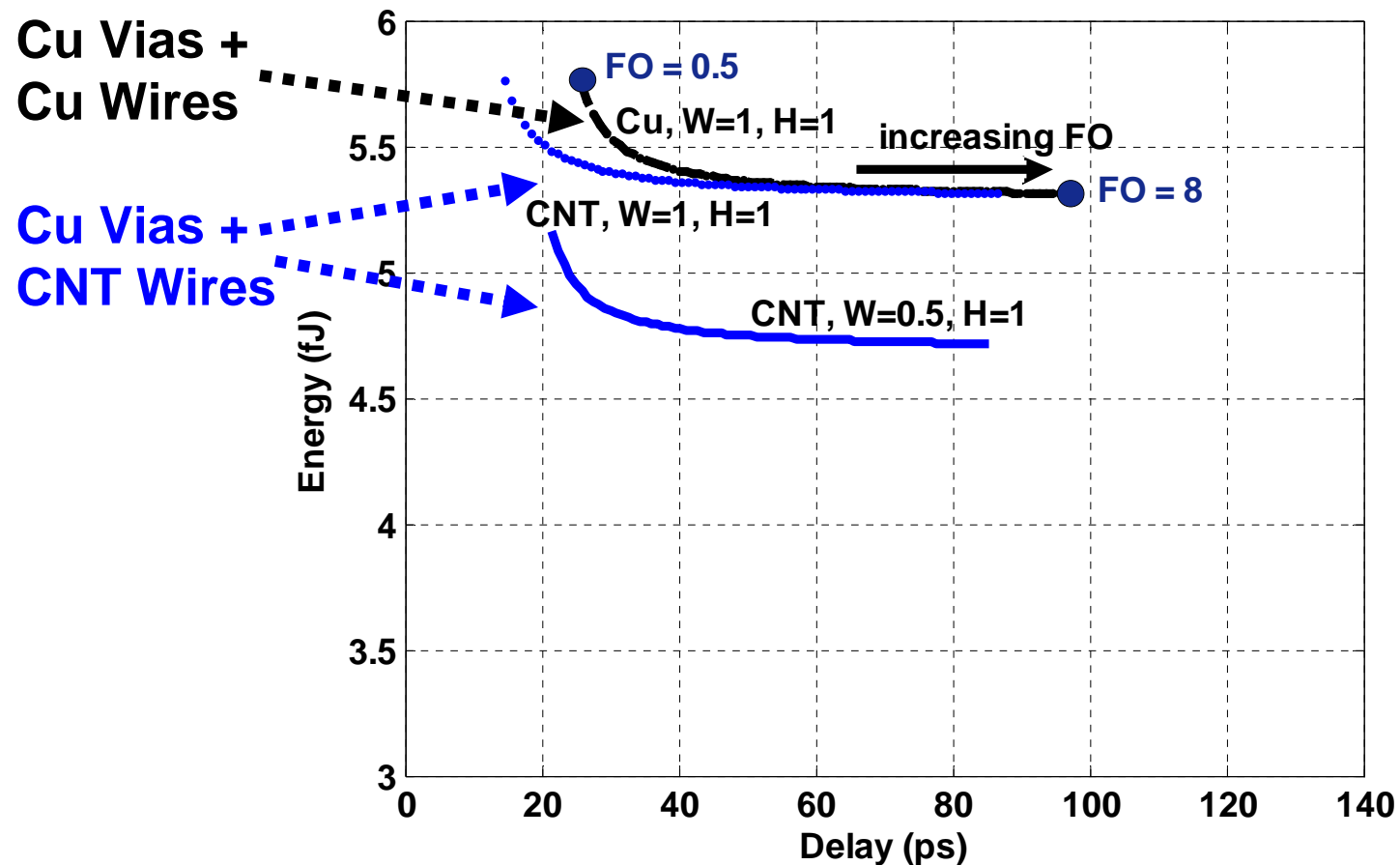
- Scale H , reverse scale T to maintain constant wire bandwidth (for comparison)
- Min. delay ($\sim H=2$) and a min. energy point ($\sim H=4$) exist

Energy vs. Delay: No Scaling



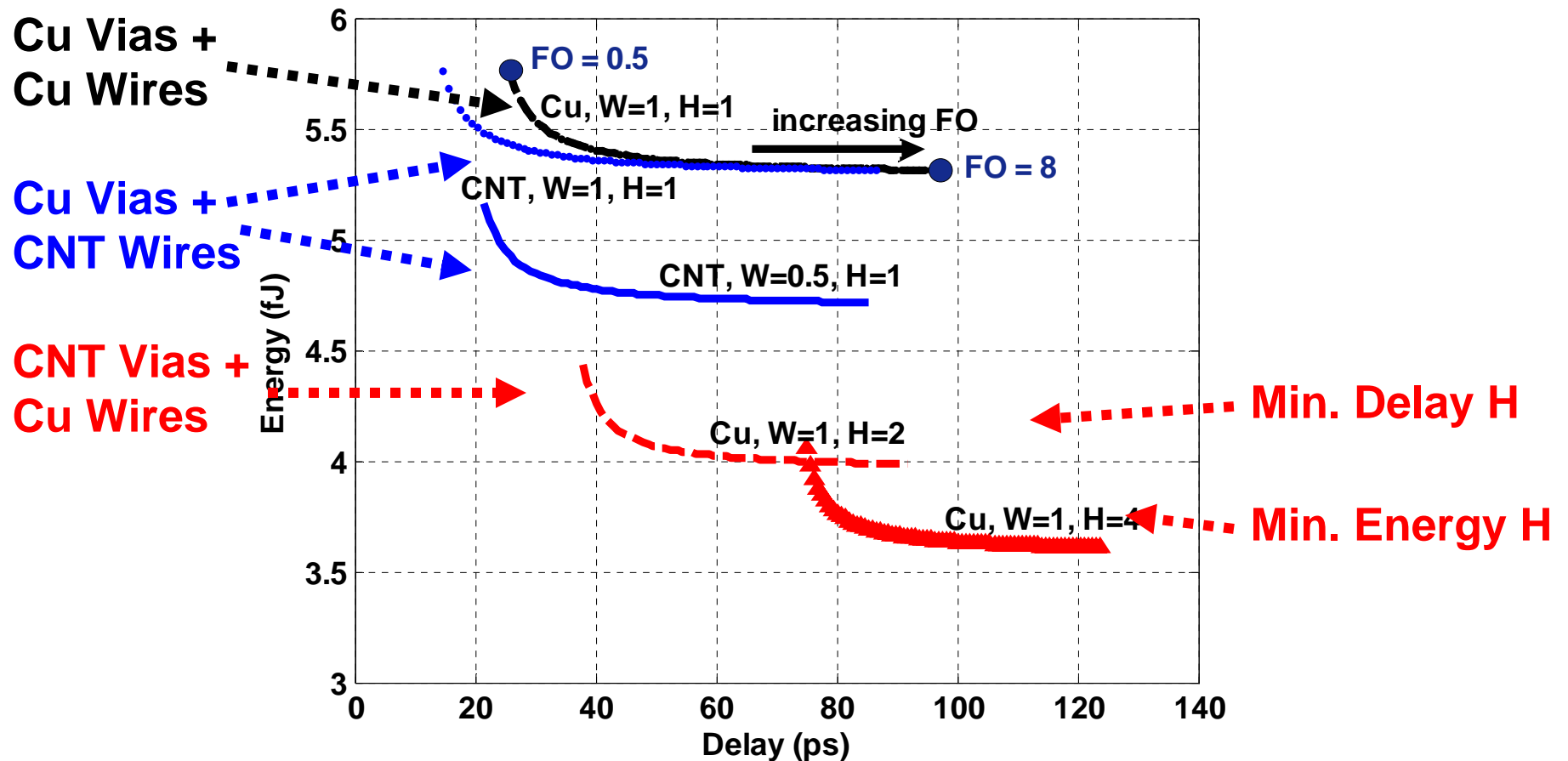
- ❑ Directly replacing Cu with CNTs (same cross-section) only yields delay improvement at lower fanouts

Energy vs. Delay: Scaling Width



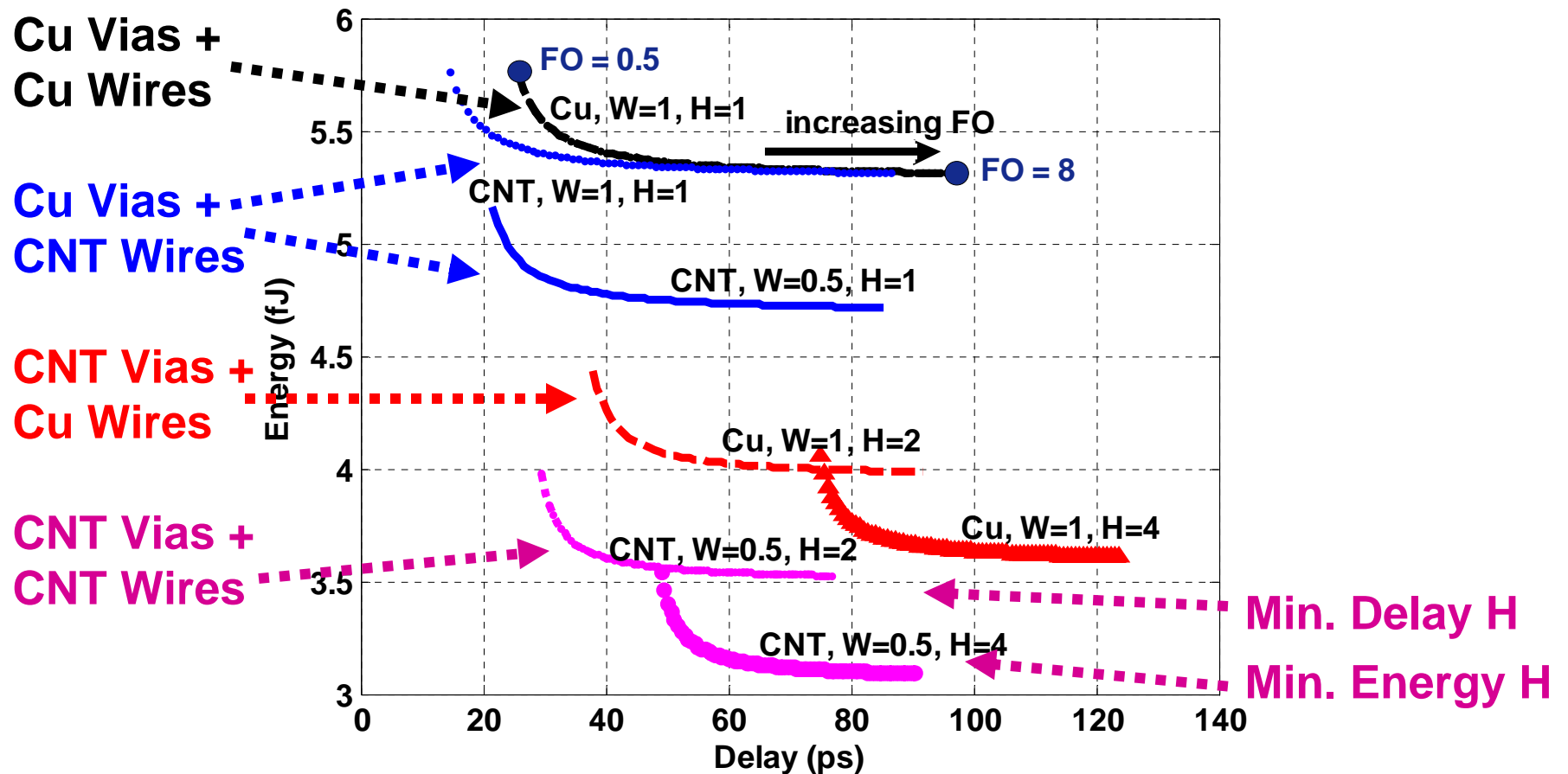
- Scaling wire width down improves energy and delay

Energy vs. Delay: Scaling ILD Height



- Scaling wire height up using CNT vias, but Cu wires improves energy with small penalty in delay.

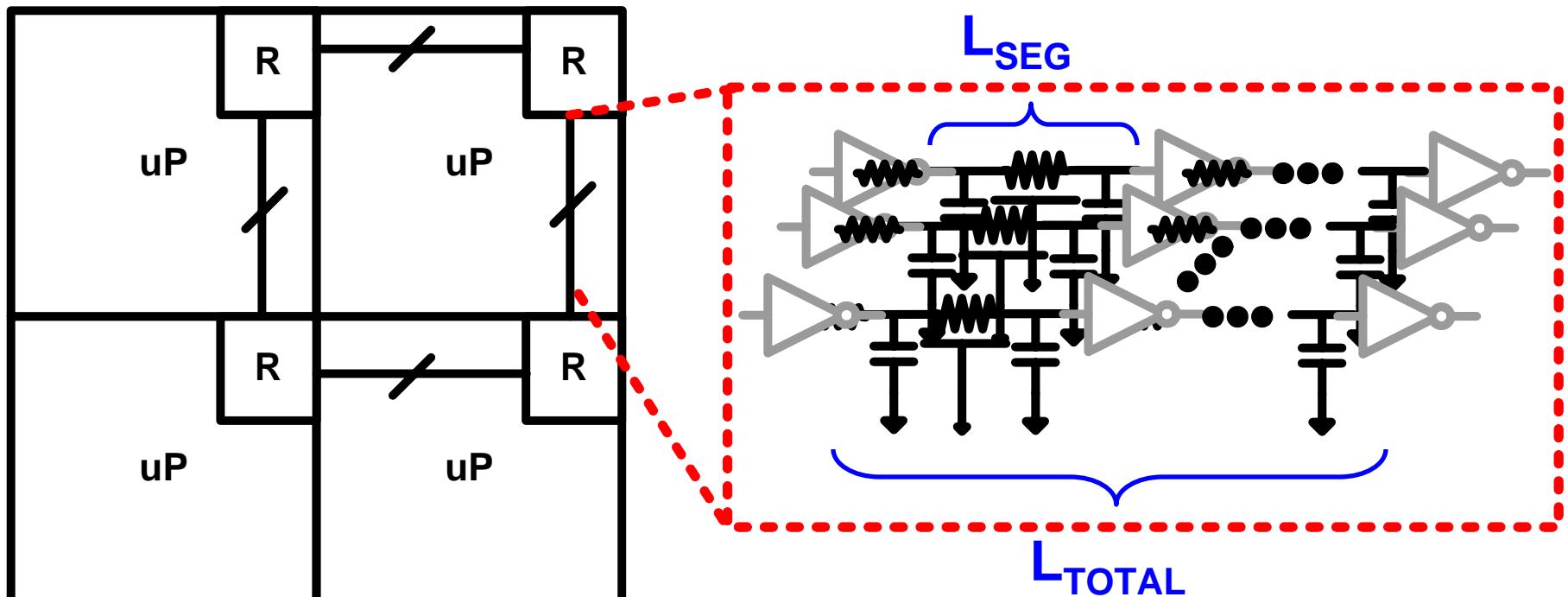
Energy vs. Delay: Scaling W & H



- Scaling both width and height result in almost 33% energy savings for the same delay

System Evaluation: On-Chip Network

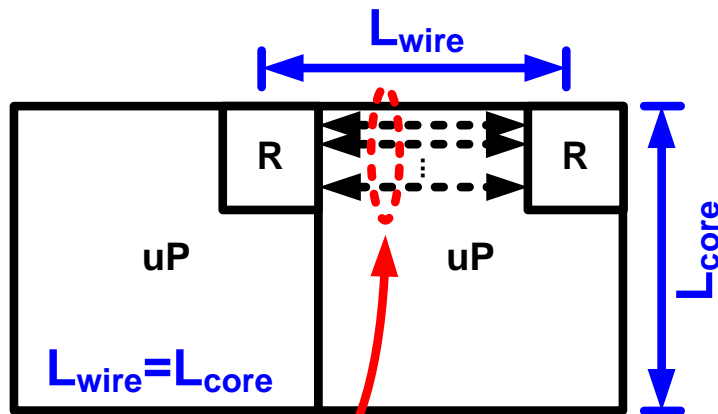
- ❑ Abstract the wire + driver model results to system level
- ❑ Extend to repeated interconnects...



$$L_{SEG} = L_{TOTAL}/N$$

$N = \# \text{ of repeaters}$

Core-to-Core Communication

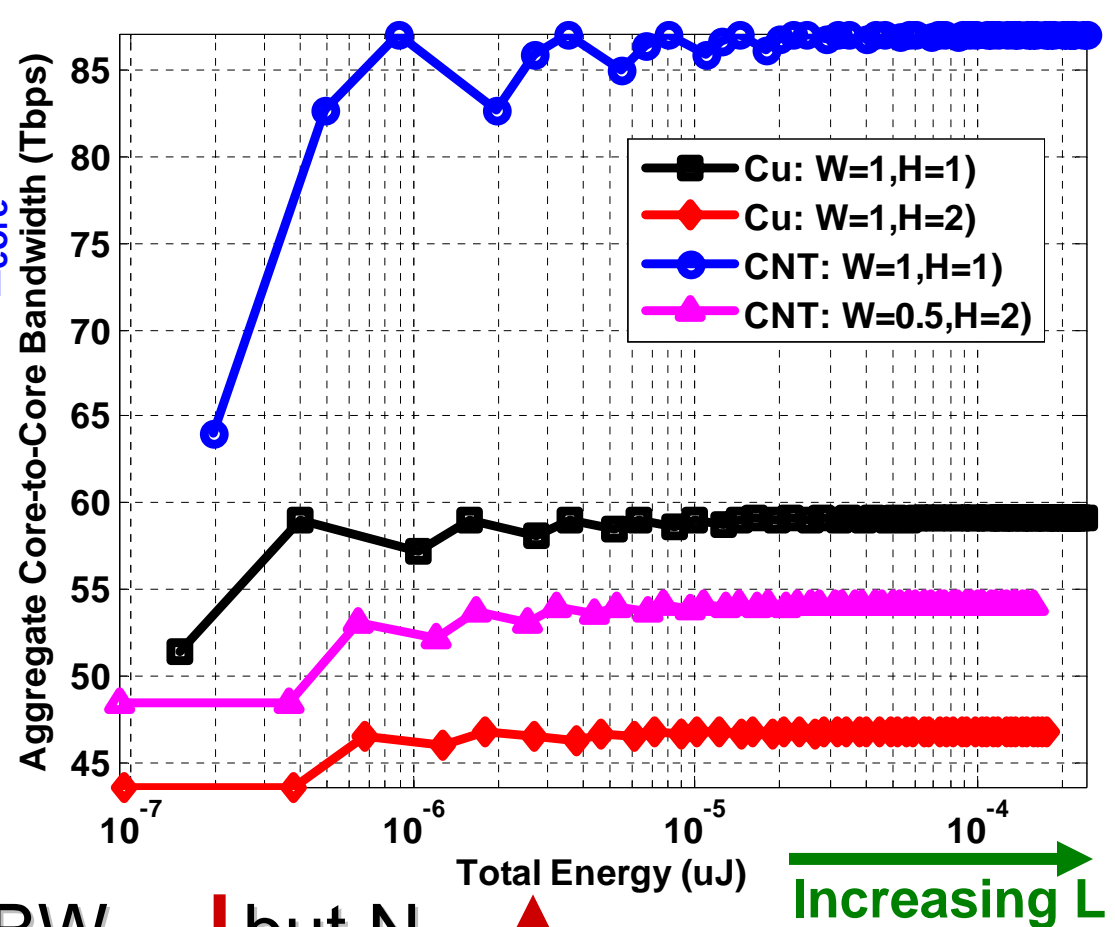


$$N_{\text{wire(max)}} = L_{\text{wire}} / P_{\text{wire (min)}}$$

$$BW_{\text{wire}} \sim 1 / D_{\text{wire}}$$

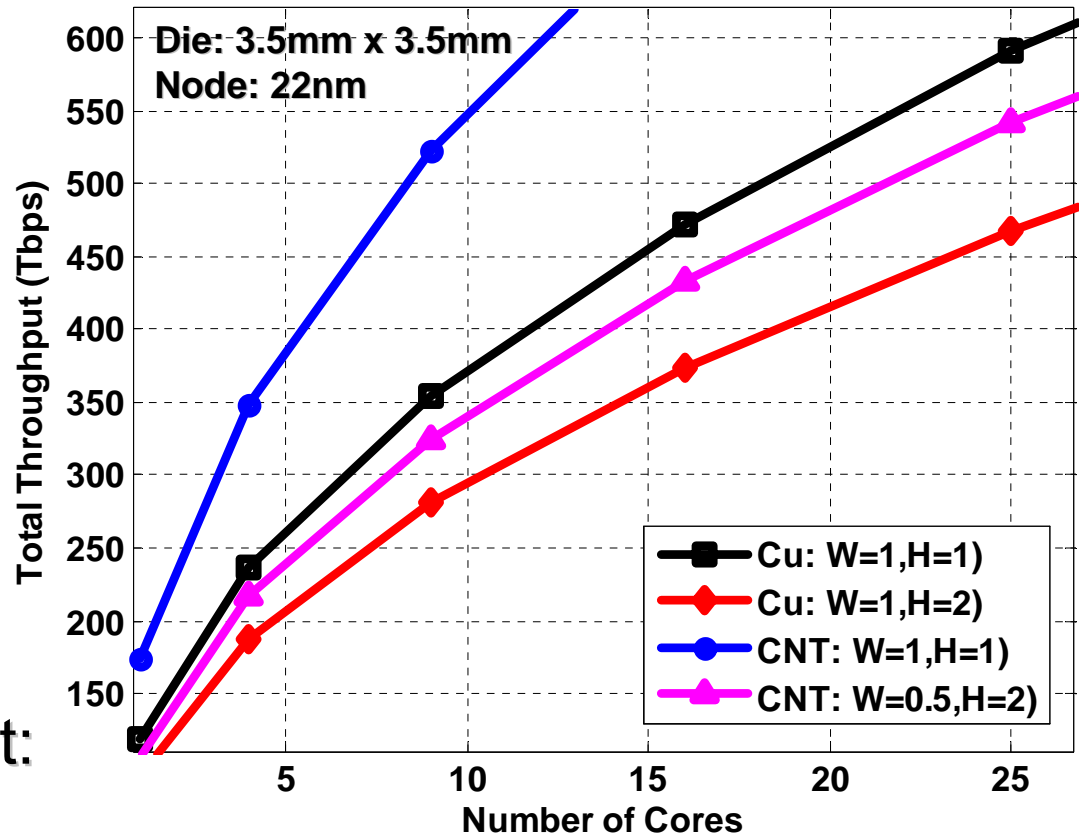
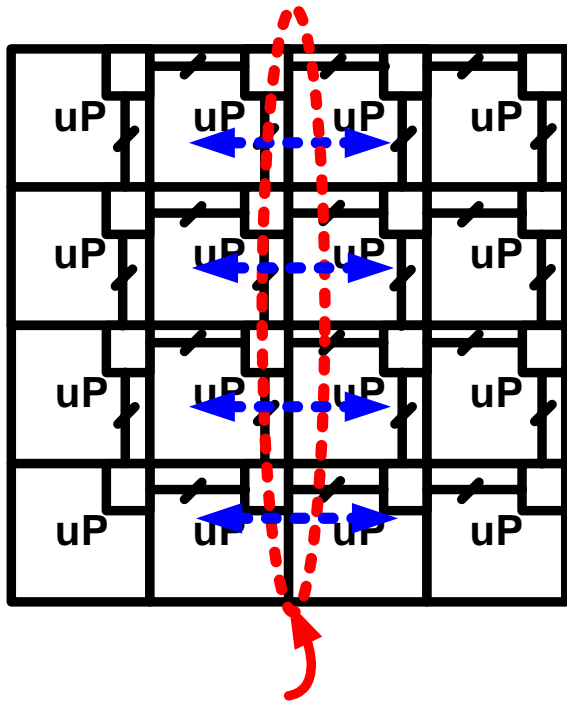
$$BW_{\text{agg}} = N_{\text{wire}} BW_{\text{wire}}$$

$$E_{\text{total}} = N_{\text{wire}} E_{\text{wire}}$$



- As the cores grow: $BW_{\text{wire}} \downarrow$ but $N_{\text{wire}} \uparrow$
- For same lengths, bandwidth comes at different energy cost for each configuration

How Many Cores? Infinite?



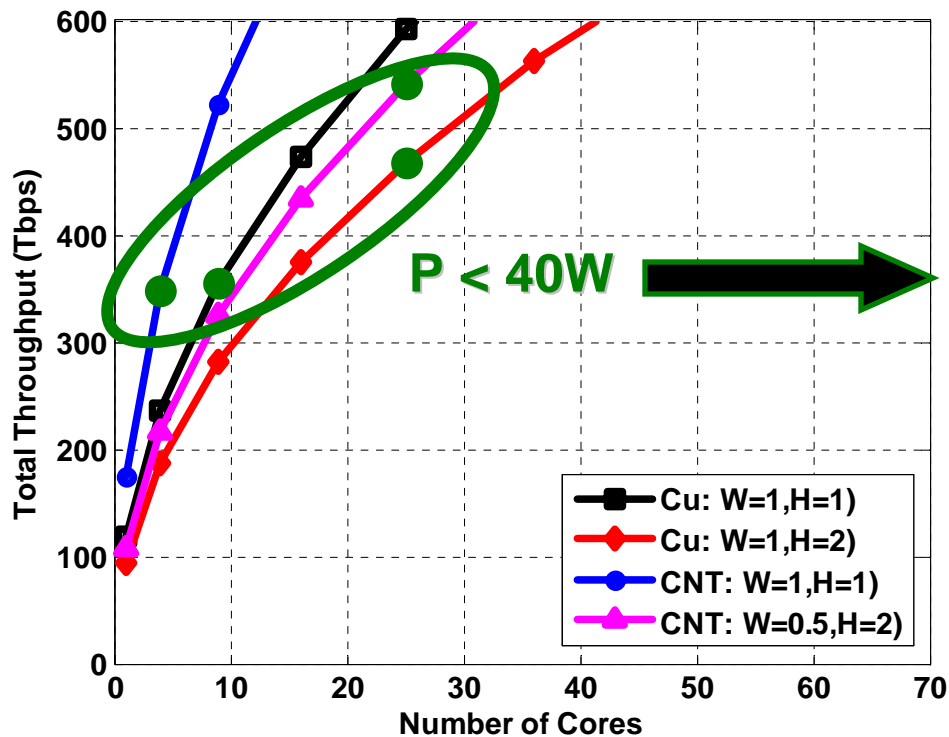
- Total system throughput:

$$T_{sys} = 2\sqrt{N_{core}} \cdot BW_{agg}$$

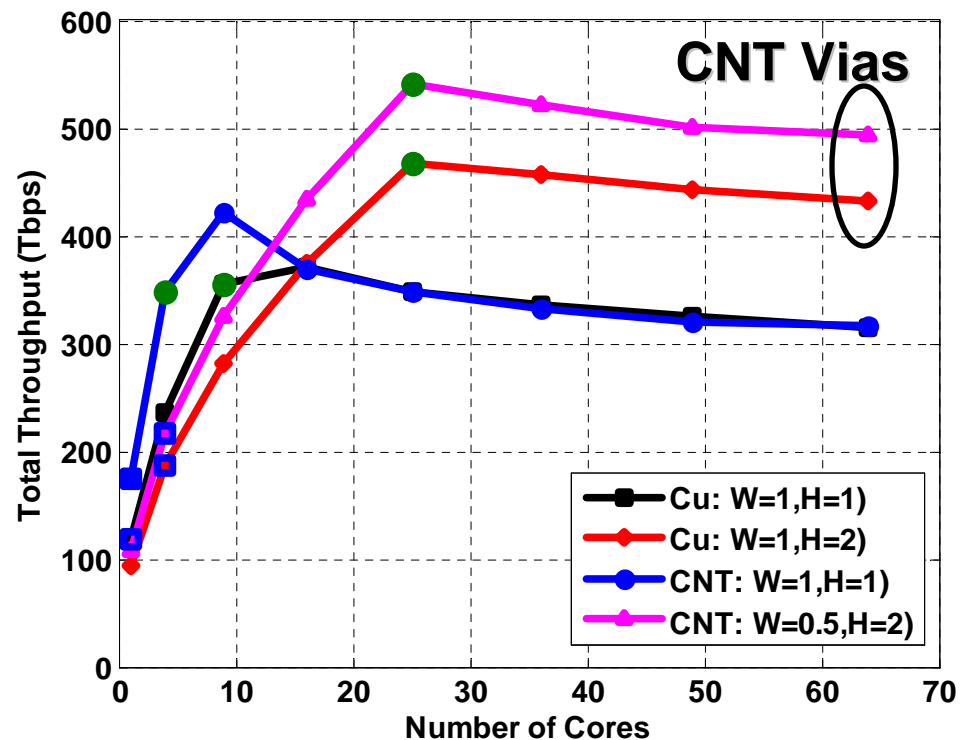
- Total system throughput monotonically increases, but...

Max. Throughput: Power Constrained

Total Throughput vs. # of Cores



Total Throughput for P < 40W



- Throughput saturates with increasing number of cores
- Lower capacitance configurations produce greater power constrained total throughput

Conclusions & Future Work

- ❑ It is vital to evaluate technology changes at all levels of the design hierarchy
- ❑ To really take advantage of CNTs, ILD stack up needs to be rescaled to proportion R_W & C_W for application needs
- ❑ Theoretical CNT Models need to be verified with measurement data
- ❑ There are still many integration/manufacturing challenges to overcome