18Gb/s Optical IO: VCSEL Driver and TIA in 90nm CMOS

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Abstract

An 18Gb/s optical data rate is achieved with a commercial GaAs VCSEL by applying rising and falling edge pre-emphasis with a 90nm CMOS driver. The pre-emphasis pulse shape can be digitally adjusted with time resolution less than one bit period. The TIA receiver has cross-coupled cascodes to increase the amplifier gain/bandwidth and operates at 12.5Gb/s to 18Gb/s depending on the input capacitance.

Introduction

Electrical IO is becoming limited by copper interconnect channel losses that depend on frequency and distance. Off-chip optical interconnect sees negligible channel losses, but data rates are limited by the intrinsic optical dynamics and electrical parasitics of the optical devices. The VCSEL driver and TIA in this paper apply circuit techniques to operate standard commercial optical components beyond the intrinsic data rates imposed by these bandwidth limits.

Digitally Tunable Pre-Emphasis VCSEL Driver

Commercial GaAs VCSELs have significant capacitance, typically 700fF, and are therefore limited by electrical parasitics as well as intrinsic optical dynamics. In [1], falling edge pre-emphasis reduces the optical fall time of experimental 990nm InGaAs VCSELs. These InGaAs devices have smaller capacitance, typically 160fF, and are not significantly limited by electrical parasitics [2]. Dual edge pre-emphasis compensates for both optical and electrical limitations in GaAs VCSELs [3], but the reported architecture has a minimum pre-emphasis pulse width of one bit period and requires phase tuning of the interleaved clocks to minimize systematic jitter. The driver presented in this paper derives timing information directly from the full-rate input data and generates pre-emphasis pulses with width resolution less than one bit period in a manner that is compatible with full-rate IO architectures.

Fig. 1 shows the proposed architecture, which provides digital control of the pre-emphasis pulse duration, modulation current and pre-emphasis current. The input splits into two paths with programmable delay difference (T_{DEL}) to generate primary and delayed data phases, D and D*, which switch two bias currents to generate modulation and pre-emphasis currents, I_D and I_{D*}. I_{D*} is inverted and scaled with respect to I_D, and the total drive current (I) resulting from the summation of the two currents at the output node contains pre-emphasis pulses of duration T_{DEL} at each data transition. DACs bias the driver in the full link and an external bias is used in the measured test circuit. Termination is included to allow 50Ω interconnect within a CMOS+VCSEL MCM package [4].

Fig. 2 shows the output stage, which consists of two current switches with differential input and single-ended output. Cascodes improve the current switching symmetry by isolating the drains of the input differential pairs from the unbalanced output swing. The pre-emphasis pulse width is set by a 4-tap digital delay line, Fig. 3A, where a buffer chain generates four data phases and a two-level MUX tree selects a tap. The simulated range is 35ps to 65ps with 10ps steps, Fig. 3B,

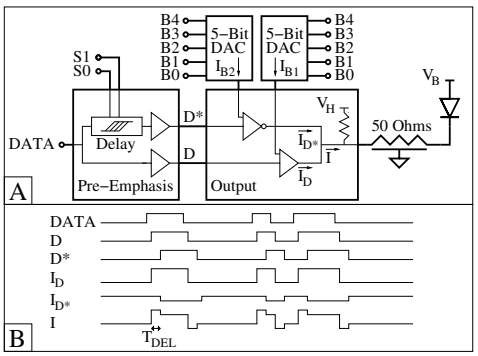

Fig. 1. Pre-emphasis block diagram (A) and basic operation (B).

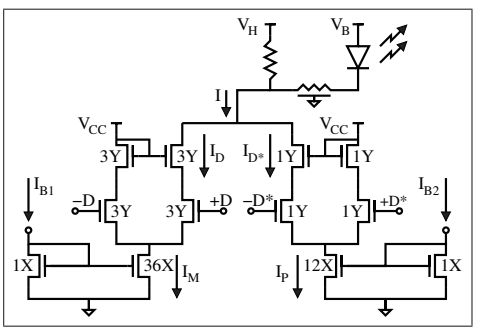

Fig. 2. VCSEL driver output stage schematic.

which allows fine tuning of the pre-emphasis width. Pre-emphasis reduces the simulated electrical rise time by 50%, from 60ps to 30ps. The output and pre-emphasis blocks occupy $0.009\mu m^2$ and $0.014\mu m^2$ on the 90nm chip [5].

The driver was measured using RF probes to drive the input with a differential PRBS and connect the output to an external 8μm aperture GaAs VCSEL. The VCSEL output was coupled to a multimode fiber and measured with a 12GHz optical receiver. The measured optical eye, Fig. 4, demonstrates that pre-emphasis improves the vertical eye opening by 122% and the horizontal eye opening by 76% for modulation from 2mA to 10mA. V_{CC}=1.2V, V_B=3.0V, D* is selected from the second tap, and the received power is 2.1dBm. With pre-emphasis, I_M=27mA, I_P=8mA, V_H=1.6V, and the power is 131mW (7.3mW/Gb/s). Without pre-emphasis, I_M=19mA, V_H=1.2V, and the power is 109mW (6.1mW/Gb/s). Reported power includes full-rate pre-emphasis generation, termination, VCSEL power, and drive strength buffering.

Cross-Coupled Cascode TIA

Differential topologies integrate the single-ended to differential conversion into the TIA, mitigate supply noise, and improve stability by allowing negative feedback from a two-stage amplifier. The core amplifier topology, Fig. 5A, improves on the standard differential pair and source-follower topology [6] with cross-coupled cascodes (M3-M4) to increase the gain to (1), which evaluates to 9.1 (2x4.55) for simulated small-signal parameters and is more than twice the gain of a differential pair with the same input pair and bias current.

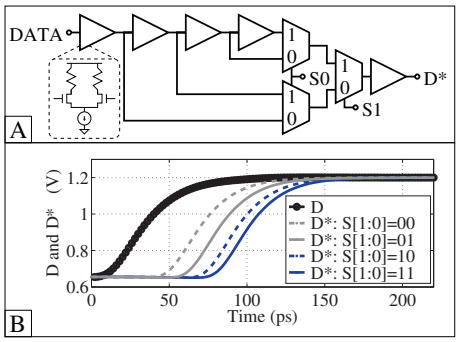

Fig. 3. Delay line architecture (A) provides sub-bit-period resolution (B).

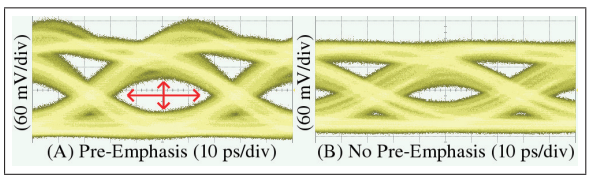

Fig. 4. Measured optical eye diagram: VCSEL driver pre-emphasis increases vertical opening by 122% and horizontal opening by 76% at 18Gb/s.

$$\frac{V_{x+}}{V_{i+}} = \frac{g_{m1}(g_{ds3}+g_{m3})}{G_L(g_{m3}+g_{ds1}+g_{ds3})+g_{ds1}(g_{ds3}-g_{m3})} \quad (1)$$

System specifications require the TIA to generate a differential 2x50mV output from a received single-ended photocurrent of 200μA peak-to-peak, which requires a transimpedance gain of 2x250Ω (54dBΩ). For 12.5Gb/s operation, 8.75GHz TIA bandwidth is required for acceptable ISI, but designing for a dominant pole at 10GHz leaves margin for the TIA to operate correctly with increased photodiode or parasitic capacitance. With a photodiode capacitance of C_I=250fF, achieving this bandwidth requires an input resistance of R_I=64Ω. The required voltage amplifier gain, A=2x3.9, is calculated from $\frac{V_O}{I_I}$=A·R_I and the feedback resistance is R_F=R_I·(1+A)=314Ω.

To implement single-ended to differential conversion, the TIA feedback must bias the negative input of the amplifier at the midpoint of the positive input. Fig. 5B and Fig. 5C compare standard symmetric feedback to the proposed common-mode feedback. Both require DC offset cancellation, shown here as I_{DC} and implemented with a DAC in the full link and an external bias in the test circuit, to generate a TIA input current with no DC component. The symmetric feedback TIA gain decreases below the R_FC_{DC} pole, so C_{DC} is impractically large for systems requiring a broadband TIA. The common-mode feedback exploits the fact that DC offset cancellation sets the current through R_F to zero at the switching threshold, which forces V_{i+}=V_{o-}. If V_{i-} differs from this shared voltage, V_{o+} moves in the opposite direction and the

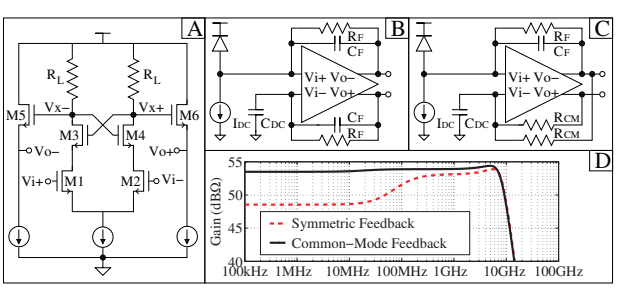

Fig. 5. Amplifier with cross-coupled cascodes (A), symmetric feedback (B), common-mode feedback (C), and comparison of gain simulations (D).

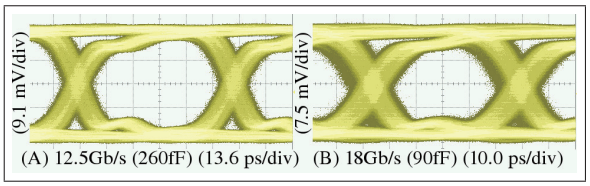

Fig. 6. Electrical TIA characterization at 12.5Gb/s and 18Gb/s.

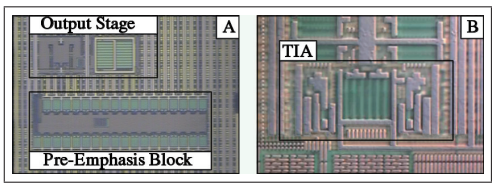

Fig. 7. Die photos of VCSEL driver (A) and TIA (B).

resistive divider pulls the circuit to the stable bias where all four voltages are equal. As the outputs are symmetric around this common-mode, the feedback is independent of the data, so C_{DC} no longer sets the TIA bandwidth and is reduced to a smaller value sufficient for high frequency noise suppression. Post-extraction AC simulations of the symmetric (C_{DC}=10pF) and common-mode feedback (C_{DC}=2pF), Fig. 5D, with 250fF input capacitance predict 9GHz bandwidth and 14mW power from a 1.8V supply. The symmetric feedback TIA gain is reduced by 4.7dBΩ below the pole, while the common-mode feedback TIA gain of 53.9dBΩ is reduced by only 0.4dBΩ, due to mismatch of the amplifier outputs resulting from the single-ended to differential conversion.

The symmetric feedback TIA was fabricated with a capacitor array at the input to allow characterization over a range of input capacitance and was measured on an RF probe station. The input was driven electrically with a 200μA PRBS, external capacitance was included at V_{i-}, and the TIA output was amplified by a LIA prior to output probing. Fig. 6A shows the 12.5Gb/s TIA eye measured with 260fF input capacitance, which is a realistic value for commercial photodiodes. Fig. 6B shows that the same TIA operates at 18Gb/s when input capacitance is scaled to 90fF. Fig. 7 shows die photos of the fabricated TIA and VCSEL driver.

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