A 500MS/s 5b ADC in 65nm CMOS

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Abstract

A 1.2V 6mW 500MS/s 5-bit ADC for use in a UWB receiver has been fabricated in a pure digital 65nm CMOS technology. The ADC uses a 6-channel time-interleaved successive approximation register architecture. Each of the channels has a split capacitor array to reduce switching energy and sensitivity to digital timing skew. A variable delay line is used to optimize the instant of latch strobing to reduce preamplifier currents.
Keywords: UWB, ADC, SAR, CMOS, time-interleaved

Introduction

Ultra-wideband (UWB) radio is an emerging technology that shows promise for very-high-data-rate wireless communication over short distances. High speed (>500MS/s) and low resolution (4-5b) ADCs are required to convert these signals. It is desirable for integration of the ADC directly with the high-performance UWB digital baseband processor in a deep sub-micron CMOS process for best digital performance. Low-power time-interleaved successive approximation register (SAR) ADCs have been demonstrated at the speeds necessary for UWB radio [1], [2]. The SAR topology is well suited for implementation in deep sub-micron CMOS due to its very low analog complexity.

This paper presents a 500MS/s 5-bit ADC in pure-digital 65nm CMOS. The ADC has 6 time-interleaved channels synchronized to a common clock; each channel uses six clock periods to perform a conversion (one for sampling followed by five bit-cycles); thus the channels sample sequentially every clock period. The ADCs have been designed to take advantage of the process technology without sacrificing robustness in the presence of increased variability. Two new techniques are incorporated to improve energy-efficiency. A split capacitor array reduces switching energy and is robust to digital delay mismatches. In the comparator, a variable delay line and on-chip delay detector optimize the instant of strobing for the regenerative latch to lengthen settling times for preamplifiers.

Technology Considerations

Deep sub-micron CMOS provides both opportunities and challenges for mixed-signal design. The SAR architecture can benefit greatly from reduced features sizes because it has significant digital but little analog complexity. The two principal analog blocks in a SAR converter are the capacitor array DAC and the comparator. The former benefits directly from the reduced gate length and lower on resistance of the switches. Sampling at the lower power supply (1.2V) is achieved by constraining the input voltage to the 0-0.4V range; thus a standard V_T NMOS samples the input. The comparators use a two stage preamplifier and a regenerative latch. Each preamplifier, seen in Fig. 2(a), uses non-minimum length input transistors to improve both matching and output impedance. While this increases the device capacitance for the same g_m, the presence of wiring parasitics reduces the overall impact.

Split Capacitor Array

The DAC is the first implementation of the split capacitor array, wherein the MSB capacitor is split into an identical copy of the rest of the array, theoretically analyzed in [3]. This array is predicted to have 37% lower switching energy than the conventional array and 1-step switching method without any increase in total capacitance or area. Besides the energy savings presented in [3], the split capacitor array is also well suited for high-speed implementations. In a conventional array, when two capacitors are required to transition on a given bit-cycle, variation in digital propagation delays can cause the array output to initially transition in the wrong direction, producing a large overdrive condition for the preamplifiers, increasing their settling times. In the split capacitor array, only one capacitor switches during any bit-cycle, providing inherent robustness against these digital timing skews, as shown in Fig. 1. Under the worst-case timing skew, the settling time is reduced by 10%.

Optimized Latch Strobing

During bit-cycling, the clock period is divided into one phase for the settling of the DAC and preamplifiers and one phase for regeneration of the latch. The latch typically resolves in much less than one 1ns even for very small inputs. The ADC sits idle after the latch settles until the start of the next bit-cycle. Self-timed bit-cycling has been proposed to use this idle time to start the next bit-cycle early [4]. This approach relaxes the preamplifier settling time requirement for all but the first bit-cycle (determining the MSB), as it has no prior bit-cycle from which to borrow. Here, a variable delay line has been inserted in series with the latch strobe signal (Fig. 2(a)) to extend analog settling time in the first half of every bit-cycle, including the first, "pre-borrowing" time from that bit-cycle's own latch phase. The slower speed requirements

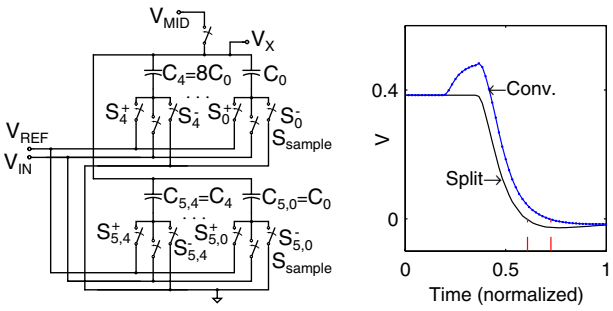

Fig. 1. 5-bit split capacitor array and simulated settling behavior under the presence of digital timing mismatch.

allows reduced preamplifier currents. To tune this delay for various clock frequencies and operating conditions, an on-chip delay detector has been designed, shown in Fig. 2(b). The latch's inputs are shorted to produce the worst case settling behavior and its outputs are captured both by a replica of the SAR digital path (R_1–R_2) and the $Done$ signal in R_3–R_4. Any difference between these outputs is an indication of the failure of the latch to resolve fast enough to meet the setup time constraints of R_1–R_2, and thus the delay should be reduced. An off-chip loop is used to determine the frequency of errors and tune the delay via a configuration register. This function could be implemented on-chip with a counter and a simple finite state machine.

Measured Results

The ADC has been fabricated in a pure-digital 65nm CMOS technology with a nominal supply voltage of 1.2V. At 500MS/s, the analog and digital supplies, excluding I/O power, consume 2.86mW and 3.06mW, respectively. Using a separate on-chip test channel with the conventional array and switching method, the measured DAC energy savings for the split capacitor array is 31%, which closely matches the theoretical model; increased bottom-plate routing accounts for the difference. The static linearity is $-0.16/0.15$ INL and $-0.25/0.26$ DNL (Fig. 3); the split capacitor array shows no linearity degradation versus the conventional array. The dynamic results are presented in Fig. 4. The SNDR does not drop by 3dB until past the Nyquist frequency. An FFT of a 239.04 MHz input sampled at 500MS/s is shown in Fig. 5. The level of offset voltage mismatch and timing skew is sufficiently low for proper reception of UWB signals. Using the figure of merit in [1], $(P/(2^{ENOB}2f_{in}))$, at the Nyquist frequency, the ADC achieves 755fJ/conv. step. At 250MS/s, 420fJ/conv. step is achieved by lowering the voltage supplies. The die photograph is shown in Fig. 6.

Acknowledgments The authors would like to thank Texas Instrumnts for fabricating the chip. This work is funded by NSF, DARPA, and an NDSEG Fellowship.

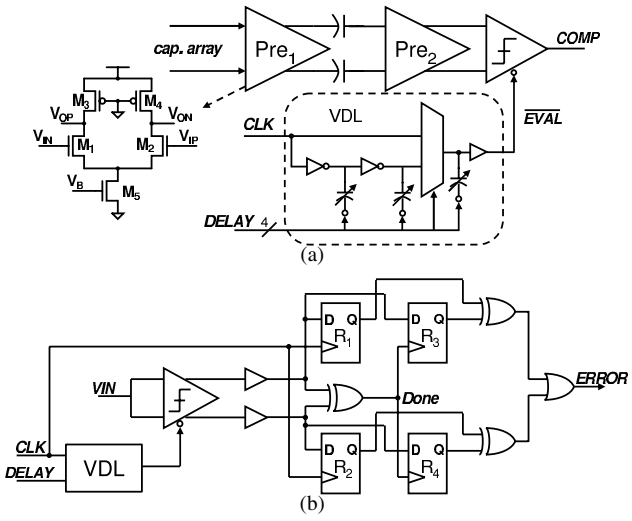

Fig. 2. Variable delay line to extend preamplifier settling times in (a) the comparator circuit and (b) the latch-delay-detect circuit.

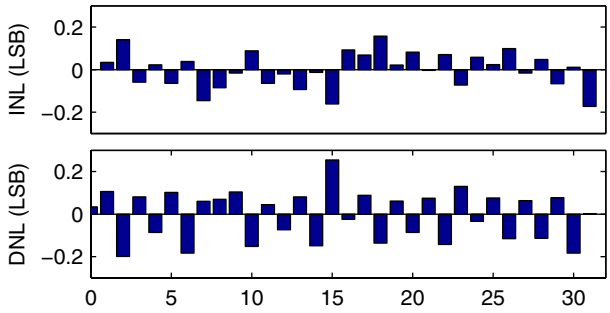

Fig. 3. INL and DNL versus output code.

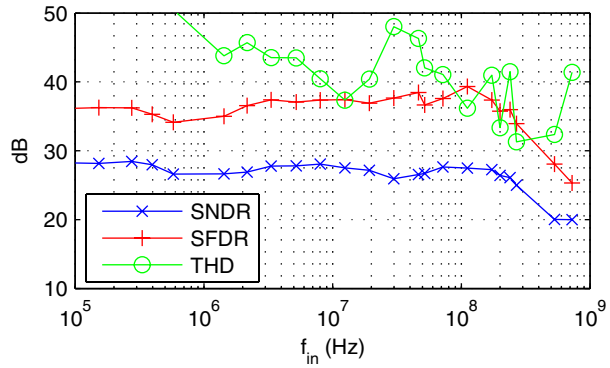

Fig. 4. SNDR and SFDR versus input frequency.

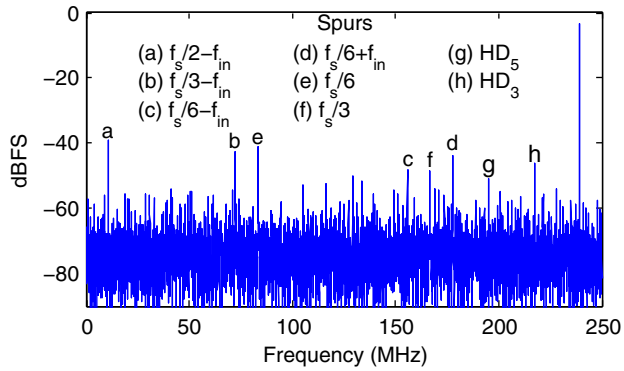

Fig. 5. FFT of 239.04MHz sine wave sampled at 500MS/s with dominant spurs labeled. (a)-(d) are from timing skew, and (e)-(f) are from offset mismatch

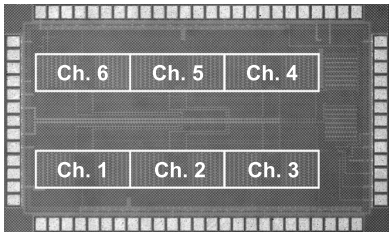

Fig. 6. Photograph of 1.9×1.2mm die.

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