An Energy-Efficient Charge Recycling Approach for a SAR Converter With Capacitive DAC

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***Abstract*— A new method for switching the capacitors in the DAC capacitor array of a successive approximation register (SAR) ADC is presented. By splitting the MSB capacitor into $b-1$ binary scaled sub-capacitors, the average switching energy of the array can be reduced by 37% compared to a conventional switching method. A formal solution of the switching energy in four different switching methods is included, and the equations are verified using HSPICE simulations of a 10b capacitor array in a 0.18μm CMOS process.**

I. Introduction

The SAR ADC is a popular topology, widely used for medium-to-high-resolution converters [1], and more recently for high-speed, low-power converters [2]. The dominant sources of power dissipation in a SAR converter are the comparator and the switching of the capacitor array. The conventional switching method efficiently charges the capacitor array during half of the bit cycling, but it is highly inefficient in the other half, throwing away charge that has been stored onto the array. We propose splitting the largest capacitor of the array into its own subarray, and thus maximize energy savings during switching. This method is compared in terms of energy efficiency in Section III to three other switching methods.

II. SAR Algorithm and Converter

A typical SAR converter is shown in Fig. 1. A capacitive DAC and a shift register produce an approximation of the input signal. The comparator, composed of preamps and a latch, determines whether this approximation is too high or too low. The approximation is improved knowing the result of the last comparison, and the process is repeated until the entire digital word is decoded. Fig. 2 shows the DAC capacitor array. The algorithm [3] is described below.

Initially, S_{sample} is high, and the entire capacitor array stores the voltage $V_{MID} - V_{IN}$. Then, at time 0, the MSB cap, C_b is connected to V_{REF}, causing V_X to settle to

$$V_X[1] = V_{MID} - V_{IN} + \frac{V_{REF}}{2} \tag{1}$$

and the latch output is

$$D_1 = \begin{cases} 1 & V_{IN} < V_{REF}/2 \\ 0 & V_{IN} > V_{REF}/2 \end{cases} \tag{2}$$

The latch output controls the next switch transition. If D_1 is low, the second largest capacitor is connected to V_{REF} ($S_{b-1}^+ = 1$), raising the voltage at V_X (we shall call this an "up" transition). If, on the other hand, D_1 is high, C_b is returned to ground and C_{b-1} is connected to V_{REF} (a "down" transition).

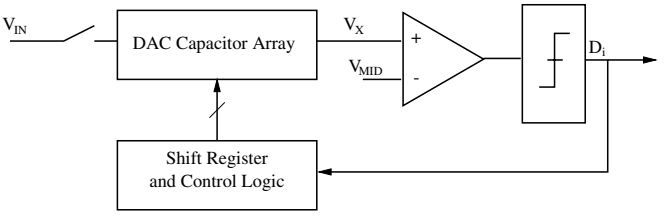

Fig. 1. Block diagram of a SAR ADC. The input is sampled directly onto a DAC capacitor array; the logic and shift register control the switching of the array to approximate the sampled input one bit at a time.

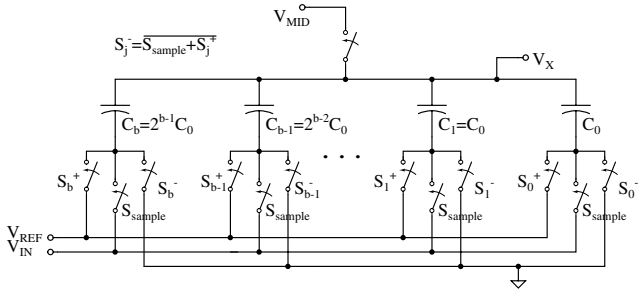

Fig. 2. b-bit single-ended DAC capacitor array.

The above process is repeated for successive capacitors in the array. At each stage, the value of V_X, after switching transients have settled, is

$$V_X = V_{MID} - V_{IN} + \frac{C_T}{C_T + C_B} V_{REF} \tag{3}$$

where C_T is the sum of all capacitors connected to the reference voltage, and C_B is the sum of all capacitors connected to ground:

$$C_T = \sum_i 2^{i-1} C_0 \quad \text{for } i \text{ such that } S_i^+ = 1 \tag{4}$$

$$C_B = \sum_i 2^{i-1} C_0 \quad \text{for } i \text{ such that } S_i^+ = 0 \tag{5}$$

III. Capacitor Switching Methods

During every bit cycle, either an "up" or a "down" transition occurs. This section analyzes four different methods of switching. All four methods behave identically for an "up"

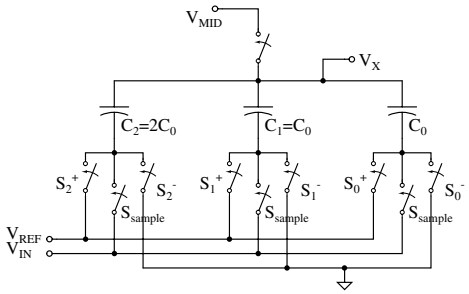

Fig. 3. 2-bit capacitor array for 1 step and 2 step switching methods.

transition; they only differ when a capacitor must be switched back from the reference voltage to ground.

For ease of computation, all calculations in this section are done for the 2-bit capacitor array shown in Fig. 3. The equations presented can be generalized to an arbitrary size capacitor array, as is done in the Matlab model in Section IV.

Assume that at time 0^-, the input voltage has been fully sampled on the capacitor array and that all switches are open. At time 0, the bottom plate of the C_2 is switched to V_{REF}. The capacitor array is then charged to reach the final value in (1). If the capacitor array settles in time T_P, the total energy drawn from V_{REF} is

$$E_{0\to1} = \int_{0^+}^{T_P} i_{REF}(t) V_{REF} dt = V_{REF} \int_{0^+}^{T_P} i_{REF}(t) dt \tag{6}$$

Since $i_{REF}(t) = -dQ_{C_2}/dt$ and charge continuity on a capacitor implies that $Q_{C_2}(0^+) = Q_{C_2}(0^-) = 2C_0V_X[0]$, (6) simplifies to

$$\begin{aligned} E_{0\to1} &= -V_{REF} \int_{0^+}^{T_P} \frac{dQ_{C_2}}{dt} dt = -V_{REF} \int_{Q_{C_2}(0^+)}^{Q_{C_2}(T_P)} dQ_{C_2} \\ &= -V_{REF}(Q_{C_2}(T_P) - Q_{C_2}(0^+)) \\ &= -V_{REF} 2C_0 \left((V_X[1] - V_{REF}) - V_X[0]\right) \\ &= C_0 V_{REF}^2 \end{aligned} \tag{7}$$

This result matches the intuition that the effective series capacitance of the array, C_0, must be charged from 0 to V_{REF}. For all following calculations, T_P is assumed to be 1 for ease of notation.

At the end of the first period of bit cycling, the value at the top plate of the capacitor array is compared to V_{MID}, producing D_1. If D_1 is 0, C_1 in Fig. 3 is connected to V_{REF}. As mentioned earlier, all four switching methods behave identically in this case, and the total energy drawn from V_{REF} can be computed as follows:

$$V_X[2] = V_{MID} - V_{IN} + \frac{3}{4} V_{REF} \tag{8}$$

$$\begin{aligned} E_{1\to2} &= -V_{REF}[2C_0 \left((V_X[2] - V_{REF}) - (V_X[1] - V_{REF})\right) \\ &\quad + C_0 \left((V_X[2] - V_{REF}) - V_X[1]\right)] \\ &= \frac{C_0 V_{REF}^2}{4} \end{aligned} \tag{9}$$

The following subsections present four different methods of performing the "down" transition if D_1 is 1 instead of 0.

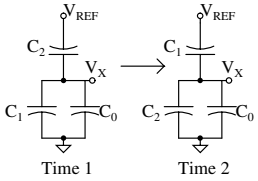

Fig. 4. A "down" transition for the 1 step switching method.

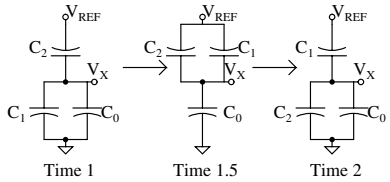

Fig. 5. A "down" transition for the 2 step switching method.

A. Conventional 1 Step Switching

The most straightforward method to switch down the MSB capacitor and switch up the MSB/2 capacitor is to switch them simultaneously as shown in Fig. 4. The energy drawn from V_{REF} while the capacitor array settles can be determined by:

$$V_X[2] = V_{MID} - V_{IN} + \frac{V_{REF}}{4} \tag{10}$$

$$\begin{aligned} E_{1\to2,\text{1step}} &= -V_{REF}[C_0 \left((V_X[2] - V_{REF}) - V_X[1]\right)] \\ &= \frac{5}{4} C_0 V_{REF}^2 \\ &= E_{TOP} + E_{SW} \end{aligned} \tag{11}$$

Here, E_{TOP} and E_{SW} represent the energy required to drive the change in V_X and to charge the new capacitor from ground to V_{REF}, respectively. They are defined as:

$$\begin{aligned} E_{TOP} &= -C_T V_{REF}(V_X[2] - V_X[1]) \\ &= C_T V_{REF}(-\Delta V_X) \end{aligned} \tag{12}$$

$$E_{SW} = C_0 V_{REF}^2 \tag{13}$$

While this method is the simplest to implement in terms of numbers of switches and clock edges, the ratio of (11) to (9) hints at a significant inefficiency, since it requires five times more energy to lower V_X than to raise it by the same amount.

B. 2 Step Switching

The second proposed method accomplishes the same transition using two switching steps instead of one. During the first step (considered from time 1 to 1.5), both C_2 and C_1 are connected to V_{REF}. This transition is identical to that in (8)-(9). Then, at time 1.5, the largest capacitor is disconnected from V_{REF} and connected to ground, as seen in Fig. 5, drawing energy

$$\begin{aligned} E_{1.5\to2} &= -C_0 V_{REF}(V_X[2] - V_X[1.5]) \\ &= \frac{C_0 V_{REF}^2}{2}. \end{aligned} \tag{14}$$

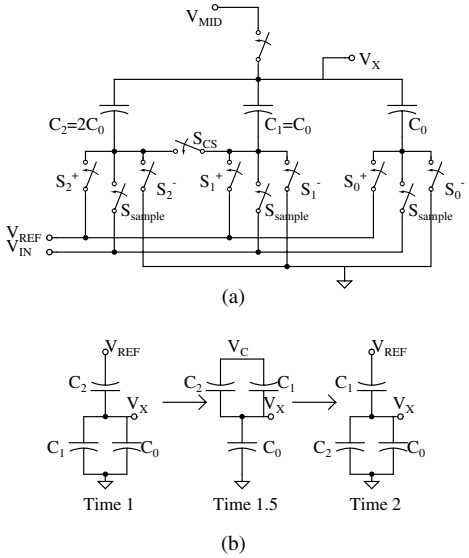

Fig. 6. Capacitor (a) array and (b) equivalent circuits for the charge sharing method. When $S_2^+ = S_1^+ = 0$ and $S_{CS} = 1$, C_1 is charged up from C_2 with no energy drawn from the supply.

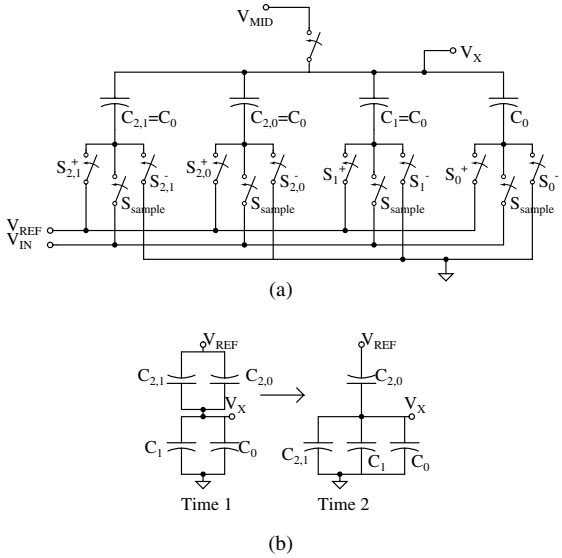

Fig. 7. The (a) modified array and (b) switching method for a two-bit capacitor array where C_2 has been split into two sub-capacitors, $C_{2,1}$ and $C_{2,0}$.

The total switching energy is thus

$$\begin{aligned} E_{1\to 2,\text{2step}} &= E_{1\to 1.5} + E_{1.5\to 2} = \frac{3}{4} C_0 V_{REF}^2 \\ &= E_{TOP} + E_{SW} + 2C_0 V_{REF} \Delta V_X \end{aligned} \tag{15}$$

Since $V_X[2] < V_X[1]$, the last term above is negative and (15) is less than (11). Qualitatively, some of the charge transferred to C_1 is reused from C_2, similar to a charge recovery scheme in switching of large data buses [4].

C. Charge Sharing (CS)

The previous subsection shows that energy savings can be achieved by using some of the charge from the largest capacitor to charge up the second capacitor. An extension of this method can be used for additional savings. Fig. 6(a) shows a modified capacitor array, with an additional switch S_{CS}. As in the above subsection, the switching is done in two phases, as seen in Fig. 6(b). In the first phase, the first two capacitors are disconnected from V_{REF} and ground and connected to each other through the new switch. During this phase, no energy is drawn from V_{REF}. Using charge conservation, the voltage at node V_C at the end of the first phase is

$$V_C[1.5] = \frac{2}{3} V_{REF}$$

Therefore, the MSB/2 capacitor is effectively charged to two-thirds of the reference voltage with zero energy expenditure.

During the second phase, the MSB capacitor is connected to ground and the MSB/2 capacitor is connected to V_{REF}. The total energy dissipated is therefore

$$\begin{aligned} E_{1\to 2,\text{CS}} &= -C_0 V_{REF} \left((V_X[2] - V_{REF}) - (V_X[1] - V_C) \right) \\ &= \frac{7}{12} C_0 V_{REF}^2 = E_{TOP} + \frac{1}{3} E_{SW} \end{aligned} \tag{16}$$

D. Capacitor Splitting

Even though charge sharing can save much of the energy in a "down" transition, some energy must still be spent charging up C_1 to V_{REF} (namely, the total energy includes a contribution from E_{SW}). To avoid charging any capacitor to V_{REF} during a "down" transition, the final method splits the MSB capacitor into two capacitors of value C_0, and then switches down one of them. This capacitor splitting results in the capacitor array shown in Fig. 7(a).

During the first bit cycle, $C_{2,1}$ and $C_{2,0}$ are both connected to V_{REF}, dissipating the energy (7). After time 1, instead of connecting C_1 to V_{REF}, $C_{2,1}$ is simply connected directly to ground, as in Fig. 7(b). This requires the energy

$$\begin{aligned} E_{1\to 2,\text{split}} &= -V_{REF} C_0 (V_X[2] - V_X[1]) \\ &= \frac{1}{4} C_0 V_{REF}^2 = E_{TOP} \end{aligned} \tag{17}$$

Thus, the capacitor splitting approach requires no energy spent to charge up a capacitor from ground to V_{REF} during a "down" transition and has achieved the same energy for an "up" and a "down" transition.

For a b-bit converter, the conventional capacitor array in Fig. 2 is modified by splitting C_b into a copy of the rest of the capacitor array, as shown in Fig. 8. During the first bit cycle, all sub-capacitors $C_{b,0} \ldots C_{b,b-1}$ of the MSB capacitor are connected to V_{REF}. For subsequent "up" transitions, the C_i in the main array is connected to V_{REF}, while for any "down" transition, the sub-capacitor $C_{b,i}$ is connected to ground. Because the capacitor array is conventionally arranged using a common centroid layout with a C_0 unit capacitor, splitting the MSB capacitor requires no extra area for the capacitor array. This approach requires twice as many switches; however,

TABLE I

SWITCHING METHODOLOGY COMPARISON

Method	E_{UP}	E_{DOWN}	# of Switches	# of Phases	Norm. $E_{uniform}$	Norm. E_{sine}
1 step	$E_{TOP}+E_{SW}$	$E_{TOP}+E_{SW}$	$b+1$	1	1.000	1.000
2 step	$E_{TOP}+E_{SW}$	$E_{TOP}+E_{SW}-2^iC_0V_{REF}\Delta V_X$	$b+1$	2	0.897	0.893
CS	$E_{TOP}+E_{SW}$	$E_{TOP}+E_{SW}/3$	$2b$	2	0.760	0.749
Splitting	$E_{TOP}+E_{SW}$	E_{TOP}	$2b$	1	0.635	0.623

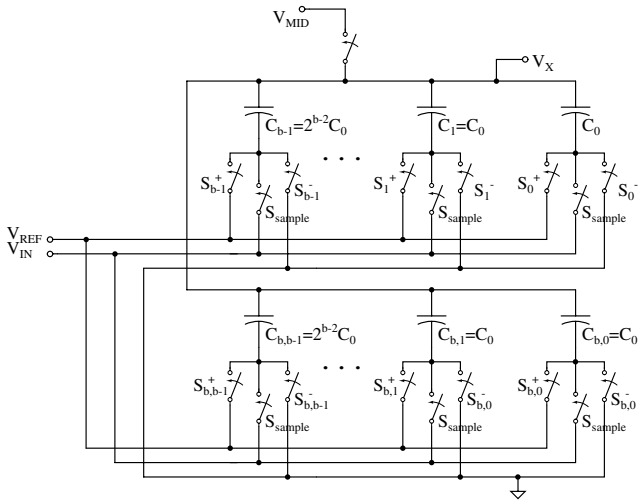

Fig. 8. b-bit split capacitor array for reduced switching energy. The largest capacitor has been split into binary scaled capacitors.

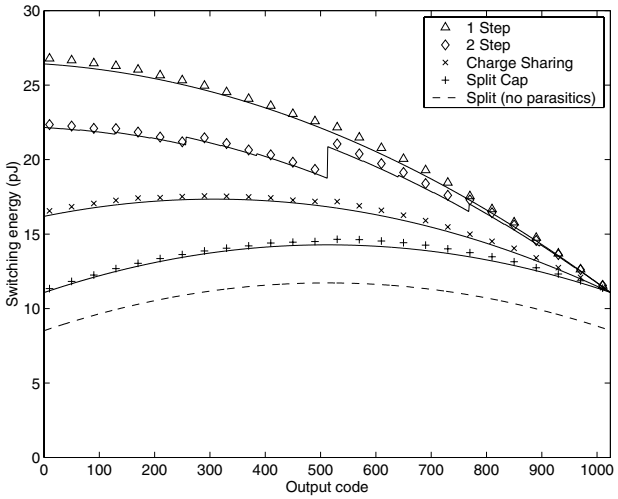

Fig. 9. Plot showing the energy versus output code required for the switching of the capacitor array. The HSPICE data points are plotted against the Matlab models (solid lines). The bottom curve shows the effect of parasitics on the Matlab model.

switches are generally small, so the area penalty is minimal.

IV. SIMULATION RESULTS

The above four switching methods have been applied to a 10b capacitor array. A Matlab model using generalized forms of (9), (11)-(13), and (15)-(17) has been developed. Fig. 9 compares this model to an HSPICE simulation of a 10b capacitor array in a CMOS 0.18 μm process.

As can be seen in the figure, neglecting parasitics on the bottom plate of the capacitors causes the model to greatly underestimate the energy. The best capacitors available on the process are poly-poly capacitors with a 20fF parasitic bottom plate capacitance for $C_0 = 100$fF.

The simulations show clearly the energy savings that can be achieved using the different methodologies. At the highest output code, all transitions are "up", so all of the switching methodologies require the same energy. At lower output codes, more "down" transitions occur in the array, so the energy savings are greatest for the capacitor splitting method at this point.

The average overall switching energy for a uniformly distributed input signal as well as for a full swing sinusoidal input can be calculated from the simulated data. The capacitor splitting method saves 37% of the switching energy compared to the conventional one step switching scheme. A comparison of the four switching methods is described in Table I.

V. CONCLUSIONS

We have presented four different switching methodologies for the capacitive DAC in a SAR ADC. The energy inefficiency present in the conventional one step switching method has been eliminated in the new capacitor splitting technique. This requires the same size capacitor array as the conventional method and only one clock phase per bit cycle. This switching method may be used to significantly reduce the power consumption in an ADC.

VI. ACKNOWLEDGMENTS

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