Dual Scalable 500MS/s, 5b Time-Interleaved SAR ADCs for UWB Applications

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***Abstract*— A dual 500MS/s, 5b ADC chip is implemented in a 0.18μm CMOS process. The two ADCs have synchronized sampling for use in an I/Q UWB receiver. Each ADC has a 6-way time-interleaved successive approximation register topology and uses full custom logic, self-timed bit-cycling, and duty cycling of the comparator preamplifiers to enable 500MS/s operation with 7.8mW power consumption.**

I. Introduction

Ultra-wideband (UWB) communication has emerged as a technology that is capable of transmitting upwards of 480Mb/s over short distances. Due to the large signal bandwidths required by the FCC, Nyquist sampling of a down-converted UWB signal requires an analog-to-digital converter (ADC) with a sampling rate of at least 500MHz. It has previously been shown that only 4 bits are required for reception in both noise- and interference-limited regimes [1]. Two ADCs are needed for I/Q demodulation from RF.

This paper presents dual 500 MS/s, 5b ADCs, implemented in a 0.18μm CMOS process using a 6-way time-interleaved successive approximation register (SAR) topology. Full custom digital logic and self-timing are used to overcome some of the power and performance penalties of the SAR topology. Each ADC consumes 7.8 mW at the maximum sampling rate. A simple bit scaling capability is also provided to scale power consumption in response to changing channel conditions as part of a full UWB receiver.

II. Topology Considerations

High-speed, low-resolution ADCs are typically implemented using a flash topology [2], [3]. While flash can achieve the highest speed possible, the number of comparisons done for each sample grows exponentially with the resolution. Recently, a very low power time-interleaved SAR has been demonstrated with similar specifications [4]. A b-bit SAR converter only requires b comparisons, which can provide substantial power savings. As each comparison requires a full clock cycle, achieving a high sampling rate requires time-interleaving. By using 6 parallel slices, with each slice taking six clock periods to convert the input, a single 500MHz system clock can be used, easing clock distribution.

The block diagram of one of the ADCs is shown in Fig. 1(a). The two ADCs on the chip share the clock and the start generator block, as well as a reference voltage buffer (not shown). Each time-interleaved slice receives the common clock and analog input signal. Only one token, which starts a conversion, is passed between slices. The first slice's start signal is common to both ADCs so that the outputs $y[0]-y[5]$ are synchronized when passed to the digital back-end. The bit-scaling controller disables unused slices, as discussed in Section III-D.

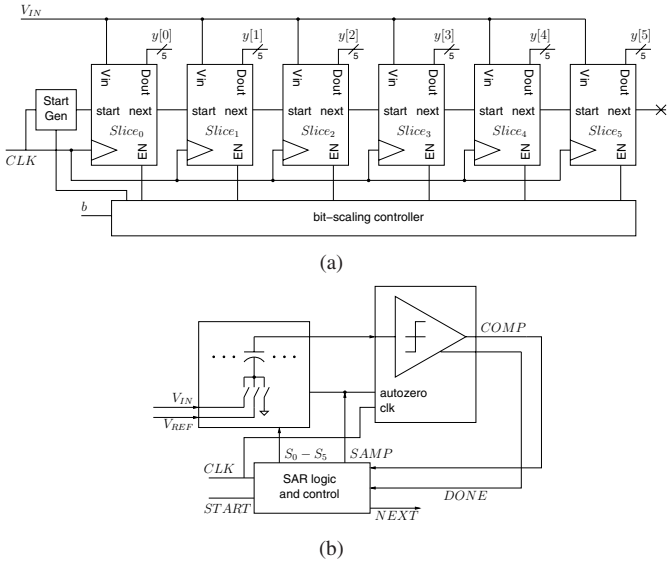


Fig. 1. (a) Top-level block diagram of ADC and (b) block diagram of each of the slices, $Slice_i$.

Each slice, as shown in Fig. 1(b), contains a DAC capacitor array that samples the input and subtracts the estimated output, a comparator consisting of a preamplifier and a latch, and a logic control block that controls the switching of the capacitor array. The figure shows a single-ended signal path, but the actual implementation is fully differential. The implementation details of the individual slices are further described in the next section.

III. Circuit Design

A. Self Timing

One disadvantage of the SAR architecture is the feedback required between successive clock periods. Specifically, the result of the previous comparison is necessary to generate an improved estimate for determining the next bit. While this feedback path is entirely digital, its latency must be minimized to allow maximum time for analog signals to settle in the DAC capacitor array and preamplifiers.

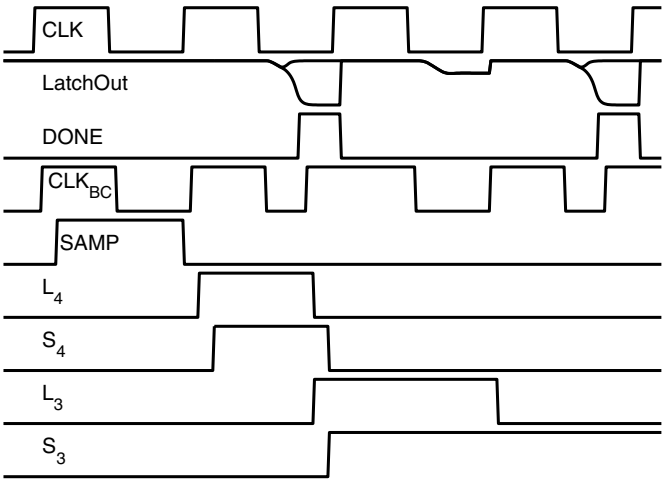


Fig. 2. Timing diagram showing sampling and the first three periods of bit-cycling. In the first bit-cycle, the $DONE$ signal triggers CLK_{BC} to start the next bit-cycle, whereas the second period shows that bit-cycling is triggered by CLK when the latch is metastable.

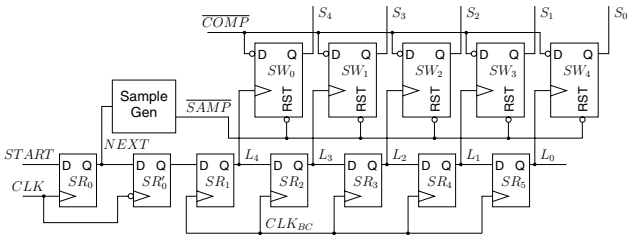


Fig. 3. SAR logic implementation. The shift registers $SR_0 - SR_5$ clock one of the switch drive registers $SW_0 - SW_4$ during every phase of bit-cycling. The outputs $S_0 - S_4$ control the DAC capacitor array.

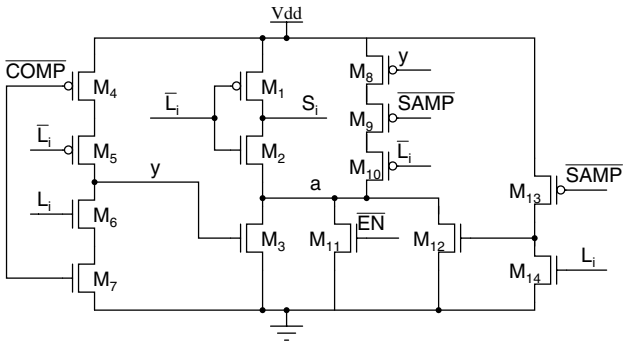


Fig. 4. Schematic of the switch drive registers.

To decrease the latency during bit-cycling, self-timing is used [5], wherein the latch triggers the start of the next bit-cycle when it has resolved a value. In effect, after the latch output has settled, the remainder of the second half of the clock period is borrowed by the DAC and preamplifiers for the next bit. Self-timing is particularly useful because the latch typically resolves in much less than 1ns (half the clock period).

The timing of the ADC is shown in Fig. 2, which considers the sampling operation and the first three bit-cycles. The assertion of $SAMP$ is delayed from the rising edge of CLK to avoid a high frequency current impulse on the analog inputs at the same time that the previous slice finishes sampling. During bit-cycling, the regeneration of the latch is always triggered by the falling edge of the system clock (CLK). In the first bit-cycle, the latch resolves quickly, asserting the $DONE$ signal (XOR of the latch outputs). This causes CLK_{BC}, the bit-cycling clock, to transition high immediately, rather than waiting for the rising edge of CLK. During the second period, the latch output is metastable and does not resolve. In this case, the rising edge of CLK_{BC} is triggered by CLK, and bit-cycling continues as normal.

B. SAR Logic

To implement a fast SAR controller, the logic, shown in Fig. 3, consists of a shift register ($SR_0 - SR_5$) and a set of switch drive registers ($SW_0 - SW_4$). $COMP$, the output of the comparator, is high ($\overline{COMP}$ low) when the DAC output (V_{REF} minus the current estimate of the input) is too high. The current bit being resolved is determined by $L_4 - L_0$, only one of which is high every period. Thus, S_i should go high on the rising edge of L_i. When L_i falls, the decision for that bit is made, bringing S_i back low only if $COMP$ is high.

This logic function is implemented in a single register, using a custom digital logic block based on dynamic registers, as shown in Fig. 4. Transistor M_1 provides a fast charge path for S_i upon the rising edge of L_i. $M_4 - M_7$ form a C^{2}MOS latch that holds the value of $\overline{COMP}$ after the falling edge of L_i and discharges S_i through $M_2 - M_3$. During sampling, $M_{12} - M_{14}$ reset S_i low. (L_i is guaranteed low at this point by logic in the shift register.) Transistors $M_8 - M_{10}$ are used to precharge node a to avoid charge sharing when M_2 turns on. Finally, M_{11} puts the register in a known state when disabled (e.g., due to bit scaling).

Using this custom logic mixed with conventional C^{2}MOS allows a faster and lower power SAR implementation. In simulations, the custom logic was 58% faster while consuming only 20% of the power of an equivalent SAR built using standard cells and static feedback flip-flops.

C. Comparator Design

The comparator is composed of two preamplifiers and a regenerative latch. The first preamplifier employs output offset compensation. To minimize current drawn by the preamplifiers when they are not actively settling, the current to the first preamplifier is disabled while the latch is resolving. The second preamplifier is kept active to ensure that the latch remains driven. The switches S_{p2} and parasitic capacitances C_{ip2}, shown in Fig. 5(a), hold the output of the first preamplifier when it is powered down.

The offset of the first preamplifier is stored on capacitor C_C during the sampling period. At this time, the second preamplifier is turned off. The bias current is disabled by M_5, shown in the preamplifier schematic in Fig. 5(b). The latch

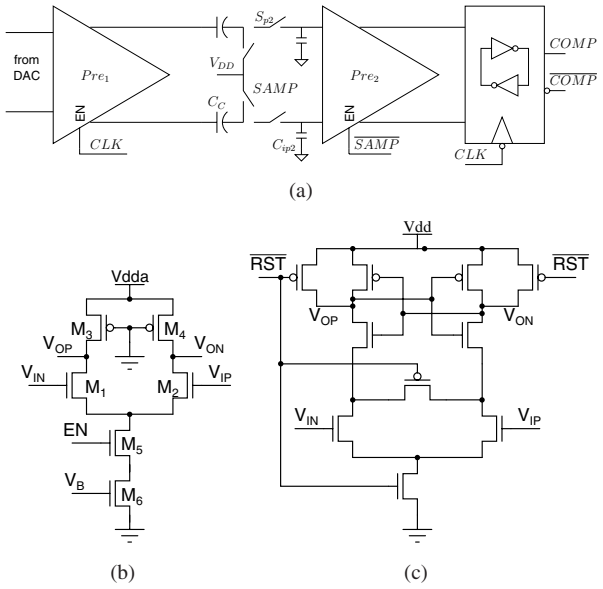


Fig. 5. (a) Comparator diagram with (b) preamplifier and (c) latch schematics.

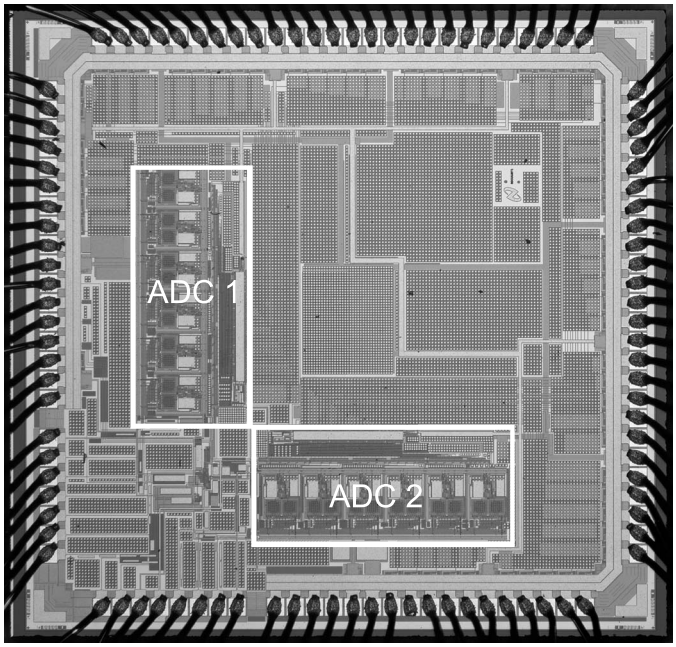


Fig. 6. Die photograph of ADC chip in 0.18μm CMOS. Total active area is 1.1mm^2.

(Fig. 5(c)) is a conventional sense-amplifier flip-flop [6].

D. Bit Scaling

For flexibility in response to varying system requirements, the ADC is capable of scaling the output resolution b from 1 to 5 bits at a constant sampling rate. Since each slice takes $b+1$ periods to resolve output, fewer slices are needed to maintain the same throughput; the unused $5-b$ slices are turned off by stopping the propagation of the $START$ signal, gating the clocks, and shutting off all bias currents. The start generation block triggers the first slice at a higher rate, which causes the $SAMP$ signal to assert at this higher slice sampling rate. As shown in Section III-B the $SAMP$ signal automatically resets bit-cycling, so the desired output resolution is achieved. A mux tree is also included to properly sort the outputs to ease the data processing of the digital back-end.

IV. Measured Results

The dual ADC chip was fabricated in a 0.18μm CMOS process with poly-poly capacitors. The die photograph of the ADC is shown in Fig. 6. The active area of each ADC is 1mm x 0.5mm. The parallel outputs of the two ADCs are output at the slice sampling rate of 83MHz and passed directly to the digital baseband. With a 500MHz sampling clock, the ADC exhibits an INL and DNL of $-0.26/0.42$ and $-0.39/0.33$ LSBs, respectively, as shown in Fig. 7. Each ADC draws $810\mu A$ from a 1.2V analog supply and 3.6mA from a 1.8V digital supply.

The dynamic performance at 500MS/s is shown in Fig. 8(a). The periodic behavior of SNDR is due to the time-interleaving. At the peak of the SNDR curve, the input frequency is aliased, with reference to the slice sampling rate, to low frequencies. The low effective resolution bandwidth (ERBW) is a result of insufficient settling time in the input sampling network.

TABLE I
Summary of measurements per ADC

Process	0.18μm, 1 poly, 5 metal CMOS
Resolution	5 bits
Active Area	1mm $\times$ 0.5mm
Sampling Rate	500MS/s
Analog Power	0.97mW @ 1.2V
Digital Power	6.5mW @ 1.8V
SNDR	20.2dB
SFDR	24dB
THD	-15dB

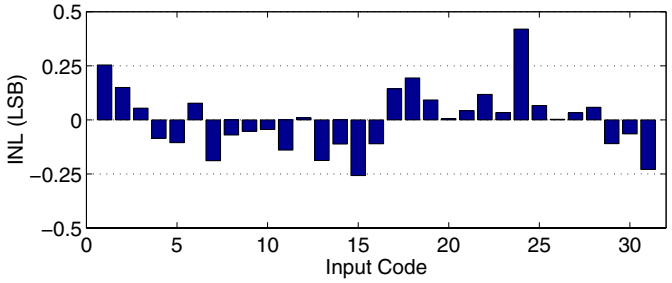
This has been confirmed by using a 125MHz sampling rate, with SNDR vs. frequency plotted in Fig. 8(b). At 125MS/s, the ADC has a figure of merit ($P/(2ERBW \cdot 2^{ENOB})$) of 1.1pJ/conversion step.

The FFT of a 170.56MHz input sampled at 500MS/s is shown in Fig. 9. The dominant harmonics are labeled. The spurs from offset between slices at multiples of $f_s/6$ are comparable to the third harmonic at -38dBFS. The spurious free dynamic range (SFDR) is better than 24dB, and the total harmonic distortion (THD) is better than -15 dB for input frequencies up to over 300MHz.

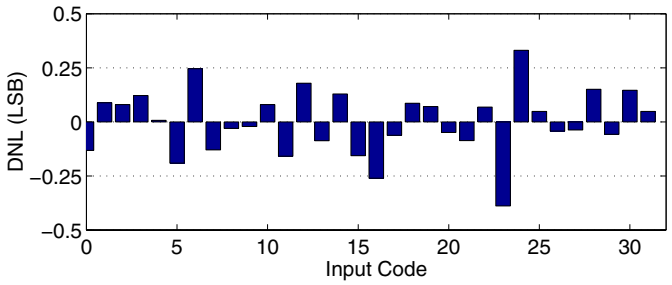
The prototype includes an optional mode to disable the duty cycling of the preamplifiers. Duty cycling reduces the analog power by 15% at 500MS/s. The power savings from bit scaling is shown in Fig. 10. Finally, the measurements are summarized in Table I.

V. Conclusion

A high-speed, low-resolution time-interleaved SAR converter has been presented that uses self-timing and efficient logic to achieve very high speed bit-cycling with maximum



(a)



(b)

Fig. 7. Plot of the (a) INL and (b) DNL vs. input code at 500MS/s.

time allocated for analog settling. Duty cycling of static bias currents in the comparator achieves analog power savings to produce a very low power implementation. A resolution scaling mechanism has also been designed to conserve power in response to changing system requirements. Two synchronized ADCs have been incorporated onto the same CMOS chip for use in a low-power I/Q receiver for ultra-wideband radio.

ACKNOWLEDGMENTS

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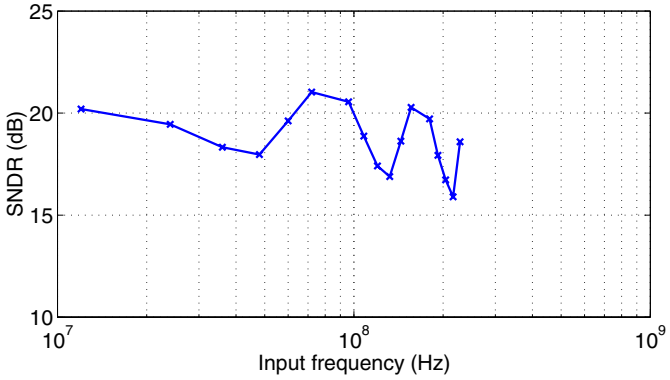
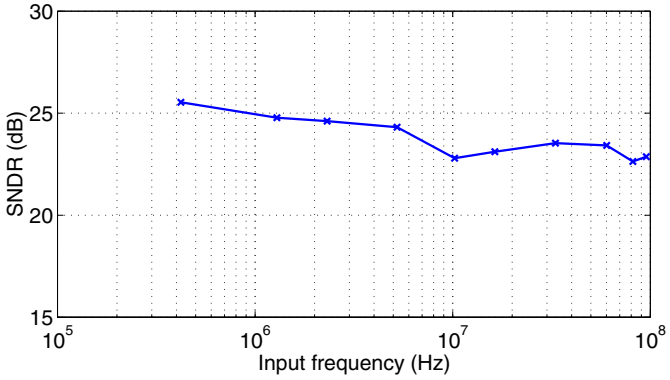


(a)



(b)

Fig. 8. Plot of SNDR vs. input frequency at (a) 500MS/s and (b) 125MS/s.

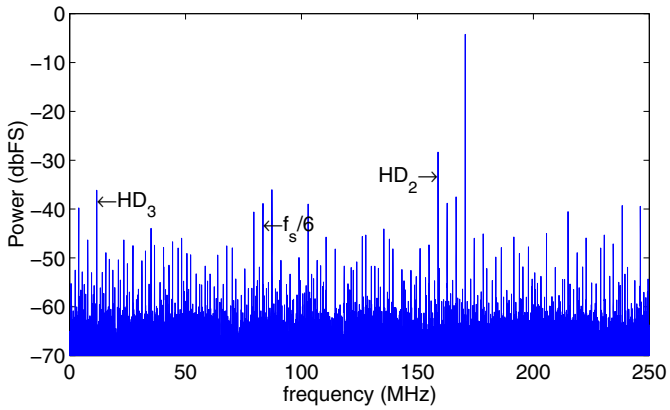


Fig. 9. FFT of a 170.56MHz input signal sampled at 500MS/s.

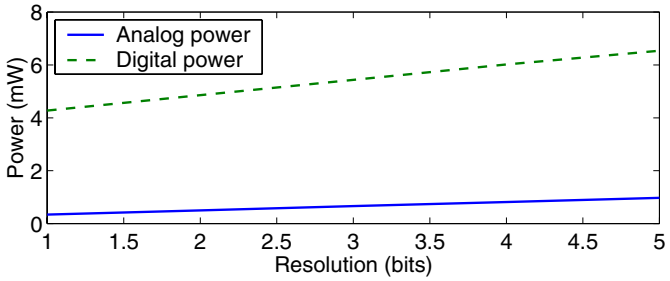


Fig. 10. Analog and digital power consumption vs. resolution for 500MS/s operation.