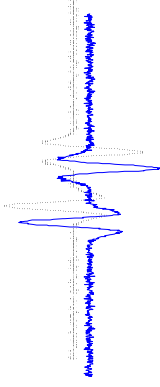
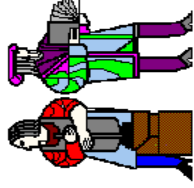


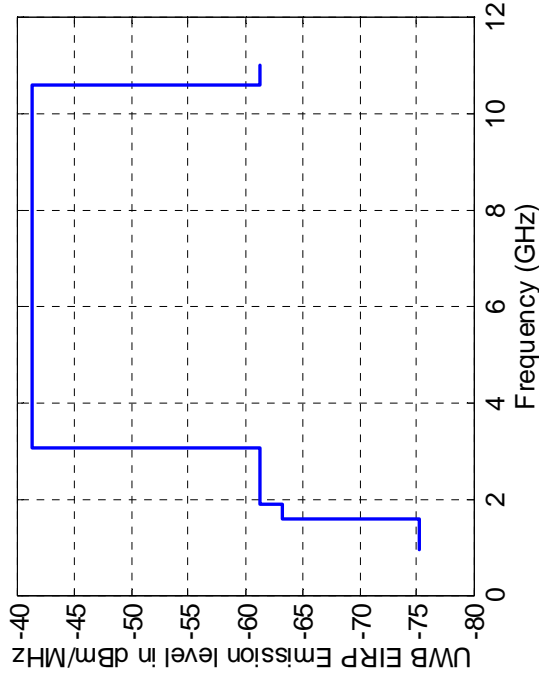
# Architectures for Energy-Aware Impulse UWB Communications



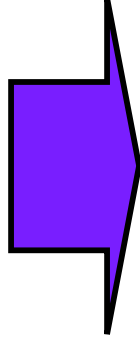
Raul Blazquez, Anantha P. Chandrakasan  
**Massachusetts Institute of  
Technology**



# UWB Radio



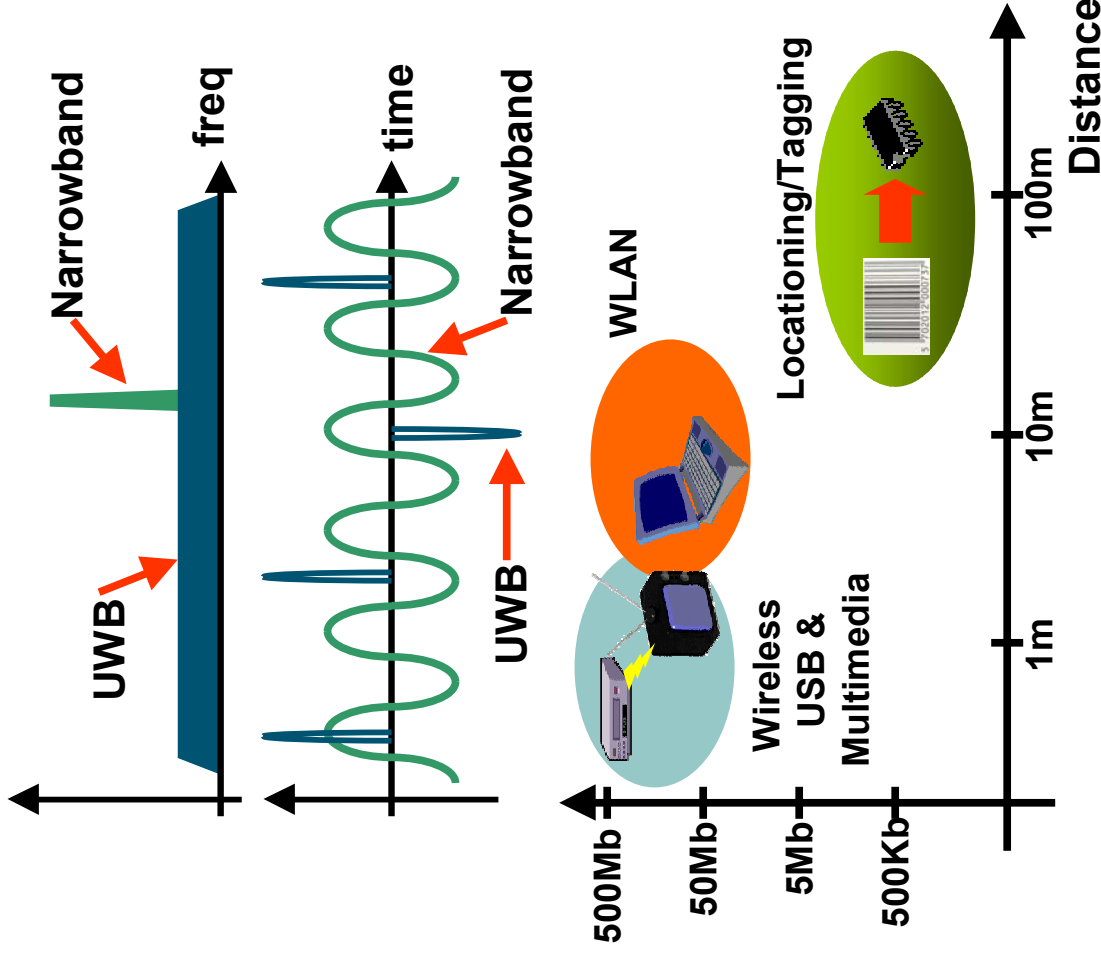
**7.5GHz of free unlicensed spectrum**



**High Data Rate**

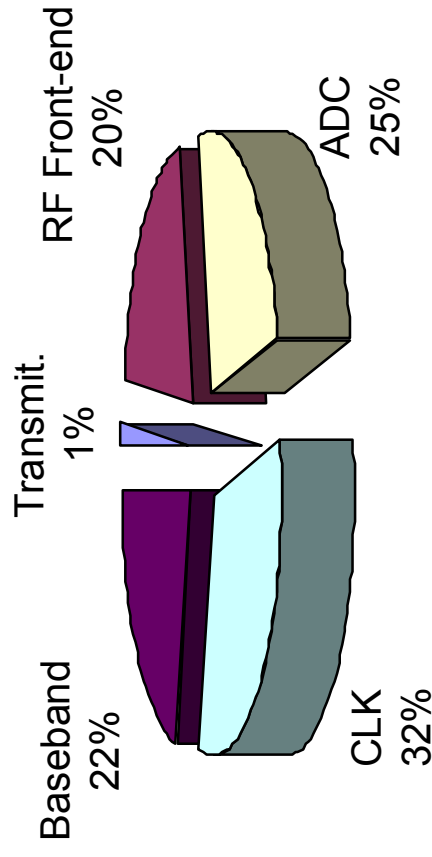
**Excellent Multipath Resolution**

**Low Interference to other systems**



# Power Budget for a UWB Transceiver

- MB-OFDM :
  - Front-end: 117.5 mW (Bergervoet et al. ISSCC'05)
  - Clock and carrier: 73.44 mW (Leenaerts et al. ISSCC'05)
  - Digital Back-end: 523 mW (Liu et al. ISSCC'05)
  - Estimated for 90nm CMOS (MBOA White paper): 93mW Tx, 169mW Rx



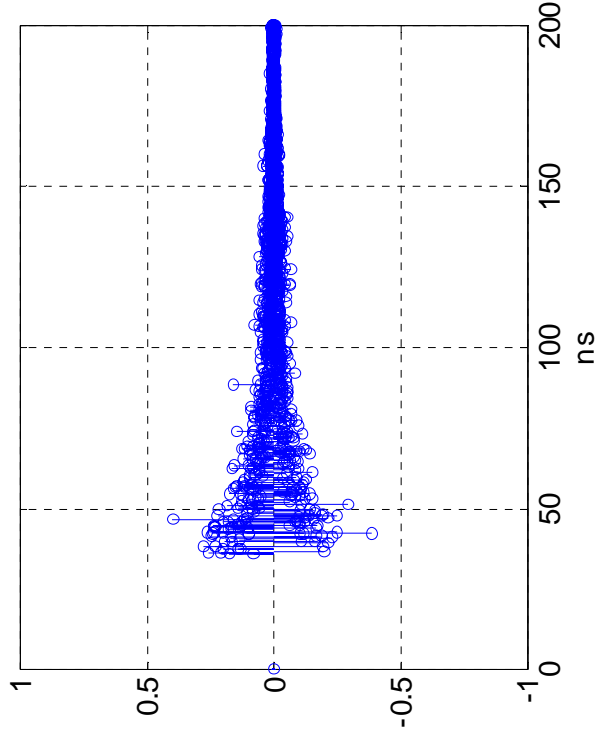
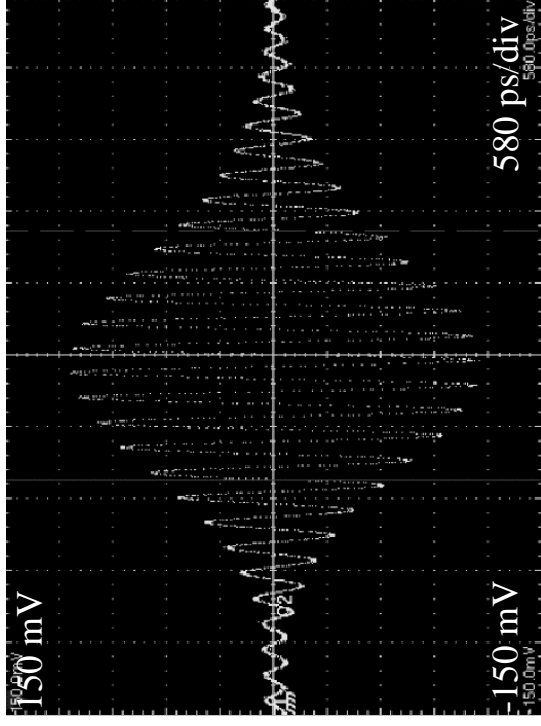
- Pulse UWB (DSSS)

- Total: 280mW (Iida et al. ISSCC'05)

**ADC and Digital baseband dominate the receiver**

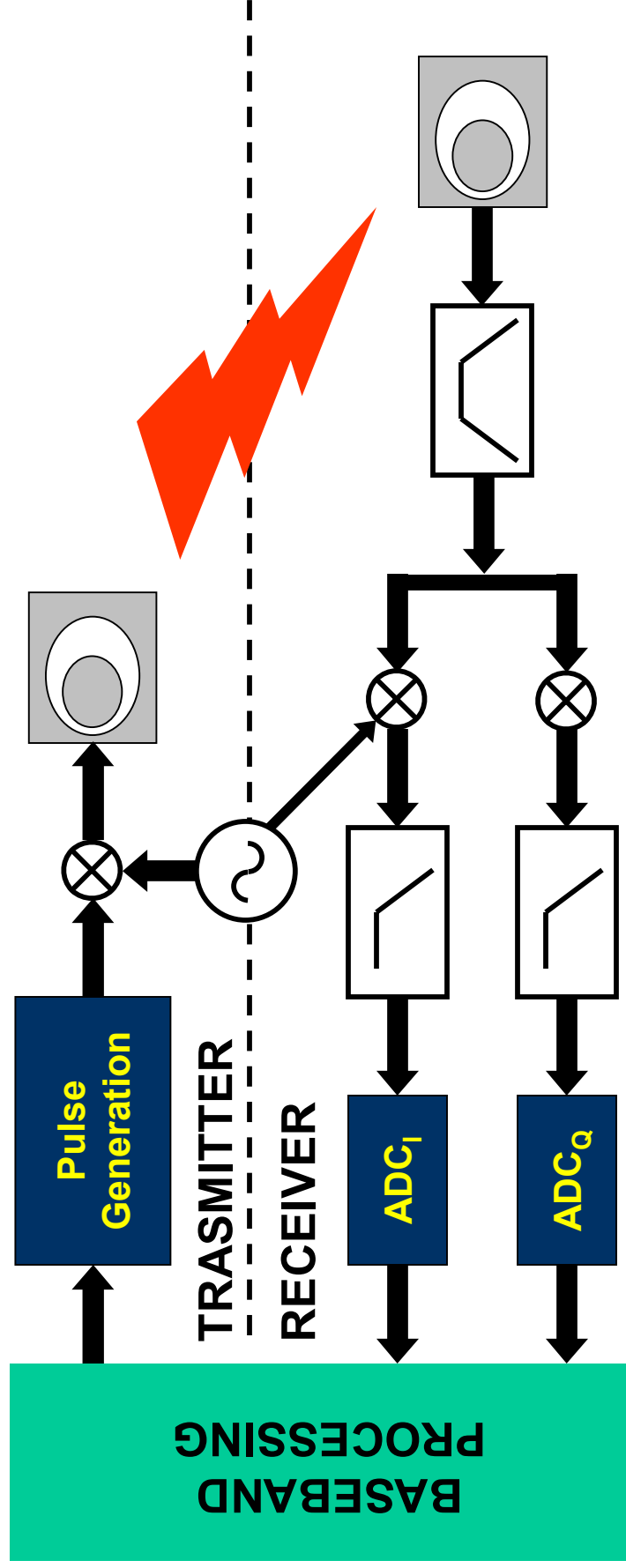
# Transceiver Specification

- 100 Mbps
- $BW_{\min} = 500 \text{ MHz}$
- Limitations:
  - Interferers (802.11a)
  - Multipath.



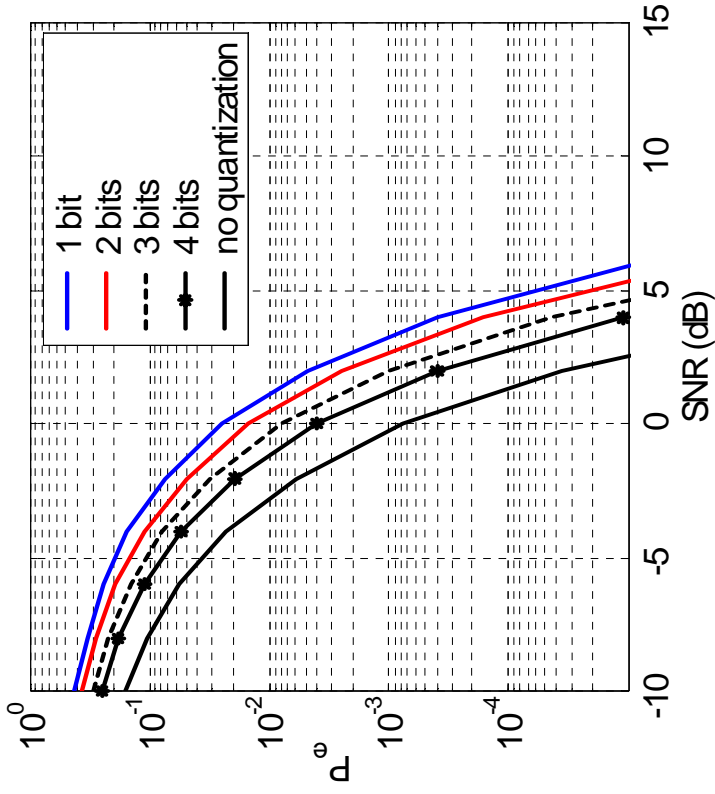
	Description	RMS Delay
CM1	LOS 0-4m	5.3ns
CM2	NLOS 0-4m	8.0ns
CM3	NLOS 4-10m	14.3ns
CM4	Extreme NLOS	25ns

# Direct Conversion Architecture

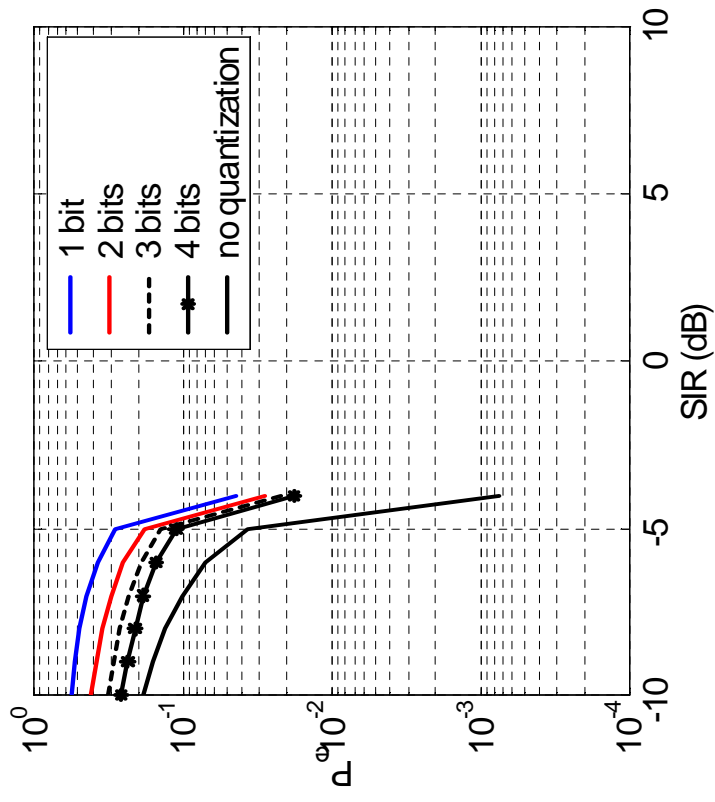


Sampling Rate: 500 Msps

# Specification of the ADC



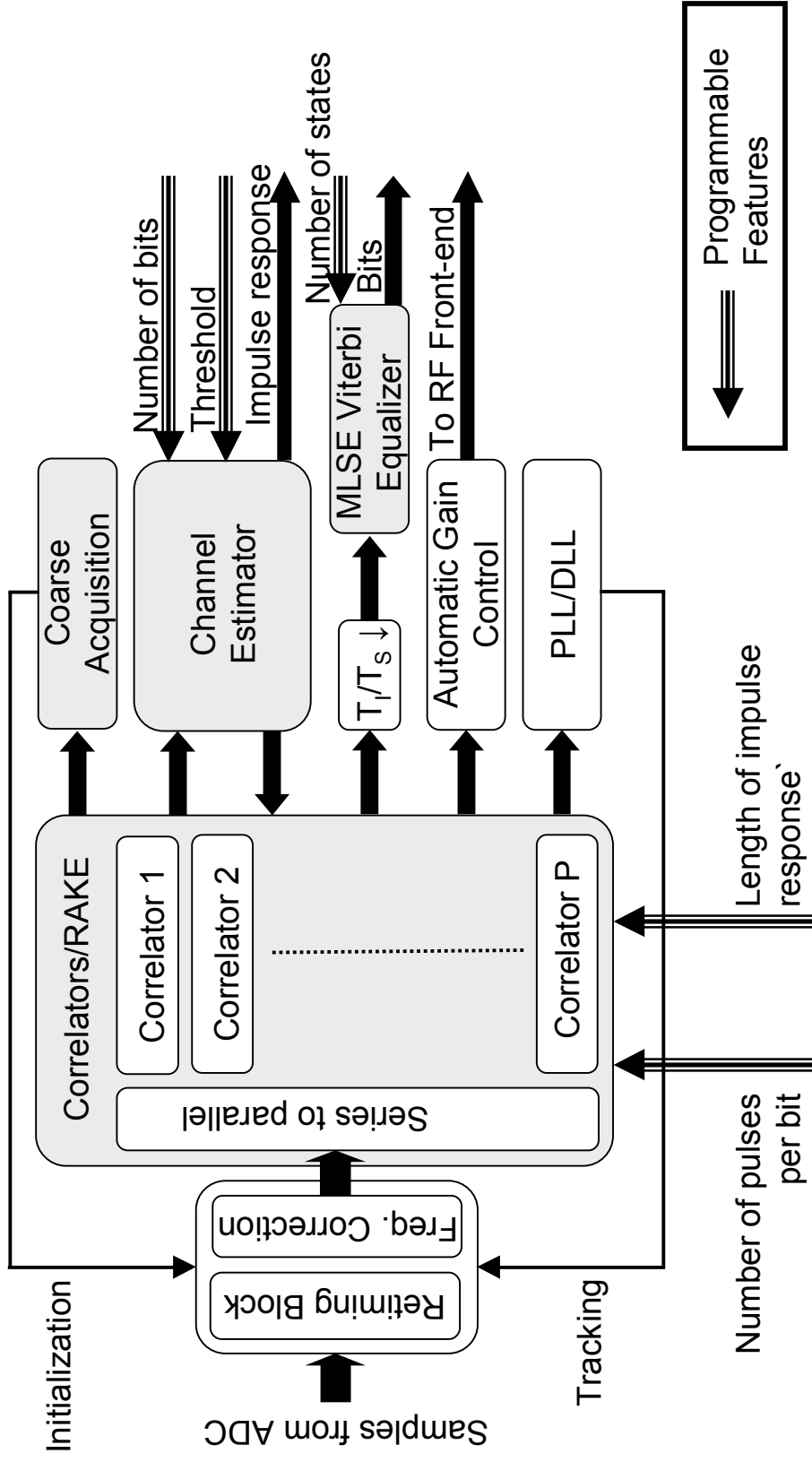
**Noise Limited Case**



**Interference Limited Case**

**4 bits sufficient for reliable UWB detection**  
**Scale down number of bits to save power**

# Energy Aware Baseband



Estimate Channel Quality  $\Rightarrow$  Adapt to minimize power

# Parallelization

- Wider integration window?

2 samples per pulse

$N_c$  pulses per bit

Case 1: 1 window  $\Rightarrow$  Width  $N$

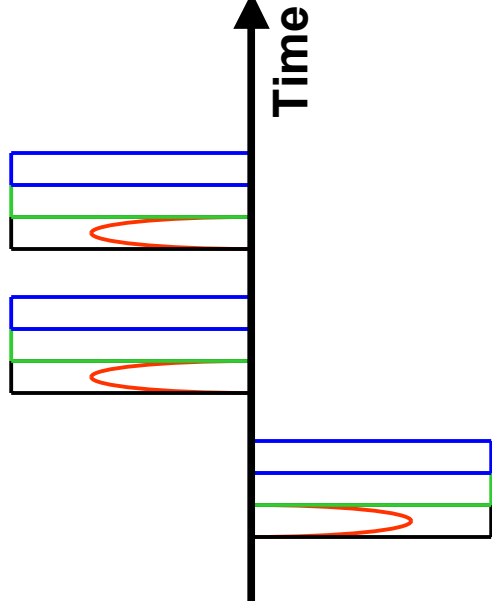
$2N_c N$  multiplications

$2N_c N - 1$  additions

Case 2:  $N$  windows  $\Rightarrow$  Width 1

$2N_c N$  multiplications

$2N_c N - N$  additions



Number of trials  $\propto N_c / \text{Duty cycle}$



# Correlators

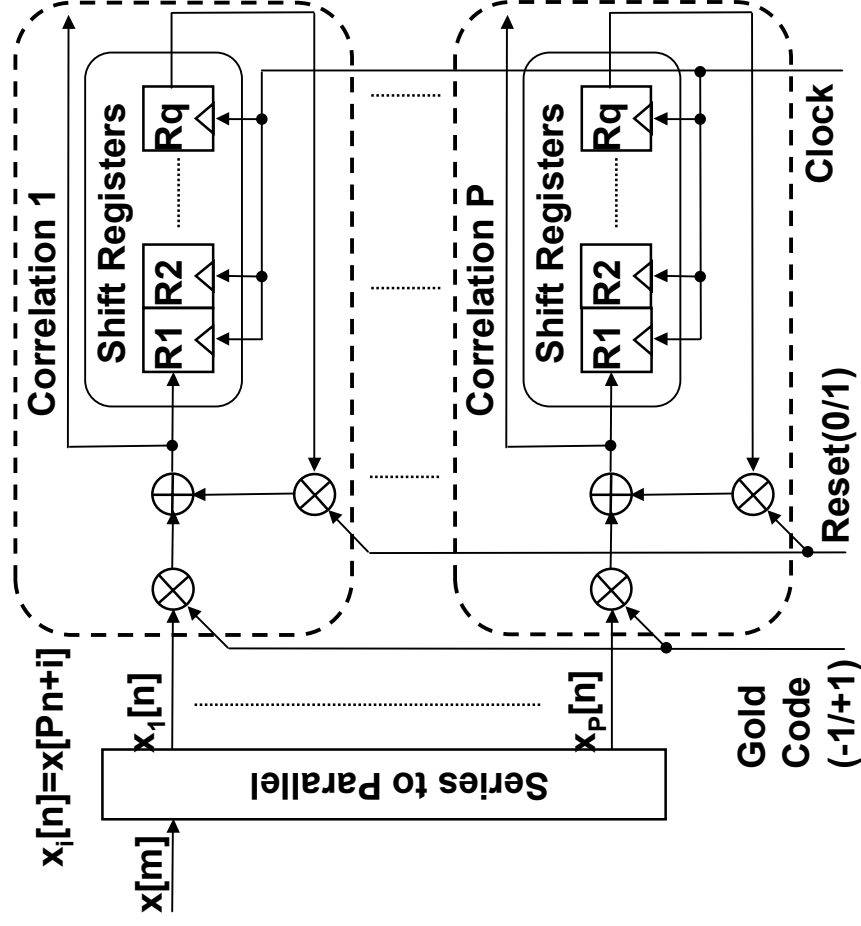
- P Correlators
- Each correlator time-shared with q correlations.

## Advantages

- Faster packet acquisition
- Clock frequency
- Dynamic Voltage Scaling

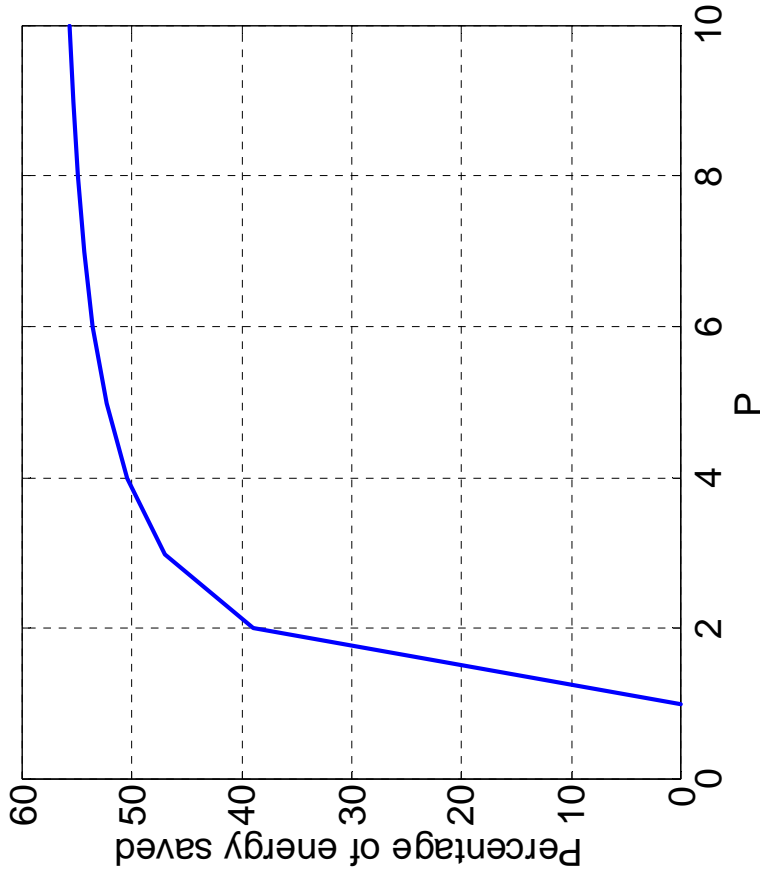
$$\text{Power} \propto (V_{DD})^2$$

**Channel estimation  
for free**

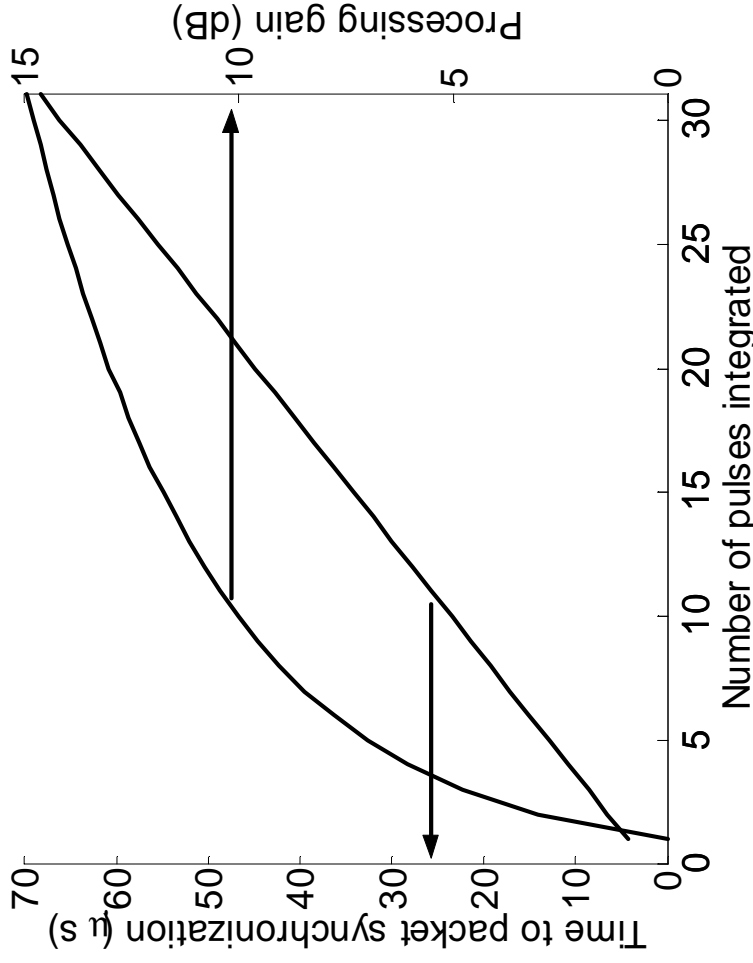


Correlators Architecture

# Coarse acquisition

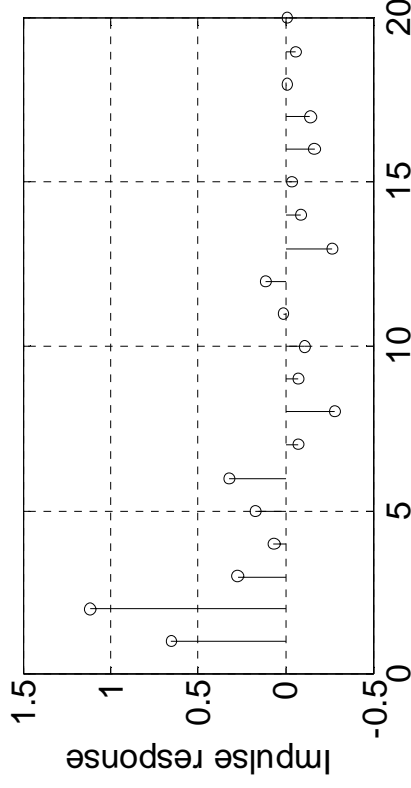


**Parallelization Savings**



**Length of correlation trade-off**

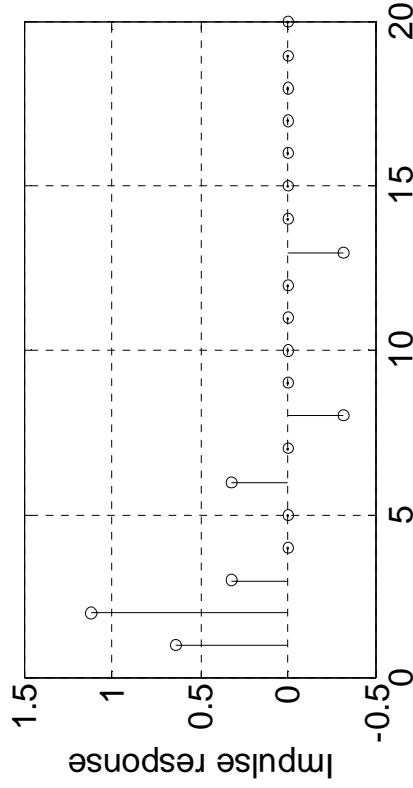
# Rake Receiver



**Channel Impulse Response  
(with multipath effects)**

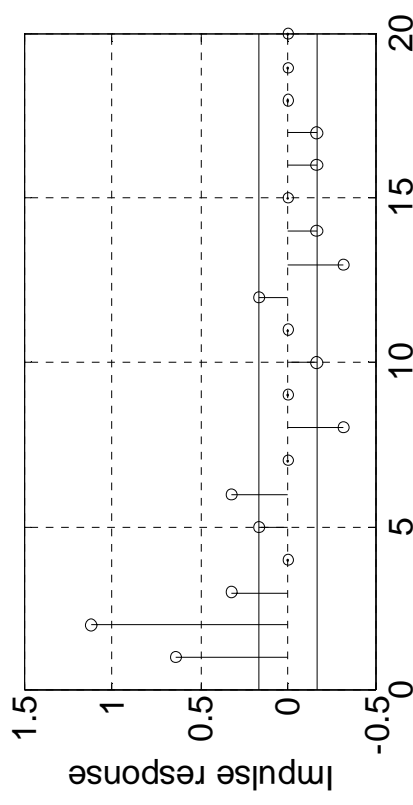
## 6 finger RAKE

Number of fingers fixed

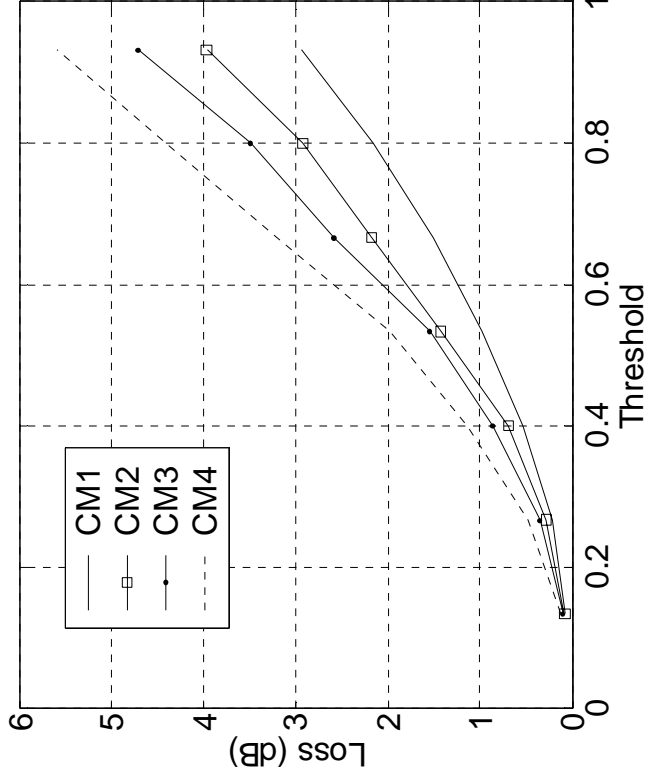


## Method implemented

Variable number of fingers based on relative amplitude of response.

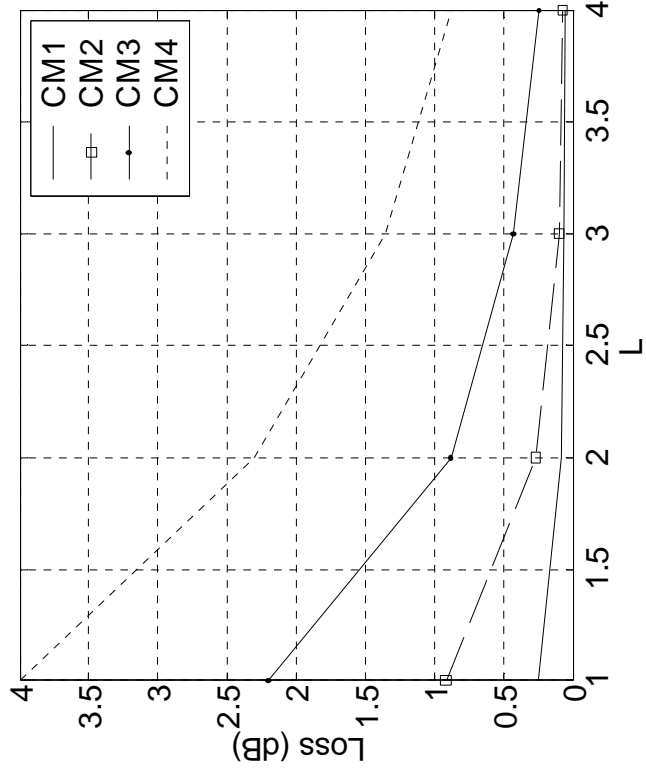


# Programmable Baseband



**MINIMUM POWER OF ECHOES**

$$\text{Energy} \propto 1/\text{Threshold}$$



**NUMBER OF STATES OF MLSE EQ.**

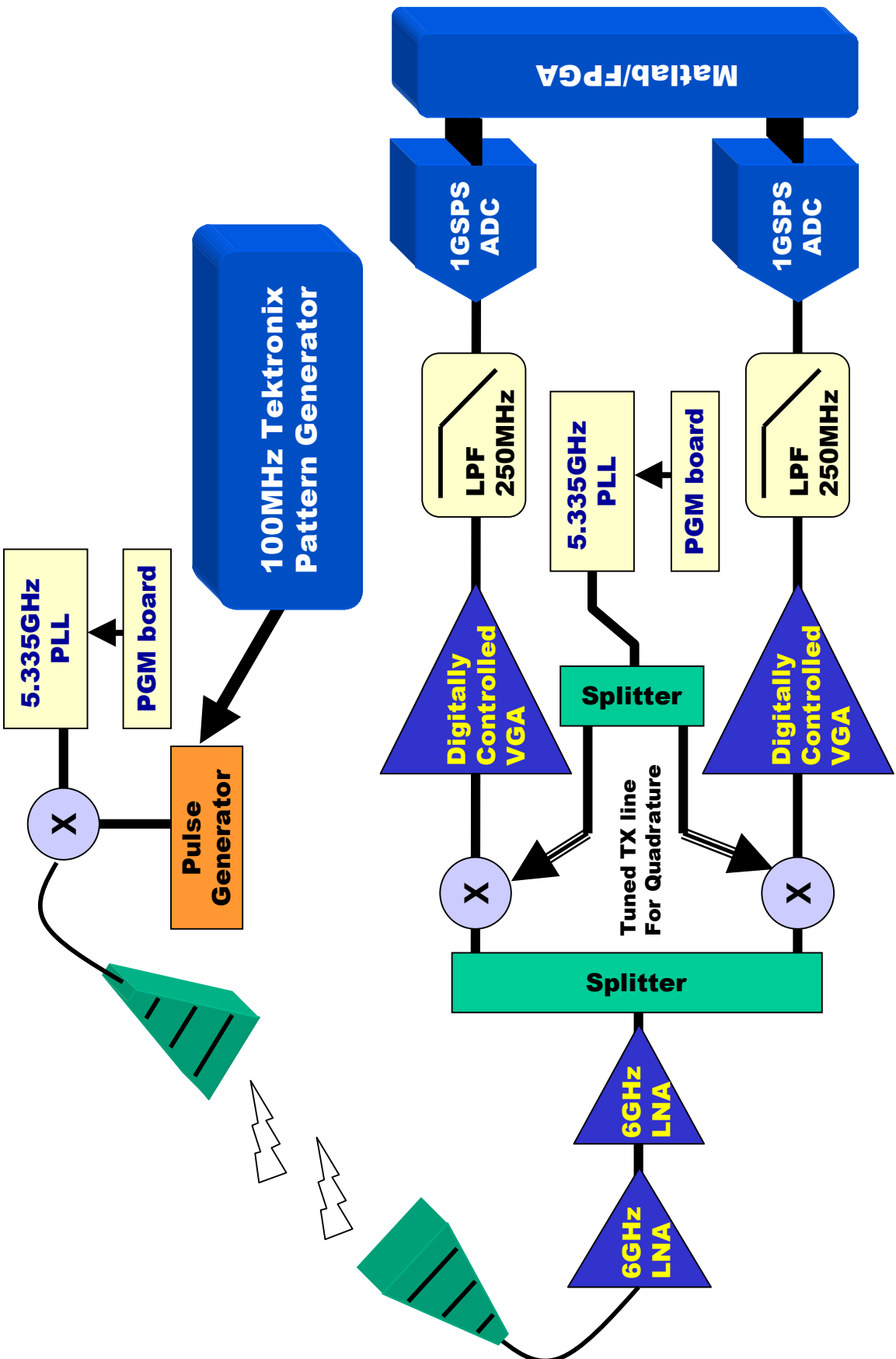
$$\text{Energy} \propto \exp(L)$$

# Adapting to the Channel

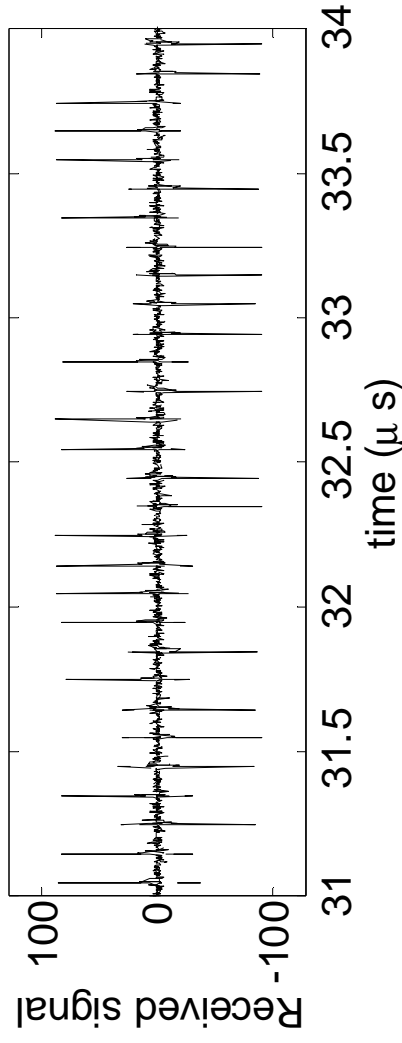
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- Digital baseband estimates channel properties:
  - Multipath (Impulse Response)
  - Signal power
- Controls over signal processing:
  - Number of states of equalizer.
  - Number of bits of ADC.
  - Threshold of the channel.

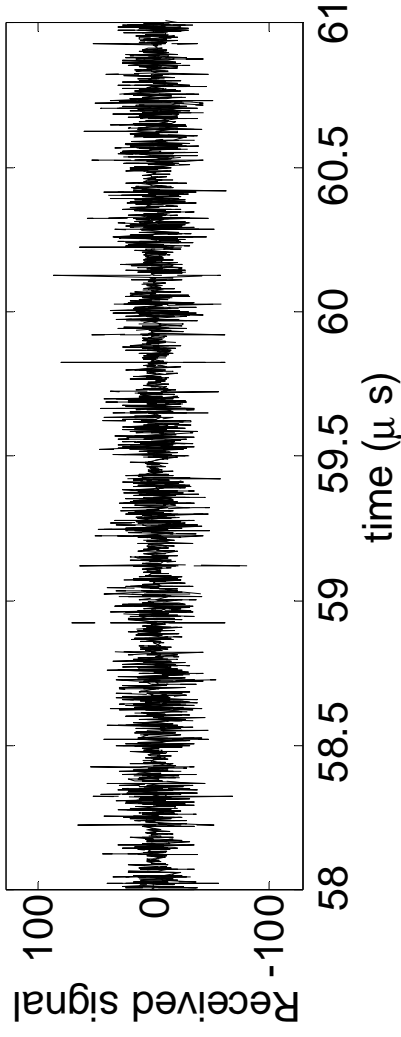
# Flexible Discrete Prototype



# Testing Using the Discrete Prototype



No Interference



SIR = -11 dB

Demonstrated 100Mbps wireless link, packets 10000 bits payload

# Conclusions

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- Higher data rate implies complexity.
- Parallelization reduces acquisition time and allows power reduction.
- Signal processing energy is traded off with quality of service and data rate.
- A discrete platform was designed, achieving 100 Mbps, wireless.