A BASEBAND PROCESSOR FOR PULSED ULTRA-WIDEBAND SIGNALS

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Abstract

This paper presents a baseband processor for pulsed ultra-wideband signals. It consists of an analog to digital converter (ADC), a clock generation system and a digital back-end. The FLASH interleaved ADC provides four bit samples at 1.2GSPS. The back-end uses parallelization to process these samples and to reduce the signal acquisition time to 70μs. The baseband processor was implemented in the same 0.18μm CMOS chip as a part of a complete transceiver. A complete 193kbps wireless link is demonstrated.

Keywords: Ultra-wideband (UWB), wireless transceiver, FLASH ADC, system-on-a-chip and correlation receiver

Introduction

Ultra-wideband (UWB) radio communication, though a widely used technology in the mm-wave radar community, is recently being re-visited by the integrated circuits community as a viable high-speed, last-meter wireless link technology. With the recent FCC ruling on UWB emissions specifications [1] and the current IEEE 802.15.3a standards committee activity for high-speed wireless local area networks, UWB transceivers have become an active area of research.

UWB signals

Contrary to traditional radio signals where data is embedded in the modulation of a narrowband sinusoidal carrier, UWB signals occupy larger bandwidths on the order of hundreds of MHz. There are two competing UWB signaling schemes for the IEEE 802.15.3a standard: pulsed UWB and multiband OFDM signals. Pulsed UWB represents a departure from traditional frequency-based data-encoding methods. Multiband OFDM signals are an extension of the signal used in the IEEE 802.11a standard, with a larger bandwidth. This work focuses on a receiver for pulsed UWB signals, using 0-300MHz baseband pulses. Each bit of information is represented with a sequence of 31 pulses with a width equal to T_p=3.3ns. Since every two consecutive pulses are separated by $50{\cdot}T_p$, the duration of a bit is D_{bit}=$1550{\cdot}T_p$. The information is encoded on the sign of the pulses, that also depends on the corresponding bit of a Gold code sequence of length 31.

The receiver is specified to achieve signal acquisition in an average time of 70μs. This time is on the same order of magnitude as the acquisition time required for lower bandwidth systems, such as IEEE 802.11.

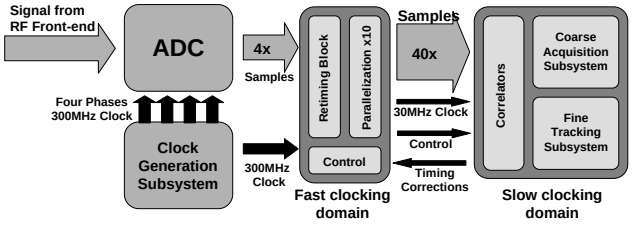

Fig. 1. Baseband processor block diagram.

System Trade-offs

An important consideration in the receiver architecture is determining the analog/digital partition. In this paper, a digital architecture that also implements all the synchronization in the digital domain is chosen. The advantages are the simplification of the analog elements in the transceiver, its scalability, and the possibility of exploring digital channel adaptability and recovery. Performing the synchronization in the digital domain eliminates the need to feed a signal from the digital domain to the clock generation subsystem.

A digital architecture depends on the feasibility of the analog to digital converter (ADC) required to digitize the signal. To allow for an all-digital timing recovery, the ADC must sample at 1.2GSPS, oversampling at twice the Nyquist rate. A FLASH ADC architecture is well suited for such a high sampling rate. Since the power consumption in FLASH ADCs scales exponentially with the number of bits of resolution, minimizing ADC resolution is critical to reduce the power consumed in the receiver. It is found that four bits of resolution are sufficient to be closer than 1dB to the infinite resolution ADC curve for bit error rate [2].

The baseband UWB receiver uses a RF front-end that amplifies the signal but does not down-convert its frequency [3]. After it, the baseband processor shown in Figure 1 demodulates the signal. The following sections describe the blocks of the baseband processor: clock generation subsystem, the ADC, and the digital back-end.

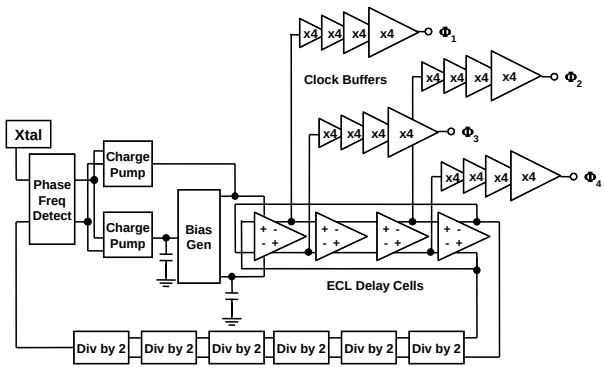

Fig. 2. Clock generation and distribution subsystem.

Clock Generation

Since the system implements a fully digital synchronization algorithm, the only input to the clocking system is the reference crystal clock, and its sole function is to track it. This is done with a phase-locked loop (PLL) based upon a design described in [4]. Figure 2 shows the block diagram of the PLL. The jitter requirements are mostly constrained by the digital back-end of the receiver. Given that the probability of losing synchronization during a 1024-bits data packet with a clock jitter of 100ps is smaller than 0.01, and the degradation in the SNR introduced in the ADC by the same jitter is smaller than 1dB, a ring-oscillator-based VCO can be used to generate the 300MHz clocks required for the ADC. The ring oscillator consists of four inverter buffers connected in a positive feedback loop, producing the four 90 degree phase-shifted clocks that drive the time-interleaved FLASH ADC. The inverter buffers are emitter-coupled-logic (ECL) with symmetric loads. The loop filter capacitor is 400pF, which can be integrated on-chip.

A second charge pump is used to provide a feed-forward zero in the type III loop filter. The bias generator is a replica of the ECL delay cells that is self-biased, and generates the control voltages for the ECL loads and tail current so that they are biased at the maximum gain and swing points for the given current density and frequency of oscillation. The common circuit structures of the charge pump, bias generator, and delay cells lends this PLL to be process-independent and low-jitter.

Analog to Digital Converter

The 4-bit ADC in the UWB receiver is comprised of four FLASH time interleaved channels running on 300MHz phase-offset clocks supplied by the PLL. A sampling rate of f_s=1.2GSPS is achieved. Figure 3 shows the block diagram of a single FLASH channel. Each channel contains a track-and-hold (T/H) circuit, followed by a bank of 15 preamplifiers, comparators and a pipelined decoder. The T/H

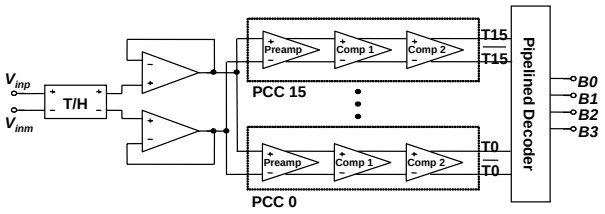

Fig. 3. A Single FLASH ADC channel. Four way interleaving is used.

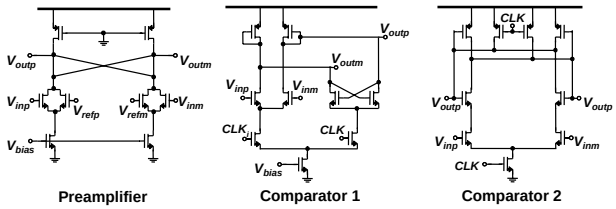

Fig. 4. Preamplifier and comparators.

is comprised of only a switch and sampling capacitor due to the low resolution required by the system. The ADC core is fully-differential for improved noise immunity and supports 500mV peak input swings. These differential blocks are shown in Figure 4. The preamplifier reduces kickback noise to the input and reference nodes and provides a very small amplitude gain (only 6dB). No further gain is needed here as most of the gain will be provided more efficiently by positive feedback in the two comparators. Comparator 1 is a track and latch comparator. Its speed advantage is due to its reduced swing. Comparator 2 is a StrongARM latch [5]. The use of two latching comparators enhances the metastability resolution of the ADC. The pipelined decoder uses an intermediate Gray code to reduce the impact of bubble errors in the performance of the ADC.

The use of a FLASH interleaved ADC has two main advantages. First, overall performance is determined by the average of all four channels rather than being limited by the worst case. This occurs because the digital back-end adds groups of four consecutive samples, coming from the four different channels, and treats the result as a single sample. This reduces the need for calibration across the channels as required in most time-interleaved ADCs.

The second advantage is that data is supplied to the back-end at a reduced data rate. The outputs of the different interleaved channels of the ADC are presented in parallel to the digital back-end. The samples from the four channels are aligned to the same 300MHz clock edge instead of creating a sample data rate clocked at 1.2GHz. The clock frequency of the digital back-end is then reduced to 30MHz.

Digital Back-end

The digital back-end recovers the information contained in the data packets from the samples given by the ADC using an approximation to the matched filter [6]. A matched filter is the optimum demodulator of a signal in AWGN, and implies the correlation of the received signal with a local template synchronized to it and comprising a sequence of perfect replicas of the received pulses. This receiver uses a sequence of rectangular pulses instead of the perfect replicas. The correlation of the incoming signal with a rectangular pulse of width T_p is equivalent to adding together four consecutive samples taken at 1.2GSPS. This simplification of the architecture comes at a cost of 1.7dB of SNR.

The synchronization of the local templates with the incoming signal is achieved in two stages: coarse acquisition and fine tracking. To reduce the coarse acquisition time below 70μs, it is necessary to calculate at least 50 correlations in parallel during this stage [7]. For fine tracking, only two correlations using contiguous templates are needed in order to implement the delay estimator needed for a delay locked loop (DLL) and to demodulate the data bits. Since timing recovery is performed in the digital domain, the delay corrections are obtained by advancing or delaying an integer number of samples.

A. Architecture

The digital back-end is divided into a fast and a slow clocking domain, as shown in Figure 1. The fast domain uses a custom layout, a 300MHz clock coming from the PLL, and is composed of a retiming block, a block that performs a 10x parallelization of the incoming ADC samples, and the main control of the digital back-end. The parallelization allows the slow domain to work with a 30MHz clock. The correlations and other mathematical operations needed to implement the synchronization and demodulation are performed using 2's-complement arithmetic in the slow domain, and their design is carried out using synthesis tools.

The retiming block provides the one-sample delay granularity required for fine tracking. The groups of four samples that are the inputs to the correlators may start with any arbitrary sample and may include samples belonging to two different ADC vectors. These groups are obtained by selectively delaying the outputs of one or more ADC interleaved channels in the retiming block.

After the parallelization, the outputs of the fast clocking domain are processed by 10 correlators as shown in Figure 5. In each 30MHz clock cycle, the four samples at its input are added together, implementing the correlation with a rectangular pulse of width T_p. The result of this addition is either added or subtracted, depending on the value of the Gold Code, to the 11-bit value stored in the shift registers five cycles before (50·T_p, equal to the time between two consecutive pulses). All multipliers in Figure 5 are implemented using 2-to-1 multiplexers because in each of them one of the

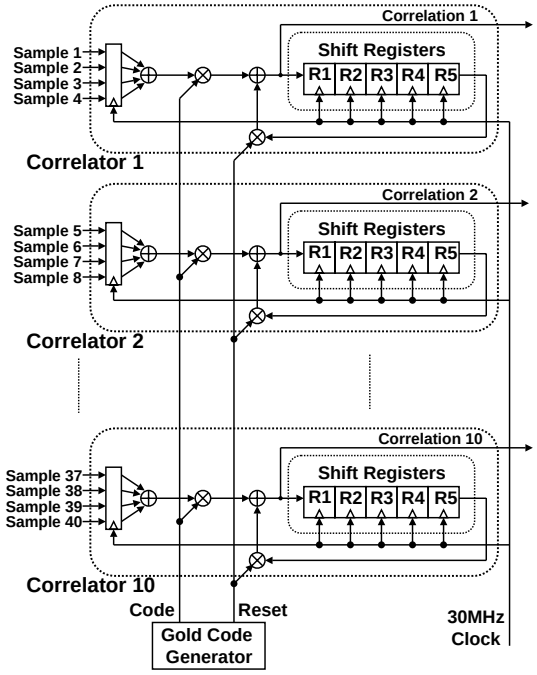

Fig. 5. Implementation of one of the correlator channels.

coefficients is one single bit. Each correlator performs five correlations at the same time, equivalent to the output of an FIR of $D_{bit} \cdot f_s$=6200 coefficients with values equal to 1, -1 or 0. The outputs from the ten correlators are used by the coarse acquisition subsystem, but only the first two are active during fine tracking. The Gold code generator is implemented with two shift registers, each of them generating a linear recursive sequence of which both the coefficients of the generating polynomial and the seed values are programmable.

The fine tracking subsystem shown in Figure 6 provides the functionality required to close the DLL. The division needed in the delay estimation is avoided by multiplying by an approximation to the inverse stored in a ROM. The ROM stores 32 seven-bit numbers and the five more significant bits of the numerator are used to choose the output. The coefficients of the filter are programmable, and it uses Baugh-Wooley multipliers. The delay decoder transforms the output of the filter into signals relevant to the fast clocking domain: the new state of the retiming block and indication of the need to start correlations a 300MHz clock cycle before (signal Advance) or later (signal Delay). The fine tracking subsystem also provides a flag to restart coarse acquisition when the signal is lost. All the outputs of the fine tracking system are ready in six 30MHz cycles.

As the 50 correlations are completed, they are read into the coarse acquisition subsystem, whose block diagram is shown in Figure 7. The memory block provides not only the value of the maximum but also the values in the two adjacent

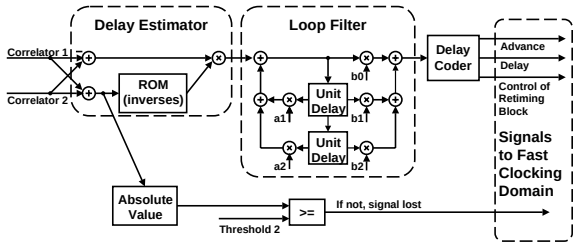

Fig. 6. Fine tracking subsystem block diagram.

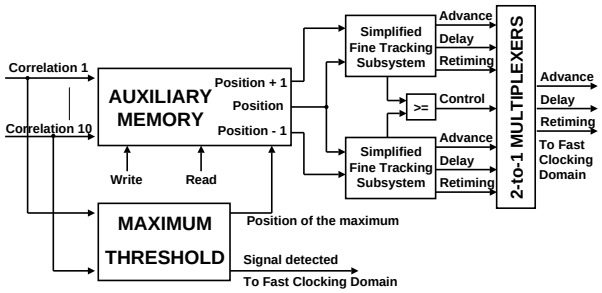

Fig. 7. Coarse acquisition block diagram.

positions. The two simplified fine tracking subsystems lack the loop filter shown in Figure 6 except for its direct path (b_0). Only the simplified fine tracking subsystem using the two positions with the most energy will be used to initialize the DLL. Detection of the signal is given in six 30MHz cycles, and the rest of the outputs are ready in seven cycles more.

All thresholds, coefficients and other parameters used in the digital back-end must be configured before its use using a serial port.

Performance results

Figure 8 shows a photograph of the 0.18μm ASIC. The PLL was verified at 300MHz and can provide much higher clock frequencies (up to 2GHz). The ADC is verified using the testing method presented in [8]. Its effective number of bits is greater than 3. The digital back-end is completely functional at a clock frequency of 300MHz. The frequency range for the coarse acquisition algorithm between a pair of transceivers is shown to be $\pm 3\%$. At 300MHz a wireless link was demonstrated at a data rate of 193kbps. Table I contains a summary of overall chip measurements.

Conclusions

The baseband processor for a UWB system-on-a-chip transceiver with a mainly digital architecture was presented in this paper. The chip was implemented in 0.18μm CMOS. The total power consumed by the baseband processor was 275mW. A wireless link with a data rate of 193kbps was demonstrated with this system.

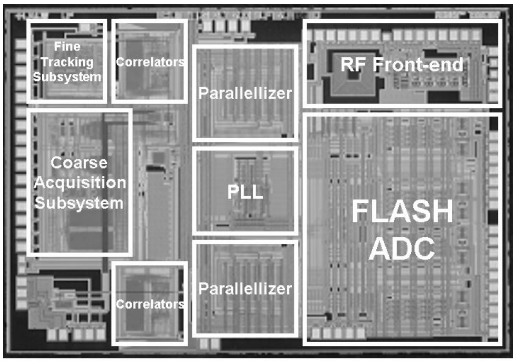

Fig. 8. Single chip UWB transceiver photograph.

TABLE I
CHIP MEASUREMENTS

Chip specifications		
Process Technology	0.18μm non-epi	
Die Size	4.3mm $\times$ 2.9mm	
Bit Rate	193kbps	
ADC Performance	Abs. Accuracy	Rel. Accuracy
Static Performance	3.1bits	3.9bits
Dynamic Performance	3.0bits	3.4bits
Power Consumption		
ADC + PLL	135mW	
CLK Buffers	65mW	
Back-End	75mW	
Total	275mW	

Acknowledgments

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