3.4 A 175mV Multiply-Accumulate Unit Using an Adaptive Supply Voltage and Body Bias (ASB) Architecture

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The power dissipation of a digital circuit is minimized by simultaneous control of power supply voltage and body bias. The technique minimizes power dissipation for varying processing rates through dynamic adjustment of V_{dd} and V_{bb}. A 16b MAC operates at 166kHz and 14nW at 175mV V_{dd}. A ring oscillator operates at 0.1V.

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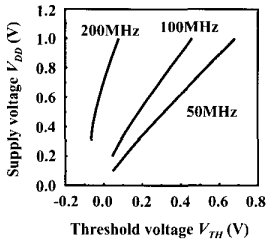
Outline

- ❑ Previous Work on Voltage Scaling
- ❑ Adaptive Supply and Body Bias architecture
- ❑ Test chip design
- ❑ Measured results
- ❑ Future Direction

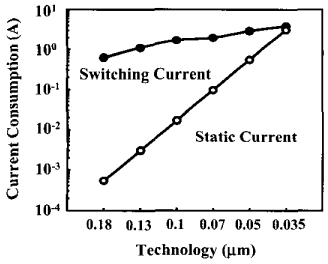
Impact of Simultaneous V_{DD} and V_{TH} Scaling

$$f_{CLK} = \frac{\beta}{C_L} \cdot \frac{(V_{DD} - V_{TH})^{\alpha}}{V_{DD}}$$



- ❑ V_{DD} and V_{TH} can be varied to keep a fixed performance
- ❑ What is the optimal Supply and Threshold?

Microprocessor Trends



- ❑ Active leakage an important concern with voltage scaling

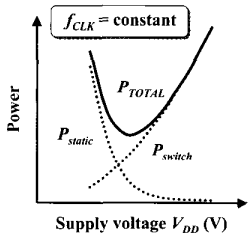
Concept of ASB Control

- ❑ Reduce V_{DD} and V_{TH} to reduce dynamic power for fixed performance

$$P_{switch} = a \cdot f_{CLK} \cdot C_L \cdot V_{DD}^2$$

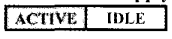
- ❑ Subthreshold leakage increases

$$P_{static} = I_{10} \cdot V_{DD} \cdot 10^{\frac{V_{TH}}{S}}$$



Previous Work: Dynamic Voltage Scaling

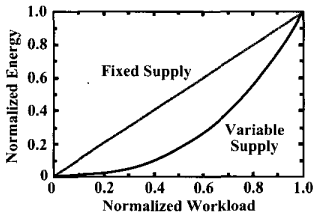
Fixed Power Supply



$$E_{FIXED} = \frac{1}{2} C V_{DD}^2$$

Variable Power Supply

$$E_{VARIABLE} = \frac{1}{2} C \left(\frac{V_{DD}}{2}\right)^2 = \frac{E_{FIXED}}{4}$$



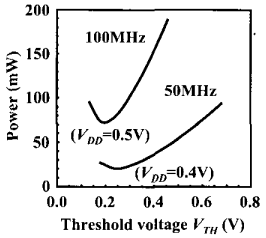
Gutnik and Chandrakasan [VLSI Circuits Symposium '96]

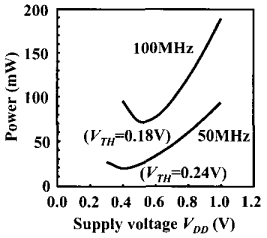
Wei, Kim, Liu, Sidiropoulos, Horowitz [ISSCC '00]

Burd, Pering, Stratakos, Brodersen [ISSCC '00]

- ❑ Adapt Power Supply Voltage to Computational Workload

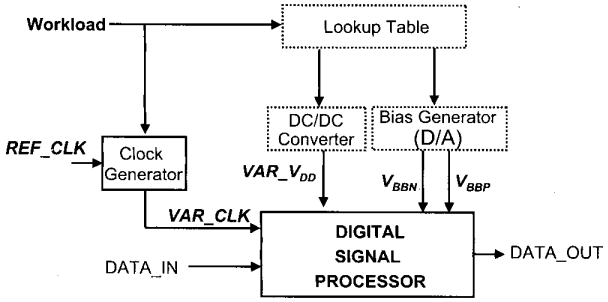
Theoretical Results





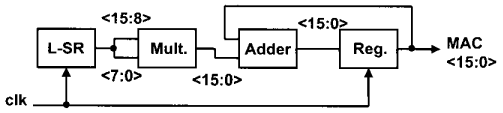
- ❑ Minimum energy point is a strong function of operating frequency
- ❑ ASB Concept: Adapt BOTH supply and threshold as operating frequency (i.e., workload varies)

ASB Architecture – Approach I

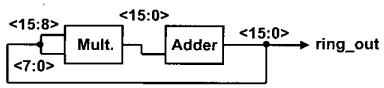


Test Chip: Simple MAC Circuit

Multiply Accumulator

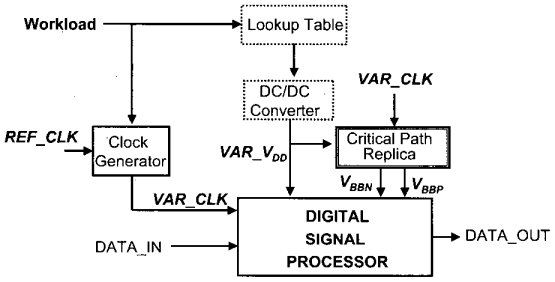


Critical path ring oscillator



❑ ***Standard Static CMOS logic/registers to allow deep voltage scaling***

ASB Architecture – Approach II



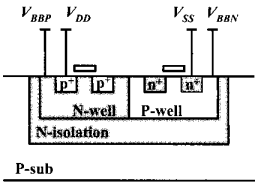
❑ ***Body bias adapted to maintain performance at a given power supply voltage***

Process Features

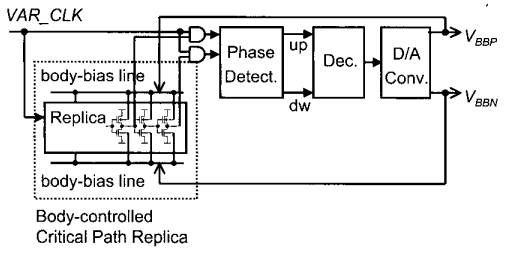
Device Characteristics

L_G:	0.14 µm
T_{OX}:	3.2 nm
Metal:	5 layers
Well:	Triple Well
V_{TH}:	0.05 V
	(V_{GS}@I_{DS}=1nA/µm)

Triple-Well Structure



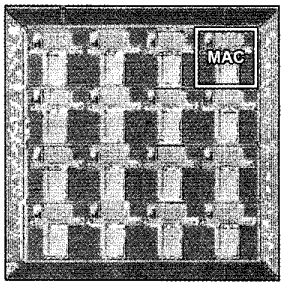
Body Biasing Using Critical Path Replica



❑ ***Body bias adapted in both directions (reverse and forward body bias) to improve dynamic range***

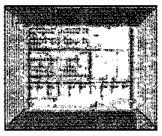
Chip Micrograph

16-bit Multiply Accumulator X 16 blocks



850 X 880 µm

Body bias Generator (ABB)



300 X 400 µm

Impact of Forward Body Bias

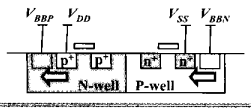
❑**ASB uses body bias control**

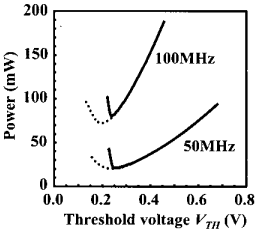
❑ **Forward bias current is proportional to *exp(V_{BB})***

$$P_{VBB} = I_{B0} \cdot V_{BB} \cdot \left[\exp\left(\frac{q}{nkT} |V_{BB}| \right) - 1 \right]$$

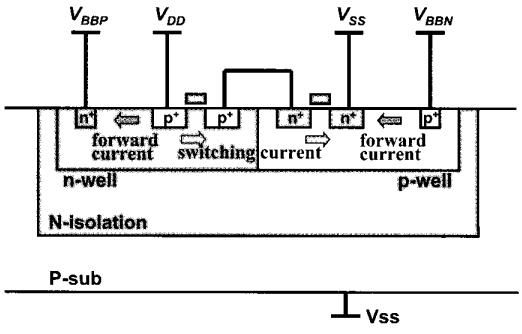
$$V_{TH} = V_{TH0} + \gamma \cdot \left(\sqrt{2\Phi_B - V_{BB}} - \sqrt{2\Phi_B} \right)$$

Forward bias : $V_{BB} > 0$





Forward Bias Current



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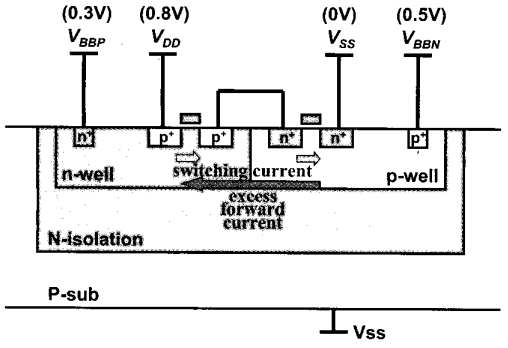
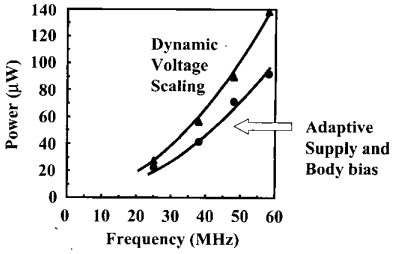
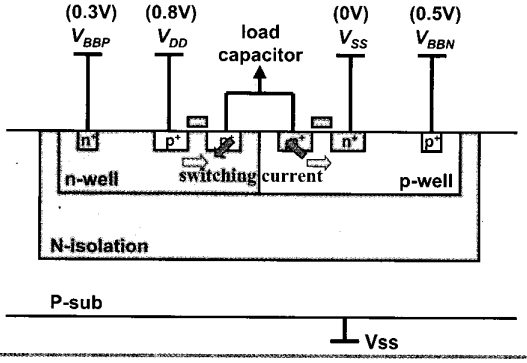
Excess Forward Bias at Low V_{DD}



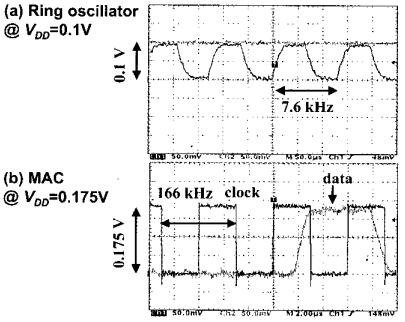
Power Reduction of ASB



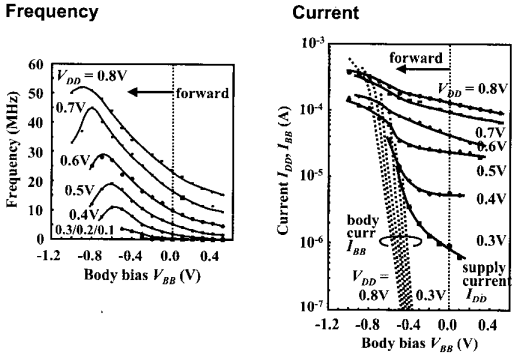
Excess Forward Bias at Low V_{DD}



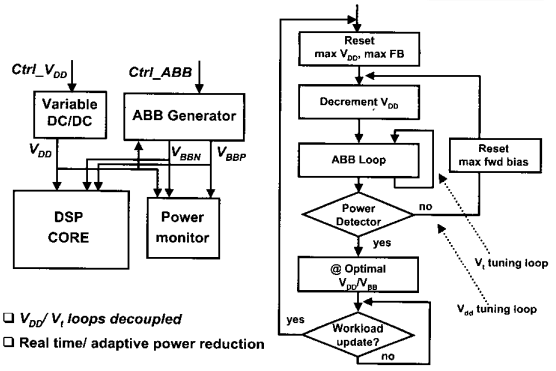
Measured Waveforms at Min. V_{DD}



MAC Performance

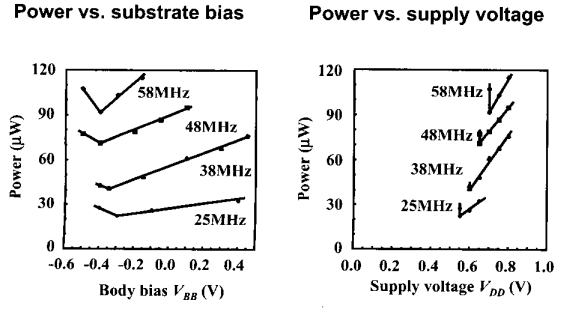


Future Direction: Auto ASB Algorithm



- V_{DD}/ V_t loops decoupled
- Real time/ adaptive power reduction

ASB Power Results



Conclusions

- ASB architecture is proposed for minimum power operation
- Forward bias increases V_{TH} dynamic range but excess biasing degrade circuit performance
- Minimum operating V_{DD} of 100mV is demonstrated for a ring oscillator and 175mV for a MAC