A 6.5GHz CMOS FSK Modulator for Wireless Sensor Applications

SeongHwan Cho Anantha P. Chandrakasan

Department of Electrical Engineering and Computer Science

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

Cambridge, MA

{chosta,anantha}@mtl.mit.edu

Abstract—

A 6.5GHz FSK modulator suitable for low power wireless sensor network is presented. The modulator employs closed loop direct VCO modulation to achieve high data rate, variable loop bandwidth technique for fast start-up rates and Σ-Δ for reduced power consumption in the divider with fine resolution in channel selection. The synthesizer, implemented in 0.25μm CMOS, achieves 20μs start-up time with an effective data rate of 2.5Mbps while consuming 22mW.

Introduction

Emerging distributed wireless microsensor networks will enable the reliable and fault tolerant monitoring of the environment. Such microsensors are required to operate for years from a small energy source, while maintaining reliable communication link to the basestation. The constraints of the sensor network are quite different from those of conventional wireless hand-held devices. Since sensors require communication of short packets in small area, start-up time plays a critical role in energy efficiency of transmission [1]. In this paper, an energy efficient transmitter for wireless sensor application is presented, that achieves fast start-up time, low power consumption and high burst data rate.

A simplified block diagram of the proposed modulator is shown in Figure 1. The frequency synthesizer is a fourth order PLL with a third order Σ-Δ for fractional channel selection of the reference frequency. High data rate FSK modulation is achieved by directly modulating the low gain control input of the VCO in closed loop. Since the PLL acts as a high pass filter when seen by the modulation input, the loop bandwidth of the PLL is kept low during data modulation. Fast start-up time is achieved by employing variable loop bandwidth technique that changes the loop parameters from a large bandwidth to a small bandwidth as the PLL approaches lock. Power consumption of the PLL is dramatically reduced by exploiting the trade-off between the complexity of the divider and the Σ-Δ. The power consumption in divider is reduced by inserting a divide-by-8 prescaler before a dual modulus divider, while the increased quantization noise is reduced by the Σ-Δ with little extra overhead.

High data rate technique: Closed loop direct VCO modulation

Several papers have been published on low power high data rate transmitter architectures for continuous phase modulated signals. The indirect modulation method that uses Σ-Δ in fractional-N synthesizer [2] is well suited for such modulation scheme and has spawned other interesting architectures where the data is pre-emphasized [3] and the loop gain mismatches are automatically calibrated [4]. However, as the data rate and carrier frequency gets higher, these architectures will consume more power mainly due to the Σ-Δ , high frequency dividers and quantizers. Another architecture that allows compact form of continuous phase modulation is the open loop direct VCO modulation architecture [5]. Although this method allows data rate that is not limited by the loop bandwidth of the PLL, it suffers from the fact that it will only work for short bursts. Closed loop direct VCO modulation [6] on the other hand is robust to these problems and still has the advantage that the upper bound on data rate is not affected by the PLL loop bandwidth as seen in the indirect modulation architecture. The disadvantage however, is that the output modulated waveform can be distorted by the negative feedback loop of the synthesizer. The distorted low frequency components of the modulated data can be compensated through the closed loop Σ-Δ modulation, but this requires extra over-

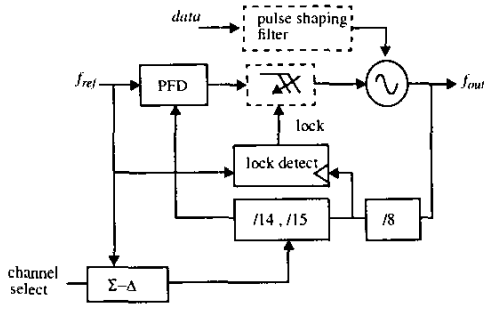

Fig. 1. Proposed BFSK Modulator Architecture

 0-7803-7310-3/02/$17.00 ©2002 IEEE

head in calibration [7]. The output modulated waveform under locked condition can be described by the following equation,

$$\phi_{mod-out} = (H(\omega_n) + \frac{K_{mod}}{s})v_{mod} \quad (1)$$

where $\phi_{mod-out}$ is the modulated output phase when the synthesizer is in lock, $H(\omega_n)$ is the loop transfer function of the PLL from the modulation input to the output, K_{mod} is the VCO gain of the modulation input and v_{mod} is the input voltage of the pulse-shaped data. For a simple second order charge pump PLL, the error, ϕ_e from the ideal modulated phase is simply,

$$\begin{aligned} \phi_e &= H(\omega_n)v_{mod} \quad (2) \\ &= -K_{mod}\frac{{\omega_n}^2(1+s\tau_z)}{s^2+2\zeta\omega_n s+{\omega_n}^2}v_{mod} \end{aligned}$$

It can be seen that the error signal is indeed a low pass function of the loop bandwidth ω_n, and hence the loop bandwidth must be kept well below the data rate.

Low power PLL technique

A. Divider vs. Σ-Δ

In the GHz regime, the power consumption of the frequency synthesizer is often dominated by the multi-modulus dividers [3], [8]. Since multi-modulus dividers consume significantly more power than fixed value prescalers, it is desirable to use fixed prescalers at high frequency stages and move the multi-modulus dividers to a later stage where operating frequency is lowered. The penalty however, is that the quantization noise from Σ-Δ will increase by 6dB each time a divide-by-two prescaler is inserted. Moreover, the frequency resolution is decreased by a factor of two. In order to cancel out the increased quantization noise and keep the same frequency resolution, complexity of the Σ-Δ must be increased that results in larger power consumption. Hence it can be seen that there is a trade-off between divider versus Σ-Δ power consumption. A circuit level simulation which shows this trade-off has been performed and the results are shown in Figure 2. In order to keep the same output noise and frequency resolution with more number of prescalers, complexity of the Σ-Δ is increased. It can be seen that the total power consumption reaches minimum when a fixed prescaler of divide-by-8 is used before a dual modulus divider. The prescaler by 8 is based on high speed divide-by-2 flip-flops as shown in Figure 3 [9], [10]. In order to operate these dividers at a low supply voltage of 1.6V with small input amplitude, the clocked transistors are biased separately from the input signals with DC blocking capacitors. Test results from the fabricated chip show power consumption of 3.2mW for the divide-by-112/120 and 0.9mW for the Σ-Δ , both at 1.6V. The achievable frequency resolution is about 1MHz.

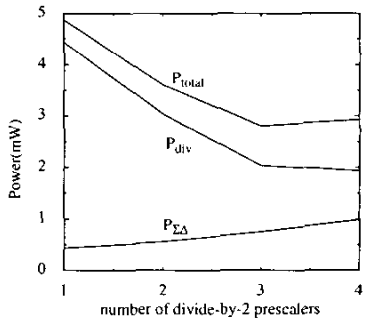

Fig. 2. Power consumption of divider and Σ-Δ

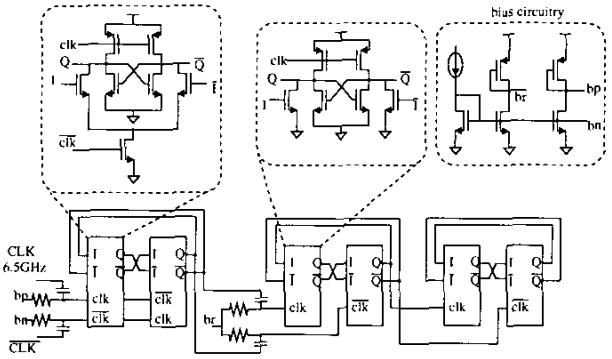

Fig. 3. Divide by 8 Prescaler

B. VCO

The VCO is a cross coupled inverter with an integrated L-C tank as shown in Figure 4. While many combinations of L-C tank exist at 6.5GHz, it is advantageous to use a small inductor and a large capacitor, since it is easier to implement smaller value high Q inductors at high frequencies. The required capacitor to achieve the desired resonant frequency is set by the two CMOS varactors and parasitic capacitances from the $-g_m$ and buffer transistors. While tuning range can be maximized by minimizing the parasitic capacitance of the -g_m and buffer transistors, $1/f$ noise can be lowered if longer length transistors are used. This increases the parasitic capacitance and hence reduces the tuning range. The implemented VCO uses NMOS devices that is two times larger than the minimum size device for lower $1/f$ noise. The VCO achieves -112dBc/Hz phase noise at 1MHz offset, while drawing 7.7mA from 2.3V. The tuning range of the VCO is measured to be about 800MHz for the high gain varactor (6.1GHz ~ 6.9GHz) and about 8MHz for the low gain varactor. The $1/f$ noise is measured to be approximately 120kHz. The high power consumption of the VCO is due to the low Q L-C tank, which has a Q of about 7.

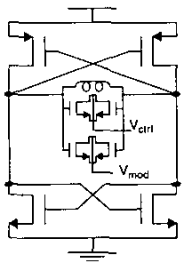

Fig. 4. Schematic of 6.5GHz VCO

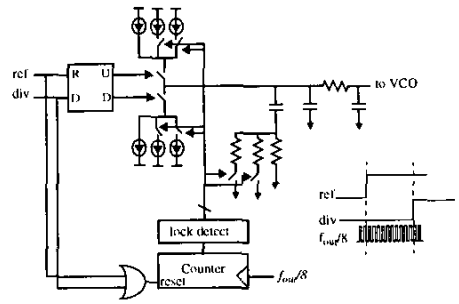

Fig. 5. Variable loop bandwidth frequency synthesizer

Fast startup technique: Variable loop bandwidth

In order to achieve fast startup transient with low loop bandwidth, a loop switching method is used [11], [12]. To allow minimal disturbance on the VCO control voltage during switching, resistive component of the loop is changed by turning off the current source and opening the resistor paths as shown in Figure 5. In addition, the loop parameters are set such that the phase margins are kept the same during loop switching. The loop bandwidth is changed to an intermediate value before being switched to its final low value to allow short small signal settling time by avoiding large difference in loop bandwidth switching. The fractional-N division in large loop bandwidth mode causes significant fluctuation of the VCO control voltage around its average value and hence, switching to a loop bandwidth with large difference causes long settling time that is dominated by the small loop bandwidth. The lock is monitored by a digital counter which counts the number of prescaled output pulses that reside between the reference and the divided clock. A lock is detected if this number is kept below a certain threshold for a period of time that corresponds to the loop bandwidth. The loop bandwidth switches from approximately 1MHz to 250kHz, then to 100kHz. The lock monitoring unit consumes 150μW and the loop filters are implemented off-chip.

Experimental results

The 6.5GHz FSK modulator, implemented only in CMOS, is fabricated in 0.25μm SiGe BiCMOS process, consuming 1.3mm x 1.1mm of die area. It is packaged in a 32-pin micro-lead frame package and has been tested on a FR-4 PCB board. The eye diagram and the spectrum of the 5Mbps Manchester encoded data are shown in Figure 8 and Figure 9, respectively. The eye was measured at one eighth the carrier frequency and the peaks that are seen in the spectrum are due to Manchester encoding. The start-up times are shown in Figure 10 and 11. It can be seen that the start-up time is reduced by a factor of 4 compared to the fixed loop bandwidth scheme shown in Figure 10. The total power consumption of the chip is 22.2mW, where the VCO consumes 17.7mW from 2.3V and the rest of the PLL consumes 4.5mW from 1.6V. To compare energy efficiencies of different radios in sensor applications, we define *Energy per bit* as the energy it takes to transmit a bit when sending a packet, which includes the startup energy of the transmitter. The comparison is shown in Figure 7, where energy efficiencies of low power high data rate radios are plotted versus packet size. It can be seen that reducing the start-up time is crucial in energy efficiency for short packet transmission.

Conclusion

An energy efficient FSK modulator for wireless sensor application was implemented. It employs variable loop technique for fast start-up time, direct VCO modulation for high data rate, and exploits trade-off between the divider and the Σ-Δ complexity for low power consumption.

Acknowledgment

The authors would like to thank H. Ainspan at IBM T.J. Watson Research Center for help in layout, IBM Burlington for chip fabrication, and Snorre Kjesbu of ABB Research for valuable technical contributions. This project is funded by ABB Corporate Research in Norway.

References

[1] A. Y. Wang, S-H. Cho, A. Chandrakasan, and C. Sodini, "Energy efficient modulation and MAC for asymmetric RF microsensor systems," in *IEEE International Symposium on Low Power Electronics and Design*, 2001, pp. 106–111.

[2] S. Willingham, M. Perrott, B. Setterberg, A. Grzegorek, and B.McFarland, "An integrated 2.4GHz frequency synthesizer with 5 μs settling and 2Mbps closed loop modulation," in *ISSCC Digest of Technical Papers*, 2000, pp. 200–201.

[3] M. Perrott, T. Tewksbury, and C. Sodini, "27 mw CMOS fractional-N synthesizer/modulator IC," in *ISSCC Digest of Technical Papers*, February 1997, pp. 366–367.

[4] D. McMahill and C. Sodini, "Automatic calibration of modulated $\Sigma - \Delta$ frequency synthesizers," in *IEEE Symposium on VLSI Circuits Digest of Technical Papers*, 2000, pp. 51–54.

[5] S. Heinen et al., "A 2.7V 2.5GHz bipolar chipset for digital communication," in *ISSCC Digest of Technical Papers*, February 1997, pp. 306–307.

[6] T. Cho et al., "A single-chip CMOS direct-conversion transceiver for 900 MHz spread-spectrum digital cordless phones ," in *ISSCC Digest of Technical Papers*, 1999, pp. 228–229.

[7] N. Filiol et al., "A 22mW Bluetooth RF transceiver with direct RF modulation and on-chip IF filtering," in *ISSCC Digest of Technical Papers*, 2001, pp. 202–203.

[8] H. Rategh, H. Samavati, and T.H.Lee, "A CMOS frequency synthesizer with an injection-locked frequency divider for a 5GHz wireless LAN receiver," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 780–787, May 2000.
[9] H. Wang, "A 1.8V 3mW 16.8GHz frequency divider in 0.25μm CMOS," in *ISSCC Digest of Technical Papers*, February 2000, pp. 196–197.
[10] B. Razavi et al., "A 13.4GHz CMOS frequency divider," in *ISSCC Digest of Technical Papers*, February 1994, pp. 176–177.
[11] F.M. Gardner, *Phase lock techniques*, Wiley, New York, 1979.
[12] C-Y Yang and S-I Liu, "Fast-switching frequency synthesizer with a discriminator-aided phase detector," *IEEE Journal of solid-state circuits*, vol. 35, no. 10, pp. 1445–1452, Oct 2000.
[13] National Semiconductor Corp., *LMX3162 Single Chip Radio Transceiver.*

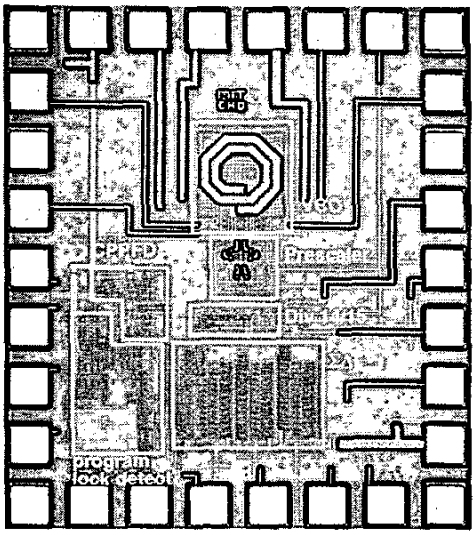

Fig. 6. Die photo of the chip

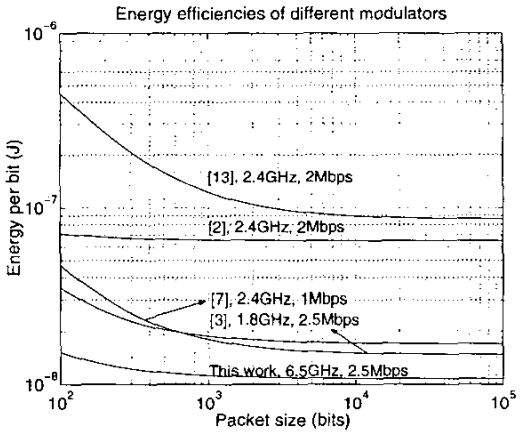

Fig. 7. Energy efficiency comparison

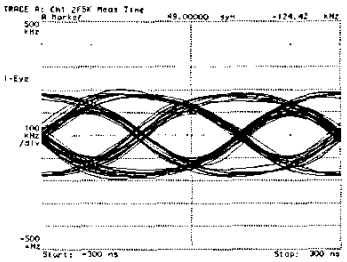

Fig. 8. Eye diagram of the 5Mbps Manchester encoded data

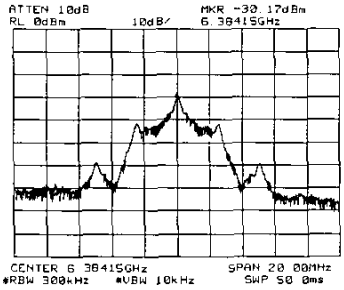

Fig. 9. Spectrum of the 5Mbps Manchester coded data

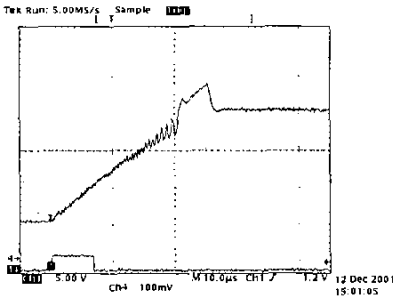

Fig. 10. Startup transient of frequency synthesizer with fixed loop

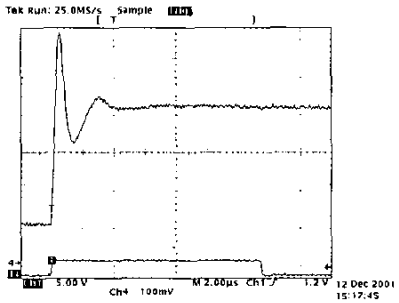

Fig. 11. Startup transient of variable loop frequency synthesizer