Optimal Supply and Threshold Scaling for Subthreshold CMOS Circuits

Alice Wang and Anantha P. Chandrakasan
Department of EECS, Massachusetts Institute of Technology, Cambridge MA 02139
<aliwang, anantha>@mit.edu

Stephen V. Kosonocky
IBM T.J. Watson Research Center, Yorktown Heights NY 10598
stevekos@us.ibm.com

Abstract

With technology scaling, power supply and threshold voltage continue to decrease to satisfy high performance and low power requirements. In the past, subthreshold CMOS circuits have been inadequate for high performance applications, but have been used in applications that require ultra low power dissipation. Many applications including medical and wireless applications, require ultra low power dissipation with low-to-moderate performance (10kHz-100MHz). In this work, using BSIM3 models, the performance and energy dissipation of 0.18-µm CMOS circuits for the range of V_{dd}=0.1-0.6V and V_{th}=0-0.6V, are analyzed to show that subthreshold CMOS circuits can be used in low performance applications. A simple characterization circuit is introduced which can be used to evaluate the performance and energy dissipation for a given process under varying activity. These results are useful in circuit design by giving insight into optimal voltage supply and threshold voltage operation for a given application specification. Characterization results show that operation at the optimal V_{dd}-V_{th} voltage levels can lead to an order of magnitude energy savings. Also additional analysis into V_{th} and temperature variations is included.

I. Introduction

In energy-constrained systems, low power design is essential for extending battery and system lifetime. Lowering voltage supply (V_{dd}) decreases energy dissipated quadratically, but also causes an increase in delay. In order to satisfy the aggressive performance requirements demanded by applications, the threshold voltage (V_{th}) should also be lowered, to have both low power operation and high performance. However, there is a cost of higher static power dissipation due to large leakage currents [1]. Other techniques used in low power design includes clock gating and dynamic voltage/frequency scaling [2][3].

Subthreshold circuit design involves scaling the supply voltage below the threshold voltage, where load capacitances are charged/discharged by subthreshold leakage currents. Leakage currents are orders of magnitude lower than drain currents in the strong inversion regime, so there is a significant limit on the maximum performance of subthreshold circuits. Therefore, traditionally, subthreshold circuits have been used for applications which require ultra-low power dissipation, with low-to-moderate circuit performance. In digital CMOS circuits, subthreshold circuits have been popular in low performance applications such as wrist watches [4] and hearing aids [5]. Both applications have very low clocking frequencies (kHz range).

This work characterizes the performance and energy dissipation for submicron circuits in the region of V_{dd}=0.1-0.6V and V_{th}=0-0.6V. A simple characterization circuit is introduced and simulations using the BSIM3 models for a 0.18-µm process show that performance in this region is adequate for most applications with low-to-moderate performance (10kHz-100MHz). This circuit also enables analysis into the energy dissipation for differing activity factors.

Voltage supply and threshold voltage scaling in the strong inversion region has been extensively studied, and this work extends the analysis into the at-threshold and subthreshold region. Different metrics have been used to study supply and threshold voltage scaling such as, energy, delay, power, energy-delay product (EDP) [6], power-delay product (PDP) [1]. In this work, contours of energy and delay for the entire design space is shown. These results give intuition about trade-offs between energy and performance, and the optimal V_{dd}-V_{th} operating region for CMOS circuits is shown.

An analysis which is important for subthreshold circuits is the sensitivity of energy and performance on threshold voltage and temperature variations. At such low voltage levels, a small voltage change can lead to large changes in current. In this work, we will show how one can design for a given constraint of variation on threshold voltage, power supply and temperature variation.

II. Subthreshold Circuits

In the strong inversion region, the active energy of a gate dominates the total energy dissipated. A model of the active energy dissipated in a circuit is

$$E_{active}=\alpha C V_{dd}^2 \quad (1)$$

where α is the activity factor, C is the total switched capacitance of the gate, and V_{dd} is the power supply. Voltage scaling has had the largest impact on reducing energy dissipation since energy has a quadratic relationship to voltage supply. However, to satisfy performance requirements, the threshold voltage is lowered. However, lowering threshold voltage has a negative impact on static or idle mode energy, which is given by

$$E_{leak} = V_{dd} K e^{\left(\frac{V_{gs}-V_{th}}{nV_T}\right)}\left[1-e^{-\frac{V_{ds}}{V_T}}\right]T_c \quad (2)$$

where, K is a technology related factor, V_T is the thermal voltage which is temperature dependent and T_c is the clock period. This equation shows that the leakage current has an exponential relationship to the threshold voltage (V_{th}) and a quadratic relationship to temperature (T).

In this work we analyze for the at-threshold region (V_{dd}=V_{th}) and the subthreshold region (V_{dd}<V_{th}). For static CMOS circuits, as voltage supplies are scaled to the 100-600 mV range, design considerations such as noise margins, switching characteristics, etc., will scale down with voltage supply. We will look into the impact of voltage scaling on performance and energy dissipation, and also perform sensitivity analysis of subthreshold circuits to changes in threshold voltage and temperature.

III. Optimal V_{dd} and V_{th} Operating Points

In previous research contours of energy-delay product (EDP) have been plotted to give the optimal operating point (for minimum EDP) in the strong inversion region [6]. In this work, we explicitly evaluate two metrics, energy and delay, for a fixed throughput system. Exploring the energy and delay for the entire region, gives better understanding into the trade-offs between low power and high performance. Also, through this analysis, the optimal supply voltage and threshold voltage operating points can be found. In this work we look at energy and delay simulations of a variable activity factor ring oscillator characterization circuit for a 0.18-µm process to build intuition about optimal V_{dd} and V_{th} scaling.

A. Variable Activity Factor Characterization Circuit

Fig. 1 shows the variable activity factor characterization circuit used in this analysis. The circuit consists of a 11-stage 2-input nand ring oscillator with 9 additional 11-stage nand delay chains driven by the ring oscillator. This circuit is used to model pipeline delays for current microprocessor design.

This circuit enables variable activity factor by changing the proportion of gates switching. The Select inputs to the delay chains can be used to “activate/deactivate” different delay chains. When all Select inputs are “high”, the activity factor 1, (i.e. all nodes in the ring oscillator are switching during the clock period). However, in typical logic gates, the activity factor is rarely equal to 1. By setting one Select input to “low”, then the corresponding For example, by selecting Select0-Select4 “high” and Select5-Select9 “low”, half of the gates are switching, while the other half is idle, and the activity factor is 1/2. As activity factor decreases, the switching energy also decreases, and total energy is dominated by leakage energy.

The delay of the circuit is the delay through the ring oscillator, giving the highest clock frequency for a given V_{dd}-V_{th} operating point. The energy of the circuit has both active energy and leakage energy.

B. Energy and Performance contours

Simulations of the energy and performance variable activity factor ring oscillator circuit in Fig. 1 are performed using BSIM3 models of a 0.18-µm process [7].

Fig. 2 shows constant normalized performance and energy curves for α=1 (constant activity). The straight thick lines are contours of constant performance. The performance varies between 10 kHz and 100 MHz. These simulations show that at the line of “at-threshold” or V_{dd}=V_{th} (diagonal dotted line), the highest achievable performance is only 10MHz. For applications which require clock frequencies lower than 10MHz, operation in the subthreshold regime is

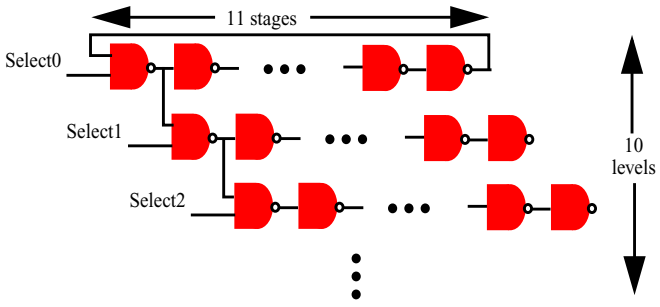

Figure 1. Circuit to show energy and performance in subthreshold region for variable activity factor.

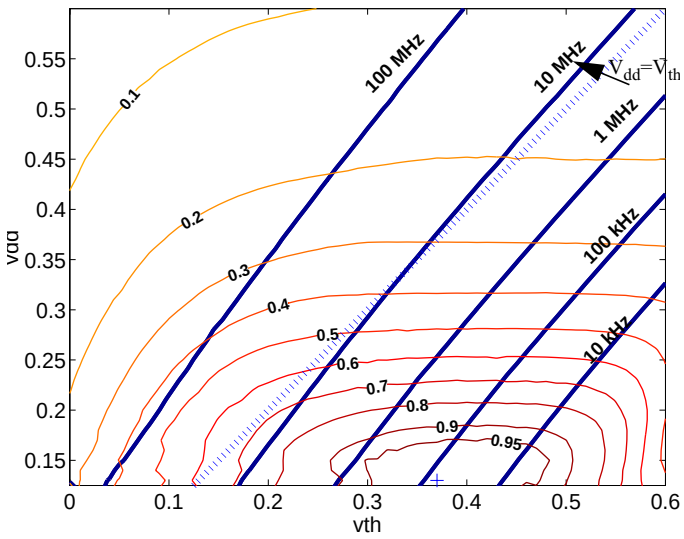

Figure 2. Constant Energy and Delay contours for ring oscillator circuit with activity factor = 1.

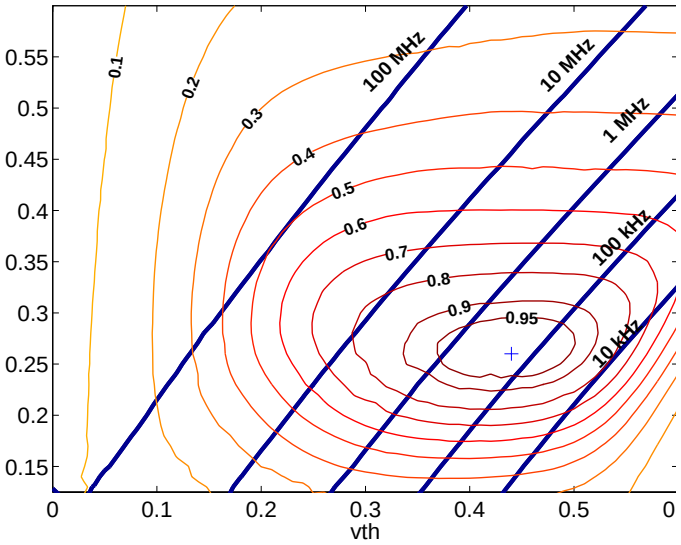

Figure 3. Constant energy and delay contours for decreased activity factor α=0.1.

suggested for minimal energy dissipation.

The thin rounded curves are contours of constant energy. The minimum energy point which is given by the '+' mark is at V_{dd}= 130mV and V_{th}= 370mV. At the minimum energy point, the energy per clock cycle dissipated by the circuit is 0.19 fJ/gate, and the ring oscillator clock frequency is 69 kHz. In order to operate at the minimum energy point of the region, the application should have extremely low performance requirements.

The contours around the minimum energy point are constant normalized energy contours which is defined as

$$\text{Normalized Energy} = \min(\text{Energy})/\text{Energy} \qquad (3)$$

which is the inverse of energy normalized by the minimum energy point. For example, the line labeled 0.5, indicates the constant energy contour which is twice the minimum energy point.

These energy contours show the relationship between leakage energy and active energy. For V_{dd}< 130 mV or when V_{th}< 370 mV leakage energy begins to dominate over active energy. Also simulations have shown that below V_{dd} = 0.2V, the output voltage of the ring oscillator is not rail-to-rail, thus sacrificing noise margins.

Next, by using the selector inputs, the activity factor can be decreased to simulate the energy dissipation of more realistic logic gates. Fig. 3 shows the effect of the activity factor (α=0.1) on the constant energy curves. This curves show that the operating points V_{dd}-V_{th} for the minimum energy point increase, as increased idle time means increased proportion of energy attributed to leakage current.

One conclusion drawn from these curves is that low-to-moderate performance circuits can benefit from hundreds of millivolt voltage supply and threshold voltage scaling. Typically, the supply voltage is 1.8V and threshold voltage is 0.47V, for high performance operation in this process. However, for many circuits where high performance is not necessary scaling down to the optimal voltage supply and threshold voltage can save orders of magnitude of energy dissipation.

The optimal V_{dd}-V_{th} operating points can be extracted from these curves, which is useful for circuit design. The optimal operating point is the V_{dd}-V_{th} which gives the minimum energy dissipated for a desired clock frequency. This point is where the performance curve is tangent to one of the energy curves. Fig. 4 shows the average energy dissipation and worst case performance of a 16-bit ripple carry adder circuit. The dotted curved line shows the optimal V_{dd}-V_{th} for the adder, for different input frequencies. These results show that the energy-performance contours of the characterization circuit can be scaled up to larger logic blocks and this analysis can be used to extract the optimal V_{dd}-V_{th} for large circuit

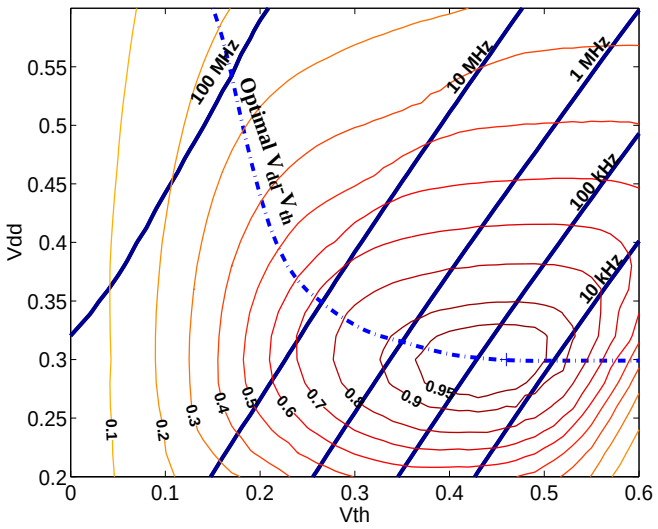

Figure 4. Average energy dissipation and performance for a 16-bit adder. The dotted line indicates the optimal V_{dd}-V_{th} operation points for the adder.

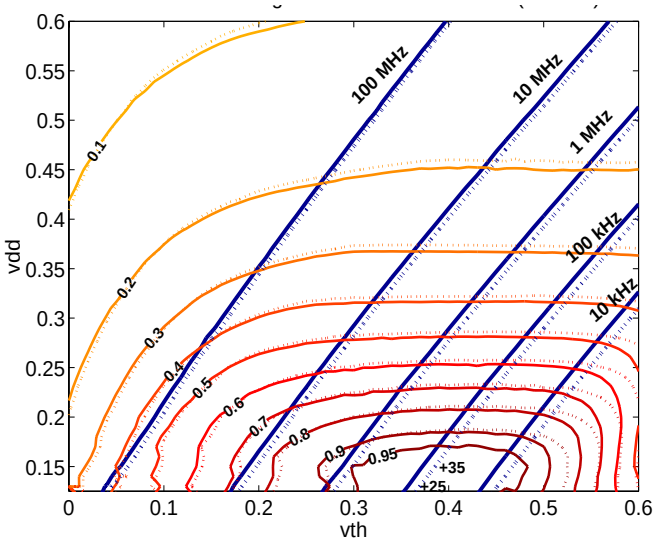

Figure 5. Comparing the energy and performance contours for the nominal case (T=25^{o}C) and the effects of increasing temperature (T=35^{o}C).

designs.

IV. Variations in V_{th} and Temperature

One of the drawbacks to operation in the subthreshold region is that the performance and energy contours are subjected to large changes due to process variations and to operating temperatures. This is impractical as voltage levels scale down to hundreds of millivolt levels and the circuits become more sensitive to operating conditions. Significant variations are caused by process variations, environment conditions and parameter uncertainty.

These contours can be used by designers to overdesign for a given constraint on the allowable variation, by doing a sensitivity analysis of the energy and performance contours. Increasing or decreasing V_{th} translates to a shift in the contours by right or left, respectively. An increase/decrease in temperature also causes additional changes in V_{th} and in leakage currents. Fig. 5 shows the effect of a small increase of temperature on the energy and performance contours.The solid line shows the nominal contours for energy and performance for T=25^{o}C, and the dotted line shows the contours for T=35^{o}C. This analysis shows that in general an increase in temperature improves performance at the expense of increasing energy dissipation. In the subthreshold region, the effect of temperature causes greater variation in performance and energy than in the strong inversion region.

In high performance circuits, the circuit junctions can achieve temperatures as high as 125^{o}C. In our analysis, the supply voltage of the subthreshold circuits are at hundreds of millivolt levels and therefore there is only a small temperature variation due to power dissipated.

An analysis of the optimal V_{dd}-V_{th} operating points with parameter variation is necessary. We assume that the worst case performance is primarily due to increased temperature and process variations which cause increased threshold voltage. Fig. 6 shows the optimal V_{dd}-V_{th} operating points for the corner which gives the worst case performance for α=0.1. When compared to the nominal case, without parameter variation, the optimal V_{dd}-V_{th} curve shifts towards higher V_{dd} and lower V_{th} for the same performance.

One conclusion from this analysis is that fine-grained threshold voltage control is necessary for subthreshold circuits. Methods previously suggested for threshold voltage control include using adaptive back biasing [8] and leakage controlled feedback circuits [9].

V. Conclusions

This research has shown the effect of voltage supply and threshold voltage scaling into the subthreshold region on two metrics: energy and performance. The energy and performance contours of a the variable activity factor characterization circuit give intuition into the effect of voltage scaling limits for a 0.18-µm process and also show that ultra low voltage circuits can achieve up 100 MHz operation. These results are helpful in circuit design of applications which require ultra low power dissipation and low-to-moderate performance. From the energy and delay curves of the variable activity factor characterization circuit, the optimal V_{dd}-V_{th} operating points for minimal energy dissipation can be found. Also we show the effect of activity factor on the opti-

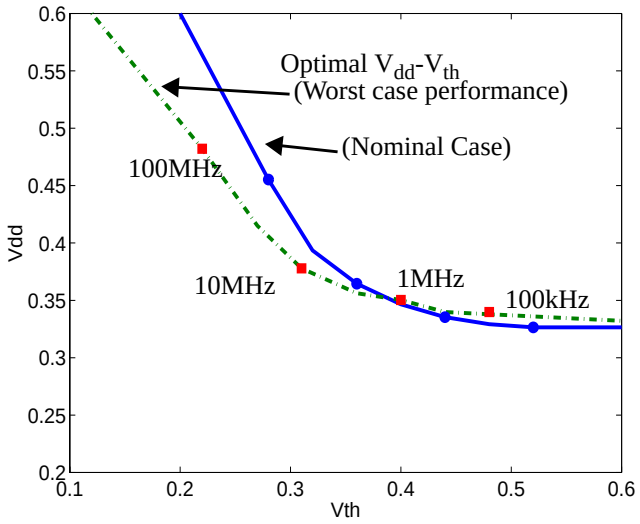

Figure 6. Optimal V_{dd}-V_{th} operating points for the worst case energy and performance corners compared to the nominal case (α=0.1)

mal operating point. Also this work can be extended to large logic block such as adders and multipliers.

Also included in this research is a parameter sensitivity analysis of threshold voltage and temperature variations. We show that the characterization circuit can also give V_{dd}-V_{th} operating points, by analyzing the worst case performance and energy contours for a given process variation and operating conditions.

VI. References

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