Wiring Requirement and Three-Dimensional Integration of Field-Programmable Gate Arrays

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ABSTRACT

In this paper analytical models for predicting interconnect requirements in field-programmable gate arrays (FPGAs) are presented, and opportunities for 3-D implementation of FPGAs are examined. The analytical models for 2-D FPGAs are calibrated by routing and placement experiments with benchmark circuits and extended to 3-D FPGAs. Based on system-level modeling, we find that in FPGAs with 20K 4-input look-up tables, the reduction in channel width, interconnect delay, and power dissipation can be over 50% by 3-D implementation.

Keywords

3-D integrated circuits, system-level modeling, wire-length, and FPGA.

1. INTRODUCTION

There are several options for implementing a digital integrated circuit in silicon. In one end of the spectrum, one can use full-custom designs that require time-intensive design, verification, and optimization to achieve maximal performance. On the other end of the spectrum, field-programmable gate array (FPGA) based design can be used. In FPGA-based implementation, a design is mapped onto an array of reconfigurable logic blocks that are connected by programmable interconnections [3, 18] . The fine-grain architecture in FPGAs is suitable for bit- and byte-level computation [3]. They can also be used as flexible logic resources for encryption, error corrections, address generations, etc. Though FPGA- based implementation requires fewer design iterations and has the advantage of shorter time-to-market, the system performance and logic density in FPGA-based implementation is not as high as full-custom designs due to the area and performance overhead of programmable interconnects.

In some recent studies, it has been found that in SRAM-based FPGAs 40%-80% of overall design delay and 90% of chip area are attributed to programmable interconnects [3, 8]. Recently, it has also been found that in SRAM-based FPGAs more than 80% of total power is dissipated in interconnects and clock networks [12]. Considering the area, delay, and power dissipation overhead, the programmable interconnect is a key design element in FPGA-based implementation.

Recently, there have been renewed interests in three-dimensional ICs to reduce interconnect delay and to increase gate density in future VLSI applications [10, 14, 15, 16, 17]. Three-dimensional integrated circuits are formed by monolithic vertical integration of multiple strata using wafer bonding, selective epitaxial growth, or recrystallization, where a stratum consists of a device layer and several interconnect levels. Cross section of a 3-D IC based on wafer bonding is shown in Figure 1.

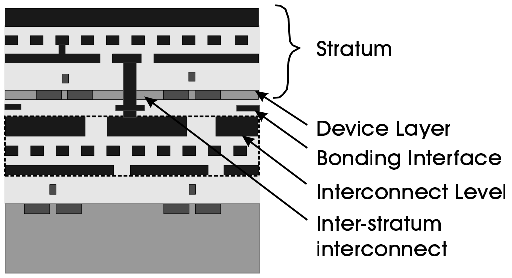

Figure 1. Cross section fo a 3-D IC based on low-temperature wafer bonding.

By 3-D integration, significant reduction in wire-length and wiring-limited chip area can be achieved [15]. Considering the overhead on delay and chip area due to the programmable interconnects, FPGA seems to be an ideal candidate that could benefit significantly by 3-D integration. In this paper, opportunities for 3-D implementation of FPGAs are explored based on system-level modeling and analysis. First, analytical models for predicting channel width in 2-D FPGAs are developed and verified, and then these models are extended to 3-D FPGAs. Some of the recent studies on 3-D FPGA were focused mainly on the FPGA architecture [1, 4, 13]. In this paper, system-level issues as well as the impact of 3-D FPGA architecture on key performance metrics such as chip area, delay, power dissipation, etc. are discussed.

2. SRAM-BASED FIELD-PROGRAMMABLE GATE ARRAYS

2.1 Background

The implementation of FPGAs in silicon falls into three groups: SRAM-programmed, antifuse-programmed, and EPROM-pro-

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grammed [18]. The configurable logic blocks in different implementations are very similar. The primary difference in various implementations is in the programmable routing architecture and the way it is configured. Due to its immense popularity, SRAM-based FPGAs will be considered in the paper. However, the modeling framework presented in this paper can be extended easily to other approaches to FPGA design.

A generic SRAM-based FPGA architecture is depicted in Figure 2. It consists of a two-dimensional array of logic blocks and horizontal and vertical routing channels. The configurable logic blocks (CLBs) or look-up tables (LUTs) can be programmed to perform a variety of functions for a set of input variables. The number of unique inputs, K, to a LUT can range anywhere from 2 to as high as 16. It has been found that for the most area-efficient design, the optimum value of K is approximately 3-4 [3].

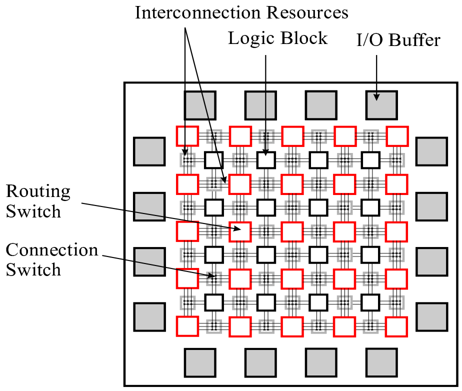

Figure 2. A generic SRAM-based field-programmable gate array.

The programmable interconnections in SRAM-based FPGA consist of routing switches, connection switches, and interconnect segments. In Figure 3, schematics of conventional routing and connection switches are shown. The routing switch is generally implemented by pass transistors or tri-state buffers. The flexibility of a routing switch is determined by the maximum allowable fan-out, F_s, provided to an incoming wiring segment by the routing switch. A popular 2-D routing switch allows each incoming wiring segment to connect to wiring segments on three other sides of the routing switch box, resulting in $F_s = 3$ [20]. An extension of this routing switch topology to 3-D will result in $F_s = 5$. The connection switches are used to establish input or output connections between programmable logic blocks and wire segments. The flexibility of a connection switch is determined by the number of tracks, F_c, each logic block pin can connect to. By routing a set of benchmark circuits, it has been found that for complete routability it is sufficient to have $0.7W \le F_c \le W$, where W is the channel width.

In early FPGAs, wiring tracks consisted mostly of short wire segments that spanned one LUT or one unit. Longer wires could be formed by connecting short wire-segments using pass transistor routing switches. Though one unit long wire segments provide good wiring utilization, they degrade the performance of long interconnections. This is because long interconnections are formed by connecting many pass transistors which add significant series resistance and capacitance. To reduce the number of pass transistors in long interconnections, wire segments of various lengths are used in high-performance FPGAs [20]. Though an assortment of wire segments reduces signal delay in long interconnections, it can result in under-utilization of many long wire segments and an increase in channel width and chip area.

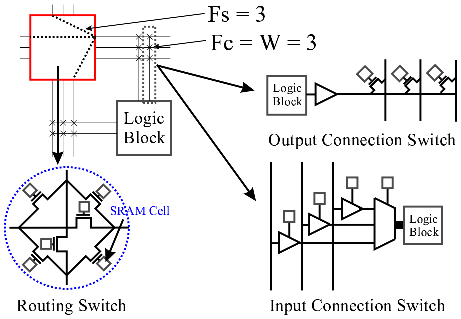

Figure 3. Programmable routing and connection switches in SRAM-based FPGAs

2.2 Performance Metrics

Some of the key performance metrics for SRAM-based FPGAs are:

Logic Density
Routability
Speed

Logic density in FPGA-based design is generally expressed in terms of gate counts per chip or unit area. It is the equivalent number of 2-input NAND gates that would be required to implement the same functionality. However, FPGAs don't consist of 2-input NAND gates. They have logic components such as LUTs, multiplexers, flip-flops, etc. A more accurate methodology for measuring logic density is based on the concept of equivalent logic cells [20]. A logic cell can be defined as the combination of a 4-input LUT and dedicated registers.

Routability describes the effectiveness in utilizing the programmable routing resource. Routability of a design in FPGAs depends strongly on the configuration of wire segments as well as on the values of W, F_s, and F_c. These parameters are determined heuristically by the wiring need of representative benchmark designs.

The *speed or performance* in FPGAs is limited by interconnect delay, and it can account for *40%-80%* of overall design delay [8]. The wiring nets in FPGAs are more resistive and capacitive compared to wiring nets of similar length in custom designs. This is due to the higher resistance and capacitance of pass transistors in programmable interconnections.

Since a large fraction of the chip area in FPGAs is dedicated to programmable interconnects, it is not surprising that most of the power in FPGAs is dissipated in reconfigurable interconnects. Recently, a detailed analysis of power consumption in Xilinx

XC4003A revealed that 80% of total power dissipation was due to driving interconnects and clock network capacitance [12].

In the next sections, a system-level modeling framework will be presented to estimate some of these performance metrics for conventional (2-D) SRAM-based FPGAs. By extending the models for 2-D FPGAs to three-dimension, key advantages for 3-D implementation of FPGAs will also be examined.

3. STOCHASTIC MODELS FOR PREDICTING ROUTABILITY IN FPGAs

The implementation of a design using FPGA consists of several steps. First, a high-level description of a circuit/system is converted to a set of boolean equations. These equations are optimized to minimize the number of logic gates and then mapped to a programmable logic array architecture. After the logic mapping, placement and routing are conducted to determine the values of configuration memory bits for connection and routing switches.

The routability of a design in FPGA-based implementation depends on the configuration of the LUTs and routing resource. Typically, they are determined by placement and routing experiments with benchmark circuits. In this section, we address the routability of a design in FPGAs, before place-and-route, based on analytical models. These models are useful for providing an early feedback for various design trade-offs without having to go though many iterations of time consuming and laborious placement and routing process.

3.1 Earlier Work

A popular analytical model for predicting routability in gate arrays is based on a two-dimensional stochastic model for channel width by Gamal [11]. His analysis suggests that the channel width, *W*, in array based FPGAs follows Poisson distribution, and the average channel width, $\overline{W}$, is given by $\overline{W} = \frac{\gamma\bar{L}}{2}$, where $\bar{L}$ is the average wire-length and γ is the average number of wires emanating from each logic block [11]. An enhancement of Gamal's model has also been proposed that takes into account multi-terminal nets for predicting channel width [5]. Recently, it has been found that routability is best predicted by estimating the total wire-length in a circuit, not by the mean wire-length times pins per cell as described in Gamal's model [6]. We also find this to be consistent with our routing and placement experiments with benchmark circuits. In [6], random net lists were generated based on a set of input parameters such as pins per LUT, Rent's parameters, etc. In deriving our model for predicting channel width, a similar methodology has been followed. However, the total wire-length is estimated based on the stochastic wire-length distribution [7, 15].

3.2 Proposed Model

We use the stochastic wire-length distribution model [7, 15] to estimate the wiring complexity in gate arrays. In a *K*-input LUT table based FPGA, Rent's constant, $k \le K + 1$, and a typical value of Rent's exponent, *p*, is in the range of *0.7-0.8* [5]. In 2-D FPGAs with one unit long wire segments, channel width is given by

$$W = \frac{\sum_{1}^{2\sqrt{N}-2} lf(l, k, p)\chi_{fpga} + l_r}{2Ne_t} \qquad (1)$$

where *l* is the wire-length, *f(l, k, p)* is the wire-length distribution, χ_{fpga} is a point-to-point to net-length conversion factor, l_r is the additional length of occupied wiring tracks due to non-ideal locations of input/output terminals in the LUT (see Figure 4), and e_t is the utilization factor of wiring tracks. The derivation of Eq. 1 is based on the assumption that for a design, the available length of wiring tracks, $W2Ne_t$, is equal to the required total wire-length, $\sum_{1}^{2\sqrt{N}-2} lf(l, k, p)\chi_{fpga} + l_r$. The values of χ_{fpga} and e_t can be estimated and calibrated by placement and routing of benchmark circuits in FPGA architecture.

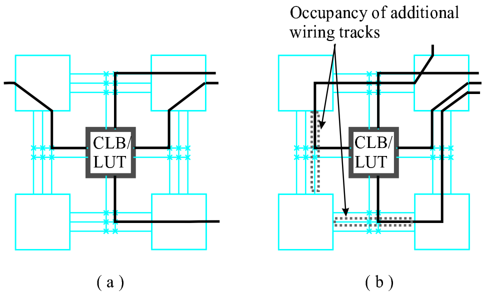

Figure 4. (a) An ideal scenario where connections to input/output terminals of a LUT do not require additional wire-segments. (b) A non-ideal scenario that requires utilization of 2 additional wire segments for making input/output connections.

3.3 Validation and Calibration

To examine the wiring complexity in SRAM-based FPGAs, we use a set of benchmark circuits and a place-and-route tool, SEGment Allocator (SEGA), developed at University of Toronto [19]. SEGA performs routing and placement to optimize for speed-performance. It is assumed that all routing channels have equal number of tracks, *W*. For simplicity, we also assume all wire segments are one unit long, $F_c = W$, and $F_s = 3$. The logic functions for the benchmark circuits are mapped to 4-input LUT based FPGAs. Using SEGA, we estimate the minimum value of *W* that would result in *100%* routability for the benchmark circuits. One of the outputs of the routing tool is the number of shared wire-segments used by nets with fan-out more than one. We find that only 5% - 10% of wire-segments are shared, resulting in $\chi_{fpga} = .90\text{-}.95$. Based on the placement and routing of benchmark circuits in SEGA, we find that e_t = .40-.50.

In Figure 5, the number of graphs or point-to-point interconnects for benchmark circuits and the projections based on Rent's rule are shown. By hierarchically partitioning a logic graph, it can be shown that the total number of point-to-point interconnects in an IC is given by [9]

$$I_{total} = \frac{fo}{fo+1} \cdot kN(1 - N^{(p-1)}) \quad (2)$$

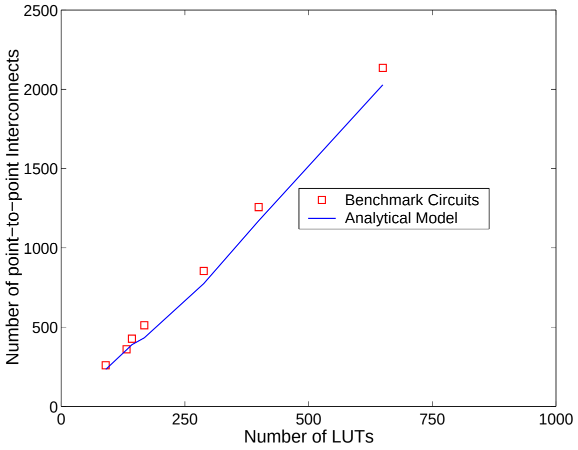

Figure 5. Number of point-to-point interconnects in benchmark circuits that are mapped to 4-input LUT based FPGAs.

We find that the analytical model, based on Donath's methodology [9], for estimating total number of interconnects agrees very well with routing and placement results from benchmark circuits. For this analysis, it has been assumed that $k = 5$ and $p = .75$. Even though individual circuits may have different Rent's parameters, interconnection complexity as a function of number of LUTs can be predicted quite accurately by assuming $k = K + 1 = 5$ and $p = .75$

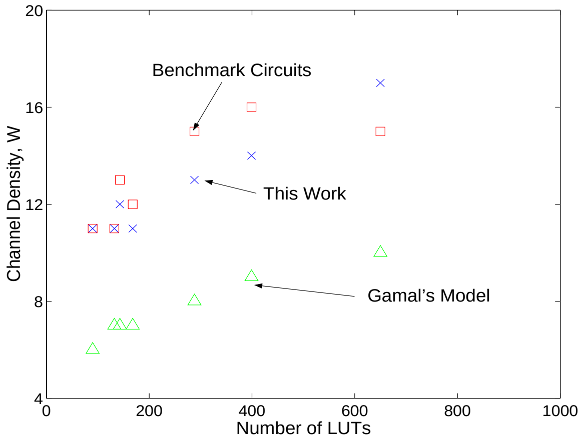

Figure 6. Channel width for the benchmark circuits, implemented in 4-input LUT based FPGAs, based on routing and placement experiments using SEGA [19] and analytical models.

Next, the channel width, *W*, is estimated using Eq. 1. Based on observation from routing and placement of benchmark circuits, we assume *50%* input/output terminals in LUTs could be located on the undesirable sides, and they contribute to additional wire-length of $l_r = 50XI_{total}l'$, where $l' = 1$. We also assume $\chi_{fpga} = .95$ and $e_t = 40\%$. In Figure 6, estimated values of channel width for the benchmark circuits are compared with the results from SEGA and Gamal's analytical model for average channel width. The agreement between our analytical models and the actual channel width is generally quite reasonable.

4. OPPPORTUTNITIES FOR 3-D IMPLEMENTATION OF FPGAS

In the earlier section, it has been shown that channel width in array-based FPGAs is proportional to the total wire-length. Three-dimensional integration can result in a significant reduction in total-wire length. As a result, the channel width in FPGA can be reduced by 3-D integration which may lead to reduction in chip area and improvements in system performance. In the past, various approaches for implementing 3-D FPGAs have been considered [4]. They include FPGAs based on 3-D routing switches with electrical or optical inter-stratum interconnections [1] or partitioning of memory and routing functions in different strata [13]. These earlier works were focused on either routing architectures or FPGA technologies. In this section, both routability and technology related issues in 3-D FPGAs will be examined.

4.1 Channel Width in 3-D FPGAs

We consider a 3-D implementation of FPGA architecture with 3-D routing switches, as shown in Figure 7 and also discussed in [1]. We assume $F_c = W$ and $F_s = 5$, where each incoming wire-segment can connect to other wire-segments on five sides of a cubic switch box. We also assume the wiring track utilization in 3-D FPGA is comparable to that of 2-D implementation. One of the drawbacks in implementing 3-D routing switch is that it would require more pass transistors and SRAM cells per routing switch box per channel. However, if the channel width can be reduced by 3-D integration, it will be possible to reduce the total number of routing switches and configurable memory bits.

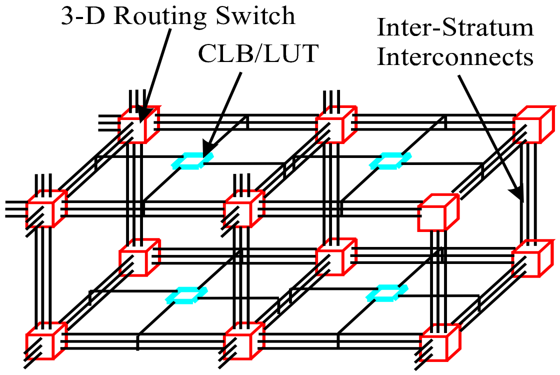

Figure 7. A 3-D implementation of FPGAs with 3-D routing switches.

Similar to Eq. 1, channel density in 3-D FPGAs is estimated by

$$W = \frac{\displaystyle\sum_{1}^{2\sqrt{N/N_z} - 2 + (N_z - 1)\cdot t_z} l f_{3D}(l, k, p, N_z)\chi_{fpga} + l_r}{\left(2N + \dfrac{(N_z - 1)N}{N_z}\right)\cdot e_t} \quad (3)$$

where $f_{3D}(l,k,p,N_z)$ is the 3-D wire-length distribution, N_z is the number of strata, t_z is the stratal pitch, and all other parameters are defined the same way as in Eq. 1. The higher value of the denominator reflects the availability of more wiring tracks due to inter-stratum wire segments. Considering our proposed 3-D IC technology [10], it has been assumed that the length of inter-stratum wire-segment between adjacent LUTs on neighboring strata is comparable to wire-length between adjacent LUTs on the same stratum. The wire-length distribution in 3-D configuration of gate arrays can be derived by extending the methodology used for estimating wire-length distribution of 2-D ICs [7, 15]. In Figure 8, estimated values of channel width are shown for 2-D and 3-D implementations of FPGAs as a function of number of LUTs. As more strata are integrated, the average and total wire-length become shorter, resulting in a significant reduction in channel width.

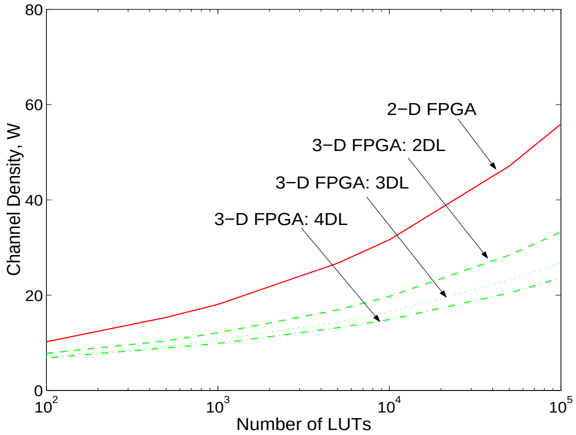

Figure 8. Channel width in 2-D and 3-D 4-input LUT based FPGAs as a function of number of LUTs. The routing resource consists of one unit long wire segments. It has been assumed that Rent's parameters *k = 5* and *p=0.75*, average *fan-out = 3.5*, χ_{fpga} *= 0.95*, and e_t *= 0.4*. DL stands for number of device layers or strata.

4.2 Logic Density

In SRAM-based FPGAs, chip area is primarily limited by the area dedicated to programmable interconnects and the configurable memory bits. In [8], by empirical observation, it has been found that *80%-90%* of the area in FPGA is dedicated to switches and wires making up the reconfigurable interconnect. The LUTs account for only a few percent of the total area. Due to the programmable interconnect overhead, there is roughly a *20X-50X* density disadvantage in FPGAs compared to a full-custom design [8].

The number of switches and programmable memory bits in FPGAs is roughly proportional to the channel width. In Section 4.1, it has been shown that by 3-D integration significant reduction in channel width can be achieved which could lead to smaller chip area and higher logic density. In this section, logic density in FPGAs will be estimated by modeling the area dedicated to LUTs, connection switches, routing switches, multiplexers, SRAMs, and buffers. The area model is based on counting the number of minimum-width transistor areas required for implementing FPGAs. We follow the methodology presented in [2] to estimate the chip area. In some recent works, dependencies of chip area and performance on transistor sizing have been investigated [2]. Based on these studies, as well as our own HSPICE-based analysis, we find that to minimize delay or power-delay product, the optimum value of pass transistor size in switches and buffers is roughly *10X-15X* the minimum-width transistor's size.

To estimate the improvements in logic density, measured by the number of LUTs per unit area per stratum, we consider FPGAs implemented with 4-input LUTs. The LUT consists of a pass transistor multiplexer, a register, and a set/reset logic block [2]. We estimate the area of input and output connection switches and routing switches using the switch configuration shown in Figure 3. We assume the buffer and pass transistor have *10X* minimum drive strength. The 3-D routing switch box requires $F_s(F_s + 1)/2 = 15$ pass transistors per channel compared to 6 transistors per channel in 2-D implementation. The area models for various components in SRAM-based FPGAs, measured in units of minimum width NMOS area, have been adopted from [2].

Using the models for chip area, improvements in LUT density have been calculated, and the simulation results are shown in Figure 9. In 3-D FPGAs, as the number of LUTs is increased, higher reduction in channel width can be achieved. As a result, the *improvement in LUT density* increases as more LUTs are integrated. Based on our analysis, in FPGAs with *70K* logic cells, the improvement in LUT density can be *25%-60%* in 3-D implementation with *2-4* strata.

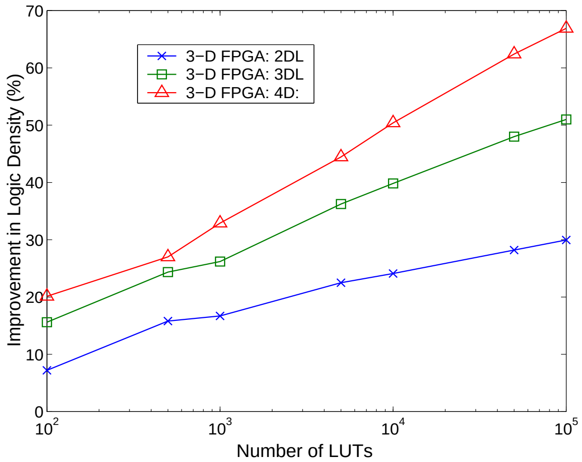

Figure 9. Improvement in logic density as function of number of LUTs and number of strata.

4.3 Interconnect Delay

In this section, interconnect delay of average length and chip-edge length interconnects in 2-D and 3-D FPGAs will estimated based on HSPICE simulation. We estimate the LUT area and wire-length assuming all wire segments are one unit long and using the models for LUT and chip area presented in [2]. Wire segments of various lengths are often used in FPGAs to reduce delay for long interconnections (see Figure 10). When long wire segments area used, as a result of under utilization of many wiring tracks, the chip area may increase [2]. In our analysis for estimating interconnect delay in long wire segments, for simplicity and illustration purposes, the increase in chip area due to the under-utilization of long wire segments is not taken into account.

We consider a 4-input LUT based FPGAs with *20K* LUTs and implemented in *.25* μ*m* technology. The estimated area per stratum for 2-D implementation and 3-D implementation with 2, 3, and 4 strata are *7.84* cm^2, *3.1* cm^2, *1.77* cm^2, and *1.21* cm^2, respectively. The corresponding values of channel density are 41, 24, 20, and 18, and the average wire-lengths, rounded to the nearest integer values, are 8, 6, 5, and 5. It is assumed that M3 and M4 interconnect levels are used for routing programmable interconnects; the wiring pitch is *8*λ, where λ is half of the minimum feature size. The estimated wiring capacitance and resistance are *2.8 pF/cm* and *540* Ω*/cm*, respectively. Though FPGAs implemented in *.25* μ*m* technology generation are considered in this study, the system-level models can be extended easily to scaled technologies. Using the monolithic 3-D integration technology [10], very high inter-stratum interconnect/via density can be achieved in scaled technologies which should be sufficient for meeting the inter-stratum connectivity requirements for 3-D FPGAs.

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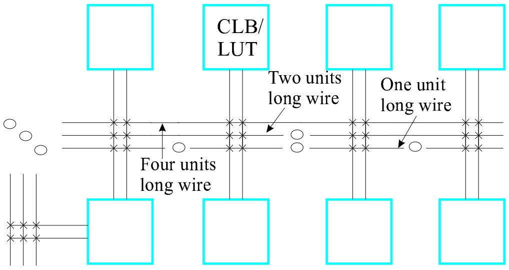

Figure 10. Alternative routing choices using various length wire segments in an SRAM-based FPGA. Wire-length is measured in units of LUT pitch, the average separation between neighboring LUTs.

We estimate interconnect delay from an output terminal of a LUT to an input terminal of another LUT, using HSPICE, for average length and chip-edge length wires. We assume average length connections are implemented using one unit long wire segments. In addition, in 3-D implementation, 2-D routing switch boxes are replaced by 3-D routing switches. The buffers and pass transistors have *10X* minimum drive strength, and a gate voltage of $V_{dd}+V_t$ is applied in pass transistors to eliminate a V_t drop across drain-to-source. HSPICE-based simulation results of interconnect delay of average-length wire in 2-D and 3-D FPGAs are shown in Figure 11. We find that the drain junction capacitance (at the output terminals of a LUT and routing switches) and interconnect capacitance are comparable for short interconnections. Both shorter wire length and reduction in channel density, *W*, result in lower capacitance for short interconnections in 3-D FPGAs, and subsequently, the reduction in interconnect delay.

Similarly, we have also examined interconnect delay of chip-edge length wires, as shown in Figure 11. We assume these wires are routed in 1/4 chip-edge length wire segments. Two cases are considered: in the first case there is no buffer driving the routing switches and in the second case *10X* buffers are inserted to drive 2-D and 3-D routing switches. We find that delay in chip-edge length connection is limited by interconnect's RC delay. The significant reduction in chip-edge length interconnection delay in 3-D FPGAs is primarily due to the lower wiring capacitance and resistance. Though the capacitive loading due to 3-D routing switches is higher compared to that of 2-D routing switches, they (3-D routing switches) do not seem to have a significant impact on overall delay.

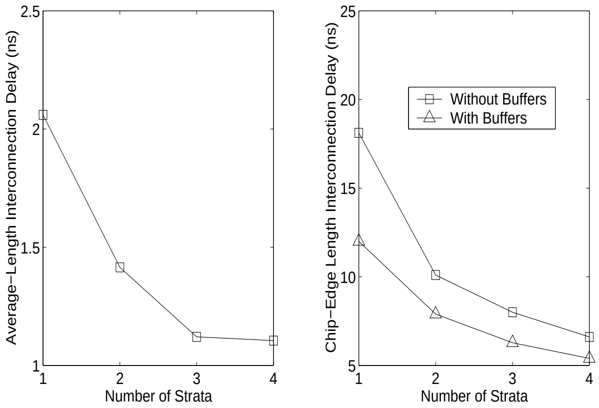

Figure 11. Interconnect delay as a function of number of strata in 2-D and 3-D FPGAs. The average-length wires are implemented by connecting one unit long wire segments, and the chip-edge length wires are implemented by connecting four 1/4 of chip-edge length wire segments.

4.4 Power Dissipation

We have also estimated the power dissipation in 2-D and 3-D FPGAs, based on system-level modeling and analysis, by taking into account power dissipation in LUTs, clock network, and programmable interconnections. In a typical 4-input LUT based 2-D FPGA, implemented in *.25* μ*m* technology node, we find that power dissipation in programmable interconnects is *50%-60%* and in clock network *37%-45%* of total power dissipation. The rest of total power dissipation is in LUTs. Within the programmable interconnection, the total power dissipation associated with connection switches, routing switches, and buffers is comparable to that of signal interconnects.

In Figure 12, estimated values of total power dissipation are presented for 2-D and 3-D FPGAs with *20K* LUTs as a function of number of strata. We assume the FPGA is implemented in *.25* μ*m* technology with *2.5 V* supply voltage; the clock frequency is *10 MHz* which is typical for FPGAs such as XC4000XV with comparable number of equivalent logic cells [20]. By 3-D integration with *2-4* strata and the same clock frequency as 2-D FPGAs, the reduction in power dissipation is *35%-55%*.

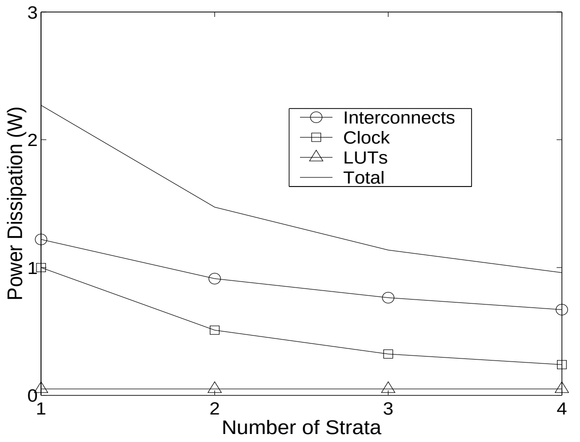

Figure 12. Power dissipation in 2-D and 3-D FPGAs with 20K logic cells and implemented in *.25* µ*m* technology node with *2.5 V* supply voltage and *100 MHz* clock frequency.

5. SUMMARY

In this paper models for predicting channel width in 2-D and 3-D FPGAs, based on stochastic wire-length distribution, have been presented, and opportunities for 3-D implementation of FPGAs have been discussed. In 3-D FPGAs with *20K* LUTs and 2-4 strata, *20%-40%* improvement in LUT density can be achieved. The reduction in interconnect delay by 3-D integration can be as much as *45%* for short interconnects and *60%* for long interconnects. Similar reduction in total power dissipation is also feasible for comparable system performance. Though simulation results are presented for *.25* µ*m* technology generation, similar studies can be performed for technology generations with smaller feature sizes. The modeling work presented here can also be extended easily to examine the impact of various segmented wiring architecture on chip area and system performance.

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