Low Power Bus Coding Techniques Considering Inter-wire Capacitances

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1. ABSTRACT

The power dissipation associated with driving data busses can be significant, especially considering the increasing component of inter-wire capacitance. Previous work on bus encoding has focused on minimizing transitions to reduced power dissipation. In this paper, it is shown that transition reduction is not necessarily the best approach for reducing power when the effects of inter-wire capacitance are considered. An electrical model for data busses designed with submicron technologies is presented along with a family of coding techniques that can reduce the average power consumption of the bus by *40%*.

2. INTRODUCTION

An important component of the power consumption in digital processors involves the transmission of data through high capacitance busses. Several techniques have been proposed to reduce the power dissipation in these busses through the use of coding techniques, low-swing signaling, and charge recycling [1] [2] [3]. The use of reduced swing communication is attractive, but also suffers from reduced signal to noise, especially as the power supply voltages are scaled [4][5][6]. An excellent reference that compare various low-swing techniques is presented in [7].

The coding of data has been explored for reducing power dissipation through the reduction of transitions. The basic idea is to add redundancy to encode the data bus. One effective technique approach proposed is the bus-invert technique in which the data bus is conditionally inverted to reduce the overall transitions [8]. If more than 50% of the bits change, the whole bus is inverted. Threfore, in addition to the data, an extra bit must be transmitted to indicate if the bus is inverted. In [9], temporal data correlations are exploited to reduce switching activity. Fundamental bounds on transition reduction are developed.

3. BUS AND DRIVER MODEL

The previous work on data bus coding use a simple electrical model in which lines are simply replaced by lumped grounded capacitors. Although this model is convenient for closed form mathematical analysis of the power consumption, it is not appropriate for submicron technologies. This is because the smaller scales make the distributive nature of the lines non negligible and even more because lines are placed geometrically closer to each other, so the interwire capacitances C_I become important with respect to the substrate capacitances C_L (see Figure 1).

In Figure 1 the lines are shown along with their dominant parasitic elements and their voltages $V_1, V_2, \ldots, V_n$. The C_L 's are the parasitic capacitors to substrate or other near by elements with constant potentials and the C_I 's are the parasitic capacitors between the lines. The values of all C_L 's are assumed to be the same. Similarly for the C_I 's. For this model not only the transitions of the voltages $V_1, V_2, \ldots, V_n$ are responsible for the power consumption but also the relative transitions of the voltages of adjacent lines. This implies that the transition activity by itself is no longer the appropriate "measure" of power consumption. This complicates the exact calculation of the power consumption (making the standard assumption that the data sequences are white noise of 0 's and 1 's). In future work, we will extend this model to include the distributed nature of the wire.

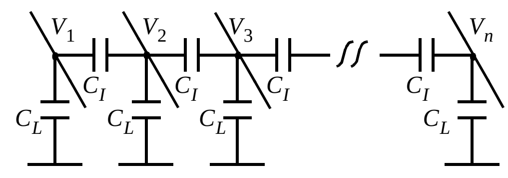

Figure 1: Simple model for the data bus.

In order to calculate the energy consumption caused by a transition using the above model, we need a model for the drivers of the lines too. We adopt the following simple one.

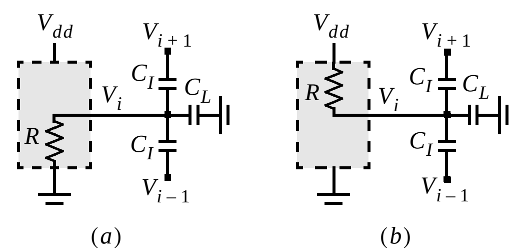

Figure 2: Equivalent circuits for the drivers

Figure 2a corresponds to the output of the line driver when it applies a low signal to the line. The resistor R is the *on* resistor of the NMOS. Similarly for the Figure 2b, R is the *on* resistor of the PMOS. The two resistors are not assumed to be constant (similar to the case described in [10] for a CMOS inverter driving a lumped capacitance).

4. DERIVATION OF THE ENERGY FUNCTION

Combining the model of the data bus with the one of the drivers, we have the circuit in Figure 3. The buffers are replaced with resistors that are either connected to power supply (V_{dd}) or GND.

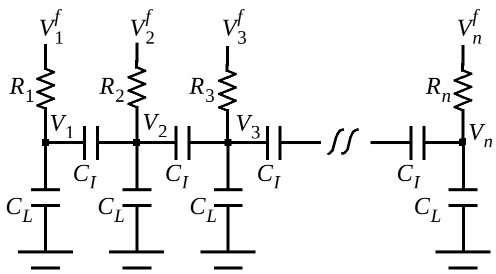

Figure 3: Drivers and lines combined

The voltages $V_1^f, V_2^f, \ldots, V_n^f$ take the values 0 or V_{dd} depending on the *logical* values of the lines we want to establish. Setting

$$\lambda = \frac{C_I}{C_L} \tag{1}$$

we have the following equations describing the operation of the circuit for $k = 2, \ldots, n-1$.

$$C_L \cdot \left[(1+\lambda) \cdot \frac{dV_1}{dt} - \lambda \cdot \frac{dV_2}{dt}\right] = \frac{V_1^f - V_1}{R_1(t)} \tag{2}$$

$$C_L \cdot \left[-\lambda \cdot \frac{dV_{k-1}}{dt} + (1+2\lambda) \cdot \frac{dV_k}{dt} - \lambda \cdot \frac{dV_{k+1}}{dt}\right] = \frac{V_k^f - V_k}{R_k(t)} \tag{3}$$

$$C_L \cdot \left[-\lambda \cdot \frac{dV_{n-1}}{dt} + (1+\lambda) \cdot \frac{dV_n}{dt}\right] = \frac{V_n^f - V_n}{R_n(t)} \tag{4}$$

Now let

$$V_1(0) = V_1^i, \ldots, V_n(0) = V_n^i \tag{5}$$

be the initial values of the voltages $V_1, V_2, \ldots, V_n$, and each of the $V_1^i, V_2^i, \ldots, V_n^i$ is either 0 or V_{dd}. The final values of the voltages practically exist and are $V_1^f, V_2^f, \ldots, V_n^f$. Here we do the reasonable assumption that the clock period is long enough for the voltages to settle in their new values. So,

$$V_1(\infty) = V_1^f, \ldots, V_n(\infty) = V_n^f \tag{6}$$

and the energy consumed (or deposited) by the driver k during the transition is:

$$E_k = \int_0^\infty V_k^f \cdot \left(\frac{V_k^f - V_k(t)}{R_k(t)}\right) dt = V_k^f \cdot \int_0^\infty \left(\frac{V_k^f - V_k(t)}{R_k(t)}\right) dt \tag{7}$$

Integrating Equation 2, 3, 4 from 0 to infinity and using Equations 5,6,7 we get,

$$E_1 = C_L \cdot [(1+\lambda) \cdot (V_1^f - V_1^i) - \lambda \cdot (V_2^f - V_2^i)] \cdot V_1^f \tag{8}$$

$$E_k = C_L \cdot [-\lambda \cdot (V_{k-1}^f - V_{k-1}^i) + (1+2\lambda) \cdot (V_k^f - V_k^i) - \ldots$$
$$\ldots - \lambda \cdot (V_{k+1}^f - V_{k+1}^i)] \cdot V_k^f \tag{9}$$

$$E_n = C_L \cdot [-\lambda \cdot (V_{n-1}^f - V_{n-1}^i) + (1+\lambda) \cdot (V_n^f - V_n^i)] \cdot V_n^f \tag{10}$$

Of course the total energy consumed during the transition is given by the sum,

$$E = \sum_{r=1}^{n} E_r = \sum_{r=1}^{n} E_r^L + \lambda \sum_{j=1}^{n-1} E_j^I . \tag{11}$$

where,

$$E_r^L = C_L \cdot V_r^f \cdot (V_r^f - V_r^i) \tag{12}$$

and

$$E_j^I = C_L \cdot [(V_{j+1}^f - V_j^f) \cdot (V_{j+1}^f - V_{j+1}^i + V_j^i - V_j^f)] \tag{13}$$
$$\ldots = C_L \cdot [(V_{j+1}^f - V_j^f)^2 + (V_{j+1}^f - V_j^f) \cdot (V_j^i - V_{j+1}^i)]$$

It should be mentioned that if we normalize the energy function by setting $C_L = 1$ and $V_{dd} = 1$, then the multiplications of the form $V_x^y \cdot V_z^w$ for any *x,y,z,w,* are reduced to logical AND operations. The calculation of E is then completed by counting *ones* and doing 5 additions and 1 multiplication (assuming λ is a convenient rational number could save a lot of complexity in the multiplication).

5. BUS CODING TECHNIQUES

For a data bus with *m-lines* a way of coding for low power is, first to expand it by adding *a-more* lines and then modify the driving circuit of the bus so that only the words of a subset Z of the (total) set $T = \{0,1\}^{m+a}$ are transmitted. Of course the subset Z must contain at least 2^m words whose average energy cost of use is less than the one of the original bus.

It is a principle of coding theory that the larger the data set you want to compress the higher the efficiency of the compression is. The same is true for the coding techniques for power reduction in data busses. Suppose that we could afford a large latency in the data transmission. Then we could store a long sequence of data, process it and then transmit it through the data bus. This in general would allow for very efficient power saving algorithms. Unfortunately a large latency is not usually accepted. In what follows we propose a family of coding schemes with minimal latency.

Let

$$D(k) = (d_1(k), d_2(k), \ldots, d_m(k)) \tag{14}$$

be the data vector that must be encoded and transmitted at the time moment k and let

$$L(k) = (l_1(k), l_2(k), \ldots, l_n(k)) \tag{15}$$

be the vector containing the logical values of the bus lines at time k. We set $n = m + a$ and decompose the vector $L(k)$ into two parts. The *data* part,

$$L^D(k) = (l_1(k), l_2(k), \ldots, l_m(k)) \tag{16}$$

and the *code* part,

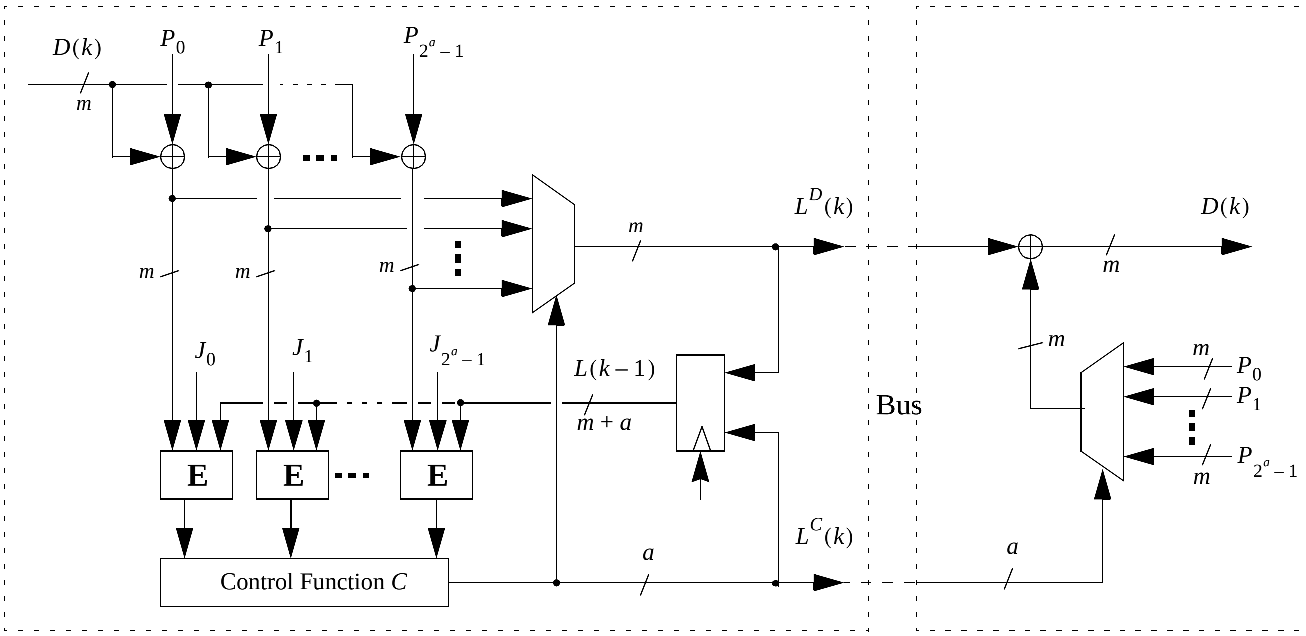

Figure 4: Bus Encoder and decoder

$$L^C(k) = (l_{m+1}(k), l_{m+2}(k), \ldots, l_n(k)) \,. \quad (17)$$

so, $L(k) = (L^D(k), L^C(k))$. In Figure 4, the encoder and decoder schemes are shown.

The function E is the energy function described above. The E-blocks in Figure 4 calculate the cost of transitions from the current state $L(k-1)$ of the extended bus to its possible now states

$$L(k) = (D(k) \oplus P_r, J_r) \quad (18)$$

for, $r = 0, 1, \ldots, 2^a - 1$. The J_r ‘s are the expressions of the index r in binary form, i.e.

$$J_0 = (0, \ldots 0), \ldots, J_{2^a-1} = (1, \ldots, 1) \quad (19)$$

Finally the *control* function C, is defined to give as output one of the J_r ‘s for which the transition from $L(k-1)$ to $L(k)$ has the *minimum* possible cost with respect to r.

5.1 A Special case

If the ratio λ is in the order of one or greater, an important part of the energy consumption E, is due to the interaction of adjacent lines. This motivates a choice of $P_r, r = 0, \ldots, 2^a - 1$ that “break” sequences of data patterns that would cause a lot of energy consumption. We give a class of such sets that has interesting energy saving results. In this case, the whole coding scheme can be thought as a generalization of the Bus-Invert technique [8].

We have chosen $P_r, r = 0, \ldots, 2^a - 1$ to be the 2^a different vectors that can be written as linear combinations of the following *basic* vectors $Y_1, Y_2, \ldots, Y_a$. In other words,

$$P_r = (r_1 \cdot Y_1) \oplus (r_2 \cdot Y_2) \oplus \ldots \oplus (r_a \cdot Y_a) \quad (20)$$

where, $r = (r_1, r_2, \ldots, r_a)$, $r_i \in \{0, 1\}$.

Y_1	**11111111111111111111111111.....11**
Y_2	**01010101010101010101010101.....01**
Y_3	**00110011001100110011001100.....11**
Y_4	**00001111000011110000111100.....11**
Y_5	**00000000111111110000000011.....11**
....	**...**
Y_a	**00000000000000000000000000.....11**

Table 1: Basic vectors for the encoder-decoder

6. SIMULATIONS

The encoder - decoder scheme described in section 4 was simulated using the class of sets P_r , $r \in \{0, 1\}^a$ defined above. A sequence of 5000, *m-bits* words was used in every simulation. The bits of the words were realizations of independent and uniformly distributed in $\{0, 1\}$ random variables. Finally, simulations were run for all combinations of the parameters, $m = 4, 8, 16, 32, 64$, $a = 1, 2, 3, 4$ and $\lambda = 0, 1, 2, \infty$. The figures below show the percentage of energy savings when the coding technique is used, this is equal to,

$$100\left(1 - \frac{E_c}{E_0}\right)\% \tag{21}$$

Where E_c is the total energy consumed when the coding was used and E_0 is the total energy consumed without coding. The energies were calculated using Equations 11,12,13. In this initial research, the power consumption of the encoder and decoder circuits were ignored. This approximation remains valid for very high capacitance data busses and for small values of the parameter *a*, where the complexity of the circuits is low.

7. CONCLUSIONS

In this paper a new coding technique for low power has been presented. It is based on an model for data bus that explicitly considers the inter-wire capacitance. It was observed that the power dissipation is no longer minimized by simply minimizing the transition activity. Depending on the technology parameters (i.e., the relative cost of inter-wire capacitance to the substrate capacitance), our proposed coding technique could save up to *40%* of the power consumed by the drivers of the lines.

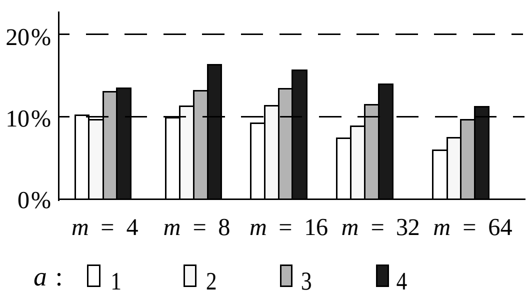

Figure 5: Power saving with $\lambda = 0$

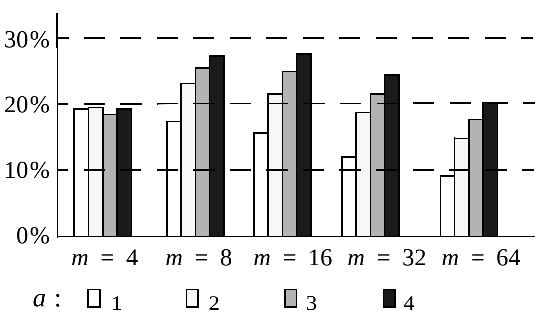

Figure 6: Power saving with $\lambda = 1$

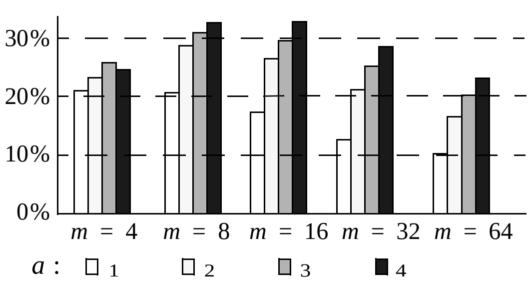

Figure 7: Power Savings with $\lambda = 2$

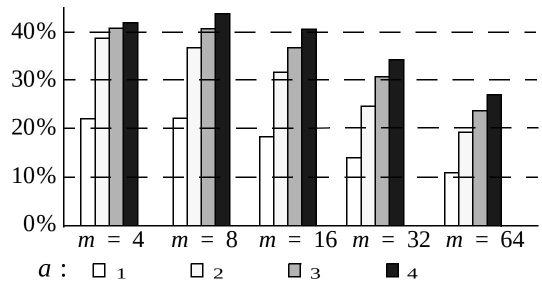

Figure 8: Power saving with $\lambda = \infty$

8. ACKNOWLEDGEMENTS

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