A Methodology for Modeling the Effects of Systematic Within-Die Interconnect and Device Variation on Circuit Performance

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Abstract: We present a methodology to study the impact of spatial pattern dependent variation on circuit performance and implement the technique in a CAD framework. We investigate the effects of interconnect CMP and poly CD device variation on interconnect delay and clock skew in both aluminum and copper interconnect technology. Our results indicate that interconnect CMP variation strongly affects interconnect delay, while poly CD variation has a large impact on clock skew in a 1 GHz design. Given this circuit impact, CAD tools in the future must account for such systematic within-die variations.

1 Introduction

Traditional statistical circuit analysis has focused mostly on random process and device variation [2,6]. However, recent studies have shown that systematic within-die (also referred to as intra-die or across chip) variation is a significant concern in high performance circuits [5,12]. For example, most of the variation resulting from chemical-mechanical polishing (CMP) of the inter-layer dielectric (ILD) is based on systematic spatial effects and varies substantially within-die [1]. If one knows the pattern dependencies, deterministic (rather than traditional random) variation models can be developed and applied to study the effects of process variation on circuit performance. Instead of using worst-case corners or monte-carlo methods to bound the variation, spatial models can be used for the systematically varying parameters, thereby reducing their uncertainty.

As technology scales, interconnect continues to play an increasingly important role. Although device delay decreases, interconnect delay increases. Accurately modeling the interconnect becomes essential for achieving maximum performance as well as ensuring that specifications are met. This is especially important for optimizing critical paths, maintaining low clock skew, and achieving acceptable crosstalk noise.

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In particular, existing parasitic RC extraction fails to account for within-die interconnect parameter variation (e.g. metal thickness, metal linewidth, and ILD thickness). Typically, interconnect technology parameters are fixed by parasitic extractors and a single fixed value is used for the ILD or metal thickness of each layer. For most efficient use of technology, circuit design in the future must account for realistic within-die interconnect and device variation.

Previous works have described methodologies for using pattern dependent variation models for interconnect RC extraction. However, [12] requires a re-extraction of interconnect parameters (capacitance and resistance) with every change in process conditions and is therefore impractical for studying the effects of different processes on large circuits. In [5], a methodology is developed to modify the original interconnect capacitance parameters, which eliminates the need for re-extraction with each process change but does not support changes in interconnect resistance or device variation effects.

In this paper, we significantly extend the previous works to allow the implementation of any type of systematic variation model based on spatial information in a CAD tool environment. We then present case studies to compare the effects of different variation sources on delay and skew, including systematic interconnect and device variation. These cases include the first reported analysis of copper CMP (erosion and dishing) variation impact on circuit performance. We show that the benefits of systematic variation models depend on the performance metric, interconnect technology, and type of circuit under consideration.

2 Interconnect Variation

To study the effects of interconnect variation, we consider the pattern dependent interconnect variation arising from CMP in both aluminum and copper interconnect technology.

2.1 Aluminum Interconnect Variation

The pattern dependent variation in Al interconnect technology results from CMP planarization of the ILD. Although CMP achieves local planarization, global non-uniformity in the ILD thickness exists across the chip. The ILD variation can be modeled as a function of the underlying metal pattern, a layout effect, as well as process factors such as the pad planarization length [8,11]. Fig. 1 shows that after CMP, dense regions have a larger final ILD thickness compared with sparse regions.

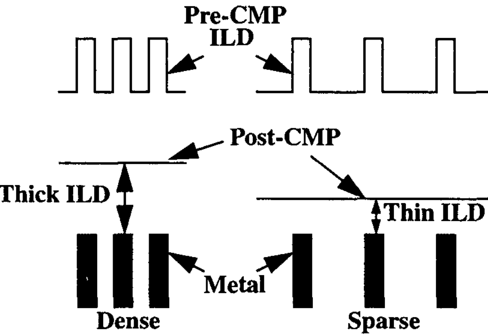

Figure 1: The effective pattern density is calculated using a moving average square window across the chip based on the pad planarization length. After CMP, dense regions are left with a larger final ILD thickness than sparse regions.

2.2 Copper Interconnect Variation

The variation mechanism discussed above is valid for oxide CMP processes, where the metal interconnect is patterned and etched before oxide deposition and CMP. Similarly, variation can be attributed to pattern dependent effects in a metal damascene CMP process. In this case, the oxide is patterned and etched, and metal is deposited followed by metal CMP. In a damascene process, the variation is in the metal wire. This causes a thickness reduction in the interconnect due to two effects known as dishing and erosion, as shown in Fig. 2.

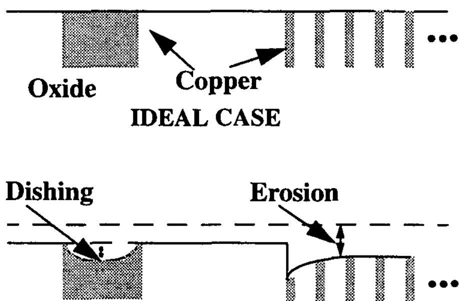

Figure 2: Wide lines experience significant metal dishing whereas fine pitch lines experience oxide erosion. Both of these effects result in metal thickness loss.

The metal thickness variation in a copper damascene CMP process can be modeled as a function of the metal pattern density, linewidth, and linespace [9,13]. Dishing is a function of linewidth and density, and erosion is a function of linespace and density. Compared to oxide (ILD) CMP, metal damascene Cu CMP is affected by relatively localized, short range interactions. In particular, pattern density variations at a distance of around $100\mu m$ can impact metal CMP, compared to the more gradual several *mm* planarization length in oxide CMP (see Fig. 3).

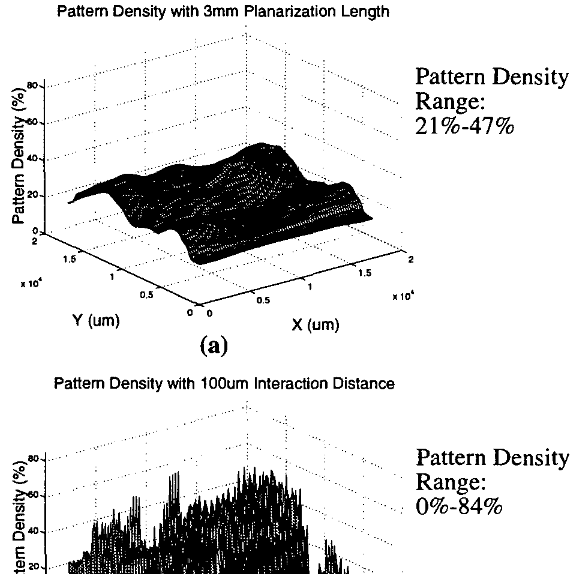

Figure 3: The $3mm$ planarization length results in a smoothly varying oxide CMP pattern density (a), but the $100\mu m$ interaction distance in Cu CMP produces a wider range of density (b).

3 Assessment Methodology

Our methodology for assessing the impact of pattern dependent variation is shown in Fig. 4. We first extract the nominal device and interconnect parameters using the layout and connectivity information for the circuit. In addition to the electrical nodes and the nominal parameter values, information about the coordinates (x,y) and geometry (length,width) is also output during the extraction, allowing us to use spatial variation models. An advantage of this approach is that circuit parameters do not need to be re-extracted with every change in process conditions, enabling a quick first pass prediction.

The variation analysis tool perturbs the extracted interconnect RC and any pattern dependent device parameters using spatial information. The interconnect (and device) geometry variation is calculated based on the pre-computed pattern density, linewidth, and linespace to the nearest neighbors (e.g. using models described in Section 2). Electrical parameter variations are computed next, and closed form expressions are used to calculate the interconnect capacitance variation [10]. Net input/output information is added to form a Spice netlist and simulate the signal delays. Critical nets at or near the target specifications may be fine tuned subsequently using a full 3D capacitance solver. Although we specifically deal with pattern dependent intra-die variation, other systematic variation effects can be easily incorporated into our methodology. Random variations can then be considered separately using conventional statistical analysis techniques.

Procedure to implement systematic variation models in a CAD tool and automate performance impact assessment:

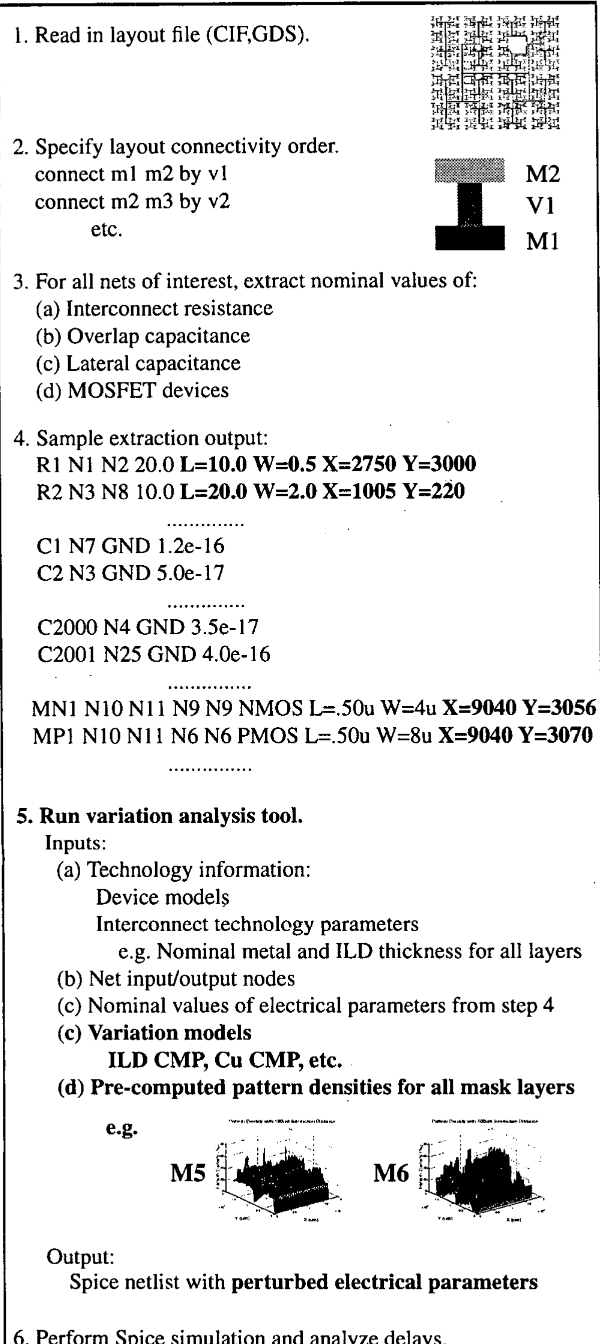

Figure 4: CAD tool implementation of the methodology used to study the effects of pattern dependent variation. Information in **bold** is used to incorporate variation effects.

4 Case Studies

Through two case studies, we demonstrate that circuit type, performance metrics, and technology determine the relative importance of the various systematic variation models.

4.1 Interconnect Delay

The delay of long interconnect lines is simulated to model the effects of CMP variation on bus lines. Since Cu CMP interconnect variation is affected by short range interactions, an array of bus lines (see Fig. 2) will be subject to varying amounts of erosion based on bit position within the array, affecting both the interconnect resistance and capacitance. Al interconnect will not experience different variation effects based on bit position since ILD variation depends on long range interactions.

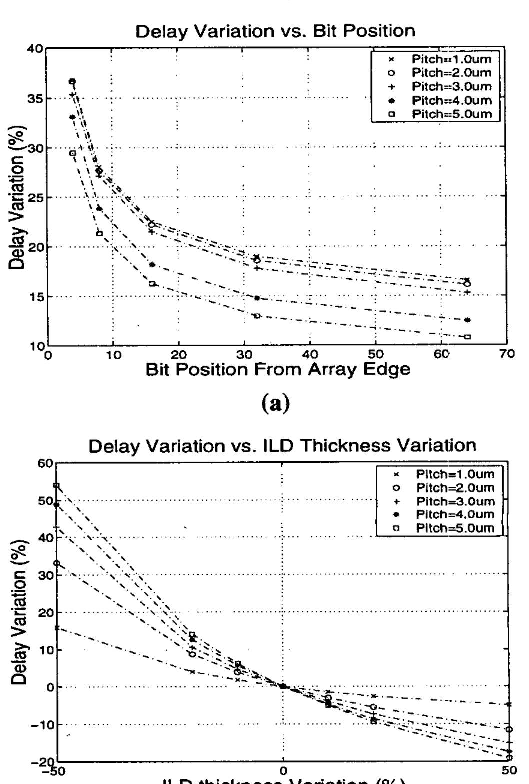

Figure 5: The simulated percentage delay variation for *5mm* interconnect (bus lines) with Cu CMP (a) and oxide CMP (b) variation based on pattern dependent models.

Delay variation for *5mm* lines at various pitch in both Al and Cu interconnect (0.60 μm metal and ILD thickness) is shown in Fig. 5. The Cu interconnect variation is modeled assuming that there is blanket oxide surrounding a large array of interconnect lines. Since the erosion is a function of bit position within the array, delay variation exists across the bus. The Al interconnect variation is modeled as a function of the average ILD thickness along the net. For high underlying pattern density, the delay may

actually be less than the nominal with oxide CMP. Comparing the two technologies, the percentage delay variation due to CMP is greatest for minimum pitch lines with Cu interconnect, but with Al interconnect the widest pitch lines experience the largest percentage delay variation. This is due to the fact that lateral coupling capacitance (and resistance) are most affected with Cu CMP, whereas overlap capacitance is affected most with oxide CMP. The maximum delay variation with Cu CMP is 64ps vs. 43ps with oxide CMP over the range of parameters considered in our study.

4.2 Clock Skew

For our second case study, we analyze the effects of pattern dependent interconnect and device variation on clock skew. Fig. 6 shows a clock tree used in clock distribution of a high speed microprocessor [3]. The circuit is designed in a $0.25\mu m$ technology using copper interconnect and is placed on the top 2 metal levels in this 6 level metal process. The clock distribution circuit is an almost symmetric H-tree, so the skew without any process variation should be small. The tree is driven by a series of cascaded drivers at the root and is loaded with latches at the tips.

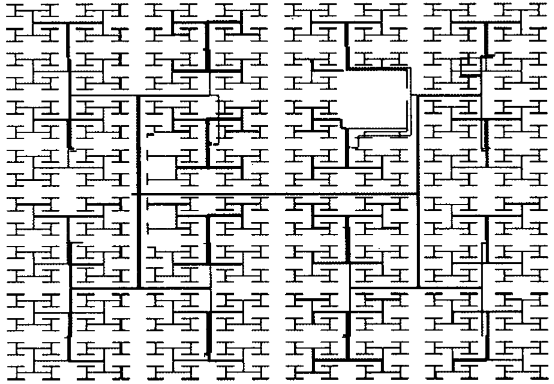

Figure 6: H-tree used to simulate the effects of interconnect and device variation on clock skew.

We analyze the effects of metal thickness variation resulting from Cu CMP in the interconnect and pattern dependent polysilicon gate length variation in the devices. Additionally, we compare the clock skews assuming that an Al interconnect with oxide CMP process is used instead.

To model the poly critical dimension (CD) variation, we assume that a pattern (density and pitch) dependent model captures the systematic variation [4]. Although optical proximity correction (OPC) is often used in correcting the lithography component of the linewidth variation, pattern dependent effects such as those due to etch microloading can still produce a systematic offset in the as-designed linewidth of up to 10% in aggressive technologies. As a conservative bound on poly CD variation, we vary the gate length on the devices at the latches by as much as 5% of the nominal. We consider a case where the underlying poly density varies in large areas on the chip (e.g. dense SRAM, random logic) and divide the chip into four quadrants, with all devices in a given quadrant experiencing a fixed percentage of poly CD variation (between 0% and 5%). Other models for device variation are possible, such as those capturing the trends across the entire chip (e.g. a poly CD "gradient" from one side of the chip to the other) [7].

Spice simulations are performed to obtain the clock skews for the various cases and summarized in Table I. The results show that most of the clock skew is due to the asymmetry of the H tree, even when interconnect CMP variation is included. The skew increases by less than 10ps with pattern dependent interconnect variation compared to almost a 50ps increase with device variation.

Table I: Maximum Clock Skew

Interconnect	Variation Source	Max Skew (ps)
Cu	None (nominal metal thick.)	34
Cu	Metal Thickness (Dishing+Erosion)	40
Al	None (nominal ILD)	59
Al	Pattern Dependent ILD	62
Cu	Poly CD (0-5% by quad.)	83

5 Results Summary

A methodology to study the effects of pattern dependent variation on circuit performance has been described. Systematic within-die variation models need to be taken into account for accurate delay simulations in high performance designs. Our results show that interconnect CMP variation can increase bus delay by more than 30%, even in Cu interconnect technology. Although clock skew is not strongly impacted by interconnect CMP variation in our case study, device gate length variation can significantly alter the path delays with an increase in the maximum skew of about 50ps. Future work will consider how systematic and random variation in interconnect and devices will impact critical circuits as a function of technology scaling and layout or design rule practices.

Acknowledgments

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