

## SOIAS: Dynamically Variable Threshold SOI with Active Substrate

Carlin Vieri, Isabel Yang, Anantha Chandrakasan, and Dimitri Antoniadis  
Massachusetts Institute of Technology, Cambridge, MA 02139

### Introduction

As supply voltages are scaled to reduce energy dissipation in integrated circuit devices, threshold voltages ( $V_t$ ) are scaled to maintain performance. In fixed throughput applications the dynamic power is usually much higher than the leakage power, and the increased subthreshold current of a low  $V_t$  is generally acceptable. But in event-driven microprocessor based application, circuits have long idle times, and the leakage power may become a significant percentage of total chip power. This paper describes a low voltage, silicon on insulator, active substrate (SOIAS) technology which addresses the problems of increased leakage currents in high performance, low voltage circuits. The threshold voltage is dynamically variable through the application of a voltage to an insulated back gate[2] for high performance and low leakage.

### SOIAS Technology

The merits of conventional, fully depleted CMOS circuits on a silicon on insulator substrate (SOI), such as near ideal subthreshold slope at low threshold voltages and low junction capacitance with a simple isolation scheme, have qualified this technology as a promising candidate for low power systems. To further exploit the advantages of fully depleted SOI for ultra-low power and high performance applications, we propose a new technology, SOI on active substrate (SOIAS).

A back gate is formed by burying a conductive layer of polysilicon under the buried oxide of an SOI CMOS device and contacting the back gate from above. Figure 1 shows the cross section of device structure. The back gate dy-

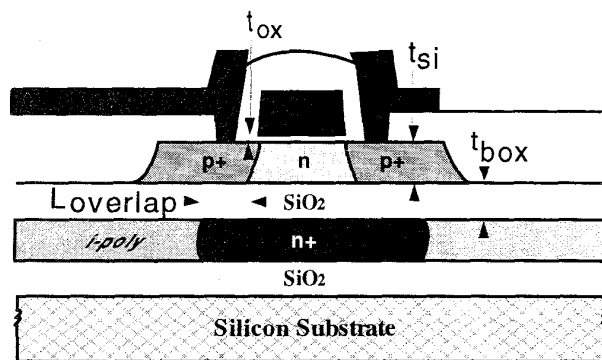


Figure 1: Cross section of a SOIAS NMOS device

namically controls the threshold voltage of the normal transistor above. Leakage power and on-currents are controlled by lowering  $V_t$  when a circuit is active and raising  $V_t$  when the circuit is idle. This addresses the opposing requirements of high performance and low power, particularly at low power supply voltages (e.g. 1.5V or less).

### Geometry Optimization

In fully depleted SOI devices, the surface potentials at the top and bottom interfaces of the silicon film are coupled. The top transistor  $V_t$  is modulated by changing the back interface surface potential (applying a voltage to the back gate). The relationship[1] between the top transistor  $V_t$  and the back gate bias is linear; the slope is approximately  $C_b C_{box} / C_{ox} (C_b + C_{box})$  where  $C_b$  is  $\epsilon_{si} / t_{si}$ ,  $C_{box}$  is  $\epsilon_{ox} / t_{box}$ , and  $C_{ox}$  is  $\epsilon_{ox} / t_{ox}$ . To achieve the maximum  $V_t$  swing ( $\Delta V_t$ ) with the minimum amount of back gate bias,  $t_{si}$  and  $t_{box}$  must be small and  $t_{ox}$  must be large. Changing the geometry of these features involves a series of trade-offs. Thinning the silicon film will increase the series resistance. Even when a thin silicide is used, the lower limit of the silicon film thickness at which reliable thin silicide can be obtained is about 40nm. Thinning the back gate oxide increases the node capacitance due to the overlap of the bottom gate with the source/drain regions, and making the front gate oxide thick reduces drive current.

We begin with a standard SOI technology with a minimum channel length of  $0.2\mu\text{m}$  and a drawn length of approximately  $0.25\mu\text{m}$ . The typical  $t_{ox}$  for such a technology is  $70\text{\AA}$ . Furthermore, the low  $V_t$  is constrained to be 200mV for adequate noise margin, and  $\Delta V_t$  must be at least 200mV for acceptable change in leakage current; i.e. the high threshold voltage is 400mV, resulting in a three decade reduction in the off current when switching from low to high  $V_t$ . Figure 2 is a plot of the energy to switch the front gate, a constant  $C_{ox} V_{dd}^2$ , and the back

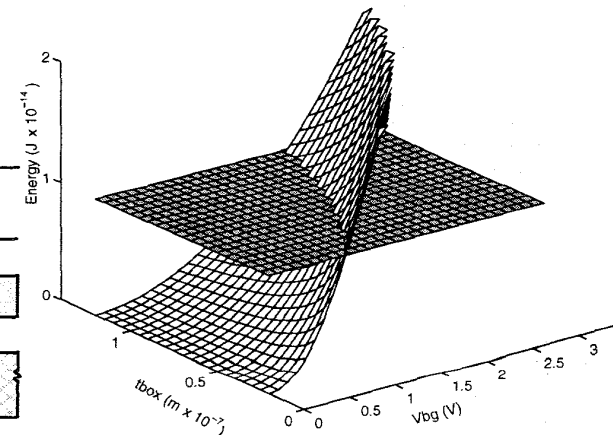


Figure 2: Front and back gate switching energies

gate switching energy as a function of  $V_{bg}$  and  $t_{box}$ . The plot of back gate switching energy has been truncated at  $2 \times 10^{-14}$  J.

With all standard process parameters fixed by performance and fabrication requirements, SOIAS provides two new "knobs" for control of leakage energy: back gate ox-

ide thickness and back gate voltage<sup>1</sup>  $V_{bg}$ . A thinner back gate oxide results in a greater  $\Delta V_t$  but increases back gate capacitance and the overlap coupling capacitance to the source/drain regions, which increases node capacitance as mentioned above. A larger  $V_{bg}$  also increases  $\Delta V_t$  but increases back gate switching energy,  $C_{box} V_{bg}^2$ , quadratically.

The energy cost to switch the back gate is minimized by reducing  $V_{bg}$  and  $t_{box}$  (i.e. achieving the specified  $\Delta V_t$  with a low  $V_{bg}$  and a high  $C_{box}$  since energy is linear in  $C$  and quadratic in  $V$ ) until parasitic capacitance from overlap with source/drain regions and the resulting increase in front gate switching energy becomes large. Under these constraints, minimum energy is achieved at  $V_{bg}$  of 2.3V and a  $t_{box}$  of 600Å.

### Energy Reduction over Conventional SOI

Once all the process parameters have been optimized, we can compare the equations for total energy in a standard SOI process and in a SOIAS process. Our mode of operation will be to “turn on” a functional module of a microprocessor by lowering its  $V_t$  when that module is needed. Examples of functional modules are adders, shifters, and multiply blocks. For this discussion a functional module will be the smallest unit with an independently controllable  $V_t$ . We will discuss probabilities of usage assuming a large number of cycles and randomly occurring instructions. This second assumption may not always be true, but it will suffice for this discussion.

The module will be turned on with some probability  $\alpha$  which we model as a two state Markov process. The back gate for this module’s transistors is switched with probability  $\beta$ , which is always less than  $\alpha$  because the back gate only switches once for a run of uses of the module. For example, if a shifter is used three times in a row in ten clock cycles,  $\alpha = 30\%$  and  $\beta = 10\%$ .

More formally, in steady state operation, if a module is being used (high  $V_t$ ), there is a probability  $\alpha$  that it will stay in that state and probability  $1-\alpha$  that it will change state (be turned off). If it is not being used, the probabilities are  $1-\alpha$  and  $\alpha$  to stay off and be turned on, respectively. To find  $\beta$  we are interested in the transition probabilities. Let  $P_{on}$  and  $P_{off}$  be the probabilities for the module being on or off, respectively. Then

$$\begin{aligned} P_{on}(1-\alpha) &= P_{off}(\alpha) \\ P_{on} + P_{off} &= 1 \\ P_{on}(1-\alpha) + P_{off}(\alpha) &= P_{sw} \end{aligned}$$

where  $P_{sw}$  is the probability that the module is switched<sup>2</sup> and is equal to  $2 \times \beta$ . Solving these equations we find that  $\beta = \alpha - \alpha^2$ . We also have a parameter  $\gamma$  which represents the switching probability of an individual transistor front gate in the module, and we assume  $\gamma = 25\%$  (in general, it is a strong function of bit transition probabilities).

The total energy dissipated in a functional module of a microprocessor during one clock cycle (period =  $t_{cyc}$ ) may now be described by the following equations. The

<sup>1</sup>By  $V_{bg}$  we mean the back gate switching voltage such that the back gate swings between zero and  $V_{bg}$  just as the front gate swings between zero and  $V_{dd}$ .

<sup>2</sup>Switching the back gate in this context is a transition from low to high to low  $V_{bg}$

first equation is for a reference SOI process with a fixed  $V_t$ , and therefore always has a high leakage component. In the second equation the total energy is composed of the front gate switching energy, the back gate switching energy, and the leakage energy for both high and low  $V_t$ . The low  $V_t$  leakage term is small even for small  $\alpha$ .

$$\begin{aligned} E_{SOI} &= \alpha\gamma C_{fg} V_{dd}^2 + IV_{dd} t_{cyc} \\ E_{SOIAS} &= \alpha\gamma C_{fg} V_{dd}^2 + \beta C_{bg} V_{bg}^2 + \alpha IV_{dd} t_{cyc} + \\ &\quad (1-\alpha) I_0 V_{dd} t_{cyc} \end{aligned}$$

Again assuming that the process parameters have been fixed the energy is determined by the algorithmic variables,  $\alpha$ ,  $\beta$ , and  $\gamma$ . At low values of  $\alpha$  the energy overhead of switching the back gate is larger than the energy saved from reduced leakage currents and SOIAS is not appropriate.

We profiled a series of programs on a typical RISC microprocessor to measure values of  $\alpha$  for three functional units: the ALU adder, the shifter, and the multiplier. Figure 3 is a contour plot of the ratio of the total energy of a benchmark SOI process and the SOIAS process

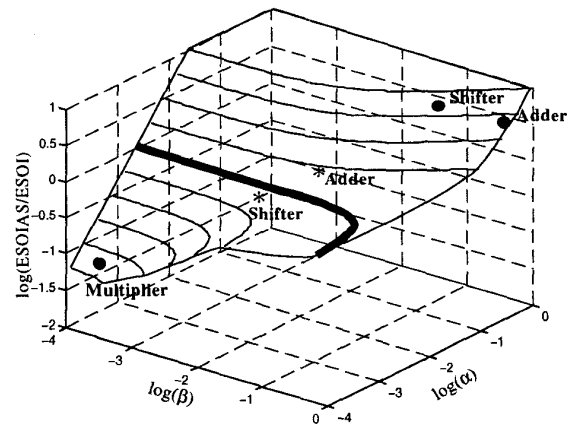


Figure 3: SOI vs. SOIAS Energy Ratio Contour Plot

for these measured values of  $\alpha$  and calculated values of  $\beta$ . The solid circles represent the functional block usage when the processor is continuously active. The stars are measured values under worst case event-driven conditions when the processor spends cycles waiting for user I/O. As the number of wait cycles increases, SOIAS becomes more appropriate. Both technologies have the same performance (front gate switching speed). Data points below the dark zero contour, i.e. values of  $\alpha$  below about 2%, show an energy reduction using SOIAS. The system designer must determine some typical  $\alpha$  and  $\beta$  values based on the system’s intended use and can then see if SOIAS is appropriate by where the modules fall on the graph of Figure 3.

### References

- [1] H.Y. Lim and J. G. Fossum. Threshold voltage of thin-film silicon-on-insulator (SOI) MOSFET’s. *Transaction on Electron Devices*, ED-30(10):1244, October 1983.
- [2] T. Tanaka et al. Analysis of p<sup>+</sup> poly Si double-gate thin-film SOI MOSFET’s. *IEDM Digest*, 1991.