

Wafer Nanotopography Effects on CMP: Experimental Validation of Modeling Methods

Brian Lee¹, Duane S. Boning¹, Winthrop Baylies², Noel Poduje³, Pat Hester³, Yong Xia³, John Valley⁴, Chris Koliopoulos⁴, Dale Hetherington⁵, HongJiang Sun⁶, Michael Lacy⁷

¹Massachusetts Institute of Technology, Cambridge MA

²BayTech Group, Weston MA

³ADE Corporation, Westwood MA

⁴ADE Phase-Shift, Tucson AZ

⁵Sandia National Laboratories, Albuquerque NM

⁶Philips Semiconductor, Albuquerque NM

⁷Lam Research, Fremont CA

ABSTRACT

Nanotopography refers to 10-100 nm surface height variations that exist on a lateral millimeter length scale on unpatterned silicon wafers. Chemical mechanical polishing (CMP) of deposited or grown films (e.g., oxide or nitride) on such wafers can generate undesirable film thinning which can be of substantial concern in shallow trench isolation (STI) manufacturability. Proper simulation of the effect of nanotopography on post-CMP film thickness is needed to help in the measurement, analysis, diagnosis, and correction of potential problems.

Our previous work has focused on modeling approaches that seek to capture the thinning and post-CMP film thickness variation that results from nanotopography, using different modeling approaches. The importance of relative length scale of the CMP process used (planarization length) to the length scale of the nanotopography on the wafer (nanotopography length) has been suggested.

In this work, we report on extensive experiments using sets of 200 mm epi wafers with a variety of nanotopography signatures (i.e., different nanotopography lengths), and CMP processes of various planarization lengths. Experimental results indicate a clear relationship between the relative scales of planarization length and nanotopography length: when the planarization length is less than the nanotopography length, little thinning occurs; when the CMP process has a larger planarization length, surface height variations are transferred into thin film thickness variations. In addition to presenting these experimental results, modeling of the nanotopography effect on dielectric CMP processes is reviewed, and measurement data from the experiments are compared to model predictions. Results show a good correlation between the model prediction and the experimental data.

INTRODUCTION

Nanotopography (height variations of 20 to 80 nm that exists over lateral distances of several millimeters) on unpatterned silicon wafers is becoming a serious issue in IC fabrication [1]. One principal concern is the interaction of nanotopography with long planarization length CMP processes that creates undesired thinning of surface films, which may lead to yield concerns in shallow trench isolation processing [6].

This work reports on the results of a set of experiments performed on 200mm epi wafers, which are divided into wafer types that exhibit distinct and identifiable nanotopography characteristics. Wafer sets, consisting of samples of each wafer type, are run on a variety of CMP proc-

esses, in which the tool, pad, and process conditions re changed. Emphasis is placed not on the specific tool, pad, or process conditions; instead, the focus is to experiment using CMP processes of varying planarization lengths.

This work also reports on an implementation of a model that can be used to predict the effect on wafer nanotopography on the CMP processing of films deposited over such wafers. This previously published model [4,5] is based on contact mechanics between the wafer and the pad, and is useful for the simulation of the CMP of large-scale structures, and thus is useful for modeling of wafer nanotopography impact on CMP. Results of the contact mechanics simulation, and comparison of the results to data measured from the post-CMP experiment wafers is given. Finally, future goals of this research are discussed.

DISCUSSION

The fundamental hypothesis here is that the interaction of the lateral length scale of the wafer nanotopography (called the nanotopography length, or NL) with the CMP process planarization length (or PL) propagates into the surface film thickness. Specifically, when the planarization length exceeds the nanotopography length (e.g., in CMP processes using stiff pads), the surface film thins in certain areas with respect to other areas.

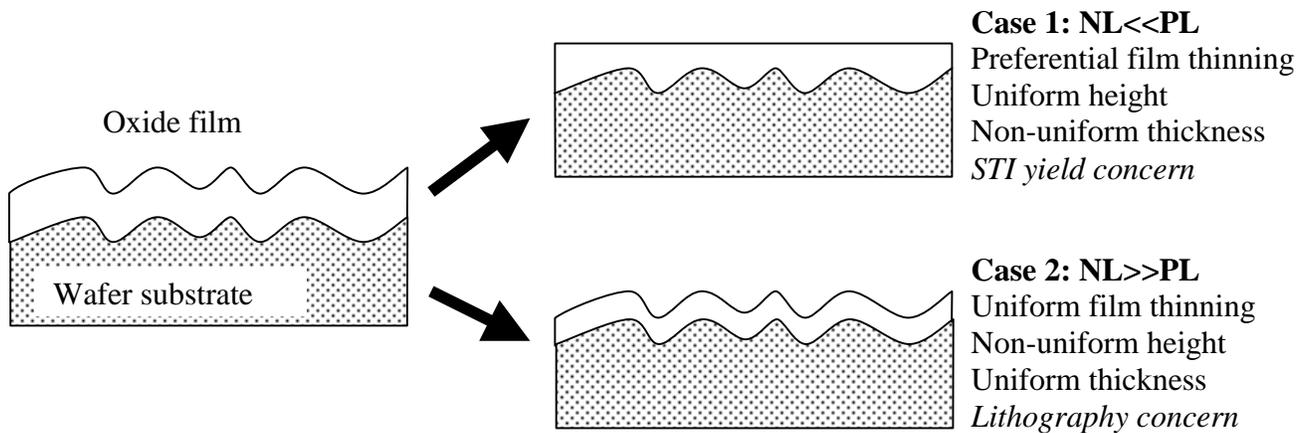


Figure 1. The importance of relative length scales in nanotopography and CMP

To model the CMP process acting on nanotopography, we consider a contact mechanics approach, based on the interaction of the pad and wafer. Contact wear CMP models, developed previously by Chekina [4] and Yoshida [5], are implemented for simulation here. The underlying concept of the contact wear model is to relate local pressures on the pad and wafer with displacement of the pad, assuming the pad behaves as an elastic material. The pressure-displacement equation is expressed in matrix form and used in a BEM method to iterate over time and simulate the CMP process.

The pressure-displacement equation, in two-dimensional form, is:

$$w(x, y) = \frac{(1 - \nu^2)}{\pi E} \iint_A \frac{p(\xi, \eta)}{[(x - \xi)^2 + (y - \eta)^2]^{\frac{1}{2}}} d\xi d\eta \quad (\text{Equation 1})$$

where ν is Poisson's ratio, E is Young's modulus, and A is the area of simulation.

The pressure-displacement equation is used to compute pad pressure p and pad displacement w at every point on the wafer surface. The calculated pressures, in turn, are used with Preston's classic glass polishing equation to calculate local removal rates:

$$RR(x, y) = K * V * p(x, y) \quad (\text{Equation 2})$$

where K is Preston's coefficient, V is velocity, $p(x,y)$ is the pressure at point (x,y) , and $RR(x,y)$ is the local removal rate at point (x,y) . The removal rates are then used to advance the film surface polish evolution over time, until the final polish time is achieved.

The contact mechanics approach is useful for modeling CMP of nanotopography since the input to the model is the initial surface height profile. While previous modeling efforts to predict the film thinning effect used an approximation of the surface nanotopography (using a fixed grid of randomly sized cylindrical structures) [6], the work here utilizes the actual measured nanotopography data and predicts forward the oxide thickness removed due to a CMP process, and compares it to actual oxide thickness removed data (measured pre-CMP thickness data minus measured post-CMP thickness data).

EXPERIMENTAL DETAILS

The starting wafers are 200 mm epi wafers, on which a 1 micron thermal oxide is grown. Four different nanotopography wafer types are reported here: one double-sided polish (labeled DSP1) and three single-sided polish (labeled SSP1, SSP2, and SSP3). Image maps illustrating the height variation of each nanotopography type are shown in Figure 2, produced using the Nanomapper™ with a 20mm double gaussian filter.

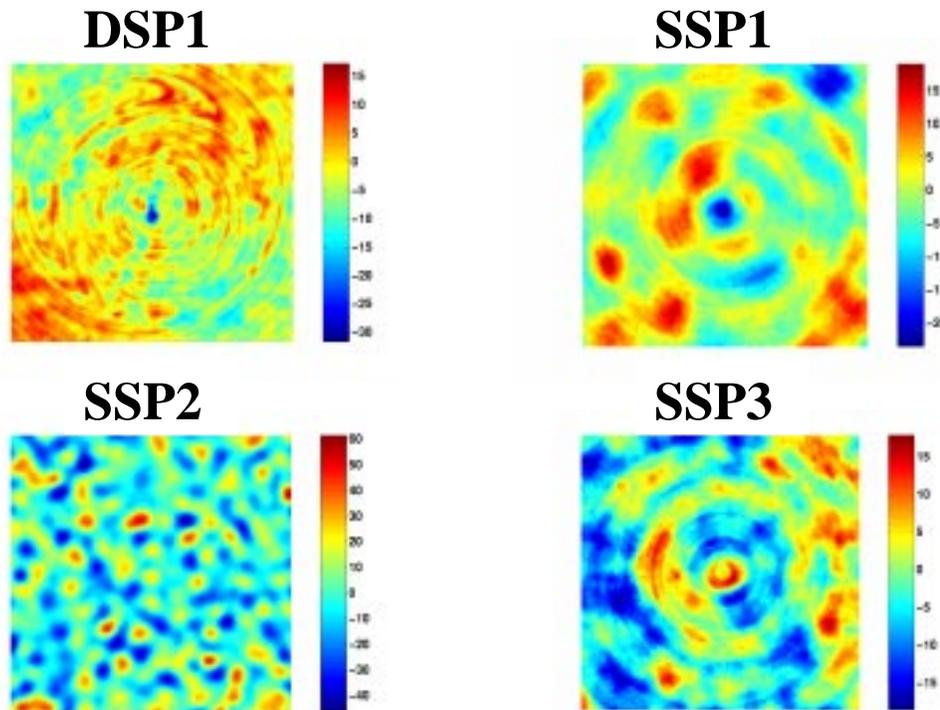


Figure 2. Image maps of the four nanotopography wafer types

Eight combinations of CMP pad/process/tool polishes are performed. These process combinations are labeled Processes A-H in this paper. The intent is to cover a range of CMP processes with different planarization lengths. Each combination is considered a separate process split and is applied to several replicates of each of the nanotopography wafer types. For each process split, patterned CMP characterization wafers are also polished, and measurements from these wafers are used to determine the planarization length of that specific process split.

Extensive measurements of starting wafer height, pre-CMP oxide thickness, and post-CMP oxide thickness are gathered. The full wafer is measured in all cases, but to eliminate edge effects in the analysis, only the central 100mm x 100mm region is used.

EXPERIMENTAL RESULTS

Using measurement data from test pattern wafers included in each process, planarization lengths are calculated using the methodology described in [3]. The extracted planarization lengths cover a large range, as shown in Table 1.

Table 1. CMP Processes: Extracted Planarization Lengths

Process	Planarization Length
A	8.4 mm
B	3.4 mm
C	1.9 mm
D	3.1 mm
E	4.6 mm
F	9.7 mm
G	6.4 mm
H	13.7 mm

Initial wafer nanotopography height measurement data is compared to oxide thickness removed (pre-CMP oxide thickness minus post-CMP oxide thickness) data for the central 100mm x 100mm region of each of the four types of wafers. In comparing the two datasets, two characteristics are studied (as shown in Figure 3): the similarity between the shapes of the two datasets, and the degree of magnitude of the height transmission from the nanotopography to the oxide thickness removed. To that end, two metrics were calculated: the correlation coefficient (similarity of “shape”) and the ratio of standard deviation of the oxide removed to the standard deviation of the nanotopography height. Both metrics are important in measuring the impact of thinning of the surface film due to the CMP process. The nanotopography and oxide thickness removed data are interpolated onto a common grid spacing, so that the correlation coefficient c can be computed, using the following formula:

$$c = \frac{\sum_i \sum_j \left(N_{ij} - \mu_N \right) \left(O_{ij} - \mu_O \right)}{\sigma_N \sigma_O} \quad (\text{Equation 3})$$

where N is the nanotopography height, O is the oxide thickness, and σ is the standard deviation. The standard deviation ratio gives a metric for the absolute magnitude of height propagated

from the nanotopography to the amount of oxide removed due to the CMP process. Both nanotopography and oxide removed data maps are first filtered with a 30mm double gaussian to remove wafer-scale trends, in order to focus on the transmitted nanotopography shape and height metrics. Calculated correlation coefficients and standard deviation ratios are shown in Table 2 and Table 3.

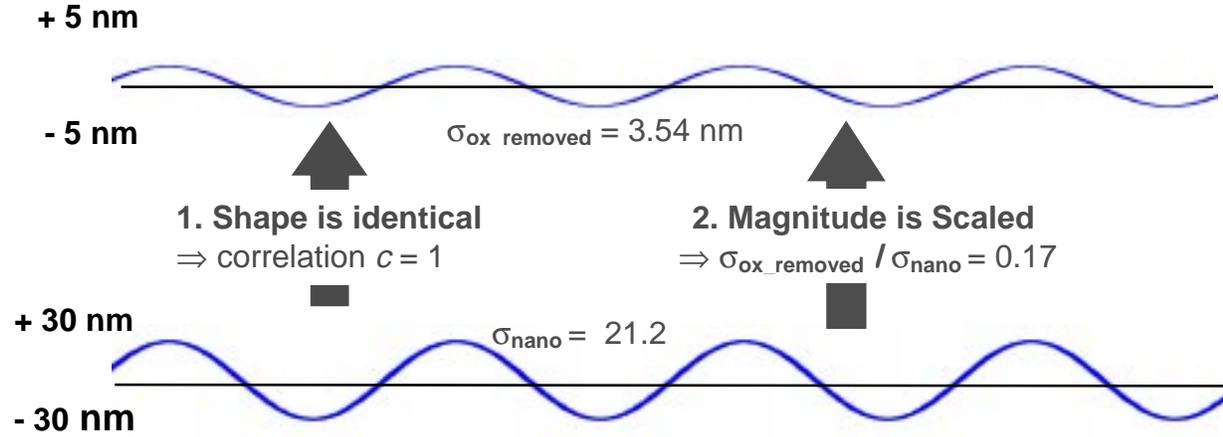


Figure 3. Illustration of metrics for nanotopography propagation

Table 2. Transmitted Shape: Correlation Coefficient Results, Nanotopography Height to Oxide Thickness Removed Comparison

Process	Planarization Length	DSP1 Corr. Coeff.	SSP1 Corr. Coeff.	SSP2 Corr. Coeff.	SSP3 Corr. Coeff.
C	1.9 mm	0.12	0.17	0.52	0.13
D	3.1 mm	0.14	0.25	0.51	0.17
B	3.4 mm	0.24	0.14	0.75	0.34
E	4.6 mm	0.06	0.12	0.40	0.14
G	6.4 mm	0.66	0.64	0.81	0.70
A	8.4 mm	0.35	0.56	0.84	0.59
F	9.7 mm	0.81	0.94	0.89	0.88
H	13.7 mm	0.54	0.65	0.88	0.60

Table 3. Transmitted Height: Standard Deviation Ratio Results, Nanotopography Height to Oxide Thickness Removed Comparison

Process	Planarization Length	DSP1 $\sigma_{ox}/\sigma_{nano}$	SSP1 $\sigma_{ox}/\sigma_{nano}$	SSP2 $\sigma_{ox}/\sigma_{nano}$	SSP3 $\sigma_{ox}/\sigma_{nano}$
C	1.9 mm	0.33 (1.1/3.4)	0.30 (1.1/3.7)	0.07 (1.2/16)	0.30 (1.0/3.5)
D	3.1 mm	0.82 (2.7/3.3)	0.69 (2.6/3.8)	0.18 (2.9/16)	0.77 (2.7/3.5)
B	3.4 mm	0.47 (1.7/3.6)	0.33 (1.2/3.5)	0.14 (1.9/14)	0.38 (1.3/3.4)
E	4.6 mm	1.33 (4.6/3.4)	1.05 (4.3/4.0)	0.29 (4.3/15)	1.01 (3.8/3.7)
G	6.4 mm	0.57 (1.7/3.1)	0.32 (1.1/3.5)	0.31 (4.4/14)	0.37 (1.4/3.9)
A	8.4 mm	1.22 (4.3/3.5)	1.26 (4.2/3.3)	0.67 (9.5/14)	1.27 (4.7/3.7)
F	9.7 mm	0.88 (3.1/3.5)	0.98 (3.3/3.3)	0.75 (11/15)	0.83 (3.0/3.6)
H	13.7 mm	0.98 (3.7/3.8)	1.14 (3.9/3.4)	0.76 (12/16)	1.23 (4.2/3.4)

The contact mechanics model is used to simulate the central 50mm x 50mm region of the wafer, with a surface discretization of 1mm x 1mm cells. Two scenarios are simulated in this work: an SSP2 wafer run on Process A (planarization length 8.4 mm) and an SSP2 wafer run on Process B (planarization length 3.4 mm). SSP2 wafers are chosen because they exhibit the largest height variation and shortest lateral variation wavelength (see Figure 2). In comparing the simulation to the measured data, the amount of film removed during the CMP process is used. Correlation coefficient and standard deviation values are computed as the metrics of comparison. Results are shown in Table 4, and demonstrate that the model provides a good estimator of the shape and magnitude of the measured data.

Table 4. Comparison Metrics for Amount of Removed Material (Model to Data)

	Process A	Process B
Correlation Coefficient	0.92	0.82
Standard Deviation, Model	9.7 nm	1.62 nm
Standard Deviation, Data	9.6 nm	1.88 nm

CONCLUSIONS

Experiments using wafers with distinct nanotopography signatures in combination with CMP processes with distinct planarization lengths have been conducted. Results from this experiment agree with our hypothesis that substantial film thinning occurs when the CMP planarization length is larger than the nanotopography length. A contact-mechanics based model is successful in predicting the CMP film removal on wafers with nanotopography, and compared results of the simulation versus measured data. Future work involves analyzing the impact of the CMP film thinning effect due to nanotopography with regard to yield concerns in STI due to nitride thinning and incomplete oxide clearing. Such work involves incorporation of the nanotopography CMP model into a pattern-based STI model, which could be used for diagnosis of potential yield problems.

ACKNOWLEDGMENTS

The authors would like to thank MEMC and SKW Associates, Inc. for supplying wafers for use in this experiment.

REFERENCES

1. S. Xu, "Effects of Silicon Front Surface Topography on Silicon Oxide Chemical Mechanical Planarization," *Electrochemical and Solid State Letters*, vol. 1, no. 4, pp. 181-182, 1998.
2. K.V. Ravi, "Wafer Flatness Requirements for Future Technologies," *Future Fab International*, no. 7, pp. 207.
3. D. Ouma, Modeling of Chemical Mechanical Polishing for Dielectric Planarization, *Ph.D Thesis*, MIT, Nov. 1998.
4. O. G. Chekina and L.M. Keer, "Wear-contact problems and modeling of chemical mechanical polishing," *J. Elec. Soc.*, vol. 145, no. 6, pp. 2100-2106, Jun. 1998.
5. T. Yoshida, "Three-dimensional chemical mechanical polishing process mode by BEM," *ECS Conf.*, Oct. 1999.
6. B. Lee, T. Gan, D. Boning, P. Hester, N. Poduje, W. Baylies, "Nanotopography Effects on Chemical Mechanical Polishing for Shallow Trench Isolation," *Advanced Semiconductor Manufacturing Conference*, Sept. 2000, pp. 425-432.