# **Electronic Devices**

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# Subthreshold Swing Improvement in MoS<sub>2</sub> Transistors by the Negative-Capacitance Effect

A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, T. Palacios Sponsorship: ONR PECASE, ARO, NSF

Obtaining a subthreshold swing (SS) below the thermionic limit of 60 mV/dec by exploiting the negative-capacitance (NC) effect in ferroelectric (FE) materials is a novel effective technique to allow the reduction of the supply voltage and power consumption in field-effect transistors (FETs). At the same time, two-dimensional layered semiconductors, such as molybdenum disulfide (MoS<sub>2</sub>), have been shown to be promising candidates to replace silicon MOSFETs in sub-5-nm-channel technology nodes. In this work, we demonstrate NC-MoS<sub>2</sub> FETs by incorporating a ferroelectric Al-doped HfO<sub>2</sub> (Al:HfO<sub>2</sub>), a technologically compatible material, in the FET gate stack. Al:HfO<sub>2</sub> thin films were deposited on p<sup>+</sup>Si wafers by atomic layer deposition. X-ray photoelectron spectroscopy (XPS) analysis was performed on the Al:HfO<sub>2</sub> films after varying the cycle ratio of Al and

Hf precursors (Figure 1 a–c). The linear fit with near unity slope shows that the Al content can be precisely controlled in the range 0%–16.7%. Moreover, the X-ray diffraction (XRD) analysis suggests a phase transition from the monoclinic phase to the orthorhombic phase upon doping. This noncentrosymmetric transition phase is a prerequisite for ferroelectric characteristics. (Figure 1d). Voltage amplification up to 1.25 times was observed in a FE bilayer stack of Al:HfO<sub>2</sub>/HfO<sub>2</sub> with Ni metallic intermediate layer. The NC-MoS<sub>2</sub> FET built on the FE bilayer showed a significant enhancement of the SS to 57 mV/dec, compared with SS<sub>min</sub> = 67 mV/dec for the MoS<sub>2</sub> FET with only HfO<sub>2</sub> as a gate dielectric. The absence of hysteresis showed the effective stabilization of the NC by using the HfO<sub>2</sub>/Al:HfO<sub>2</sub> bilayer.



▲ Figure 1: (a & b) XPS analysis of AI-doped  $HFO_2$  films with different AI contents deposited on Si wafers with TMA/ TEMAH cycle ratios ranging from 0 to 16.7%, (c) AI content of the AI: $HFO_2$  films extracted from the XPS spectra shown in (a) and (b) as a function of the TMA/TEMAH cycle ratio, (d) XRD patterns of undoped and 7.3% AI-doped  $HFO_2$ .



▲ Figure 2: Schematic of the NC-MoS<sub>2</sub> FET with a HfO<sub>2</sub>/ Al:HfO<sub>2</sub> bilayer stack with Ni used as the intermediate metal, (b) schematic of a reference regular MoS<sub>2</sub> FET with a HfO<sub>2</sub> gate dielectric. In both (a) and (b), a highly doped Si wafer is used as the back gate, (c) transfer characteristics and transconductance of the NC-MoS<sub>2</sub> FET and reference MoS<sub>2</sub> FET at room temperature, (d) comparison of the SS of the NC-MoS<sub>2</sub> FET with that of the reference MoS<sub>2</sub> FET.

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## Frequency Response of Graphene Electrolyte-Gated Field-Effect Transistors (EGFETs)

C. Mackin, E. McVay, T. Palacios Sponsorship: ISN

Graphene consists of an atomically thin layer of sp<sup>2</sup>-bonded carbon atom arranged in a hexagonal lattice. Graphene exhibits a number of promising electrical, optical, mechanical, and chemical properties making it well suited for a range of chemical and biological sensing applications. Graphene is chemically stable and does not form a native oxide, which enables a direct interface with many chemical and biological environments and allows graphene to take full advantage of ultrahigh interface capacitance resulting from the electric double layer phenomenon. This high interface capacitance, however, also raises the concern of impaired frequency response due to parasitics.

Two highly accurate models have been developed to study and predict the DC behavior of graphene electrolyte-gated field-effect transistors (EGFETs). Little work, however, has been reported on the AC capabilities of graphene EGFETs. An accurate frequency response model is critical for developing high-speed chemical and biological sensor applications.

This work develops a frequency-dependent smallsignal model for graphene EGFETs. Graphene EGFETs are microfabricated to experimentally determine intrinsic voltage gain and frequency response and to develop a frequency-dependent small-signal model. Graphene EGFETs' small-signal model transfer functions are found to contain a unique pole due to an additional resistive element, which stems from the electrolyte gating of these devices. Intrinsic voltage gain, cutoff frequency, and transition frequency for the microfabricated graphene EGFETs are approximately 3.1 V/V, 1.9 kHz, and 6.9 kHz, respectively. This work marks a critical step in the development of highspeed chemical and biological sensors using graphene EGFET technology for a variety of applications such as electrophysiology.



▲ Figure 1: Intrinsic voltage gain as a function of drain-source voltage and gate-source voltage as calculated from DC characterization.



▲ Figure 2: Fit of experimental graphene EGFET magnitude response with newly developed small-signal model for graphene EGFETs (common-source amplifier configuration inset).

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## Graphene-on-GaN Hot Electron Transistor with van der Waals Heterojunction Base-Collector Junction

A. Zubair, A. Nourbakhsh, J.-Y, Hong, M. Qi, D. Jena, J. Kong, M. Dresselhaus, T. Palacios Sponsorship: ARO, STC CIQM, NSF, AFOSR Foldable and Adaptive Two-dimensional Electronics MURI

The hot electron transistor (HET) is a promising device concept that can potentially overcome the limitations of heterojunction bipolar transistors (limited by the diffusion of the minority carriers across the base) and high-electron- mobility transistors (limited by the saturation velocity of carriers and the lithography of the gate) in ultra-high frequency applications. The HET is a unipolar and majority carrier device in which the baseto-emitter voltage controls the transport of ballistic hot electrons through a transit layer smaller than the mean free path of the carriers. Single layer graphene is an ideal material for the base layer of HETs for potential THz applications. The ultra-thin body (~0.34 nm) and exceptionally long mean free path maximize the probability for ballistic transport across the base of the HET.

The existing graphene-base HETs with SiO<sub>2</sub>/Si as an emitter stack suffer from low current density. In this work, we use 3-nm MBE-grown AlN on bulk ammonothermal n-GaN substrate. The GaN/AlN heterostructure has a higher tunneling current than Si/SiO<sub>2</sub> due to smaller conduction band offset at the junction. The epitaxial nature of the AlN/GaN also provides a high quality trap-free interface. The output current density and gain of the device depends on the extraction efficiency of the collector. The use of ALD dielectrics with large conduction band offset as collector barriers in existing HETs not only reduces the current density but also creates defect on the graphene surface during deposition. However, the atomic layers of two-dimensional materials (i.e. WSe<sub>2</sub>) can be mechanically transferred onto any arbitrary substrate or paired with another atomic layer (i.e. graphene) to form a van der Waals heterojunction with a defect-free, sharp interface.

We demonstrate, for the first time, the operation of a high performance HET using a graphene/WSe2 as a base-collector barrier. The resulting device, with a GaN/AlN heterojunction as emitter, exhibits a current density of 50 A/cm<sub>2</sub>, current gain above 3, and 75% injection efficiency, which are record values among graphene-base HETs. These results not only provide a scheme to overcome the limitations of graphenebase HETs toward THz operation but are also the first demonstration of a GaN/vdW heterostructure in HETs, revealing the potential for novel electronic and optoelectronic applications.



▲ Figure 1: Schematic on-state energy band diagram of an HET with GaN/AIN emitter stack and graphene/WSe<sub>2</sub> base-collector stack when  $V_{CB}$  > OV (dotted line) and  $V_{CB}$  < OV (solid line).



Figure 2: Injection efficiency as function of  $V_{CB}$  at different constant emitter injections in common-base mode. Inset shows the Gummel plot of the same device at  $V_{CB}$  = 3V.

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## High Linearity GaN-Transistors for RF and High Power Amplification

S. Joglekar, U. Radhakrishna, T. Palacios Sponsorship: RUAG, ONR PECASE

The recent proliferation of mobile devices and the surge in the demand for internet of things (IoT) is promoting the need for efficient wireless data communication. Key emergent applications ranging from 5G-LTE, WIMAX, Sat-Com, and CAT-TV to radar, space applications, D2D, and other communication protocols in the range of L-band to millimeter-wave must operate within stringent constraints on the spectral bandwidth and adjacent-channel interference. In addition, the base station accounts for 56% of the total power consumed in a typical end-to-end cellular network; the RF power amplifier (PA) in the base station contributes a significant portion of this power budget. As a result, there is a strong need to achieve high-linearity high-efficiency PAs to avoid intermodulation distortion and channel interference.

In this work, we exploit the properties of the AlGaN/ GaN heterostructure system, along with a new device architecture to attain device-level implementation of high linearity. The proposed device, seen in Figure 1, is based on a nano-ribbon (NR) structure. Numerous NRs with varying width form the channel of the transistor and are connected in parallel to form the device. In comparison to a planar AlGaN/GaN transistor of the same effective width, the NR-GaNFET displays a lower g'm (double derivative of transconductance, an important measure of linearity), as seen in Figure 2a. In addition, large signal linearity improvement has been demonstrated in these NR-based devices. Figure 2b shows that use of this approach improves the fundamental output power and delays the saturation in output power  $\mathrm{P}_{\mathrm{out}}$  at 6 GHz. Simultaneously, the harmonic outputs at 12 and 18 GHz are reduced considerably compared to a planar device, as seen in Figures 2c and d. In conclusion, high linearity in GaN transistors is demonstrated by both DC and large signal measurements using the new device architecture.



▲ Figure 1: Schematic of NR structure device.



▲ Figure 2: Device data for planar and NR device showing (a) g"<sub>m</sub> vs. gate voltage, showing lowering of g"<sub>m</sub> for NR device, (b) delayed output power saturation for an NR device; (c) and (d) lower first and second harmonic outputs, respectively, for a NR device.

## Novel Device Design for High Linearity GaN Power Amplifier

J. Hu, D. Piedra, U. Radhakrishna, J. Grajal, T. Palacios Sponsorship: RUAG

Gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) have been an emerging technology for the use in next-generation wireless communication systems. The combination of high-electron-mobility and critical electric field allows unprecedented power levels, power-added-efficiency (PAE), and breakdown voltage in GaN power amplifiers (PAs). Despite the advances in GaN radio frequency technology, the non-linearity characteristics of GaN PAs and the impact on the circuit performance have not been thoroughly investigated.

The goal of this project is to understand the key device design parameters and their impact on the amplifier linearity, eventually to improve the  $g_{\rm m}$  and  $f_{\rm T}$  linearity characteristics of GaN PAs by means of

device-level and thermal design without compromising the aforementioned figures of merit.

From the results based on the MIT Virtual Source GaNFET-RF model, we understand that the primary non-linear content in  $g_m$  occurs in the region of transition from weak to strong accumulation. This causes significant higher-order harmonic components and intermodulation distortion in power amplification. To solve this problem, we propose several new approaches to engineer the transition between weak and strong accumulation in GaN multi-finger power amplifiers. In this way, we are able to tailor the overall transconductance characteristics, and thus the IMD due to higher order transconductance can be minimized.

## Vertical GaN Power FinFETs on Bulk GaN Substrates

M. Sun, Y. Zhang, T. Palacios Sponsorship: ARPA-E

Lateral GaN transistors on Si substrates with operating voltage up to 650 V are now commercially available. However, for high-voltage high-current applications, a vertical structure is preferred because 1) its die area does not depend on the breakdown voltage; 2) the surface is far from the high electric field regions, which minimizes trapping effects; and 3) high current levels are typically possible, thanks to the easier current extraction when the source and drain contacts are positioned vertically on opposite sides of the wafer. The most studied vertical GaN transistor structures, the current aperture vertical electron transistor (CAVET) and trench metal-oxide-semiconductor field-effect transistors (MOSFETs), have made significant progress in performance, but they still face great challenges. One of the major challenges for these two structures is the p-GaN layer. A GaN vertical power Fin fieldeffect transistor (FinFET) with only n-type GaN epilayers is demonstrated, as shown in the cross-sectional scanning electron microscope (SEM) image in Figure

2. The current is controlled through a sub-micron finshape vertical channel, which is surrounded by gate metal electrodes.

An enhancement-mode GaN vertical power FinFET with sub-micron channels is demonstrated. Combining dry/wet etching achieves a smooth vertical fin profile. The fabricated transistor showed a threshold voltage of 1 V and specific on resistance of 0.089 m $\Omega$ cm<sup>2</sup> (Figure 1) with a highly doped n<sup>+</sup> GaN cap layer. The  $I_{on}/I_{off}$  ratio is up to 10<sup>11</sup>. The subthreshold swing is 75 mV/dec; the hysteresis is very small, which demonstrates the excellent material quality of the wet-etched sidewall. By proper engineering, the peak electric field distribution, a blocking voltage of 800 V was achieved (Figure 2). These results make this vertical GaN power FinFET very promising for highvoltage, high-current, low-cost, high-performance power electronics applications. Detailed information about this technology appears in the third reading.



▲ Figure 1: Output characteristics of the power FinFET with channel length 250 nm. The current density is calculated by averaging the active fin areas of the transistor.



▲ Figure 2: Off-state leakage curves of three transistor edge termination designs: 1) without field plate, 2) with field plate, and 3) with both field plate and field oxide. The inset shows the cross-sectional SEM image of the power FinFET.

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# Local Stress and Electric Field Measurements in GaN HEMTs with Micro-Raman Spectroscopy

K. R. Bagnall, C. E. Dreyer, D. Vanderbilt, E. N. Wang Sponsorship: MIT/MTL GaN Energy Initiative, ONR, SMART-LEES

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are one of the most promising compound semiconductor technologies for high power amplifiers and high voltage power conversion systems. However, elevated channel temperatures and high electric fields in critical areas of these devices are believed to cause performance degradation and premature failure through structural damage and electrochemical reactions. Thus, achieving the full potential of GaN-based transistors requires state-of-the-art experimental characterization techniques with high spatial resolution and multiphysics modeling of self-heating, thermoelastic, and piezoelectric effects.

In this work, we have developed an experimental technique for simultaneously measuring the vertical electric field along the c-axis and the inverse piezoelectric (IPE) stress in the c-plane with  $\approx 1~\mu m$  spatial resolution via micro-Raman spectroscopy. In collaboration with computational material scientists at Rutgers University, we discovered the correct electric

field dependence of the optical phonon frequencies of wurtzite GaN, which are strongly affected by the E<sub>z</sub> field component through the internal structural r parameter. We found that the vertical electric field shown in Figure 1 more strongly shifts the optical phonon frequencies in GaN HEMTs measured by micro-Raman spectroscopy than the in-plane stress does. For the first time, we demonstrated experimental measurement of the electric field in a semiconductor device with micro-Raman spectroscopy and gained detailed insight into the role of impurities in the GaN buffer on the electrostatic behavior of the transistor. This work represents a new opportunity to perform simultaneous electrical, thermal, and mechanical measurements in semiconductor devices with a single experimental technique. We anticipate that our work will enable unprecedented insight into the complex electro-thermo-mechanical physics of GaN transistors and enable the development of GaN HEMTs with record performance and reliability.



▲ Figure 1: (a) Optical microscope image of the GaN HEMT under test. (b) The average vertical electric field in the gatedrain access region derived from the experimental micro-Raman measurements and the 3-D electro-mechanical model of the HEMT, which agree quantitatively to within 35%.

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## Reliability of GaN-Based Devices Integrated with Silicon

W. A. Sasangka, G. J. Syaranamual, R. I. Made, C. L. Gan, C. V. Thompson Sponsorship: SMART

There is strong interest in monolithic integration of Al-GaN/GaN high electron mobility transistors (HEMTs) and light emitting diodes (LEDs) with Si complementary metal-oxide semiconductor (CMOS) circuits. Also, the use of Si substrates for fabrication of GaN-based HEMTs and LEDs allows less expensive large-scale production and also opens up many new applications. However, the constraints on the reliability of these devices are still not fully understood

Dislocations are known to be associated with both physical and electrical degradation mechanisms of AlGaN/GaN-on-Si HEMTs. We have observed evidence for threading dislocation movement toward the gateedges in AlGaN/GaN-on-Si HEMT under high reverse bias stressing (Figure 1). Stressed devices have higher threading dislocation densities (i.e.,  $\sim 5 \times 10^{9}/\text{cm}^{2}$ ) at the gate-edges, as compared to unstressed devices (i.e., ~2.5 ×  $10^{9}$ /cm<sup>2</sup>). Dislocation movement correlates well with high tensile stress (~1.6 GPa) at the gate-edges, as seen from inverse piezoelectric calculations and X-ray synchrotron diffraction residual stress measurements. Based on Peierls stress calculations, we believe that threading dislocations move via glide in  $(11-20)/{1-100}$ and (11-20)/{1-101} slip systems. This result illustrates the importance of threading dislocation mobility in controlling the reliability of AlGaN/GaN-on-Si HEMTs.

We have also investigated the influence of the two-dimensional electron gas (2DEG) in AlGaN/GaN HEMTs on their reliability under ON-state conditions. Devices stressed in the ON-state showed a faster decrease in the maximum drain current (IDmax) compared to identical devices stressed in the OFFstate with a comparable electric field and temperature. Scanning electron microscope (SEM) images of ON-state stressed devices showed pit formation at locations away from the gate-edge in the drain-gate access region. Cross-sectional transmission electron microscope (TEM) images also showed dark features at the AlGaN/SiN interface away from the gate edge (Figure 2). Electron energy loss spectroscopy (EELS) analysis of the dark features indicated the presence of gallium, aluminum and oxygen. These dark features correlate with pits observed in the SEM micrographs. We propose that in addition to causing joule heating, energetic electrons in the 2D electron gas contribute to device degradation by promoting electrochemical oxidation of the AlGaN.

In ongoing research we are investigating the effects of density of SiN passivation layers on the reliability of AlGaN/GaN-on-Si HEMTs and characterizing defects generated during constant current stressing of InGaNon-Si LEDs.



▲ Figure 1: Threading dislocation density as a function of distance from the center of the gate for devices stressed at different gate voltages (VG).



▲ Figure 2: Electrochemical oxidation mechanism of AlGaN under on-state stressing.

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## Gate Current Degradation of InAIN/GaN HEMTs under Electrical Stress

Y. Wu, J. A. del Alamo Sponsorship: NRO

InAlN/GaN high-electron-mobility-transistors (HEMTs) have emerged as promising candidates for high-power millimeter wave applications due to their excellent gate-length scaling potential. This potential stems from the high spontaneous polarization of InAlN that yields a large 2DEG density at the InAlN/GaN interface even with a very thin barrier layer. However, in nanometer-scale InAlN/GaN HEMTs, the use of a very thin barrier layer brings gate leakage current and reliability concerns. Our work focuses on studying the degradation mechanisms of the gate leakage current under both ON-state stress and  $V_{DS} = 0$  stress.

Under simultaneous high-power conditions (simultaneously high  $V_{DS}$  and  $I_D$ ), besides drain current drop and a positive threshold voltage shift, we have observed an unusual leakage path being created between the gate and the source, as shown in Figure

1. We have proposed that under these conditions, the gate-source diode is strongly forward biased and there is significant gate current. The combination of high gate current, high temperature, and strong electric field across the AlN barrier on the source side generates defects, which increase gate leakage on that side of the device. In addition, local heating produces gate sinking and a positive  $V_T$  shift.

To further prove our hypothesis, we have conducted a room temperature  $V_{DS} = 0$  V stress experiment with positive  $V_G$  increasing from 0.1 V to 2.5 V. Similar permanent electrical degradation was produced but this time on both the source and drain sides, as demonstrated by Figure 2. This degradation is consistent with our hypothesis that high forward  $V_G$ under high temperature leads to an anomalous gate leakage current increase.



▲ Figure 1:  $I_G$ - $V_G$  characteristics (measured at 25°C) at  $V_{DS}$ =0 before (solid lines) and after (dashed lines) constant stress at  $V_{DSstress}$  = 25 V and  $I_{Dstress}$  = 400 mA/mm.  $I_S$  and  $I_D$  are also indicated. After stress,  $I_G$  and  $I_S$  increase by several orders of magnitude. In contrast,  $I_D$  shows a much smaller increase.



▲ Figure 2:  $I_G$ - $V_G$  characteristics (measured at 25°C) at  $V_{DS}$ =0 before (solid lines) and after (dashed lines) positive  $V_G$  step-stress-recovery experiment with  $V_{DS}$ =0.  $I_S$  and  $I_D$  are also indicated. After stress,  $I_G$  roughly splits in half between  $I_D$  and  $I_S$ , indicating degradation on both source and drain sides of the device.

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## **OFF-State TDDB in High-Voltage GaN MIS-HEMTs**

S. Warnock, J. A. del Alamo Sponsorship: Texas Instruments

With the promise of higher-frequency, higher-temperature, and more efficient operation, GaN-based transistors show enormous potential for high-voltage power management applications. The AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT) is the most suitable device structure for power switches, offering lower gate leakage than its HEMT counterpart. GaN devices show great promise, but several reliability challenges remain to be addressed before these devices can achieve widespread commercial deployment. Time-dependent dielectric breakdown (TDDB), a catastrophic condition arising after prolonged high-voltage gate stress, is a particularly important concern.

In this work, we explore TDDB under OFF-state conditions; that is, a negative gate bias is used to turn off the channel, and a high positive bias is applied to the drain terminal. This is the most common state of a power switching transistor in a power management circuit. In the OFF state, there is a high electric field through the gate dielectric at the gate edge on the drain side, as shown in Figure 1. Under prolonged stress, this will inevitably result in dielectric defect formation and eventual dielectric breakdown. It is uncommon to think of TDDB under OFF-state conditions; although there is limited work on this topic in GaN HEMTs, this reliability concern in MIS-HEMTs has thus far been overlooked.

We find that in OFF-state stress, the presence of transient instabilities such as current collapse and threshold voltage (VT) shift have a dramatic impact on the device TDDB statistics, as seen in Figure 2. The statistics in blue result from OFF-state TDDB experiments in the dark: they do not follow the expected linear distribution, and the breakdown times span many orders of magnitude. By using ultraviolet (UV) light during stress to prevent pervasive trappingrelated effects, we can observe intrinsic TDDB behavior, as shown by the data in red. The use of UV light highlights the fact that trapping effects during stress cause significant overestimation of device breakdown voltage under OFF-state stress conditions.

In order to develop accurate lifetime models for GaN MIS-HEMTs, much care must be taken to ensure that a device's lifetime does not become distorted by transient trapping-related degradation effects.



▲ Figure 1: Sketch of a GaN MIS-HEMT illustrating the electric field distribution across the gate dielectric during OFF-state stress. Electric field lines in white yield the electric field profile in blue.



▲ Figure 2: Weibull plot of time-to-breakdown  $t_{BD}$  for OFF-state stress experiment without UV light in blue, and under illumination by 3.5 eV UV light, in red.  $V_{DS,stress}$ =89 V for UV data and 118 V for measurements in the dark.  $V_{GS,stress}$ =  $V_{T0}$ -5 V.

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# Time-Dependent Dielectric Breakdown in High-Voltage GaN MIS-HEMTs: The Role of Temperature

A. Lemus, S. Warnock, J. A. del Alamo Sponsorship: Texas Instruments

There is a large demand for energy-efficient power electronics, for which silicon-based devices – the current market standard – are not ideal. GaN, however, has material properties (such as its large band gap of 3.4 eV) well-suited for power efficiency. GaN-based transistors offer a promising solution for these applications, but several reliability challenges remain. The motivation of our work is to address a specific reliability concern and failure mode known as time-dependent dielectric breakdown (TDDB). We study GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs), sketched in Figure 1, which have a lower gate leakage than HEMTs, as necessary for power switches.

Time-dependent dielectric breakdown (TDDB) is a catastrophic event that occurs in field-effect transistors under prolonged high-voltage gate bias stress. This results in defect formation in the device

dielectric, which facilitates current flow between the gate and its conductive channel. Eventually, a highly conductive path will suddenly form in the dielectric. The instantaneous power dissipation through the path creates a short that destroys the device. Our interest is in exploring how this TDDB mechanism occurs in GaN devices and how it is affected by temperature.

We choose to conduct our TDDB experiments at several different temperatures under constant positive gate voltage stress. We observe a negative correlation between temperature and the breakdown time of our devices, as Figure 2 shows. However, we also found that the activation energy for TDDB in these devices is rather small. In fact, it is significantly smaller than other reported values in the GaN MIS-HEMT system.

This research ultimately aims to contribute to the understanding of TDDB in GaN MIS-HEMTs towards the goal of developing a TDDB lifetime model.



▲ Figure 1: Structure of GaN MIS-HEMT used for this TDDB study.



▲ Figure 2: Weibull distribution for time to hard breakdown (tHBD) for devices at four different temperatures. Hard breakdown occurred sooner in devices tested at higher temperatures.

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  presented at Compound Semiconductor Manufacturing Technology Conference (CS MANTECH), 2015.
- S. Warnock and J. A. del Alamo, "Progressive Breakdown in High-Voltage GaN MIS-HEMTs," presented at the IEEE International Reliability
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## Gate Dielectric Reliability under AC Stress in High-Voltage GaN Field-Effect Transistors

E. S. Lee, S. Warnock, J. A. del Alamo Sponsorship: Texas Instruments

Energy-efficient electronics have been gaining attention as a solution to meet the growing demand for energy and sustainability. GaN field-effect transistors (FET) show great promise as high-voltage power transistors due to their ability to withstand a large voltage and carry large current. However, at the present time, the GaN metal-insulator-semiconductor high-electronmobility-transistor (MIS-HEMT), the device of choice for electric power management, is excluded from commercialization due to many challenges, including gate dielectric reliability. Under continued gate bias, the dielectric ultimately experiences a catastrophic breakdown that renders the transistor useless, a phenomenon called time-dependent dielectric breakdown (TDDB).

Our research aims to understand the physics of TDDB in GaN MIS-HEMTs. So far, efforts have been focused on constant stress due to the ease of experimental and instrumental setup. In contrast, our research aims to study the effects of applying AC stress to the gate. This mimics the real-world operating environment of FETs in power conversion circuits where they experience rapid transitions between different conducting states. In Si metaloxide–semiconductor FETs (MOSFETs), a marked difference in TDDB time for AC stress and DC stress has been demonstrated. However, to our knowledge, similar studies have not yet been carried out in GaN MIS-HEMTs.

Figure 1 shows a comparison between the statistical distribution of dielectric hard breakdown times (T<sub>HBD</sub>) for DC stress and AC stress under positive gate bias stress in transistors from our industrial collaborator. The statistical distribution of breakdown times follows the Weibull distribution. The plot graphs ln(-ln(1-F)) versus time to yield a linear fit, where F is the cumulative device failure fraction. We can see that, for the same conditions, AC stress at 10 kHz yields a statistical distribution with a longer hard breakdown time. Figure 2 shows that increasing the AC frequency beyond 10 kHz is of minimal relevance. These results may imply that the different voltages in AC stress may contribute to the recovery of the device.

While we are still in the very early stages of experimentation, we aim to show whether AC stress TDDB and DC stress TDDB in GaN MIS-HEMTs shows the clear difference observed in Si devices.



▲ Figure 1: Weibull plot of  $T_{HBD}$  for DC stress and AC stress at 10 kHz. DC:  $V_{GS,stress} = 12.7 \text{ V}, V_{DS,stress} = 0 \text{ V}.$ AC:  $V_{GS \text{ Hi,stress}} = 12.7 \text{ V}, V_{GS \text{ LO}, stress} = 0 \text{ V}, V_{DS,stress} = 0 \text{ V},$ duty cycle = 50%, f = 10 kHz. There is a clear increase in  $T_{HBD}$  for AC stress.



▲ Figure 2: Weibull plot of  $T_{HBD}$  for AC stress at 10 kHz and 100 kHz. In both cases,  $V_{GS \text{ Hi,stress}} = 12.7 \text{ V}$ ,  $V_{GS \text{ LO}, \text{stress}} = 0 \text{ V}$ ,  $V_{DS, \text{stress}} = 0 \text{ V}$ , duty cycle = 50%. There is no significant change in  $T_{HBD}$  for the two frequencies.

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## Effect of Doping on Self-Aligned InGaAs FinFETs

A. Vardi, J. A. del Alamo Sponsorship: DTRA, Lam Research

InGaAs is a promising candidate as channel material for complementary metal-oxide semiconductor (CMOS) technologies beyond the 7-nm node. In this dimensional range, only high aspect-ratio (AR) 3-D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive InGaAs Fin field-effect transistor (FinFET) prototypes have been demonstrated recently. However, as the fin width is scaled down to 10 nm, severe On-current degradation is observed. The origin of this performance degradation is still unclear.

In this work, we study the effect of  $\delta$ -doping on the performance of self-aligned InGaAs FinFETs. We closely follow the fabrication process of selfaligned planar InGaAs quantum-well metal-oxidesemiconductor FETs (MOSFETs) realized previously but added a dry-recess process for the n<sup>+</sup> InGaAs cap. The starting material used for this study is shown in Figure 1(a). Low- resistivity Mo is first sputtered as contact metal, followed by SiO<sub>2</sub> chemical vapor deposition. The gate pattern is defined by electronbeam lithography. The SiO<sub>2</sub> and Mo layers are then etched by reactive ion etching (RIE). After this, the top n<sup>+</sup> InGaAs cap is dry-etched in a well-controlled manner (Figure 1b). Fins are then patterned in the recessed area using 60-nm-thick HSQ and E-beam lithography, and RIE etched. This process yields fins as narrow as 20 nm with an aspect ratio of 8. The fins are highly vertical in the top ~70 nm. After fin etching, several cycles of digital etching are applied to further

reduce the fin width down to as low as 7 nm and reduce the sidewall roughness. Gate dielectric composed of 3-nm  $HfO_2$  is deposited by atomic layer deposition and sputtered Mo is used as a gate metal and patterned by RIE. The device is finished by via opening and pad formation. In this process, the HSQ that defines the fin etch is kept in place. This makes our FinFETs doublegate transistors with carrier modulation only on the fin sidewalls (Figure 1c).

The electrical characteristics normalized to gate periphery  $(2xH_c)$ , where  $H_c$  is the channel thickness defined in Figure 1a of a device with  $W_f$ =10 nm,  $L_g$ =50 nm (AR=  $H_c/W_f=5$ ) for the structure w/ (red) and w/o (blue)  $\delta$ -doping are shown in Figure 2a–b. Well-behaved characteristics and good sidewall control are obtained.  $R_{on}$  are 540 and 960  $\Omega$ · $\mu$ m, and a peak transconductance,  $g_m$ , of 630 and 430  $\mu$ S/ $\mu$ m are obtained at  $V_{DS}$ =0.5 V for the doped and undoped structures, respectively. Although the doped sample shows superior On performance, the Off current and subthreshold swing of the undoped sample are better. The saturated  $S_{min}$  is 88 and 74 mV/ dec for doped and undoped samples, respectively. The reason for this performance difference is related to electrostatics within the fins. While in the undoped sample, carriers accumulate along the fin sidewalls, in the doped fins there are also carriers in the body of the fins. This enhances the conductivity of doped fins; however, it takes a larger negative gate voltage to deplete those fins, and the Off performance degrades.







Figure 2: Electrical characteristics of FinFET with  $L_g$ =50 nm and  $W_f$ =10 nm fabricated on doped (red) and undoped (blue) structures. (a) output and (b) subthreshold.

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## High-Resolution Transmission Electron Microscopy of III-V FinFETs

L. Kong, W. Lu, A. Vardi, J. A. del Alamo Sponsorship: Lam Research, UROP

III-V materials have great potential for integration into future complementary metal-oxide semiconductor technology due to their outstanding electron transport properties. InGaAs n-channel metal-oxide semiconductor field-effect transistors have already demonstrated promising characteristics, and the antimonide material system is emerging as a candidate for p-channel devices. As transistor technology scales down to the sub-10-nm regime, only devices with a 3-D configuration can deliver the necessary performance. III-V Fin field-effect transistors (FinFETs) have displayed impressive characteristics but have shown degradation in performance as the fin width is scaled to the sub-10-nm regime. In this work, we use high-resolution transmission electron microscopy (HRTEM) in an effort to understand how interfacial properties between the channel and high-k dielectric affect device performance.

At the interface between the channel material, such as InGaSb or InGaAs, and the high-k gate dielectric, properties of interest include defect

density, interdiffusion between the semiconductor and dielectric, and roughness of the dielectricsemiconductor interface. Using HRTEM, we can directly study this interface and try to understand how it is affected by different processing conditions and its correlation with device characteristics.

We have analyzed both InGaSb and InGaAs FinFETs. In electrical characteristics, InGaSb p-channel FinFETs with thinner fins display inadequate gate control of the channel current. HRTEM images of the InGaSb FinFETs reveal non-uniformity in the dielectric as well as interdiffusion between the InGaSb and (Figure 1). We are exploring different passivation techniques to improve this interface.

We have also performed HRTEM on novel InGaAs FinFETs with sub-10-nm fins that display superior electrical characteristics. HRTEM images show a clean interface between the dielectric and the channel (Figure 2). We are using HRTEM to further analyze the electrostatics and quantum behavior by analyzing fin width, shape, and crystallographic orientation.



🔺 Figure 1: HRTEM image of InGaSb fin. The interface between 🔺 Figure 2: HRTEM image of InGaAs fin. The interface between the dielectric and channel is not sharp due to interdiffusion between the dielectric and channel is sharp and well defined. InGaSb and Al<sub>2</sub>O<sub>3</sub>.

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## Digital Etching for Sub-10-nm III-V Multi-Gate MOSFETs

W. Lu, X. Zhao, J. A. del Alamo

Sponsorship: DTRA, Korea Institute of Science and Technology, Lam Research, NSF, Samsung

As complementary metal-oxide semiconductor (CMOS) technology keeps advancing, new materials are under active research in the hope of replacing Si in future generations. III-V multi-gate transistors such as InGaAs Fin field-effect transistors (FinFETs) or nanowire gate-all-around metal-oxide-semiconductor field-effect transistors (MOSFETs) are regarded as some of the most promising candidates. As the physical size of Si FinFETs is shrinking, it is critical to develop the technology to fabricate III-V 3-D devices in the sub-10-nm range. In this dimensional regime, precise etching control is the key challenge.

Digital etching is an etching technique that separates the oxidation and oxide removal steps characteristic of chemical etching. It makes both the oxidation and oxide removal self-limiting, thus enabling nanometer-scale control of the etching process. In the last few years, the use of digital etching has enabled demonstrations of aggressively scaled III-V FinFETs and nanowire MOSFETs. However, so far digital etching has been applied only to arsenide-based III-Vs. It is not applicable to highly reactive compounds such as antimonides. In addition, the mechanical yield of digitally etched vertical nanowires dramatically degrades at and below 10 nm in diameter.

In this project, we have developed a novel nonaqueous digital etching technique that enables the fabrication of sub-10- nm vertical fins and nanowires. The new approach uses acids dissolved in alcohol, which has less surface tension than water and therefore exerts smaller mechanical forces against the nanowires. We obtain a consistent 1 nm/cycle etching rate on both InGaAs- and InGaSb-based heterostructures. We show an over 97% yield in the fabrication of sub-10-nm vertical nanowires. We have also demonstrated a record 5-nm diameter nanowire with a height of 230 nm and an aspect ratio of 46. Finally, we fabricated InGaAs vertical single nanowire MOSFETs using this technique. Those transistors have a linear subthreshold swing of 70 mV/dec, one of the best values reported in such devices. The subthreshold swing shows that the new digital etching technique is effective in yielding a high-quality surface in InGaAs nanowires. We are now working towards applying this technique to demonstrate InGaAs and InGaSb FinFETs and vertical nanowire MOSFETs with sub-10-nm fin width and nanowire diameter.



▲ Figure 1: InGaAs vertical nanowire with 5-nm diameter, 230 height obtained after 10 cycles of digital etch in H<sub>2</sub>SO<sub>4</sub>: methanol.



▲ Figure 2: Subthreshold characteristics of single vertical nanowire transistors with 40- and 20-nm diameter, with lowest subthreshold swing of 70 mV/dec. The inset shows S vs. I<sub>D</sub> of these devices.

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## **III-V Vertical Nanowire Transistors for Ultra-Low Power Applications**

X. Zhao, A. Vardi, J. A. del Alamo Sponsorship: NSF E3S STC, Lam Research, SRC

In future logic technology for the Internet of Things and mobile applications, reducing transistor power consumption is of paramount importance. Beyond Si complementary metal-oxide semiconductors (CMOS), transistor technologies based on III-V materials are widely considered as a leading solution to lower power dissipation by enabling dramatic reductions in the transistor supply voltage. Vertical nanowire (VNW) transistor technology holds promise as the ultimately scalable device architecture. VNW metal-oxide-semiconductor field-effect transistors (MOSFETs) have been predicted to offer significant advantages compared to their lateral counterpart in terms of density-performance-power tradeoffs. The VNW transistor architecture also fully unleashes the advantage of III-V materials by enabling bandgap engineering along the transport direction, opening the door for the tunnel-FET (TFET), a quantum device that potentially break the power limits of MOSFETs.

This work demonstrates InGaAs-based VNW MOSFETs and TFETs fabricated via a top-down approach. Record performance has been achieved

in our latest InGaAs VNW MOSFETs in terms of the trade-off between subthreshold swing (S) and ON current, as benchmarked in Figure 1. The performance improvement over an earlier generation of MOSFETs comes mainly from a much better oxide/semiconductor interface enabled by improved atomic-layer-deposition chamber conditioning and rapid thermal annealing.

Stemming from the same reasons, our latest VNW TFETs have also shown state-of-the-art performance, delivering room-temperature sub-thermal S over two orders of magnitude of current (Figure 2). The current level of the steep slope region was also among the highest ever reported. The improved oxide/ semiconductor interface also greatly suppressed the significant temperature dependence of our previous generation of TFETs, which was attributed to a tunnel-assisted generation process through a high concentration of interface traps. In our newest devices, the subthreshold swing appears to saturate at a very low level at low temperatures, highlighing the potential of the NW geometry.



▲ Figure 1: Benchmark of peak transconductance and minimum subthreshold swing at drain bias of 0.5 V for InGaAs and InAs VNW MOSFETs. A record I<sub>on</sub> of 200  $\mu$ A/ $\mu$ m is obtained at an I<sub>off</sub> = 100 nA/ $\mu$ m and V<sub>dd</sub> = 0.5 V.



▲ Figure 2: Subthreshold swing vs. I<sub>d</sub> characteristics of an InGaAs/InAs heterojunction VNW TFET demonstrated in this work, revealing sub-thermal behavior over two orders of magnitude of current. Inset shows the TFET schematic cross section.

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## A Compact Tunnel Field-Effect Transistor Model Including the Impacts of Non-Idealities

R. N. Sajjad, U. Radhakrishna, W. Chern, D. A. Antoniadis Sponsorship: NSF E3S, NSF/SRC NEEDS

The tunnel field-effect transistor (TFET) has the promise of low power switching due to its tunneling-dependent steep subthreshold swing (Figure 1a). Because of non-idealities such as the oxide-semiconductor interface traps and non-abrupt band edges (Figure 1b), practical TFETs produce higher leakage currents and higher subthreshold swing than ideal. We develop a physics-based compact model that captures these non-idealities. Our model also contains the details of TFET device physics such as the drain-voltage influence on the quantum capacitance, the superlinear output characteristics, negative differential resistance, etc. The model is tested against multiple TFET data. Figure 1c-d shows the model fits of two sets of experimental data. The minimum leakage current that originates from the trap assisted tunneling depends strongly on temperature in the experiments. The subthreshold swing decreases with reduced temperature since the contribution from the trap assisted tunneling decreases. Our model allows prediction of performance in the absence of interface traps and provides guidance for future material growth and device fabrication. Based on the compact model, we also developed a Verilog-A model that allows us to simulate circuits based on TFETs.



▲ Figure 1: (a) Ideal band to band tunneling in a TFET causes a steep switching in current under ideal conditions. The switching rate is steeper than in a MOSFET. (b) However, in practice, the OFF state current can still flow via surface traps and phonon emission, yielding a non-negligible source-drain current. (c-d) The compact model is applied to two different experiments, showing good agreement with the data at different temperatures.

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## Metal Oxide Thin-Films as the Basis of Memristive Nonvolatile Memory Devices

T. Defferriere, D. Kalaev, J. L. M. Rupp, H. L. Tuller Sponsorship: CMSE, NSF

The design of silicon-based memory devices over the past 50+ years has driven the development of increasingly powerful and miniaturized computers with the demand for increased computational power and data storage capacity continuing unabated. However, fundamental physical limits are now complicating further downscaling. The oxide-based *memristor*, a simple M/I/M structure, in which the resistive state can be reversibly switched by application of appropriate voltages, promises to replace classic transistors in the future. It has the potential to achieve an order-of-magnitude-lower operation power than existing *RAM* technology and paves the way for neuromorphic memory devices relying on non-binary coding. Our studies focus on understanding the mechanisms that lead to memristance in a variety of insulating and mixed ionic electronic conductors, thereby providing guidelines for material selection and for achieving improved device performance and robustness.

## Solution-Processed High-Voltage Organic Thin-Film Transistor

A. Shih, A. I. Akinwande Sponsorship: DARPA

Organic-based thin-film transistors (OTFTs) have been identified as excellent candidates for flexible electronics due to the weak van der Waals forces between small molecules. Electronics and sensors based on OTFTs can be made on arbitrary curved surfaces, allowing for the development of wearable electronics such as artificial skin. However, enabling truly ubiquitous electronics through OTFTs demands not only a high performance, but also a wide range of operating voltages. There are many applications that demand a high operating voltage beyond that capable of a typical thin-film transistor. For example, ferroelectric liquid, electrophoretic or electro-optic displays, digital X-ray imaging, poly-Si cold cathodes, and other sophisticated integrated microelectromechanical systems (MEMS) all require large operating voltages to function.

In this work, we are developing a solutionprocessed high-voltage organic thin-film transistor (HVOTFT) based on the organic semiconductor TIPSpentacene, operable at over a hundred volts. The design of the HVOTFT is shown in Figure 1a. We have employed a bottom contact architecture along with the dielectrics Parylene-C and BZN ( $Bi_{1.5}Zn_1Nb_{1.5}O_7$ ). The TIPS-pentacene is dissolved in a high boiling point solvent, and the solution is then drop-casted on top of the contacts to form the active thin-film. The key design structure is to introduce an ungated region in series with the traditional gated region. The gated region allows for standard transistor switching behavior, while the ungated region enables the high voltage operation by acting as a non-linear resistor.

The device has been successfully fabricated on glass substrates as well as on flexible polyimide wafers, as shown in Figure 1b. Currently, devices exhibit good performances with charge carrier mobility of ~0.05 cm<sup>2</sup>/ V·s,  $I_{on}/I_{off}$  of 10<sup>4</sup> and operating voltages beyond 100 V, as shown in Figure 2. Although mobility,  $I_{on}/I_{off}$  ratio, and breakdown voltage are relatively low compared to our pentacene evaporated devices, recent efforts to have a self-patterned crystal growth for better thickness control as well as transistor isolation have proven promising.



▲ Figure 1: (a) Cross-sectional view of the HVOTFT, (b) OTFTs made on flexible polyimide substrates.



▲ Figure 2: High-voltage output characteristics of HVOTFTs made from TIPS-pentacene via dropcasting. The channel length is 5 µm with a 10-µm ungated region. The channel width is 250 µm.

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