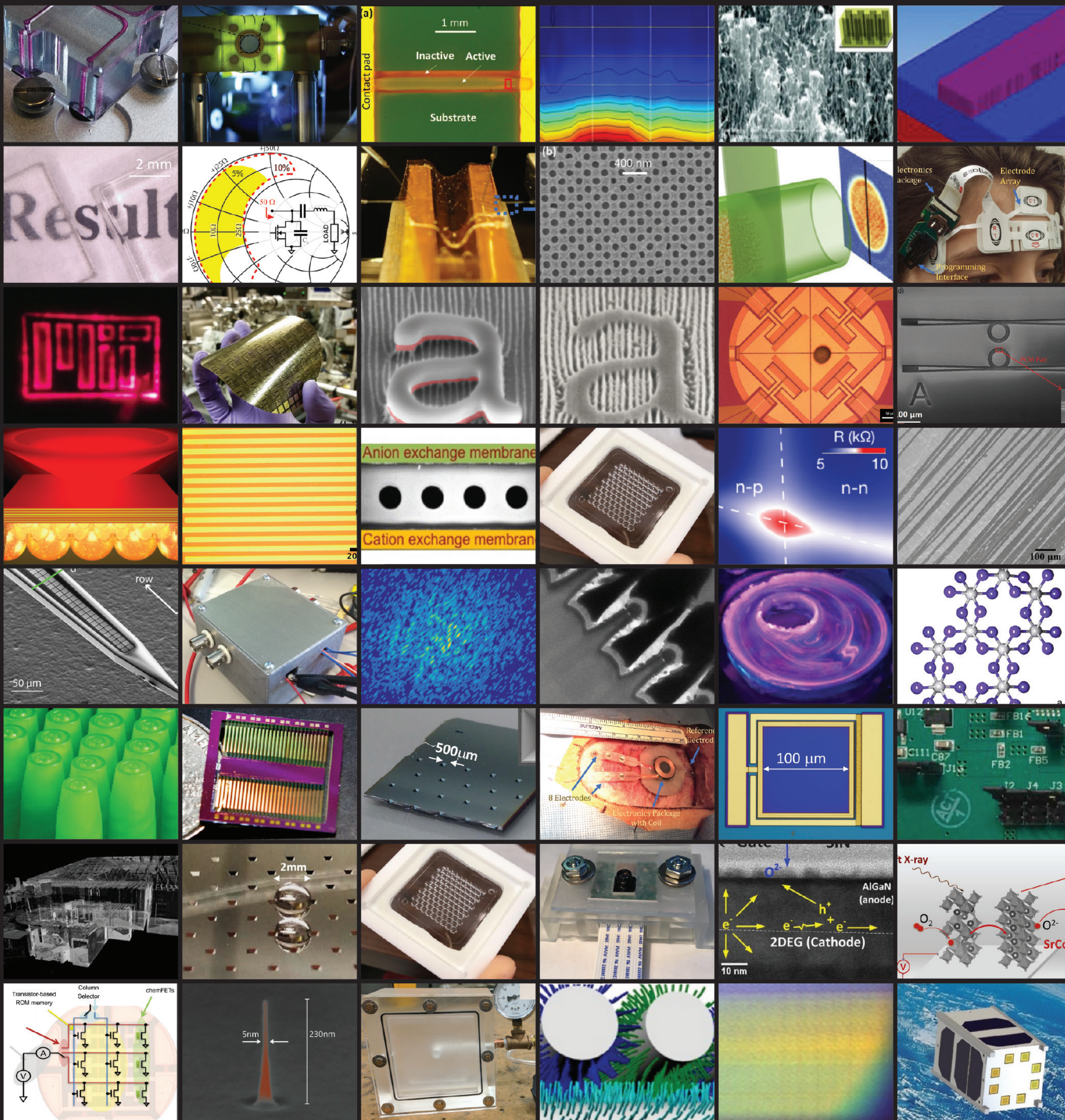

ANNUAL RESEARCH REPORT 2017

MICROSYSTEMS TECHNOLOGY LABORATORIES

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MTL Annual Research Report 2017

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Foreword

I am happy to bring to you the 2017 Annual Research Report of the Microsystems Technology Laboratories. It highlights the research and educational activities of faculty, staff, students, postdocs, and visitors associated with MTL during MIT Fiscal Year 2017.

MTL is predicated on the notion that nanoscale science and technology can help solve some of the world's greatest problems in areas of energy, communications, water, health, information, and transportation, among others. In this regard, MTL's mission is to foster world-class research, education, and innovation at the nanoscale. In all these and other important areas of human concern, as showcased in this report, researchers at MIT are carrying out fundamental research and engineering in materials, structures, devices, circuits and systems using MTL's facilities and CAD services, in search of new solutions to persistent problems. MTL's activities encompass integrated circuits, systems, electronic and photonic devices, MEMS, bio-MEMS, molecular devices, nanotechnology, sensors, and actuators, to name a few. MTL's research program is highly interdisciplinary. MTL's facilities are open to the entire MIT community and the outside world. Nearly 600 MIT students and postdocs from 23 different Departments, Laboratories, or Centers carried out their research in MTL's facilities in the last fiscal year. In addition, researchers from several companies, as well as government research laboratories and domestic and international universities, use MTL's facilities annually.

To accomplish its mission, MTL manages a set of experimental facilities in buildings 39 and 24 that host more than 150 fabrication and analytical tools. We strive to provide a flexible fabrication environment that is capable of long-flow integrated processes that yield complex devices while, at the same time, presenting low-barrier access to fast prototyping of structures and devices for users with very different levels of experience. Our fabrication capabilities include diffusion, lithography, deposition, etching, packaging, and many others. Our lab can handle substrates from small, odd-shaped pieces to 6-inch wafers. The range of materials continues to expand well beyond Si and Ge to include III-V compound semiconductors, nitride semiconductors, graphene and other 2D materials, polymers, glass, organics, and many others.

MTL also manages an information technology infrastructure that supports state-of-the-art computer-aided design (CAD) tools for device, circuit, and system design. Together with a set of relationships with major semiconductor manufacturers, MTL makes available to its community some of the most advanced commercial integrated circuit fabrication processes available in the world today.

MTL could not accomplish its mission without the vision, commitment, and generosity of a number of companies that comprise the Microsystems Industrial Group (MIG). The MIG supports the operation of MTL's facilities, and it also advises the faculty on research directions, trends, and industrial needs. The list of current MIG members can be found in the "Acknowledgments" section of this report.

The research activities described in these pages would not be possible without the dedication and passion of the fabrication, IT, and administrative staff of MTL. Day in and day out, they strive to support MTL users in the pursuit of their dreams. They do this in a professional and unassuming manner. Their names do not usually end up in the research papers, but that does not diminish the significance of their contributions. To them and to all of you who support in your own way the activities of MTL, a most sincere thank you!

Jesús A. del Alamo
Director, Microsystems Technology Laboratories
Donner Professor
Professor of Electrical Engineering
Department of Electrical Engineering and Computer Science
July 2017

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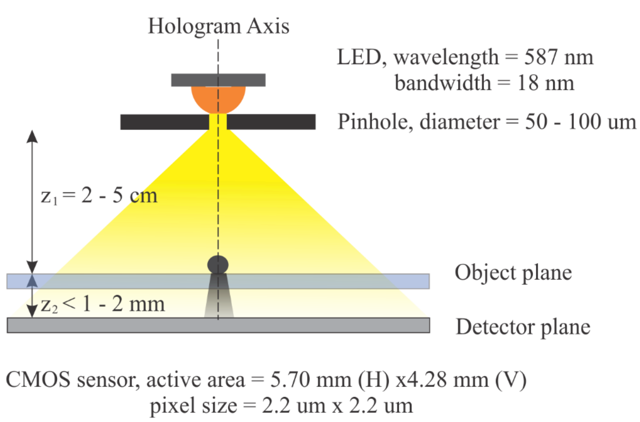
Biological, Medical Devices, and Systems

Microfluidics and Computational Imaging for Measuring Cells' Intrinsic Properties

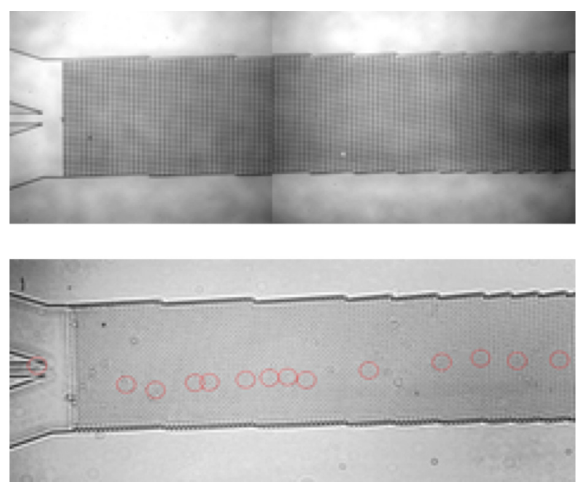
N. Apichitsopa, J. Voldman
Sponsorship: Bose Research Award

Scientific-grade optical microscopes are very powerful tools in the field of microfluidics as they can be used to observe the behaviors of micro-objects of interest inside the microfluidic devices. While conventional optical microscopes are limited by the small field of view (FOV), e.g., ~1-2 mm^2 for a 10X objective, the footprint of a microfluidic platform is typically ~cm^2. This mismatch of the FOV of the microscope and the footprint of the device restricts the area of the device and the number of micro-objects that can be viewed at the same specific time points. Although mechanically moving and observing different areas of the device under the microscope is acceptable for objects with fewer dynamic movements, it is not suitable for objects with fast movement in large-footprint particle separation devices.

Computational microscopy has been shown to provide large FOV with an order of magnitude larger than the 10X objective. We propose to combine visual observation from large FOV computational microscopy with separation of cells via a label-free microfluidic platform in order to study cell size. This system will benefit from the parallel and gentle separation of label-free cells via a microfluidic platform and parallel tracking of multiple cells in a large FOV, in contrast to the gold standard, flow cytometry, which is able to rapidly identify properties of cells in a single stream via emittance of external fluorescent cell markers. A prototype of the integrated platform was designed and fabricated. The prototype consists of a digital in-line holographic microscopy system (Figure 1) and a microfluidic deterministic lateral displacement array, which separates particles based on size. Each system was first characterized separately and later integrated, so that individual cells inside the deterministic lateral displacement array could be recorded and tracked with the large FOV digital in-line holographic microscopy system (Figure 2).



▲ Figure 1: Schematic of the large-FOV digital in-line holography system.



▲ Figure 2: Stitched microscope images of the deterministic lateral displacement array system (top) and the recorded holograms from the same device as cells flowed from left to right (bottom). Red circles depict detected cells.

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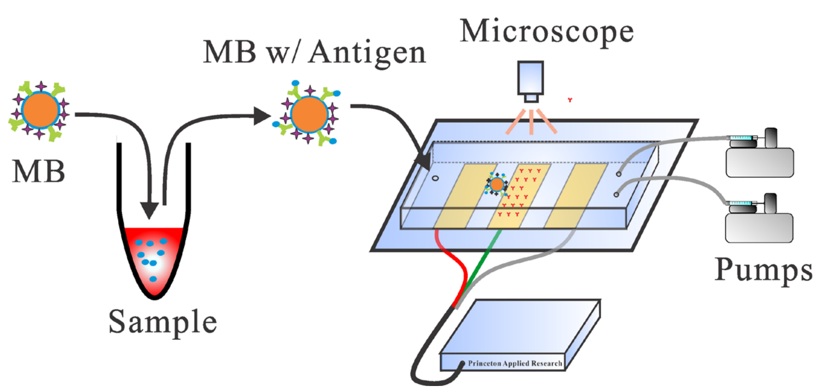
Microfluidic and Electronic Detection of Protein Biomarkers

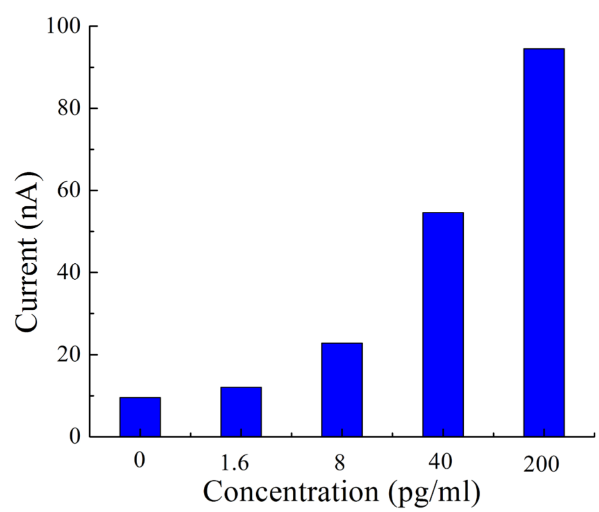
D. Wu, J. Voldman
Sponsorship: Analog Devices, Inc.

Measuring proteins biomarkers in blood is of significant clinical importance and has a substantial market. However, traditional blood tests performed in centralized laboratories take days to deliver results to patients. The need for large volumes (~mL) of blood samples also makes it challenging to perform testing of newborns and even premature infants, who have very limited blood. We are developing a bead-based microfluidic electronic biosensor that gives immediate results and requires a small volume (μL) of blood, potentially allowing testing of neonates.

The biosensor is illustrated in Figure 1 after magnetic microbeads conjugated with antibodies and enzymes are added to the sample, the biomarkers bind to antibodies because of the specific interaction between proteins and antibodies. The use of magnetic microbeads shortens the diffusion length of proteins to antibodies and thus significantly accelerates the binding process. The magnetic beads are then sent to the sensor, which consists of microfluidic channels and microelectrodes, and eventually attach to the antibodies immobilized on electrodes. The enzymes on microbeads catalyze chemical reactions and generate current, which is measured by external electronics. The amount of protein in the original sample is associated with the measured current. Figure 2 shows the results of measuring human IL-6 (~22 kDa). The results indicate that the sensitivity of our sensor is about 1 pg/mL, which is sufficient to measure most of the protein biomarkers in blood.



▲ Figure 1: Illustration of the biosensor.



▲ Figure 2: Results of measuring human IL -6.

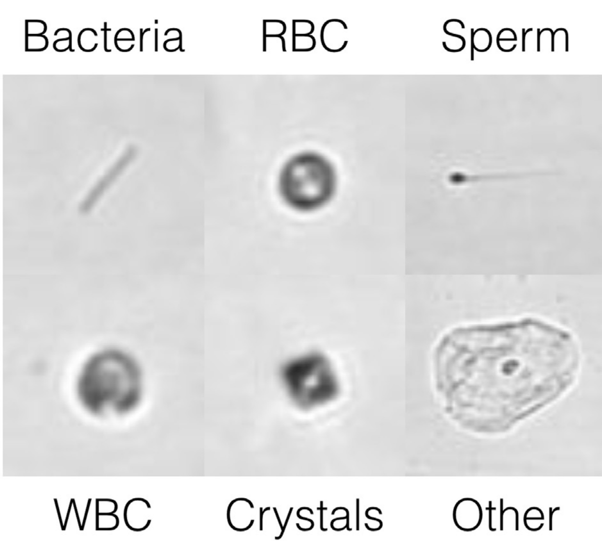
A Cell-Counting System for Point-of-Care Blood and Urine Analysis

S. R. Primas, C. G. Sodini
Sponsorship: MEDRC, Analog Devices, Inc.

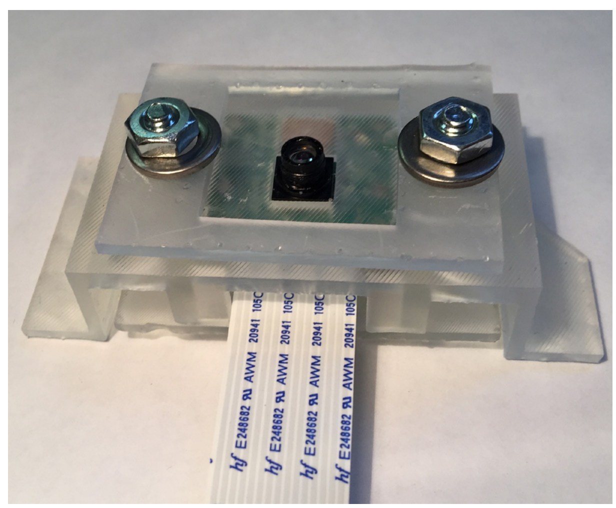
Quantifying the concentration of medically relevant cells in blood and urine remains one of the most in-demand diagnostic techniques in medicine. For example, complete blood counts (CBCs) are conducted at nearly every medical checkup to monitor diseases ranging from anemia to chronic inflammatory diseases to HIV. And, with urine, cell-counting is used to conclusively determine bacteria concentrations for the detection of urinary tract infections (UTIs). UTIs lead to 6.7 million physician office visits and 2.6 million ER visits per year in the United States.

Due to the cost and complexity of blood and urine cell counts, the majority are conducted at a medical lab instead of at the point-of-care. These labs use either expensive flow-cytometers (e.g., the Sysmex UF-1000i is $125,000) or manual classification by trained professionals using a microscope. An inexpensive and automated cell-counting system would significantly increase the access to these important diagnostic tests and even enable them to be performed at the point-of-care.

This project focuses on developing both automated cell classification and an inexpensive image acquisition system. For the automated classification, the system uses a 7-layer convolutional neural network in TensorFlow to differentiate among six categories of particles observed in urine: bacteria, red blood cells, sperm, white blood cells, crystals, and an "other" category (see Figures 1 and 2). To obtain images at a low cost with a sufficiently high resolution, we use a reversed lens approach. By adding a reversed lens onto the original lens (<$6US for the lenses), we achieve a field-of-view equivalent to the size of the image sensor while maintaining a pixel resolution between 0.9-1.2um/pixel (depending on the pixel density of the image sensor). By combining these approaches, we hope to demonstrate a proof-of-concept of a low-cost cell-counting system for point-of-care applications.



▲ Figure 1: Microscopic images of particles found in urine. These are pre-labeled reference images used to train the convolutional neural network and validate functionality.



▲ Figure 2: The image acquisition device includes a 5-megapixel CMOS image sensor (OV5647), a reversed lens setup, and a jig used to control the distance between the object and the lens.

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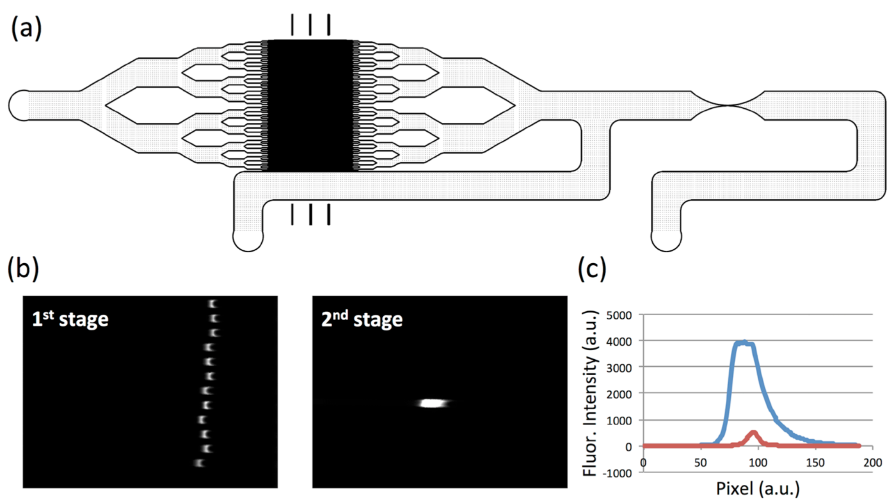
Amplification-Free Nucleic Acid Analysis for Point-of-Care Tuberculosis Diagnostics

W. Ouyang, J. Han
Sponsorship: NIH

Tuberculosis (TB) is one of the world's most widely spread diseases, with one third of the global population being infected. In 2014, 9.6 million people fell ill with TB and 1.5 million died from the disease, 95% of which occurred in developing countries. While a total of 150 millions TB tests (including 80 million point-of-care tests) are ordered each year, most existing TB diagnostic methods—microscopy, culture, or nucleic acid amplification tests—do not match all the Affordable Sensitive Specific User-friendly, Rapid/Robust, Equipment-free, Deliverable (ASSURED) criteria for the resource-poor milieu where most infections occur. In this work, we aim to develop a rapid (<30 min) nucleic acid-based diagnostic platform without engaging the commonly used nucleic acid amplification process, which is expensive, complicated, prone to false positives, and requires trained personnel. This goal will be achieved by a billion-fold microfluidic electrokinetic concentrator that dramatically increases the local concentration of nucleic acids, in which a simple assay is concurrently performed to recognize target nucleic acids with specific sequences.

We have previously demonstrated a microfluidic electrokinetic concentrator that can enrich negatively-charged molecules by ten thousand fold within 15 minutes. We are now working on a multi-stage concentrator that performs a first-stage concentration with thousands of the aforementioned concentrators, followed by a second-stage concentration that collects and concentrates the first-stage concentrated molecules, thereby significantly increasing the overall concentration capability. Our primary results in a two-stage (16-1) concentrator indicates that we could increase the concentration factor from ~10^4 to ~10^5 (Figure 1). We will further scale up by introducing thousands of channels in the first stage to further push the concentration performance. To detect nucleic acid specific to TB, we have developed a mobility shift assay in the concentrator with a limit of detection of ~1 pM. TB patient DNA samples were incubated with a fluorescent complementary DNA probe. During testing in the concentrator, the target-probe and probe formed two separate peaks due to different electrical mobility, enabling us to quantify the level of TB DNA in the sample. By further increasing the concentration capacity of the concentrator, we can hopefully lower the limit of detection to sub-femtomolar.



▲ Figure 1: (a) Design of a two-stage microfluidic electrokinetic concentrator. (b) Fluorescence images of the concentration plugs in the first and second stages. (c) Comparison of the concentration plug in the first (purple) and second (blue) stages.

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Nanofluidic Transport of Molecules in Enamels by Electrokinetic Flows

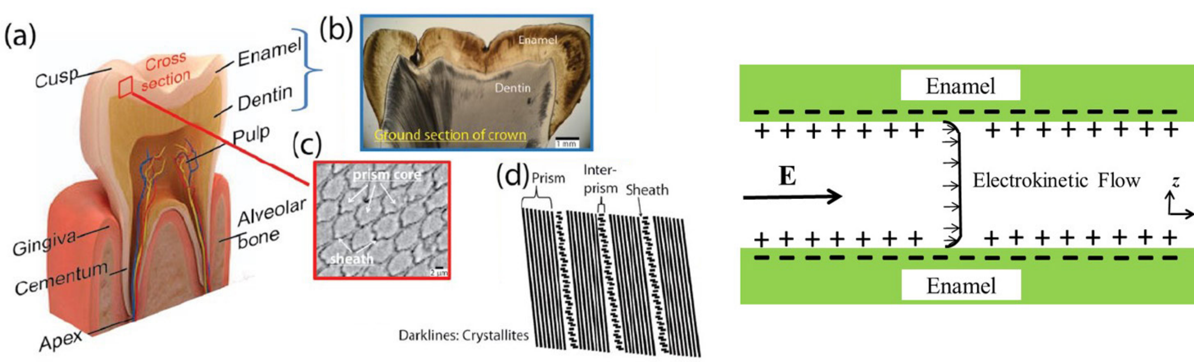
C. Peng, J. Han, in collaboration with H.-Y. Gan, F. Sousa, S. Park, S. J. Lee
Sponsorship: Colgate

The ability to infiltrate various molecules and resins into dental enamel is highly desirable in dentistry, yet transporting materials into dental enamel is limited by the nanometric scale of their pores, as Figure 1 shows. Materials that cannot be infiltrated into enamel by diffusion/capillarity may have molecules that are larger than a critical threshold, perhaps the size of the pores of enamel. It has been demonstrated that electrokinetic flow has been adopted to improve the infiltration of molecules and resin to the dental enamal. Figure 1 shows the preliminary published results of such use of electrokinetic flow to infiltrate enamel.

In the current work, the enamel ground sections are prepared by removing dentin from the tooth ground sections and seated in the microfluidic platform. We study the infiltration of different ion molecules such as Ca^{2+}, K^{+}, and Na^{+} into the enamel nanopores by using electrokinetic flows. We have demonstrated that the fluorescence probes binding to the specific ions have been transported through the enamel. Meanwhile, the current change in this process has been monitored, and it shows that the current increases during the infiltration due to the increasing overall conductivity. Laser scanning confocal microscope images of the enamel cross-section demonstrate that the fluorescence probes binding to the ions have infiltrated into the nanopores of the enamel. Micro-hardness tests (Vickers) and nano-indentation trials have been carried out by our collaborators on trial samples of both whole teeth and grounded sheets of enamel.

We study the improved health of the whole tooth due to use of resin infiltration using electrokinetics, which will be a big boost to clinical care in the near future. This study is the first demonstration that resin can be infiltrated through the enamel and dentin nanopores. By using laser scanning confocal microscopy, fluorescence microscopy, mass spectroscopy, and ion selective electrode technique, we will test how the F^{-}, Na^{+}, K^{+}, and Ca^{2+} ions infiltrate into the teeth. Micro-hardness and chemical resistance of the teeth after the resin polymerization will be tested. This will be a very promising technique to improve dental health in a very short time and will shed light on future *in vivo* utility in the clinic. This technique might be a solution to the weak bonding between filling resin and pulp-dentin-enamel surfaces after treatment of cavities.

This study opens opportunities to use a new biomedical technique in dental applications and may find utility in clinical dental treatments.



▲ Figure 1: Diagram of enamel and its pores. (a) Anatomy of a mature human tooth. (b) Light microscopy image of ground section of tooth crown showing enamel, dentin, enamel-dentin junction, and an outline of enamel prisms. (c) Cross section of enamel prisms showing prism core and sheaths, and (d) Line drawing of hydroxyapatite crystallites as oriented in prismatic and interprismatic enamel separated by prism sheaths. Right: Schematic of electrokinetic flow inside the enamel nanopores.

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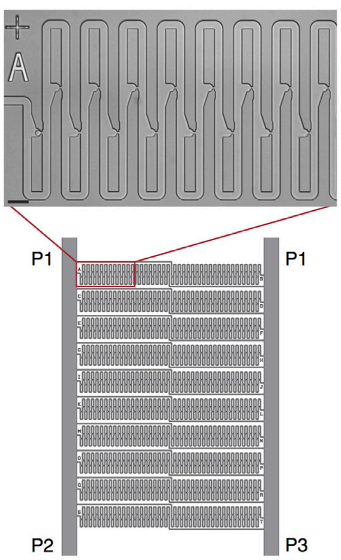
A Microfluidic Platform Enabling Single-Cell RNA-seq of Multigenerational Lineages

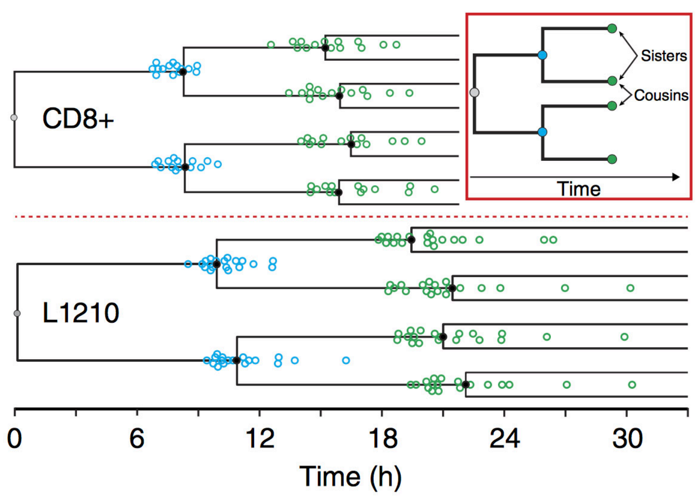
R. J. Kimmerling, G. L. Szeto, J. W. Li, A. S. Genshaft, S. W. Kazer, K. R, Payer, J. Borrajo, P. C. Blainey, D. J. Irvine, A. K. Shalek, S. R. Manalis
Sponsorship: NIH

We introduce a microfluidic platform that enables off-chip single-cell RNA-seq after multi-generational lineage tracking under controlled culture conditions. We use this platform to generate whole-transcriptome profiles of primary, activated murine CD8+ T-cell and lymphocytic leukemia cell line lineages. Here we report that both cell types have greater intra- than inter-lineage transcriptional similarity. For CD8 + T-cells, genes with functional annotation relating to lymphocyte differentiation and function—including Granzyme B—are enriched among the genes that demonstrate greater similarity of intra-lineage expression level. Analysis of gene expression covariance with matched measurements of time since division reveals cell type-specific transcriptional signatures that correspond with cell cycle progression. We believe that the ability to directly measure the effects of lineage and cell cycle-dependent transcriptional profiles of single cells will be broadly useful to fields where heterogeneous populations of cells display distinct clonal trajectories, including immunology, cancer, and developmental biology.

Our platform utilizes an array of hydrodynamic traps within a fluidic design optimized to capture and culture single cells for multiple generations on-chip (Figure 1). These trap structures rely on differences in hydrodynamic resistance between the trapping pocket and a bypassing serpentine channel to deterministically capture single cells. Given these differences, media can be rapidly and continuously perfused through the bypass channels while maintaining minimal flow across the traps in order to ensure constant nutrient repletion with low and uniform shear stress on the cells. This independent flow control also allows for rapid buffer exchange without dislodging trapped cells, thus enabling on-chip implementation of standard cell staining techniques such as immunocytochemistry and fluorescent labeling. Single cells were cultured for two generations on-chip before release for sequencing. This allowed us to define sister and cousin cell pairs for each lineage (Figure 2).



▲ Figure 1: Schematic representation of the hydrodynamic trap array consisting of 20 lanes of traps (inset shows an optical micrograph of a single trapped cell—scale bar, 20 μm).



▲ Figure 2: Overlay of lineage trees from single CD8+ T cells (n=15) and L1210 cells (n=20) established with time-lapse imaging in the hydrodynamic trap array. As a demonstration of lineage construction, one lineage for each cell type (black circles) has connecting lines indicating familial history.

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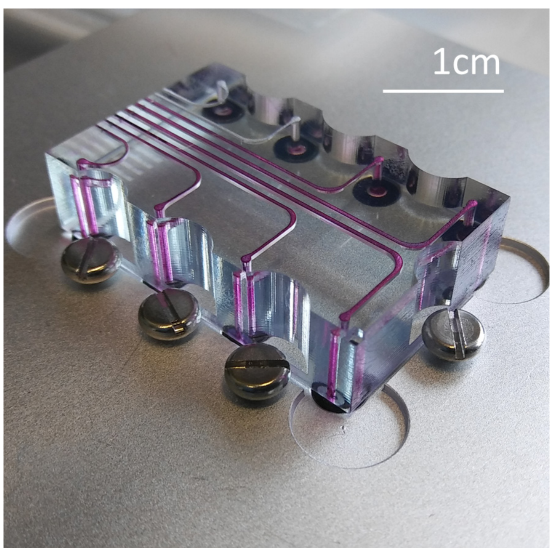
3-D Printed Microfluidics for Modelling Tumor Microenvironments

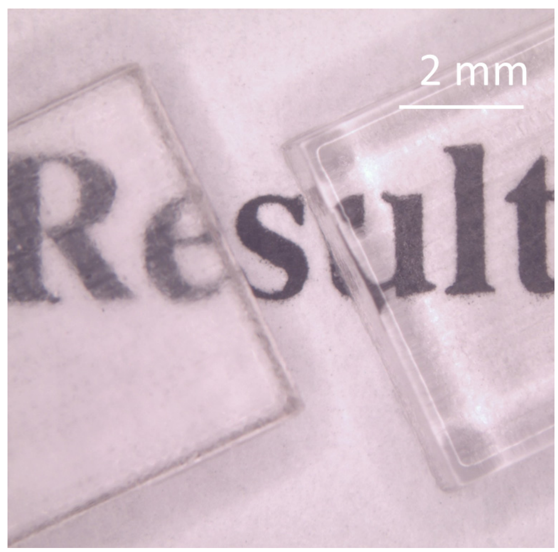
A. L. Beckwith, J. T. Borenstein, L. F. Velásquez-García
Sponsorship: The Charles Stark Draper Laboratory, Inc.

Microfluidic devices show promise as enablers of the exploration, development, and customization of medical treatments beyond traditional capabilities while saving time and cost. However, one of the principal barriers to broad application of microfluidic technologies in healthcare is related to the inherent challenges in device fabrication. Soft lithography approaches are generally restricted to planar, simple geometries and a few material options and are prone to large device-to-device dimensional variation. Current manufacturing methods for complex microfluidic devices, e.g., multi-substrate bonded micromachining, are technically challenging, time-intensive, and constrained by existing microfabrication capabilities that affect the fabrication yield. 3-D printing has the potential to significantly reduce the cost and time to manufacture microfluidics while maintaining a required level of device functionality. Additionally, 3-D printing enables rapid iteration of device designs and construction of complex microchannel features that may otherwise be difficult, impractical, or unfeasible to attain.

In this project, we are developing a Tumor Analysis Platform (TAP) that mimics interactions between tumors and the immune system in the human body, providing a microenvironment for testing the effectiveness of drugs. This microfluidic system is capable of testing treatments on tumors directly from the patient in a laboratory model to determine which therapies most effectively kill that patient's cancer. We are investigating digital light projection/stereolithography (DLP/SLA) to fabricate complex monolithic microfluidic devices that are transparent, non-cytotoxic, compatible with commonly used sterilization procedures, and, in general, suitable for biological applications. Current research has focused on exploring the biocompatibility, optical properties, minimum feature size resolution, and manufacturing repeatability of different printable materials (Figures 1 and 2). Future work will focus on implementing and characterizing different TAP designs.



▲ Figure 1: SLA 3-D printed channels with rectangular cross-sections. Channel widths as small as 275 μm were successfully printed and filled with red dye.



▲ Figure 2: Chip of 3-D printed material evidencing high transparency to visible light.

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Integration of Nanofluidics in Commercial CMOS

H. Meng, J. Kim, A. Atabaki, R. Ram
Sponsorship: Bose Corporation

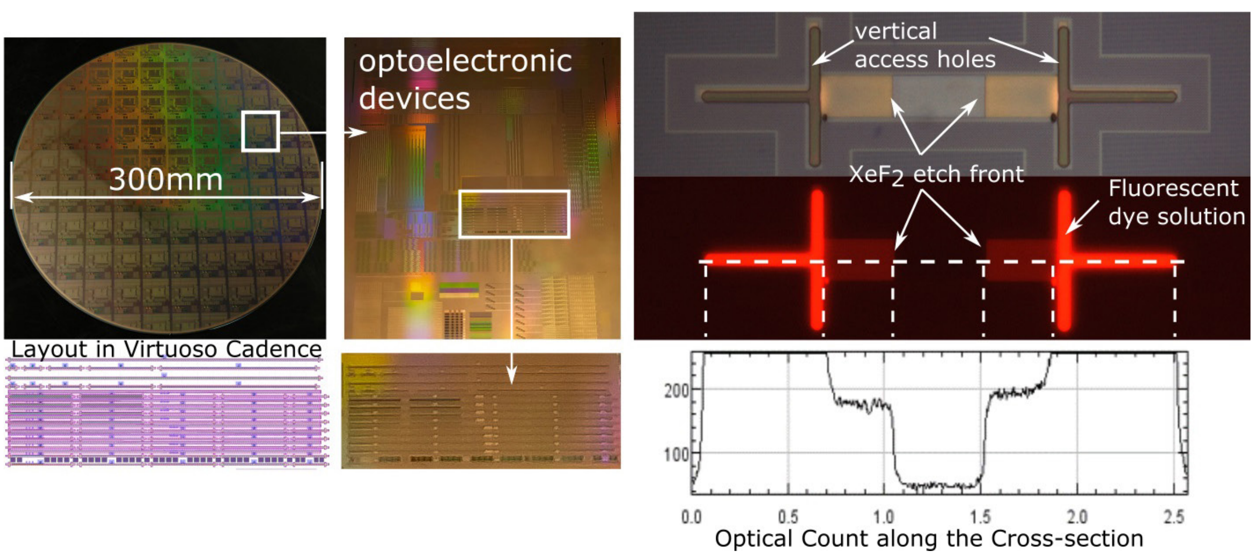
Lab-on-complementary-metal-oxide-semiconductor (CMOS) is an emerging platform for bio-sensing applications. Integration of various sensors and active circuits into a single CMOS chip provides benefits including ultra-compact form factor, enhanced signal collection efficiency, reduction of noise and massively parallel sensing. Nanofluidics offers the ability to engineer systems with comparable complexity and scale to biomolecules and opens the door to a new generation of molecular tools. A novel approach to leverage the precision and scale of CMOS to integrate nanofluidics, nanophotonics, and nanoelectronics on the same platform is presented.

Nanofluidic channels are integrated within a modified IBM 65-nm (10LP) CMOS process. The nanofluidics are introduced by sacrificial etching of the polysilicon typically used for the transistor gate, for local interconnection, and for precision resistors. The polysilicon can be patterned at the critical dimension of the process (65 nm in our case), and the polysilicon features are routinely placed with an accuracy of approximately 1 nm. This polysilicon can be placed either over a gate oxide and silicon or over a silicon dioxide isolation layer.

As shown in Figure 1, the devices are fabricated in a 300-nm wafer, with a die size around 25mm x 30mm. Microelectronic devices are integrated alongside the nanochannels. Photolithography and reactive ion etching are used to access the polysilicon through the metal interconnect stack. Nano-channels are etched by gas phase XeF_2 through these access holes. Due to extreme high extinction ratio of XeF_2, it is possible to etch high aspect ratio channels.

SU-8 is used to pattern fluid reservoirs on top of CMOS chips. As shown in Figure 1, by loading fluorescent dye (Texas Red), it is possible to demonstrate (a) the wetting properties of the XeF_2 etched channels and (b) the relatively low autofluorescence of the inter-metal dielectric stack.

In summary, we present the first attempt to fabricate nanofluidic channels in microelectronics CMOS chips using the polysilicon in the transistor gate as a sacrificial layer. Fluorescent molecules dissolved in water can be easily loaded into the channels and imaged with signal strength significantly over the autofluorescence of the CMOS dielectric stack.



▲ Figure 1: Nanofluidics fabricated in a bulk 65-nm CMOS process on the same chip are active optoelectronic devices. The layout uses parameterized cells in Virtuoso Cadence. The nanochannel is successfully wetted by water based solution and a clear signal is visible above the autofluorescence.

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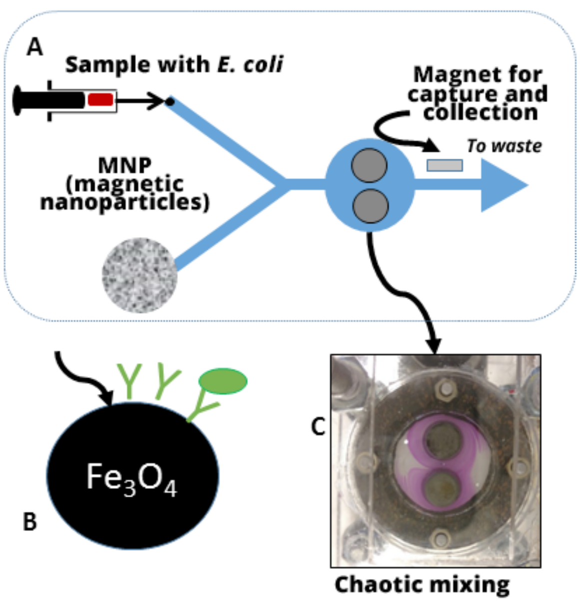
Capture and Concentration of Pathogens in Chaotic Flows

M. M. Alvarez, G. Trujillo de Santiago, E. Fernández-Castillo, A. Risso, G. Prakash, P. I. Sánchez-Rellstab,
A. Khalilpour, A. Khademhosseini
Sponsorship: MIT- Tecnológico de Monterrey Nanotechnology Program

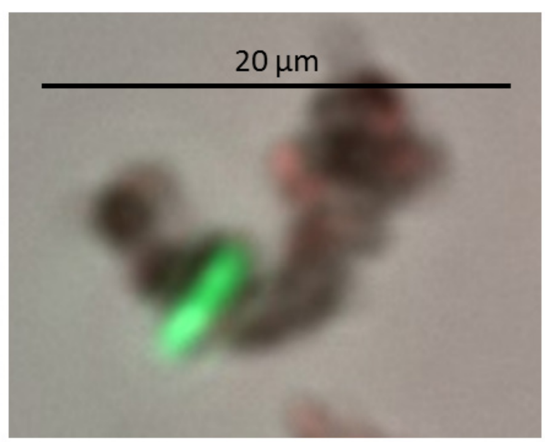
Infectious diseases of both viral and bacterial origin continue to be a health threat to millions of people in developed and underdeveloped countries. One successful treatment strategy for cases of sepsis or viral infections is the effective capture and removal of the pathogenic agent from the bloodstream. We are presently developing filter-less technologies for the direct capture of bacteria (i.e., *Escherichia coli*) and eventually viruses (i.e., Ebola virus-like particles).

We use a portable system for the capture of pathogens circulating through a microfluidic chamber. The system (Figure 1A) is based on the specific recognition of proteins on membranes or capsids; it integrates the use of (a) anti-pathogen polyclonal antibodies, (b) magnetic nanoparticles (MNP), (c) a microfluidic chaotic flow system, and (d) a neodymium magnet. Anti-pathogen antibodies are covalently immobilized within commercial magnetic nanoparticles to fabricate nanoparticles that will bind pathogens (Figure 1B). Our experiments compare the performance of different immobilization strategies (amino-carboxylic covalent binding and streptavidin-biotin binding) and different magnetic nanoparticle sizes (range 30 nm - 800 nm).

The heart and distinctive feature of our system is a microfluidic chamber in which the binding particles and the pathogen are mixed by the action of a laminar chaotic flow produced by the alternating rotation of two cylinders (Figure 1C). The intimate contact induced by this chaotic laminar flow promotes the capture of the pathogen by individual nanoparticles or nanoparticle clusters. The trapped pathogens are then concentrated by a simple magnet located downstream from the microchamber (Figure 2). This platform has key advantages over currently available methods, which are mostly based on the use of microfluidic channels or filtering membranes: (a) it is faster, (b) it offers superior capture due to the intimate mixing induced by the chaotic flow, and (c) it is easy to use.



▲Figure 1: Experimental system. (a) Microfluidic system for the capture and concentration of pathogen particles (i.e., *E. coli* expressing green fluorescent protein), (b) NMP functionalized with anti-*E. coli* antibodies, (C) A chaotic flow system: the blinking vortex.



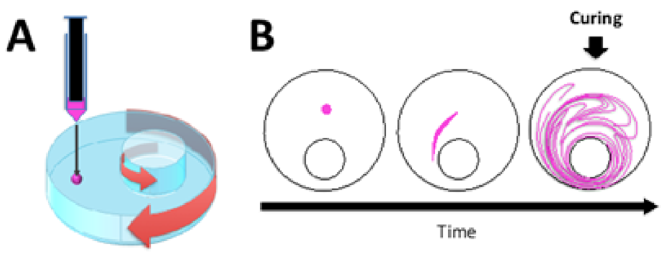
▲Figure 2: Fluorescent *E. coli* bacteria captured and concentrated in NMPs.

3-D Chaotic Printing

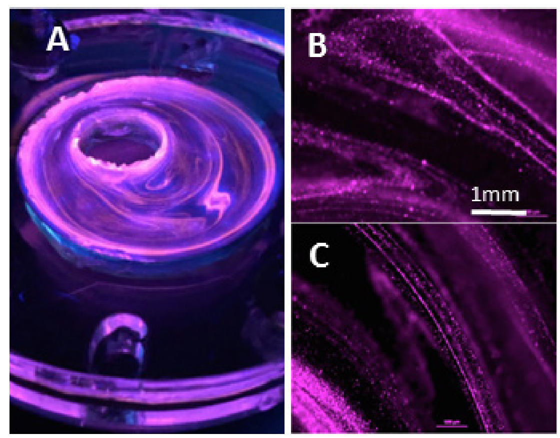
G. Trujillo-de Santiago, M. M. Alvarez, M. Samandari, G. Prakash, G. Chandrabhatla, B. Batzaya, P. P. S. S. Abadi, S. Mandla, R. Avery, A. Nasajpour, N. Annabi, Y. S. Zhang, A. Khademhosseini
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program, CONACyT, Fundación México en Harvard

Chaos has the ability to create complex and predictable structures. We use simple chaotic flows for the fabrication of complex 3-D microstructures in cross-linkable or curable liquids, using a process that we refer to as 3-D chaotic printing. We inject a drop of ink (i.e., a drop of a miscible liquid, fluorescent beads, or cells) into a viscous Newtonian liquid and then apply a chaotic mixing recipe. This generates a complex microstructure in just a few flow applications (Figure 1). This structure is then preserved with high fidelity and reproducibility by rapid crosslinking or curing of the material. The 3-D structure is the result of the rapid alignment of the injected material to the flow manifold (Figure 2). Therefore, its main features are reproducible and the overall process of fabrication is quite robust. Moreover, since the process is deterministic, it is amenable to computational modeling using computational fluid dynamics.

We currently explore applications for this technology, including the rational reinforcement of constructs by the chaotic alignment of cells and nanoparticles, the fabrication of cell-laden fibers, the development of highly complex multi-lamellar and multi-cellular tissue-like structures for biomedical applications, and the fabrication of bioinspired catalytic surfaces.



▲ Figure 1: Scheme of 3-D chaotic printing: a strategy to fabricate micro-patterned constructs using cross-linkable polymers and chaotic flows (i.e., the Journal Bearing flow), (a) a drop of "ink" (i.e., microparticles, nanoparticles, cells) is dispensed in a chaotic system, (b) after the iterative application of a chaotic recipe, a fine and complex microstructure emerges. Exposure to a curing agent freezes this microstructure.



▲ Figure 2: A PDMS construct with pink fluorescent miroparticles showing a fine chaotic micropattern using the Journal Bearing flow, (a) overall view of the construct, (b & c) close-up showing the fine microstructure resulting from the application of the chaotic flow.

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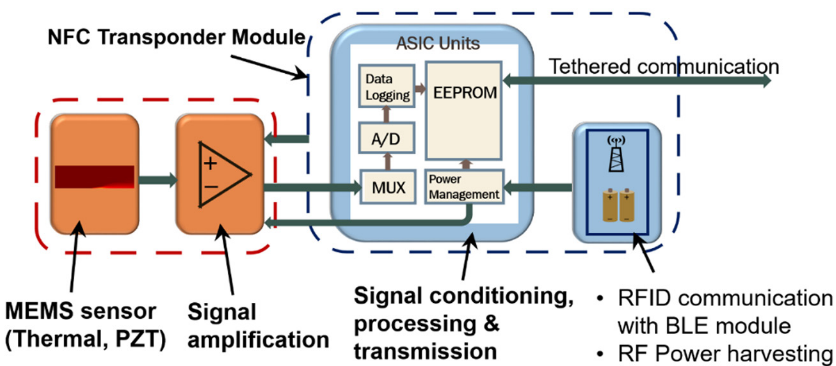
Thin-Film Transistors for Implantable Medical Devices

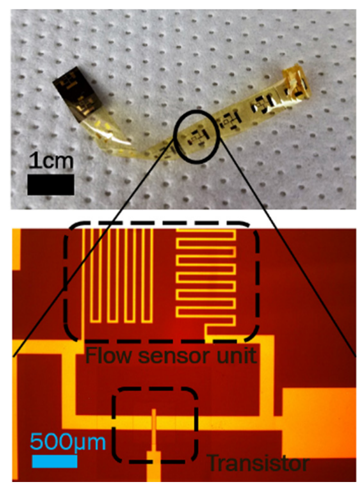
Y. Hosseini, L. F. Velásquez-García, D. S. Boning
Sponsorship: TruSpine

Miniaturization and implantation of medical devices with the ability to monitor vital body parameters can enable new opportunities for medical procedures. The implantable medical devices market is estimated to grow at 5.5% compound annual growth rate (CAGR) to reach a $55B size market by 2025. In this regard, flexible hybrid electronic systems have gained attention during the last several years for deployment on various platforms such as smart lenses, cardiac implants, and brain implants, as well as in wireless modules for communication systems integrated with these implants.

In this project, we are exploring the integration of various microsystems such as sensors, thin-film transistors (TFTs), silicon microelectronics, and radio frequency identification (RFID) modules on flexible platforms (Figure 1). The goal of this project is to fabricate the essential components of these systems in a single process to reduce the integration complexity for implementing different technologies. Our initial work has focused towards integration of TFT electronics and thermal sensors on a polyimide substrate for flow sensing applications. The TFT is fabricated as a back-gate transistor, with aluminum oxide as gate insulator and indium-gallium-zinc-oxide (IGZO) as n-type channel. The thermal flow sensor consists of a combination of a heater and a resistance temperature detector (RTD) system. The thermal flow sensor consists of Au electrodes and is the extension of one of the transistor metal layers (Figure 2). This metal layer can be further extended to serve as a signal path, bonding pad, and RFID coil. Current work focuses on characterizing, optimizing, and addressing the reliability issues related to the operation of these TFTs for signal conditioning for sensing applications.



▲ Figure 1: The design outlook for integrated microsystems for sensing applications for implantable medical devices.



▲ Figure 2: TFTs on a flexible platform with inset image showing the integrated thermal flow sensor connection to the electronic system.

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Building Synthetic Cells for Sensing Applications

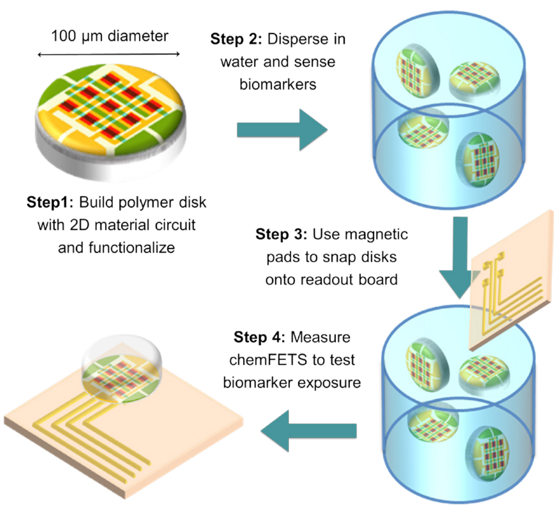
M. Hempel, E. McVay, J. Kong, T. Palacios
Sponsorship: AFOSR

Miniaturized sensors equipped with communication capabilities enable a new paradigm of sensing in areas such as health care and environmental monitoring. For example, instead of a patient measuring blood sugar by pricking a finger and analyzing a drop of blood externally, a microscopic sensor platform in the blood stream could sense the glucose concentration internally and communicate data to the outside world non-invasively.

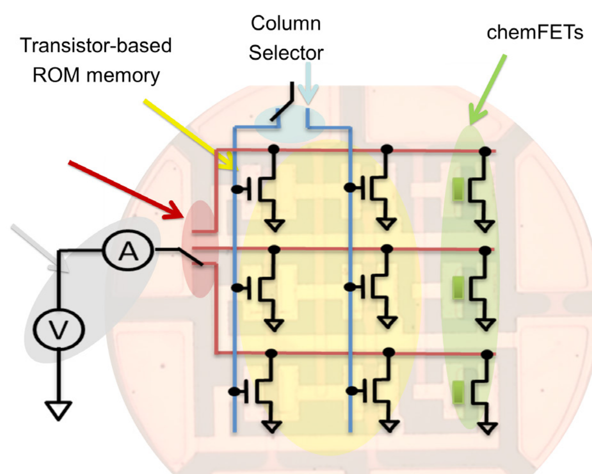
In this project, we work towards this vision by developing a microscopic sensor platform, called a synthetic cell (SynCell) that can sense chemical substances in liquid media. The concept of our first SynCell demonstration is shown in Figure 1. After fabrication, the SynCells are lifted off and dispersed in water. Upon exposure to a specific substance, the chemical sensors onboard the SynCell are designed to permanently change their electrical resistance. Later on, they will be retrieved by using magnetic pads and analyzed externally.

To realize this concept, we designed 100-um-wide flexible polymer disk that has three chemical sensors, a stored ID number in the form of ROM transistors, and integrated magnetic readout pads as shown in Figure 2. The transistor channels and sensors are made of a single atomic layer of molybdenum disulfide (MoS_2), which is a perfect material for this application because it is flexible and easy to integrate into membrane-like electronics. Furthermore, it is an excellent material to build digital electronics and very sensitive sensors.

With our first iteration of the SynCells, we demonstrated functional transistors and developed a process to lift the disks off the fabrication substrate and disperse them in solution. We also showed the ability to manipulate the SynCells with external magnetic fields. In the next steps, we want to show fully functional SynCells and demonstrate the ability to magnetically retrieve them.



▲ Figure 1: SynCell concept of sensing an analyte in a liquid environment. After chemical exposure, the SynCell will be retrieved by magnetic pads and measured externally.



▲ Figure 2: The Syncell consists of 3 chemically sensitive transistors, as well as 6 transistors that give the cell a unique ID number for identification.

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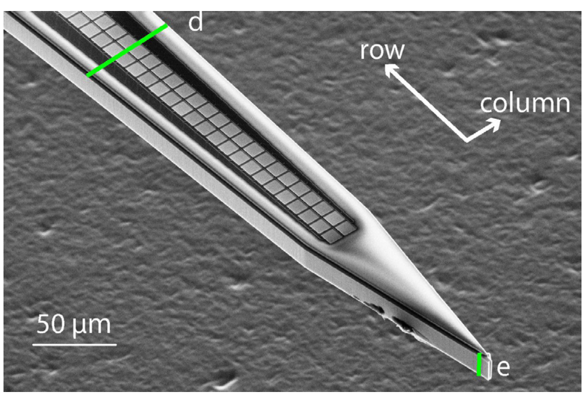
Close-Packed Silicon Microelectrodes for Scalable Spatially Oversampled Neural Recording

J. Scholvin, K. Payer, C. G. Fonstad, E. S. Boyden
Sponsorship: Simons Center for the Social Brain at MIT, Paul Allen Family Foundation, NYSCF, NIH, NSF, CBMM

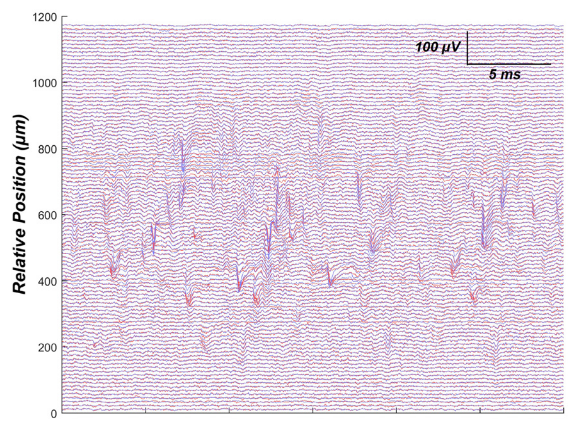
Two major goals of neuroscience are to understand how the activity of individual neurons yields network dynamics and how network dynamics yields behavior (and causes disease states). Reaching this goal requires innovative neuro-technologies with orders-of-magnitude improvements over traditional methods. Nanofabrication can provide the scalable technology platform necessary to record with single-spike resolution the electrical activity from a large number of individual neurons, in parallel and across different regions of the brain. By combining innovations in fabrication, design, and system integration, we can scale the number of neural recording sites: from traditionally a small number of sparse sites, to currently over 1000 high-density sites, and in the future beyond many thousands of sites distributed through many brain regions.

We designed and implemented close-packed silicon microelectrodes (Figure 1) to enable the spatially oversampled recording of neural activity (Figure 2) in a scalable fashion, using a tight continuum of recording sites along the length of the recording shank, rather than discrete arrangements of tetrode-style pads or widely spaced sites. This arrangement, thus, enables spatial oversampling continuously running down the shank, so that sorting of spikes recorded by the densely packed electrodes can be facilitated for all the sites of the probe simultaneously.

We use MEMS microfabrication techniques to create thin recording shanks and a hybrid lithography process that allows a dense array of recording sites, which we connect to with submicron-dimension wiring. We have performed neural recordings with our probes in the live mammalian brain. Figure 2 illustrates the spatial oversampling potential of closely packed electrode sites.



▲ Figure 1: Close-up view of the tip section of a recording shank, showing the two columns and a dense set of rows. The close-packed pads are visible as light squares in the center of the shank. Insulated metal wires connect to the individual sites, running next to the recording sites along length of the shank, visible as dark lines flanking the rows of light squares. The shank itself has a width of ~50-60 µm in the region shown (d), and is 15 µm thick (e).



▲ Figure 2: Example of *in vivo* data from a 2-column by 102-row shank. The spatial oversampling enables spikes to be picked up by many nearby recording sites (9 x 9-µm pads, at a 10.5-µm pitch), to facilitate automated data analysis. The data shown here is a snapshot of data collected by a multi-shank, 1020-channel device.

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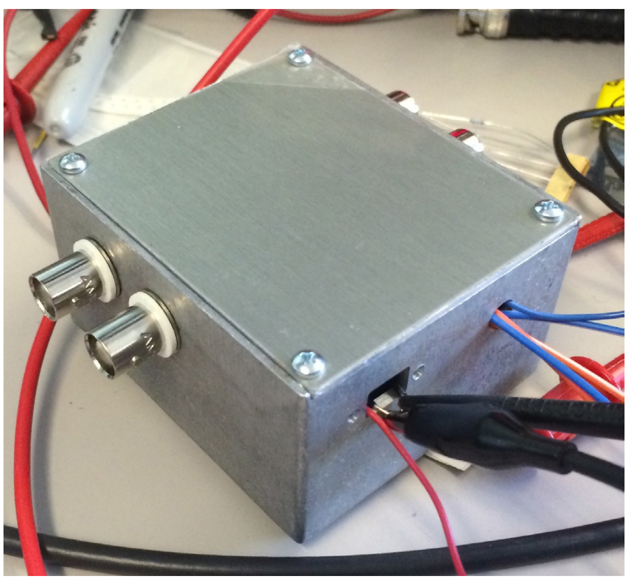
A Portable Bioimpedance Spectroscopy Measurement System for Congestive Heart Failure Management

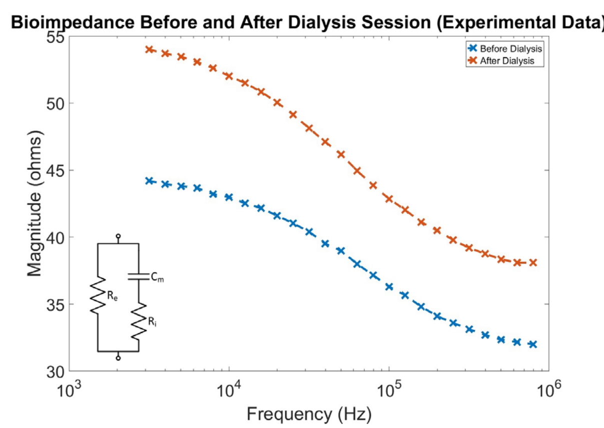
M. K. Delano, C. G. Sodini
Sponsorship: MEDRC, Analog Devices, Inc.

Congestive heart failure (CHF) is a chronic medical condition that causes reduced exercise tolerance; shortness of breath; and fluid buildup in the lungs, legs, and abdomen. The disease must be managed carefully to prevent hospitalizations. While CHF-related mortality has reduced in recent years, this reduction has been accompanied by an increase in hospitalizations and readmissions. A home monitoring and management system for patients with CHF could help reduce the number of CHF-related hospitalizations and reduce the impact of CHF on the United States healthcare system.

We have developed a portable (and eventually wearable) bioimpedance spectroscopy system (BIS) to monitor fluid status levels of patients at the calf via a wearable compression sock. Our system has been evaluated in the lab and with healthy volunteers, and we are in the process of testing the system alongside a commercial BIS system (SFB7) in the hemodialysis unit at MGH to measure volume change. A wearable CHF home management system that includes our BIS system, coupled with self-tracking tools and behavior change concepts, could empower patients to more easily manage their condition and reduce the likelihood of (re)hospitalization.



▲Figure 1: The portable bioimpedance spectroscopy measurement system inside the enclosure.



▲Figure 2: Bioimpedance spectra for a dialysis patient before (blue) and after (red) their session. Increased impedance at low frequencies implies increase Re (extracellular resistance) and decreased edema.

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Wearable and Long-Term Subdermal Implantable Electroencephalograms

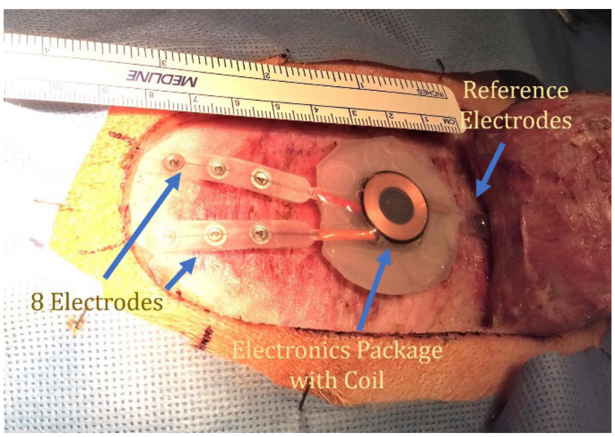
J. Yang, C. G. Sodini
Sponsorship: CICS

Electroencephalography (EEG) has long been used by neurologists to aid in diagnosing and treating neurological disorders ranging from sleep apnea to epilepsy. EEG can also be used as a quantitative measure of the depth of anesthesia for intensive care unit (ICU) monitoring. However, inherent difficulties still exist in capturing EEG data for extended periods of time on the order of days to weeks in humans. Such difficulties due to implementation challenges and usability lead to patient non-compliance. These challenges also curtail EEG use in clinical ICU settings due to the complexity of the setup.

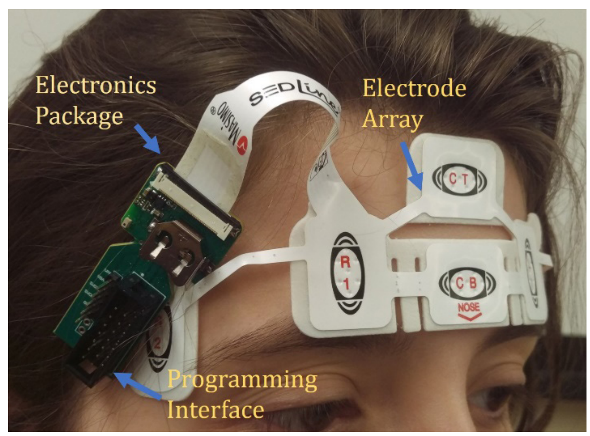
This work aims to address these issues by extending the functionality and performance of a previously designed EEG ASIC. A design for a subdermal, implantable EEG recording system for long-term EEG monitoring as well as a simplified wearable EEG sensor is realized.

The implantable design is an 8-channel, 250Hz bandwidth EEG system in a 14.0mm x 15.5mm package that is wirelessly powered by an external device through inductively coupled coils with backscattering. The device is placed subdermally above the skull for continuous patient EEG monitoring for up to a month to aid neurologists with epilepsy diagnosis. This device is especially important given the severity of antiepileptic drugs' side effects. The performance of this device is verified through animal studies in pigs.

This work is also extended to the design of a wearable, wireless EEG patch for clinical settings. The device is a 20mm x 24mm, 4-channel, 250Hz bandwidth, Bluetooth low-energy (BTLE) electronics package with adhesive electrodes that can be quickly applied. This device is aimed to assist neurologists and anesthesiologists to titrate anesthetic drugs as well as more accurately monitor depth of anesthesia in operating room settings. Results are verified using patient data in clinical settings.



▲ Figure 1: Subdermal EEG device being implanted into a live pig model. The 8 electrodes point towards the nose of the pig; ground and reference electrodes point towards the back.



▲ Figure 2: Wearable EEG device with programmer interface board attached. The device is adhered to the user's forehead by adhesive electrodes.

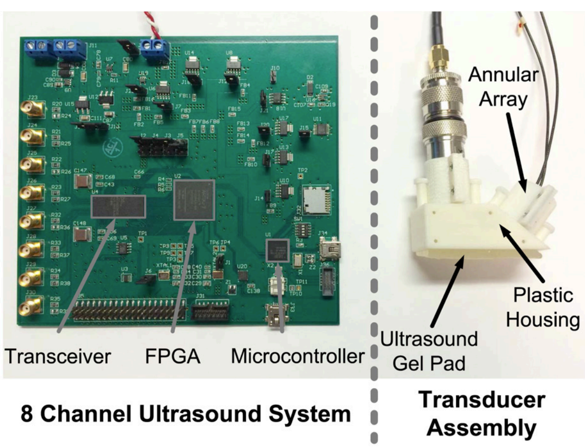
Continuous and Non-Invasive Arterial Pressure Waveform Monitoring using Ultrasound

J. Seo, C. G. Sodini, H.-S. Lee
Sponsorship: Samsung Fellowship, MEDRC, Phillips

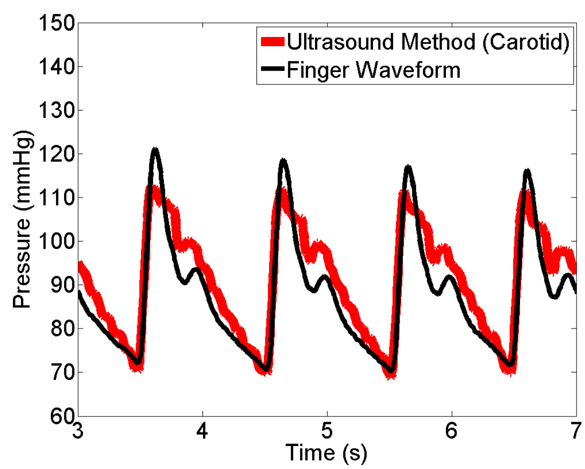
An arterial blood pressure (ABP) waveform provides valuable information for understanding cardiovascular diseases. The ABP waveform is usually obtained through an arterial line in an intensive care unit (ICU). Although considered the gold standard, this method brings the disadvantage of its invasive nature. Non-invasive methods based on vascular unloading, such as Finapres, are not suitable for prolonged monitoring due to their obstructive nature. Therefore, reliable non-invasive ABP waveform estimation has long been desired by medical communities. Medical ultrasound is an attractive imaging modality because it is inexpensive, free of ionizing radiation, and suitable for portable system implementation.

The proposed ultrasonic ABP waveform monitoring is achieved by observing the pulsatile changes of the cross-sectional area and identifying the elastic property of the arterial vessel, represented by the pulse wave velocity (PWV; the propagation speed of a pressure wave along an arterial tree) with a diastolic blood pressure measurement as a baseline. The PWV can be estimated by obtaining a flow-area plot and then measuring the slope of an initial linear region in the flow-area plot during a reflection-free period (e.g. the early systolic stage).

A prototype ultrasound device was designed to obtain a blood flow waveform and a diameter waveform simultaneously to implement the proposed technique as shown in Figure 1. A pre-clinical test was conducted on nine healthy human subjects to demonstrate the proof of concept. Figure 2 presents the comparison between the ABP waveform obtained at the middle finger with Finapres and the ABP waveform at the left common carotid artery from the prototype. The sharper ABP peaks from the Finapres are expected due to the reflection at the peripheries. Currently, the clinical study in comparison to the gold standard A-line measurement in the ICU at the hospital is being prepared.



▲Figure 1: The prototype ultrasound system and transducer assembly. The system is capable of a sufficient data rate to display blood flow and arterial pulsation simultaneously. Ultrasound gel pad is utilized to achieve acoustic coupling between the transducer surface and the skin.



▲Figure 2: Comparison of the estimated carotid ABP waveform to the finger ABP waveform. The finger waveform shows a sharper systolic peak due to pulse pressure amplification at peripheral arterial sites. Diastolic pressures from both methods are aligned.

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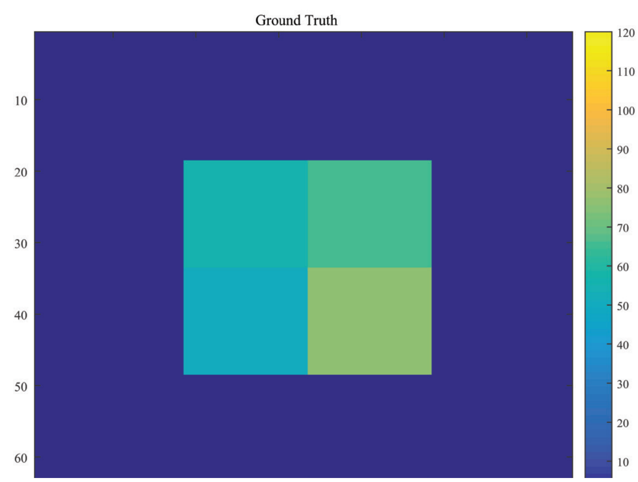
Three-Dimensional, Magnetic Resonance-Based Electrical Properties Mapping

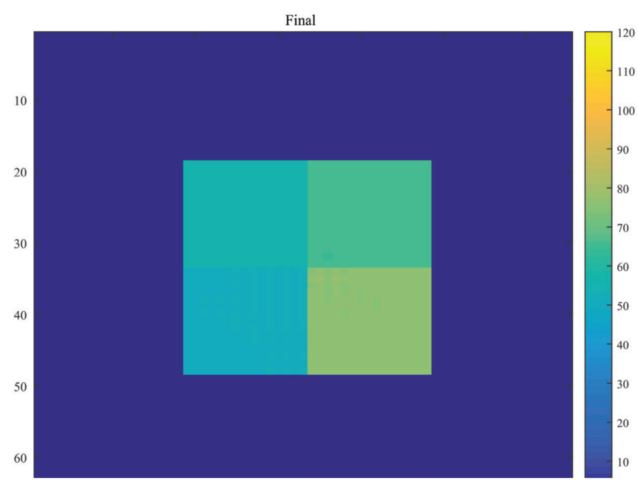
J. E. C. Serrallés, A. G. Polimeridis, R. Lattanzi, D. K. Sodickson, J. K. White, L. Daniel
Sponsorship: NSF

Magnetic resonance imaging (MRI) has proven to be a safe and versatile tool in medical practice and clinical research. Clinical MRI typically relies on magnetization, T1-weighting, and T2-weighting as its contrast mechanisms. The dependence on these mechanisms is disadvantageous because these quantities are not guaranteed to vary from tissue to tissue, potentially obscuring the true contrast of the tissues. Additionally, the use of magnetization discards valuable information that describes how the scatterer interacts with fields generated by a scanner. The aim of our research is instead to use this extraneous information to generate maps of relative permittivity and conductivity, thereby significantly increasing contrast in MR images at the expense of computation time.

The task of inferring these material properties is referred to as inverse scattering, a subclass of what are called inverse problems. Inverse scattering problems typically suffer from slow convergence rates and require several full-wave electromagnetic simulations per iteration of the procedure. Our approach, called Global Maxwell Tomography, uses a volume integral equation suite, MARIE, which is custom-tailored for the typical MR setting and which results in runtimes that render the inference process tractable. Our algorithm is capable of reconstructing the known electrical properties of objects, in simulation, with use of measured MR data on the horizon. The ability to infer electrical property maps rapidly from MR data would not only improve the reliability of MRI but also pave the way for applications like automated tumor identification, patient-specific MR shimming, and real-time monitoring of heat deposition in tissue by MR coils, among others.



▲ Figure 1: Relative permittivity map of phantom with known electrical properties and geometry, along a central slice. This constitutes the ground truth to which the algorithm should converge.



▲ Figure 2: Reconstructed relative permittivity map of the same phantom, when starting from a completely homogeneous initial guess. Reference fields are generated in simulation.

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MARIE: A MATLAB-Based Open Source MRI Electromagnetic Analysis Software

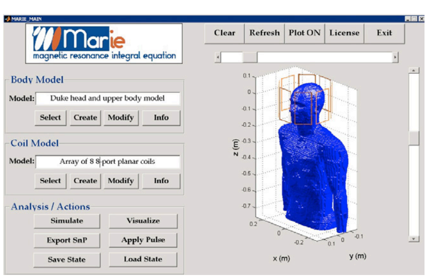
J. F. Villena, A. Polimeridis, J. E. C. Serralles, L. Wald, E. Adalsteinsson, J. White, L. Daniel
Sponsorship: NIH, Skoltech Initiative on Computational Mathematics

Our Magnetic Resonance Integral Equation suite (MARIE) is a numerical software platform for comprehensive frequency-domain fast electromagnetic (EM) analysis of MRI systems. The tool is based on a combination of surface and volume integral equation formulations. It exploits the characteristics of the different parts of an MRI system (coil array, shield, and realistic body model), and it applies sophisticated numerical methods to rapidly perform all the required EM simulations to characterize the MRI design: computing the un-tuned coil port parameters, obtaining the current distribution for the tuned coils, and obtaining the corresponding electromagnetic field distribution in the inhomogeneous body for each transmit channel.

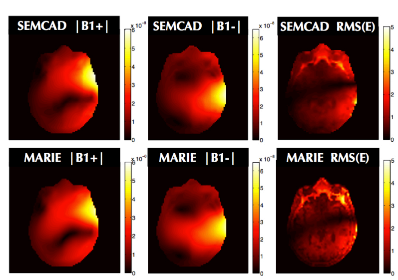
The underlying engine of MARIE is based on integral equation methods applied to the different domains that exist in traditional MRI problems (for example, except in interventional cases, the coil and body occupy separate spaces). The natural domain decomposition of the problem allows us to apply and exploit the best modeling engine to each domain. The inhomogeneous human body model is discretized into voxels and modeled by volume integral equation (VIE) methods. The homogeneous conductors that form the coil design and shield are tessellated into surface triangles (that allow the modeling of complex and conformal geometries), and modeled by surface integral equation (SIE) methods. Both models are coupled by applying standard dyadic Green functions. Due to the nature of integral equation methods, there is no need to model or discretize the surrounding air or non-electromagnetic materials, although the solution fields can be computed anywhere outside the discretized domain by applying the same free-space Green functions. No boundary condition needs to be defined (integral equations satisfy the radiation condition by construction), which simplifies the setting of the problem for the user: the inputs are the voxelized definition of the inhomogeneous body model, the tessellated geometry of the coil design (which the external ports defined), and the frequency of operation.

Once the models are generated, fast numerical methods are applied to solve the complete system. A set of nested iterative methods with the appropriate preconditioning is used to solve the effect of each port. Fast Fourier transform (FFT) techniques exploit the regularity of the voxelized grid and accelerate the matrix vector products. Depending on the different scenarios for analysis, some numerical models or tasks can be pre-computed to accelerate the solution, and many strategies are used to reduce either computational time or memory consumption.

The software runs on MATLAB and is able to solve a complex scattering problem in ~2-3 min. on a standard single GPU-accelerated windows desktop machine. On the same platform, it can perform a frequency sweep of a complex coil in ~3-5 min. per frequency point. Furthermore, it can solve the complete inhomogeneous body and coil system in ~5-10 min. per port, depending on the model resolution and error tolerance required. Intended to be a development platform, it includes a simple and intuitive graphic user interface (see Figure 1 for a snapshot) for standard analysis and a set of well-documented scripts to illustrate how to use the core numerical functions to perform more advanced analyses, to allow experienced users to create their own analysis by using or modifying the existing code. The input of the body is voxel-based and can be read from simple files that define position and tissue properties. The input of the coil design is based on standard triangular geometric descriptions, widely popular and with multiple open-source mesh generators available. The underlying numerical routines can be used to generate standard results, such as the B1+, B1-, and E maps presented in Figure 2, or to address other relevant problems, such as the generation of ultimate intrinsic SNR and SAR on realistic body models, fast coil design and optimization, and generation of patient-specific protocols, among others.



◀ Figure 1: Snapshot of MARIE's graphic user interface with body and coil models loaded, for which the simulation results are shown in Figure 2.



◀ Figure 2: Comparison of the (left) B1+, (center) B1-, and (right) RMS(E) maps for a body model. Top maps are with SEMCAD (SPEAG), bottom with MARIE.

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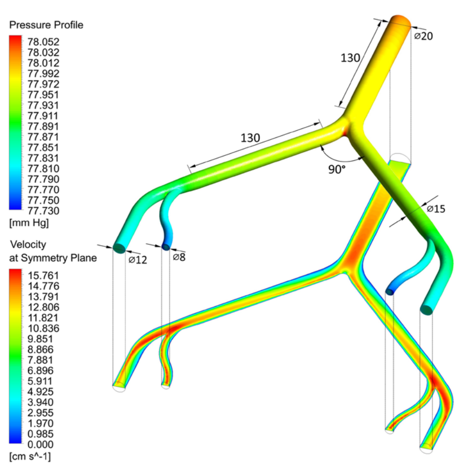
Automated Modeling of Large-Scale Arterial Systems

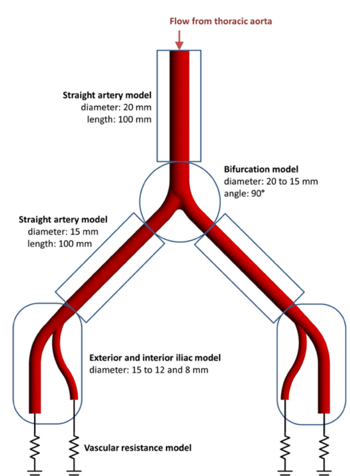
Y.-C. Hsiao, Y. Vassilevski, S. Simakov, L. Daniel
Sponsorship: MIT-Skoltech

Diagnosing medical conditions based on non-invasive (or minimally invasive) measurements requires simultaneous modeling for both local pathological arteries and global arterial networks in order to correlate the available measurements with the actual pathologies. For instance, diagnosing atherosclerosis or an aneurysm requires detailed understanding of the pressure and flow inside the bifurcation segments. Such information is typically not measurable at pathological sites but may still be attainable if it can be inferred from other measurements. Therefore, it is crucial to develop accurate yet efficient global arterial models such that the correlations between the pathologies and the available measurements can be established. The final diagnosis can be obtained by solving an inverse problem for the pathological parameters, for instance, aneurysm internal diameter, arterial wall thickness, plague stiffness, etc.

For this strategy to be effective, the model for such a large-scale arterial network must be compact, computationally tractable, and field-solver-accurate. We have proposed an innovative technique to automatically generate nonlinear dynamic models using measurement data or simulations results from partial-differential-equation (PDE) solvers, as shown in Figure 1. The generated models are guaranteed numerically stable, both when simulated alone and when interconnected within a network. This stability enables the hierarchical modeling capability, generating models for local sub-networks such as branches and bifurcations and interconnecting them to form a global network. An example of such geometry decomposition is demonstrated in Figure 2. This approach allows full exploitation of artery geometries without compromise due to the shape complexity. In addition, because the modeling efforts are subdivided into local model generations, the corresponding finite-element problems for generating training data have a tractable size. Therefore, the fluid dynamics PDEs, such as viscosity and turbulence, can be fully utilized to capture all types of nonlinearities without simplification.



▲ Figure 1: Pressure profile (upper) and velocity profile (lower) of the human abdominal aorta and iliac arteries.



▲ Figure 2: Arterial network decomposition into local models. Each model is automatically generated using our proposed algorithm. The simulation of the overall system is accurate, efficient, and guaranteed numerically stable.

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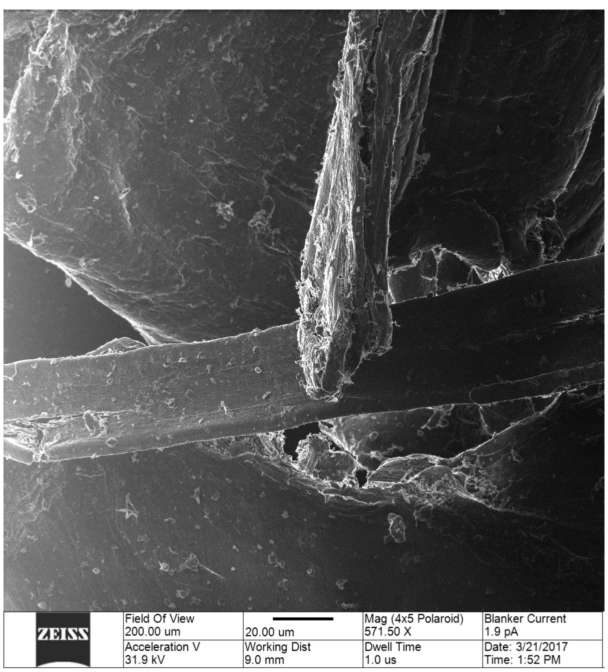
Living Materials Library

B. Datta, S. Sharma, N. Oxman, V. M. Bove, Jr.
Sponsorship: MIT Media Lab Research Consortium

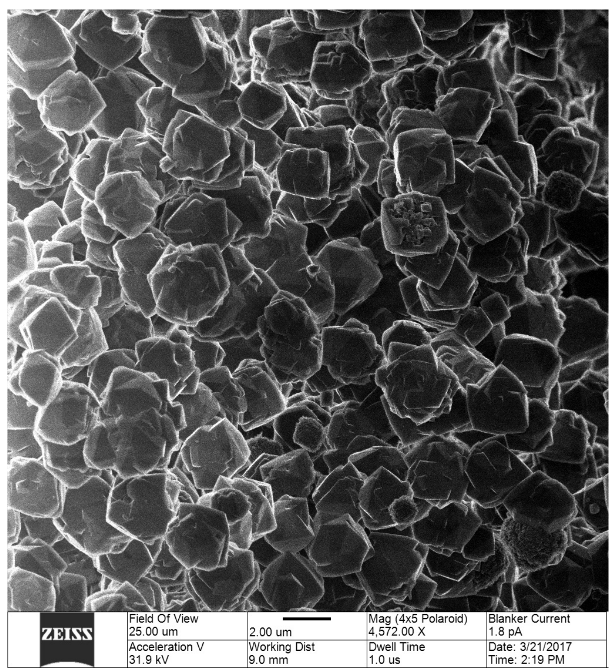
The control of living systems as part of design interfaces is of interest to both the scientific and design communities due to the ability of living organisms to sense and respond to their environments. They may, for example, detect and break down harmful environmental agents or create beneficial products when environmental levels drop below a certain threshold. However, it is also important for these systems to be reversible so that the biological components are active only when their functionality is necessary, and the system can remain dormant otherwise.

The Living Material Library is an exploration of tunable hybrid systems. Our work in this area demonstrates the means through which intrinsic material properties may be functionally changed through environmental factors and, in turn, serve as dynamic substrates for living systems. Nearly all organisms have highly developed sensing capabilities and have been shown to respond behaviorally to changes in substrate properties. By creating a tunable and reversible material system, we explore how cell behavior such as adhesion, patterning, and differentiation may be influenced via an active interface.

In this iteration, we propose a reversible material system that allows for control of living interactions (much like a light switch). We are particularly interested in fluid material systems (such as electrorheological fluids) that transition from a liquid-like to a solid-like state when exposed to electric fields and currents. This endeavor brings to light the complex relationship between dynamic materials and living systems. While other methods of cell intervention often rely on light, chemicals, or temperature, here we explore substrate material properties as inputs for organisms. Our library may allow for more directed inquiry into processes such as collective cell durotaxis, general mechanotaxis, and active sensing. This marks an initial foray into establishing candidate design methods for responsive applications.



▲ Figure 1: Candidate material for responsive material substrate (helium ion microgram of chitosan).



▲ Figure 2: Candidate material for responsive material substrate (helium ion microgram of zeolite 13x).

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Circuits and Systems

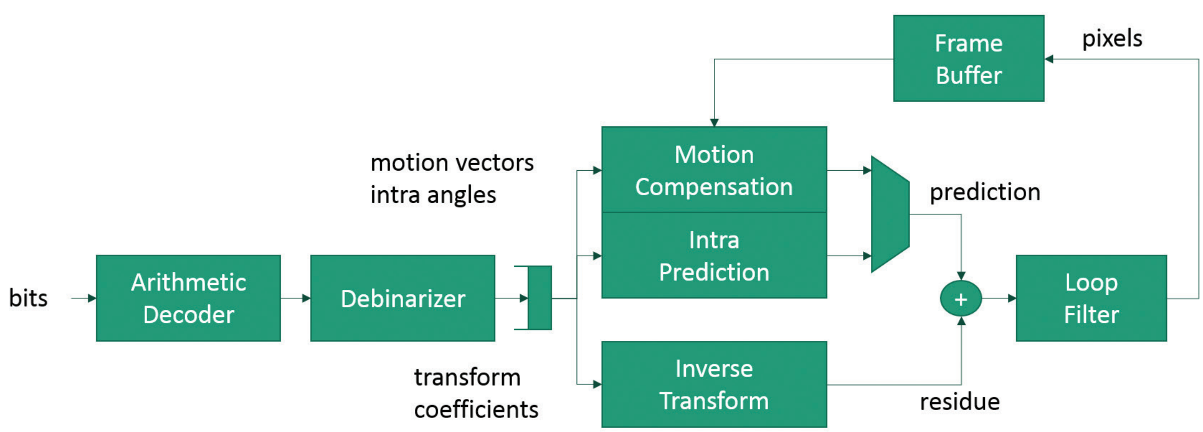
An Energy-Efficient, Fully Integrated 1920x1080 H.265/HEVC Decoder with eDRAM

M. Tikekar, V. Sze, A. P. Chandrakasan
Sponsorship: TSMC University Shuttle Program, NSF

Video playback on mobile devices has become extremely popular in recent years to the extent that video accounts for 55% of all mobile data traffic. In response, new video coding standards that efficiently compress video without sacrificing quality have been developed. H.265/ High Efficiency Video Coding (HEVC), the state-of-the-art video-coding standard, achieves 2x coding efficiency over its predecessor H.264/Advanced Video Coding (AVC). However, it comes at the cost of increased energy and area for video decoding due to computational complexity and memory accesses. In particular, data movement to/from off-chip dynamic random-access memory (DRAM) dominates energy consumption, consuming 2.8x-6x more energy per pixel than the processing itself. Accordingly, the focus of this work is to minimize the energy cost of data movement for an H.265/HEVC decoder.

Wearable devices such as smartwatches, smart glasses, and fitness trackers have stringent budgets for power (< 100mW) and form factor. Previous work has focused on video specifications of 4K and beyond, which are better suited for devices with larger power budgets like smartphones, tablets, set-top boxes, etc. The large frames need to be stored in DRAM, which dominates the overall system power. For example, our previous chip uses DDR3 memory which has a background power of 92mW. Embedded DRAM (eDRAM) helps reduce system power and physical footprint but requires more frequent refreshes than DRAM.

In this work, we propose several techniques to reduce the amount of data movement and optimize for overall system energy. The energy cost of data movement consists of active power for reading from/writing to memory and standby power for retaining memory contents. Through optimized data storage and movement, both active and standby energy cost can be minimized. We demonstrate the proposed techniques in a fully integrated H.265/HEVC decoder that does not require any external components.



▲ Figure 1: Block diagram of H.265/HEVC video decoder showing main processing blocks and syntax elements. The memory bandwidth and chip power are dominated by data access to the frame buffer by the motion compensation unit.

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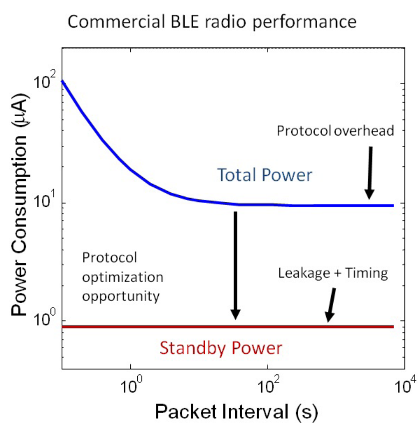
Ultra-Low-Power, High-Sensitivity Secure Wake-Up Transceiver for the Internet of Things

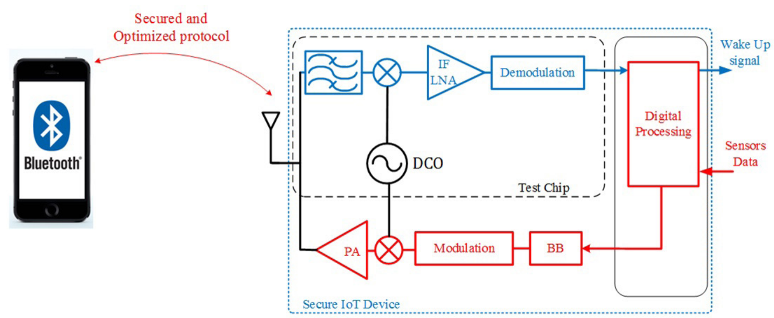
M. R. Abdelhamid, A. P. Chandrakasan
Sponsorship: Delta Electronics

Nanopower Internet-of-Things (IoT) devices are evolving yearly and increasing in size to an estimate of more than 70 billion devices in just ten years. Such devices usually operate at short ranges for personal health monitoring, home automation systems, and longer-range industrial monitoring. Unfortunately, all of these nodes consume a huge portion of their energy on their wireless communication systems. In this work, we propose protocol optimizations for sensor-node driven communications. For base-station driven communication, we propose to achieve power reduction through an ultra-low-power wake-up receiver with optimizations in the protocols as well as the circuits.

Wireless protocols such as Bluetooth low energy (BLE) are optimized for short packets with small preambles and header sizes. However, low duty-cycle performance in the default connected-mode of operation is limited by periodic beacons and the requirement that the node absorbs the timing uncertainties. The analysis of a commercial BLE radio performance, shown in Figure 1, shows that the average power is bounded to tens of microwatts due to the protocol overhead. Such consumption would not last several years using conventional coin cell batteries. Fortunately, the standby power is much less, and an optimized protocol can be developed to complete the wake-up without a full connection while achieving sub-μW consumption. On the wake-up receiver chain, the design can exploit the protocol trade-offs as well as the wake-up scheme to maintain the system specifications. Additionally, the tremendous growth of IoT devices allows open communication among all sorts of devices. With such a huge amount of data flowing through the network, security becomes a critical issue. Hence, we propose the wake-up transceiver system shown in Figure 2, where a transmitter closes the loop by providing small amounts of data sporadically upon request and creates a two-way communication channel for secure wake-ups and transmissions.



▲ Figure 1: Commercial BLE performance analysis.



▲ Figure 2: Block diagram of the proposed wake-up receiver.

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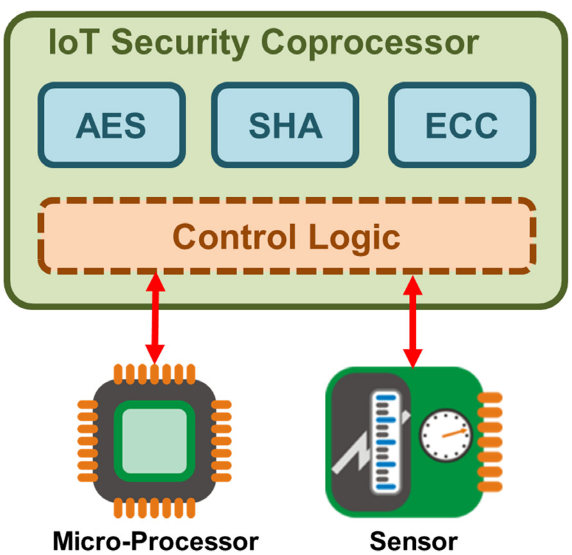
Energy-Efficient Security-Acceleration Core for the Internet of Things

U. Banerjee, C. Juvekar, A. P. Chandrakasan

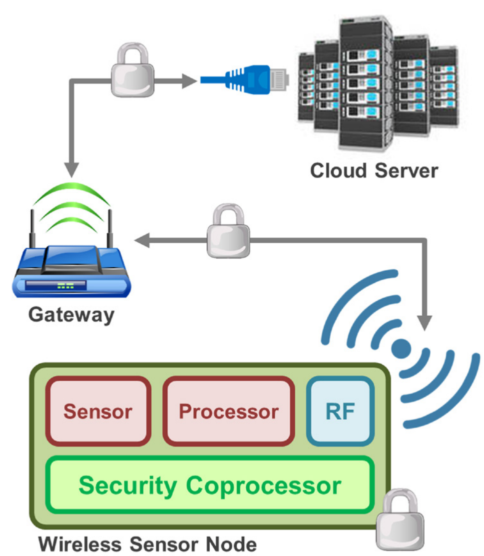
The Internet of Things (IoT) has introduced a vision of an Internet where all computing and sensing devices are interconnected. Digitally connected devices are encroaching on every aspect of our lives, including our homes, cars, offices, and even our bodies. Researchers estimate that there will be over 50 billion wireless connected devices by 2020. On one hand, the IoT enables fundamentally new applications, but on the other, these devices are attractive targets for cyber attackers, thus making IoT security a major concern. According to a security survey from 2016, only 10% IoT products have adequate security features.

Most commercial IoT transceivers either have no security implementations in hardware or only support symmetric key primitives like Advanced Encryption Standard (AES). To achieve end-to-end security in IoT networks, public key algorithms, like elliptic curve cryptography (ECC) are indispensable. Software implementations of these algorithms involve significant computational costs, and the power consumption presents a bottleneck in resource-constrained environments. In this work, we propose to design low-power security-acceleration hardware that interfaces with a standard micro-processor and supports ECC for key exchange and digital signatures, along with standard cryptographic components like AES (Figure 1), thus alleviating the security and efficiency trade-off observed in embedded devices.

Our work also focuses on optimizing network security protocols for efficient implementation in embedded devices. Standard implementations of these protocols tend to have a large communication overhead, which becomes an additional concern for battery-powered or energy-harvesting IoT devices. Therefore, our proposed hardware can not only secure private data using low power cryptographic computations, but also reduce energy consumption of the RF transceiver (Figure 2).



▲Figure 1: Security coprocessor for IoT to accelerate cryptographic primitives like AES, SHA and ECC. The hardware accelerator, which interfaces with a micro-processor, can be used to implement standard transport layer security protocols.



▲Figure 2: Wireless sensor node using the proposed security coprocessor to send encrypted data all the way to the cloud. Application payloads are fully encrypted so that intermediate nodes can process and modify network addresses without gaining access to the actual data.

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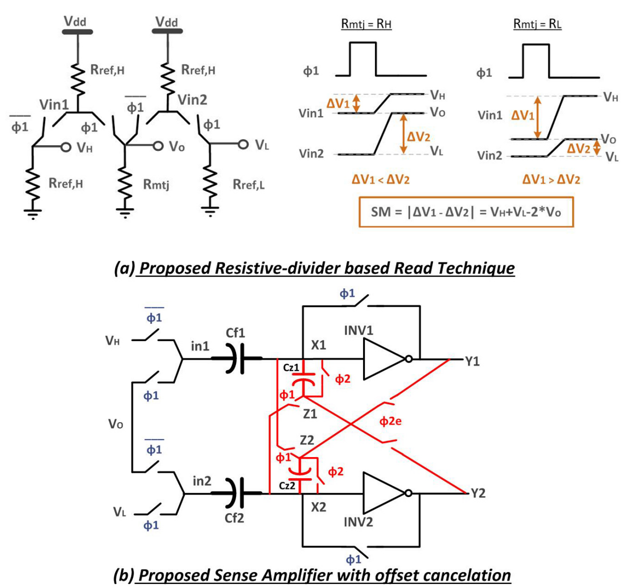
An Offset-Cancelling, Four-Phase Voltage Sense Amplifier for Resistive Memories in 14-nm CMOS

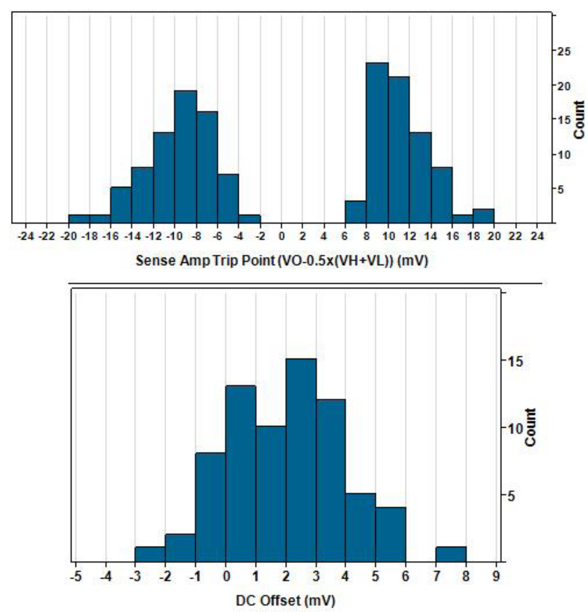
A. Biswas, U. Arslan, F. Hamzaoglu, A. P. Chandrakasan
Sponsorship: Intel Corporation

Resistive memories are a class of non-volatile embedded memories that have the potential to be a universal memory technology by providing the density of dynamic random access memory (DRAM), the speed of static random access memory (SRAM), and the non-volatility of Flash. Resistive memories typically consist of a 1T-1R structure, i.e., a resistive storage device, e.g., a magnetic tunnel junction (MTJ) for spin-transfer-torque random access memory (STT-RAM) and an access transistor. There are two resistance states: high-resistance (R_H '1') and low-resistance (R_L '0'), where R_H = (1+TMR)*R_L. For MTJ devices the tunnel-magneto-resistance ratio (TMR) is typically around 100%-200%, depending on technology, temperature, etc., which makes it challenging to distinguish the two resistance states correctly. On the other hand, due to increasing variations in sub-32-nm complementary metal-oxide semiconductor (CMOS) processes along with variation in MTJ resistance, it becomes challenging to design a read-sensing scheme that achieves low read disturbance and high yield.

In this work, we try to address these issues to design a robust read-sensing circuit for resistive memories that would work for yield >5.5σ and reduce power consumption. The robustness to variations is achieved mainly in two ways. First, due to the pseudo-differential nature of the sensing scheme (comparing data to two references 'ref1' and 'ref0'), we get 2x the signal margin as compared to a single reference scheme. Second, the offset-cancellation of the sense-amplifier (SA) makes it more suitable to tolerate variation from the array due to MTJ resistance variation. The proposed SA was implemented in a 14-nm CMOS process. It achieved correct operation with 20mV input and a DC offset-σ of 1.9mV. This shows that the SA can tolerate large variations from the memory array to achieve a high yield. On the other hand, due to the offset-cancellation technique, the SA can be designed using small devices to achieve low area and power. Hence it benefits from CMOS technology scaling.



▲Figure 1: (a) Proposed resistive-divider based pseudo-differential read sensing technique for resistive memories, (b) Proposed 4-phase sense amplifier with full offset-cancellation.



▲Figure 2: Measured sense amplifier offset distribution for data '0' and data '1'. DC offset is shown at the bottom.

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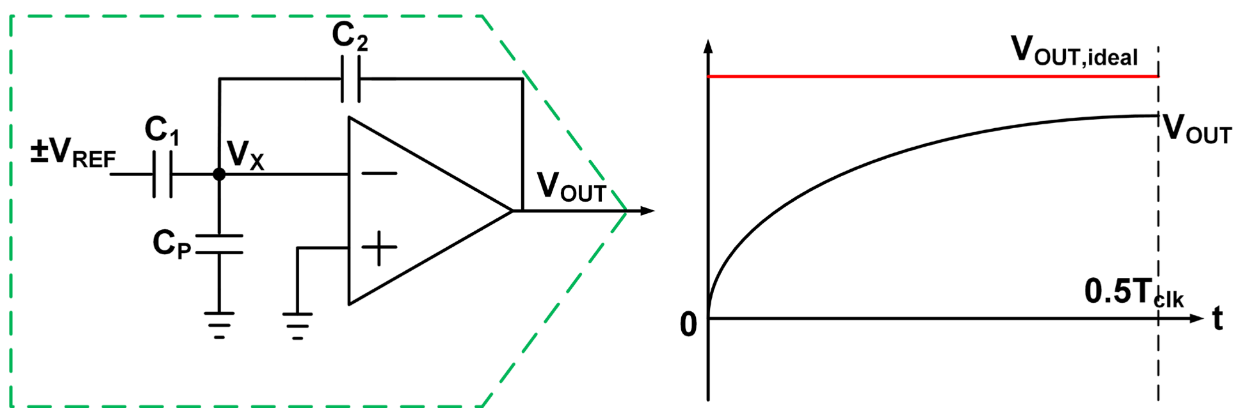
A Pipelined ADC with Low-Gain, Low-Bandwidth Op-amps

T. Jeong, A. P. Chandrakasan, H.-S. Lee
Sponsorship: Korea Foundation for Advanced Studies, CICS, STMicroelectronics

Among various analog-to-digital converter (ADC) architectures, pipelined ADCs are well suited for applications that need medium to high resolution above hundreds-of-megahertz sampling rate. In order to obtain good linearity, conventional pipelined ADCs must minimize MDAC charge-transfer error by employing high-gain, fast-settling op-amps (Figure 1). However, such op-amp design has become increasingly difficult due to the reduced intrinsic gain and voltage headroom in a fine-line complementary metal-oxide semiconductor (CMOS) technology. With low intrinsic gain devices, either gain-boosting technique or multi-stage topology is necessary to make the op-amp meet the gain requirement. Using a decreased power supply demands larger capacitance to maintain the same level of SNR. As a result, the power consumption of op-amps becomes prohibitively large.

In order to address this issue, numerous techniques have been proposed. Digital calibration has been one of the popular ways to use low-performance op-amps in pipelined ADCs. By taking advantage of digital computation, op-amp-induced MDAC charge-transfer errors are measured and removed in the digital domain. More specifically, dithering injection or the least-mean-square algorithm has been exploited to model the MDAC nonlinearity and digitally calibrate the error. In the same context of relaxing op-amp performance requirements, novel analog circuit techniques have also been developed. Virtual ground reference technique and correlated level shifting are techniques that improve MDAC performance without using high-performance op-amps. In some approaches, op-amps are completely replaced by other circuitries that are more amenable to the scaled CMOS technologies. A zero-crossing-based pipelined ADC is a representative example of such approaches.

In this project, we propose a digital calibration scheme for op-amp-based pipelined ADCs. To validate the functionality of the proposed calibration technique, a proof-of-concept ADC has been designed in 28-nm CMOS technology and is currently being fabricated.



▲ Figure 1: Settling behavior of MDAC during charge-transfer phase.

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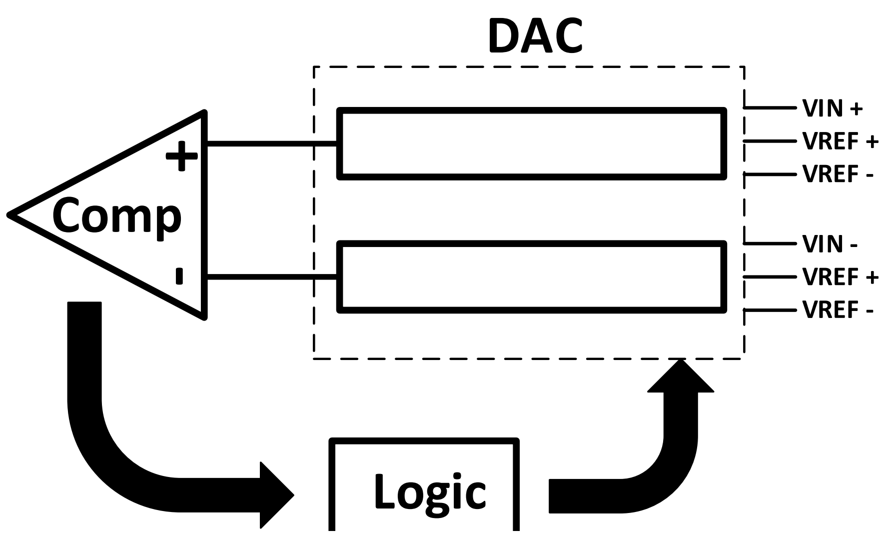
Data-Dependent SAR ADC

H. S. Khurana, H.-S. Lee, A. P. Chandrakasan
Sponsorship: CICS

This work on successive-approximation-register (SAR) analog-to-digital converters (ADCs) (Figure 1) aims at improving data-dependent savings in energy in key components of a SAR ADC by leveraging the information available from the signal's immediate past samples and the signal type. The dominant energy consuming components are the DAC and comparator.

Energy expenditure in DAC per sample conversion depends on the DAC topology and sequence of steps taken during successive approximations. Energy in a comparator is directly proportional to the number of comparisons done per sample conversion. A design with data-dependent savings takes advantage of the correlation between successive samples in completing the conversion in fewer bit-cycles and also operate DAC energy-efficiently.

Previous work presents data-dependent savings by doing least-significant-bit (LSB) first successive approximation to convert an input sample. By starting with a previous sample and doing LSB-first, the algorithm converges in a fewer number of cycles than conventional most-significant-bit (MSB) first SAR conversion. Fewer cycles translate into energy savings in the comparator and DAC. Another work developed successive approximation algorithms to find a sub-range from the full range in a few cycles before carrying on a binary search in this small range. In this work, we investigate a SAR ADC with a search algorithm based on the statistical characteristics of the signal for optimum energy expenditure.



▲ Figure 1: SAR ADC.

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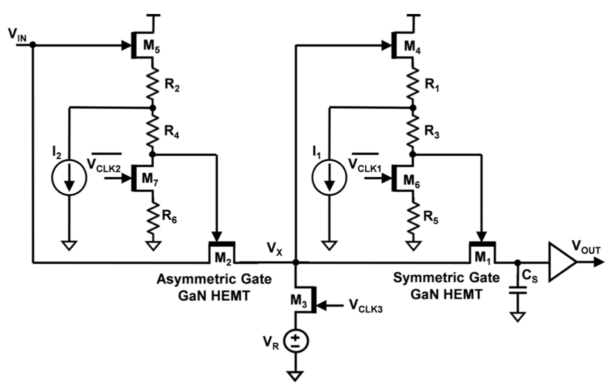
High-Performance GaN HEMT Track-and-Hold Sampling Circuits with Digital Post-Correction

S. Chung, P. Srivastava, X. Yang, T. Palacios, H.-S. Lee
Sponsorship: MIT/MTL GaN Energy Initiative, ONR

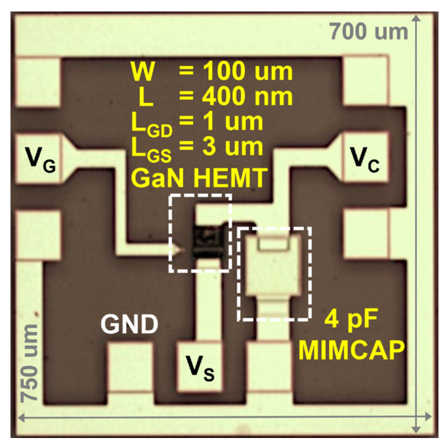
The performance limit of integrated systems for emerging high-performance applications such as ultra-fine imaging and sensing, advanced wireline communication, and data server optical networks often comes from analog-to-digital converters (ADCs) whose performance is, in turn, limited at least partly by a track-and-hold sampling circuit (THSC). The low supply voltage of deeply scaled complementary metal-oxide semiconductor (CMOS) transistors determines the THSC input signal range, therefore becoming a fundamental barrier to the signal-to-noise ratio (SNR) of CMOS circuits.

This research ultimately aims to design ultra high-performance THSCs in GaN-on-Si technology, which monolithically integrates GaN high-electron-mobility transistors (HEMTs) with Si-CMOS transistors. Operating GaN HEMTs at a high voltage (>30 V) allows a very large input swing (>16 V) and provides performance beyond the limit of CMOS THSCs. As a first step, we designed two GaN HEMT THSCs. The first THSC was fabricated in a commercial GaN foundry technology on SiC substrate, providing 98-dB SNR at 200-MS/s (Figure 1). The second THSC design was fabricated in a GaN technology that was developed at MTL on Si substrate, which operates at 1 GS/s thanks to a higher current-gain cutoff frequency f_T and external gate-bootstrapping clock (Figure 2).

While these two GaN THSCs achieved very high SNR at a given input frequency, they suffered from nonlinearity. We characterized how the static nonlinearity and dynamic memory effects of GaN HEMT THSCs affect the sampled output; we observed that the GaN HEMT dynamic on-resistance does not significantly degrade the THSC linearity because the capacitive load does not suffer from on-resistance variation on the sampled voltage. We identified that most of the dynamic nonlinearity originates from the GaN HEMT source-follower buffers for gate-bootstrapping sampling clock generation. Although dynamic nonlinearity correction techniques are mature with RF power amplifiers (PAs) and improve PA linearity typically by 20-40 dB depending on signal bandwidth and modeling accuracy, these pre-distortion techniques cannot be directly applied to THSCs. To overcome this challenge, we are developing a digital post-correction technique, which will demonstrate improved linearity of GaN HEMT THSCs without using a dedicated reference ADC.



▲Figure 1: Pseudo-differential two-stage track-and-hold sampling circuit in 0.25-µm GaN HEMT technology on SiC substrate, which demonstrates 200-MS/s 98-dB SNR and 240-MHz track-mode bandwidth.



▲Figure 2: Track-and-hold sampling circuit with external gate-bootstrapping clock in a GaN technology developed at MTL on Si substrate, which provides over 700-MHz track-mode bandwidth and operates at 1 GS/s.

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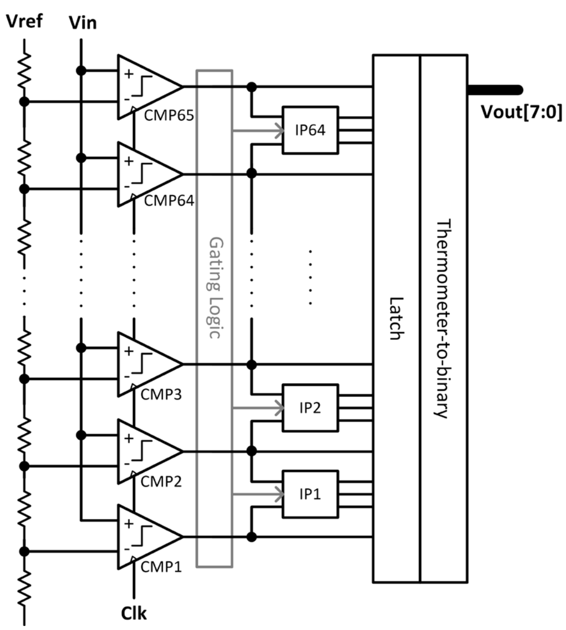
A CMOS Flash ADC for a GaN/CMOS Hybrid Continuous-Time ΔΣ Modulator

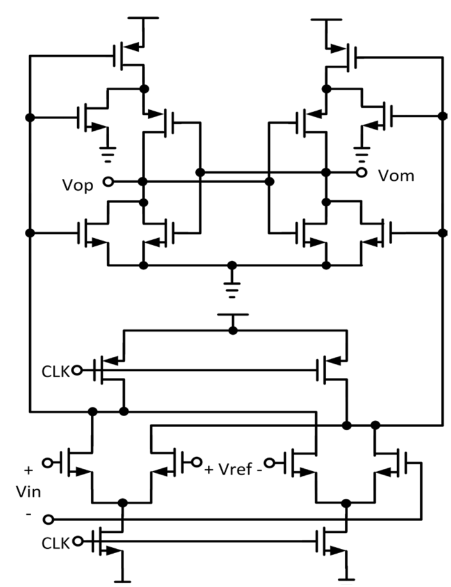
X. Yang, H.-S. Lee
Sponsorship: ONR

High-speed and low-resolution flash analog-to-digital converters (ADCs) are widely used in applications such as 60-GHz receivers, serial links, and high-density disk drive systems, as well as in quantizers in delta-sigma modulators. In this project, we propose a flash ADC with a reduced number of comparators by means of interpolation. One application for such a flash ADC is a hybrid gallium-nitride (GaN) and complementary metal-oxide semiconductor (CMOS) delta-sigma modulator. The GaN first stage exploits the high-voltage property of the GaN while the CMOS backend employs high-speed, low-voltage CMOS. This combination may achieve an unprecedented signal-to-noise ratio (SNR)/bandwidth combination by virtue of its high input signal range and high sampling rate.

One key component of the hybrid modulator is a flash ADC. To take advantage of the high signal-to-thermal-noise ratio of the proposed system, the quantization noise must be made as small as possible. Therefore, a high-speed, 8-bit flash ADC is proposed for this system. Sixty-five comparators are used to achieve the six most significant bits. Sixty-four interpolators are inserted between the comparators to obtain two extra bits. The input capacitance of this design is ¼ of the conventional 8-bit flash ADC. Therefore, a higher operating speed can be achieved. We introduce gating logic so that only one interpolator is enabled during operation, which reduces power consumption significantly. A high-speed, low-power comparator with low noise and low offset requirements is a key building block in the design of a flash ADC. We choose a two-stage dynamic comparator because of its fast operation and low power consumption. With the scaling of CMOS technology, the offset voltage of the comparator keeps increasing due to greater transistor mismatch. In this project, we also propose a novel offset compensation method that eliminates the speed problem.



▲Figure 1: Flash ADC architecture, with 65 comparators and 64 2-bit interpolators.



▲Figure 2: Schematic of the two-stage dynamic comparator.

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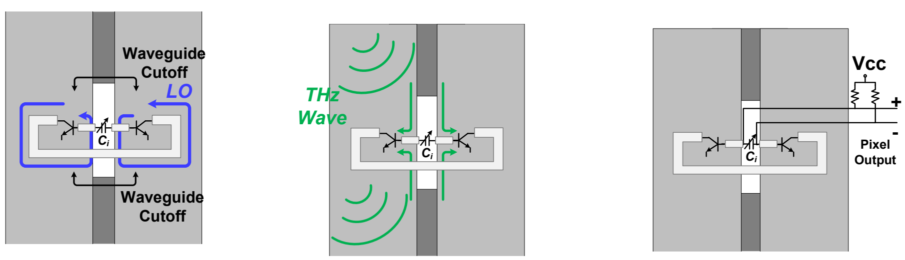
Terahertz Beam-Steering Imager Using a Scalable 2D-Coupled Architecture and Multi-Functional Heterodyne Pixels

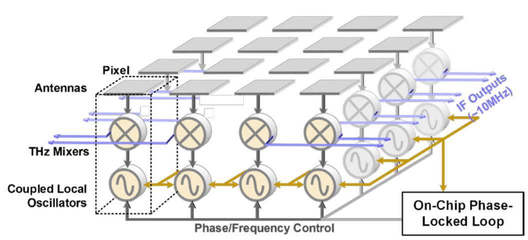
G. Zhang, C. Wang, J. Holloway, R. Han
Sponsorship: CICS, IHP Germany

Terahertz (THz) imaging has increasing potentials in industrial quality control, security screening, and accurate distance mapping for short-range applications such as robots, augmented reality, and virtual reality sensing. With the development of a high-power THz illumination source, future deployment of THz imaging in autonomous vehicles is also possible in order to complement lidar, which fails to operate under foggy and dusty conditions, as well as microwave/mmWave radar, which does not provide high resolution. An ideal imager calls for high spatial/ranging resolution, high sensitivity, fast scanning speed, and low SWaP-C (size, weight, power, and cost). A THz imager formed by a large-scale heterodyne sensing array in a silicon integrated circuit provides the opportunity to achieve all these requirements at once.

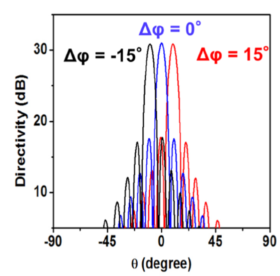
In this project, we develop a multi-functional design of heterodyne pixel and a scalable array architecture. Shown in Figure 1, a compact electromagnetic structure simultaneously performs voltage-controlled 140-GHz local oscillation, 280-GHz-signal receiving, sub-harmonic mixing, and intermediate-frequency (IF) signal extraction. Each pixel consumes 10-mW power and achieves a sensitivity of 2.9 pW in simulation. The local oscillator (LO) of the pixel is phase coupled with its neighbors; the whole oscillator array is then stabilized by an on-chip THz phase-locked loop (PLL, Figure 2). This architecture gives excellent array scalability. First, the LO power is evenly distributed and does not degrade in a larger array scale as a normal centralized array does. Second, the phase noise of the coupled LO network improves linearly with the array size. The simulated phase noise at 1-MHz frequency offset is -90 dBc/Hz for an 8x8 array and -101 dBc/Hz for a 32x32 array. This chip is capable of digital beam steering, too. The simulated response of a steered beam direction for a 32x32 array is shown in Figure 3. A chip prototype with 10x10 array is currently under fabrication using a 130-nm SiGe BiCMOS process.



▲Figure 1: The design of the pixel: (left) the LO oscillation, (mid) 280 GHz signal receiving and sub-harmonic mixing, (right) and IF signal extraction.



▲Figure 2: The architecture of the chip with LO coupling and control by an on-chip PLL.



▲Figure 3: Beam steering result of a 32x32 array.

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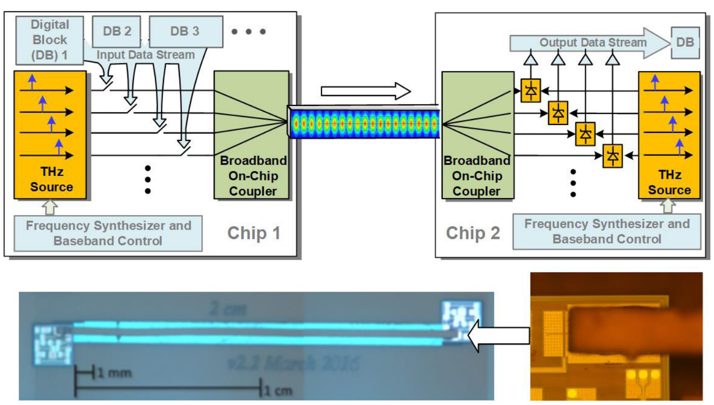
Broadband Inter-Chip Link Using a Terahertz Wave on a Dielectric Waveguide

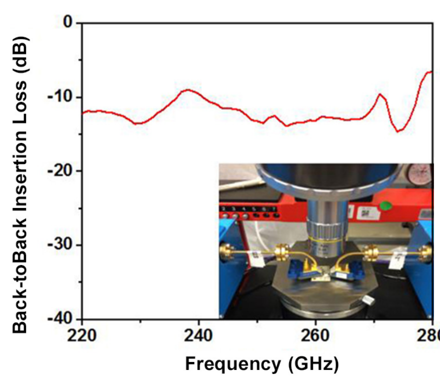
J. Holloway, Z. Hu, R. Han
Sponsorship: ONR, MIT Lincoln Laboratory, Analog Devices, Inc.

The development of data links between different microchips of an on-board system has encountered a speed bottleneck due to the excessive transmission loss and dispersion of the traditional inter-chip electrical interconnects. Although high-order modulation schemes and sophisticated equalization techniques are normally used to enhance the speed, they also lead to significant power consumption. Silicon photonics provide an alternative path to solve the problem, thanks to the excellent transmission properties of optical fibers; however, the existing solutions are still not fully integrated (e.g., an off-chip laser source is used) and normally require process modification to the mainstream complementary metal-oxide semiconductor (CMOS) technologies.

Here, we aim to utilize a modulated THz wave to transmit broadband data. Similar to the optical link, the wave is confined in dielectric waveguides, with sufficiently low loss (~0.1dB/cm) and bandwidth (>100GHz) for board-level signal transmission (Figure 1). In commercial CMOS/BiCMOS platforms, we have previously demonstrated high-power THz generation with modulation, frequency conversion, and phase-locking capabilities. In addition, a room-temperature Schottky-barrier diode detector (in 130-nm CMOS) with <10pW/Hz$^{1/2}$ sensitivity (antenna loss excluded) is also reported. The proposed data link will leverage these techniques to achieve a >100Gbps/channel transmission rate with <1pJ/bit energy efficiency. As the first step of this project, we have designed a new broadband chip-to-fiber THz wave coupler. In contrast to previous couplers using off-chip antennas, our THz coupler is entirely implemented using the metal backend of a CMOS process and requires no post-processing (e.g., wafer thinning). The structure is also fully shielded, which prevents THz power leakage into the silicon substrate. Conventional on-chip radiators using ground shield work are the resonance type (e.g., patch antenna) and have only <5% bandwidth. In comparison, our design is based on a traveling-wave, tapered structure, which supports broadband transmission. A proof-of-concept is shown in Figure 1: two on-chip couplers are connected with a 2-cm waveguide using Rogers 3006 dielectric material. The entire back-to-back setup exhibits only ~11dB insertion loss across over 60-GHz bandwidth (Figure 2).



▲Figure 1: (Top) High-speed, energy-efficient inter-chip transmission using guided terahertz wave. (Bottom) A test structure including a pair of back-to-back THz integrated couplers separated by a 2-cm dielectric waveguide using Rogers 3006.



▲Figure 2: The measured back-to-back insertion loss using a two-port network analyzer in the WR-3 band.

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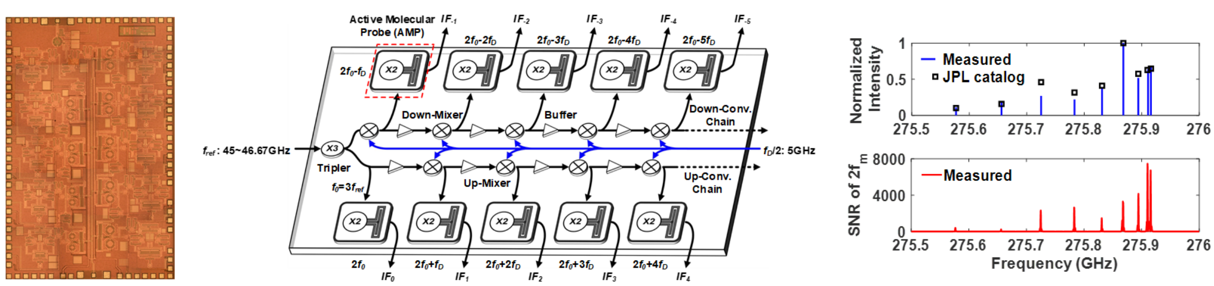
Bilateral Dual-Frequency-Combs-Based 220-to-320GHz Spectrometer in 65-nm CMOS for Gas Sensing

C. Wang, R. Han
Sponsorship: NSF, MIT Lincoln Laboratory, CICS

Millimeter-wave/terahertz rotational spectroscopy offers an ultra-wide detection range of gas molecules for chemical and biomedical sensing. The linewidth of the absorption spectrum, limited by the Doppler effect of molecules, has a quality factor near 10^6, indicating absolute specificity for molecule identification. Therefore, broadband, energy-efficient, and high-precision complementary metal-oxide semiconductor (CMOS) spectrometers are in high demand. Spectrometers using narrow-pulse sources and electromagnetic scattering, although broadband, fail to provide resolution that meets the requirement for absolute specificity. Alternatively, spectrometers using a single tunable tone not only exhibit significant trade-off between bandwidth and performance, but also have a low speed limited by molecular saturation, which sets an upper bound for the single tone power. Given a typical 10-kHz resolution and 1-ms integration time, scanning a 100-GHz bandwidth with a single signal tone takes as long as 3 hours.

We report a rapid, energy-efficient spectrometer based on a bilateral, dual-frequency-comb architecture. This architecture generates and detects multiple comb lines by using cascaded continuous frequency conversion. Due to the narrow band operation of each conversion stage, it significantly increases the performance and energy efficiency of the system. A 220-to-320GHz CMOS spectrometer prototype based on this architecture is demonstrated with a total measured radiated power of 5.2 mW, which is evenly distributed among 10 comb lines. It also serves as a 10-channel heterodyne receiver with a noise figure of 14.6 to 19.5 dB within the 220-320GHz band. Through the bi-directional parallel operation, this spectrometer increases the scanning speed by 20×. In addition, the improved signal-to-noise ratio reduces the integration time at each frequency point, so the scanning speed and energy efficiency are thus further improved. A fraction of rotational absorption spectrum of acetonitrile (CH_3CN) is measured, and it agrees with the JPL molecule catalog and demonstrates the absolute specificity of the spectrometer.



▲ Figure 1: System architecture and measured spectrum of CH_3CN using the wideband THz CMOS spectrometer.

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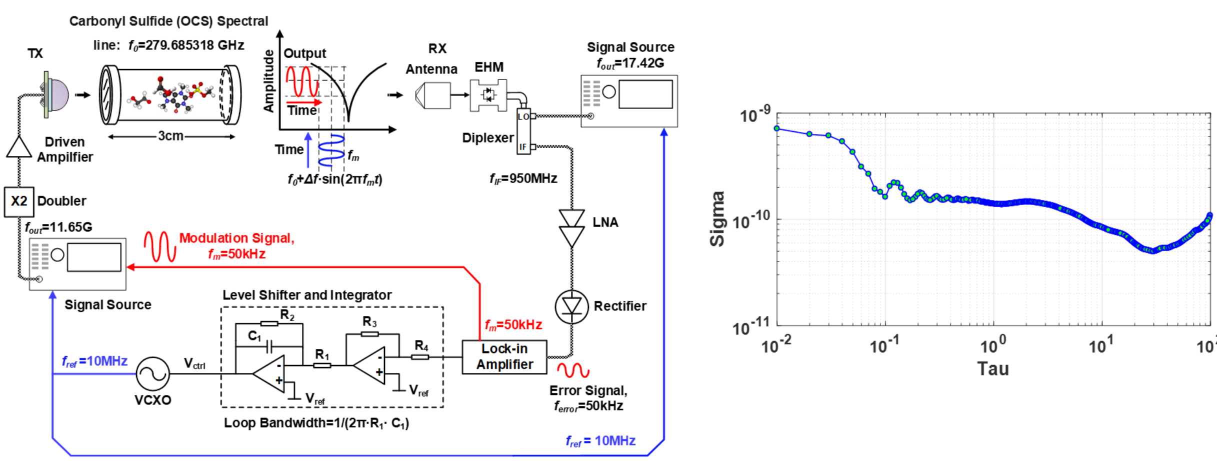
High-Stability, Miniature Terahertz Molecular Clock on CMOS

C. Wang, J. P. Mawdsley, R. Han
Sponsorship: MIT Lincoln Laboratory, NSF, Texas Instruments

Frequency reference is an essential component in most electronic systems. Applications such as communication, navigation, and reconnaissance in portable platforms or under GPS-denied environments demand highly stable frequency references (Allan deviation 1×10-12, τ=1s), which exceed the capability of widely used temperature or oven-compensated crystal oscillators. Currently, chip scale atomic clocks (CSACs), which rely on hyperfine states of alkali atoms, are used at high cost. In this work, we develop a low-cost miniature clock on a complementary metal-oxide semiconductor (CMOS), which relies on rotational energy state transitions of gaseous molecules at low-THz range. The spectral line probed by the spectrometer inside our molecular clock has a slightly lower quality factor Q compared to that in CSACs but a much higher signal-to-noise ratio (SNR). The short-term frequency stability, determined by the product of Q and SNR, is therefore improved. The chemically stable gas molecules used in this clock also provide frequency robustness against environmental variations (temperature, pressure, Stark effect, and Zeeman effect), leading to excellent long-term stability.

An experimental system of molecular clock has been demonstrated. The spectral line at 279.865GHz of carbonyl sulfide (OCS) is chosen for its strong absorption and simple molecular structure. The system probes the spectral line using frequency modulated terahertz waves and dynamically adjusts a crystal oscillator to synchronize the output center frequency of the terahertz transmitter with the spectral line. The preliminary measured Allan deviation (frequency stability) with τ=30s is 5×10^{-11}. To achieve ultra-low size, weight, power consumption, and cost (SWaP-C), a CMOS molecular clock is under development. On the transmitter side, it adopts a 40-bits ΔΣ fractional PLL with integrated FSK modulation function. On the receiver side, a homodyne detector along with lock-in detection is used. In simulation, an Allan deviation of 2×10^{-12} (τ=100s) and DC power consumption of 50 mW are obtained.



▲ Figure 1: System architecture and measured Allan deviation of the molecular clock.

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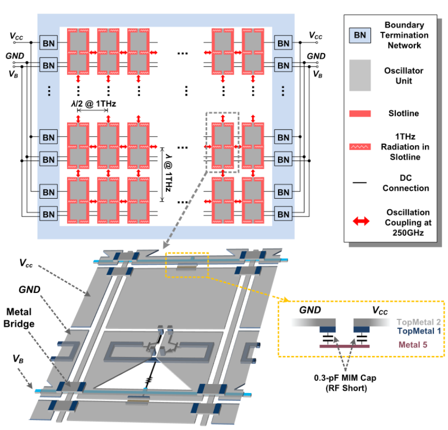
2D Quasi-Optical Power Combining at 1 THz: An 80-μW Source in Silicon

Z. Hu, R. Han
Sponsorship: Analog Devices, Inc., Leibniz-Institut für innovative Mikroelektronik, SMART

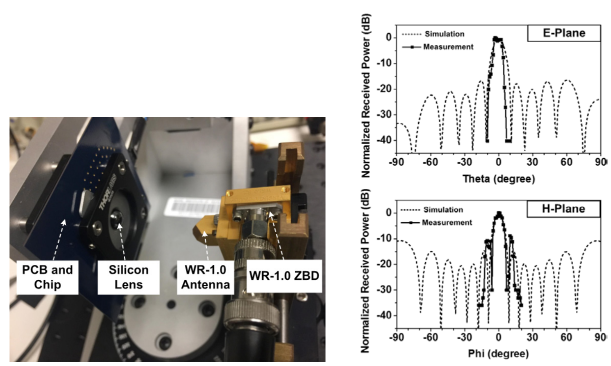
Generating high-power signal in the mid terahertz (THz) range is a challenge since this frequency band lies beyond the f_{max} of all silicon-based transistors and below the typical operation range of quantum cascaded lasers. Nevertheless, unique properties of waves in this band are highly beneficial for several research fields: (i) high-resolution real-time THz imaging, (ii) vibrational spectroscopy of large bio-molecules, (iii) sub-μm-precision vibrometry, etc. The total radiated power of previously reported radiator chips near-1 THz was below 10 μW. In addition, there is no prior research on quasi-optical power combining in this band, since two challenges remain unsolved: (i) maintenance of strong coupling across a large-scale array and (ii) high-density placement of radiator structures with the integration of oscillator, antennas, and couplers, within a limited area of ($\lambda/2$ by $\lambda/2$). In this work, we have successfully addressed these issues and built a high-power 2D-scalable 1THz radiator array in silicon.

Figure 1 shows a conceptual diagram of our design: the chip consists of oscillator units coupled in a 2D fashion. Coupling is achieved by slotlines on the four edges of each unit, which strongly lock the phase (and hence frequency) with its four adjacent counterparts. Inside each unit, there are two self-feeding oscillators, coupled in the differential mode, generating 250-GHz fundamental (f_0) oscillation and resultant harmonics. Among all harmonics, only $4f_0$ signal at 1 THz is radiated while other lower harmonics are re-injected into transistors for up-mixing to $4f_0$. This critical function is achieved by forming the standing-wave patterns inside the slotlines of the unit so that near-field radiations at f_0 and $3f_0$ are cancelled between horizontally adjacent slots while the radiation at $2f_0$ is cancelled between vertically adjacent slots.

Lastly, the standing waves at $4f_0$ in all horizontal slotlines are in phase, which leads to efficient coherent radiation. Due to the compactness of the design, the spacing between neighboring dipole slot antenna structures is $\lambda_{1THz}/2$ in both horizontal and vertical directions, permitting large array scale (91 antennas in total) and high radiation directivity (24 dB). Figure 2 shows the setup and results for radiated power and pattern measurements using a zero-biased diode detector. The measured total radiated power is 80 μW, which is 10× higher than the prior state-of-the-arts, and the equivalent isotropically radiated power is 13 dBm. The chip was fabricated using IHP 0.13-μm SiGe BiCMOS technology.



▲Figure 1: The architecture of the radiator array: (top) overview of the array and (bottom) 3-D view of a single unit.



▲Figure 2: Radiation measurement using zero-biased diode: (left) measurement setup and (right) measured E-/H-plane radiation pattern.

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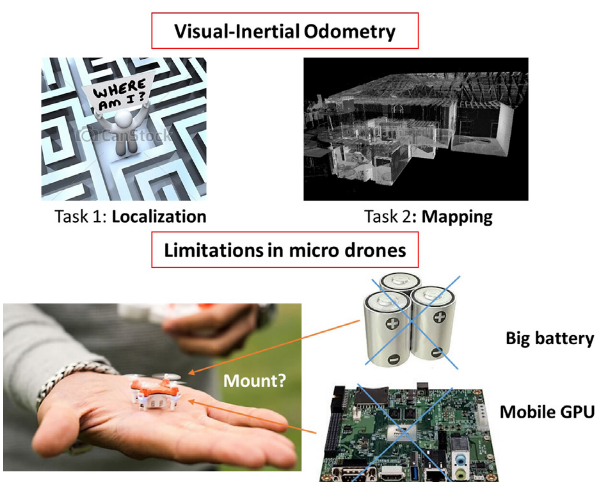
uVIO: Energy-Efficient Accelerator for Microdrone Navigation in GPS-Denied Environments

A. Suleiman, Z. Zhang, L. Carlone, S. Karaman, V. Sze
Sponsorship: Air Force Office of Sponsored Research

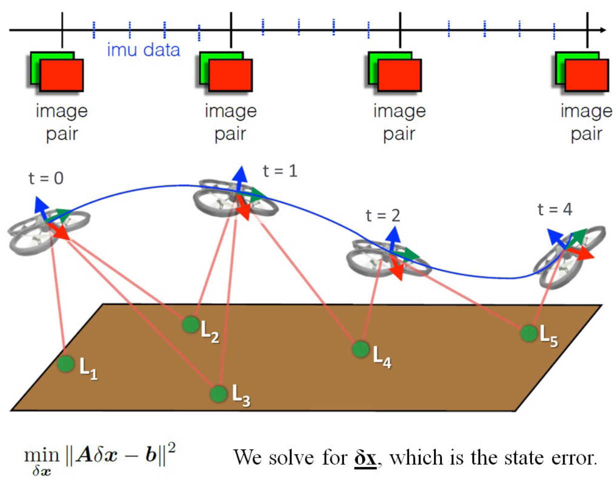
Drones are getting increasingly popular nowadays; it is reported that their sales have tripled in the last year. Microdrones specifically are easily portable and can fit in a pocket. Equipped with multiple sensors like cameras and inertial measurement unit (IMU), the functionality of drones is getting more powerful and smart, e.g., they track objects, build accurate 3-D maps, and even avoid obstacles. These capabilities are enabled by powerful computing platforms like CPUs and GPUs, which consume a lot of energy, installed on the drones. Both the size of these platforms as well as the battery's weight and limited energy make it prohibitive to deploy to microdrones, which can be as small as two inches and operate on very small batteries as shown in Figure 1.

In this project we present uVIO, an energy-efficient hardware accelerator for microdrone navigation in GPS-denied environments. The hardware is co-optimized with the algorithm and the drone design to enable a lightweight drone (~100 grams). The microdrone is equipped with a stereo camera and an IMU and can operate in real time without any external communications. The accelerator is designed to be energy-efficient to operate on a small battery, satisfying the overall payload weight of the drone.

The proposed accelerator implements a robust and optimized visual inertial odometry (VIO) algorithm, shown in Figure 2. It combines the visual information and the IMU measurements to estimate the position, orientation, and velocity of the microdrone as well as the 3-D environment via Gauss-Newton algorithm. The implementation is highly parallelized and pipelined to achieve real-time performance and energy efficiency. This accelerator gives a microdrone the smart sensing capability, which now only exists in large drones with bulky batteries. It enables numerous applications where large drones do not fit, such as indoor exploration and surveillance as well as rescue operations in collapsed buildings.



▲ Figure 1: Visual-inertial odometry output of localization and mapping are the first steps to enable autonomous navigation. With microdrones, this is extremely challenging with both power and weight limitations.



▲ Figure 2: VIO pipeline takes the visual 3-D point cloud and the IMU data over a time horizon and solves a global optimization problem to refine the drone pose (also called "state").

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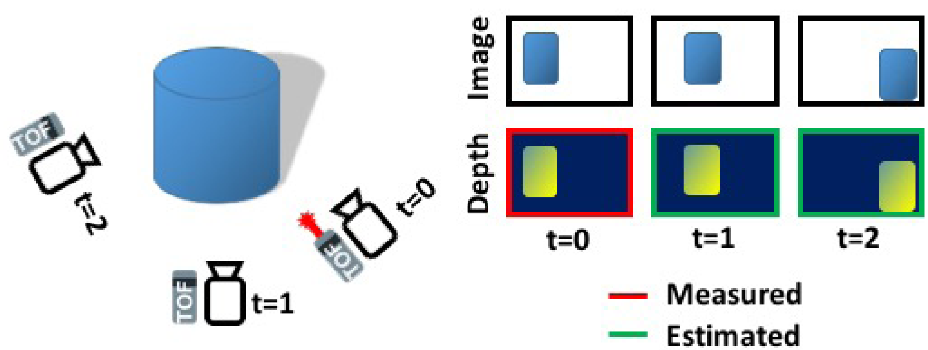
Depth Estimation for Low-Power Time-of-Flight Imaging

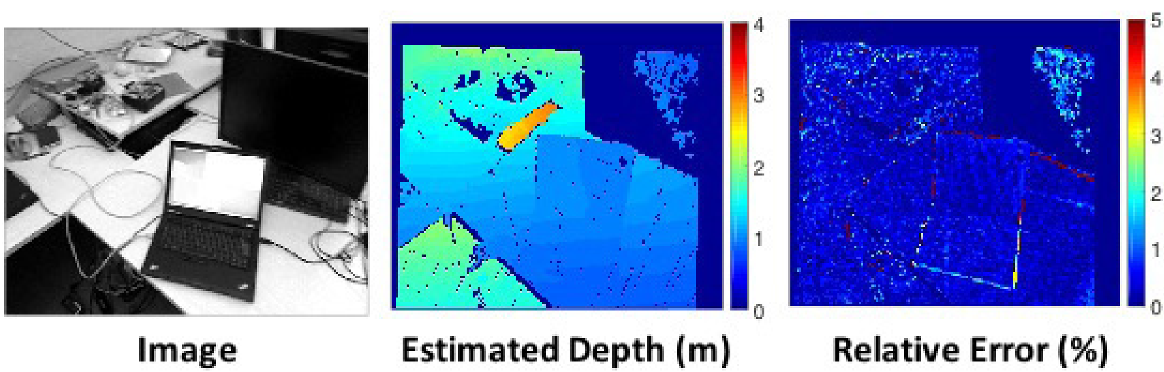
J. Noraky, V. Sze
Sponsorship: Analog Devices, Inc.

Depth sensing is used in a variety of applications that range from augmented reality to robotics. One way to measure depth is with a time-of-flight (TOF) camera, which obtains depth by emitting light and measuring its round trip time. TOF cameras are appealing because they are compact, have no moving parts, and require minimal computation to obtain depth. However, the illumination source of TOF cameras requires a significant amount of power and limits the application time for mobile and battery-operated devices. To reduce the power for TOF imaging, we propose an algorithm that leverages images, which can be efficiently collected alongside the TOF camera, to estimate depth maps without the need of continuously illuminating the scene (Figure 1).

Our technique is best suited for estimating the depth of rigid objects and uses the temporal correspondences between images to estimate the 3-D motion of objects in the scene, from which a new depth map can be obtained. Our algorithm is computationally simple and produces 640 × 480 depth maps at 30 FPS on a low power embedded platform. We evaluated our technique on a RGB-D dataset, where it estimated depth maps (Figure 2) with a mean relative error of 0.85% while reducing the total power required for depth sensing by 3×.



▲ Figure 1: Minimize the power of TOF imaging by minimizing its usage and estimate new depth maps using images.



▲ Figure 2: Example of the estimated depth map obtained using our approach. Pixel-wise relative error is shown in the third column.

Phase-Shift Impedance Modulation for Fast Response Dynamic Impedance Matching

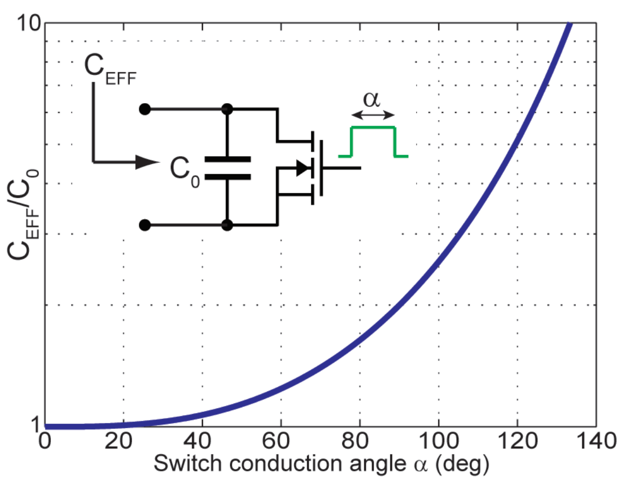
A. S. Jurkov, D. J. Perreault
Sponsorship: MKS Instruments Inc.

Accurate, rapid, and dynamically-controlled impedance matching offers significant advantages to a wide range of present and emerging radio-frequency (RF) power applications such as software-defined radios, frequency-agile and adaptive RF transmitters and receivers, the design of new types of highly-efficient RF power amplifiers, plasma drivers, generators, wireless power transfer, and many other industrial processes.

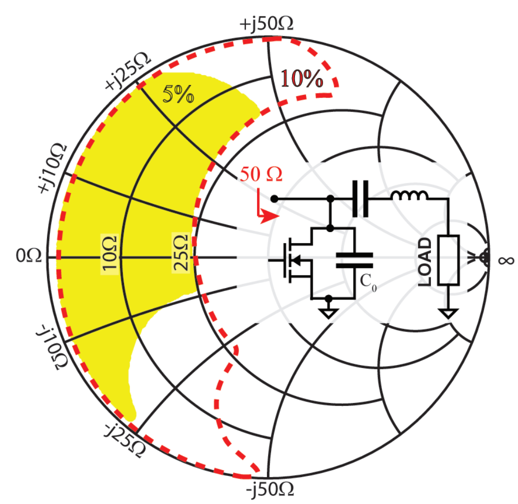
For high-frequency (HF) and very-high-frequency (VHF) applications, e.g., 3-300 MHz, a tunable impedance matching network (TMN) is typically implemented as an ideally lossless, lumped-element reactive network, in which some of its reactive elements are realized as variable (tunable) components. Conventional techniques for implementing variable reactances for high power RF applications often impose limitations on tuning resolution or speed.

This work proposes an approach to TMNs that allows for a combination of much faster and more accurate impedance matching than is available with conventional techniques and is suitable for use at high-power levels. This implementation is based on a narrow-band technique, termed here phase-switched impedance modulation (PSIM). The notion of phase-switched variable reactances relies on the ability to modulate the effective impedance of a switched reactive element (capacitor, inductor, or some combination of both) at the switching frequency (i.e., the RF frequency). In essence, it is a narrow-band technique for controlling the effective impedance seen looking into the terminals of a reactive element at the frequency at which this element is switched (including either by a shunt or a series switch) by appropriately adjusting the phase and/or duty-cycle of the switch (Figure 1).

A TMN prototype that demonstrates the performance of a PSIM-based implementation is designed to provide a 50-Ω match over a load impedance range associated with inductively-coupled plasma processes and operate in a narrow frequency band centered around 13.56 MHz (Figure 2). Ongoing work aims to further explore PSIM-based design of both variable and fixed-frequency matching networks and a new class of switching RF power amplifiers that can operate efficiently over wide load and frequency range.



▲ Figure 1: PSIM allows modulation of the effective capacitance C_{EFF} (at the switching frequency) by varying the conduction angle α of the switch. Zero-voltage switching can be ensured by appropriately synchronizing the switch to the current in the PSIM element.



▲ Figure 2: Load impedance matching range (5% and 10% frequency modulation) of a PSIM-based prototype. This design employs modulation of both switch conduction angle and frequency to achieve a 50-Ω impedance match.

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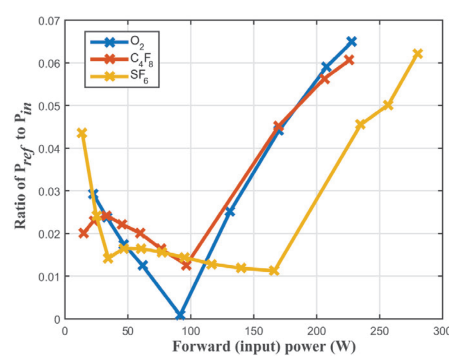
Dynamic Matching System for Radio-Frequency Plasma Generation

A. Al Bastami, A. S. Jurkov, P. Gould, M. Hsing, M. A. Schmidt, J. Ha, D. J. Perreault
Sponsorship: MIT

The use of plasma in the processing of materials has become prevalent in a wide range of industries. A commonly used means of generating these plasmas is to inductively couple energy from a radio-frequency (RF) power amplifier into the chamber containing the gas to be ionized (e.g., by driving RF current through a coil wound around the chamber). Key challenges in RF plasma generation include efficiently generating and controlling the RF power delivered into the plasma while maintaining acceptable loading of the associated RF power amplifier under the high operating frequency (e.g., 13.56 MHz) and the highly-variable conditions in a plasma system. Inductively coupled plasma (ICP) loads represent a dynamically variable load impedance that depends on gas type and pressure, operating mode, power level, and other features. The effective load impedance can vary substantially in both its real and reactive components, making matching challenging.

Because the effective loading provided by the plasma coil varies greatly across operating conditions, a tunable matching network is typically utilized between the power amplifier and the plasma coil. However, this tends to be costly and bulky, and it exhibits a slow response to load changes. We introduce a dynamic matching system for ICP generation that losslessly maintains near-constant driving point impedance (for low reflected power) across the entire plasma operating range. This new system utilizes a resistance compression network (RCN), an impedance transformation stage, and a specially-configured set of plasma drive coils to achieve rapid adjustment to plasma load variations. As compared to conventional matching techniques for plasma systems, the proposed approach has the benefit of relatively low cost and fast response and does not require any moving components. We develop suitable coil geometries for the proposed system and treat the design of the RCN and matching stages, including design options and tradeoffs. A prototype system is implemented (Figure 1) and its operation is demonstrated with low pressure ICP discharges with O_2, C_4F_8, and SF_6 gases at 13.56 MHz and over the entire plasma operating range of up to 250 W (Figure 2).

▲ Figure 1: The proposed plasma drive system with O_2 being ionized during a plasma ashing process. The orthogonal coils on the plasma chamber can be seen in the center of the photograph, with the single-input two-output matching system in the sealed enclosure to its right.



▲ Figure 2: Results showing the ratio of reflected power to input power, plotted across the entire range of plasma operation.

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Magnetic Field Sensing for Smart Industrial Infrastructure

C. Zhang, D. Pan, J. H. Lang
Sponsorship: Harting Technology Group

This newly initiated project seeks to develop hardware and algorithms to support the contactless measurement of currents in connectors. A natural future extension of this project is to develop hardware and algorithms to support the contactless measurement of voltages. Such measurements in turn will support the development of smart industrial infrastructure that monitors the power and signals passing through them. In concert with signal processing and machine learning algorithms, the electrical data might be used to further monitor upstream sources and downstream loads. For example, it might be possible with enough "intelligence" to learn normal operation from prior transmitted power and signals and then recognize future signatures that predict subsequent failures, making the power and data infrastructure truly smart.

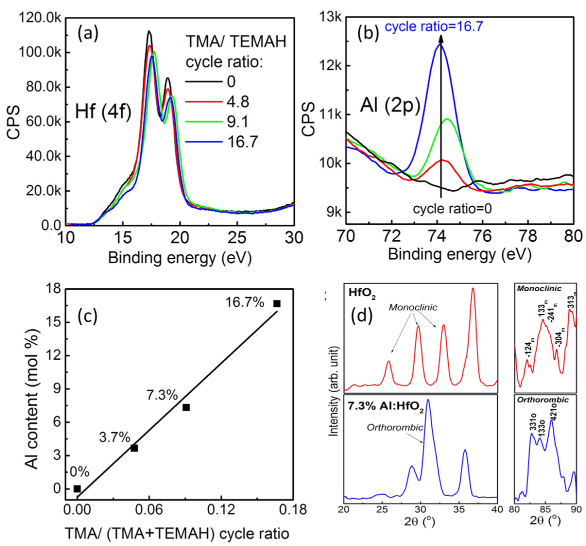
During the initial part of this project, we have developed a random-walk algorithm to find the best layout of magnetic-field sensors around a connector for measuring the internal connector currents in the presence of external magnetic field disturbances, nearby magnetizable materials, and conductors. The objective is to reduce the error of the measured currents to the same level as the inevitable noise in the magnetic field measurements. In parallel, we are building an experimental system to validate and demonstrate the ability to detect connector current.

Electronic Devices

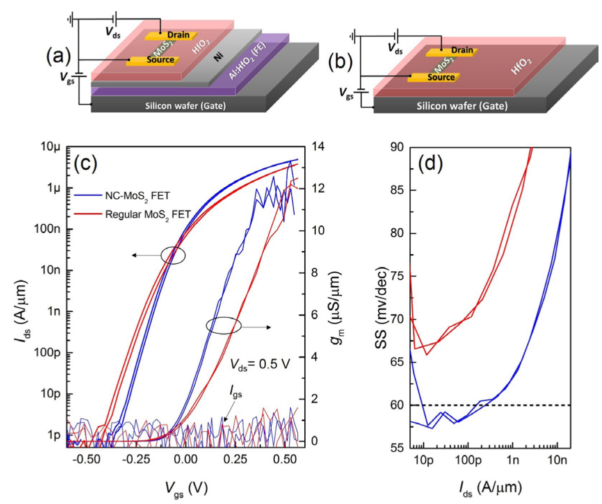
Subthreshold Swing Improvement in MoS_2 Transistors by the Negative-Capacitance Effect

A. Nourbakhsh, A. Zubair, S. Joglekar, M. Dresselhaus, T. Palacios
Sponsorship: ONR PECASE, ARO, NSF

Obtaining a subthreshold swing (SS) below the thermionic limit of 60 mV/dec by exploiting the negative-capacitance (NC) effect in ferroelectric (FE) materials is a novel effective technique to allow the reduction of the supply voltage and power consumption in field-effect transistors (FETs). At the same time, two-dimensional layered semiconductors, such as molybdenum disulfide (MoS_2), have been shown to be promising candidates to replace silicon MOSFETs in sub-5-nm-channel technology nodes. In this work, we demonstrate NC-MoS_2 FETs by incorporating a ferroelectric Al-doped HfO_2 (Al:HfO_2), a technologically compatible material, in the FET gate stack. Al:HfO_2 thin films were deposited on p^+Si wafers by atomic layer deposition. X-ray photoelectron spectroscopy (XPS) analysis was performed on the Al:HfO_2 films after varying the cycle ratio of Al and Hf precursors (Figure 1 a–c). The linear fit with near unity slope shows that the Al content can be precisely controlled in the range 0%–16.7%. Moreover, the X-ray diffraction (XRD) analysis suggests a phase transition from the monoclinic phase to the orthorhombic phase upon doping. This noncentrosymmetric transition phase is a prerequisite for ferroelectric characteristics. (Figure 1d). Voltage amplification up to 1.25 times was observed in a FE bilayer stack of Al:HfO_2/HfO_2 with Ni metallic intermediate layer. The NC-MoS_2 FET built on the FE bilayer showed a significant enhancement of the SS to 57 mV/dec, compared with SS_{min} = 67 mV/dec for the MoS_2 FET with only HfO_2 as a gate dielectric. The absence of hysteresis showed the effective stabilization of the NC by using the HfO_2/Al:HfO_2 bilayer.



▲ Figure 1: (a & b) XPS analysis of Al-doped HfO_2 films with different Al contents deposited on Si wafers with TMA/TEMAH cycle ratios ranging from 0 to 16.7%, (c) Al content of the Al:HfO_2 films extracted from the XPS spectra shown in (a) and (b) as a function of the TMA/TEMAH cycle ratio, (d) XRD patterns of undoped and 7.3% Al-doped HfO_2.



▲ Figure 2: Schematic of the NC-MoS_2 FET with a HfO_2/Al:HfO_2 bilayer stack with Ni used as the intermediate metal, (b) schematic of a reference regular MoS_2 FET with a HfO_2 gate dielectric. In both (a) and (b), a highly doped Si wafer is used as the back gate, (c) transfer characteristics and transconductance of the NC-MoS_2 FET and reference MoS_2 FET at room temperature, (d) comparison of the SS of the NC-MoS_2 FET with that of the reference MoS_2 FET.

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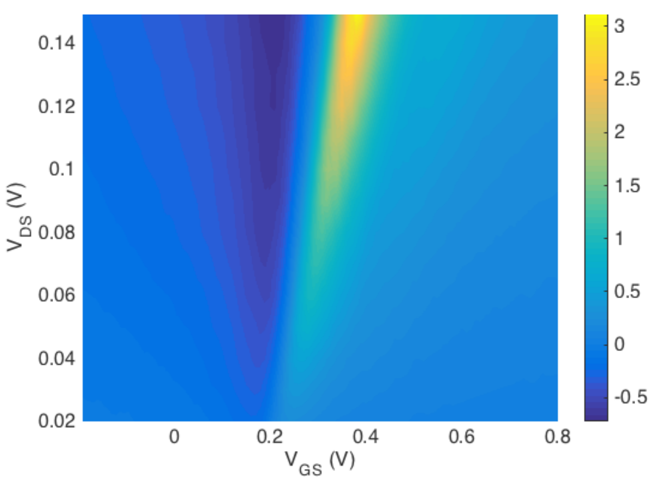
Frequency Response of Graphene Electrolyte-Gated Field-Effect Transistors (EGFETs)

C. Mackin, E. McVay, T. Palacios
Sponsorship: ISN

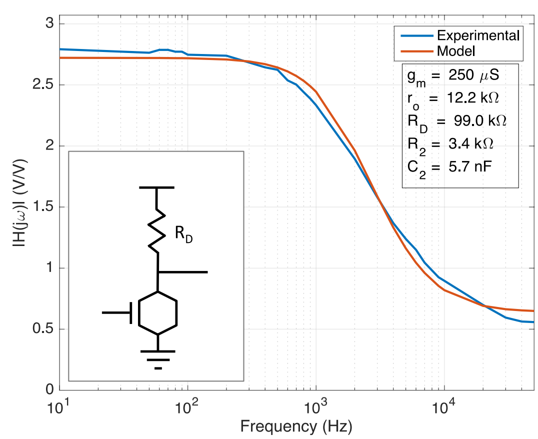
Graphene consists of an atomically thin layer of sp²-bonded carbon atom arranged in a hexagonal lattice. Graphene exhibits a number of promising electrical, optical, mechanical, and chemical properties making it well suited for a range of chemical and biological sensing applications. Graphene is chemically stable and does not form a native oxide, which enables a direct interface with many chemical and biological environments and allows graphene to take full advantage of ultrahigh interface capacitance resulting from the electric double layer phenomenon. This high interface capacitance, however, also raises the concern of impaired frequency response due to parasitics.

Two highly accurate models have been developed to study and predict the DC behavior of graphene electrolyte-gated field-effect transistors (EGFETs). Little work, however, has been reported on the AC capabilities of graphene EGFETs. An accurate frequency response model is critical for developing high-speed chemical and biological sensor applications.

This work develops a frequency-dependent small-signal model for graphene EGFETs. Graphene EGFETs are microfabricated to experimentally determine intrinsic voltage gain and frequency response and to develop a frequency-dependent small-signal model. Graphene EGFETs' small-signal model transfer functions are found to contain a unique pole due to an additional resistive element, which stems from the electrolyte gating of these devices. Intrinsic voltage gain, cutoff frequency, and transition frequency for the microfabricated graphene EGFETs are approximately 3.1 V/V, 1.9 kHz, and 6.9 kHz, respectively. This work marks a critical step in the development of high-speed chemical and biological sensors using graphene EGFET technology for a variety of applications such as electrophysiology.



▲ Figure 1: Intrinsic voltage gain as a function of drain-source voltage and gate-source voltage as calculated from DC characterization.



▲ Figure 2: Fit of experimental graphene EGFET magnitude response with newly developed small-signal model for graphene EGFETs (common-source amplifier configuration inset).

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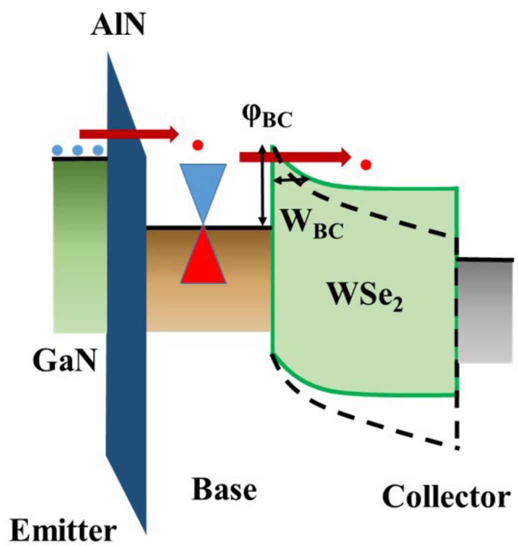
Graphene-on-GaN Hot Electron Transistor with van der Waals Heterojunction Base-Collector Junction

A. Zubair, A. Nourbakhsh, J.-Y, Hong, M. Qi, D. Jena, J. Kong, M. Dresselhaus, T. Palacios
Sponsorship: ARO, STC CIQM, NSF, AFOSR Foldable and Adaptive Two-dimensional Electronics MURI

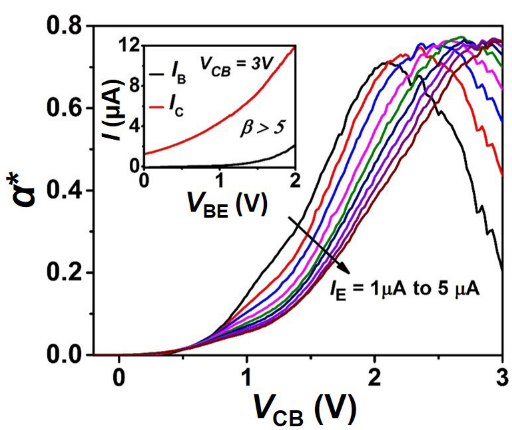
The hot electron transistor (HET) is a promising device concept that can potentially overcome the limitations of heterojunction bipolar transistors (limited by the diffusion of the minority carriers across the base) and high-electron- mobility transistors (limited by the saturation velocity of carriers and the lithography of the gate) in ultra-high frequency applications. The HET is a unipolar and majority carrier device in which the base-to-emitter voltage controls the transport of ballistic hot electrons through a transit layer smaller than the mean free path of the carriers. Single layer graphene is an ideal material for the base layer of HETs for potential THz applications. The ultra-thin body (~0.34 nm) and exceptionally long mean free path maximize the probability for ballistic transport across the base of the HET.

The existing graphene-base HETs with SiO_2/Si as an emitter stack suffer from low current density. In this work, we use 3-nm MBE-grown AlN on bulk ammonothermal n-GaN substrate. The GaN/AlN heterostructure has a higher tunneling current than Si/SiO_2 due to smaller conduction band offset at the junction. The epitaxial nature of the AlN/GaN also provides a high quality trap-free interface. The output current density and gain of the device depends on the extraction efficiency of the collector. The use of ALD dielectrics with large conduction band offset as collector barriers in existing HETs not only reduces the current density but also creates defect on the graphene surface during deposition. However, the atomic layers of two-dimensional materials (i.e. WSe_2) can be mechanically transferred onto any arbitrary substrate or paired with another atomic layer (i.e. graphene) to form a van der Waals heterojunction with a defect-free, sharp interface.

We demonstrate, for the first time, the operation of a high performance HET using a graphene/WSe2 as a base-collector barrier. The resulting device, with a GaN/AlN heterojunction as emitter, exhibits a current density of 50 A/cm_2, current gain above 3, and 75% injection efficiency, which are record values among graphene-base HETs. These results not only provide a scheme to overcome the limitations of graphene-base HETs toward THz operation but are also the first demonstration of a GaN/vdW heterostructure in HETs, revealing the potential for novel electronic and optoelectronic applications.



▲ Figure 1: Schematic on-state energy band diagram of an HET with GaN/AlN emitter stack and graphene/WSe_2 base-collector stack when V_{CB} > 0V (dotted line) and V_{CB} < 0V (solid line).



▲ Figure 2: Injection efficiency as function of V_{CB} at different constant emitter injections in common-base mode. Inset shows the Gummel plot of the same device at V_{CB} = 3V.

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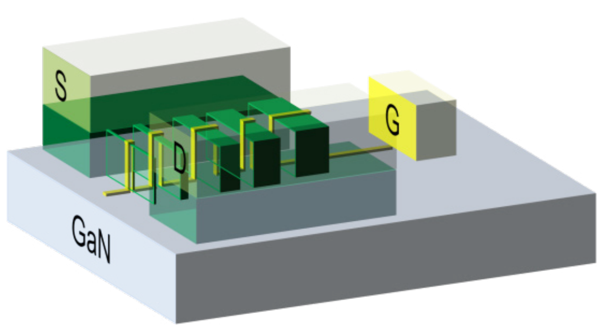
High Linearity GaN-Transistors for RF and High Power Amplification

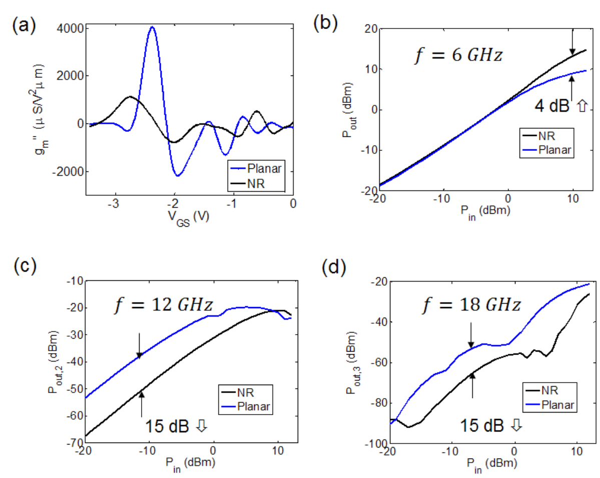
S. Joglekar, U. Radhakrishna, T. Palacios
Sponsorship: RUAG, ONR PECASE

The recent proliferation of mobile devices and the surge in the demand for internet of things (IoT) is promoting the need for efficient wireless data communication. Key emergent applications ranging from 5G-LTE, WIMAX, Sat-Com, and CAT-TV to radar, space applications, D2D, and other communication protocols in the range of L-band to millimeter-wave must operate within stringent constraints on the spectral bandwidth and adjacent-channel interference. In addition, the base station accounts for 56% of the total power consumed in a typical end-to-end cellular network; the RF power amplifier (PA) in the base station contributes a significant portion of this power budget. As a result, there is a strong need to achieve high-linearity high-efficiency PAs to avoid intermodulation distortion and channel interference.

In this work, we exploit the properties of the AlGaN/GaN heterostructure system, along with a new device architecture to attain device-level implementation of high linearity. The proposed device, seen in Figure 1, is based on a nano-ribbon (NR) structure. Numerous NRs with varying width form the channel of the transistor and are connected in parallel to form the device. In comparison to a planar AlGaN/GaN transistor of the same effective width, the NR-GaNFET displays a lower g”m (double derivative of transconductance, an important measure of linearity), as seen in Figure 2a. In addition, large signal linearity improvement has been demonstrated in these NR-based devices. Figure 2b shows that use of this approach improves the fundamental output power and delays the saturation in output power P_{out} at 6 GHz. Simultaneously, the harmonic outputs at 12 and 18 GHz are reduced considerably compared to a planar device, as seen in Figures 2c and d. In conclusion, high linearity in GaN transistors is demonstrated by both DC and large signal measurements using the new device architecture.



▲ Figure 1: Schematic of NR structure device.



▲ Figure 2: Device data for planar and NR device showing (a) g''_m vs. gate voltage, showing lowering of g''_m for NR device, (b) delayed output power saturation for an NR device; (c) and (d) lower first and second harmonic outputs, respectively, for a NR device.

Novel Device Design for High Linearity GaN Power Amplifier

J. Hu, D. Piedra, U. Radhakrishna, J. Grajal, T. Palacios
Sponsorship: RUAG

Gallium nitride (GaN)-based high-electron-mobility transistors (HEMTs) have been an emerging technology for the use in next-generation wireless communication systems. The combination of high-electron-mobility and critical electric field allows unprecedented power levels, power-added-efficiency (PAE), and breakdown voltage in GaN power amplifiers (PAs). Despite the advances in GaN radio frequency technology, the non-linearity characteristics of GaN PAs and the impact on the circuit performance have not been thoroughly investigated.

The goal of this project is to understand the key device design parameters and their impact on the amplifier linearity, eventually to improve the g_m and f_T linearity characteristics of GaN PAs by means of device-level and thermal design without compromising the aforementioned figures of merit.

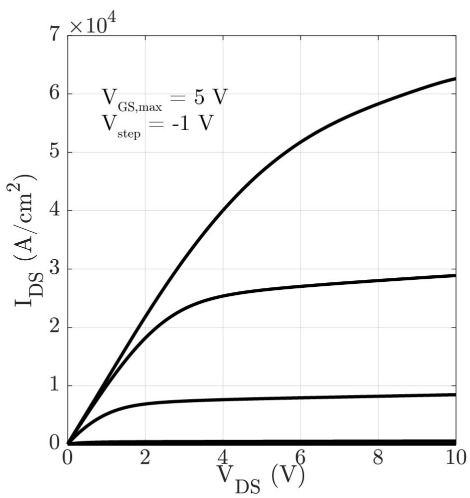
From the results based on the MIT Virtual Source GaNFET-RF model, we understand that the primary non-linear content in g_m occurs in the region of transition from weak to strong accumulation. This causes significant higher-order harmonic components and intermodulation distortion in power amplification. To solve this problem, we propose several new approaches to engineer the transition between weak and strong accumulation in GaN multi-finger power amplifiers. In this way, we are able to tailor the overall transconductance characteristics, and thus the IMD due to higher order transconductance can be minimized.

Vertical GaN Power FinFETs on Bulk GaN Substrates

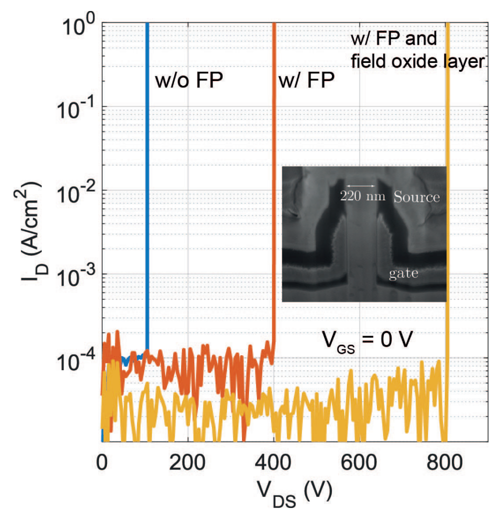
M. Sun, Y. Zhang, T. Palacios
Sponsorship: ARPA-E

Lateral GaN transistors on Si substrates with operating voltage up to 650 V are now commercially available. However, for high-voltage high-current applications, a vertical structure is preferred because 1) its die area does not depend on the breakdown voltage; 2) the surface is far from the high electric field regions, which minimizes trapping effects; and 3) high current levels are typically possible, thanks to the easier current extraction when the source and drain contacts are positioned vertically on opposite sides of the wafer. The most studied vertical GaN transistor structures, the current aperture vertical electron transistor (CAVET) and trench metal–oxide–semiconductor field-effect transistors (MOSFETs), have made significant progress in performance, but they still face great challenges. One of the major challenges for these two structures is the p-GaN layer. A GaN vertical power Fin field-effect transistor (FinFET) with only n-type GaN epilayers is demonstrated, as shown in the cross-sectional scanning electron microscope (SEM) image in Figure 2. The current is controlled through a sub-micron fin-shape vertical channel, which is surrounded by gate metal electrodes.

An enhancement-mode GaN vertical power FinFET with sub-micron channels is demonstrated. Combining dry/wet etching achieves a smooth vertical fin profile. The fabricated transistor showed a threshold voltage of 1 V and specific on resistance of 0.089 mΩcm² (Figure 1) with a highly doped n⁺ GaN cap layer. The I_{on}/I_{off} ratio is up to 10^{11}. The subthreshold swing is 75 mV/dec; the hysteresis is very small, which demonstrates the excellent material quality of the wet-etched sidewall. By proper engineering, the peak electric field distribution, a blocking voltage of 800 V was achieved (Figure 2). These results make this vertical GaN power FinFET very promising for high-voltage, high-current, low-cost, high-performance power electronics applications. Detailed information about this technology appears in the third reading.



▲ Figure 1: Output characteristics of the power FinFET with channel length 250 nm. The current density is calculated by averaging the active fin areas of the transistor.



▲ Figure 2: Off-state leakage curves of three transistor edge termination designs: 1) without field plate, 2) with field plate, and 3) with both field plate and field oxide. The inset shows the cross-sectional SEM image of the power FinFET.

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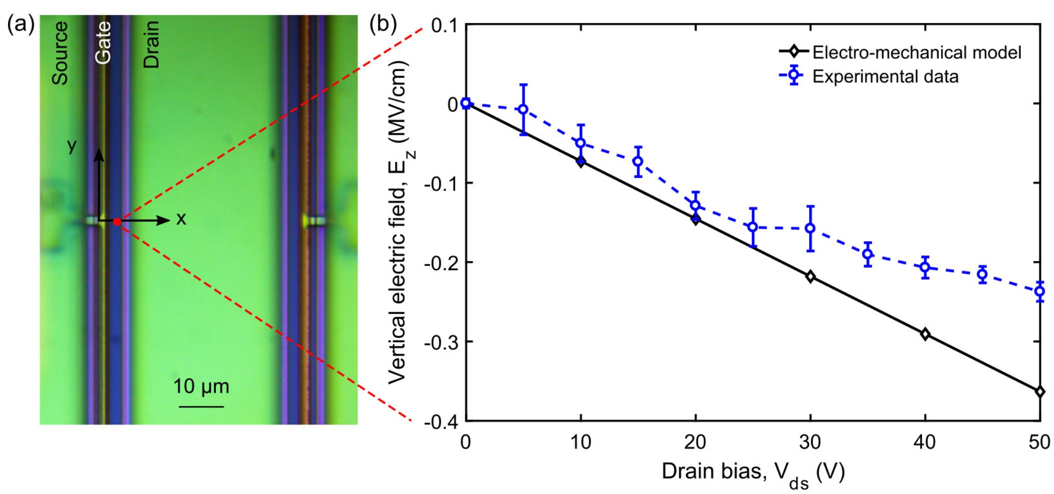
Local Stress and Electric Field Measurements in GaN HEMTs with Micro-Raman Spectroscopy

K. R. Bagnall, C. E. Dreyer, D. Vanderbilt, E. N. Wang
Sponsorship: MIT/MTL GaN Energy Initiative, ONR, SMART-LEES

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are one of the most promising compound semiconductor technologies for high power amplifiers and high voltage power conversion systems. However, elevated channel temperatures and high electric fields in critical areas of these devices are believed to cause performance degradation and premature failure through structural damage and electrochemical reactions. Thus, achieving the full potential of GaN-based transistors requires state-of-the-art experimental characterization techniques with high spatial resolution and multiphysics modeling of self-heating, thermoelastic, and piezoelectric effects.

In this work, we have developed an experimental technique for simultaneously measuring the vertical electric field along the c-axis and the inverse piezoelectric (IPE) stress in the c-plane with ≈1 μm spatial resolution via micro-Raman spectroscopy. In collaboration with computational material scientists at Rutgers University, we discovered the correct electric field dependence of the optical phonon frequencies of wurtzite GaN, which are strongly affected by the E_z field component through the internal structural r parameter. We found that the vertical electric field shown in Figure 1 more strongly shifts the optical phonon frequencies in GaN HEMTs measured by micro-Raman spectroscopy than the in-plane stress does. For the first time, we demonstrated experimental measurement of the electric field in a semiconductor device with micro-Raman spectroscopy and gained detailed insight into the role of impurities in the GaN buffer on the electrostatic behavior of the transistor. This work represents a new opportunity to perform simultaneous electrical, thermal, and mechanical measurements in semiconductor devices with a single experimental technique. We anticipate that our work will enable unprecedented insight into the complex electro-thermo-mechanical physics of GaN transistors and enable the development of GaN HEMTs with record performance and reliability.



▲ Figure 1: (a) Optical microscope image of the GaN HEMT under test. (b) The average vertical electric field in the gate-drain access region derived from the experimental micro-Raman measurements and the 3-D electro-mechanical model of the HEMT, which agree quantitatively to within 35%.

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Reliability of GaN-Based Devices Integrated with Silicon

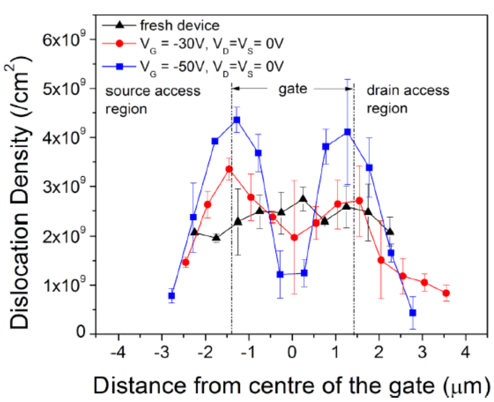
W. A. Sasangka, G. J. Syaranamual, R. I. Made, C. L. Gan, C. V. Thompson
Sponsorship: SMART

There is strong interest in monolithic integration of AlGaN/GaN high electron mobility transistors (HEMTs) and light emitting diodes (LEDs) with Si complementary metal-oxide semiconductor (CMOS) circuits. Also, the use of Si substrates for fabrication of GaN-based HEMTs and LEDs allows less expensive large-scale production and also opens up many new applications. However, the constraints on the reliability of these devices are still not fully understood

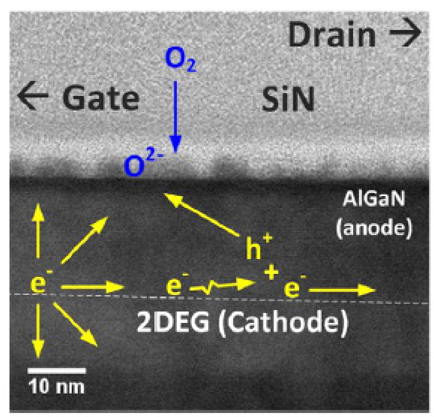
Dislocations are known to be associated with both physical and electrical degradation mechanisms of AlGaN/GaN-on-Si HEMTs. We have observed evidence for threading dislocation movement toward the gate-edges in AlGaN/GaN-on-Si HEMT under high reverse bias stressing (Figure 1). Stressed devices have higher threading dislocation densities (i.e., ~5 × 10^9/cm^2) at the gate-edges, as compared to unstressed devices (i.e., ~2.5 × 10^9/cm^2). Dislocation movement correlates well with high tensile stress (~1.6 GPa) at the gate-edges, as seen from inverse piezoelectric calculations and X-ray synchrotron diffraction residual stress measurements. Based on Peierls stress calculations, we believe that threading dislocations move via glide in ⟨11-20⟩/{1-100} and ⟨11-20⟩/{1-101} slip systems. This result illustrates the importance of threading dislocation mobility in controlling the reliability of AlGaN/GaN-on-Si HEMTs.

We have also investigated the influence of the two-dimensional electron gas (2DEG) in AlGaN/GaN HEMTs on their reliability under ON-state conditions. Devices stressed in the ON-state showed a faster decrease in the maximum drain current (IDmax) compared to identical devices stressed in the OFF-state with a comparable electric field and temperature. Scanning electron microscope (SEM) images of ON-state stressed devices showed pit formation at locations away from the gate-edge in the drain-gate access region. Cross-sectional transmission electron microscope (TEM) images also showed dark features at the AlGaN/SiN interface away from the gate edge (Figure 2). Electron energy loss spectroscopy (EELS) analysis of the dark features indicated the presence of gallium, aluminum and oxygen. These dark features correlate with pits observed in the SEM micrographs. We propose that in addition to causing joule heating, energetic electrons in the 2D electron gas contribute to device degradation by promoting electrochemical oxidation of the AlGaN.

In ongoing research we are investigating the effects of density of SiN passivation layers on the reliability of AlGaN/GaN-on-Si HEMTs and characterizing defects generated during constant current stressing of InGaN-on-Si LEDs.



▲ Figure 1: Threading dislocation density as a function of distance from the center of the gate for devices stressed at different gate voltages (VG).



▲ Figure 2: Electrochemical oxidation mechanism of AlGaN under on-state stressing.

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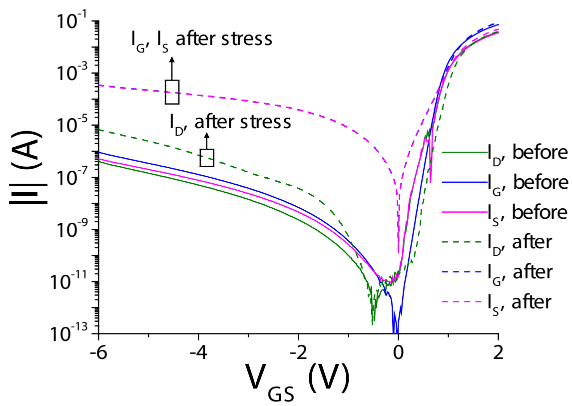
Gate Current Degradation of InAlN/GaN HEMTs under Electrical Stress

Y. Wu, J. A. del Alamo
Sponsorship: NRO

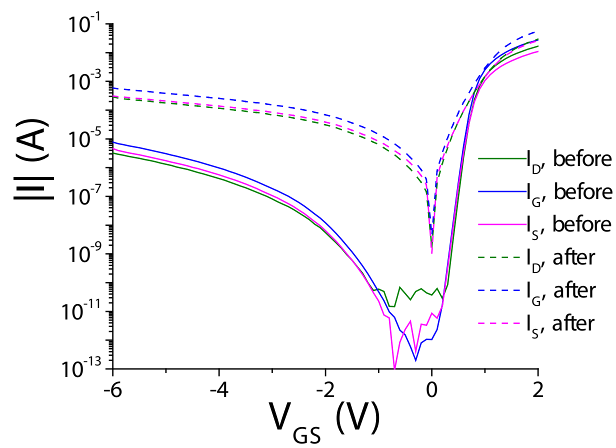
InAlN/GaN high-electron-mobility-transistors (HEMTs) have emerged as promising candidates for high-power millimeter wave applications due to their excellent gate-length scaling potential. This potential stems from the high spontaneous polarization of InAlN that yields a large 2DEG density at the InAlN/GaN interface even with a very thin barrier layer. However, in nanometer-scale InAlN/GaN HEMTs, the use of a very thin barrier layer brings gate leakage current and reliability concerns. Our work focuses on studying the degradation mechanisms of the gate leakage current under both ON-state stress and V_{DS} = 0 stress.

Under simultaneous high-power conditions (simultaneously high V_{DS} and I_D), besides drain current drop and a positive threshold voltage shift, we have observed an unusual leakage path being created between the gate and the source, as shown in Figure 1. We have proposed that under these conditions, the gate-source diode is strongly forward biased and there is significant gate current. The combination of high gate current, high temperature, and strong electric field across the AlN barrier on the source side generates defects, which increase gate leakage on that side of the device. In addition, local heating produces gate sinking and a positive V_T shift.

To further prove our hypothesis, we have conducted a room temperature V_{DS} = 0 V stress experiment with positive V_G increasing from 0.1 V to 2.5 V. Similar permanent electrical degradation was produced but this time on both the source and drain sides, as demonstrated by Figure 2. This degradation is consistent with our hypothesis that high forward V_G under high temperature leads to an anomalous gate leakage current increase.



▲ Figure 1: I_G-V_G characteristics (measured at 25°C) at V_{DS}=0 before (solid lines) and after (dashed lines) constant stress at $V_{DSstress}$ = 25 V and $I_{Dstress}$ = 400 mA/mm. I_S and I_D are also indicated. After stress, I_G and I_S increase by several orders of magnitude. In contrast, I_D shows a much smaller increase.



▲ Figure 2: I_G-V_G characteristics (measured at 25°C) at V_{DS}=0 before (solid lines) and after (dashed lines) positive V_G step-stress-recovery experiment with V_{DS}=0. I_S and I_D are also indicated. After stress, I_G roughly splits in half between I_D and I_S, indicating degradation on both source and drain sides of the device.

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OFF-State TDDB in High-Voltage GaN MIS-HEMTs

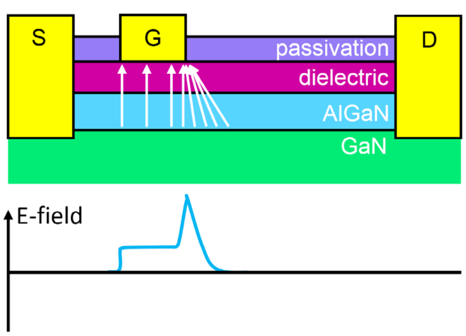
S. Warnock, J. A. del Alamo
Sponsorship: Texas Instruments

With the promise of higher-frequency, higher-temperature, and more efficient operation, GaN-based transistors show enormous potential for high-voltage power management applications. The AlGaN/GaN metal-insulator-semiconductor high electron mobility transistor (MIS-HEMT) is the most suitable device structure for power switches, offering lower gate leakage than its HEMT counterpart. GaN devices show great promise, but several reliability challenges remain to be addressed before these devices can achieve widespread commercial deployment. Time-dependent dielectric breakdown (TDDB), a catastrophic condition arising after prolonged high-voltage gate stress, is a particularly important concern.

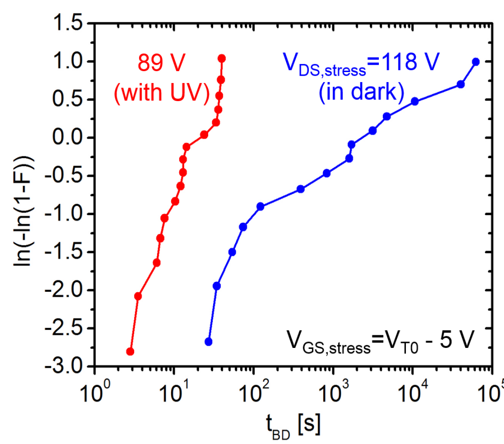
In this work, we explore TDDB under OFF-state conditions; that is, a negative gate bias is used to turn off the channel, and a high positive bias is applied to the drain terminal. This is the most common state of a power switching transistor in a power management circuit. In the OFF state, there is a high electric field through the gate dielectric at the gate edge on the drain side, as shown in Figure 1. Under prolonged stress, this will inevitably result in dielectric defect formation and eventual dielectric breakdown. It is uncommon to think of TDDB under OFF-state conditions; although there is limited work on this topic in GaN HEMTs, this reliability concern in MIS-HEMTs has thus far been overlooked.

We find that in OFF-state stress, the presence of transient instabilities such as current collapse and threshold voltage (VT) shift have a dramatic impact on the device TDDB statistics, as seen in Figure 2. The statistics in blue result from OFF-state TDDB experiments in the dark: they do not follow the expected linear distribution, and the breakdown times span many orders of magnitude. By using ultraviolet (UV) light during stress to prevent pervasive trapping-related effects, we can observe intrinsic TDDB behavior, as shown by the data in red. The use of UV light highlights the fact that trapping effects during stress cause significant overestimation of device breakdown voltage under OFF-state stress conditions.

In order to develop accurate lifetime models for GaN MIS-HEMTs, much care must be taken to ensure that a device's lifetime does not become distorted by transient trapping-related degradation effects.



▲ Figure 1: Sketch of a GaN MIS-HEMT illustrating the electric field distribution across the gate dielectric during OFF-state stress. Electric field lines in white yield the electric field profile in blue.



▲ Figure 2: Weibull plot of time-to-breakdown t_{BD} for OFF-state stress experiment without UV light in blue, and under illumination by 3.5 eV UV light, in red. $V_{DS,stress}$=89 V for UV data and 118 V for measurements in the dark. $V_{GS,stress}$= V_{T0}-5 V.

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Time-Dependent Dielectric Breakdown in High-Voltage GaN MIS-HEMTs: The Role of Temperature

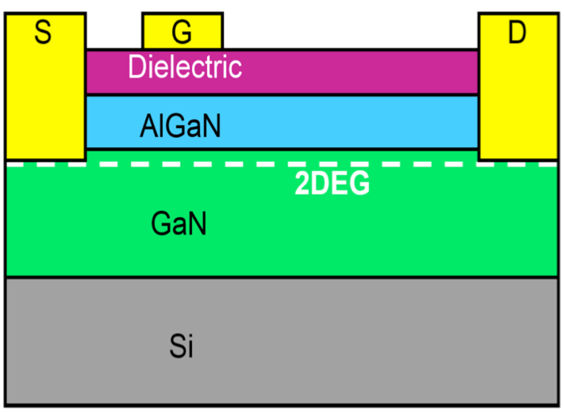
A. Lemus, S. Warnock, J. A. del Alamo
Sponsorship: Texas Instruments

There is a large demand for energy-efficient power electronics, for which silicon-based devices – the current market standard – are not ideal. GaN, however, has material properties (such as its large band gap of 3.4 eV) well-suited for power efficiency. GaN-based transistors offer a promising solution for these applications, but several reliability challenges remain. The motivation of our work is to address a specific reliability concern and failure mode known as time-dependent dielectric breakdown (TDDB). We study GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs), sketched in Figure 1, which have a lower gate leakage than HEMTs, as necessary for power switches.

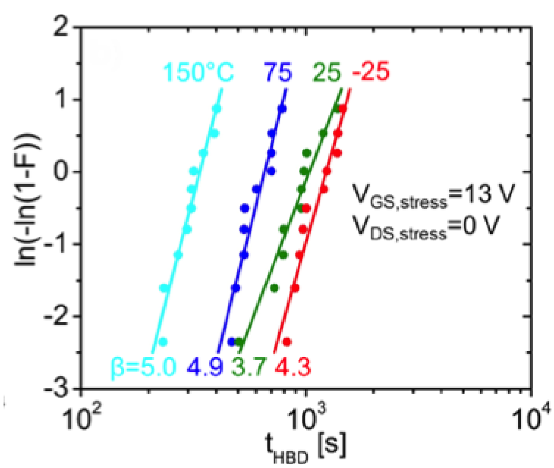
Time-dependent dielectric breakdown (TDDB) is a catastrophic event that occurs in field-effect transistors under prolonged high-voltage gate bias stress. This results in defect formation in the device dielectric, which facilitates current flow between the gate and its conductive channel. Eventually, a highly conductive path will suddenly form in the dielectric. The instantaneous power dissipation through the path creates a short that destroys the device. Our interest is in exploring how this TDDB mechanism occurs in GaN devices and how it is affected by temperature.

We choose to conduct our TDDB experiments at several different temperatures under constant positive gate voltage stress. We observe a negative correlation between temperature and the breakdown time of our devices, as Figure 2 shows. However, we also found that the activation energy for TDDB in these devices is rather small. In fact, it is significantly smaller than other reported values in the GaN MIS-HEMT system.

This research ultimately aims to contribute to the understanding of TDDB in GaN MIS-HEMTs towards the goal of developing a TDDB lifetime model.



▲ Figure 1: Structure of GaN MIS-HEMT used for this TDDB study.



▲ Figure 2: Weibull distribution for time to hard breakdown (tHBD) for devices at four different temperatures. Hard breakdown occurred sooner in devices tested at higher temperatures.

FURTHER READING

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- S. Warnock and J. A. del Alamo, "Progressive Breakdown in High-Voltage GaN MIS-HEMTs," presented at the *IEEE International Reliability Physics Symposium (IRPS)*, 2016.
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Gate Dielectric Reliability under AC Stress in High-Voltage GaN Field-Effect Transistors

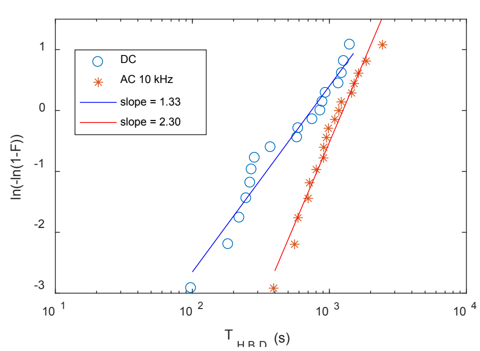
E. S. Lee, S. Warnock, J. A. del Alamo
Sponsorship: Texas Instruments

Energy-efficient electronics have been gaining attention as a solution to meet the growing demand for energy and sustainability. GaN field-effect transistors (FET) show great promise as high-voltage power transistors due to their ability to withstand a large voltage and carry large current. However, at the present time, the GaN metal-insulator-semiconductor high-electron-mobility-transistor (MIS-HEMT), the device of choice for electric power management, is excluded from commercialization due to many challenges, including gate dielectric reliability. Under continued gate bias, the dielectric ultimately experiences a catastrophic breakdown that renders the transistor useless, a phenomenon called time-dependent dielectric breakdown (TDDB).

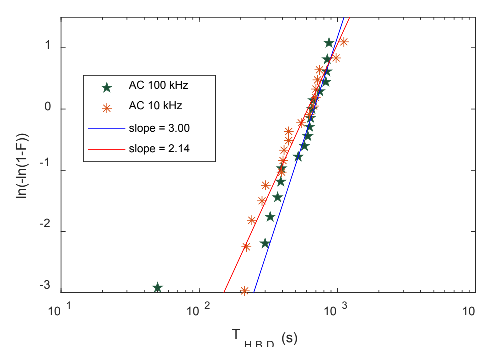
Our research aims to understand the physics of TDDB in GaN MIS-HEMTs. So far, efforts have been focused on constant stress due to the ease of experimental and instrumental setup. In contrast, our research aims to study the effects of applying AC stress to the gate. This mimics the real-world operating environment of FETs in power conversion circuits where they experience rapid transitions between different conducting states. In Si metal–oxide–semiconductor FETs (MOSFETs), a marked difference in TDDB time for AC stress and DC stress has been demonstrated. However, to our knowledge, similar studies have not yet been carried out in GaN MIS-HEMTs.

Figure 1 shows a comparison between the statistical distribution of dielectric hard breakdown times (T_{HBD}) for DC stress and AC stress under positive gate bias stress in transistors from our industrial collaborator. The statistical distribution of breakdown times follows the Weibull distribution. The plot graphs ln(-ln(1-F)) versus time to yield a linear fit, where F is the cumulative device failure fraction. We can see that, for the same conditions, AC stress at 10 kHz yields a statistical distribution with a longer hard breakdown time. Figure 2 shows that increasing the AC frequency beyond 10 kHz is of minimal relevance. These results may imply that the different voltages in AC stress may contribute to the recovery of the device.

While we are still in the very early stages of experimentation, we aim to show whether AC stress TDDB and DC stress TDDB in GaN MIS-HEMTs shows the clear difference observed in Si devices.



▲ Figure 1: Weibull plot of T_{HBD} for DC stress and AC stress at 10 kHz. DC: $V_{GS,stress}$ = 12.7 V, $V_{DS,stress}$ = 0 V. AC: $V_{GS\ Hi,stress}$ = 12.7 V, $V_{GS\ LO,\ stress}$=0 V, $V_{DS,stress}$ = 0 V, duty cycle = 50%, f = 10 kHz. There is a clear increase in T_{HBD} for AC stress.



▲ Figure 2: Weibull plot of T_{HBD} for AC stress at 10 kHz and 100 kHz. In both cases, $V_{GS\ Hi,stress}$ = 12.7 V, $V_{GS\ LO,\ stress}$=0 V, $V_{DS,stress}$ = 0 V, duty cycle = 50%. There is no significant change in T_{HBD} for the two frequencies.

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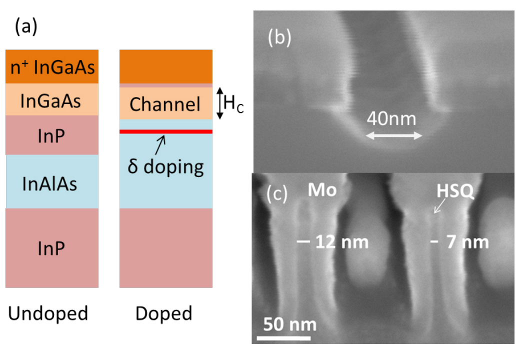
Effect of Doping on Self-Aligned InGaAs FinFETs

A. Vardi, J. A. del Alamo
Sponsorship: DTRA, Lam Research

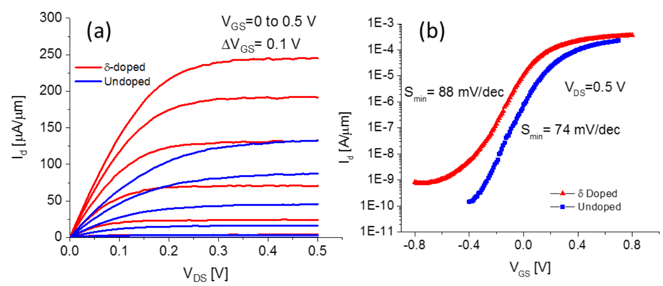
InGaAs is a promising candidate as channel material for complementary metal-oxide semiconductor (CMOS) technologies beyond the 7-nm node. In this dimensional range, only high aspect-ratio (AR) 3-D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive InGaAs Fin field-effect transistor (FinFET) prototypes have been demonstrated recently. However, as the fin width is scaled down to 10 nm, severe On-current degradation is observed. The origin of this performance degradation is still unclear.

In this work, we study the effect of δ-doping on the performance of self-aligned InGaAs FinFETs. We closely follow the fabrication process of self-aligned planar InGaAs quantum-well metal–oxide–semiconductor FETs (MOSFETs) realized previously but added a dry-recess process for the n^+ InGaAs cap. The starting material used for this study is shown in Figure 1(a). Low- resistivity Mo is first sputtered as contact metal, followed by SiO_2 chemical vapor deposition. The gate pattern is defined by electron-beam lithography. The SiO_2 and Mo layers are then etched by reactive ion etching (RIE). After this, the top n^+ InGaAs cap is dry-etched in a well-controlled manner (Figure 1b). Fins are then patterned in the recessed area using 60-nm-thick HSQ and E-beam lithography, and RIE etched. This process yields fins as narrow as 20 nm with an aspect ratio of 8. The fins are highly vertical in the top ~70 nm. After fin etching, several cycles of digital etching are applied to further reduce the fin width down to as low as 7 nm and reduce the sidewall roughness. Gate dielectric composed of 3-nm HfO_2 is deposited by atomic layer deposition and sputtered Mo is used as a gate metal and patterned by RIE. The device is finished by via opening and pad formation. In this process, the HSQ that defines the fin etch is kept in place. This makes our FinFETs double-gate transistors with carrier modulation only on the fin sidewalls (Figure 1c).

The electrical characteristics normalized to gate periphery ($2xH_c$), where H_c is the channel thickness defined in Figure 1a of a device with W_f=10 nm, L_g=50 nm (AR= H_c/W_f=5) for the structure w/ (red) and w/o (blue) δ-doping are shown in Figure 2a–b. Well-behaved characteristics and good sidewall control are obtained. R_{on} are 540 and 960 Ω·µm, and a peak transconductance, g_m, of 630 and 430 µS/µm are obtained at V_{DS}=0.5 V for the doped and undoped structures, respectively. Although the doped sample shows superior On performance, the Off current and subthreshold swing of the undoped sample are better. The saturated S_{min} is 88 and 74 mV/dec for doped and undoped samples, respectively. The reason for this performance difference is related to electrostatics within the fins. While in the undoped sample, carriers accumulate along the fin sidewalls, in the doped fins there are also carriers in the body of the fins. This enhances the conductivity of doped fins; however, it takes a larger negative gate voltage to deplete those fins, and the Off performance degrades.



▲ Figure 1: (a) Schematic diagram of doped and undoped epi structure. SEM image of (b) device with L_g=40 nm after dry recess and (c) fins in a finished device.



▲ Figure 2: Electrical characteristics of FinFET with L_g=50 nm and W_f=10 nm fabricated on doped (red) and undoped (blue) structures. (a) output and (b) subthreshold.

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High-Resolution Transmission Electron Microscopy of III-V FinFETs

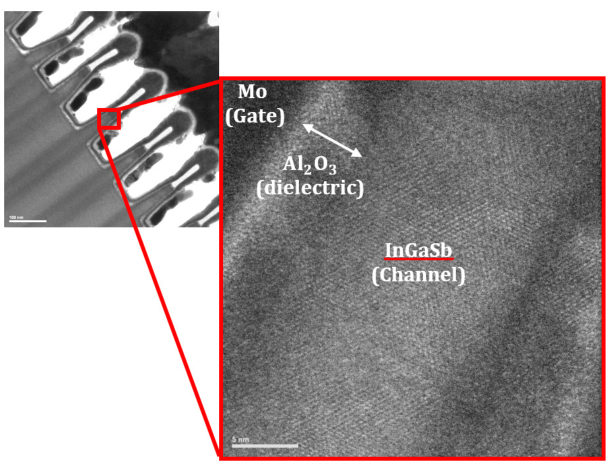
L. Kong, W. Lu, A. Vardi, J. A. del Alamo
Sponsorship: Lam Research, UROP

III-V materials have great potential for integration into future complementary metal-oxide semiconductor technology due to their outstanding electron transport properties. InGaAs n-channel metal-oxide semiconductor field-effect transistors have already demonstrated promising characteristics, and the antimonide material system is emerging as a candidate for p-channel devices. As transistor technology scales down to the sub-10-nm regime, only devices with a 3-D configuration can deliver the necessary performance. III-V Fin field-effect transistors (FinFETs) have displayed impressive characteristics but have shown degradation in performance as the fin width is scaled to the sub-10-nm regime. In this work, we use high-resolution transmission electron microscopy (HRTEM) in an effort to understand how interfacial properties between the channel and high-k dielectric affect device performance.

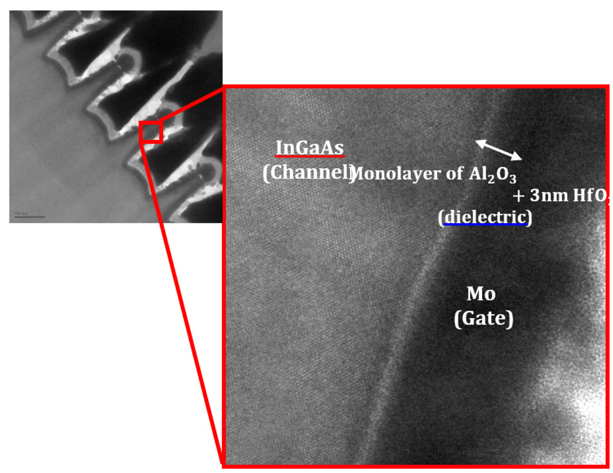
At the interface between the channel material, such as InGaSb or InGaAs, and the high-k gate dielectric, properties of interest include defect density, interdiffusion between the semiconductor and dielectric, and roughness of the dielectric-semiconductor interface. Using HRTEM, we can directly study this interface and try to understand how it is affected by different processing conditions and its correlation with device characteristics.

We have analyzed both InGaSb and InGaAs FinFETs. In electrical characteristics, InGaSb p-channel FinFETs with thinner fins display inadequate gate control of the channel current. HRTEM images of the InGaSb FinFETs reveal non-uniformity in the dielectric as well as interdiffusion between the InGaSb and (Figure 1). We are exploring different passivation techniques to improve this interface.

We have also performed HRTEM on novel InGaAs FinFETs with sub-10-nm fins that display superior electrical characteristics. HRTEM images show a clean interface between the dielectric and the channel (Figure 2). We are using HRTEM to further analyze the electrostatics and quantum behavior by analyzing fin width, shape, and crystallographic orientation.



▲ Figure 1: HRTEM image of InGaSb fin. The interface between the dielectric and channel is not sharp due to interdiffusion between InGaSb and Al_2O_3.



▲ Figure 2: HRTEM image of InGaAs fin. The interface between the dielectric and channel is sharp and well defined.

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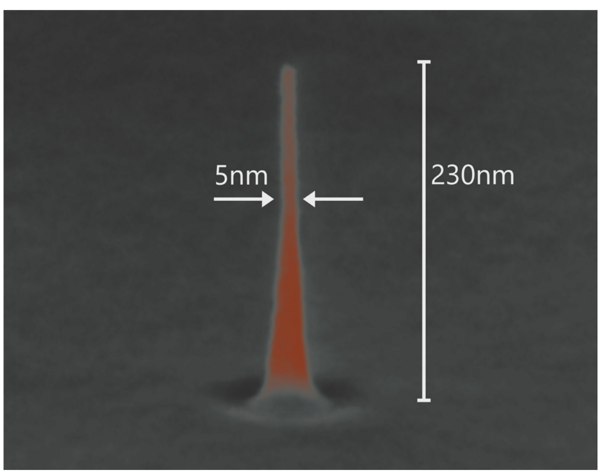
Digital Etching for Sub-10-nm III-V Multi-Gate MOSFETs

W. Lu, X. Zhao, J. A. del Alamo
Sponsorship: DTRA, Korea Institute of Science and Technology, Lam Research, NSF, Samsung

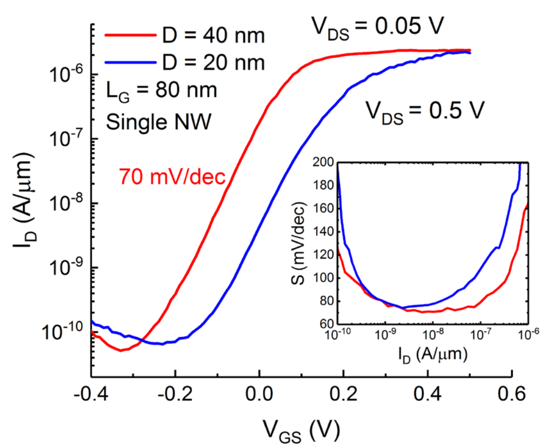
As complementary metal-oxide semiconductor (CMOS) technology keeps advancing, new materials are under active research in the hope of replacing Si in future generations. III-V multi-gate transistors such as InGaAs Fin field-effect transistors (FinFETs) or nanowire gate-all-around metal–oxide–semiconductor field-effect transistors (MOSFETs) are regarded as some of the most promising candidates. As the physical size of Si FinFETs is shrinking, it is critical to develop the technology to fabricate III-V 3-D devices in the sub-10-nm range. In this dimensional regime, precise etching control is the key challenge.

Digital etching is an etching technique that separates the oxidation and oxide removal steps characteristic of chemical etching. It makes both the oxidation and oxide removal self-limiting, thus enabling nanometer-scale control of the etching process. In the last few years, the use of digital etching has enabled demonstrations of aggressively scaled III-V FinFETs and nanowire MOSFETs. However, so far digital etching has been applied only to arsenide-based III-Vs. It is not applicable to highly reactive compounds such as antimonides. In addition, the mechanical yield of digitally etched vertical nanowires dramatically degrades at and below 10 nm in diameter.

In this project, we have developed a novel non-aqueous digital etching technique that enables the fabrication of sub-10- nm vertical fins and nanowires. The new approach uses acids dissolved in alcohol, which has less surface tension than water and therefore exerts smaller mechanical forces against the nanowires. We obtain a consistent 1 nm/cycle etching rate on both InGaAs- and InGaSb-based heterostructures. We show an over 97% yield in the fabrication of sub-10-nm vertical nanowires. We have also demonstrated a record 5-nm diameter nanowire with a height of 230 nm and an aspect ratio of 46. Finally, we fabricated InGaAs vertical single nanowire MOSFETs using this technique. Those transistors have a linear subthreshold swing of 70 mV/dec, one of the best values reported in such devices. The subthreshold swing shows that the new digital etching technique is effective in yielding a high-quality surface in InGaAs nanowires. We are now working towards applying this technique to demonstrate InGaAs and InGaSb FinFETs and vertical nanowire MOSFETs with sub-10-nm fin width and nanowire diameter.



▲ Figure 1: InGaAs vertical nanowire with 5-nm diameter, 230 height obtained after 10 cycles of digital etch in H_2SO_4: methanol.



▲ Figure 2: Subthreshold characteristics of single vertical nanowire transistors with 40- and 20-nm diameter, with lowest subthreshold swing of 70 mV/dec. The inset shows S vs. I_D of these devices.

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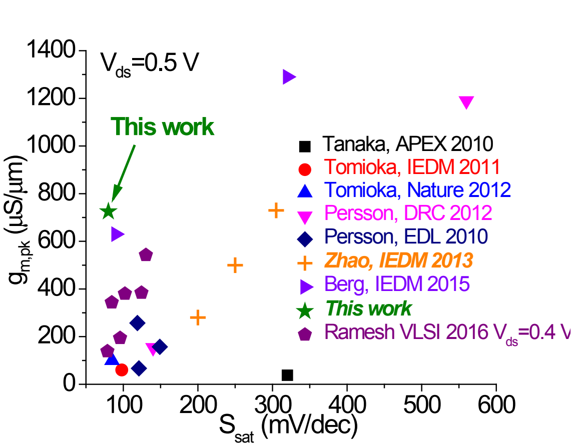
III-V Vertical Nanowire Transistors for Ultra-Low Power Applications

X. Zhao, A. Vardi, J. A. del Alamo
Sponsorship: NSF E3S STC, Lam Research, SRC

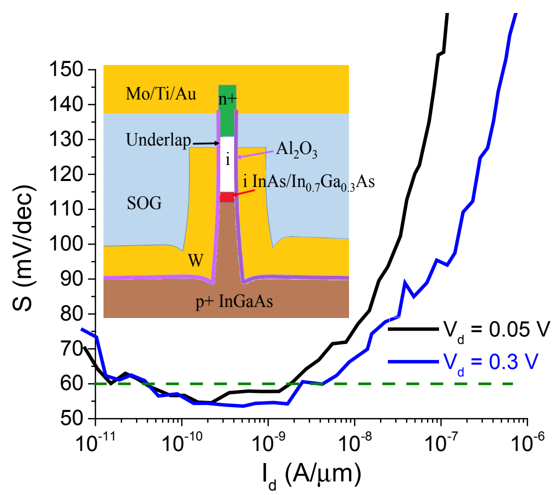
In future logic technology for the Internet of Things and mobile applications, reducing transistor power consumption is of paramount importance. Beyond Si complementary metal-oxide semiconductors (CMOS), transistor technologies based on III-V materials are widely considered as a leading solution to lower power dissipation by enabling dramatic reductions in the transistor supply voltage. Vertical nanowire (VNW) transistor technology holds promise as the ultimately scalable device architecture. VNW metal–oxide–semiconductor field-effect transistors (MOSFETs) have been predicted to offer significant advantages compared to their lateral counterpart in terms of density-performance-power tradeoffs. The VNW transistor architecture also fully unleashes the advantage of III-V materials by enabling bandgap engineering along the transport direction, opening the door for the tunnel-FET (TFET), a quantum device that potentially break the power limits of MOSFETs.

This work demonstrates InGaAs-based VNW MOSFETs and TFETs fabricated via a top-down approach. Record performance has been achieved in our latest InGaAs VNW MOSFETs in terms of the trade-off between subthreshold swing (S) and ON current, as benchmarked in Figure 1. The performance improvement over an earlier generation of MOSFETs comes mainly from a much better oxide/semiconductor interface enabled by improved atomic-layer-deposition chamber conditioning and rapid thermal annealing.

Stemming from the same reasons, our latest VNW TFETs have also shown state-of-the-art performance, delivering room-temperature sub-thermal S over two orders of magnitude of current (Figure 2). The current level of the steep slope region was also among the highest ever reported. The improved oxide/semiconductor interface also greatly suppressed the significant temperature dependence of our previous generation of TFETs, which was attributed to a tunnel-assisted generation process through a high concentration of interface traps. In our newest devices, the subthreshold swing appears to saturate at a very low level at low temperatures, highlighing the potential of the NW geometry.



▲ Figure 1: Benchmark of peak transconductance and minimum subthreshold swing at drain bias of 0.5 V for InGaAs and InAs VNW MOSFETs. A record I_{on} of 200 µA/µm is obtained at an I_{off} = 100 nA/µm and V_{dd} = 0.5 V.



▲ Figure 2: Subthreshold swing vs. I_d characteristics of an InGaAs/InAs heterojunction VNW TFET demonstrated in this work, revealing sub-thermal behavior over two orders of magnitude of current. Inset shows the TFET schematic cross section.

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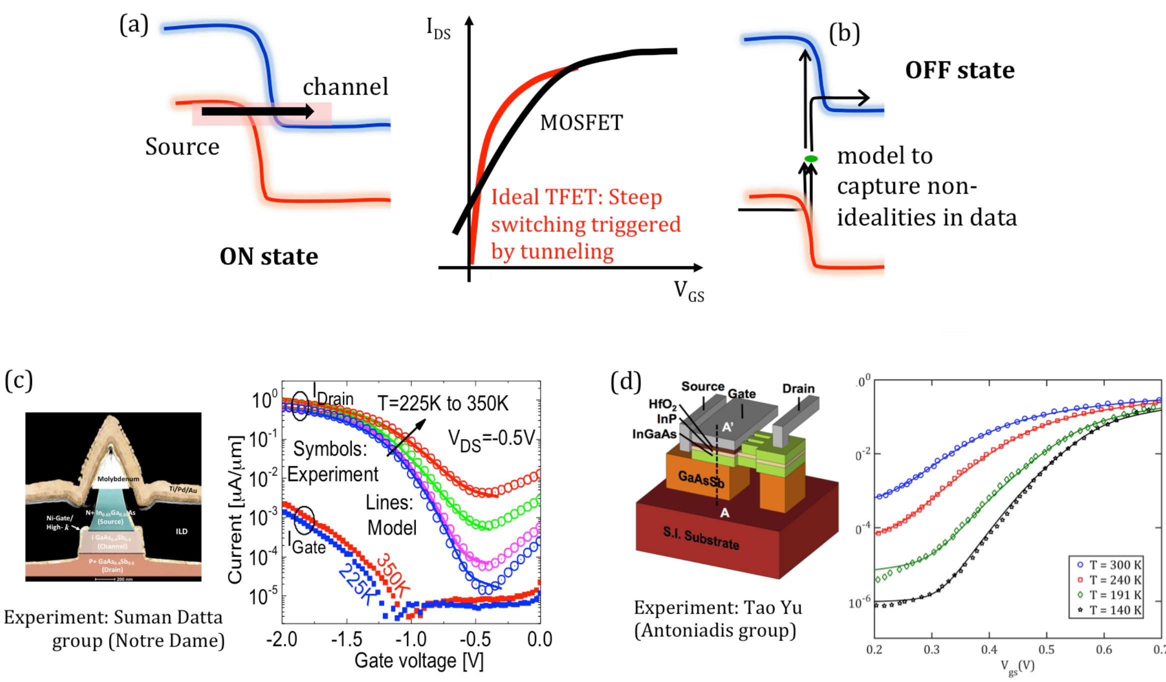
A Compact Tunnel Field-Effect Transistor Model Including the Impacts of Non-Idealities

R. N. Sajjad, U. Radhakrishna, W. Chern, D. A. Antoniadis
Sponsorship: NSF E3S, NSF/SRC NEEDS

The tunnel field-effect transistor (TFET) has the promise of low power switching due to its tunneling-dependent steep subthreshold swing (Figure 1a). Because of non-idealities such as the oxide-semiconductor interface traps and non-abrupt band edges (Figure 1b), practical TFETs produce higher leakage currents and higher subthreshold swing than ideal. We develop a physics-based compact model that captures these non-idealities. Our model also contains the details of TFET device physics such as the drain-voltage influence on the quantum capacitance, the superlinear output characteristics, negative differential resistance, etc. The model is tested against multiple TFET data. Figure 1c-d shows the model fits of two sets of experimental data. The minimum leakage current that originates from the trap assisted tunneling depends strongly on temperature in the experiments. The subthreshold swing decreases with reduced temperature since the contribution from the trap assisted tunneling decreases. Our model allows prediction of performance in the absence of interface traps and provides guidance for future material growth and device fabrication. Based on the compact model, we also developed a Verilog-A model that allows us to simulate circuits based on TFETs.



▲ Figure 1: (a) Ideal band to band tunneling in a TFET causes a steep switching in current under ideal conditions. The switching rate is steeper than in a MOSFET. (b) However, in practice, the OFF state current can still flow via surface traps and phonon emission, yielding a non-negligible source-drain current. (c-d) The compact model is applied to two different experiments, showing good agreement with the data at different temperatures.

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Metal Oxide Thin-Films as the Basis of Memristive Nonvolatile Memory Devices

T. Defferriere, D. Kalaev, J. L. M. Rupp, H. L. Tuller
Sponsorship: CMSE, NSF

The design of silicon-based memory devices over the past 50+ years has driven the development of increasingly powerful and miniaturized computers with the demand for increased computational power and data storage capacity continuing unabated. However, fundamental physical limits are now complicating further downscaling. The oxide-based *memristor*, a simple M/I/M structure, in which the resistive state can be reversibly switched by application of appropriate voltages, promises to replace classic transistors in the future. It has the potential to achieve an order-of-magnitude-lower operation power than existing *RAM* technology and paves the way for neuromorphic memory devices relying on non-binary coding. Our studies focus on understanding the mechanisms that lead to memristance in a variety of insulating and mixed ionic electronic conductors, thereby providing guidelines for material selection and for achieving improved device performance and robustness.

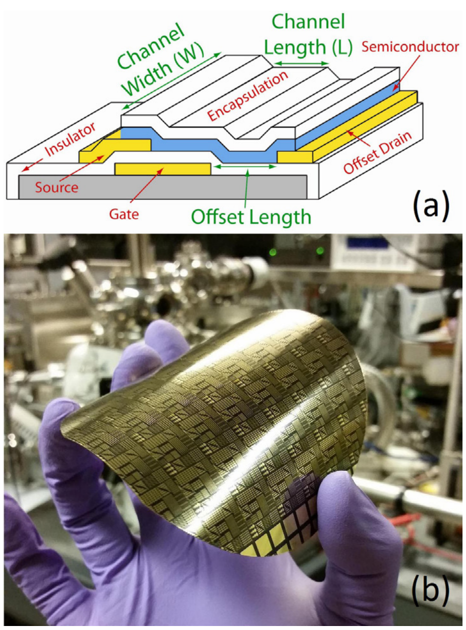
Solution-Processed High-Voltage Organic Thin-Film Transistor

A. Shih, A. I. Akinwande
Sponsorship: DARPA

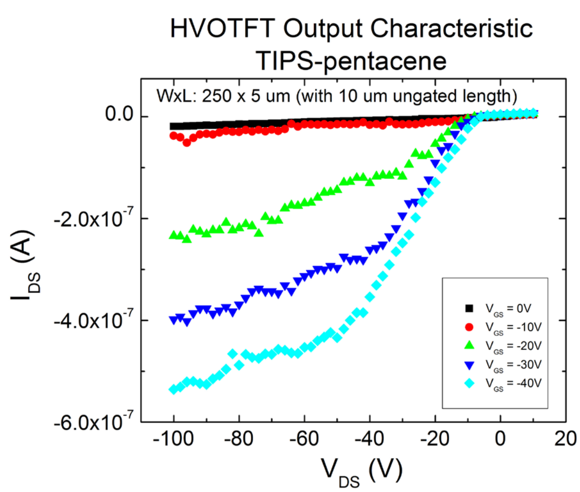
Organic-based thin-film transistors (OTFTs) have been identified as excellent candidates for flexible electronics due to the weak van der Waals forces between small molecules. Electronics and sensors based on OTFTs can be made on arbitrary curved surfaces, allowing for the development of wearable electronics such as artificial skin. However, enabling truly ubiquitous electronics through OTFTs demands not only a high performance, but also a wide range of operating voltages. There are many applications that demand a high operating voltage beyond that capable of a typical thin-film transistor. For example, ferroelectric liquid, electrophoretic or electro-optic displays, digital X-ray imaging, poly-Si cold cathodes, and other sophisticated integrated microelectromechanical systems (MEMS) all require large operating voltages to function.

In this work, we are developing a solution-processed high-voltage organic thin-film transistor (HVOTFT) based on the organic semiconductor TIPS-pentacene, operable at over a hundred volts. The design of the HVOTFT is shown in Figure 1a. We have employed a bottom contact architecture along with the dielectrics Parylene-C and BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$). The TIPS-pentacene is dissolved in a high boiling point solvent, and the solution is then drop-casted on top of the contacts to form the active thin-film. The key design structure is to introduce an ungated region in series with the traditional gated region. The gated region allows for standard transistor switching behavior, while the ungated region enables the high voltage operation by acting as a non-linear resistor.

The device has been successfully fabricated on glass substrates as well as on flexible polyimide wafers, as shown in Figure 1b. Currently, devices exhibit good performances with charge carrier mobility of ~0.05 cm²/V·s, I_{on}/I_{off} of 10^4 and operating voltages beyond 100 V, as shown in Figure 2. Although mobility, I_{on}/I_{off} ratio, and breakdown voltage are relatively low compared to our pentacene evaporated devices, recent efforts to have a self-patterned crystal growth for better thickness control as well as transistor isolation have proven promising.



▲ Figure 1: (a) Cross-sectional view of the HVOTFT, (b) OTFTs made on flexible polyimide substrates.



▲ Figure 2: High-voltage output characteristics of HVOTFTs made from TIPS-pentacene via drop-casting. The channel length is 5 μm with a 10-μm ungated region. The channel width is 250 μm.

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Energy

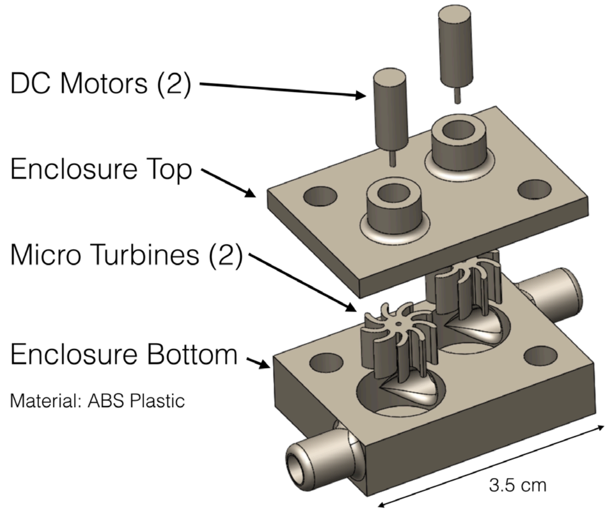
Energy Harvesting Footwear

H. Akay, R. Xu, S.-G. Kim
Sponsorship: SUTD

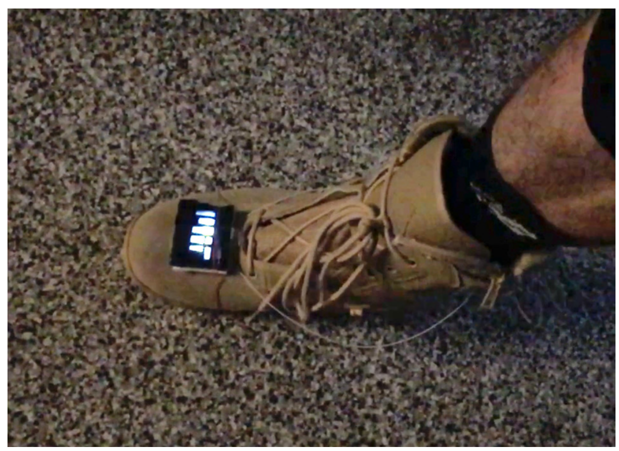
Most portable electronic devices are power-limited by battery capacity, and recharging these batteries often interrupts the user's experience with the device. This product presents an alternative to powering portables by converting regular human walking motion to electricity. The shoe design harvests electric power using rubber lungs, distributed in the sole of a running shoe, to drive a series of micro-turbines connected to small DC motors.

The number and position of lungs are optimized to harvest the maximum airflow from each foot-strike. The rubber lungs exhale when compressed and inhale during decompression. The turbine enclosure is designed symmetrically so that regardless of the direction of flow, the turbines continue to spin in the same direction. Therefore, energy is harvested during both stepping and lifting-off of the foot.

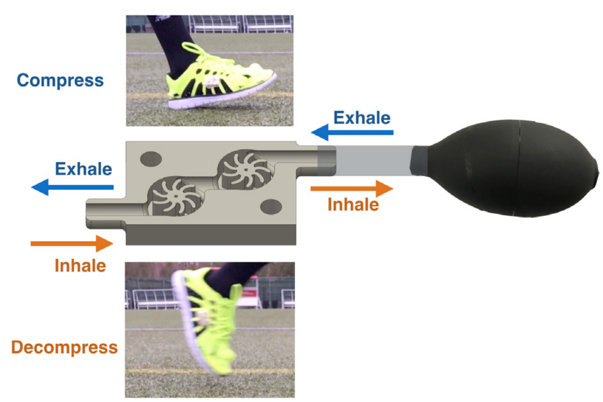
A prototype shoe was fitted on the right foot of a 75-kg test subject and produced an average continuous power of 90 mW over a 22.4 Ω load during walking at 3.0 mph. Ongoing research includes applying this design to a fully functional boot that transmits GPS coordinates, powered solely by the user's footsteps.



▲ Figure 1: Exploded view of dual-turbine air harvester assembly.



▲ Figure 2: MIT Logo illuminated by a single footstep.



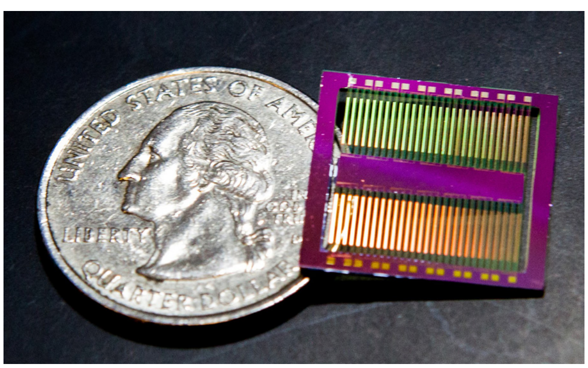
▲ Figure 3: Pump system inhales and exhales, driving turbines continuously

MEMS Energy Harvesting from Low-Frequency and Low-Amplitude Vibrations

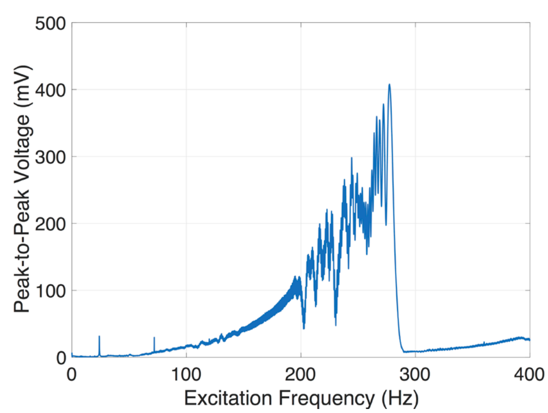
R. Xu, H. Akay, S.-G. Kim
Sponsorship: MIT-Singapore University of Technology and Design International Design Center

Vibration energy harvesting at the micro-electrical-mechanical system (MEMS) scale will promisingly advance exciting applications such as wireless sensor networks and the Internet of Things by eliminating troublesome battery-changing or power wiring. On-site energy generation could be an ideal solution to powering a vast number of distributed devices usually employed in these systems. To enable the envisioned battery-less systems, a fully assembled energy harvester at a size of a quarter-dollar coin should generate robustly 101~102µW of continuous power from ambient vibrations (mostly less than 100 Hz and 0.5 g acceleration) with wide bandwidth. We are inching close to this goal in terms of power density and bandwidth, but not in terms of low-frequency and low-amplitude operations. Our previous research with nonlinear resonating bridge-structure-based energy harvesters achieved 2.0 mW/mm3 power density with >20% power bandwidth. However, they were operated with input vibrations of >1 kHz at 4 g, which practically limits the use of this technology for harvesting energy from real environmentally available vibrations. Many believed this is an inherent limitation imposed on the MEMS-scale structures.

We approached this problem with a buckled-beam-based bi-stable nonlinear oscillator. Compared to mono-stable nonlinear oscillations, we found bi-stable oscillations could bring more dynamics phenomena to help reduce the operating frequency. An electromechanical lumped model has been built to simulate the dynamics of the clamped-clamped buckled beam based piezoelectric energy harvesters. A meso-scale prototype verified the theoretical prediction, showing that the same energy harvester in a bi-stable configuration generated more power than the mono-stable configuration at lower frequencies. Residual stress-induced buckling was proposed and implemented through micro-fabrication to build the MEMS energy harvester. The multi-layer bridge structure has employed compressive residual stress in the micro-fabricated thin-films to reach overall compression and balanced stress distribution with respect to the neutral axis. As a main control parameter, the total compression can be tuned to exceed the critical buckling load and induce buckling. The buckled beam oscillates nonlinearly at large amplitude to maintain a wide bandwidth at much lower frequencies. The MEMS prototype of a quarter-dollar coin size (Figure 1) has been built and is being tested. The preliminary testing shows an order-of-magnitude-lower operating frequency range than the same sized mono-stable device we previously developed (Figure 2).



▲ Figure 1: The quarter-dollar coin-sized MEMS energy harvester (18mm × 18mm). The harvester consists of arrays of buckled beams coupled with a central proof mass.



▲ Figure 2: Frequency response (open-circuit voltage) of the MEMS prototype. The input vibrations from the electromagnetic shaker swept from 20Hz to 1000Hz at 0.5g.

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Broadband Acoustic Energy Harvesting via Synthesized Electrical Loading

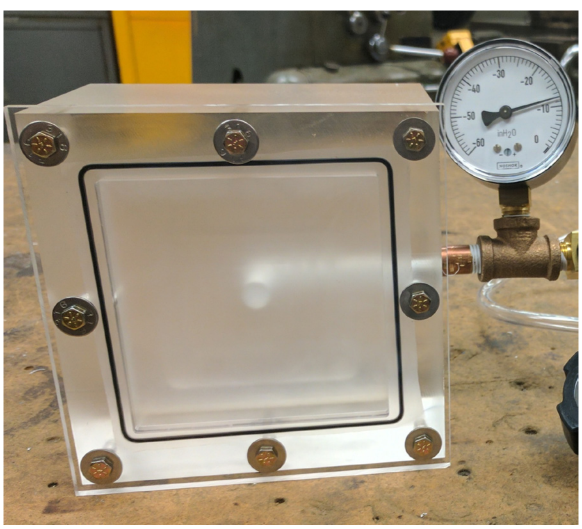
N. M. Monroe, J. H. Lang, A. P. Chandrakasan
Sponsorship: Ferrovial, S. A.

With the rise of the Internet of Things and connected devices, the need for self-powered wireless sensor nodes is ever increasing. One promising technology for self-powered sensor nodes in noisy environments is acoustic energy harvesting: deriving energy from ambient sound. Current acoustic energy harvester designs have limited performance; they are typically based on resonant structures, yielding narrowband energy collection and therefore low energy collection from broadband noise sources. In addition, current acoustic energy harvesters tend to the micro-electro-mechanical scale (square microns), with consequently low power outputs. This work addresses the size and bandwidth limitations of such harvesters. A large-scale acoustic energy harvester is designed based on piezoelectric polyvinylidene fluoride (PVDF) film tens of square cm in size, with the potential to scale further.

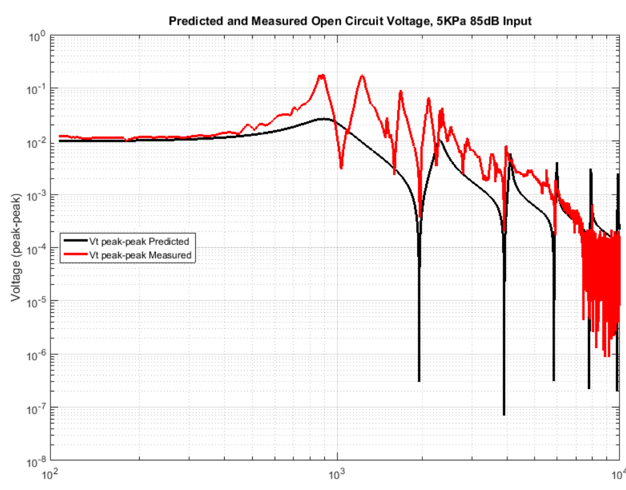
An energy-based dynamics analysis of such a system driven by an acoustic source yields an equivalent electromechanical resistor-inductor-capacitor (RLC) circuit model and subsequently a Thévenin equivalent model, looking into the piezoelectric element's terminals. Optimal broadband energy harvesting is achieved with a conjugate matched load over broad a frequency range. Such a load is realized as a combination of resistive and negative capacitive impedances. We realize this load initially with operational amplifier circuitry and later losslessly (in theory) using power factor correction-like switched H-bridge circuitry, with control algorithms to force a transfer function impedance of voltage and current. Essentially reactive power is invested in exchange for an increase in real power.

The harvester prototype has been fabricated (see Figure 1) and electromechanical model validated experimentally (see Figure 2). The load circuitry is in initial stages of testing, with a focus on broadband energy harvesting between 50-1000 Hz.

A successful result could pave the path towards acoustically powered sensor nodes, particularly in the case of broadband noisy environments such as airports and highways. There is also potential for application in the context of noise isolation.



▲ Figure 1: Assembled acoustic energy harvester with active collection area of 100 cm².



▲ Figure 2: Modeled (black) and measured (red) open circuit voltage of harvester with 85 dB acoustic input. Model considers only first mode of film motion.

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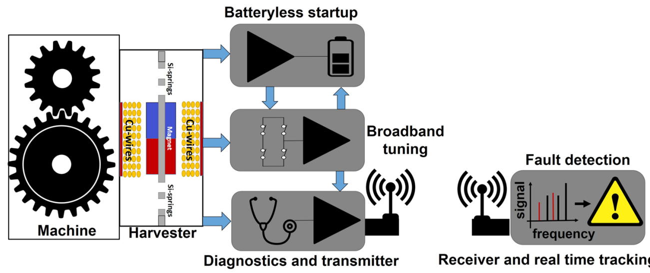
MEMS-Based Energy Harvesting System for Machine Health Monitoring

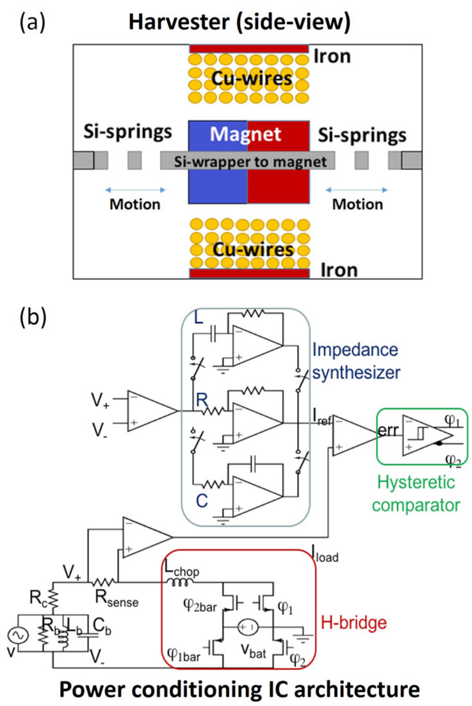
A. Shin, U. Radhakrishna, J. H. Lang, A. P. Chandrakasan
Sponsorship: Analog Devices, Inc.

Vibration-based machine health monitoring provides an effective method of tracking the real-time performance of machines to enable predictive maintenance and avoid machine downtime. Sensors are attached to the vibrating parts that can provide data indicative of machine health. The key challenges to powering such systems are building sensors that can operate at low vibration signals, tolerance to manufacturing variations, a small form-factor, designing low-power electronics for battery-less operation, and efficient power extraction.

To support such systems, a Lorentz-force-based micro-electrical-mechanical (MEMS) energy harvesting system is proposed that can extract 50 uW from machine vibrations around 50 Hz with external acceleration in the range of 0.2-1 g. The harvester consists of a spring-mass system fabricated using a standard Si-MEMS process that oscillates under external vibrations. Magnets embedded in the mass create time-varying magnetic flux during their translational motion. Voltage is induced in windings placed above and below the plane of motion of the spring-mass system in accordance with Faraday's Law. The harvester is designed to have a matched translational resonance frequency of 50 Hz to maximize power extraction, with higher-frequency alternate resonant modes. The geometry parameters are optimized to achieve a power output of 100 uW, while retaining compactness and mechanical stability. The associated power electronics is designed to deliver 50 uW to the load at a 1.8-V regulated output voltage. A boost converter based on an H-bridge topology is implemented to perform impedance tuning and reactive power conditioning for maximizing power extraction under 5% variation in harvester-resonant frequency due to manufacturing tolerances. The circuit also achieves cold-startup using a Meissner-oscillator topology that can start from low voltages of ~100 mV under 5% off-resonance conditions. The integrated circuit implemented in the TSMC 180-nm process can be co-packaged with the harvester and forms a compact energy harvesting system solution for machine health monitoring.



▲ Figure 1: System architecture for a MEMS-based energy harvester and power-conditioning circuit targeted for machine health monitoring. The electronics includes battery-less startup, frequency tuning, and boost conversion to a 1.8-V output voltage.



▲ Figure 2: (a) A cross-sectional schematic of the MEMS electromagnetic harvester showing the magnet as a proof mass and the MEMS springs that support magnet motion during external vibrations. (b) The circuit architecture showing the H-bridge topology to achieve impedance matching and efficient charge transfer to the load battery.

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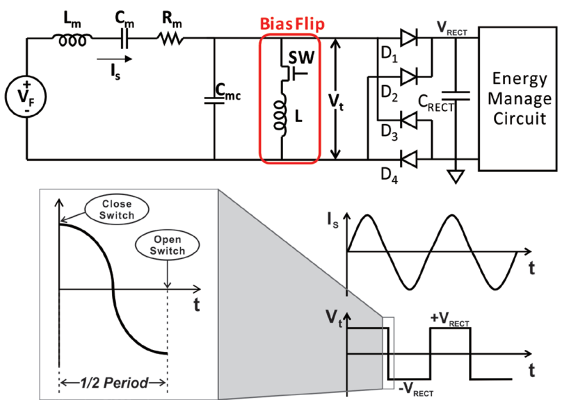
Use of the Bias Flip Technique in Vibration Energy Harvesting

S. Zhao, D. Buss, J. H. Lang

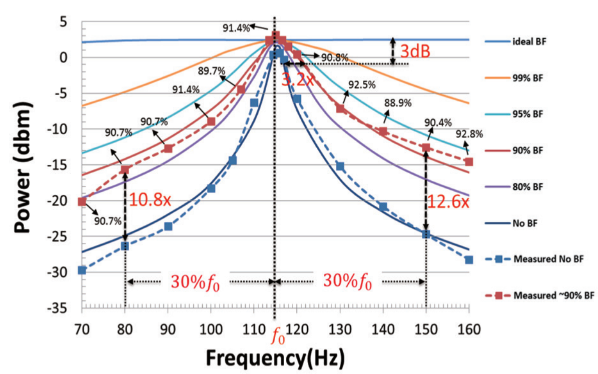
Harvesting ambient vibration energy through piezoelectric (PZ) energy harvesting devices (EHDs) can provide power for low-power wireless sensor nodes. In order to maximize harvested power at a single frequency, a high-Q resonator is required. However, in most practical applications, the source vibration frequency varies with time, and output power drops dramatically as the source vibration frequency deviates from the resonant frequency.

Our research shows that the resonant frequency can be tuned using an electronic circuit called bias flip (BF). Figure 1 shows the diagram of the PZ energy harvesting system with the BF technique. The BF circuit adiabatically flips the voltage across the output capacitor of the EHD in such a way that it cancels the reactive impedance of the mechanical circuit and achieves phase alignment between the output current and voltage. The BF technique was first used to improve the harvested power at resonant frequency. In this research, we explore ways that the BF technique can be used to cancel the internal reactive impedance of the EHD away from the resonant frequency. The goal of this research is to achieve near-optimum output power from a single frequency even when the frequency deviates from the mechanical resonance frequency of the EHD. If the BF were completely adiabatic, we could achieve optimum output power away from resonance. However, parasitic resistances in the switch and the inductor of the BF circuit lead to loss. We have been able to achieve 90% BF efficiency, and this gives some improvements. As shown in Figure 2, we can improve the 3dB bandwidth by ~3x and improve power by ~10x at frequencies 30% above resonance (150 Hz) or below resonance (80 Hz).

The future work is improving harvested power by reducing the influence of circuit parasitics, such as developing alternative BF topologies, redesigning the PZ EHD, and combining BF technique with other approaches.



▲ Figure 1: Diagram of the PZ energy harvesting system based on BF technique and associated operation waveforms at resonant frequency.



▲ Figure 2: Simulation and experiment results with MIDE V20W PZ EHD for harvested power as a function of vibration frequency with different BF efficiencies under 1-g acceleration.

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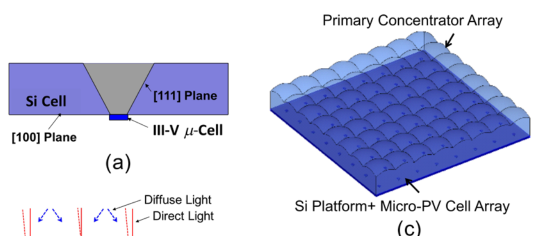
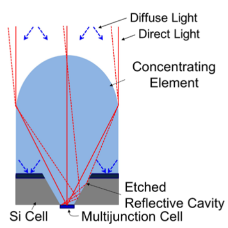
High-Performance Low-Cost Integrated Micro-Scale Photovoltaics

T. Gu, L. Li, D. Li, B. Jared, G. Keeler, B. Miller, W. Sweatt, S. Paap, M. Saavedra, C. Alford, J. Mudrick, U. Das, S. Hegedus,
A. Tauke-Pedretti, J. Hu
Sponsorship: ARPA-E

High-efficiency, low-cost photovoltaics (PV) techniques beyond Si are critical for new price learning curves and further market penetration of solar technology. By dramatically scaling down the dimensions of multijunction cells to the 100s of microns regime and accordingly concentrating micro-optics, emerging micro-scale PV technologies potentially offer several unprecedented benefits, such as enhanced cell performance, reduced module costs, superior interconnect flexibility, improved heat dissipation, and a thin module form factor.

To fully exploit the PV cell/optic size scaling effects, a novel wafer integrated micro-scale photovoltaic (WPV) approach is developed. Employing low-cost fabrication and integration techniques, such a PV+ technology seamlessly combines the high performance of concentrator PV (CPV) and the low costs of flat panel Si PV. The key notion is a multifunctional Si cell platform that is hybrid-integrated with high-performance multijunction micro-cell arrays and simultaneously provides optical micro-concentration, hybrid photovoltaics, and mechanical micro-assembly functionalities (Figure 1). The Si cell embeds micro-fabricated reflective cavity structures at wafer level to serve as efficient non-imaging micro-optics for concentrating direct sunlight onto III-V cells as well as mechanical alignment features. It also collects diffuse sunlight, a considerable portion of the global radiation that cannot be captured by conventional CPV systems. Our baseline prototypical module (Figure 2) demonstrates a >100% improvement of the concentration-ratio x acceptance-angle product, compared to state-of-the-art CPV technologies, leading to dramatically reduced III-V cell and module fabrication costs, sufficient angular tolerance for low-cost trackers, and an ultra-compact form factor as thin as Si panels, which makes the WPV module compatible with commercial flat panel infrastructures. Analyses and industrial-scale cost modeling indicate that the PV+ approach is able to provide 40-50% and 20-40% more annual energy production per unit area across the USA than conventional Si PV and CPV, respectively, while fully leveraging the module- and system-level cost benefits of low-cost Si PV.

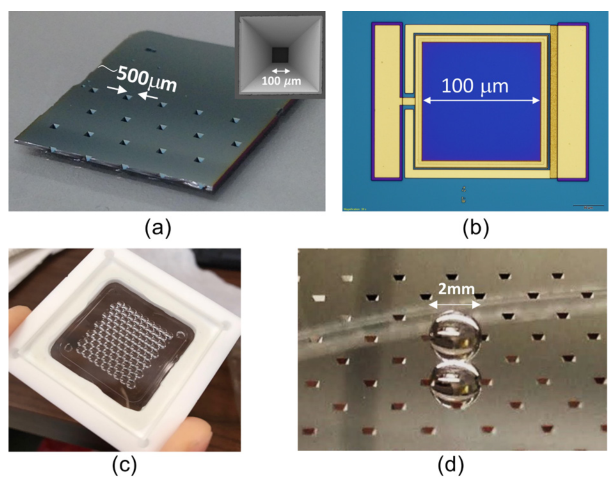




LCOE Component	PV	CPV	WPV
Module Cost	Low	High	Low
Tracker Cost	Low	High	Low
Installation Cost	Low	High	Low
O&M Cost	Low	High	Low
Soft. BOS Cost	High	High	Low
Energy Generation	Low	High	High

(d)

▲ Figure 1: A novel wafer-integrated PV+ concept: (a) multi-functional Si cell platform integrated with multi-junction micro-cells, (b & c) a baseline WPV consists of a molded lens array layer, a multi-functional Si cell, and an integrated array of high concentration multijunction micro-cells, (d) comparison of WPV with traditional Si-PV and CPV.



▲ Figure 2: WPV prototypical module: (a) Si platform with etched cavity arrays, (b) III-V micro-cell; (c) packaged molded PDMS primary lens array, (d) self-aligned ball-lens concentrator positioned on a Si cavity.

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Stored Energy as a Measurable Unit of Radiation Damage in Materials

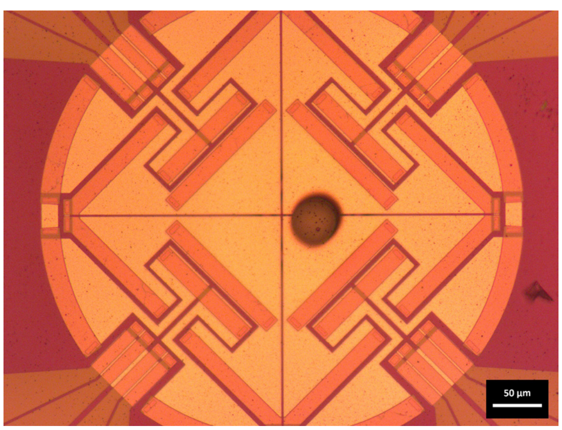
C. A. Hirst, R. C. Connick, L. Abel, K. Carter, S. Lowder, P. Cao, M. P. Short
Sponsorship: MIT-Singapore University of Technology and Design Collaboration Office, International Design Centre

When particle radiation passes through a material, it can knock host atoms off their lattice sites. This leads to the formation of defects that change the material's properties. The unit currently used to describe radiation damage is the average number of displacements per atom (dpa) in the material. However, this value overestimates the defect population as it does not account for recombination and annihilation of defects following their formation.

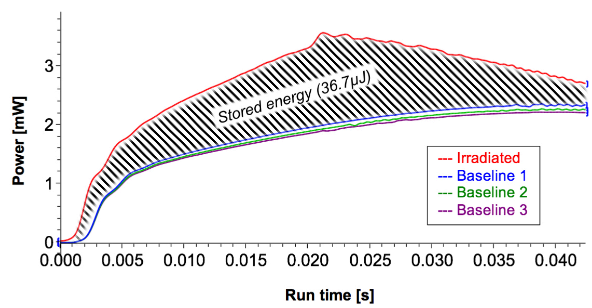
The atoms in these defects have an associated energy that is greater than that of atoms in a perfect crystal. We propose to measure the stored energy of the defects through fast differential scanning calorimetry (DSC) and correlated molecular dynamics simulations. This stored "Wigner" energy is determined by the size, number, and type of defects present in the material, thereby accounting for any recombination that has occurred. Knowledge of the true distribution of defects will allow accurate predictions of a material's properties to be made over practical lengths and timescales.

Samples were prepared using electron beam physical vapor deposition (ebeam PVD) of pure Al onto the SiN-based chip. A shadow mask was utilized to restrict the deposition to a 50-µm-spot size within the analysis region of a Mettler Toledo UFS1 twin calorimeter chip (see Figure 1). The chip and sample were then irradiated with 3.4MeV He^{2+} ions to a fluence of 3.5 x 10^{18} ions/cm2 in the CLASS tandem ion accelerator.

These were then analyzed by heating from room temperature to 450°C at 10,000Ks^{-1} in a Mettler Toledo Flash DSC. The difference between the first (irradiated) and subsequent (baseline) heating curves is the difference between defected and "perfect" material. This represents the stored energy released by the sample during heating, i.e., the annealing out of the irradiation induced defects (see Figure 2). These initial results are proof of the concept with further work including a systematic investigation of irradiation dose versus stored energy and an evaluation of heating rate, irradiation dose rate, and sample preparation effects.



▲ Figure 1: Bright field optical image showing the successful deposition (ebeam PVD) of a 1-µm-thick, ø 50 µm, pure Al sample within the analysis region of a Mettler Toledo UFS1 twin calorimeter chip.



▲ Figure 2: Consecutive heating curves showing the release of energy from the sample during the first (irradiated) heating ramp compared to subsequent (baseline) ramps. Run time is directly proportional to temperature from 30°C to 450°C, with the heating rate 10,000Ks^{-1}.

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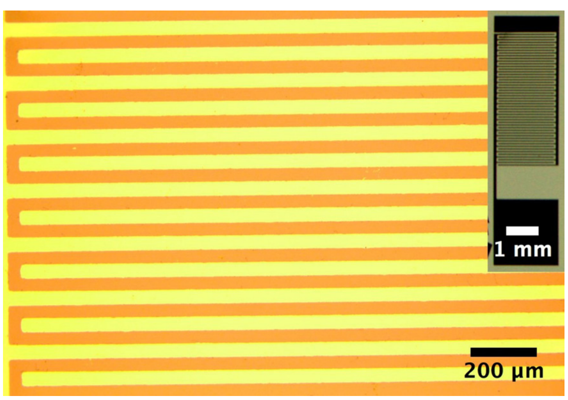
Interdigitated Electrodes for *in situ* Measurements of Electrochemical Devices

J. G. Swallow, T. Defferriere, H. L. Tuller, K. J. Van Vliet
Sponsorship: U.S. Department of Energy Office of Science

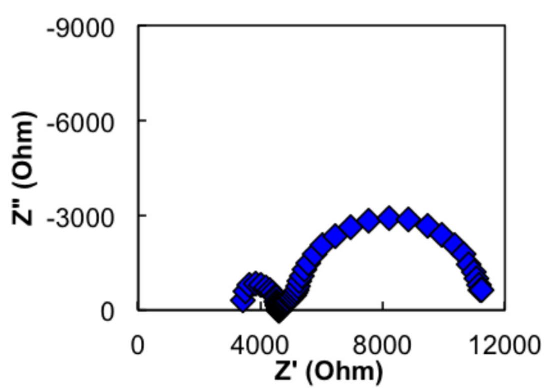
Solid oxide fuel cells (SOFCs) and lithium ion batteries are electrochemical energy conversion and storage devices that rely heavily on materials known as non-stoichiometric oxides. This class of oxides can tolerate very large point defect concentrations that enable useful properties including ionic conductivity or gas exchange reactivity. For SOFCs, ionic conductivity is enabled by transport of oxide ions through a vacancy-mediated mechanism, while oxygen gas exchange operates through incorporation of oxide ions into existing oxygen vacancy sites. Thus, the electrochemical transport and reactivity properties of non-stoichiometric oxides are highly dependent on oxygen vacancy concentration and kinetics, which depend on environmental conditions including temperature, *T*, and oxygen partial pressure, pO2.

In order to understand the electrochemical performance of oxide materials in the range of environments that might be present in operating devices (e.g., T > 600°C, pO2 between 0.2 and 10-15 atm), it is necessary to measure these properties *in situ*. Thin-films are excellent model systems for this purpose, due to their well-controlled compositions and simple geometries that are optimal for rapid testing with electrochemical impedance spectroscopy (EIS). To measure the electronic and ionic conductivity of such films, electrodes that maximize signal to noise are required. Specifically, interdigitated electrodes (IDEs) like those shown in Figure 1 can significantly improve the signal-to-noise ratio over that of simple electrodes and may be fabricated with extreme reproducibility and precision using photolithography.

To fabricate devices like the one shown in Figure 1, photolithography was used to pattern 40-µm IDE photoresist masks onto the surface of an oxide film grown by pulsed laser deposition on a single crystal substrate. Platinum electrodes were then sputtered onto these masks. This was followed by chemical lift-off to remove the remaining photoresist. Such devices may be tested using EIS under a range of conditions, including varied temperatures or gas atmospheres. Spectra like the one shown in Figure 2 can be used to understand how the ionic and electronic transport characteristics of the oxide film are affected by environmental conditions of temperature and oxygen partial pressure.



▲ Figure 1: IDEs fabricated by photolithography on oxide films grown by pulsed laser deposition. The inset shows a low magnification view of device geometry.



▲ Figure 2: EIS of a non-stoichiometric oxide film taken using IDEs like those shown in Figure 1 at 640°C. IDEs provide large effective electrode area that enhances signal-to-noise.

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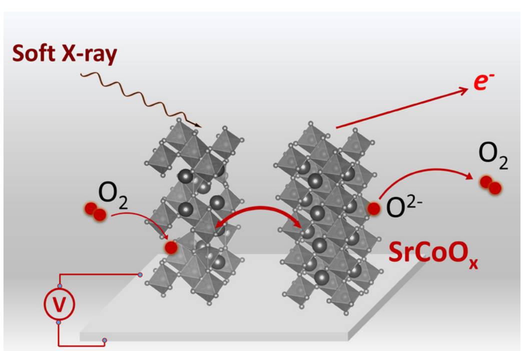
Controlling the Phase and Properties of Functional Oxides by Electrochemical Potential

Q. Lu, S. R. Bishop, G. Vardar, H. L. Tuller, B. Yildiz
Sponsorship: NSF

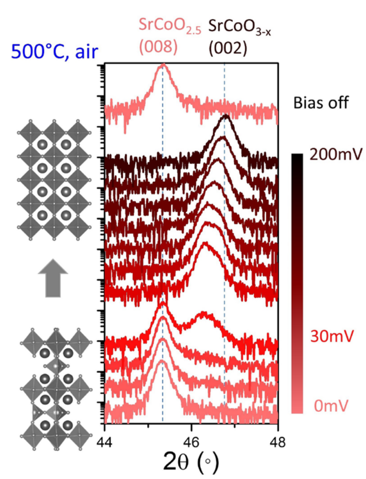
Functional oxides play an important role in the performance of novel electronic devices and energy-storage technologies owing to their highly tunable properties, which can be largely altered via external stimuli. The change of physical properties, including electrical conductivity and magnetism, induced in a controlled and non-volatile fashion can potentially enable emerging information-storage devices. We have developed a new means of tuning the crystal structure and electronic structure by using electrochemical potential to control the oxygen content in the oxide. The aim is to trigger phase transition electrochemically and obtain distinctly different physical and chemical properties. We employed advanced *in situ* material characterization tools to reveal the mechanism of electrochemically induced oxide phase transitions. Our findings can potentially guide the design of new types of electronic devices based on this mechanism.

We implemented this novel method of controlling oxide properties in model system of $SrCoO_x$, which can take two different crystal structures depending on the oxygen stoichiometry, i.e., oxygen-deficient layered brownmillerite-structured $SrCoO_{2.5}$, which is a semiconductor, and oxygen-rich perovskite-structured $SrCoO_3$, which is metallic. By using *in situ* X-ray diffraction, we could probe the electrochemically triggered phase transition between these two crystal structures. We found that an electrochemical bias of merely 25 mV was sufficient to trigger the phase transition, while it is very difficult to obtain this phase transition by conventional chemical methods. We further utilized *in operando* synchrotron-based X-ray spectroscopic tools to depict the evolution of the electronic structure of $SrCoO_x$ during the phase transition. The transition allows for a large change in the electronic structure and electronic conductivity.

This electrochemical method of controlling phase and properties is applicable to a wide range of oxides that have multivalancy and associated distinct phases. We have recently applied this strategy to another functional oxide of importance to electronic devices, i.e., vanadium oxide, VO_x. We revealed a new, electrochemically controlled branch of metal-to-insulator transition between two VO_x phases. The transition can be triggered at a wide range of temperatures, from room temperature to several hundreds of Celsius degrees. This approach opens a new route for designing new "ionotronic" (i.e., "ionic + electronic") devices based on VO_x.



▲Figure 1: Schematic showing the electrochemically controlled phase change and property control (exemplified by $SrCoO_x$). Oxygen ions are incorporated or removed from the oxide structure depending on the polarity of the biases applied. Soft X-ray spectroscopy is used to probe the phase and electronic structure change during this process.



◀Figure 2: *In situ* X-ray diffraction pattern on $SrCoO_x$. Electrochemical bias was applied to alter the phase and crystal structure from $SrCoO_{2.5}$ to $SrCoO_{3-x}$, which leads to the change in the shown peak position.

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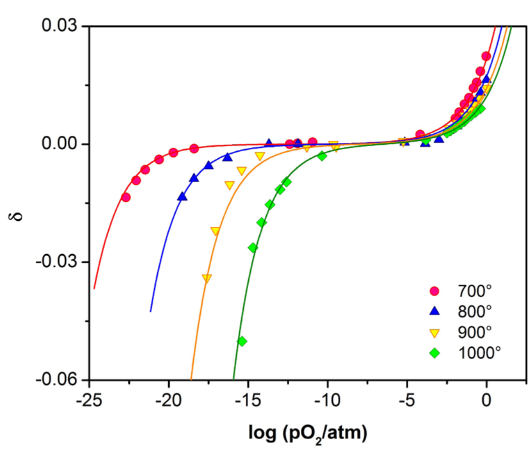
Electro-Chemo-Mechanical Studies of Perovskite-Structured Mixed Ionic-Electronic Conducting $SrSn_{1-x}Fe_xO_{3-x/2+\delta}$

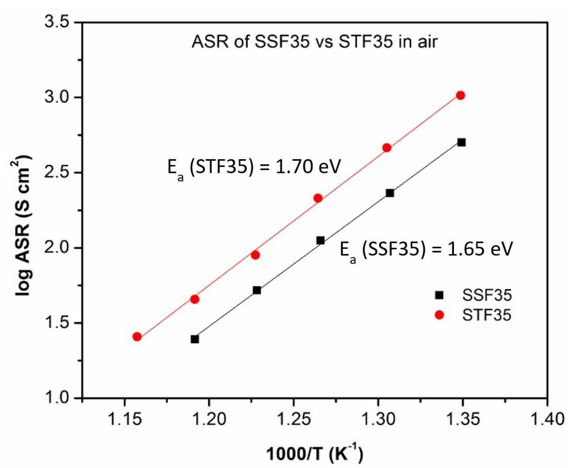
C. S. Kim, S. R. Bishop, N. H. Perry, H. L. Tuller
Sponsorship: Skolkovo Foundation

High efficiency and fuel flexibility make solid oxide fuel cells (SOFCs) attractive for conversion of fuels to electricity. Reduced operating temperatures, desirable for reduced costs and extended operation, however, result in significant losses in efficiency. This loss has been traced primarily to slow cathode surface reaction kinetics. In this work, we extend previous studies on the promising mixed ionic and electronic conducting perovskite-structured $SrTi_{1-x}Fe_xO_{3-x/2+\delta}$ (STF) materials system, whose exchange kinetics were correlated with the minority electron charge density by replacing Ti with Sn, due to its distinct band structure and higher electron mobility.

Oxygen nonstoichiometry and the defect chemistry of the $SrSn_{1-x}Fe_xO_{3-x/2+\delta}$ (SSF) system were examined by thermogravimetry as a function of oxygen partial pressure in the temperature range of 973-1273 K. Marginally higher reducibility was observed compared to corresponding compositions in the STF system. The bulk electrical conductivity was measured in parallel to examine how changes in defect chemistry and electronic band structure, associated with the substitution of Ti by Sn, impact carrier density and ultimately electrode performance. Bulk chemical expansion was measured by dilatometry as a function of oxygen partial pressure, while surface kinetics were examined by means of AC impedance spectroscopy. The electro-chemo-mechanical properties of SSF were found not to differ significantly from the corresponding composition in STF. Key thermodynamic and kinetic parameters for $SrSn_{0.65}Fe_{0.35}O_{2.825+\delta}$ (SSF35) were derived, including the reduction enthalpy, electronic band gap, anion Frenkel enthalpy, oxygen vacancy migration energy, and electron and hole mobilities. Though slightly shifted by the larger size of Sn, the defect equilibria and the cathode area specific resistance differed only in a limited way from that in STF. This small difference was attributed to properties being largely dominated by Fe and not by the substitution of Ti with Sn.



▲ Figure 1: Oxygen nonstoichiometry δ as a function of pO_2 and temperature for SSF35.



▲ Figure 2: Comparison of temperature dependence of area specific resistance of SSF35 and STF35 thin-film electrodes.

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Controlling Concentration and Nature of Oxygen Defects in Layered Cuprate-Based Materials by Electrical Bias

C. S. Kim, H. L. Tuller
Sponsorship: Skolkovo Foundation

Both the nature and concentration of oxygen defects in oxide materials can have a significant impact on their physical and chemical properties as well as key interfacial reaction kinetics such as oxygen exchange with the atmosphere, important of sensor, fuel cell and electrolysis cell operation. Most commonly, the desired oxygen defect concentration, or equivalently oxygen nonstoichiometry, is attained in a given material by controlling the oxygen partial pressure and temperature in which it is equilibrated or annealed. This approach, however, is limited by the range of oxygen partial pressures readily experimentally achievable and requires knowledge of the applicable defect chemical model. In this study, we fine-tune oxygen defect concentrations in promising rare earth cuprate (RE_2CuO_4: RE = rare earth) solid oxide fuel cell cathode materials by application of electrical potentials across an yttria-stabilized zirconium supporting electrolyte. These layered perovskites can incorporate both oxygen interstitials and vacancies, thereby broadening the range of investigations. Oxygen nonstoichiometry values are determined by in-situ measurement of chemical capacitance and are compared with corresponding information available for bulk specimens. These studies are expected to provide further insight into the defect and transport mechanisms that support enhanced SOFC cathode performance.

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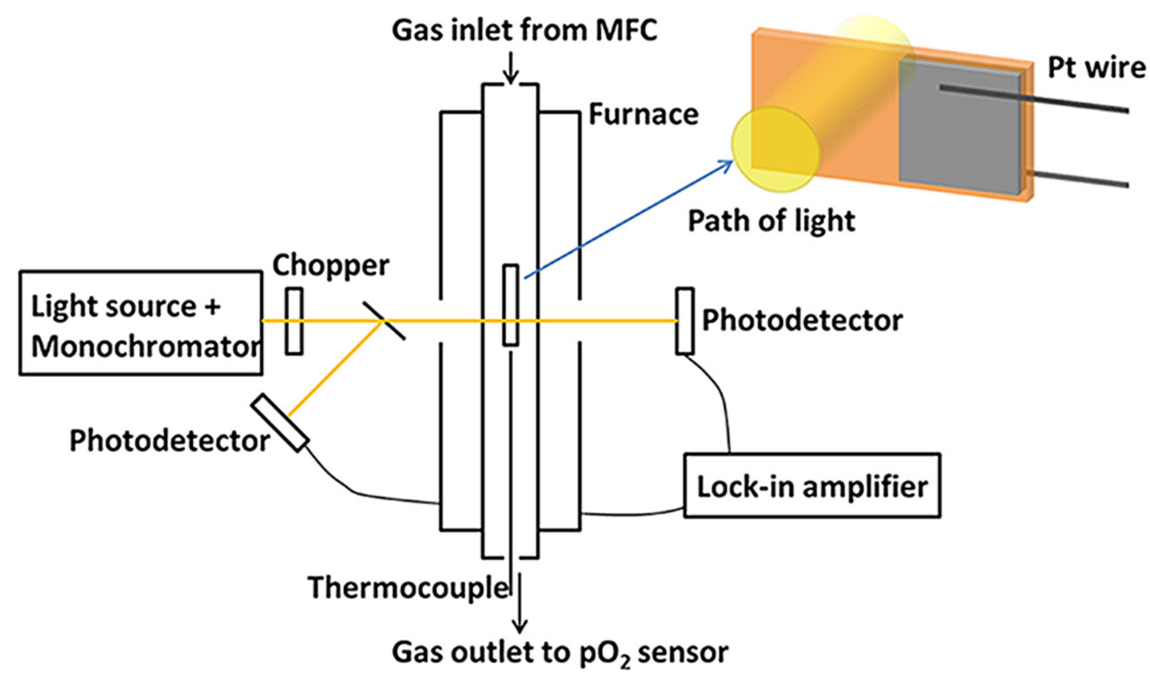
Utilization of $BaSnO_3$ and Related Materials Systems for Transparent Conducting Electrodes

M. Campion, S. R. Bishop, H. L. Tuller
Sponsorship: NSF

Efficient transparent electrode materials are vital for applications in smart window, LED display, and solar cell technologies. These materials must possess a wide band gap for minimal optical absorption in the visible spectrum while maintaining a high electrical conductivity. Tin-doped indium oxide (ITO) has been the industry standard for transparent electrodes, but the use of the rare element indium has led to a search for better material alternatives. $BaSnO_3$ represents a promising alternative due to its high electron mobility and resistance to property degradation under oxidizing conditions, but the mechanisms by which processing conditions and defect chemistry affect the final material properties are not well understood.

This work seeks to better understand the relationships between processing, defect chemistry, and material properties of $BaSnO_3$, in order to better establish the consistent and controllable use of $BaSnO_3$ as a transparent electrode. To accomplish these goals, methods such as in-situ resistance and impedance monitoring during annealing will be applied. In addition, a variety of novel methods such as the *in situ* monitoring of optical transmission (shown in Figure 1) during annealing and the in-situ monitoring of resistance during physical vapor deposition will be utilized to investigate $BaSnO_3$. Direct measurements of the key constants for the thermodynamics and kinetics of oxidation in donor-doped $BaSnO_3$ will be experimentally determined for the first time. This increase in understanding will provide a predictive model for determining optical properties, carrier concentrations, and electron mobilities in $BaSnO_3$, which may be become increasingly important due to its high electron mobility, high temperature stability, and favorable crystal structure.



▲ Figure 1: Schematic of experimental setup to be used for simultaneous in-situ measurement of the optical transmission and electrical conductivity of thin-film BaSnO3 samples during annealing under controlled atmosphere and temperature.

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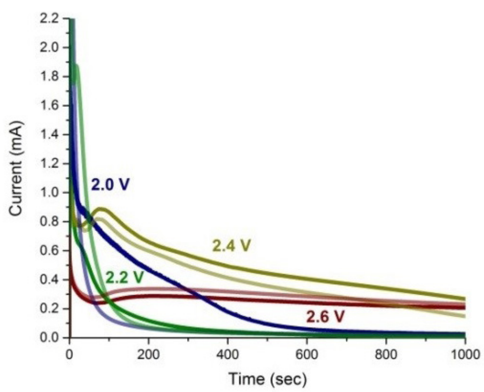
Understanding Mechanisms and Optimizing Capacity for Lithium-O_2 Batteries

T. Batcho, D. Kwabi, Y. Shao-Horn, C. V. Thompson
Sponsorship: Skoltech Center for Electrochemical Energy Storage

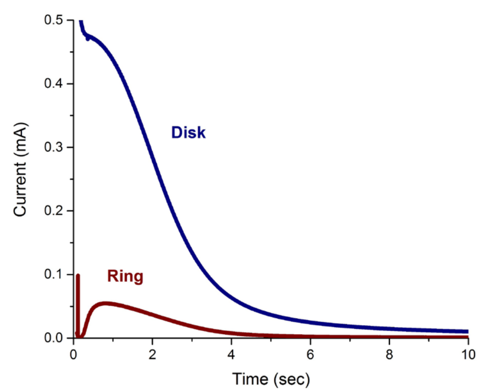
Lithium-O_2 batteries hold promise for the next generation of electric vehicles and other applications. By reacting oxygen directly with lithium ions to form Li_2O_2 on discharge, they can achieve energy densities 3-5 times higher than current lithium-ion batteries. Because Li_2O_2 forms an electrically insulating film during discharge that passivates the electrode surface, obtaining optimal volumetric capacities requires an understanding of the mechanisms that control Li_2O_2 film formation.

High volumetric capacities can be achieved by promoting the growth of large toroidal deposits of Li_2O_2 as opposed to thin-films, which cut off cell discharge prior to full void space filling of the electrode. Li_2O_2 can form by a surface pathway involving two-electron transfers into a film or by a solution pathway involving a one-electron transfer to create solvated LiO_2 that chemically forms toroidal Li_2O_2. We study the mechanisms of nucleation and growth by the surface pathway to promote more efficient void filling. Potentiostatic discharges provide useful information about the kinetics of the film formation as the driving force for Li_2O_2 is fixed, which allows the application of existing models for electrodeposition to our system to extract rates of surface nucleation and growth. Our initial efforts have focused on performing potentiostatic discharges on carbon paper in a standard cell. This method shows that potential determines the rate of film growth (Figure 1), but it provides no means to separately characterize the mechanisms of the surface and solvent processes.

To distinguish current that forms Li_2O_2 in solution from current that forms Li_2O_2 on the electrode, we use the rotating ring disk electrode technique (RRDE). RRDE reduces oxygen at an inner disk electrode to form insoluble Li_2O_2 on that electrode or soluble LiO_2 that is swept to an outer ring electrode by a convection current created by rotating the setup (Figure 2). Since we directly measure the amount of soluble species at the ring, we can calculate the amount of Li_2O_2 formed by the surface pathway. This allows us to model the nucleation and growth kinetics of the surface film formation. We use RDDE to study how solvent properties and potential govern surface film growth kinetics, which will be key in achieving high void-filling high volumetric capacity Li-O_2 batteries.



▲ Figure 1: Current transients for potentiostatic discharges at a range of potentials in 0.1 M $LiClO_4$ DMSO on carbon paper. Peaks occur at longer times at higher potentials (lower overpotentials), suggesting slower nucleation/growth rates.



▲ Figure 2: Disk current transient (blue) and corresponding ring current transient (red) for a 2.4V discharge in 0.1 M $LiClO_4$ DMSO. The ring current gives a measure of the amount of soluble species produced on the disk.

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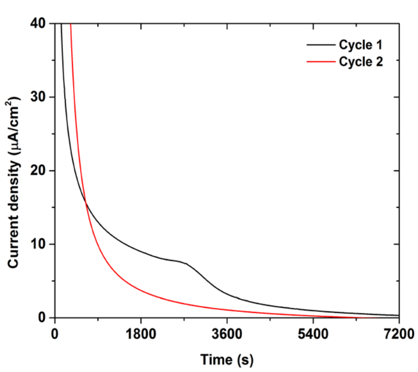
Kinetic Studies of the Initial Lithiation Si Thin-Film Anodes

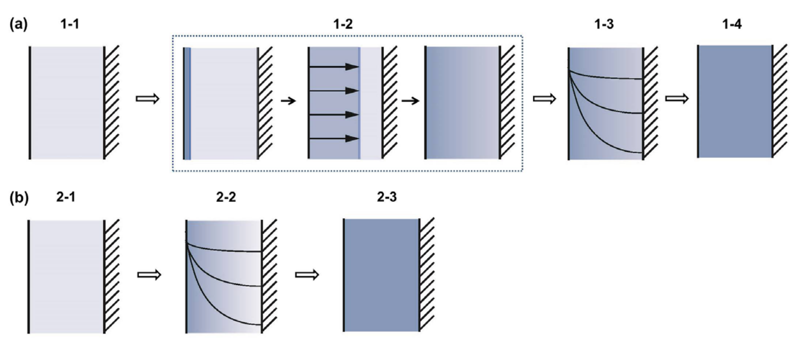
J. Miao, C. V. Thompson
Sponsorship: SMART, Skoltech Center for Electrochemical Energy Storage

Li-ion batteries are the most widely used secondary batteries. Researchers have been aiming for larger capacity and energy density, better cycling performance, and safer operation. Also, in response to the trend toward miniaturized device development in the electronic and health industries, all-solid-state planar microbatteries have received special attention because they can be integrated with complementary metal-oxide semiconductor (CMOS) technology and offer improved safety since no liquid electrolyte is used. Among known anode materials, Si is a promising candidate for applications in microbatteries. It has extraordinarily high volumetric and gravimetric capacities (8375 Ah/cm^3, 3579 Ah/kg), along with a low discharge potential and thus a high energy density. The reason that Si exhibits such high capacities is related to its alloying mechanism during lithiation and delithiation. Quite different from conventional intercalation anodes, the lithiation of amorphous Si proceeds by bond breakage and formation of new atomic scale structures in a series of phase transformations. Unfortunately, this mechanism also leads to a large volume expansion and can lead to battery failure. To explore the alloying lithiation process of Si thin-films and better understand the reaction mechanisms and the potential for material optimization, electrochemical methods and material analysis were used to study the irreversible phase transition that occurs in the first lithiation cycle and the change in transformation mechanisms between cycles.

It was found that the current vs. time plot for the first lithiation in the first charge-discharge cycle (Figure 1, black curve) during potentiostatic lithiation shows a step feature that cannot be explained using the single phase diffusion model that is often envisioned for the lithiation process. The time at which the step occurs increases with increasing film thickness, suggesting a transformation mechanism involving the motion of a planar interface, as shown in Figure 2(a). The behavior leading to the step can be divided into two regimes, with the curve before the step showing a square root of time dependence and the curve after the step fitting an exponential decay. This division is consistent with diffusion limited thickening of the lithiated phase (Figure 2a), followed by elimination of the Li concentration gradient in the fully transformed film. In the second lithiation cycle, the step feature is absent (Figure 1, red curve). This absence suggests that after the transformation in cycle 1, the single phase diffusion model applies (Figure 2b). Therefore, it is concluded that the two-phase coexistence and interface propagation process that occurs in cycle 1 leads to an at least partly irreversible expansion of the Si structure during cycle 1. Modification of this process might allow optimization of battery performance in subsequent cycles.



▲ Figure 1: Current density vs. time plots for a 315- nm-thick amorphous Si (a-Si) thin-film in cycle 1 and cycle 2 in potentiostatic tests.



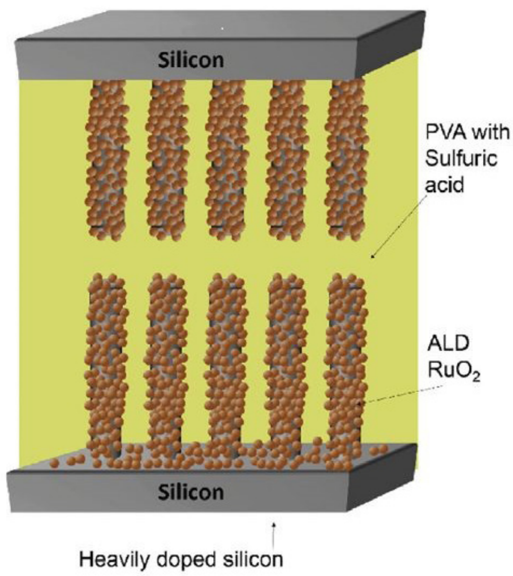
▲ Figure 2: (a) Cycle 1 and (b) Cycle 2 lithiation models under a constant potential for a 315-nm- thick a-Si thin-film.

Integrated All-Solid-State Supercapacitors for Si Microsystems

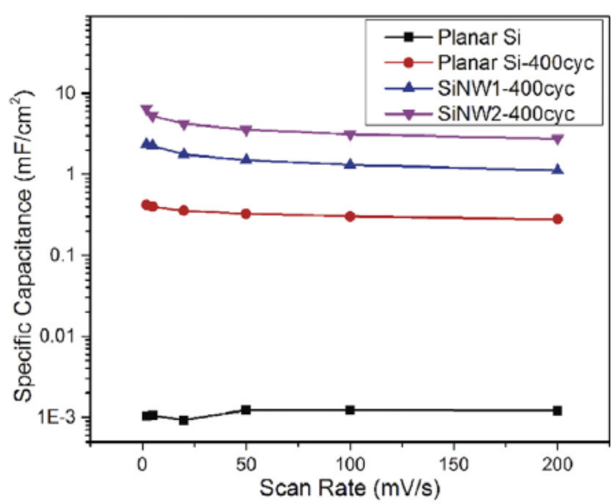
W. Zheng, Q. Cheng, D. Wang, C. V. Thompson
Sponsorship: SMART

Autonomous microsystems require devices for energy storage. Thin-film microbatteries store energy at high density but typically operate at low power, while capacitors can operate at high power but do not provide high density storage. Autonomous microsystems, such as autonomous sensors, require both high energy density storage for efficient use of space and high power for broadcast of data. We are developing all-solid-state thin-film microbatteries, discussed elsewhere, and nanowire-array supercapacitors that can be fabricated using the tool set for complementary metal-oxide semiconductor (CMOS) processing.

Solid-state on-chip supercapacitors based on ruthenium oxide coated silicon nanowires were fabricated. Ordered arrays of silicon nanowires were made using metal-assisted anodic etching (MAAE), as in Figure 1. Atomic layer deposition (ALD) was used to form a uniform coating of ruthenium oxide on high-aspect-ratio silicon nanowires at a moderate temperature of 290°C. Coated nanowire electrodes were studied using cyclic voltammetry and charge-discharge tests in a neutral Na_2SO_4 electrolyte, and a specific capacitance of 19 $mFcm^{-2}$ was achieved at 5 mVs^{-1}. Solid-state nanowire capacitors were then fabricated with symmetric face-to-face nanowire arrays separated by a polymer-based solid electrolyte. This device exhibited a specific capacitance as high as 6.5 $mFcm^{-2}$ at 2 mVs^{-1}, as Figure 2 shows. The full device was tested over 10,000 cycles under galvanostatic charge/discharge at 0.4 $mAcm^{-2}$ and showed a retention of 92% of the specific capacitance. The specific capacitance was found to scale with the total nanowire surface area, by controlling the aspect ratios of the wires. The solid-state nanowire-based device also achieved high specific energies without sacrificing power performance.



▲ Figure 1: Schematic of the symmetric solid-state on-chip supercapacitor based on RuO_x- coated arrays of silicon nanowires (SWNs).



▲ Figure 2: Specific capacity versus scan rate for all-solid-state planar capacitors with and without RuO_x coatings and silicon nanowire capacitors with two different NW aspect ratios.

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MEMS, Field-Emitter, Thermal, and Fluidic Devices

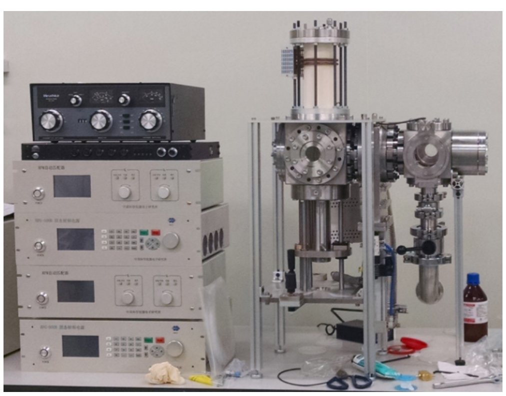
Development of a Tabletop Fabrication Platform for MEMS Research, Development, and Production

M. D. Hsing, P. A. Gould, M. A. Schmidt
Sponsorship: MTL

A general rule of thumb for new semiconductor fabrication facilities (Fabs) is that revenues from the first year of production must match the capital cost of building the fab itself. With modern fabs routinely exceeding $1 billion to build, this rule serves as a significant barrier to entry for research and development and for groups seeking to commercialize new semiconductor devices aimed at smaller market segments and requiring a dedicated process. To eliminate this cost barrier, we are working to create a suite of tools that will process small (~1") substrates and cumulatively cost less than $1 million. This suite of tools, known colloquially as the 1" Fab, offers many advantages over traditional fabs. By shrinking the size of the substrate, we trade high die throughputs for significant capital cost savings, as well as substantial savings in material usage and energy consumption. This substantial reduction in the capital cost will drastically increase the availability of semiconductor fabrication technology and enable experimentation, prototyping, and small-scale production to occur locally and economically.

To implement this suite of 1" Fab tools, our current research has primarily been focused on developing a 1" Fab deep reactive ion etcher (DRIE). DRIE tools are used to create highly anisotropic, high aspect-ratio trenches in silicon—a crucial element in many MEMS processes that will benefit from a 1" Fab platform. In 2015-2016 we completed the development of the tool, and in this past year, our focus has been on optimizing its design for manufacturability. We ultimately demonstrated the manufacturability of the tool by setting up a satellite laboratory in Beijing, China with our research collaborators at the General Research Institute for Nonferrous Metals (GRINM). (See Figure 1 for a photo of the system set up in China). Our GRINM colleagues are helping develop etch recipes and providing feedback on the operation of the tool. We have also been working with the Perreault group at MIT to develop a low-cost, resistance-compression-based impedance matching network for use with this DRIE system and other plasma-based processing tools

In addition to the optimization of the DRIE tool, we are currently developing novel PECVD and magnetron sputtering tools. In the PECVD research, we are exploring the use of inductively coupled plasma sources and non-pyrophoric mixtures of silane gas for Si-based film depositions. For sputtering, we are looking at novel techniques for creating low cost multi-layer film stacks. These two new systems will leverage the pre-existing 1" Fab modular infrastructure and will be fully compatible with the common base assembly that was developed for the 1" Fab DRIE system, as shown in Figure 2.



▲ Figure 1: View of the basic components of the 1" Fab DRIE system.

▲ Figure 2: 1" Fab tools utilizing a common base assembly.

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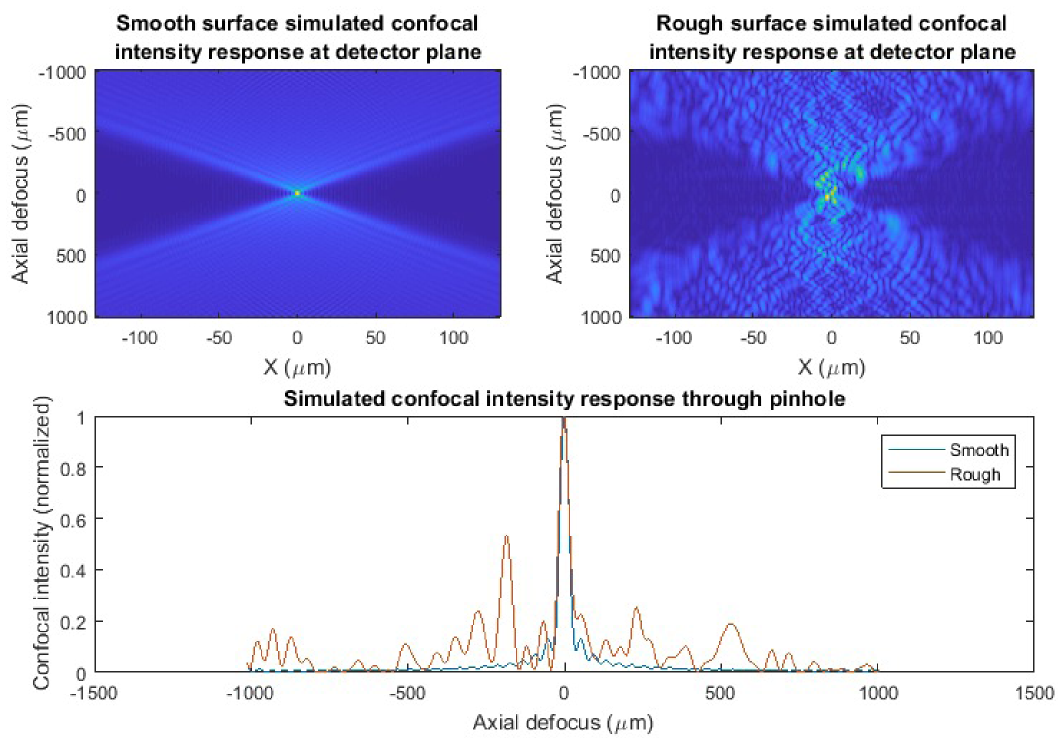
Development of in-situ Depth Profiler for Real-Time Control in a Deep Reactive Ion Etcher

C. Teale, M. A. Schmidt, G. Barbastathis

Standard process development for micro and nanofabrication etching cycles rely on open-loop trial and error testing of recipes to achieve optimal etch depths and uniformities. This strategy is non-optimal for research and fabrication of novel devices where one-of-a-kind experiments can not justify lengthy process development times. As an alternative, we are developing an in-situ depth measurement device for real-time feedback of etch depth and uniformity. This will facilitate far shorter process development times, ideally enabling the desired etch to be achieved on the first process run.

Many system constraints make this very difficult and preclude the use of existing technology. We are pursuing an optical measurement approach based on a parallelized confocal design. The measurement must be done at a distance of around 8" through an aperture of around 2" in diameter, significantly limiting the numerical aperture. We are currently investigating the fundamental resolution limits of a confocal depth measurement under these conditions. We expect the dominant noise source to be laser speckle which will result from coherent illumination of the rough surface left by the plasma etching process. Calculations and simulations indicate that the confocal depth measurement is significantly corrupted by this speckle noise, severely limiting the depth resolution to around 100 μm. The desired depth resolution is around 1 μm which should be achievable if the specke noise could be removed. By measuring and characterizing the statistical properties of the rough surface's height distribution, we hope to remove the speckle noise and significantly improve the achievable depth resolution.



▲ Figure 1: (top, left) Smooth surface simulated confocal intensity response at detector plane, (top, right) rough surface simulated confocal instensity response at detector plane, and (bottom) simulated confocal intensity response through pinhole.

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Resonant Body Transistor with MIT Virtual Source (RBT-MVS) Compact Model

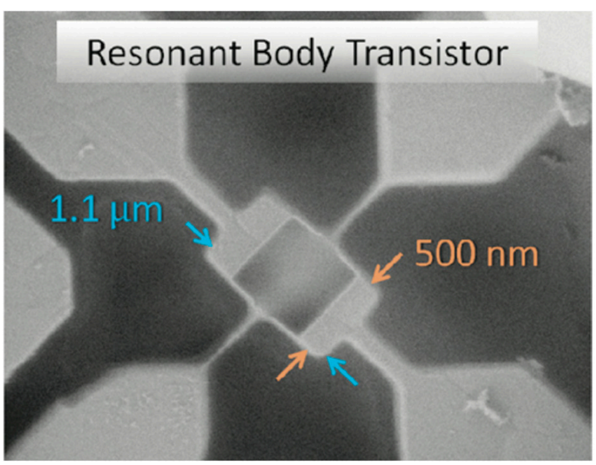
B. Bahr, D. Weinstein, L. Daniel
Sponsorship: NSF NEEDS

High-Q mechanical resonators are crucial components for filters and oscillators that are essential for radio frequency and analog circuits. It is highly desirable for resonators to scale to GHz-frequencies and beyond to meet today's challenging requirements in terms of speed and data rates. Furthermore, aggressive scaling requirements call for monolithic integration with complementary metal-oxide semiconductor (CMOS) circuits to allow for a smaller footprint and reduced parasitics and power consumption. Micro-electro-mechanical (MEM) resonators represent a potential solution for frequency and footprint scaling, along with monolithic integration in CMOS.

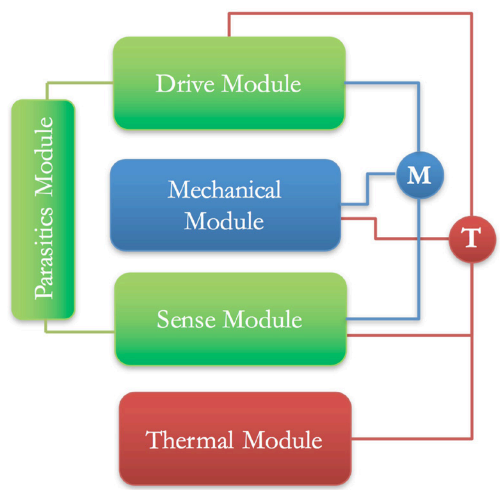
A resonant body transistor (RBT) is a MEM resonator with a field-effect transistor (FET) incorporated into the resonator structure. The FET is intended for active sensing of the mechanical vibrations through piezoresistive modulation of the channel mobility. RBTs also rely on electrostatic internal dielectric transduction for actuation, by means of metal–oxide–semiconductor capacitors (MOSCAPs). Such sensing and actuation enable these devices to easily scale to multi-GHz frequencies while being compatible with CMOS manufacturing technologies.

Compact modeling for these devices is essential to gain a deeper insight into the tightly coupled physics of the RBT while emphasizing the effect of the different parameters on the device performance. It also grants circuit designers and system architects the ability to quickly assess the performance of prospective RBTs while minimizing the need for computationally intensive coupled-multiphysics finite element method (FEM) simulations.

The RBT compact model is developed as a set of modules, each representing a physical phenomenon. Mechanical resonance, FET sensing, MOSCAP driving, and thermal modules are the most notable. The modules are interconnected through a set of nodes (namely, mechanical nodes and a thermal node) to represent the coupling between the different physics. This modular approach enables the seamless expansion of the RBT model either by incorporating new physics, adding driving or thermal sources, or mechanically coupling multiple RBTs together. A modified version of the MIT Virtual Source (MVS) model is used to implement both the electrostatic driving (as a MOSCAP) and the piezoresistive active FET sensing. The full model is developed in Verilog-A and available on nanohub.org.



▲ Figure 1: The first RBT, developed by D. Weinstein and S. Bhave in 2009 at Cornell University.



▲ Figure 2: Modular RBT model, with each physical phenomenon represented by a module. Different modules are connected through a mechanical node (M) and thermal node (T).

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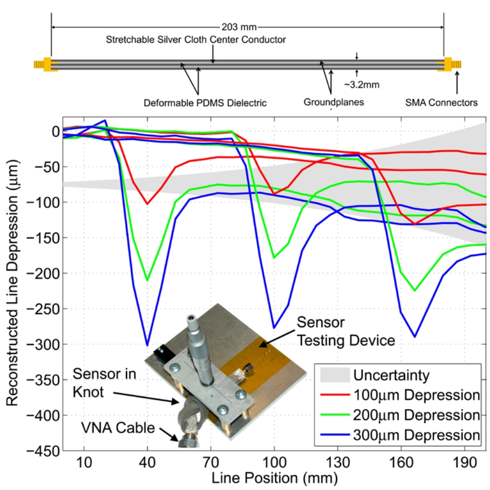
Shielded, Flexible, and Stretchable Tactile Pressure and Shear Sensors Based on Deformable Microwave Transmission Lines

M. E. D'Asaro, D. B. Sheen, J. H. Lang
Sponsorship: NSF CSNE

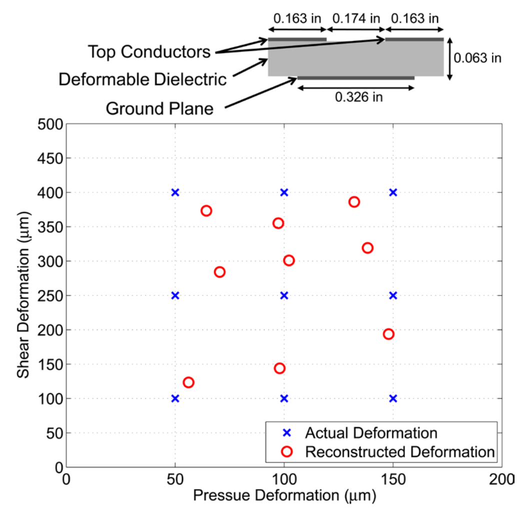
Tactile sensors and skins aimed at replicating the human sense of touch are an active topic of research with numerous potential applications in areas including robotics, healthcare, and prosthetics. Current skin technology is limited by mechanical fragility, complex fabrication, and the need for large numbers of connections to external electronics. We have developed a new sensing technology based on microwave transmission lines that address these challenges.

The pressure sensor (Figure 1) consists of a shielded flexible and stretchable 3-mm-thick transmission line constructed with conductors made of stretchable conductive cloth and a dielectric made of silicone rubber. Where pressure is applied, the dielectric deforms causing a change in the local characteristic impedance of the line. We have developed an algorithm that can reconstruct the deformation of the line as a function of position, based on the terminal impedance of the line measured across a wide frequency range (30 MHz to 6 GHz). This algorithm can also correct for resistive loss in the transmission line. To demonstrate this sensor, three different pressure deformations were applied at each of three locations, and the responses were combined to create Figure 1. Due to the shielding, the sensor performs correctly even when tied in a knot (with updated baseline subtraction).

We have also developed a shear sensor (Figure 2) capable of measuring deformation due to applied pressure, and separately, deformation due to the force applied parallel to the surface of the sensor. This device consists of two independent transmission lines, which are constructed so that pressure causes equal impedance change but shear causes unequal change, allowing pressure to be differentiated from shear. Shear sensors are rare in the field of tactile skins; this technique, requiring only two connections, has promise for inexpensive and simple wide-area flexible and stretchable pressure and shear sensors.



▲ Figure 1, top: Diagram of shielded pressure sensor. Main: Loss-corrected response of sensor to pressure of various magnitudes and at various locations. Inset: Sensor on testing apparatus shown tied in a knot with no significant effect on response.



▲ Figure 2, top: Cross-section of shear sensor showing conductors and dielectric. Main: Sensor response to various magnitudes of simultaneous pressure and shear. (Actual applied pressure and shear plotted for comparison.)

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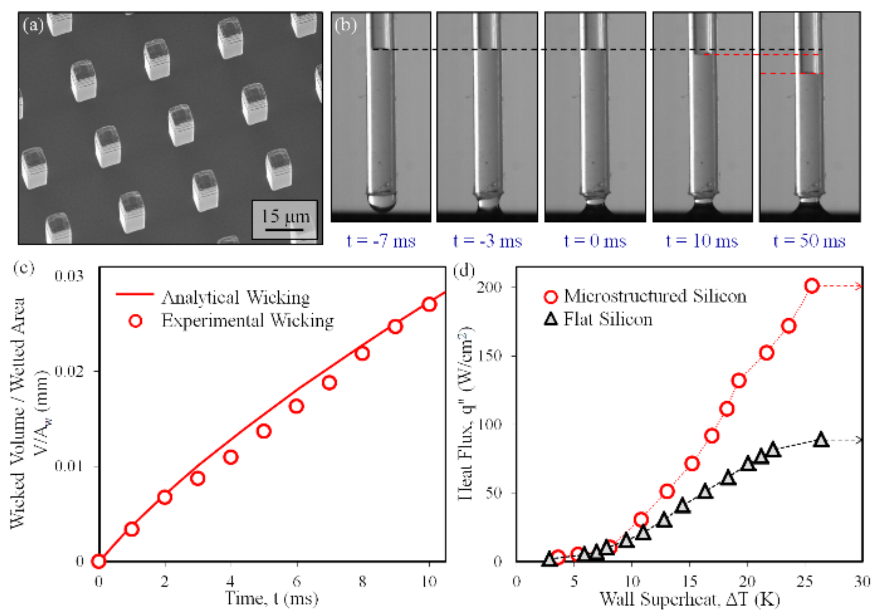
Micro-Engineered Pillar Structures for Pool-Boiling CHF Enhancement

M. Rahman, G. Saccone, M. Bucci, J. Buongiorno
Sponsorship: Exelon Corporation, MISTI

Increasing the performance of phase-change heat transfer phenomena is key to the development of next-generation electronics as well as power generation systems and chemical processing components. Surface-engineering techniques could be successfully deployed to achieve this goal. For instance, by engineering micro/nano-scale features, such as pillars, on the boiling surface, it is possible to attain 100% enhancement in pool boiling critical heat flux (CHF). Researchers have been working on several CHF enhancing micro- and nano-structured surfaces for years. However, due to the complexity of CHF phenomena, there is still no general agreement on the enhancement mechanism. An investigation of the effect of micropillar height on surface capillary wicking and the associated pool-boiling CHF enhancement has been conducted. Several silicon micropillar structures have been fabricated using MTL photolithography and DRIE facilities.

The surfaces were characterized using MTL's scanning electron microscope (SEM), as shown in Figure 1a. The surfaces were then characterized by measuring the capillary wicking rate as presented in Figure 1b. A mechanistic capillary wicking estimation has been provided and compared with experimental wicking results (Figure 1c). Finally, the performance of such structures was characterized through traditional pool boiling experiments (Figure 1d). The results demonstrate the benefits of wicking promoted by these structures in terms of CHF enhancement.

The microstructured surfaces fabricated at MTL have also been tested in pool-boiling with an electric field applied to replace for low gravity in space applications. A further increase in CHF has been observed due to the application of the electric field, on both flat and micro-structured silicon heaters. Notably, the combined use of passive (micro-structured surfaces) and active (electric field) CHF enhancement techniques has produced the maximum CHF enhancement.

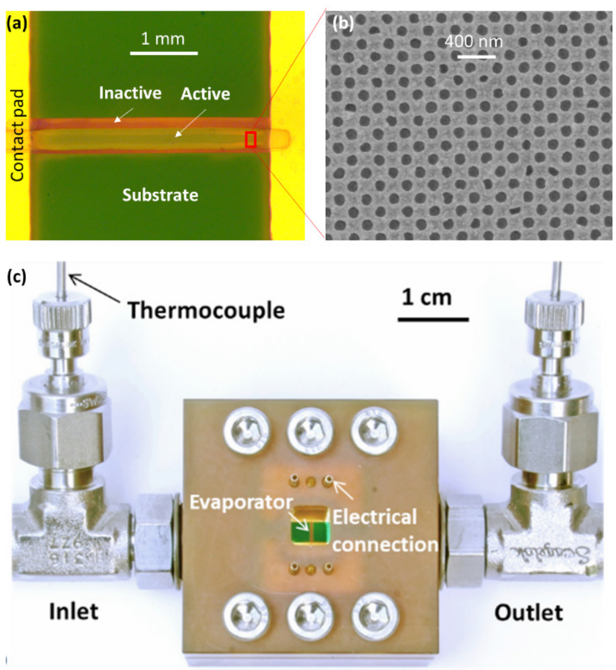


▲ Figure 1: Microstructured surfaces for CHF enhancement, (a) SEM image of a fabricated surface, (b) high speed images wicking experiment, (c) comparison of analytical and experimental wicking, (d) pool boiling result of a microstructured surface compared to flat silicon reference surface.

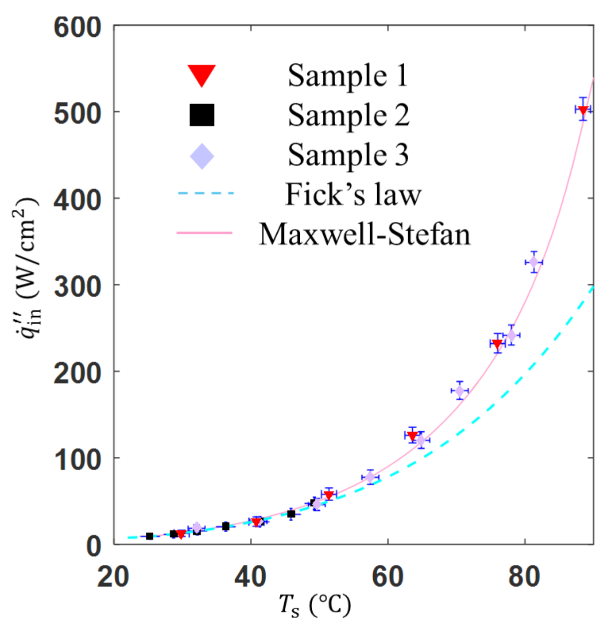
An Ultra-Thin Nanoporous Membrane Evaporator

Z. Lu, K. L. Wilke, D. J. Preston, I. Kinefuchi, E. Chang-Davidson, E. N. Wang
Sponsorship: AFOSR

Evaporation is a ubiquitous phenomenon found in nature and widely used in industry. Fundamental understanding of the interfacial transport during evaporation remains limited to date as it is generally challenging to characterize the heat/mass transfer at the interface level, especially when the heat flux is high (> 100 W/cm2). In this work, we were able to accurately monitor the temperature of the liquid-vapor interface, reduce the thermal-fluidic transport resistance, and mitigate the clogging risk due to contamination. This was done with an ultra-thin (≈ 200-nm thickness) nanoporous (≈ 130-nm pore diameter) membrane evaporator, Figure 1 a, b, and c. At a steady state, we demonstrated high heat fluxes across the interface (≈ 500 W/cm2) with pure evaporation into an air ambient over a total evaporation area of 0.20 mm2. In the high flux regime, we showed the breakdown of Fick's first law of diffusion and the importance of convective transport caused by evaporation itself (Figure 2). The present work improves the fundamental understanding of evaporation and paves the way for applications of high flux phase change devices.



▲Figure 1: (a) Image of the ultra-thin nanoporous evaporator from an optical microscope: two Au contact pads are connected by a suspended membrane (~ 200-nm thick); the active part is nanoporous and coated with Au (≈ 40-nm thick) while the inactive part is impermeable and non-metallic, (b) image of the nanopores patterned in the active part of the membrane from a scanning electron microscope, (c) image of the test rig with a liquid feed-through and electrical connections.



▲Figure 2: Heat flux $\dot{q}''_{in}$ vs. surface temperature T_s over a large range of evaporative heat fluxes: the red triangles, black squares, and purple diamonds are the experimental data from Samples 1, 2, and 3, respectively. The blue dash line and the pink solid line represent the model prediction from Fick's law and the Maxwell-Stefan equation, respectively.

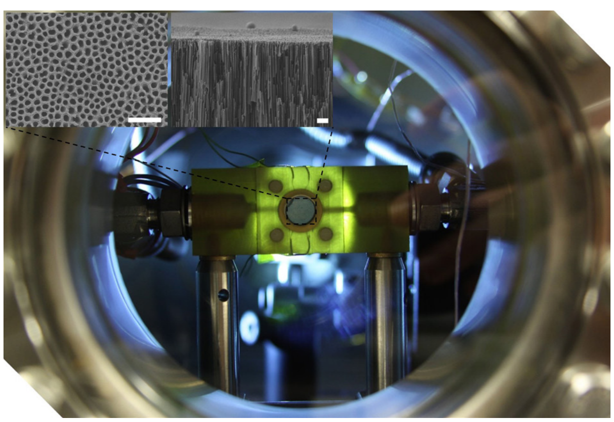
Thin-Film Evaporation from Nanoporous Membranes for Thermal Management

K. L. Wilke, B. Barabadi, Z. Lu, T. J. Zhang, E. N. Wang
Sponsorship: The Masdar Institute of Science and Technology, MIT

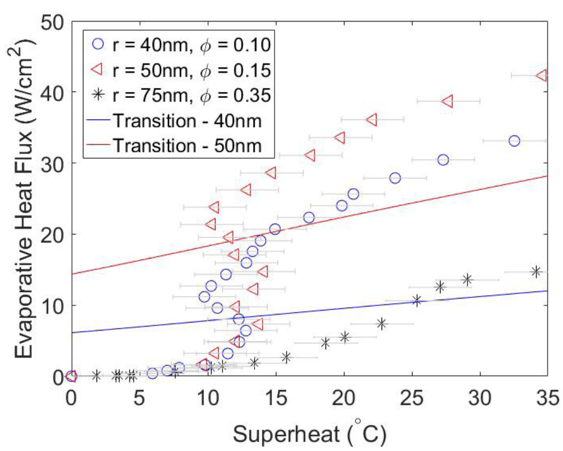
Performance and lifetime of emerging electronics are often dictated by the ability to dissipate heat generated in the device. In fact, a number of advanced electronics can generate heat fluxes exceeding 1000 W/cm2, such as gallium nitride high electron mobility transistors, and pump lasers. To put that in context, the heat flux of a typical electric stovetop is more than 100x less. The large heat fluxes generated in these devices, coupled with the negative impact on the device's performance, has created the need for new thermal management techniques. Thin-film evaporation from nanopores has emerged as a promising candidate by reducing the thermal transport resistance across the liquid film while simultaneously providing capillary pumping. The combination of low resistance and large capillary pumping allows large heat fluxes to be dissipated with minimal temperature rise in the device.

In this work, we study the dependence of evaporation from nanopores on a variety of geometric parameters, including pore diameter, membrane porosity, and the location of the meniscus within the pore. Anodic aluminum oxide membranes were used as an experimental template. A bi-philic treatment was used to create a hydrophobic section of the pore to control meniscus location. This membrane was sealed in a text fixture shown in Figure 1. Heat was supplied to the membrane, and the resulting temperature was monitored.

We demonstrated different heat transfer regimes and observed more than an order-of-magnitude increase in dissipated heat flux by confining fluid within the nanopore, as seen in Figure 2. Similar tests were run systematically varying pore diameter, porosity, and meniscus location within the pore. We were able to show that pore diameter had little effect on evaporation performance at these pore diameters due to the negligible conduction resistance from the pore wall to the evaporating interface. The dissipated heat flux scaled linearly with porosity as the evaporative area increased. Furthermore, it was demonstrated that moving the meniscus as little as 1 µm into the pore could decrease performance significantly. The results of this study provide a better understanding of evaporation from nanopores and provide guidance in future high heat flux thermal management device design.



▲ Figure 1: Test fixture seen from a viewport in the experimental vacuum chamber. Insets show scanning electron microscopic images of the anodic aluminum oxide membranes used for evaporation tests. Scale bars: 1µm



▲ Figure 2: Surface temperature vs. heating power for samples of different pore diameter and porosity.

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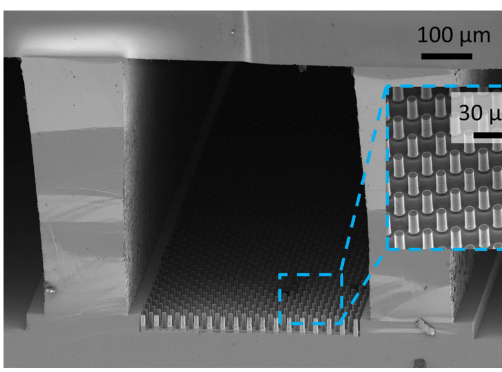
Suppressing High-Frequency Temperature Oscillations in Microchannel Heat Sinks with Surface Structures

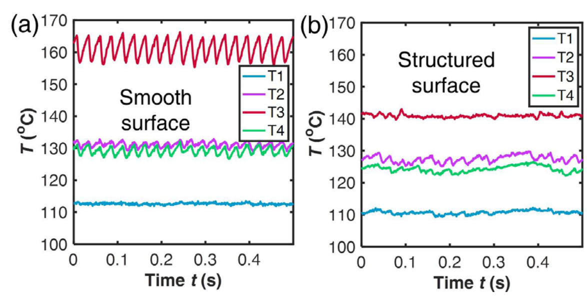
Y. Zhu, D. S. Antao, J. D. Sircar, T. J. Zhang, E. N. Wang
Sponsorship: ONR

Thermal management of high performance electronic devices such as gallium nitride (GaN) power amplifiers and solid-state lasers is critical for their efficient and reliable operation. Two-phase microchannel heat sinks are attractive for thermal management of high heat flux electronic devices, yet flow instability, which can lead to thermal and mechanical fatigue, remains a significant challenge. Much work has focused on long-timescale (~seconds) flow oscillations, which are usually related to the compressible volume in the loop. However, the rapid growth of vapor bubbles, which can also cause flow reversal, occurs on a much shorter timescale (~tens of milliseconds). While this high-frequency oscillation has often been visualized with high-speed imaging, its effect on the instantaneous temperature has not been fully investigated due to the typical low sampling rates of the sensors.

We propose to suppress this high-frequency temperature oscillation using surface microstructures that promote capillary wicking during flow boiling. We fabricated microchannels with micropillar arrays on the bottom heated surface (Figure 1). The geometries of the micropillars were optimized based our previously developed numerical model that maximizes the capillary flow. We then investigate the temperature response as a result of the high-frequency flow oscillation in microchannel heat sinks with smooth and microstructured surfaces with a measurement data acquisition rate of 1000 Hz. For smooth surface microchannels, the fluid flow oscillated between a complete dry-out and a rewetting annular flow due to the short-timescale flow instability, which caused high-frequency and large amplitude temperature oscillations (10 ˚C in 25 ms, Figure 2a). In comparison, hydrophilic surface structures on the microchannel promoted capillary flow, which delayed and suppressed dry-out in each oscillation cycle, and thus significantly reduced the temperature oscillation (Figure 2b) at high heat fluxes. This work suggests that promoting capillary wicking via surface structures is a promising technique to reduce thermal fatigue in high heat flux, two-phase, microchannel thermal management devices.



▲ Figure 1: Scanning electron micrograph of the cross-sectional view fabricated microchannel (width = height = 500 µm) with microstructures investigated in this study. Magnified view shows the micropillar arrays (diameter *d*=10 µm, pitch *l*=30 µm, and height *h*=25 µm).



▲ Figure 2: Time-resolved temperature measurement of (a) a smooth surface microchannel and (b) a structured surface microchannel (mass flux = 100 kg/m^{2}s, heat flux = 400 W/cm^2). T1-T4 are the measured temperatures along various locations at the backside of the microchannel.

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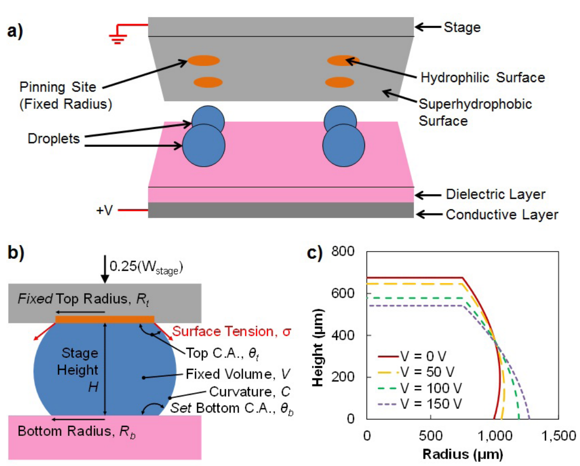
EWOD Actuation of a Vertical Translation and Angular Manipulation Stage

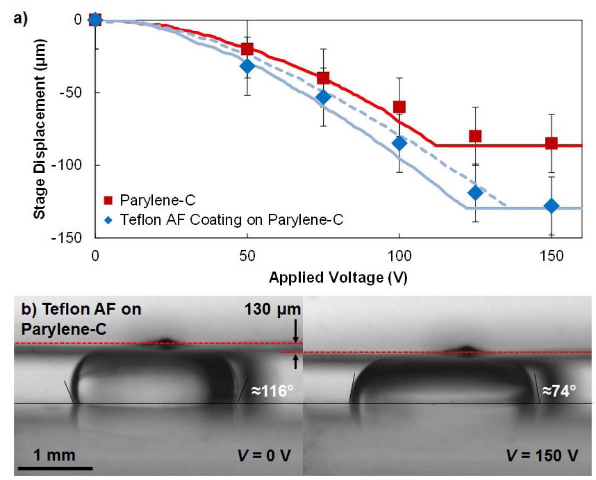
D. J. Preston, A. Anders, B. Barabadi, E. Tio, Y. Zhu, D. A. Dai, E. N. Wang
Sponsorship: ONR

Adhesion and friction during physical contact of solid components in microelectromechanical systems (MEMS) often lead to device failure. Translational stages that are fabricated with traditional silicon MEMS typically face these tribological concerns. Meanwhile, electrowetting, a phenomenon whereby the contact angle of a fluid can be changed with an applied voltage, allowing control of droplet shape, has had a limited role in MEMS applications. We show through modeling and experimental demonstration that the electrowetting-on-dielectric (EWOD) technique has the potential to eliminate solid-solid contact during MEMS stage operation by actuating via deformable liquid droplets placed between the stage and base to achieve stage displacement as a function of applied voltage (Figure 1).

Our EWOD stage is capable of linear spatial manipulation with resolution of 10 µm over a maximum range of 130 µm and angular deflection of approximately ±1°, comparable to piezoelectric actuators (Figure 2). We demonstrate with our model that a higher intrinsic contact angle on the EWOD surface can further improve the translational range, which was validated experimentally by comparing different surface coatings. The capability to operate the stage without solid-solid contact offers potential improvements for applications in micro-optics, actuators, and other MEMS devices.



▲Figure 1: (a) Tops of the droplets contact the underside of the stage at hydrophilic copper pinning sites surrounded by a superhydrophobic surface, and bottoms of the droplets rest on the EWOD-actuated base, (b & c) device actuation is modeled for a single axisymmetric droplet, with expected stage height shown for a 2-µL droplet on a surface with a Young contact angle of 110°.



▲Figure 2: (a) Combining the Lippmann-Young equation with the axisymmetric droplet model shown in Figure 1 b & c allows prediction of the stage height as a function of applied voltage, which is in good agreement with the experimental results for stage deflection, (b) experimental images show the stage vertical translation at an applied voltage of 150 V, which resulted in a deflection of 130 µm.

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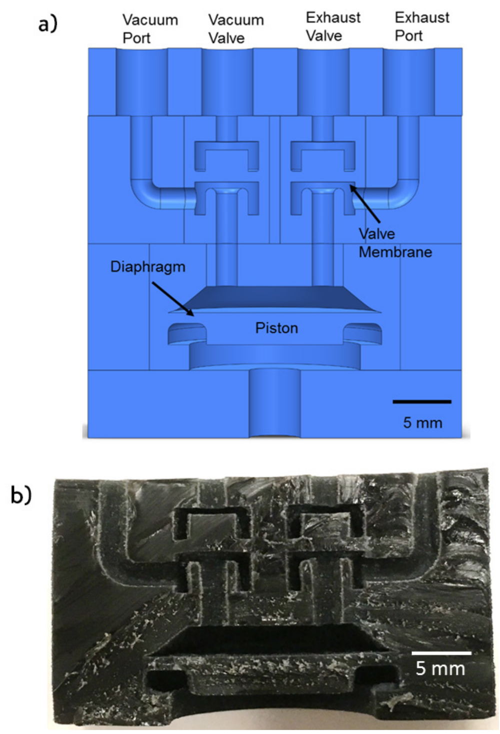
Additively Manufactured Miniature Diaphragm Vacuum Pumps

A. P. Taylor, L. F. Velásquez-García
Sponsorship: Edwards Vacuum

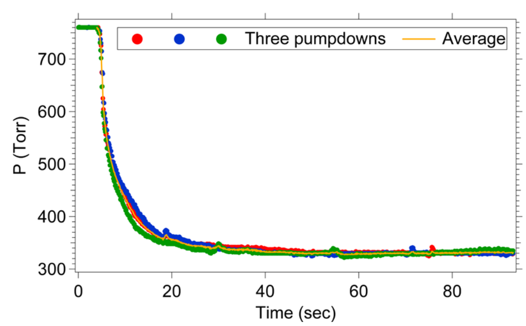
Miniaturized pumps supply fluids at precise flow rates and pressure levels in a wide variety of microfluidic systems. In particular, microfabricated positive displacement pumps that exploit gas compressibility to create vacuum have been reported as a first pumping stage in non-zero flow, reduced-pressure miniaturized systems, such as mass spectrometers. Compared to standard microfabrication, additive manufacturing offers the advantages of rapid prototyping, larger displacements for better vacuum generation and larger flow rate, freeform geometries, and a broader material selection while attaining minimum feature sizes on par with microfluidic systems (out-of-plane features in the 10-300-µm range and in-plane features in the 25-500-µm range). In addition, a number of 3-D printing techniques make possible the definition of leak-tight, closed channels or cavities, sometimes involving a second sacrificial material that is removed after printing.

Using polyjet 3-D printing technology with 42-µm XY pixelation and 25-µm layer height, a single-stage vacuum pump design with active valves and a total pumping volume of 1 cm^3 with 5% dead volume was implemented (Figure 1a). Devices were printed in the acrylate based, UV curable photopolymer TangoBlack Plus® (Shore 27A) in one piece (Figure 1b) or in two halves for ease in removing the sacrificial material. The pumps were pneumatically actuated and consistently pumped down a 1 cm^3 volume from atmosphere to 330 Torr in under 50 seconds operating at 3.27 Hz (Figure 2); from the data, the effective flow rate of the device is estimated at 8.7 cm^3/min.

The compression chamber diaphragms exhibited lifetimes approaching 20,000 cycles, while the valves' membranes have not leaked after >1-million cycles. Current work focuses on increasing the diaphragm lifetime, reducing the ultimate pressure, and improving the mass flow rate vs. pressure pump characteristics.



▲ Figure 1: (a) Design of the miniature diaphragm pump, and (b) image of a pump printed in one piece.



▲ Figure 2: Vacuum port pressure vs. time for several pump downs and average pump down characteristic, 3.27 Hz actuation.

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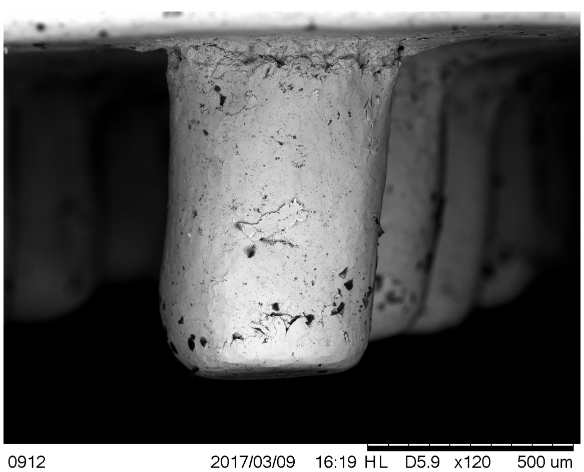
Evaluation of Lost-Wax Micromolding for Additive Manufacturing of Miniaturized Metallic Vacuum Components

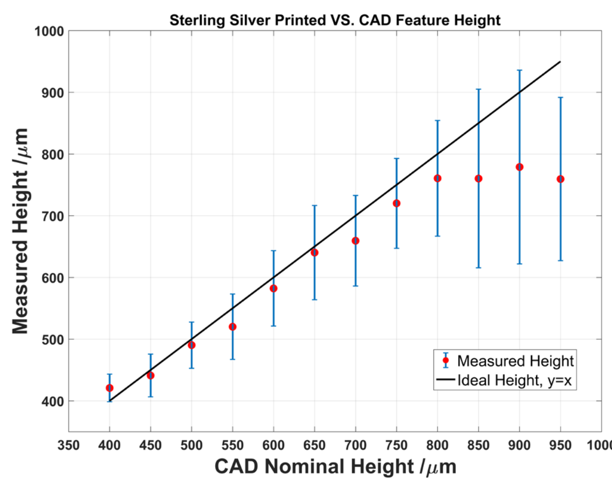
Z. Sun, L. F. Velásquez-García
Sponsorship: MIT, Skoltech Program

In contrast to traditional subtractive methods, additive manufacturing (AM) is a process of joining materials layer by layer to generate solid structures from computer-aided design (CAD) data. Benefits of AM include the reduction of the raw materials required to make the part, fast manufacturing speed, versatility, and adaptability. Furthermore, AM has the potential to enable novel designs that could not be fabricated with conventional machining practices and to enhance the capability of true 3-D micromanufacturing. Standard 3-D printing of metallic parts is done via selective laser sintering, where a coherent photon beam is used to create a solid from the melting of metal powders. However, the printed structures are coarse and porous with profusely outgassing surfaces and have electrical conductivity and mechanical strength less than those of the bulk material. Therefore, there is a need for better AM technologies to fabricate vacuum-compatible miniaturized metallic structures.

In this project, we are exploring lost-wax micromolding as an alternative AM technology for metal parts. Wax masters printed via stereolithography were duplicated in sterling silver by encasing the master in a ceramic mold, removing the wax by melting it, and filling-in with metal the cavities left within the mold after wax removal; finally, the parts are extracted from the mold and polished. An array of pillars (Figure 1) with diameter varying from 350 μm to 500 μm and height from 400 μm to 950 μm was created to characterize feature size repeatability (Figure 2). We found close agreement between the intended and cast heights for cylinders 400 μm to 750 μm tall; however for taller cylinders, the measured values are smaller than expected, and the standard deviation is also larger. This might be related to the way high aspect-ratio pillars with a small diameter solidify during casting. Further work will focus on completing the exploration of this technology to print solid, pore-free metal parts including characterization of physical properties such as roughness, thermal diffusivity, and vacuum outgassing.



▲ Figure 1: Scanning electron microscope (SEM) image of the side view of one pillar in the sterling silver resolution matrix.



▲ Figure 2: Measured lost-wax cast height vs. CAD file height in the sterling silver resolution matrix.

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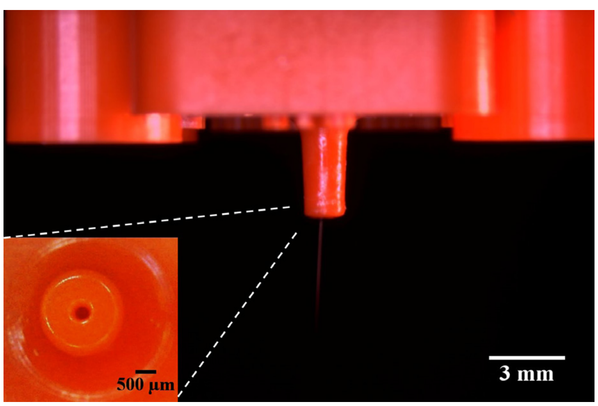
3-D Printed Multiplexed Electrospinning Sources for Large Production of Nanofibers

E. García-López, D. Olvera-Trejo, L. F. Velásquez-García
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

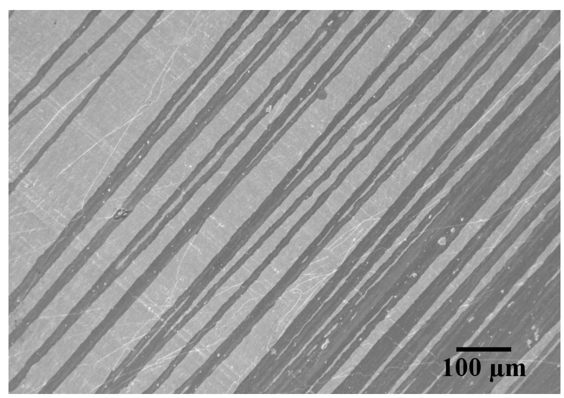
Electrospinning is a versatile process that creates ultrathin nanofibers via electro-hydrodynamical jetting. Electrospun nanofibers are used in a wide variety of biomedical (i.e., tissue healing/scaffolding, drug delivery), energy (i.e., electrodes, solar cells), and microsystem applications (i.e., sensors, batteries). Even though electrospinning is the only technique capable of generating nanofibers of arbitrarily length using a wide variety of feedstock, the throughput of an electrospinning emitter is very low, making difficult the use of these fibers in commercial products. Multiplexing the emitters, i.e., implementing arrays of emitters that work in parallel, is an attractive approach to increase the throughput of electrospinning sources without sacrificing the quality of the fibers generated. Microfabricated multiplexed electrospinning sources that achieve uniform operation at low voltage and large emitter density have been reported. However, these devices do not really solve the problem well as they are made with standard microfabrication, which is expensive and time-consuming.

In this project, we are exploring stereolithography (SLA) to create disposable electrospinning sources capable of high-throughput generation of fibers. In SLA, UV light is focused on a photopolymer while 3-D layers are created through crosslinking, making it possible to print complex three-dimensional structures. The SLA process has several advantages over competing approaches such as a higher resolution, higher quality surface, higher customization, and the creation of watertight imprints.

Devices with emitters with 300-µm internal diameter have been created (Figure 1). Measured per-emitter vs. flow rate characteristics using a PEO solution demonstrates that the arrays operate uniformly. Current research focuses on maximizing the throughput of the sources by emitter multiplexing, exploring approaches for charging up the emitted jets to produce thinner fibers, and in collecting and characterizing aligned PEO nanofibers using a drum as a collector system for tissue engineering applications (Figure 2).



▲ Figure 1: 3-D printed device with one emitter producing PEO nanofibers.



▲ Figure 2: Aligned PEO nanofibers collected using a rotating drum collector.

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Atmospheric Microplasma-Based 3-D Printing of Metallic Microstructures

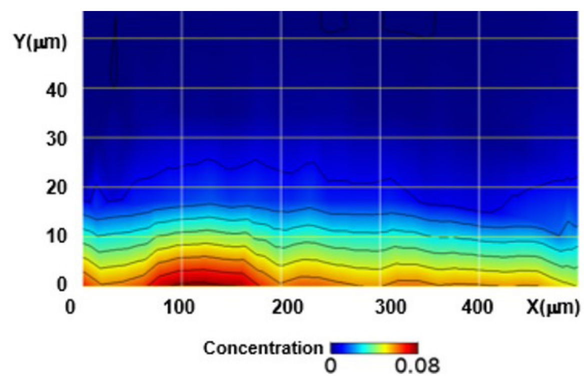
Y. Kornbluth, R. Mathews, L. Parameswaran, L. M. Racz, L. F. Velásquez-García
Sponsorship: MIT Lincoln Laboratory

State-of-the-art additive manufacturing techniques for metallic microstructures cannot yet deliver the feature resolution, electrical conductivity, and material choice flexibility needed for high-performance microcircuits. Further, many current and proposed additive manufacturing approaches for fine-geometry metal features require high-temperature post-processing and restrict the substrate material. We aim to develop a microplasma-based sputtering system able to direct write a wide range of materials onto any substrate. We have modeled, designed, and constructed a first-generation system that sputters gold onto a substrate. By manipulating the metal at the atomic level, we retain the resistivity of bulk metal, and by sputtering the metal, we eliminate the need for post-processing or lithographic patterning.

We use a microplasma to sputter metal at atmospheric pressure, obviating the need for a vacuum. Our microplasma generator uses electrostatic fields to focus the imprints. With a suitable electrode arrangement, we can shape electrostatic fields that will guide the ionized fraction of the working gas towards a localized spot on the substrate. The directed ions will collide with other gas atoms and, crucially, with sputtered metal atoms from the sputtering target. The net force due to these collisions will indirectly guide the metal atoms towards the desired part of the substrate. This indirect electrostatic focusing not only mitigates the inherent spread of the sputtered material caused by collisions at atmospheric pressure, but also enables feature definition. In the absence of collisions, the printed line will be wider than the sacrificial cathode. By focusing the sputtered material, we achieve imprints significantly narrower than the cathode. This precludes the need to machine sacrificial electrodes as small as our desired printed lines.

Our microplasma head has a central target wire acting as the cathode, surrounded by four electrodes (Figure 1), two biased at a positive voltage (relative to the grounded target) to form the plasma, and the other two biased at a negative voltage to focus the plasma. By both pulling and pushing the plasma, COMSOL simulations predict imprints orders of magnitude narrower than the cross section of the target wire (Figure 2).

▲ Figure 1: A picture of two electrode assemblies. The target wire is installed at the center of the structure. The resulting plasma sputters metal atoms from the target, which then are carried towards the substrate by the gas flow and the electrostatic drag.



▲ Figure 2: COMSOL simulation results showing a top-down view of the distribution of sputtered material on the substrate. Only one quarter of the substrate is shown because the simulation is symmetric on the two in-plane axes. For an optimized set of parameters, simulations predict that a 15-µm-wide (full width half maximum) gold line is printed on the substrate.

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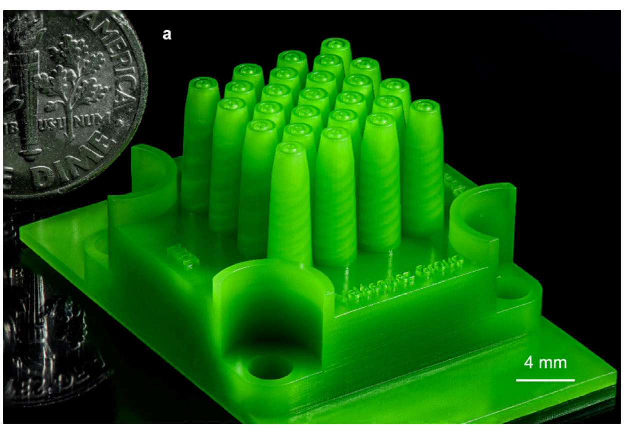
MEMS Electrohydrodynamic High-Throughput Core-Shell Droplet Sources

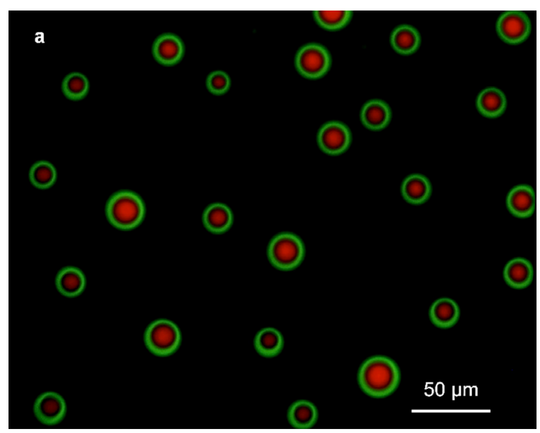
D. Olvera-Trejo, L. F. Velásquez-García
Sponsorship: MIT-Tecnológico de Monterrey Nanotechnology Program

Coaxial electrospraying is a microencapsulation technology based on electrohydrodynamic jetting of two immiscible liquids that allows precise control with low size variation of the geometry of the core-shell particles it generates. Coaxial electrospraying is a very promising microencapsulation technique because (i) it is easy to implement, (ii) it can operate at room temperature and at atmospheric pressure, (iii) it does not require a series of steps in the encapsulation process, (iv) it can generate compound droplets with narrow size distribution, and (v) it can be used to encapsulate a great variety of materials of interest to biomedical and engineering applications. State-of-the-art coaxial electrospray sources have very low throughput because they have only one emitter. Consequently, coaxial electrosprayed compound particles are compatible with only high-end applications and research.

An approach to increasing the throughput of a coaxial electrospray source without affecting the size variation of the emitted compound microparticles is to implement arrays of coaxial emitters that operate in parallel. However, no miniaturized coaxial array sources have been reported, probably due to the inherent three-dimensionality of the emitter geometry and the hydraulic network required for uniform array operation, which is at odds with the planar nature of traditional microfabrication. In this project, we demonstrated the first MEMS multiplexed coaxial electrospray sources in the literature. Miniaturized core-shell particle generators with up to 25 coaxial electrospray emitters (25 emitters·cm^{-2}) were fabricated via digital light projection/stereolithography (DLP/SLA, Figure 1), which is an additive manufacturing process based on photopolymerization of a resin that can create complex microfluidics. The characterization of emitter arrays with the same emitter structure but different array size demonstrates uniform array operation. The core/shell particles produced by these additively manufactured sources are very uniform (Figure 2); the size distribution of these compound microparticles can be modulated by controlling the flow rates fed to the emitters.



▲ Figure 1: DLP/SLA 3-D printed monolithic array of coaxial electrospinning emitters.



▲ Figure 2: Core-shell microdroplets generated by massively multiplexed MEMS coaxial electrospray sources. The feedstock was colored with fluorescent dyes to help visualize the structure of the droplets.

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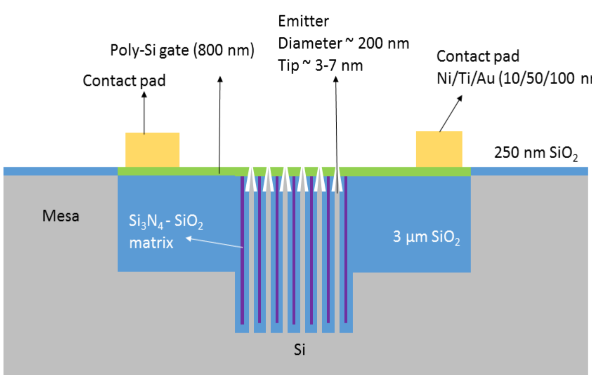
High Current Density Si-field Emission Arrays (FEAs)

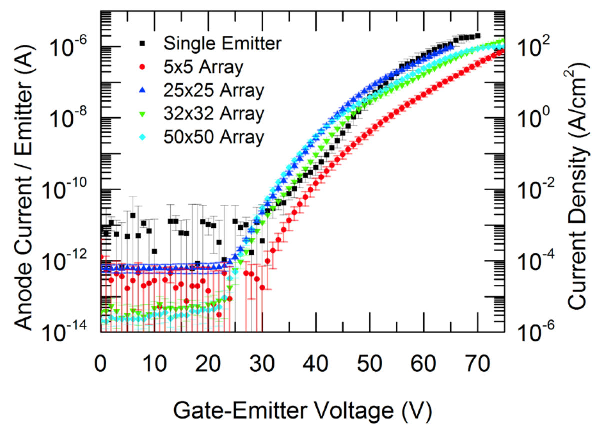
G. Rughoobur, S. A. Guerrera, A. I. Akinwande
Sponsorship: RAVEN/IARPA

Silicon field emitter arrays (FEAs) are excellent cold cathodes that have not been fully exploited due to the nonzero tip radius distribution causing lower utilization of the arrays. This discrepancy in emitter tips causes sharper tips to burn out (by Joule heating) before duller tips, and therefore the maximum current achievable is small. In this work, we focus on achieving high current density Si FEAs, by integrating high-aspect ratio Si nanowires as to limit the supply of electrons and hence saturate the maximum current to avoid the burn-out of the sharper tips.

Si nanowires of height ~10 µm and 100-200-nm diameter limit the current and improve reliability through velocity saturation and the pinch-off of majority carriers. To prevent charge injection and minimize the gate-substrate capacitance, a 2-µm-thick SiO_2 insulator is added, and the Si nanowires are embedded in a conformal dielectric matrix consisting of Si_3N_4 and SiO_2. High current densities are achieved as the nanowires (current limiter) are integrated with each field emitter, thereby preserving a high density of operational emitters (~10^8 emitters/cm²) without burning out. These Si FEAs have also been shown to provide consistent current scaling of array sizes from a single emitter to 25,000 emitters, low voltage ($V_{GE} < 60$ V), high current density ($J > 100$ A/cm²), and long lifetime ($\tau > 100$ hours at 100 A/cm², > 100 hours at 10 A/cm², and > 300 hours at 100 mA/cm²). Compared to conventional Si FEAs operating without a current limiter, the device architecture shown here demonstrate a current density improvement of > 10 folds and low turn-on voltage (8.5 V). Cold cathodes based on Si-FEAs incorporating a current limiter have high potential in applications ranging from X-ray imaging, RF amplifiers, and THz sources to deep UV sources, ion sources, and neutron sources.



▲Figure 1: Device architecture demonstrating the 200-nm-diameter 10-µm-tall Si nanowires integrated below the field emitters, embedded in a dielectric matrix encapsulated with a poly-Si gate and metal pads for contact.



▲Figure 2: Comparison of the transfer characteristics of 5 different devices scaled by the number of emitters showing values of $J \sim 100$ A/cm².

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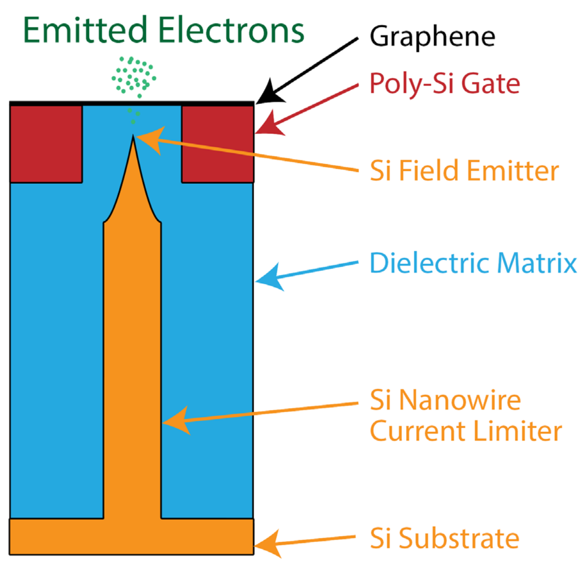
Field Emission from Silicon Tips Embedded in a Dielectric Matrix

N. Karaulac, S. A. Guerrera, M. T. Cole, W. I. Milne, A. I. Akinwande
Sponsorship: DARPA, IARPA

Field emitter arrays (FEAs) are a class of cold cathodes with promising potential in a variety of applications requiring high current density electron sources. However, FEAs have not yet achieved widespread usage because of fundamental challenges that limit their reliability in systems. Field emission from conducting surfaces requires high fields and pristine surfaces; these surfaces are vulnerable to adsorption-desorption processes by residual gas molecules, leading to emission current fluctuations and tip erosion. Moreover, electron transport through insulators often leads to impact ionization and dielectric breakdown. This project explores electron emission from field emitter tips that are embedded in a dielectric matrix, specifically silicon dioxide, as a potential approach to address reliability problems in classical field emitters.

In the project, arrays of silicon emitter tips that are individually regulated by silicon nanowires are being fabricated. The silicon nanowires have diameters between 100-200 nm and heights of 10 µm, resulting in an aspect ratio of 50-100:1. The emitter tips typically have radii of 5 nm with a log-normal distribution and a density of 10^8 tips/cm^2. Further, the silicon nanowires function as current limiters that improve reliability by preventing premature tip burn-out due to Joule heating, thermal runaway, and cathodic arcs. Chemical mechanical polishing (CMP) was used to form the self-aligned gates. The silicon tips formed by oxidation sharpening are embedded in a dielectric matrix and are not released. A diagram of the structure is shown in Figure 1.



▲ Figure 1: Diagram of a silicon field emitter tip embedded in silicon dioxide with single-layer graphene on top.

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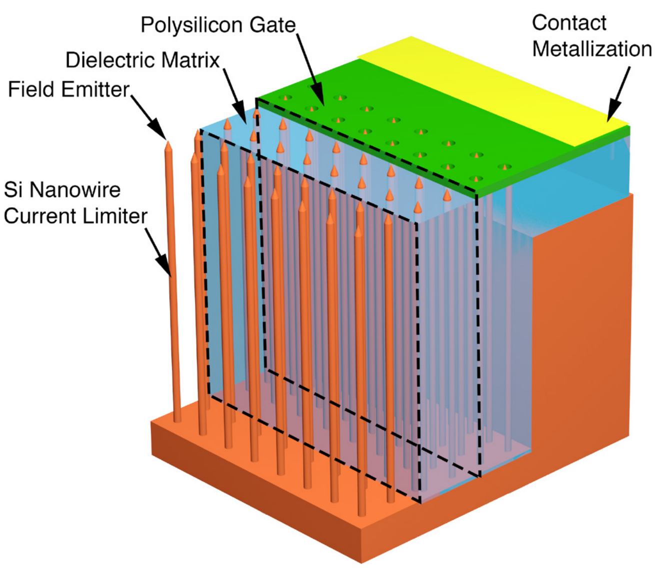
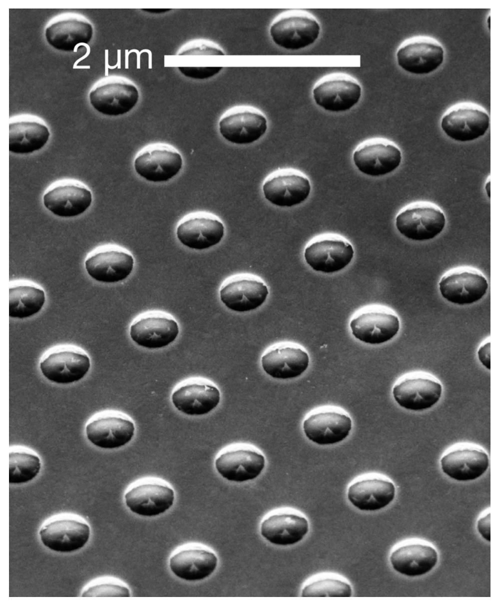
A Silicon Field Emitter Array as an Electron Source for Phase Controlled Magnetrons

W. Chern, S. Guerrera, A. I. Akinwande
Sponsorship: AFOSR

Magnetrons are a highly efficient (>90%), high-power vacuum-based microwave source. In a magnetron, free-electrons in vacuum are subject to a magnetic field while moving past open metal cavities, resulting in resonant microwave radiation to be emitted. Current state-of-art magnetrons use a heated metal filament to thermionically emit electrons into vacuum continuously and are not addressable. This work seeks to replace the heated metal filament as a source of electrons with silicon field emitter arrays in order to improve the efficiency and increase the power, especially when several sources are combined. Silicon field emitter arrays, schematic shown in Figure 1, are devices that are normally off and are capable of high current densities plus spatial and temporal addressing. These arrays consist of a many sharp tips made of silicon sitting on long silicon nanowires that limit the current of the electron emission. Electrons from the silicon tip tunnel into a vacuum as a result of the high electric field of the applied bias on the polysilicon gate. Pulsing the electric field applied on the gate can turn the arrays on and off. The proposed use of silicon field emitter arrays in a magnetron will allow injection locking and hence phase control of magnetrons. Phase-controlled magnetrons have multiple applications in areas where high-power microwave sources are desired.





▲ Figure 1: (Left) 3-D rendering of Si device structure. For clarity, layers have been omitted in different regions of the rendering to show detail. In the front, the bare silicon nanowires [200-nm diameter & 10-μm height] with sharp tips. (Right) Top-view of a fabricated device with 350-nm gate aperture and 1-μm tip-to-tip spacing.

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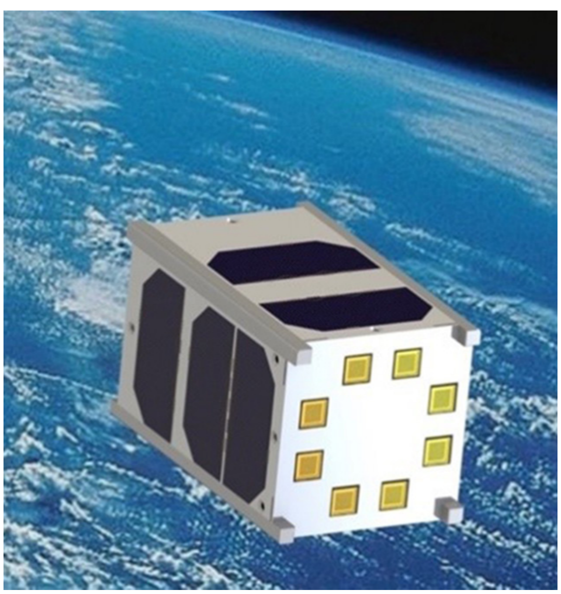
Ion Electrospray Thrusters for Microsatellite Propulsion

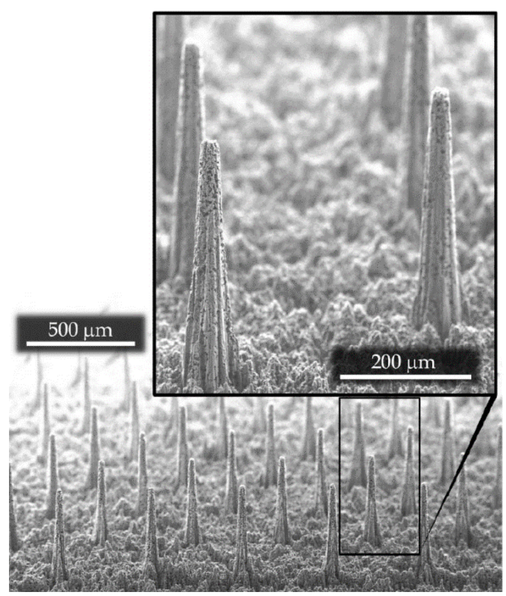
D. Freeman, D. Krejci, C. Fucetola, H. Li, A. Bost, P. Lozano
Sponsorship: U.S. Department of Defense

Ion electrospray propulsion systems (iEPS) are high specific impulse, low thrust, and extremely scalable devices; these characteristics make them excellent candidates for propulsion systems on microsatellites, which require some small amount of maneuverability primarily for station-keeping. Like other ion engines, they utilize an electrostatic potential to accelerate charged particles across a gap to relatively high velocities to generate thrust. Utilizing ionic liquids – a special class of molten salts that do not evaporate in vacuum, thanks to their negligible vapor pressure – drastically increases the propellant density and obviates the need for a stage in which the propellant is first ionized, thus further reducing mass and volume requirements. The thrusters themselves are extremely simple in that they are passively fed through capillary action and require no moving parts. However, high electric fields, on the order of 10^9 V m^{-1}, are required to extract ions from the liquid. This entails careful fabrication of the porous emitter substrates, which feature an array of roughly five hundred tips, patterned into the surface via laser ablation. By providing a sharp tip, the electric field is effectively intensified to the point that ions can be extracted, through a sharpening effect similar to coronal discharge.

The thrusters are constructed from several component parts. The frames are made via microelectromechanical (MEMS) processing: a silicon base layer, an insulating glass layer, and finally a top silicon layer with alignment features to correctly locate the tip array is etched and then anodically bonded. To those frames a porous substrate is affixed after being shaped and polished. A tip array is patterned into the substrate via laser ablation. Next, a silicon electrode grid, also fabricated with MEMS processing, is bonded to the frame so that the grid holes are aligned to the tip array, completing the emitter. The emitters are then bonded onto tanks that passively transport propellant to the emitter. The tanks are mounted on electronic power supply/control boards, creating a finished engine that may be integrated into a spacecraft. Four small satellites (CubeSats) equipped with these thrusters have already been launched into space. Our team is currently working on a new project, set to launch during Q1 of 2018.



▲Figure 1: Illustration of 8 iEPS emitters, mounted on a small satellite.



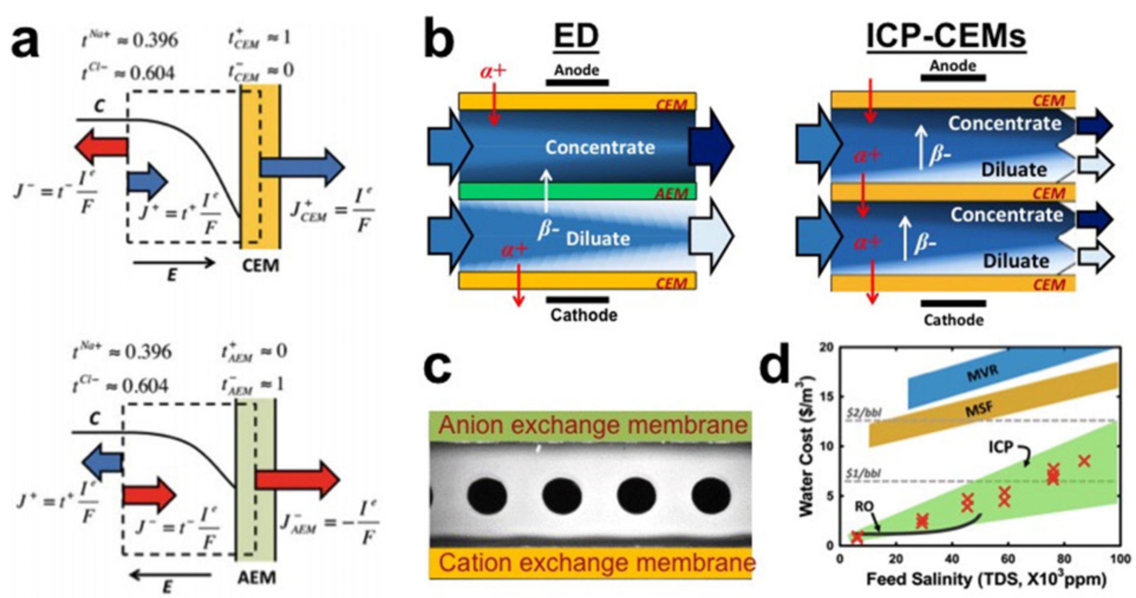
▲Figure 2: SEM of a patterned emitter chip. Periodically blanking the beam of a picosecond 355-nm laser ablates the material around the tips.

Enhanced Water Desalination in Electromembrane Systems

S. Choi, B. Kim, J. Yoon, J. Han, B. Al-Anzi, J. White, S. V. Pham
Sponsorship: Kuwait-MIT Center Signature Research Project, KFAS

Currently, reverse osmosis (RO) is considered the leading technology for desalination, and the operational efficiency of RO has been significantly improved over the last two decades with a thorough energy analysis. On the other hand, electrical desalination can be more advantageous in certain applications due to the diversity of allowed feed conditions, operational flexibility, and the relatively low capital cost needed (the size of a system is generally small). Yet, electromembrane desalination techniques such as electrodialysis (ED) have not been modeled in full detail, partially due to scientific challenges involving the multiphysics nature of the process.

In addition, while current ED relies on bipolar ion conduction (Figure 1b), removing one pair of a cation and an anion simultaneously, one final but most important point is that desalination achieved by means of an anion exchange membrane (AEM) and a cation exchange membrane (CEM) should be considered separately and independently (Figure 1a). Based on the intrinsically different ion transport near AEM and CEM, our group previously presented a novel process of ion concentration polarization (ICP) desalination (Figure 1b), which can basically enhance the amount of salt reduction, by examining unipolar ion conduction through both experiments and numerical modeling. In our studies, we investigate the effects of embedded microstructures on mass transport enhancement; these microstructures affect the electrical energy efficiency of an ED system for its current application of brackish (low salinity) water desalination (Figure 1c); we also explore the technical and economic feasibility of the ICP desalination for potential applications in the emerging field of high-salinity brine desalination (Figure 1d).



▲ Figure 1: (a) Schematic diagram of counter-ion/co-ion transport near CEM/AEM, (b) schematics of ED (left) and ICP desalination (right), (c) microfluidic image of ED channel with embedded structures, (d) water cost plot for various desalination technologies in a range of feed salinities.

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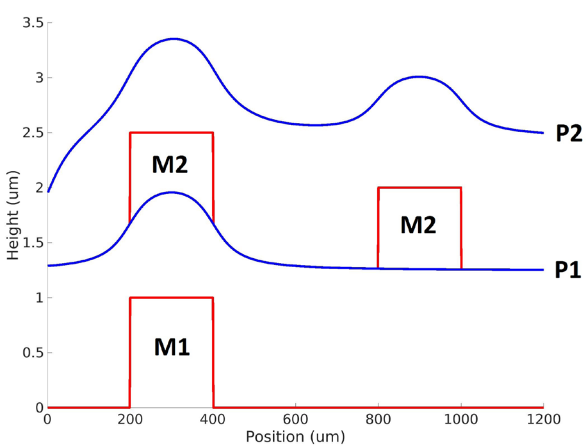
Nanotechnology and Nanomaterials

Modeling and Controlling Variations in Advanced 2.5D Packaging Fabrication

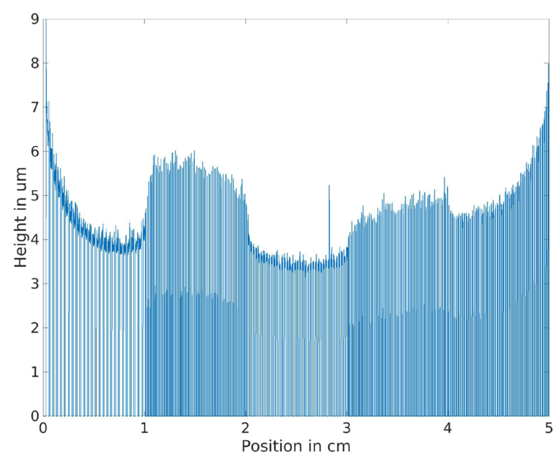
C. I. Lang, D. S. Boning
Sponsorship: TSMC

Re-distribution layers (RDLs) are separate packaging layers dedicated to connecting die to one other and to external I/O ports in advanced 2.5D packaging technologies. These layers can be made smaller than the bulky metal traces in conventional substrate packaging, reducing electrical delay and power consumption. Currently, the damascene process is the most common method to create the copper traces in RDLs. However, due to the required inclusion of chemical mechanical polishing (CMP), this process is significantly more expensive than semi-additive electrochemical plating (ECP) and dielectric spin-coating (DSC) processes. The semi-additive techniques are typically avoided as, without CMP, they suffer from thickness variations following the fabrication of each layer. As multiple layers are fabricated, these variations compound and can result in a structure with significant topographical and electrical performance concerns.

Here, we model and predict the non-uniformities in both the DSC (Figure 1) and ECP (Figure 2) process. We first design test vehicles (TVs) which represent topographies common in RDLs, most notably the copper lines and vias, and use these to experimentally determine the thickness variations caused by each process. We then develop empirical models based on these results. The DSC process is modeled as a convolution between the underlying topography (typically the copper lines) and an appropriately chosen impulse response, while the ECP growth rate is modeled as a function of the effective line width and spacings. Finally, we are currently developing and testing dummy fill and cheesing patterns that have the potential to control the variations from both processes. These patterns can be applied to any existing RDL layout, thus ensuring surface planarity without the use of CMP.



▲Figure 1: Mock RDL cross section consisting of two metal layers and two polyimide layers. Spin coating over non-uniform surfaces leads to variations that carry through to subsequent layers.



▲Figure 2: Cross section of copper interconnects grown using ECP. Differences in line widths and spacings lead to different growth rates and structural variations.

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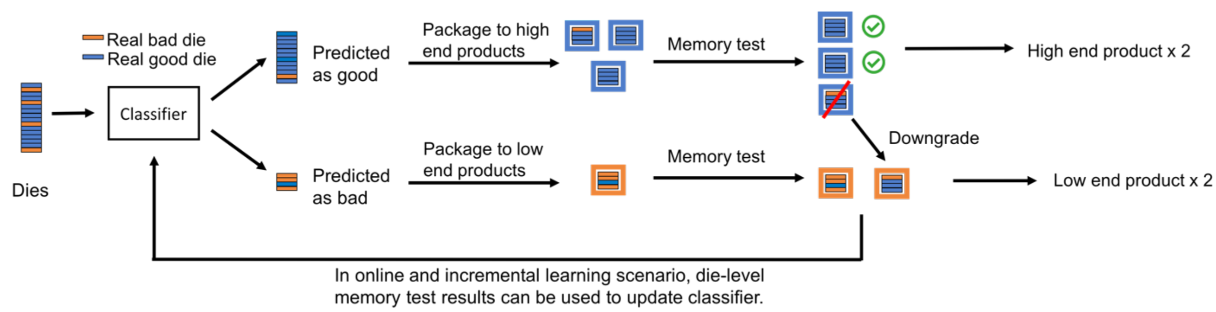
Online and Incremental Machine Learning Approaches for IC Yield Improvement

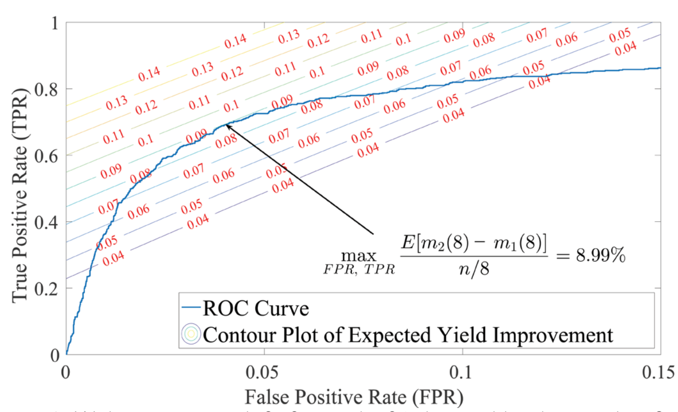
H. Chen, D. S. Boning

In the competitive semiconductor manufacturing industry, where large amounts of data are generated, data-driven quality control technologies are gaining increasing importance. In this work, we build machine learning models for high-yield and time-varying semiconductor manufacturing processes. Challenges include class imbalance and concept drift. Class imbalance is due to high manufacturing yield causing small numbers of failure cases compared to passing cases. Concept drift refers to unexpected or unknown changes in the statistical properties of the dataset. Batch and online ensemble machine learning techniques are proposed to address the problem of class imbalance. An incremental learning framework that combines classifiers trained on different data chunks is designed to overcome the problem of concept drift.

We study the packaging and testing process in chip stack flash memory as an application. We build a mathematical model and demonstrate the possibility of yield improvement using a classifier to detect bad dies before packaging. Experimental results demonstrate significant yield improvement potential using real data from industry. Without concept drift, for stacks of 8 dies, an approximately 9% yield improvement can be achieved. In a longer periods of time with realistic concept drift, our incremental learning approach achieves approximately 1.4% yield improvement in the case of a stack of 8 dies and 3.5% in the case of a stack of 16 dies, which are 4.4×× and 1.5×× of the yield improvement using a single classifier trained only on the most recent data.



▲ Figure 1: The packaging and memory testing process with a classifier.



▲ Figure 2: Without concept drift, for stack of 8 dies, yield without a classifier= 77.54%; yield with a classifier= 86.53%, optimal classification threshold=0.68.

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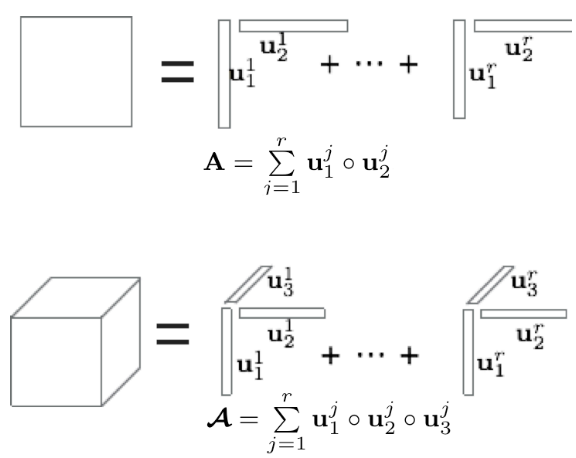
Tensor Recovery for Stochastic Simulation of Nanoscale Devices and Circuits with Many Process Variations

Z. Zhang, T.-W. Weng, L. Daniel
Sponsorship: NSF NEEDS, AIM Photonics

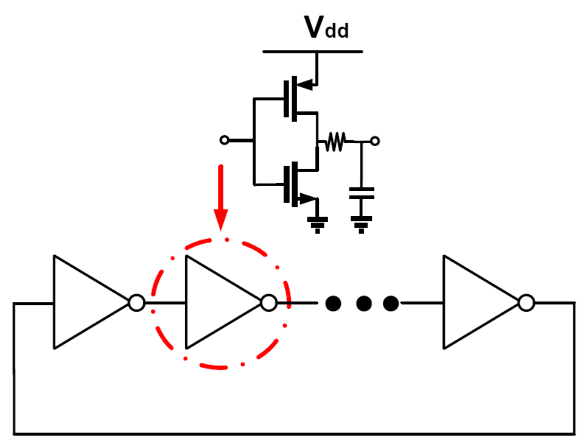
Process variations have become a "red-brick" problem that the semiconductor industry is progressing toward. A random fluctuation at the atomic scale can cause a large impact on the performance of nanoscale and device simulations. In order to increase chip yields, the uncertainties caused by process variations must be well estimated and controlled before a final fabrication. In traditional EDA tools, Monte Carlo-type simulators perform such a task. Recently, stochastic spectral methods have emerged as a promising alternative. They are much more efficient than Monte Carlo simulators for certain design cases, but their efficiency can degrade as the number of process variations increases.

Our approach can efficiently handle design problems with 50 to 60 uncorrelated random parameters. We represent the huge number of device/circuit simulation samples in stochastic collocation by a tensor, which is a representation of a high-dimensional data array. Then, similar to the matrix case, we can exploit the low-rank structure of a tensor to reduce the storage and computational cost, as shown in Figure 1. Combining this low-rank property with the sparse property in high-dimensional generalized polynomial-chaos expansion, we have suggested a low-rank and sparse tensor recovery model. This optimization model allows us to estimate the huge number of unknown simulation samples based on a small number of available simulation results. Therefore, the computational cost can be reduced from an exponential one to a linear one.

This approach has been successfully applied to solve stochastic modeling and simulation problems in microelectromechanical systems (MEMS) design and in complementary metal-oxide semiconductor (CMOS) integrated circuit (IC) design. For the CMOS ring oscillator with 57 uncorrelated process variations in Figure 2, stochastic collocation using a standard deterministic numerical integration requires 1.6E27 simulation samples, whereas our tensor recovery approach only needs 300 simulation samples to construct a highly accurate (with 1% relative error) stochastic model for the oscillator frequency.



▲ Figure 1: Low-rank decomposition of a matrix (top) and low-rank decomposition of a tensor (bottom). The low-rank decomposition allows representation of high-dimensional data arrays using a few vectors.



▲ Figure 2: A CMOS ring oscillator. This circuit has 57 independent random parameters describing the variations of transistor threshold voltage, gate oxide thickness, channel length, and width.

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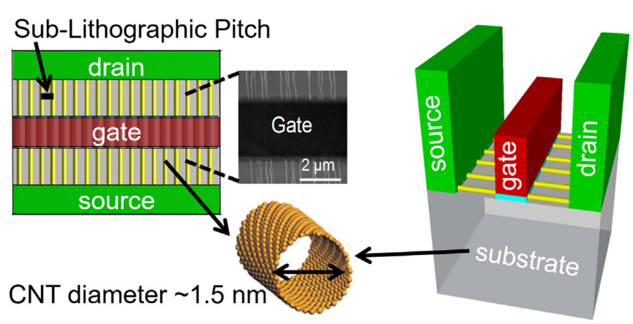
Realizing Monolithic Three-dimensional Integrated Circuits with Emerging Nanotechnologies

T. Srimani, M. Bishop, M. M. Shulaker
Sponsorship: Analog Devices, Inc.

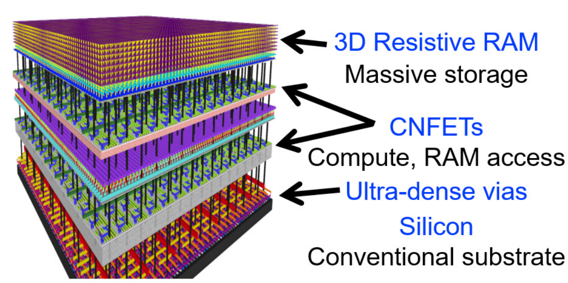
The computing demands of future data-intensive applications far exceed the capabilities of today's electronics and cannot be met by isolated improvements in transistor technologies or integrated circuit (IC) architectures alone. Rather, transformative nanosystems that leverage the unique properties of emerging nanotechnologies to create new three-dimensional IC architectures are required to deliver unprecedented performance and energy efficiency. However, emerging nanomaterials and nanodevices are subject to significant imperfections and variations; thus, realizing functional circuits, let alone transformative nanosystems, has previously been infeasible.

As an example, carbon nanotubes (CNTs) are a promising emerging nanotechnology with exceptional electrical, thermal, and physical properties. Due to these benefits, very-large-scale integrated (VLSI) digital circuits fabricated from carbon nanotube field-effect transistors (CNFETs) are projected to run 3X faster than silicon FinFETs, while simultaneously consuming 3X less energy, resulting in an order-of-magnitude improvement in energy-delay product (EDP, a metric of energy efficiency) for digital VLSI circuits. Despite demonstrations of high performance and scaled CNFETs, realizing VLSI-scale CNFET circuits has previously been prohibited by substantial imperfections and variations to CNTs. For instance, due to the imprecise control over CNT properties, CNTs can be either semiconducting or metallic (metallic CNTs have little or no bandgap and result in increased circuit leakage power and incorrect logic functionality), and non-uniform spacing between CNTs results in variations in the number of CNTs within each CNFET (resulting in degraded noise resilience, increased delay variations, and decreased yield). To overcome these obstacles, we are developing new fabrication and processing techniques, as well as new circuit design techniques. Importantly, while relying on processing or design solutions alone is insufficient, combining approaches allows us to overcome these obstacles and realize, for the first time, energy-efficient VLSI digital systems made from CNFETs.

Additionally, CNFETs present a unique opportunity to radically impact systems beyond providing improved transistors. Specifically, CNFETs enable monolithic 3-D nanosystems, with multiple layers of computation, memory, and sensing densely integrated over the same starting substrate, truly embodying computation immersed in memory and sensing. This is enabled by the very low processing temperatures (<200°C) of many emerging nanotechnologies (CNFETs for sensors and circuits, and resistive RAM or spin-transfer torque magnetic RAM, for memory). Owing to this monolithic 3-D integration, conventional back-end-of-line inter-layer vias can be used connect vertical layers, which are over 1,000X denser than the through-silicon-vias (TSVs) used with conventional chip-stacking today. We are currently designing, fabricating, and testing monolithic 3-D nanosystem hardware prototypes.



▲ Figure 1: Carbon nanotube field-effect transistor (CNFET).

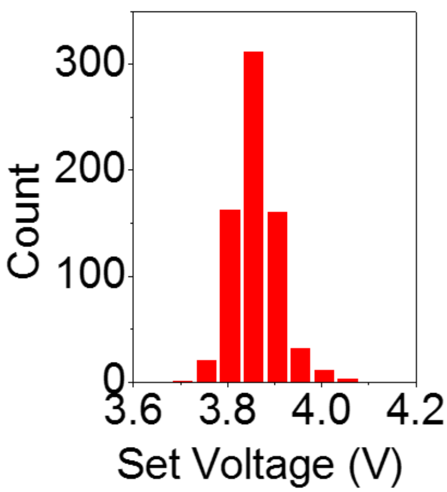


▲ Figure 2: Schematic of a monolithic 3-D IC.

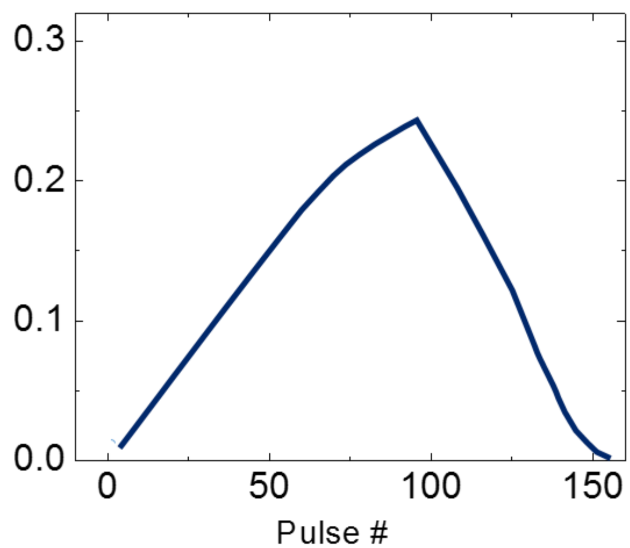
Novel Device Structure for Neuromorphic Computing Array

S. Choi, S. Tan, Y. Kim, J. Kim

Neuromorphic computing has recently emerged as a non-Von Neumann computing method for ultrafast real-time data processing. It utilizes analog switching to represent multiple synaptic weights by varying conductance in the vertical filaments formed in the switching medium, centering around this technology is the memristor which is considered to be a suitable hardware platform for neuromorphic computing. Conventional memristors typically utilize a defective amorphous solid as a switching medium for defect-mediated formation of conducting filaments. However, the imperfection of the switching medium also causes stochastic filament formation, leading to spatial and temporal variation of the devices. Our group proposes a silicon-based epitaxial random access memory (epiRAM), where we precisely confine the conducting paths in the single-crystalline films, resulting in unprecedented device performances. MIT's epiRAM exhibits extremely low temporal/spatial variation, linear synaptic weight update, high on/off ratio, great endurance, long retention time, and self-selectivity. This performance is suitable for large-scale neuromorphic computing hardware. Figure 1 shows cycle-to-cycle set voltage variation for 700 switching cycles, and Figure 2 shows analog behavior of the epiRAM where we obtain linear potentiation and depression.



▲ Figure 1: Cycle-to-cycle variation.



▲ Figure 2: Linear potentiation and depression.

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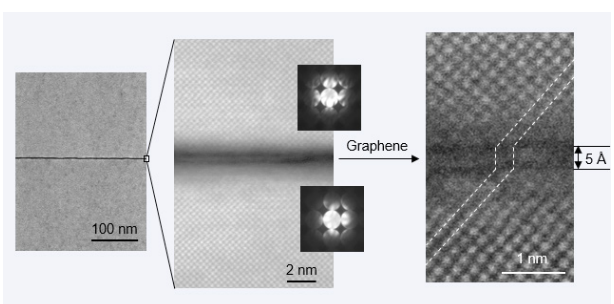
Remote Epitaxy through Graphene for Two-Dimensional Material Based Layer Transfer

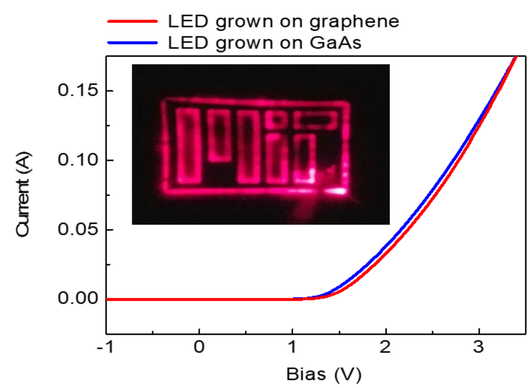
Y. Kim, S. Cruz, K. Lee, K. Qiao, J. Kim
Sponsorship: Masdar Institute of Science and Technology, LG Electronics

Van der Waals epitaxy (vdWE) has gained great interest for crystalline growth as it substantially relaxes the strict lattice matching requirements in conventional heteroepitaxy and allows for facile layer release from the vdW surface. In recent studies, vdWE was investigated on two-dimensional (2D) materials grown or transferred on arbitrary substrates, with the primary notion that the 2D material is the sole epitaxial seed layer in vdWE. However, the underlying substrate may still play a role in determining the orientation of the overlayers since the weak vdW potential field from 2D materials may barely screen the stronger potential field from the substrates.

Here, we reveal that the epitaxial registry of adatoms during epitaxy can be assigned by the underlying substrate remotely through 2D materials by modulating the interaction gap between the substrate and the epilayer. Our study shows that remote epitaxial growth can be performed through a single-atom-thick gap defined by monolayer graphene at the substrate-epilayer interface. Simulations using density functional theory (DFT) prove that remote epitaxy can occur within a ~9 Å substrate-epilayer gap. We experimentally demonstrate successful remote homoepitaxy of GaAs(001) on GaAs(001) substrates through monolayer graphene (Figure 1). The concept is extended for remote epitaxy of other semiconductors such as InP and GaP. The grown single-crystalline films are then rapidly released from the vdW surface of graphene. To prove the functionality of GaAs film grown via remote homoepitaxy, we have successfully grown and fabricated light emitting diodes (LEDs) on graphene/GaAs substrate (Figure 2). This concept, here termed 2D material based layer transfer (2DLT), suggests a method to copy/paste any type of semiconductors films from the underlying substrates through 2D materials then rapidly released and transferred to the substrates of interest. With the potential to reuse graphene-coated substrates, 2DLT will greatly advance non-Si electronics and photonics by displacing the high cost of non-Si substrates.



▲Figure 1: High resolution STEM images showing excellent remote alignment of the (001) GaAs lattices through the graphene. Convergent beam electron diffraction patterns (001) from the epilayer (top) and the substrate (bottom) show identical zinc blend (001) orientations.



▲Figure 2: *I-V* curves of LEDs grown on graphene/GaAs substrates and directly on GaAs. Inset exhibits the emitted red light from the LEDs grown on the graphene/GaAs substrate.

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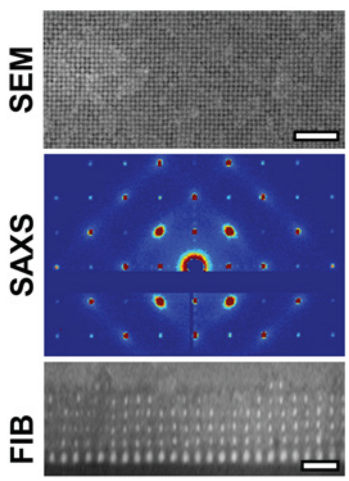
Epitaxy: Programmable Atom Equivalents versus Atoms

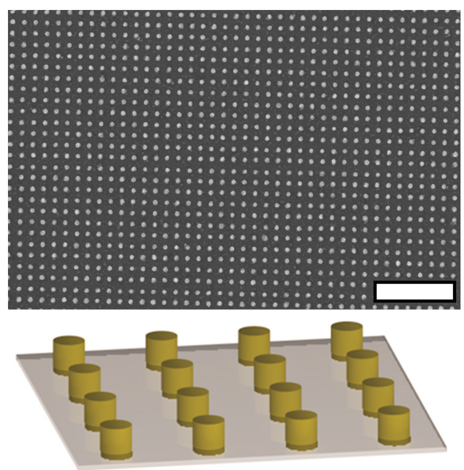
M. X. Wang, S. E. Seo, P. A. Gabrys, D. Fleischman, B. Lee, Y. Kim, H. A. Atwater, R. J. Macfarlane, C. A. Mirkin
Sponsorship: AFOSR, NSF

The programmability of DNA makes it an attractive structure-directing ligand for the assembly of nanoparticle (NP) superlattices in a manner that mimics many aspects of atomic crystallization. These superlattices have potential application as sensors, waveguides, or structural materials due to their unique optical, mechanical, and other physical properties. However, integrating these materials into devices requires complete control over lattice structure and shape, and the synthesis of multilayer single crystals of defined size remains a challenge. Though previous studies considered lattice mismatch as the major limiting factor for multilayer assembly, thin film growth depends on many interlinked variables. In preliminary work in the Macfarlane Laboratory, a more comprehensive approach has been taken to study fundamental elements of assembly, such as the growth temperature and the thermodynamics of interfacial energetics, to achieve epitaxial growth of NP thin films. Under equilibrium conditions, single crystalline, multilayer thin films can be synthesized over 500 × 500 μm^2 areas on lithographically patterned templates (Figure 1), whereas deposition under kinetic conditions leads to the rapid growth of glassy films. Importantly, these superlattices follow the same patterns of crystal growth demonstrated in atomic thin film deposition, allowing these processes to be understood in the context of well-studied atomic epitaxy and enabling a nanoscale model to study fundamental crystallization processes. Through understanding the role of epitaxy as a driving force for NP assembly, we are able to realize 3-D architectures of arbitrary domain geometry and size.

Single-crystal alignment is achieved through the introduction of an epitaxial driving force. Gold posts are patterned on a silicon substrate using conventional electron beam lithography (EBL) techniques and electron beam evaporation. The posts are commensurate in size and shape to the gold NPs utilized and functionalized with DNA. When the posts are positioned to mimic a continuous (100) plane of a body-centered cubic (bcc) superlattice with arbitrary macroscopic shape (Figure 2), the DNA-NPs self-assemble atop the pattern, maintaining epitaxy.



▲ Figure 1: Scanning electron microscopy (SEM), small-angle X-ray scattering, and SEM of cross-section following focused-ion beam (FIB) milling of a 10-layer DNA-NP epitaxial thin film. Scale bars for SEM and FIB are 500 and 200 nm, respectively.



▲ Figure 2: Schematic of substrate patterned by EBL. Gold posts are designed to mimic the size, shape, and placement of the DNA-NP gold cores in the (100) plane of a bcc arrangement.

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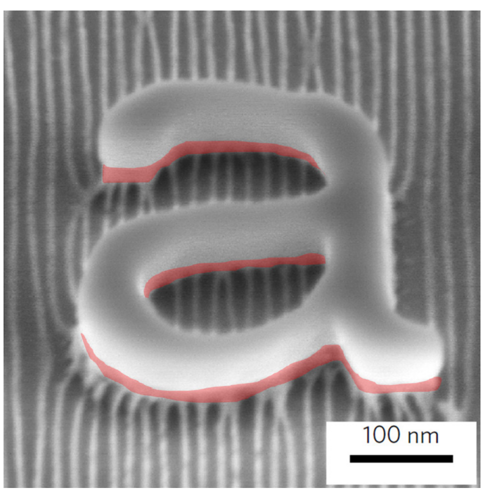
Sub-10-nm Patterning via Self-Assembled Block Copolymer and Vapor-Phase Deposited Topcoat

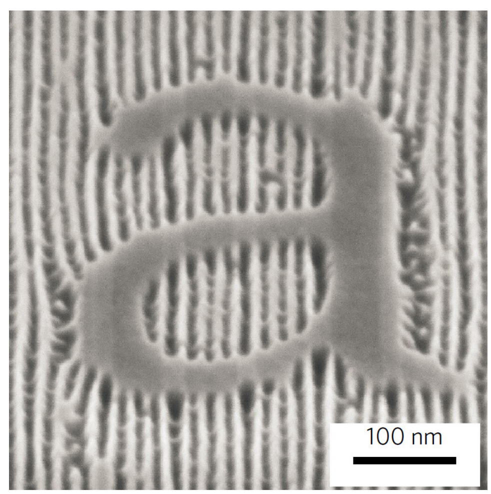
D. H. Kim, H. S. Suh, P. Moni, S. Xiong, L. E. Ocola, N. J. Zaluzec, K. K. Gleason, P. F. Nealey
Sponsorship: NSF

The semiconductor industry has made a great effort to produce sub-10-nm patterns in a cost-effective way as the feature size is getting close to the limit of the wavelength of the UV light source in current photolithography. As an enabling technology, block copolymers (BCP) can be self-assembled to nanoscale structures by thermal anneal with no UV light. In particular, for sub-10 nm patterning, we developed a new technology employing directed self-assembly (DSA) of highly segregating BCP and a topcoat deposited by initiated chemical vapor deposition (iCVD). iCVD, a dry process, enabled the deposition of a crosslinked polymeric topcoat on the BCP films without any damage to the BCP films. We here discovered that the iCVD made a unique interface between the BCP films and topcoat through grafting intrinsically. The interface achieves a non-preferential surface for domains of the multiple BCPs, thereby resulting in the desirable perpendicular orientation of the BCP domains. In addition, because the crosslinked topcoat is chemically durable against solvents of e-beam resist, we could fabricate additional topcoat patterns on the BCP films by e-beam lithography. The post-patterning enabled by iCVD permits positioning of a sub-10-nm patterning area on a Si wafer, which is more beneficial to the interconnect devices in the semiconductor industry.

Figure 1 shows sub-10-nm line-and-space patterns behind a micron size letter pattern, "a," after DSA and dry etching. Figure 1 confirms that the patterned iCVD topcoat (red) beneath the e-beam resist pattern is holding a sub-10-nm domain, achieving dual-scale patterns. Then, we successfully transferred the patterns to a Si wafer by a dry etching process as seen in Figure 2. As the iCVD process can be readily scaled up to a larger area, we anticipate that iCVD topcoats will enable the widespread implementation of DSA in nanomanufacturing to create sub-10-nm scale patterns.



▲ Figure 1: Scanning electron microscopic (SEM) images of dual-scale alumina patterns with vapor phased topcoat (red) beneath e-beam resist. The topcoat assists the perpendicular orientation of BCP domains, thereby creating sub-10-nm line-and-space patterns behind a micro-size letter pattern.



▲ Figure 2: SEM images of Si patterns after transferring with the mask in Figure 1.

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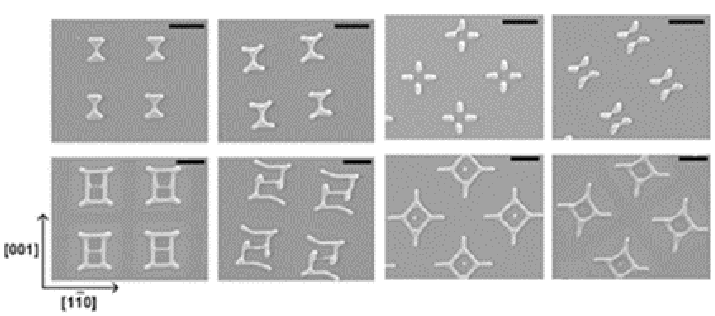
Experimental Characterization and Modeling of Templated Solid-State Dewetting of Thin Single-Crystal Ni Films

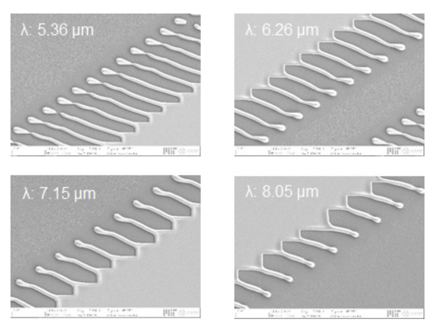
Y. A. Shin, G. H. Kim, S. Jahangir, R. V. Zucker, J. Ye, W. Ma, B. Yildiz, W. C. Carter, C. V. Thompson
Sponsorship: NSF

Templated solid-state dewetting provides a simple method for film patterning to form complex structures (Figure 1). The patterns that result from solid state dewetting are affected by various instabilities that develop at retracting edges and the features they lead to. These include pinch-off to form wires parallel to retracting film edges, instabilities at corners in retracting edges ("corner instabilities"), and Rayleigh-like instabilities that lead to break up of wire-like features. Previously we reported on the strong effects of crystalline anisotropy on the Rayleigh-like instability and identified factors that stabilize wire-like features. In the past year, we reported on experimental characterization and modeling of the corner instability and established the conditions that lead to the development of the unstable edge retraction when corners are present in film edges. We also characterized the effects of the annealing ambient on anisotropy in the rate of edge retraction and consequent changes in the patterns that form as a result of dewetting. We found that changing the gases and gas flow rates during annealing causes surface reconstructions that affect the anisotropy of the energy of the surfaces of the films and the anisotropy of surface diffusion. Control of the ambient gas during annealing provides an additional means of controlling the types of patterns that result from simple templating.

We are currently focusing on a fingering instability that can occur during edge retraction and results in formation of parallel wire-like features with different orientations from those that develop as a result of rim-pinch-off (Figure 2). Understanding and controlling whether pinch-off or fingering occurs is important for development of techniques for controlled pattern formation. When fingering occurs, it is also desirable to control the size and spacing of wires that form. In the past year, we have demonstrated that the initial roughness of a film edge determines whether pinch-off or fingering occurs, with rough edges leading to fingering. To further understand this phenomenon and to control it, we have used edges with controlled patterned roughness to template the fingering instability. We have found that the spacing of wires formed due to fingering can be controlled by the period of the patterned roughness. We have also found that controlling the period of the fingering process affects the kinetics of the fingering. Our ability to control the fingering process allows us to develop kinetic models that can be used to design templates that will lead to specific complex structures during solid-state dewetting. Through these studies, we are developing a suite of methods that can be used to suppress dewetting when it is undesirable and to control it for use in pattern formation.



▲ Figure 1: Patterns formed by solid state dewetting of square patches of Ni films patterned with different sizes and crystallographic orientations.



▲ Figure 2: Wires formed by templating a fingering instability using patterned periodic edge roughness.

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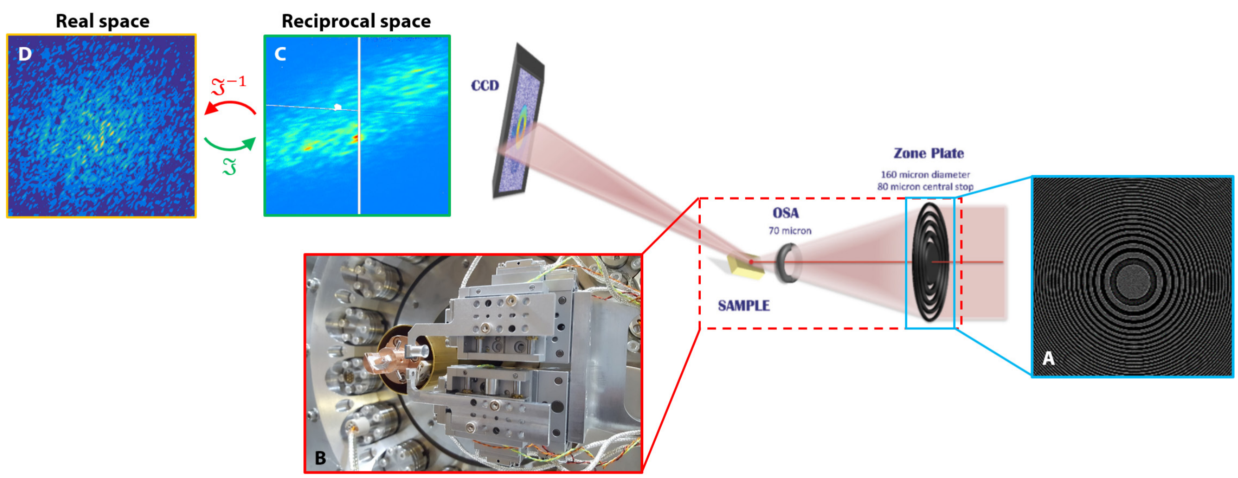
Coherent Soft X-Ray Diffractive Imaging of Magnetic Nanotextures

J. Li, J. Pelliciari, R. Comin
Sponsorship: MIT Startup Funds

The ability to image the nanoscale structure of materials with tunable magnetic textures is pivotal for the development of low-power and nonvolatile data storage technologies. Soft X-ray imaging has emerged in the last decade as a powerful and accurate methodology to resolve the bulk domain structure of several magnetic materials—magnetic multilayers, buried interfaces, or skyrmion lattices—as well as nanoelectronic devices under operating conditions.

Soft X-ray imaging relies on two main requirements: (i) the ability to focus a collimated X-ray beam on a spot the size of a few tens of nm and (ii) the development of algorithms capable of inverting the information in reciprocal space (diffraction pattern) back to real space. We have recently commissioned a new soft X-ray nanofocusing setup installed at beamline CSX-1 of the National Synchrotron Light Source II. The schematics of this setup are shown in Figure 1. A key element is the Fresnel zone plate (Figure 1a), fabricated at MTL, which acts as a diffractive phase mask to focus X-rays to a 70-nm spot at the sample. The beam spot can be moved with the aid of piezo-based nanopositioners (Figure 1b), which translate the X-ray optics while keeping the sample in a fixed position. Diffracted X-rays are collected with a CCD camera in the far field (~30 cm from the sample). The resulting speckle pattern (Figure 1c) encodes the information on the nanoscale magnetic texture in reciprocal (Fourier) space and can be acquired in less than a second. By Fourier-inverting back onto real space, we can unveil the domain structure in real space with an ultimate accuracy of 10-20 nm (Figure 1d).

We plan to apply this new method to the study of magnetic materials in their pure state (single crystal or thin films) as well as in a device configuration, where the use of a contactless probe enables the study of the material or device response *in operando*. Our future focus is on transition metal- and rare-earth-based compounds, particularly those exhibiting antiferromagnetic order, which can be switched on very fast (picosecond) timescales.



▲ Figure 1: Coherent soft X-ray diffraction setup at the National Synchrotron Light Source II. Main panel: schematics of the X-ray optics used in coherent diffraction; a Fresnel zone plate (fabricated at MTL; SEM image in (a) focuses X-rays down to a ~70- nm spot at the sample position; diffracted X-rays are imaged with a CCD camera, (b) inside view of the diffraction chamber, with piezo-actuated nanopositioners located upstream of the sample stage (copper), (c & d) example of speckle pattern (c) from antiferromagnetic domain structure of a $NdNiO_3$ thin film, and corresponding reconstructed domain pattern in real space (d). C and d are related by a Fourier transform.

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Information Limit of Domain-Wall-Based Nanowire Devices

S. A. Siddiqui, S. Dutta, C. A. Ross, M. A. Baldo
Sponsorship: NSF

Spintronic and magnetic devices use the spin of electrons instead of their charge to implement ultra-low-power logic and memory applications. In domain-wall-based magnetic devices, charge or spin currents move the boundary between different magnetic domains in a nanowire. Rather than flipping the orientation of the entire wire at once, this incremental approach improves the energy efficiency. Domain walls, however, can be pinned by the line edge roughness of nanowires, affecting the operation of the devices. Notches created by edge roughness comparable to the width of domain walls have been identified as the most effective pinning sites for domain walls, although the precise relation between the line edge roughness and domain wall pinning sites is unknown. Here, we show the autocorrelation of pinning sites with the line edge roughness in sub-100-nm-wide Co-wires. We have shown both experimentally and with simulation that the correlation length of edge roughness defines the effective pinning site distribution for domain walls in individual nanowires. If we apply a self-affine model for the intrinsic roughness of fabricated edges, our result identifies the limit for information density in magnetic nanowires used in both domain-wall-based logic and memory devices.

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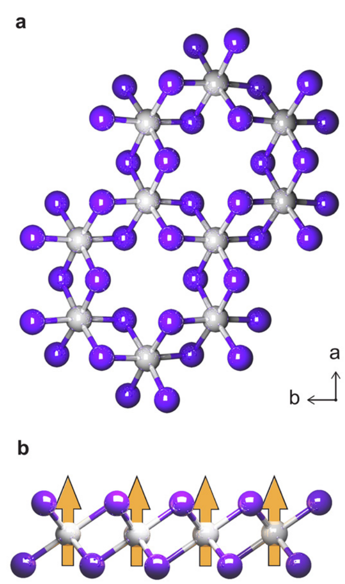
Layer-Dependent Ferromagnetism in a van der Waals Crystal Down to the Monolayer Limit

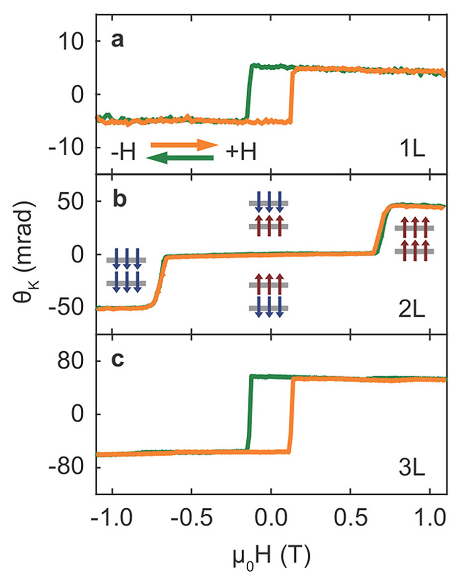
D. R. Klein, E. Navarro-Moratalla, B. Huang, G. Clark, R. Cheng, K. Seyler, D. Zong, E. Schmidgall, M. A. McGuire, D. H. Cobden, W. Yao, D. Xiao, P. Jarillo-Herrero, X. Xu
Sponsorship: NSF, U. S. Department of Energy, Gordon and Betty Moore Foundation

Since the discovery of graphene just over a decade ago, the field of 2D materials has expanded to include a broad range of materials including conductors, insulators, semiconductors, and superconductors. Surprisingly, no intrinsic magnets made it into the 2D materials family until just very recently. In a study published in *Nature*, our group along with collaborators at the University of Washington have, for the first time, experimentally demonstrated long-range ferromagnetic order in an atomically-thin crystal, chromium triiodide (CrI_3), down to the monolayer limit (crystal structure shown in Figure 1). This is the first ferromagnet in the family of 2D materials. In the same way, in which graphene permitted studying the transport of electrons in a true 2D lattice, monolayer CrI_3 opens the door for the study of magnetism in the true 2D limit.

We first cleave bulk crystals of CrI_3 down to few-layer flakes, including monolayer flakes just one unit cell (three atoms) thick. Then, we probe the materials using magneto-optical Kerr effect (MOKE) spectroscopy, which reveals the out-of-plane magnetization of the field. We reveal a dramatic dependence of the magnetic ground states on the number of layers in a CrI_3 crystal. First, we observe 2D Ising ferromagnetic behavior of the monolayer below its Curie temperature of 45 K (Figure 2). Moreover, bilayer CrI_3 crystals exhibit antiferromagnetism, which can be explained by the two layers of the crystal containing opposite spins that cancel each other out to reveal a net zero magnetization. By just adding one additional layer to bilayer CrI_3, one recovers a strong out-of-plane magnetization in the trilayer crystal as the interlayer coupling constant switches sign. Our results pave the way for further studies of interfacing 2D CrI_3 with other atomically-thin materials in van der Waals heterostructures, which could revolutionize technologies in magnetoelectronics, information, and spin-based data storage.



▲ Figure 1: Crystal structure of CrI_3 as viewed along the (a) **c**-axis (top-down) and (b) **a**-axis (in-plane). Cr^{3+} and I^- ions are displayed in white and purple, respectively.



▲ Figure 2: Polar MOKE signals of (a) mono-layer, (b) bilayer, and (c) trilayer flakes of CrI_3 as a function of applied magnetic field.

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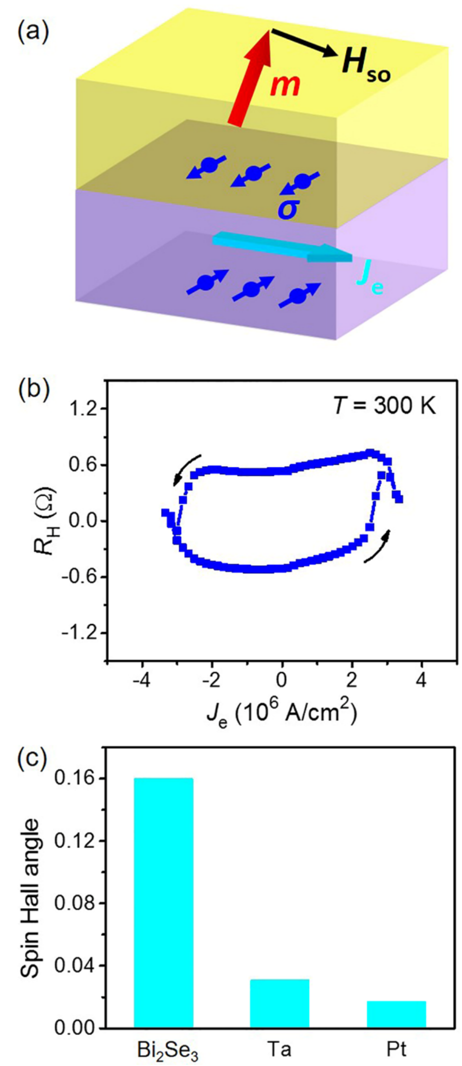
Room Temperature Spin-Orbit Torque Switching Induced by a Topological Insulator

J. Han, S.A. Siddiqui, J. Finley, L. Liu, A. Richardella, N. Samarth
Sponsorship: NSF

Recent studies on the topological insulators (TI) have attracted great attention due to the rich spin-orbit physics and promising applications in spintronic devices. In particular, the strongly spin-moment coupled electronic states have been extensively pursued to realize efficient spin-orbit torque (SOT) switching. However, so far current-induced magnetic switching with TI has been observed only at cryogenic temperatures. Whether the topologically protected electronic states in TI could benefit from spintronic applications at room temperature remains a controversial issue.

In this work, we report SOT switching in a TI/ferromagnet heterostructure with perpendicular magnetic anisotropy (PMA) at room temperature. Ferrimagnetic cobalt-terbium (CoTb) alloy with robust bulk PMA is directly grown on a classical TI material, Bi_2Se_3. The low switching current density provides definitive proof of the high SOT efficiency from TI and suggests the topological spin-momentum locking in TI even if it is neighbored by a strong ferromagnet. Furthermore, the effective spin Hall angle of TI is determined to be several times larger than commonly used heavy metals. Our results demonstrate the robustness of TI as an SOT switching material and provide an avenue towards applicable TI-based spintronic devices.



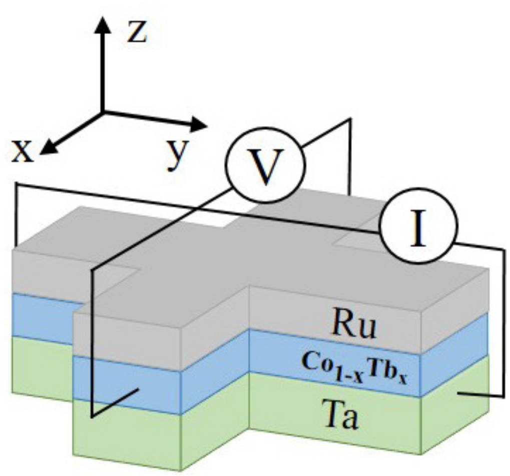
▲ Figure 1: (a) Schematic of SOT in Bi2Se3/CoTb heterostructure. (b) Room temperature SOT switching in Bi2Se3/CoTb. Hall resistance is measured when sweeping a direct current (DC) under a bias magnetic field along the current direction. (c) Absolute values of the effective spin Hall angles of Bi2Se3, Pt, and Ta measured by our experiments.

Spin-Orbit Torque in Compensated Ferrimagnetic Cobalt-Terbium Alloys

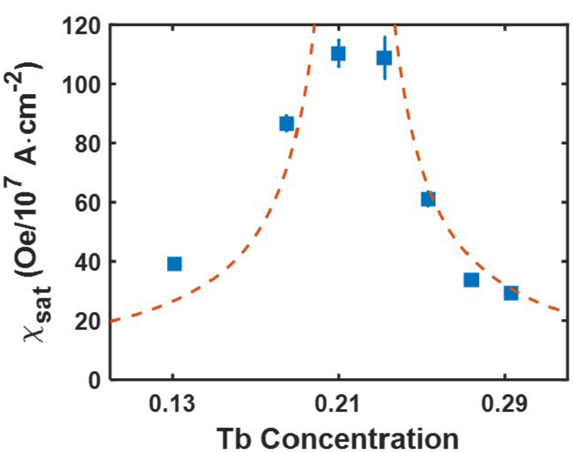
J. Finley, L. Liu
Sponsorship: NSF, SRC

Spintronic devices promise to be an energy-efficient alternative to complementary metal-oxide semiconductor devices for logic and memory. However, in order to be more competitive, further reductions in switching energy and switching speed are needed. There has been great interest recently in using antiferromagnetically coupled materials as opposed to ferromagnetic materials to store information. Compared with ferromagnetic materials, antiferromagnetically coupled systems exhibit fast dynamics as well as immunities against perturbations from external magnetic fields, potentially enabling spintronic devices with higher speed and density. Despite the potential advantages of information storage in antiferromagnetically coupled materials, it remains unclear whether one can control the magnetic moment orientation efficiently because of the canceled magnetic moment.

Here, we report spin-orbit torque induced magnetization switching of ferromagnetic $Co_{1-x}Tb_x$ thin films (Figure 1). By varying the relative concentrations of the two atomic species, one can reach compensation points where the net magnetic moment or angular momentum goes to zero. We demonstrate current induced switching in all of the studied film compositions, including those near the magnetization compensation point. We then quantify the spin-orbit torque induced effective magnetic field, where we find that close to the compensation point, there is a divergent behavior that scales with the inverse of magnetization (Figure 2), which is consistent with the conservation of angular momentum. Moreover, we also quantified the Dzyaloshinskii-Moriya interaction (DMI) energy in the $Ta/Co_{1-x}Tb_x$ system, and we found that the energy density increases as a function of the Tb concentration. This tunable DMI could be potentially useful for spintronic applications that employ stable magnetic textures for information storage. The large effective spin-orbit torque, the previously demonstrated fast dynamics, and the minimal net magnetization in these ferrimagnetic systems promise spintronic devices that are faster and more scalable than traditional ferromagnetic systems.



▲ Figure 1: Schematic of the film stack and Hall bar device geometry. A ferrimagnetic $Co_{1-x}Tb_x$ layer is sandwiched between the Ta spin-torque generating layer and a Ru capping layer.



▲ Figure 2: Saturation efficiency χ_{sat}, which is proportional to the spin-orbit torque effective magnetic field, for different $Co_{1-x}Tb_x$ films. The saturation efficiency is largest near the magnetic moment compensation point.

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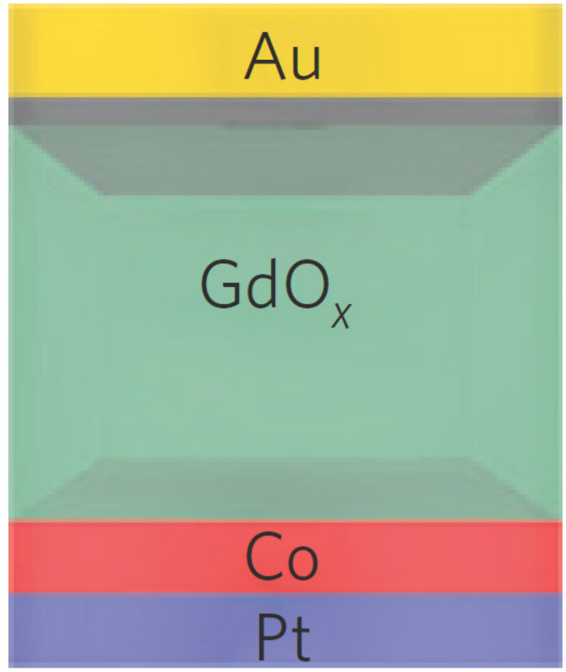
Research on CMOS-Compatible High-K Dielectrics for Magneto-Ionic Memory

S. Kim, H. L. Tuller, in collaboration with A. J. Tan, G. S. Beach
Sponsorship: CMSE, Interdisciplinary Research Groups, NSF

High-k dielectrics play a key role in modern microelectronic circuitry, given their ability to provide reduced leakage currents while providing adequate capacitance in ever smaller nano-dimensioned metal-oxide semiconductor field-effect transistor (MOSFET) devices. Recently, the Beach group at MIT demonstrated the ability to modulate the magnetic properties of transition metal thin-films by electrical bias across thin-films of Gd_2O_3 (Figure 1). The reversible switching was demonstrated to be assisted by the electro-migration of oxygen ions to and away from the transition metal/Gd_2O_3 interface. This novel process, now called "magneto-ionic control," creates new opportunities for nonvolatile information storage.

Previous research showed that the device's operation depends on the thickness of the dielectric layer, its interaction with the ambient atmosphere, and the device's temperature. These dependencies suggest that this magneto-ionic device is an electrochemical device operating via interfacial reaction, migration, and diffusion. However, questions remain about the origins of its mechanisms. In this study, we intend to establish a strategy for enhancing the performance of the device by investigating the underlying operating mechanisms; we ultimately hope to test the potential of this novel device in memory applications. To understand the diffusion in the oxide layer, we have undertaken a detailed examination of the properties of Gd_2O_3, a model oxide, and related oxides as well as investigated device design to implement studies with controlled parameters.



▲ Figure 1: Structure of magneto-ionic device.

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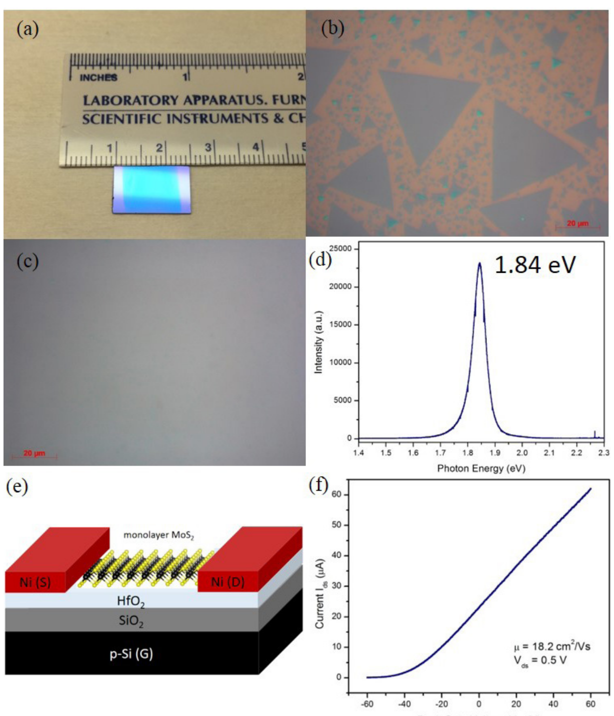
CVD Growth of High-Quality Transition Metal Dichalcogenide Monolayers and their Intrinsic Electronic Transport Properties

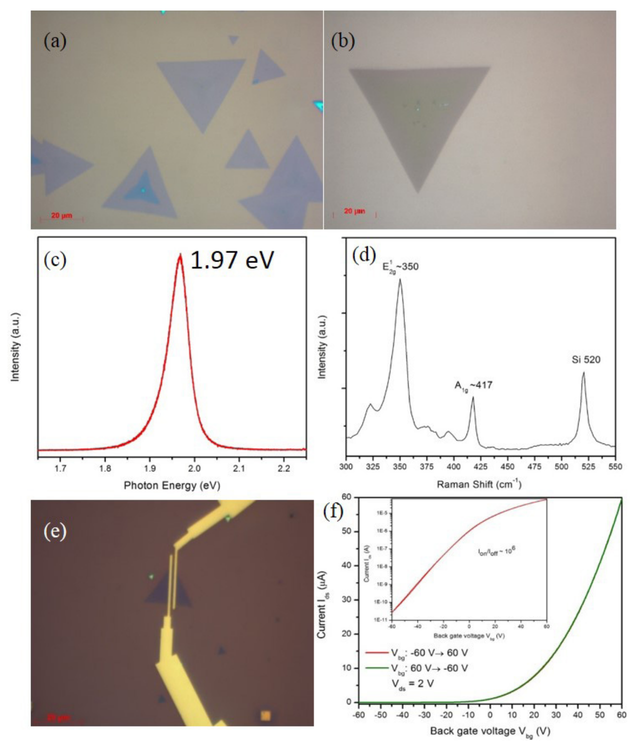
P.-C. Shen, J. Kong
Sponsorship: NSF E3S

Monolayer transition metal dichalcogenides (TMDs) such as molybdenum disulfide (MoS_2) and tungsten disulfide (WS_2) have been attractive for use in ultra-scaled electronic and optoelectronic devices because of their atomically thin thicknesses, direct band gaps, and strong spin-orbit interactions. Technologies for the mass-production of high-quality, large-area, and atomically thin TMD films or single-crystal grains are highly needed in order to bring them to practical applications. Our group has developed reliable methods for growing high-quality monolayer MoS_2 and WS_2 via chemical vapor deposition (CVD) and investigated their intrinsic and high-k dielectrics enhanced electrical transport properties for device applications. Our group has also focused on defect characterization of TMDs.

Figure 1 shows the photo and optical images of the as-grown monolayer MoS_2 films and single-crystal domains. The continuous area of the MoS_2 thin films grown in this work is typically ~ 1 cm x 1 cm. The triangular domain of MoS_2 single crystals can be found at the edges of the continuous region with a side length as large as ~ 60 µm. Our CVD-grown MoS_2 films show a PL to Raman peak intensity ratio as high as ~ 100 and a full-width-half-maximum as small as ~ 55 meV, suggesting an excellent optical quality. The peak room-temperature field-effect mobility of MoS_2 reaches ~ 18 $cm^2\,V^{-1}\,S^{-1}$. On the other hand, Figure 2 presents the optical images and electrical transport properties of the CVD-grown WS_2 monolayers. The as-grown WS_2 exhibits n-type semiconducting behavior with a direct band gap at 1.97 eV and a field-effect mobility of ~ 7 $cm^2\,V^{-1}\,S^{-1}$.



▲ Figure 1: (a) Photo of centimeter-scale monolayer MoS_2 grown on SiO_2/Si wafer. (b) Optical images of CVD-grown triangular domains and (c) completely continuous film of MoS_2. (d) Room temperature PL of MoS_2 films. (e) Schematic of back-gated MoS_2 FET using HfO_2/SiO_2 hybrid gate dielectric and Ni electrodes. (f) Transport properties of single-layer MoS_2 field-effect transmitters (FETs).



▲ Figure 2: (a) Optical images of as-grown monolayer WS_2 grains. (b) Triangular domain of WS_2 with ~ 65-µm side length. (c) Typical PL and (d) Raman spectra of as-grown WS_2 monolayers. (e) Optical micrograph of typical Ni/WS_2/SiO_2/Si FET. (f) Transfer characteristics of back-gated WS_2 transistor with Ni contacts. (scale bars: 20 µm).

High Speed Roll-to-Roll Production of Atomically Thin (2D) Materials Using a Split Zone CVD Reactor

P. R. Kidambi, D. Mariappan, A. Vyatskikh, M. Feldmann, A. J. Hart
Sponsorship: MIT Energy Initiative, U. S. Department of Energy

Large-area applications of 2D materials such as membranes and barrier films require a means of cost-effective roll-to-roll manufacturing. We have designed and assembled a split zone CVD reactor for roll-to-roll synthesis of 2D materials by chemical vapor deposition (CVD). The reactor configuration consists of an annealing and growth zone separated by a narrow slit through which the catalytic flexible metallic substrate (foil) passes from one end of the reactor to the other. The design of this system was guided by flow simulations. Using the system constructed in our laboratory, we demonstrate synthesis of uniform, high quality graphene at speeds up to 500 mm/min, specifically for membrane and barrier applications. A detailed investigation into the process parameters that influence the growth of graphene on a moving substrate allows us to identify process optimization techniques for roll-to-roll synthesis and subsequent processing for manufacturing of films with tailored nanoscale porosity. We reflect on the scalability of this process and general principles for roll-to-roll CVD of other 2D materials.

▲ Figure 1: Split zone CVD reactor for roll to roll production of 2D materials.

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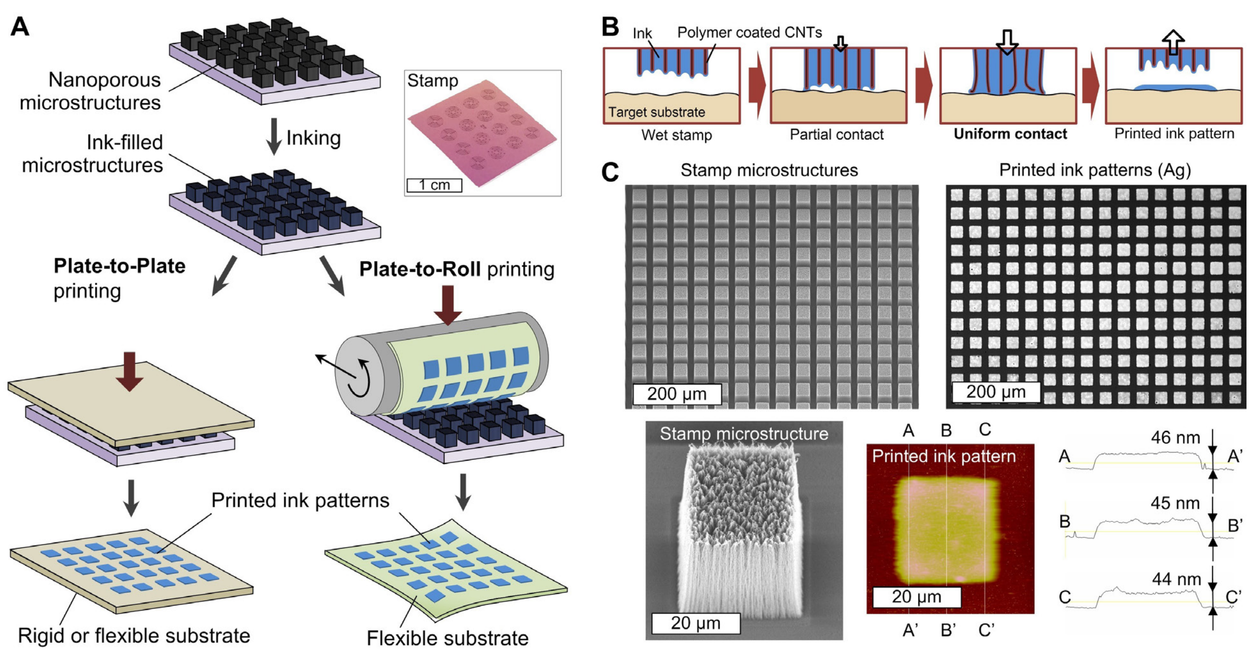
Ultrathin High-Resolution Flexographic Printing Using Nanoporous Stamps

S. Kim, H. Sojoudi, H. Zhao, D. Mariappan, G. H. McKinley, K. K. Gleason, A. J. Hart
Sponsorship: MIT Department of Mechanical Engineering, NSF, AFOSR

Since its invention in ancient times, relief printing, commonly called flexography, has been used to mass-produce artifacts ranging from decorative graphics to printed media. At present, higher resolution flexography is essential to the manufacturing of low-cost, large-area printed electronics. However, due to contact-mediated liquid instabilities and spreading, the resolution of flexographic printing using elastomeric stamps is limited to 50-100 µm. Here, we introduce engineered nanoporous microstructures as a next-generation stamp material, comprising polymer-coated aligned carbon nanotubes (CNTs). We design and engineer the highly porous CNT microstructures to be wetted by colloidal inks and to transfer a thin layer to a target substrate upon brief mechanical contact. We demonstrate printing of diverse micron-scale patterns of a variety of functional nanoparticle inks, including Ag, ZnO, WO_3, and CdSe/ZnS, onto both rigid and compliant substrates. The printed patterns have highly uniform nanoscale thickness (5-50 nm) and match the stamp features with high fidelity (edge roughness ~0.2 µm). We derive conditions for uniform printing based on nanoscale contact mechanics, characterize high-conductivity printed Ag lines and transparent conductors after thermal annealing, and achieve continuous printing at a speed of 0.2 m/s. The latter represents a combination of resolution and throughput that far surpasses industrial printing technologies.



▲ Figure 1: Direct printing of ultrathin colloidal ink patterns using microstructured nanoporous stamps. Schematics of the printing procedure (a) and the uniform transfer of ink (b) from the nanoporous stamp to the target substrate surface via conformal contact, (c) scanning electrode microscopy image of stamp features comprising an array of squares (side length, 25 µm), along with corresponding optical and atomic force microscopy images of the resulting printed Ag ink (particle size, <10 nm; 50-60 weight % in tetradecane) patterns.

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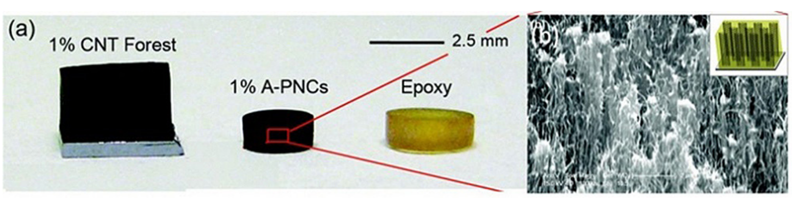
Aligned CNT-Based Microstructures and Nanoengineered Composite Macrostructures

B. L. Wardle, E. Cohen, H. Cornwell, N. Fritz, Y. Gao, R. Kopp, J. Lee, R. Li, D. Lidston, X. Ni, I. Stein
Sponsorship: MIT NECST Consortium, NSF, AFOSR, AFRL, ONR, ISN, NASA NSTRT, NDSEG, NSF Fellowships

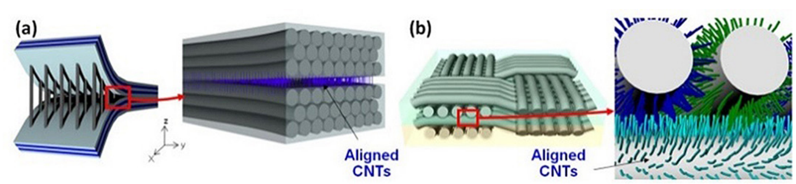
Materials comprising carbon nanotubes (CNTs), such as hierarchical nanoengineered advanced composites for aerospace applications, are promising new materials thanks to their mechanical and multifunctional properties. We have undertaken a significant experimentally based program to understand both microstructures of aligned-CNT nanocomposites and hierarchical nanoengineered advanced composites macrostructures hybridized with aligned CNTs.

Aligned nanocomposites are fabricated by mechanical densification and polymer wetting of aligned CNT forests. Here the polymer is typically an unmodified aerospace-grade epoxy. CNT forests are grown to mm-heights on 1-cm^2 Si substrates using a modified chemical vapor deposition process. Following growth, the forests are released from the substrate and can be handled and infiltrated. The volume fraction of the as-grown CNT forests is about 1%; however, the distance between the CNTs (and thus the volume fraction of the forest) can be varied by applying a compressive force along the two axes of the plane of the forest to give volume fractions of CNTs exceeding 20% (see Figure 1a). Variable-volume fraction-aligned CNT nanocomposites were characterized using optical, scanning electron (SEM), transmission electron (TEM) microscopy, 3-D TEM, and X-ray computed tomography (CT) to analyze dispersion and alignment of CNTs as well as overall morphology. Extensive mechanical property testing and modeling are underway, including 3-D constitutive relations and fracture toughness.

Nanoengineered hierarchical composites hybridized with aligned CNTs are prepared by placing long (>20 µm) aligned CNTs at the interface of advanced composite plies as reinforcement in the through-thickness axis of the laminate (see Figure 2). Three fabrication routes were developed: transplantation of CNT forests onto pre-impregnated plies ("nanostitching"), placement of detached CNT forests between two fabrics followed by subsequent infusion of matrix, and *in-situ* growth of aligned CNTs onto the surface of ceramic fibers followed by infusion or hand-layup. Aligned CNTs are observed at the composite ply interfaces and give rise to significant improvement in interlaminar strength, toughness, and electrical properties. Extensions of the CNT-based architectures to ceramic-matrix nanocomposites and towards multifunctional capabilities are being developed, including structural health monitoring and deicing.



◀ Figure 1. Controlled-morphology polymer nanocomposites: (a) Image of 1% aligned-CNT forest, 1% A-PNCs and pure epoxy samples, (b) SEM image of 1% A-PNCs with an inset schematic of the CNT alignment direction.



◀ Figure 2: Aligned-CNT nano-engineered composite macro-scale architectures, (a) nanostitching and (b) fuzzy fiber.

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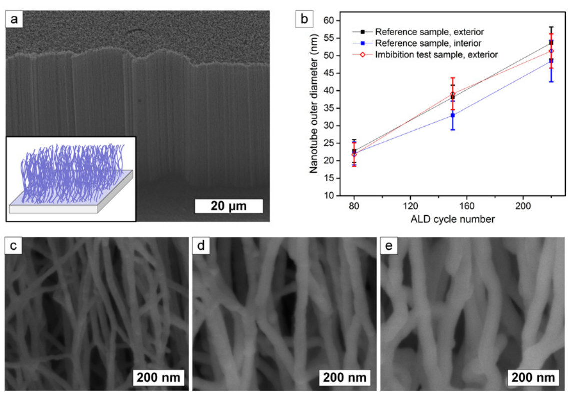
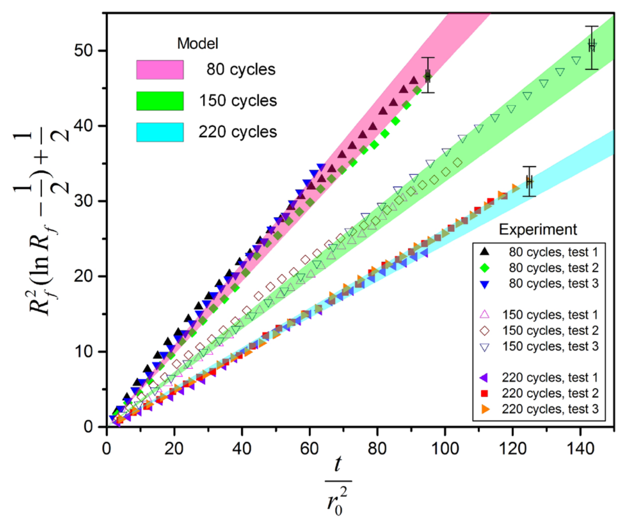
Liquid Imbibition in Ceramic-Coated Carbon Nanotube Films

H. Zhao, C. Jacob, H. A. Stone, A. J. Hart
Sponsorship: AFOSR, MITEI

Understanding of the liquid imbibition dynamics in nanoporous materials is important to advances in chemical separations, phase change heat transfer, electrochemical energy storage, and diagnostic assays. We study the liquid imbibition behavior on films of ceramic-coated vertically aligned carbon nanotubes (CNTs). The nanoscale porosity of the films is tuned by conformal ceramic coating via atomic layer deposition (ALD) as shown in Figure 1, enabling stable liquid imbibition and precise measurement of the imbibition dynamics without capillary densification of the CNTs. We show that the imbibition rate decreases as the ceramic coating thickness increases, which effectively changes the CNT-CNT spacing and therefore decreases the permeability. We derive a Darcy's law-based model that incorporates an expression for the permeability of nanoscale post arrays and show that the model fits the experimental results with high accuracy (Figure 2). The tailorable porosity, along with controllable surface wettability and mechanical stability of coated CNTs, suggests their suitability for application-guided engineering and for further investigation of imbibition behavior at finer length scales.



▲ Figure 1: (a) Scanning electron microscopic (SEM) image of an Al_2O_3-coated CNT forest. (b) Outer diameters of Al_2O_3-CNTs as a function of the ALD cycle number. (c-e) SEM images of CNT forests coated with 80, 150, and 220 ALD cycles of Al_2O_3.



▲ Figure 2: Comparison of model and experiments of liquid imbibition on a 57-μm-tall Al_2O_3-CNT forest, with fitted pitch value p = 78 nm.

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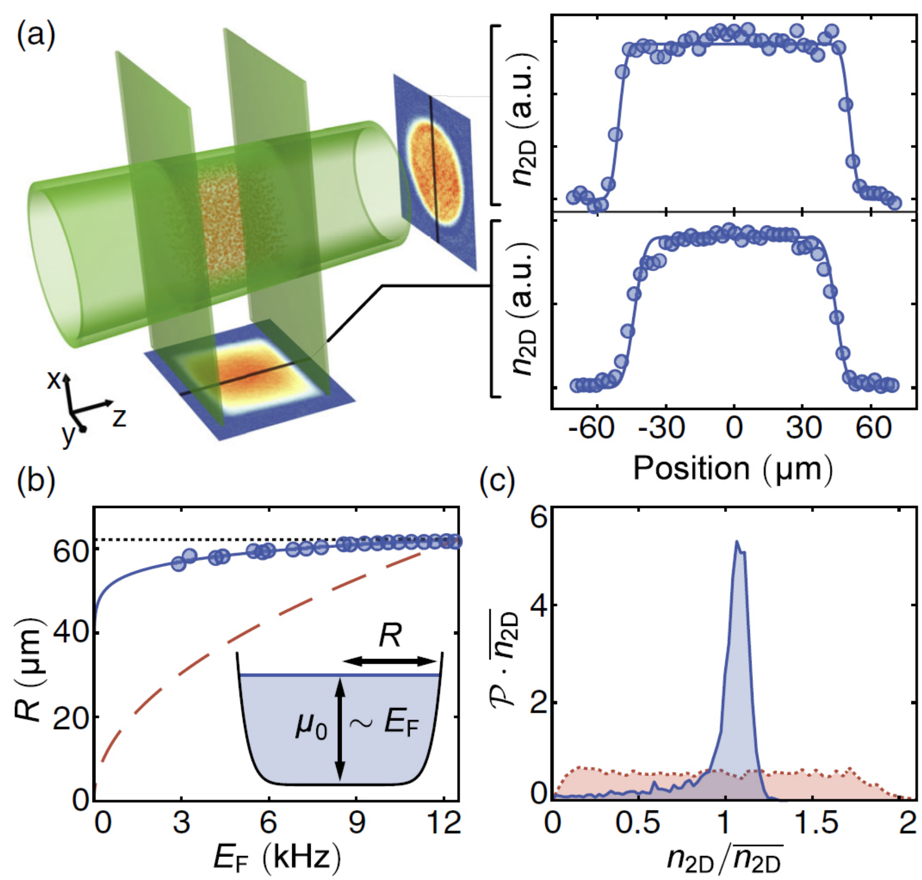
Homogeneous Atomic Fermi Gases

B. Mukherjee, Z. Yan, P. B. Patel, Z. Hadzibabic, T. Yefsah, J. Struck, M. W. Zwierlein
Sponsorship: NSF, ARO, AFOSR, Packard Foundation

We report on the creation of homogeneous Fermi gases of ultracold atoms in a uniform potential. In the momentum distribution of a spin-polarized gas, we observe the emergence of the Fermi surface and the saturated occupation of one particle per momentum state: the striking consequence of Pauli blocking in momentum space for a degenerate gas. Cooling a spin-balanced Fermi gas at unitarity, we create homogeneous superfluids and observe spatially uniform pair condensates. For thermodynamic measurements, we introduce a hybrid potential that is harmonic in one dimension and uniform in the other two. The spatially resolved compressibility reveals the superfluid transition in a spin-balanced Fermi gas, saturation in a fully polarized Fermi gas, and strong attraction in the polaronic regime of a partially polarized Fermi gas.



▲ Figure 1: Homogeneous Fermi gas. (a) Schematic of box trap and cuts through column-integrated density profiles along axial and radial directions. (b) Radius of cloud as function of Fermi energy. Dotted black and dashed red lines correspond to perfect box potential and harmonic potential, respectively, and are scaled to converge at highest E_F. Blue solid line corresponds to power law potential $V(r) \sim r^{16}$. (c) Measured radial probability density $P(n_{2D})$ for column integrated density n_{2D}, averaging about 20 in-trap images. Blue solid and red dashed lines correspond to uniform and gaussian traps, respectively.

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Photonics and Optoelectronics

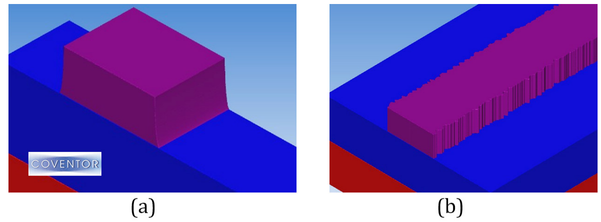
Design for Manufacturability (DFM) Models, Methods, and Tools for Silicon Photonics

S. I. El-Henawy, G. Martinez, D. Moon, M. B. McIlrath, D. S. Boning
Sponsorship: AIM Photonics

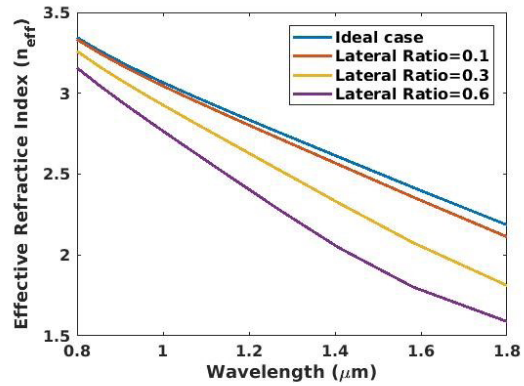
Silicon photonics, where photons instead of electrons are manipulated, shows promise for higher data rates, lower energy communication and information processing, biomedical sensing, Lab-On-A-Chip, and novel optically based functionality applications such as wavefront engineering and beam steering of light. In silicon photonics, both electrical and optical components can be integrated on the same chip, using a shared silicon integrated circuit (IC) technology base. However, silicon photonics does not yet have mature process, device, and circuit variation models for the existing IC and photonic process steps; this lack presents a key challenge for design in this emerging industry.

Our goal is to develop key elements of a robust design for manufacturability (DFM) methodology for silicon photonics. This design includes using statistical modelling to capture manufacturing variations, both systematic and random, at the wafer, chip, or feature scales and predicting their impact on photonic device and circuit levels. These variation-aware models and methods will help enable tomorrow's silicon photonics designers to predict and optimize behavior, performance, and yield of complex silicon photonic devices and circuits, just as IC designers do today.

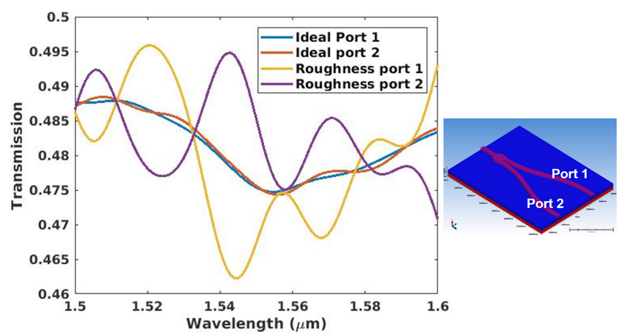
To achieve this goal, we model the process variation effects, such as side wall verticality and edge roughness (Figure 1), on the optical behavior represented in the refractive index (Figure 2) or transmitted power variation in a splitter device (Figure 3). Also, we carry out Monte Carlo simulations in which the geometric variations for the optical components are simulated with Gaussian distributed variations and the resulting probability distribution functions (pdfs) for losses and the refractive index are calculated. Such models and simulations for different active and passive optical components will help to provide variation-aware models and methods for emerging process design kits for silicon photonic technologies.



▲Figure 1: Effect of process variation on a silicon waveguide structure over oxide; (a) side wall verticality, (b) edge roughness.



▲Figure 2: Effect of sidewall verticality variation on waveguide refractive index.



▲Figure 3: Effect of Gaussian edge roughness on Y-Branch transmission in the two different branches; imbalance is seen with roughness.

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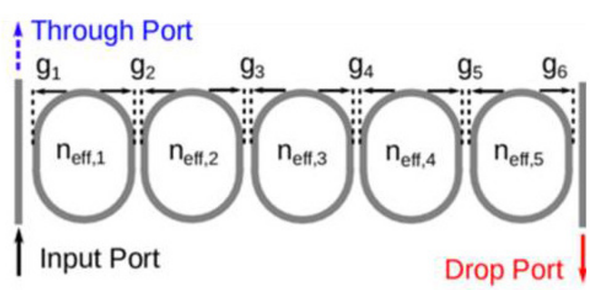
Stochastic Simulation and Robust Design Optimization of Integrated Photonic Filters

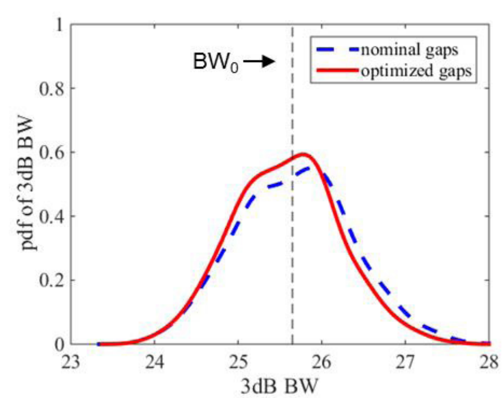
T. W. Weng, D. Melati, A. Melloni, L. Daniel
Sponsorship: NSF

Photonics is rapidly emerging as a mature and promising technology, and it is evolving from a pure research topic to a market-ready player, aiming at achieving large production volumes and low fabrication costs. Pushed by these motivations, Process Design Kits, circuit simulators, generic foundry approaches, and multi-project-wafer runs are quickly changing the way that photonic circuits are conceived and designed. On the other hand, stochastic uncertainties such as fabrication variations are unavoidable in production processes. It is well known that such uncertainties can have a dramatic impact on the functionality of fabricated circuits. In order to obtain a high quality design of a photonic circuit, it is important to include such uncertainties during the early design stages. Hence, uncertainty quantification techniques become fundamental instruments to efficiently obtain the statistical information and to achieve a high-quality design.

Monte Carlo simulation is commonly exploited to evaluate the impact of fabrication uncertainties on the functionality of the designed circuits. Although effective, it suffers from a slow convergence rate and requires a long computation time. Meanwhile, stochastic spectral methods have recently been regarded as a promising alternative for statistical analysis due to their fast convergence. The key idea is to approximate the output quantity of interest (e.g., the bandwidth of a filter) with a set of orthonormal polynomial basis functions, known as generalized polynomial chaos expansion. Our goal in this work is to develop an efficient, robust design-optimization technique based on the state-of-the-art sampled-based stochastic spectral methods, which are mainly used for statistical analysis in the field of uncertainty quantification. Figure 1 shows a fifth-order directly coupled ring resonator used to demonstrate our technique. Due to fabrication process variations, the gap g and effective phase index neff of each ring resonator are uncertain, so the 3dB bandwidth varies greatly. In this example, we would like to design the nominal gap g for each ring that minimizes the mean-square-error of 3dB bandwidth. Figure 2 plots simulation results of the un-optimized nominal design and optimized nominal design. We show that the optimized circuits are more robust to fabrication process variations and achieve a reduction of 11 % to 35 % in the mean-square-errors of the 3dB bandwidth than un-optimized nominal designs.



▲ Figure 1: A 5-ring coupled resonator.



▲ Figure 2: Probability density functions of 3dB. Bandwidth of the un-optimized nominal design (blue dash line) and optimized nominal design (red line).

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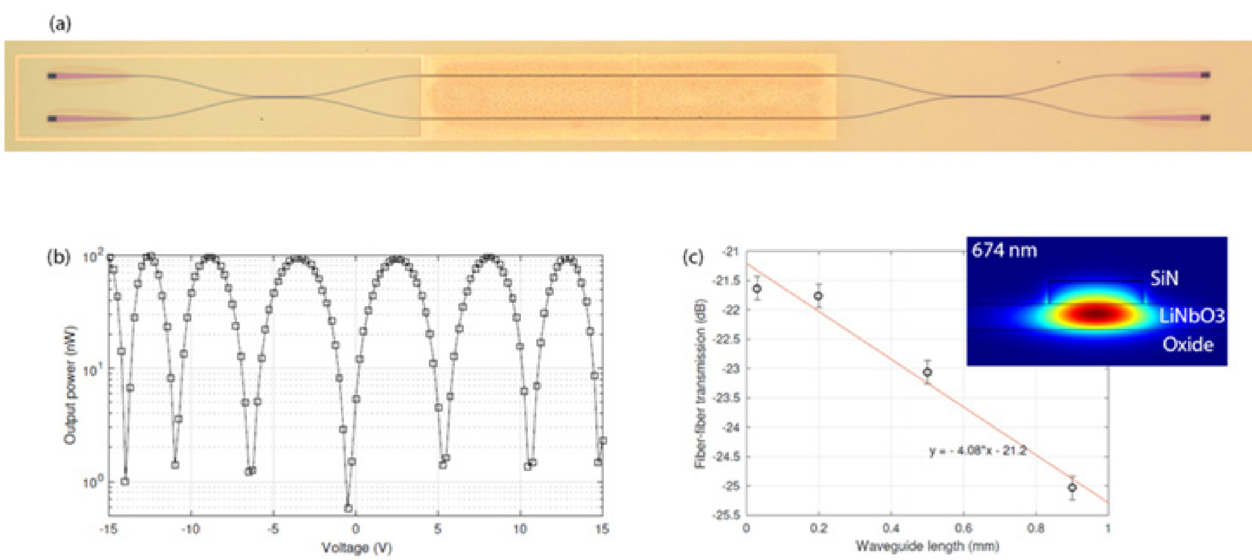
Visible Wavelength Integrated Modulators using Hybrid Waveguides

K. K. Mehta, G. N. West, R. J. Ram
Sponsorship: NSF, Lincoln Laboratory

Infrared integrated optics has proven useful for reducing system size, cost, and complexity for instruments from classical computers to sensors. Visible wavelength integrated photonic devices were the logical next step but common visible waveguides lack the ability to modulate light. We use a hybrid silicon nitride/lithium niobate (SiN/LN) platform to demonstrate visible-wavelength (674 nm) integrated waveguides and Mach-Zehnder-type modulators. The waveguides have propagation loss of ~4.0 dB/cm, and the MZMs were measured to have V_π = 3.0V.

Lithium niobate is one of the most commonly used electro-optically tunable materials for devices such as telecom modulators, due to its large r_{33} tensor component (~31 pm/V). Unfortunately, fabrication methods for directly etching lithium niobate are poor—argon ion etching is the method of choice, but it leaves rough, sloped sidewalls poorly suited to integrated photonic devices. We use the "hybrid" approach, where a layer of high-index material (silicon nitride, ~160 nm) is deposited on top of a thin film of lithium niobate (~215 nm) and patterned using electron beam lithography. The mode effective index around this silicon nitride ridge is then higher than the slab mode, leading to optical confinement. As the mode intensity largely exists inside the lithium niobate, direct electro-optic tuning is achievable.

Tested MZMs had 1 mm and 3 mm modulation lengths (Figure 1a) with Ti/Au contacts in a push-pull configuration deposited directly on the surface of the lithium niobate. The measured extinction was >20 dB. The measured V_π is lower than the voltage predicted by calculations of the mode confinement and applied field, likely due to a contribution from the piezoelectric properties of lithium niobate at low frequencies (Figure 1b).



▲ Figure 1: (a) Optical micrograph of a Mach-Zehnder-type modulator, with an actively modulated length of 1 mm, (b) power transmission as a function of voltage for a tested device, showing a V_π of 3.0V near zero bias, (c) loss of straight waveguide test structures. Inset: Simulated mode profile in the waveguide cross section.

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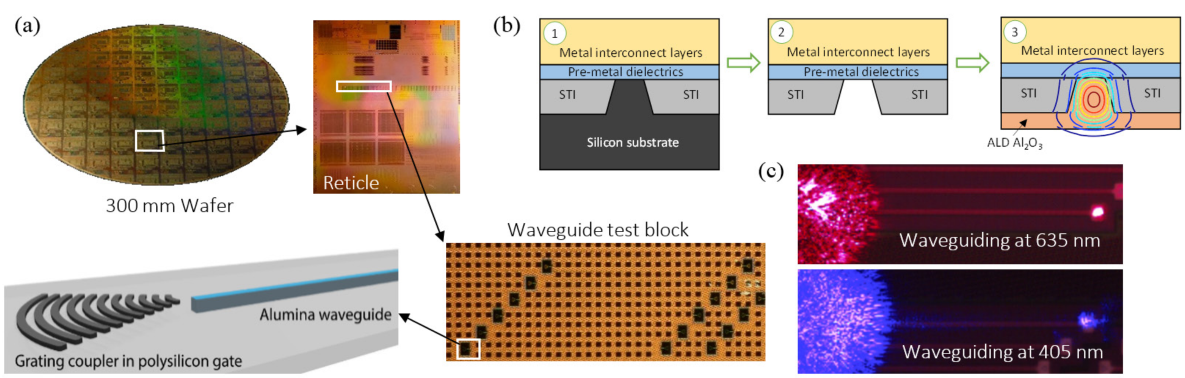
Visible Integrated Photonics in Microelectronic CMOS

A. H. Atabaki, G. N. West, R. J. Ram
Sponsorship: DARPA

Despite numerous advances in visible/near-infrared (VIS/NIR) integrated photonic devices and platforms, less progress has been made toward scalable VIS/NIR platforms that integrate active and passive photonic devices (e.g., waveguides, resonators, and photodetectors). Many VIS/NIR optical applications, from sensing to quantum information processing, require a combination of optical functions from optical addressing and detection to modulation and filtering. Our ability to envision new systems and architectures for these applications hinges on integrated photonic platforms that enable these functions in a scalable fashion. Such platforms are essential to provide the combination of design flexibility and scale-up needed for the next generation of sensing, imaging, and quantum information processing systems.

In this work, our goal is to develop a powerful integrated photonic platform for UV/VIS/NIR wavelengths by implementing passive and active photonic devices monolithically with electronics in a standard complementary metal-oxide semiconductor (CMOS) process. We design all of our devices in CMOS, and implement the passive structures through backend processing of the CMOS chips. Our devices are fabricated in a 300-mm CMOS foundry using IBM's 65-nm bulk CMOS process (Figure 1a). We use the shallow-trench isolation (STI) mask with deep-sub-micron lithography resolution to define a template in the silicon substrate for subsequent incorporation of the passive devices. The CMOS die is flip-chip bonded on a handle, and the silicon under the passives is removed in the XeF2 etcher. The remaining oxide template is then isotropically filled with 200 nm of Al_2O_3 with atomic layer deposition (ALD) at 120˚C. Figures 1a and 1b show the CMOS device and waveguide fabrication process. We also repurposed the transistor gate polysilicon to design very compact grating couplers (Figure 1a). Figure 1c shows light guiding at red and violet in these backend waveguides. Our approach avoids any lithography in post processing, which simplifies fabrication and guarantees perfect alignment of all devices.



▲Figure 1: (a) Photos of the wafer and reticle and micrograph of the waveguide test block. Schematic of the polysilicon grating couplers and waveguide structure shown on the left, (b) backend fabrication steps for VIS waveguides. E-field of the fundamental Transverse Electric (TE) mode is overlaid on panel 3, (c) micrographs of the chip with red and violet light coupled into the Al_2O_3 waveguides. Bright light on the right side of the photos is the guided light radiated out of the chip.

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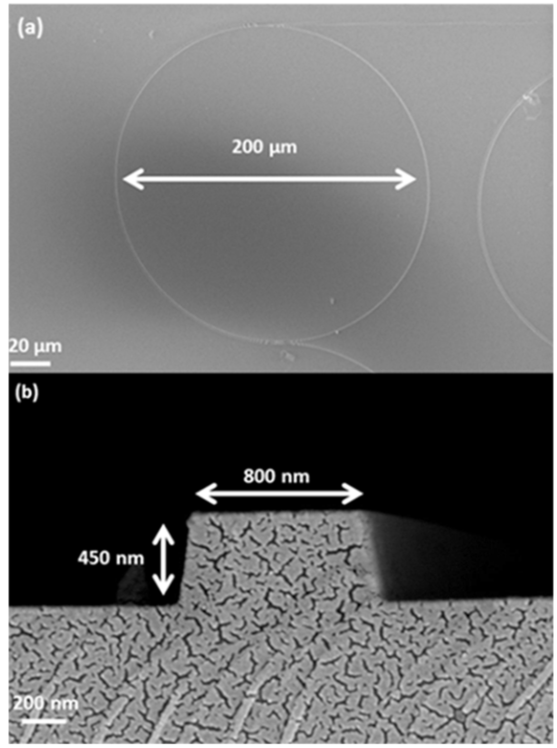
SiC-on-Insulator-on-Chip Photonic Device in a Radiative Environment

D. Ma, Z. Han, Q. Du, J. Hu, L. Kimerling, A. Agarwal
Sponsorship: DTRA

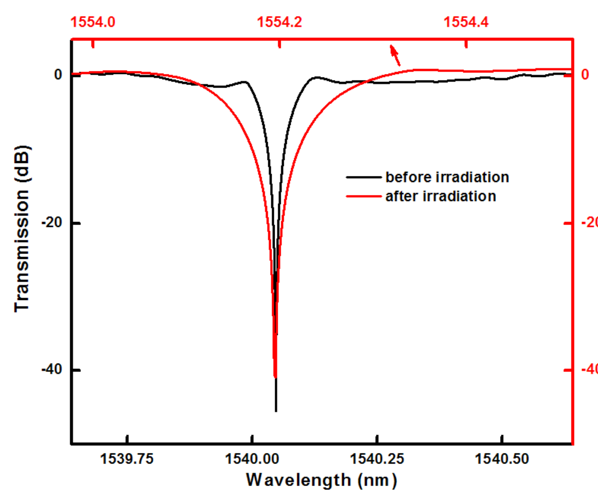
Silicon carbide (SiC) has played significant roles in a variety of electronic and photonic devices in the past decade due to its excellent properties including high irradiation tolerance, stability despite exposure to high temperatures and harsh chemicals, high thermal conductivity, and high Young's modulus. SiC is a good candidate material for on-chip microphotonics because of its high refractive index, large band gap, and complementary metal-oxide semiconductor (CMOS) compatibility. SiC can serve in both active and passive photonic device components. The CMOS compatibility of SiC enables low-cost device processing and scalable industrial applications, highlighting its advantage over other large band gap non-CMOS–compatible semiconductors.

A plasma enhanced chemical vapor deposition (PECVD) system using a silane and methane gas mixture has been used to deposit an amorphous SiC layer on a 6-inch Si wafer with a top layer of 3-micron thermal oxide (Silicon Quest International, Inc.). To pattern and fabricate the SiC-on-insulator photonic device (a resonator), a chromium metal mask was used. Fluorine chemistry was used to dry etch SiC using reactive ion etching. The etch parameters were optimized to enhance the etch rate while still delivering low-loss sidewall profiles as shown in Figure 1.

The effect of gamma irradiation on a SiC resonator was investigated by measuring its quality factor before and after exposing the device to high dose (60 Mrad) gamma irradiation. The quality factor maintained the same order of magnitude, and the resonant peak at critical coupling remained in the near IR range as shown in Figure 2. Both these results demonstrate the gamma irradiation tolerance of the SiC-on-insulator photonic device.



▲Figure 1: Scanning electron microscopic images of (a) the top view and (b) the cross section of the SiC-on-insulator device. (The texture on the cross-section image was due to the gold conductive coating for better image resolution.)



▲Figure 2: Comparison of the resonant peak before (black) and after (red) 60 Mrad gamma irradiation.

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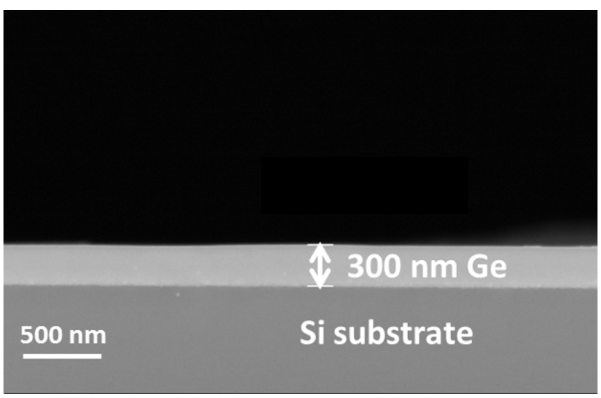
Germanium Electroabsorption Modulator for Silicon Photonic Integration

D. Ma, L. C. Kimerling, J. Michel
Sponsorship: Futurewei Technologies, Inc.

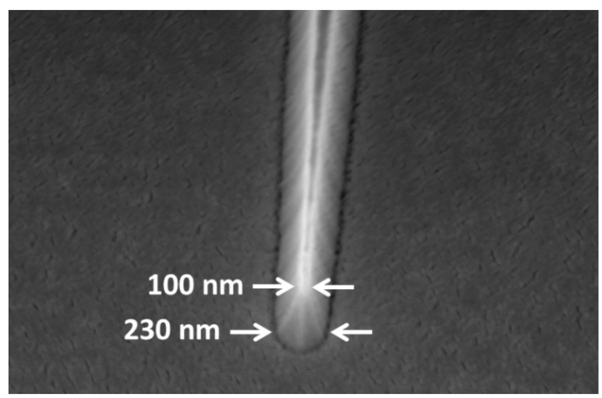
Photonic modulators on Si substrate with high speed and low energy consumption are important components for integrated photonics. The Ge-on-Si system provides an opportunity for integrated electro-absorption modulators that turn the material from transparent to opaque in the working wavelength regime under an applied electric field. Although Ge is an indirect gap semiconductor, its energy difference between the direct gap and indirect gap is as small as 136 meV. The direct band gap of 0.8 eV corresponds to a wavelength of 1550 nm, which is the most technically important wavelength in optical communications and the most commonly used in Si photonics.

The fast speed and low energy consumption of the Ge modulator require high-quality Ge on Si heteroepitaxy. The threading dislocation density, as well as film crystallization and composition, were monitored and controlled. During the ultrahigh vacuum chemical vapor deposition, a constant-composition buffer layer was first deposited at low temperature. Despite the large lattice mismatch, the buffer layer is planar due to limited surface-diffusion, which prevents surface islanding. The buffer layer thickness was optimized to maintain high film quality, on which the high quality Ge epitaxial film was grown at high temperature followed by thermal annealing.

The Si photonic integrated Ge modulator was designed with efficient light coupling from the Si waveguide to the Ge modulator using a Ge taper structure. The effect of taper dimensions on the insertion loss of modular was evaluated in a finite element model and considered in the device fabrication. Insertion loss is the major source of loss when the light signal is transferred from the Si waveguide to the Ge modulator. A fabrication process using electron beam lithography and chemical dry etching has been developed. The pattern formed by the photoresist was transferred using reactive ion etching (REI) to fabricate the Ge taper, which produced a tapered tip with sidewall angle of 100 degrees. A gradually sloped taper tip might improve the coupling efficiency between the Si and Ge components and lower the insertion loss of the modulator because the light couples more effectively through a medium with a gradually changing refractive index.



▲Figure 1: Cross-sectional view, scanning electron microscopy (SEM) image of epitaxial Ge layer on Si substrate.



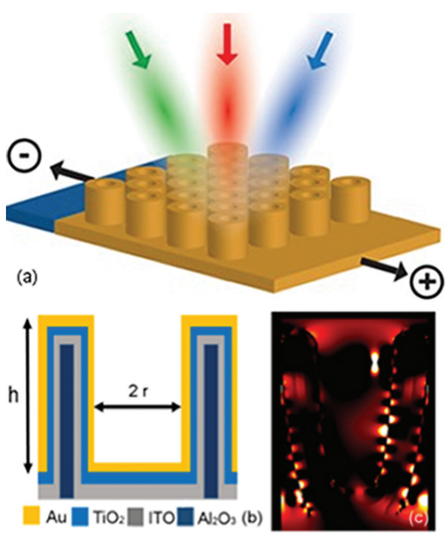
▲Figure 2: Top-front view SEM image of taper tip fabricated via REI.

Surface-Plasmon-Induced Anisotropic Hot Electron Momentum Distribution in a Metallic-Semiconductor Photonic Crystal

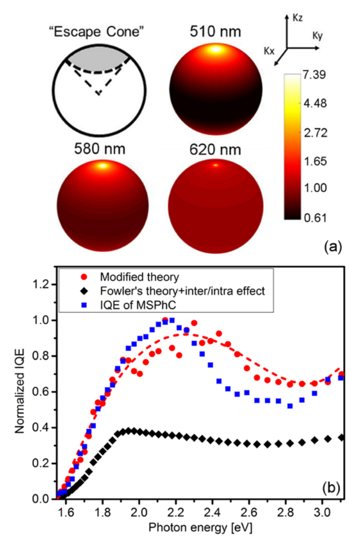
X. H. Li, J. Chou, W. L. Kwan, A. El-Faer, S.-G. Kim
Sponsorship: Masdar Flagship Program

Metallic-semiconductor Schottky hot carrier devices have been found to be a promising solution for harvesting photons with energy lower than the bandgap of semiconductors, which is of crucial importance for realizing efficient solar energy conversion. In recent years, extensive efforts have been devoted to utilizing surface plasmon resonance to improve light absorption of devices by creating strong light-metallic-nanostructure interaction, which generates hot electrons through non-radiative decay. However, how surface plasmon enhances the efficiency of hot electron collection is still debatable.

We recently reported a metallic-semiconductor photonic crystal (MSPhC) with 2D nano-cavity arrays for photochemical energy conversion, which showed a sub-bandgap photoresponse centered at the surface plasmon polariton (SPP) resonance wavelength. Here we developed a theoretical model of internal photoemission in this device by incorporating the effects of anisotropic hot electron momentum distribution caused by SPP. As shown in Figure 1, the structure could generate SPP at the Au/TiO_2 interface along the sidewall of the nano-cavity, with resonance wavelength of 590 nm (photon energy of 2.1 eV). Near resonant wavelength, surface plasmon dominates the electric field in the thin Au layer, which generates hot electrons with high-enough momentum preferentially normal to the Schottky interface, as shown in Figure 2a. The influences of interband and intraband transition and SPP are incorporated to model the internal quantum efficiency of this device, as shown in Figure 2b. The anisotropic hot electron momentum distribution largely enhances the IQE and photoresponse near SPP resonance wavelength. Compared with the widely used Fowler's theory of Schottky internal photoemission, our model can better predict IQE of surface-plasmon-assisted hot electron collection. Combined with large-scale photonic design tools, this quantum-level model could be applied for tuning and enhancing the photoresponse of Schottky hot carrier devices.



▲ Figure 1: (a) Schematic of the metallic-semiconductor photonic crystal with 2D nano-cavity array, (b) Schematic of the cross-section of MSPhC, (c) SPP at the Au/TiO_2 interface along the cavity sidewall at 590 nm, obtained from FDTD simulation.



▲ Figure 2: (a) Anisotropic hot electron momentum distribution caused by SPP. SPP enhances distribution of hot electrons inside the "escape cone" on internal photoemission, (b) Comparison of our model and Fowler's theory on predicting IQE of MSPhC.

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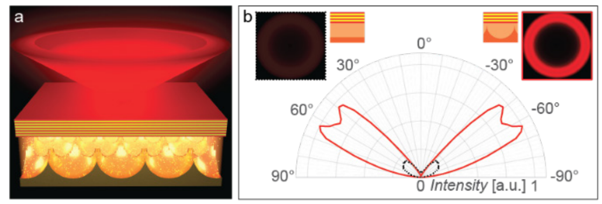
Light-Emitting Surfaces with Tailored Emission Profile for Compact Dark-Field Imaging Devices

C. Chazot, C. J. Rowlands, R. J. Scherer, I. Coropceanu, Y. Kim, K. Broderick, S. Nagelberg, P. So, M. Bawendi, M. Kolle
Sponsorship: MTL, MISTI

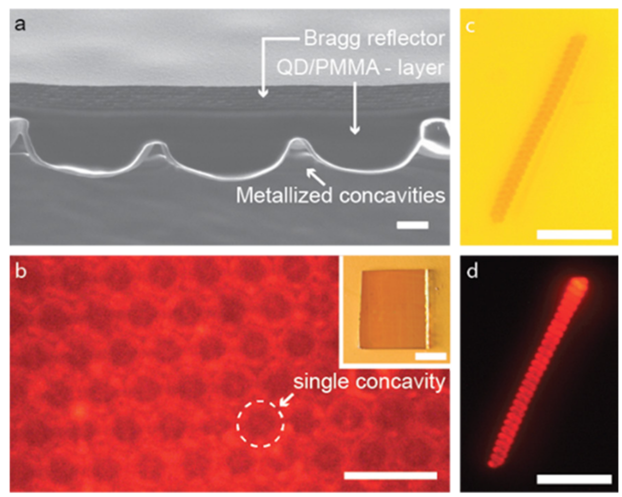
Dark field microscopy is a well-known imaging technique used to enhance the contrast in unstained samples by suppressing low spatial frequency contributions (areas of uniform intensity), thereby emphasizing high spatial frequency components (for instance edges) in the image. The sample is illuminated with light incident on the sample at a high angle that is not collected by the objective lens, unless it is scattered by the imaged object. Even though it is a simple method that provides high-quality images, it usually requires a classic bulky optical microscope, with dedicated objectives and filtering cubes.

Here, we present research aimed at creating a lab-on-chip dark-field imaging device that can provide dark field imaging capabilities without the need for sophisticated equipment. We produce a micro-patterned fluorescent surface with a spatially tunable light emission profile, consisting of quantum dots in a polymer matrix sandwiched between a Bragg reflector on the top and semi-spherical micro-concavities at the bottom. While the quantum dots emit light in all directions, the confinement between the Bragg mirror and the semi-spherical cavities allow only light to exit from the surface in a limited angle range. The color of the emitted light is determined by the quantum dots' emission spectrum, while the stop band of the Bragg reflector imposes directionality. Tuning of the Bragg reflector band-gap, or the combination of Bragg reflectors with different band-gaps, allows for the creation of a rich variety of light emission profiles.

To maximize light emission in the desired limited angle range, an array of bioinspired, hexagonally arranged semi-spherical gold micro-reflectors is used. Each patterned surface measures 1" x 1", and more than 10 Bragg reflectors can be assembled on it, providing the same number of dark-field imaging ring profiles. A sample placed on top of the surface will be illuminated with light of the desired angular distribution only, which for dark-field imaging would be at angles larger than the numerical aperture of the imaging objective. This surface with tailorable light emission profile constitutes a highly compact, simple, tunable solution for dark-field imaging, which could for instance find application in miniaturized imaging devices for microbiology.



▲ Figure 1: (a) Concept schematic of the emission profile of a dark-field enabling light-emitting surface, (b) calculated angular light emission profile for a substrate with flat bottom surface (black curve and left inset) and a substrate with patterned bottom reflector (red curve and right inset).



▲ Figure 2: (a) SEM cross-section view of the light-emitting dark-field substrate. Scale bar 1 μm, (b) Top view of the device. Scale bar 10 μm. Inset shows a macroscopic top-view of the assembled system, (c & d) comparison of the microscope images of a marine micro-organism in bright field imaging (c) and surface-enabled dark-field imaging (d); scale bars 20 μm.

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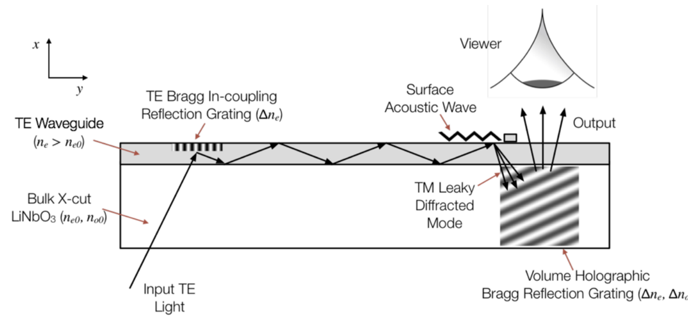
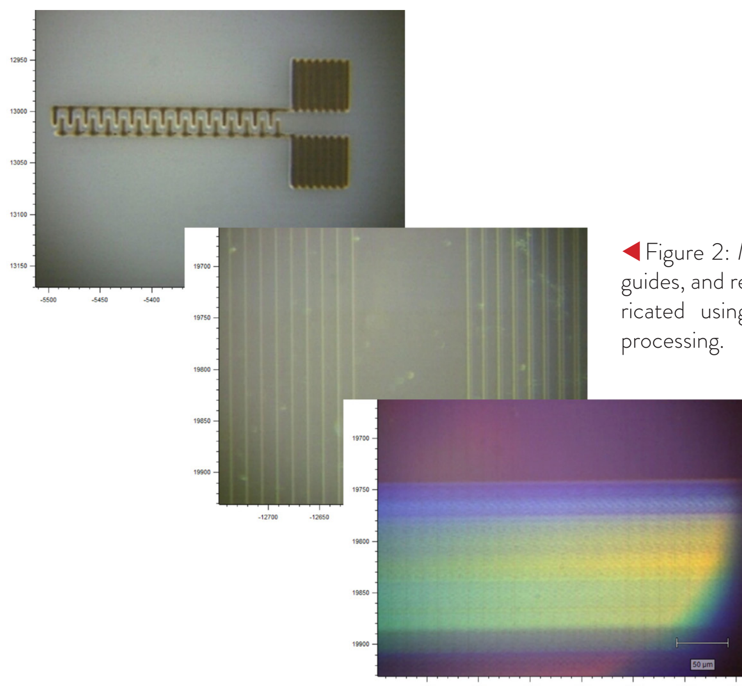
See-Through Light Modulators for Holographic Video Displays

S. Jolly, N. Savidis, B. Datta, V. M. Bove, Jr.
Sponsorship: MIT Media Lab Research Consortium, AFRL

In this research (a collaboration with Dr. Daniel Smalley of Brigham Young University), we design and fabricate acousto-optic, guided-wave modulators in lithium niobate for use in holographic and other high-bandwidth displays. Guided-wave techniques make possible the fabrication of modulators that are higher in bandwidth and lower in cost than analogous bulk-wave acousto-optic devices or other spatial light modulators used for diffractive displays; these techniques enable simultaneous modulation of red, green, and blue light. In particular, we are investigating multichannel variants of these devices with an emphasis on maximizing the number of modulating channels to achieve large total bandwidths. To date, we have demonstrated multichannel full-color modulators capable of displaying holographic light fields at standard-definition television resolution and at video frame rates. Our current work explores a device architecture suitable for wearable augmented reality displays and other see-through applications, in which the light outcouples toward the viewer (Figure 1), fabricated using femtosecond laser micromachining (Figure 2).



▲ Figure 1: Diagram of near-eye version of our device.



◀ Figure 2: Metal features, waveguides, and reflection gratings fabricated using femtosecond laser processing.

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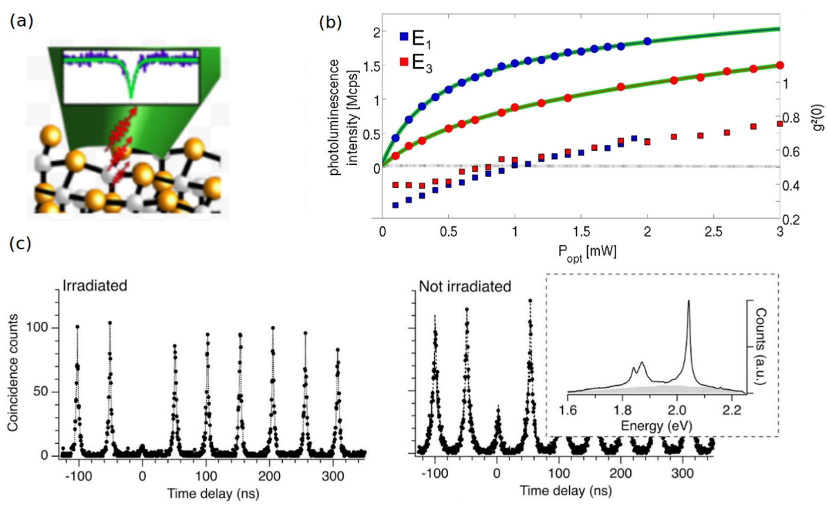
Atomic Color Centers in Wide-Bandgap Semiconductors

B. Lienhard, G. Grosso, H. Moon, T. Schröder, K.-Y. Jeong, S. Mouradian, T.-J. Lu, I. Aharonovich, D. Englund
Sponsorship: NSF CIQM, ARL-CDQI, U.S. Department of Energy: Basic Energy Sciences

Atoms and atom-like emitters play central roles in many areas of quantum information processing, including using them as single-photon sources, nonlinearities, and quantum memories. In recent years, there has been tremendous progress in developing quantum emitter systems based on crystallographic defects in wide-bandgap semiconductors. The interest in solid-state quantum emitters started with in diamond embedded nitrogen vacancy (NV) color centers, which have well-defined optical transitions as well as electronic spin states that can be controlled optically or by microwave radiation. They represent prime systems for solid-state quantum technologies including quantum repeaters, nanoscale sensors, single-photon nonlinearities, and single-photon sources.

Single-crystal silicon carbide (SiC) is another wide-bandgap semiconductor with wider industrial applications than diamond in optoelectronics, high power electronics, and microelectromechanical systems. Recently, we identified a single-photon emitter in 4H-SiC in the visible spectrum, illustrated in Figure 1a. The emitter is photostable at both room and low temperatures and enables 2 million photons per second, shown in Figure 1b. Furthermore, cryogenic measurements reveal a narrow zero phonon line with a linewidth ~0.1 nm that accounts for more than 30% of the total photoluminescence spectrum.

Another emergent material for quantum memories and quantum emitters is layered 2-D materials. They have also recently been shown to host a range of single-photon emitters. Demonstration of quantum emission in 2-D hBN now broadens its appeal for quantum information processing applications. Atom-like defects in hBN confine electronic levels within the extremely wide band gap (5.955 eV) and result in photostable and surprisingly robust emitters with single-photon emitter characteristics. The emission energy of these emitters spans a large spectral band, limiting individual emitter indistinguishability. Recently, we were able to improve optical properties, indicated in Figure 1c, and demonstrated spectral tuning of such hBN emitters. The tunability promises the generation of many quantum emitters with frequency-matched emission.



▲ Figure 1: (a) Schematic of single-photon emitter (SPE) in silicon carbide, (b) intensity and single-photon emission purity measurement of SPE in silicon carbide, (c) pulsed second-order autocorrelation histograms in purified (irradiated) and untreated area of SPE in hexagonal boron nitride. Inset shows a spectrum indicating the sum of the spectral components of the SPE (black) and background (gray).

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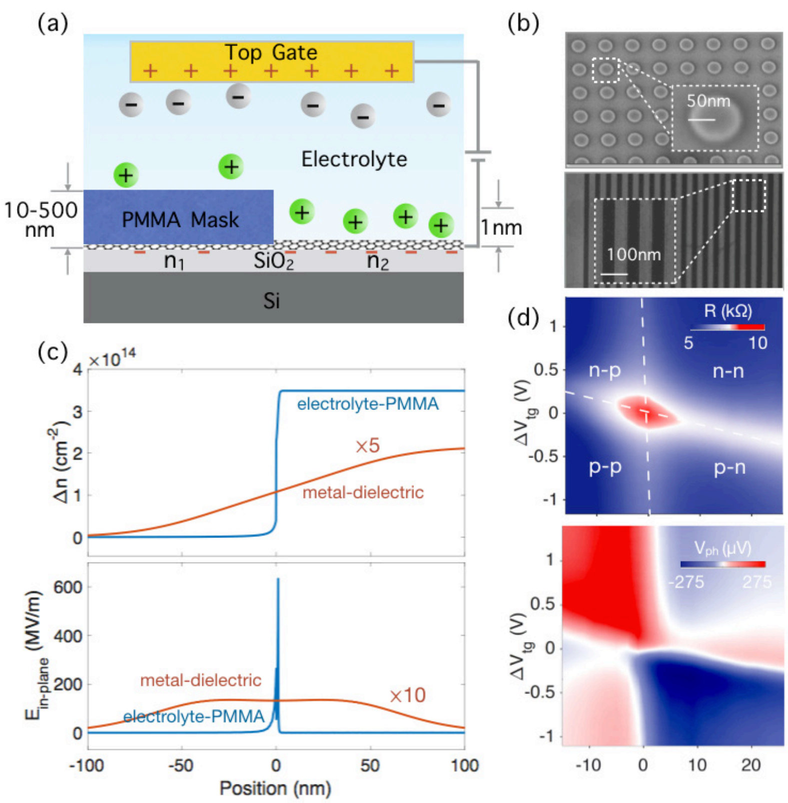
Self-Aligned Local Electrolyte Gating of 2-D Materials with Nanoscale Resolution

C. Peng, D. K. Efetov, S. Nanot, R.-J. Shiue, G. Grosso, Y. Yang, M. Hempel, P. Jarillo-Herrero, J. Kong, F. Koppens, D. Englund
Sponsorship: ONR, MIT Lincoln Laboratory

A central challenge in making 2-D material-based devices faster, smaller, and more efficient is to control their charge carrier density at the nanometer scale. Traditional gating techniques based on capacitive coupling through a gate dielectric cannot generate strong and uniform electric fields at this scale due to divergence of the fields in dielectrics. This field divergence limits the gating strength, boundary sharpness, and pitch size of periodic structures and restricts possible geometries of local gates (due to wire packaging), precluding certain device concepts, such as plasmonics and transformation optics based on metamaterials.

Here we present a new gating concept based on a dielectric-free, self-aligned electrolyte technique that allows spatial modulation of charges with nanometer resolution. We employ a combination of a solid-polymer electrolyte gate and an ion-impenetrable e-beam-defined resist mask to locally create excess charges on top of the gated surface. Electrostatic simulations indicate high carrier density variations Δn = 1014 cm-2 across a length of 10 nm at the mask boundaries on the surface of a 2-D conductor, resulting in a sharp depletion region and a strong in-plane electric field of 6×10^8 V/m across the so-created junction.

We apply this technique to the 2-D material graphene to demonstrate the creation of tunable p-n junctions for optoelectronic applications. We also demonstrate the spatial versatility and self-aligned properties of this technique by introducing a novel graphene thermopile photodetector in the mid-infrared.



◀Figure 1: (a) Geometry and working principle of nanoscale electrolytic doping of 2-D materials with PMMA screening mask. n_1 and n_2 denote charge carrier densities in mask-protected region and exposed region, respectively, (b) simulated charge carrier density n profile and in-plane electric field intensity $E_{in-plane}$ for single junction, compared between proposed electrolyte-PMMA-mask gating and metal-dielectric split gating schemes, (c) scanning electron micrographs of fabricated PMMA masks on graphene with nanoscale dimensions. (d) Resistance R and photovoltage V_{ph} as function of V_{tg} and V_{bg}, measured at p-n interface created by PMMA-electrolyte doping technique.

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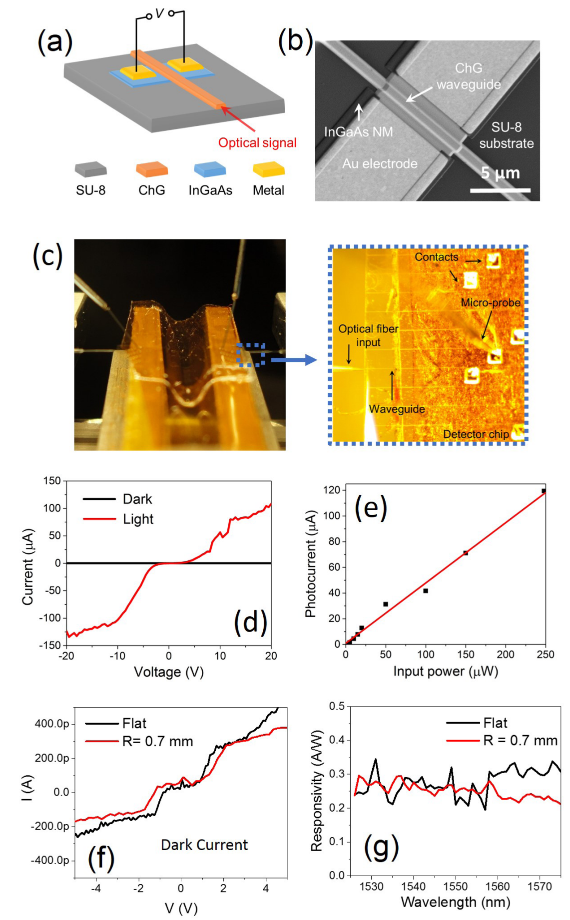
Flexible Chalcogenide Glass Waveguide Integrated Photodetectors

L. Li, H. Lin, J. Michon, Y. Huang, J. Li, C. Smith, K. Richardson, J. Hu

Flexible photodetectors are important components for imaging, communications, and sensing applications. Traditional photodetectors are typically made on rigid semiconductor substrates and couple to incident light via free space. Here we present an experimental demonstration of waveguide coupled flexible photodetectors. By taking advantage of the substrate-blind integration capacity of chalcogenide glass photonic components, high index contrast glass optical waveguides were monolithically integrated on InGaAs nanomembrane metal semiconductor metal photodetectors hybrid-bonded to flexible substrates (Figure 1a-b).

To monitor the photodetector response, we have assembled the measurement setup shown in Figure 1c. A pair of motion stages was used to control the bending of the flexible detector, and another two tapered lens-tip fibers were used to couple light from a laser into and out of the waveguides. Two micro-probes were used to detect the electrical response. Figure 1d plots the current-voltage (I-V) curves of the detector measured in the dark and under illumination with 250-µW incident optical power at 1550-nm wavelength. The device shows a negligible saturation dark current of 0.5 nA at 10 V bias. The photocurrent increases linearly with increasing optical power, as shown in Figure 1e. Slope of the response curve yields a responsivity of 0.5 A/W at 1550 nm, corresponding to an external quantum efficiency of 40%. Further, the dark current and photo response of the device remain unchanged with bending radii down to 0.7 mm, which represents a significant improvement in mechanical flexibility over previously demonstrated semiconductor NM photodetectors (Figure 1f-g).



▲Figure 1 Waveguide integrated flexible detectors. (a) Schematic diagram of the glass waveguide-integrated photodetector, (b) SEM micrograph of a detector, (c) photo of the testing setup, (d) I-V response of the detector in the dark and under illumination, (e) photocurrent of the detector as a function of input optical power in the waveguide, (f) I-V response in the dark under flat and bending condition, (g) spectral response of the detector at -5 V bias under flat and bending condition.

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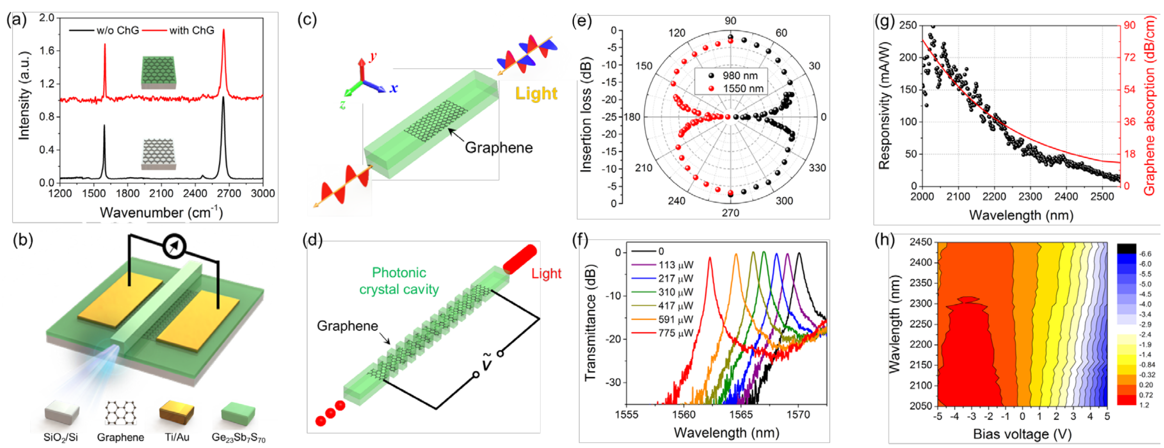
Monolithically Integrated Glass on Two-Dimension Materials Photonics

H. Lin, Y. Song, Y. Huang, D. Kita, S. Deckoff-Jones, K. Wang, L. Li, J. Li, H. Zheng, Z. Luo, H. Wang, S. Novak, A. Yadav, C. Huang, R. J. Shiue, D. Englund, T. Gu, D. Hewak, K. Richardson, J. Kong, J. Hu

Two-dimensional (2-D) materials are of tremendous interest to integrated photonics given their singular optical characteristics spanning light emission, modulation, saturable absorption, and nonlinear optics. The current approach to integrating 2-D materials with photonic devices generally relies on transferring these atomically thin crystals onto prefabricated photonic components, which limits the yield and fully utilizing their capabilities. To resolve these issues, an alternative integration route entails growing an optically thick chalcogenide glass (ChG) film directly on 2-D materials and lithographically patterning it into functional photonic devices. Figure 1a displays the Raman spectra of monolayer CVD graphene before and after coating with a 450-nm- thick ChG film. No defect-related peaks (D, D' or D+G) were observed after ChG deposition, indicating that the low-temperature glass deposition does not introduce structural defects into graphene. We further confirm that the structures of other 2-D materials (MoS2, black phosphorus, InSe, and hexagonal BN) likewise remain intact after ChG deposition.

Such integration compatibility not only leads to a bottom-up process to fabricate mid-IR photodetectors (Figures 1b and 1g) or modulators, but also facilitates the fabrication of unconventional multi-layer structures incorporating 2-D materials to optimally engineer their interactions with the optical mode. As an example, we exploit the giant optical anisotropy of graphene and modal symmetry in graphene-sandwiched waveguides to demonstrate an ultra-broadband polarizer (Figure 1c and 1e) and a thermo-optic switch with energy efficiency an order of magnitude higher than previous reports (Figures 1d and 1f). In addition, the insulating ChG can function as a gate dielectric. We harness this feature to demonstrate the first mid-IR graphene waveguide modulator (Figure 1h). We foresee that the versatile glass-on-2D-material platform will significantly expedite and expand integration of 2-D materials to enable new photonic functionalities.



▲Figure 1: (a) Raman spectra of as-transferred monolayer CVD graphene (black) and graphene covered with a $Ge_{23}Sb_7S_{70}$ glass layer (red), schematic diagrams of (b) mid-IR waveguide-integrated detector, (c) graphene-sandwiched waveguide polarizer, and (d) photonic crystal thermo-optic switch, (e) polar diagram showing the polarizer performance at 980-nm and 1550-nm wavelengths, (f) optical transmission spectra of the switch at varying input power levels into the graphene heater, (g) mid-IR broadband spectral dependences of the detector's responsivity (at 1.5 V bias) and calculated optical absorption in the graphene layer, and (h) measured color contour maps showing wavelength and bias dependent modulation depth of the device in dB/mm (relative to its transmittance at zero bias).

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Broadband Optical Phase Change Materials and Devices

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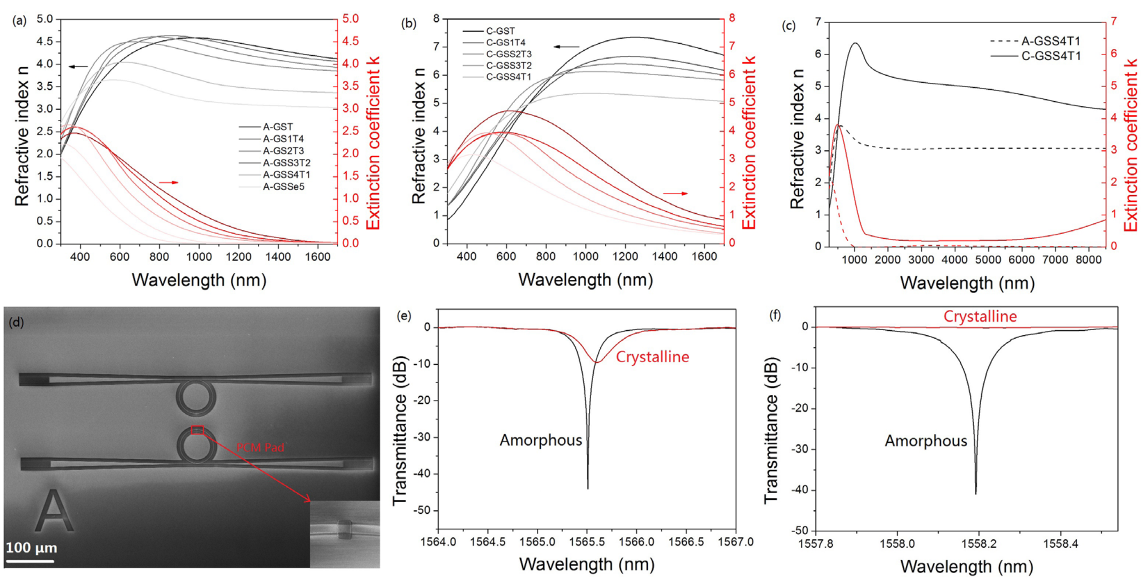
Sponsorship: DoD

Optical phase change materials (O-PCMs) are a class of materials that exhibit extraordinarily large optical property change (e.g., index change $\Delta n > 1$) when undergoing a solid-state phase transition. These materials, such as Ge-Sb-Te (GST) compounds, have been exploited for a plethora of optical applications including optical switching, reconfigurable metasurface, and non-volatile display. Traditional phase change materials, however, generally suffer from large optical losses even in their dielectric states. The large optical losses fundamentally limit the performance of photonic devices based on traditional O-PCMs.

Here we report the synthesis, characterization and device integration of a new class of O-PCMs, Ge-Sb-Se-Te (GSST) alloys. A series of GSST thin films with the compositions of $Ge_2Sb_2Se_xTe_{5-x}$ (x = 1, 2, 3, 4, and 5) were prepared using thermal evaporation. We experimentally validated that Se substitution for Te results in an increase in the optical band gap, enabling low loss operation in the telecommunication bands (Figure 1a and 1b). Meanwhile, the GSST materials claim reduced free carrier concentrations and mobility compared to GST, which effectively suppresses free carrier absorption in the infrared. Figure 1c shows that the $Ge_2Sb_2Se_4Te_1$ (GSS4T1) material features broadband transparency covering 1 micron to the long wave infrared (LWIR). The low optical loss of the GSS4T1 alloy leads to an exceptionally better performance than $Ge_2Sb_2Te_5$ (GST 225).

We deposited and patterned GSST and GST pads on SiN micro-ring resonators. Figure 1e and 1f plot the transmittance spectra of micro-ring devices integrated with the GST 225 and the GSS4T1 O-PCMs when they are switched from amorphous to crystalline state. The device integrated with the GSS4T1 material claims a large on/off contrast ratio of 41 dB and an insertion loss of 0.2 dB, both of which represent significant improvements compared to state-of-the-art GST-based devices.



▲Figure 1: (a & b) optical properties of (a) amorphous and (b) crystalline GSST alloys, (c) optical properties of amorphous (dashed lines) and crystalline (solid lines) GSS4T1 from the visible to LWIR, (d) SEM images of fabricated devices, (e & f) transmission spectra of (e) GST-based and (f) GSS4T1-based devices.

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High-Performance Inorganic CsPbBr3 Perovskite Light-Emitting Diodes by Dual Source Vapor Deposition

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Sponsorship: U.S. Department of Energy EFRC

Organometal halide-based perovskites, with the typical chemical formula ABX_3, have emerged as a promising class of semiconducting materials for thin-film optoelectronics in the past few years. Those semiconductors possess unique electro-optical properties, such as long-range carrier diffusion length, high absorption coefficients, and low levels of defect states, yielding solar cells with over 20% power conversion efficiency. While many of the research efforts have been captivated by the potential of their photovoltaic applications, perovskites are nonetheless promising light emitters. Indeed, color-tunable electrically-driven perovskite light-emitting diodes (PeLEDs) have tremendous potential for novel display and lighting applications. In addition to its bright photoluminescence (PL) and excellent wavelength tunability, $CsPbX_3$ (X=I, Br, Cl) in particular exhibits superior thermal and chemical stabilities when compared to organic-inorganic analogs such as $CH_3NH_3PbX_3$.

Unfortunately, low solubility limits of CsBr precursor hinder the fabrication of a dense, compact $CsPbBr_3$ layer with complete coverage and smooth morphology via solution processing. Incomplete coverage of perovskite emitting layers results in substantial leakage current that has limited the luminescent efficiency of previously reported cesium-based PeLEDs. Physical vapor deposition of fully inorganic $CsPbX_3$ perovskites offers a scalable alternative to solution processing. In this work, we report a systematic approach for preparation of highly efficient $CsPbBr_3$ PeLEDs using vacuum deposition. Fabrication of $CsPbBr_3$ thin films with complete surface coverage and reduced roughness in addition to precise control over the film thickness and stoichiometry is demonstrated. Perovskite films are optimized for the best device performance by varying parameters including evaporation rate, film thickness, and composition of the as-deposited perovskite layer. As a result, $CsPbBr_3$-based PeLEDs that exhibit narrow green emission significantly reduced leakage current; therefore, substantially improved brightness and efficiency were realized.

Multilayer Thin Films for Hot Carrier Filtering and Spectroscopy

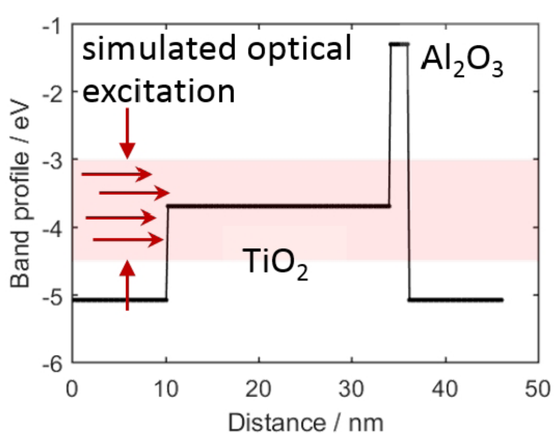
Z. J. Tan, N. X. Fang

Hot carriers are electrons or holes not in thermal equilibrium with its lattice. They can be generated electrically by injection through a barrier layer or optically from plasmonic excitations. These hot carriers can have useful large excess energy of several eVs much larger than the energy which can be supplied thermally under practical conditions.

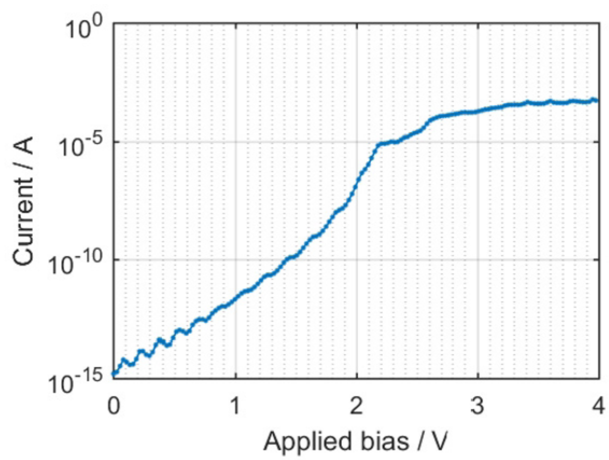
However, it is difficult to harvest the full potential of these hot carriers due to their fast thermalization times. Furthermore, there is very little insight into how one can control or measure the energy profile of these hot carriers due to the lack of robust experimental techniques that can probe these carriers before thermalization sets in.

We perform simulations to show that the use of multilayer dielectric films can be used as bandpass filters to retrieve the energy profile of hot carriers (see Figures 1 and 2). The measured electrical current through a crossbar structure separating such a stack of dielectric film can be inverted to deduce the initial energy profile of generated hot carriers because hot carriers with different energies have different transmissions across the barriers. Existing work with hot carrier filtering uses only single layer oxides. We show that a dual layer TiO_2/Al_2O_3 stack has a high discriminatory power for hot carrier spectroscopy.

We are fabricating devices to compare with our theoretical predictions. In our device, optical generation of hot carriers is optimized by choosing the material and thickness of the metal terminal to increase absorptivity at 405 nm. Joint density-of-state calculations show that highly energetic hot electrons can be produced in Au beyond an illumination energy threshold of 3 eV. We intend to use our multilayer dielectric films to perform energy spectroscopy on these hot carriers.



▲Figure 1: Simulated conduction band-edge profile for a TiO_2/Al_2O_3 stack and assuming a uniform profile of optically generated carriers at the source.



▲Figure 2: The simulated electrical current shows a bend (at 2.2 V) whose properties are dependent on the band profile design and the energy profile of hot electrons are the source. An experimental version of this graph will allow us to deduce the actual energy profile of generated hot carriers.

Research Centers

Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Eight faculty members participate in the CICS: Director Hae-Seung Lee, Duane S. Boning, Anantha Chandrakasan, Ruonan Han, David Perreault, Max Shulaker, Charles Sodini, and Vivienne Sze.

CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed, THz, and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, biomedical circuits, deep learning systems, emerging technologies, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy.

CICS's research portfolio includes all research projects that the eight participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

MIT/MTL Center for Graphene Devices and 2D Systems

Professor Tomás Palacios, Director

The MIT/MTL Center for Graphene Devices and 2D Systems (MIT-CG) brings together MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional materials.

Graphene and other two-dimensional (2D) materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines thanks to their extreme properties. These materials are the lightest, thinnest, strongest materials we know of, at the same time that they have very rich electronic and chemical properties. For more than 40 years, MIT has led the work on the science and engineering of 2D materials. More recently, since 2011, the MIT/MTL Center for Graphene Devices and 2D Systems (MIT-CG) has played a key role in coordinating most of the work going on at MIT on these new materials, and in bringing together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced technologies and strategies that enable 2D materials, devices, and systems to provide discriminating or break-through capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials to optoelectronics, RF communications, and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools, and analysis for the creation of a vision for the future of new systems enabled by 2D materials.

Some of the multiple benefits of the Center's membership include complimentary attendance to meetings, industry focus days, and live webcasting of seminars related to the main research directions of the Center. The members of the Center also gain access to a resume book that connects students with potential employers, as well as access to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today's challenges for these materials, devices, and systems.

MIT/MTL Gallium Nitride (GaN) Energy Initiative

Professor Tomás Palacios, Director

The MIT/MTL Gallium Nitride (GaN) Energy Initiative (MIT GaN) is an interdepartmental program that brings together 10 MIT faculty and more than 40 other researchers and industrial partners to advance the science and engineering of GaN-based materials and devices for energy applications.

The GaN Energy Initiative provides a holistic approach to GaN research for energy applications, and it coordinates work on the growth, technology, novel devices, circuits, and systems to take full advantage of the unique properties of GaN. The GaN Energy Initiative is especially interested in developing new beyond-state-of-the-art solutions to system-level applications in RF power amplification, mixed signal electronics, energy processing, and power management, as well as advanced optoelectronics. Most of the work is done on GaN materials and devices that are compatible with Si fabrication technologies, in close collaboration with industrial partners to accelerate the insertion of these devices into systems.

The MIT/MTL Gallium Nitride (GaN) Energy Initiative organizes numerous activities to advance the understanding of GaN materials, technology and devices. Some of these activities include webcast of seminars and annual meetings, as well as joint collaborations with industry partners. The Initiative also elaborates a resume book of graduating students and provides timely access to white papers and pre-prints through its website.

The MIT Medical Electronic Device Realization Center

Professor Charles Sodini, Director

The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will, in turn, transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personal medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personal medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication, and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient's needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry's societal transformation, Medical Electronic Devices.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacture devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners' diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure, and cerebral blood flow velocity. Since its founding in 2011, MEDRC has grown from 2 to 5 sponsoring companies with several other companies in serious discussions. There are currently fifteen MEDRC funded research projects that are defined by ten MIT faculty, ten clinicians, and our sponsoring companies supporting approximately twenty students. A visiting scientist from a project's sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

In addition to the strong relationship with MTL, MEDRC is associated with MIT's Institute for Medical Engineering and Science (IMES), that has been charged to serve as a focal point for researchers with medical interest across MIT. MEDRC has been able to create strong connections with the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. With the support of MTL and IMES, MEDRC will serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

M. Shulaker, et. al., "3D NanoSystem Integrated Heterogeneous Nanotechnologies for Computation Immersed in Memory," [in press], 2017.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

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A. Al-Obeidi, D. Kramer, R. Moenig, and C. V. Thompson, "Mechanical Stresses and Crystallization of Lithium Phosphorous Oxynitride-Coated Germanium Electrodes during Lithiation and Delithiation," *J. Power Sources*, vol. 306, 817-825, 2016.

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SELECTED PUBLICATIONS

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Glossary

TECHNICAL ACRONYMS

ADC	Analog-to-Digital Converters
CMOS	Complementary metal–oxide–semiconductor
CNT	Carbon nanotubes
FET	Field-effect transistor
MOSFET	Metal–oxide–semiconductor field-effect transistor

MIT ACRONYMS & SHORTHAND

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
ISN	Institute for Soldier Nanotechnologies
KI	David H. Koch Institute for Integrative Cancer Research
LL	Lincoln Laboratory
MAS	Program in Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MIT-CG	MIT/MTL Center for Graphene Devices and 2D Systems
MITEI	MIT Energy Initiative
MIT-GaN	MIT/MTL Gallium Nitride (GaN) Energy Initiative
MISTI	MIT International Science and Technology Initiatives
MIT-SUTD	MIT-Singapore University of Technology and Design Collaboration Office
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
↥**SMART**	Singapore-MIT Alliance for Research and Technology Center
↥**SMART-LEES**	SMART Low Energy Electronic Systems Center
SUTD-MIT	MIT-Singapore University of Technology and Design Collaboration Office

U.S. GOVERNMENT ACRONYMS

AFOSR	U.S. Air Force Office of Scientific Research
AFRL	U.S. Air Force Research Laboratory
ARL	U.S. Army Research Laboratory
↳**ARL-CDQI**	U.S. Army Research Laboratory Center for Distributed Quantum Information
ARO	Army Research Office
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
DARPA	Defense Advanced Research Projects Agency
DoD	Department of Defense
DoE	Department of Energy
↳**EFRC**	U.S. Department of Energy: Energy Frontier Research Center (Center for Excitonics)
DTRA	U.S. DoD Defense Threat Reduction Agency
IARPA	Intelligence Advanced Research Projects Activity
↳**RAVEN**	Rapid Analysis of Various Emerging Nanoelectronics
NASA	National Aeronautics and Space Administration
↳**GSRP**	NASA Graduate Student Researchers Project
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
↳**NCI**	National Cancer Institute
NRO	National Reconnaissance Office
NSF	National Science Foundation
↳**CBMM**	NSF Center for Brains, Minds, and Machines
↳**CIQM**	Center for Integrated Quantum Materials
↳**CSNE**	NSF Center for Sensorimotor Neural Engineering
↳**E3S**	NSF Center for Energy Efficient Electronics Science
↳**IGERT**	NSF The Integrative Graduate Education and Research Traineeship
↳**NEEDS**	NSF Nano-Engineered Electronic Device Simulation Node
↳**SEES**	NSF Science, Engineering, and Education for Sustainability
↳**STC**	NSF Science-Technology Center
ONR	Office of Naval Research

OTHER ACRONYMS

CNRS Paris	Centre National de la Recherche Scientifique
CONACyT	Consejo Nacional de Ciencia y Tecnología (Mexico)
IEEE	Institute of Electrical and Electronics Engineers
IHP Germany	Innovations for High Performance Microelectronics Germany
KFAS	Kuwait Foundation for the Advancement of Sciences
MASDAR	Masdar Institute of Science and Technology
NTU	Nanyang Technological University
NUS	National University of Singapore
NYSCF	The New York Stem Cell Foundation
SRC	Semiconductor Research Corporation
↥NEEDS	NSF/SRC Nano-Engineered Electronic Device Simulation Node
SUTD	Singapore University of Technology and Design
TEPCO	Tokyo Electric Power Company
TSMC	Taiwan Semiconductor Manufacturing Company

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