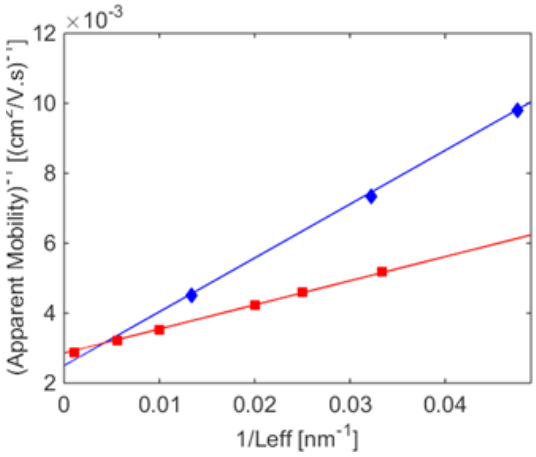
Electronic Devices

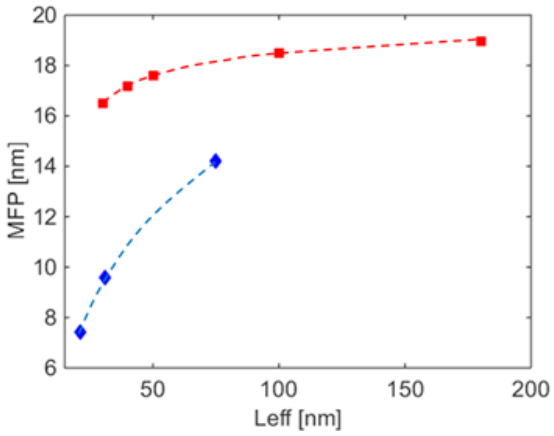
On Apparent Electron Mobility in Si nMOSFETs from Diffusive to Ballistic Regimes

D. A. Antoniadis
Sponsorship: Ray and Maria Stata Chair

The Matthiessen-law combination of diffusive and ballistic mobility provides a framework to explain the decrease of apparent mobility in near-ballistic field-effect transistors (FETs). While this theory works well for III-V FETs reported to date, it under-predicts the mobility decrease in several Si experiments, raising concerns about FET performance in the near-ballistic regime. In this work, recent SOI planar and FinFET n-MOSFET I-V data are analyzed in detail, accounting for the effect of channel degeneracy. Assuming a channel-length independent mean free path (MFP), it is demonstrated that good agreement can be obtained with the conventional Matthiessen-law combination modified to include the effect of drain-channel backscattering recently proposed by Natori et al [1]. On the other hand, good agreement can also be obtained with the Matthiessen-law combination if the MFP is assumed to be channel-length dependent. The full range of $I_d(V_{gs}, V_{ds})$ is well modeled by incorporating either of these effects in a recent transmission-based compact model, but drastically different critical lengths for backscattering must be used in the Landauer formulation in the saturation region. It is also shown that this apparent anomaly is technology-dependent and its effect in overall device performance is discussed.



▲ Figure 1: Comparison of extracted apparent mobilities for the ETSOI (squares) where R=0.2 and FinFET (diamonds) where R=0.65, technologies. The channel degeneracies correspond approximately to N_s=6x10^{12} cm^{-2}, which occurs at V_{gs}=0.5 and 0.8 V, respectively. Mean free paths in both cases are assumed independent of channel length with values 19.7 and 26 nm respectively.



▲ Figure 2: MFP vs. L_{eff} for the ETSOI (squares) where and FinFET (diamonds) technologies. Channel degeneracy corresponds to N_s=6x10^{12} cm^{-2}. Dashed lines are guides to the eye only. The long-channel MFP from for the same degeneracy for these two technologies is 19.7 and 26 nm respectively.

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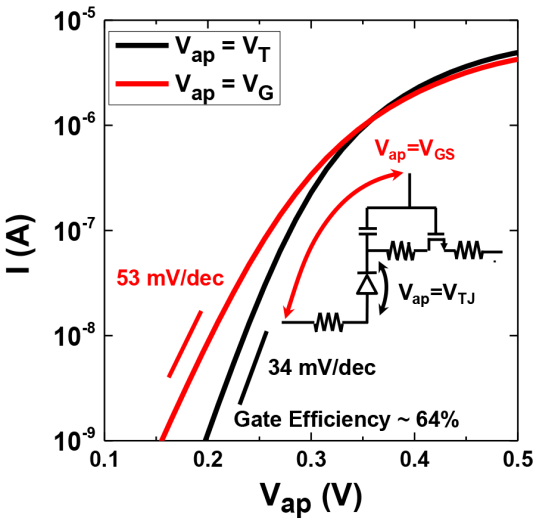
Gate Efficiency in InGaAs/GaAsSb Quantum-well Tunnel-FETs

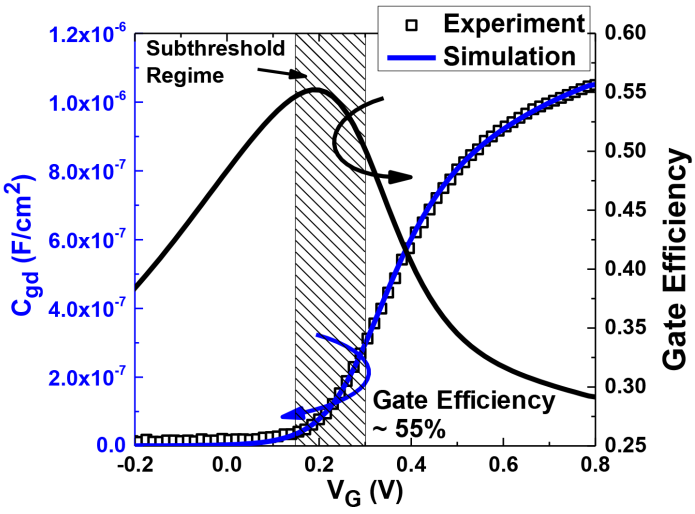
T. Yu, U. Radhakrishna, J. L. Hoyt, D. A. Antoniadis
Sponsorship: NSF E3S

The tunnel field-emission transistor (TFET), in which carrier injection is determined by gate-controlled tunneling from the source to the channel, has been attractive as one of the promising candidates for future ultra-low-power applications. In this study, *inline-TFETs* with tunneling direction aligned to the gate electric field are designed, fabricated, and analyzed based on InGaAs/GaAsSb material. Using ultrathin InGaAs/GaAsSb quantum-wells (QWs), the device fabrication technology was developed and the tunneling properties of two successive generations of QWTFETs were investigated. In the first generation QWTFETs, the limitation of gate oxide quality on InGaAs and parasitic thermal currents manifested itself in degraded subthreshold swing (SS) of 140 mV/dec, as well as strongly temperature-dependent SS from 300 K to 77 K. The second generation QWTFETs with sub-nm InP cap between the gate oxide and InGaAs channel and revised structure design has demonstrated improved SS of 87 mV/dec at 300 K and temperature-independent SS below 140 K, indicating the achievable tunneling current steepness with the current device design.

Physical modeling and quantum simulations based on the low-temperature I-V characteristics were used to analyze the fundamental gate efficiency of the experimental QWTFETs to reveal the ultimate intrinsic tunneling steepness of the InGaAs/GaAsSb tunneling junction. The extracted gate efficiency around 55-64% is due to the coupling of the gate capacitance and tunneling junction capacitance and degrades significantly the attainable SS in the QWTFET. On the other hand, the implied intrinsic tunneling steepness of the InGaA/GaAsSb is around 30 mV/dec, almost identical to previously reported non-abruptness of the conduction/valence band-edge into the bandgap. The result indicates the possibility of achieving SS as low as 38 mV/dec in QWTFETs by improving gate efficiency (GE) by up to 78% with proposed optimized parameters based on simulation results.



▲Figure 1: Comparison between the I-V characteristics with voltage applied at the gate and directly across the tunneling junction. The ratio of the subthreshold swings indicates a GE of ~64%.



▲Figure 2: C-V and extracted GE based on the quantum simulation of the InGaAs/GaAsSb MOS capacitor. GE is defined by the change in first sub-band energy (ΔE_1) over the change in the gate potential (ΔqV_G). The extracted GE_{max} is ~55%, close to the value extracted from the model.

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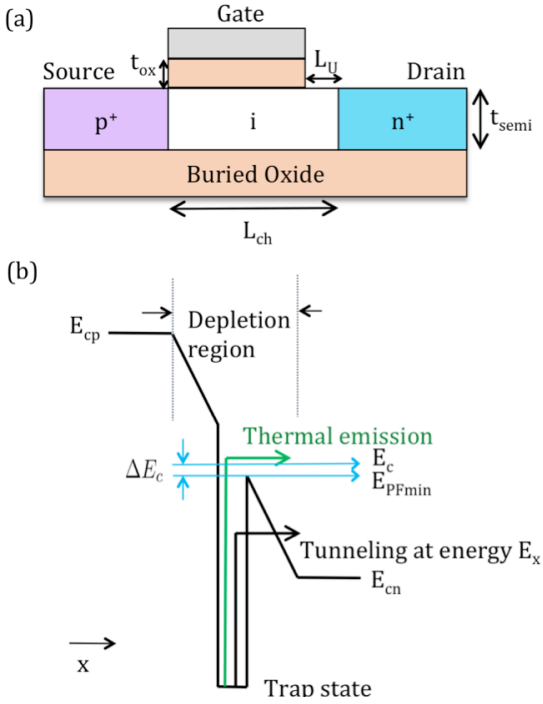
Impact of Trap-Assisted Tunneling on the Performance of Tunnel Field-Effect Transistors

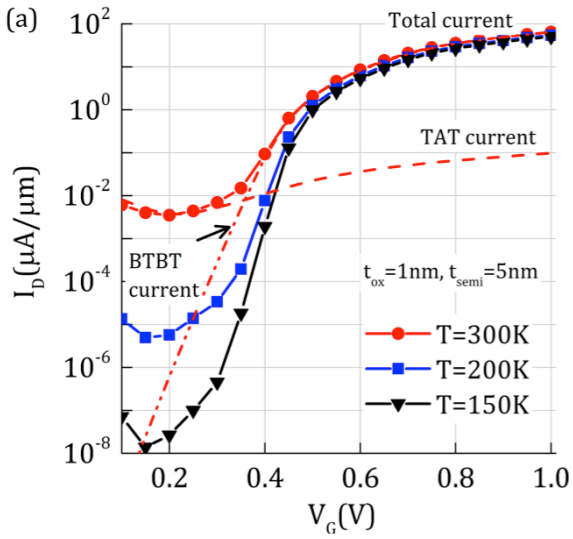
R. Sajjad, W. Chern, J. L. Hoyt, D. A. Antoniadis
Sponsorship: NSF E3S

Tunnel field-effect transistors (TFETs) are promising candidates for low-power logic applications. They have strong potential to reduce energy dissipation by relying on band-to-band tunneling (BTBT) for carrier injection to achieve steep turn-ON and thus reduce the logic circuit supply voltage. However, most experiments so far have failed to show subthermal switching.

In our model, we show that trap assisted tunneling (TAT) (Figure 1) due to surface interface traps is the principal mechanism of leakage current in TFETs. With a modified Shockley-Read-Hall formalism, we show that the TAT obscures the steepest part of the BTBT current for realistic trap densities. Through a multi-phonon process, an electron (or hole) can be emitted to a trap state, followed by tunneling into the conduction band (or the valence band for a hole), giving rise to the TAT. The minimum subthreshold swing (SS) is a combined result of the trap density, sharpness of the band edge (Urbach tail), and material parameters (Figure 2). We show that the TAT current is greatly enhanced with a high electric field in the tunnel barrier, in the same way as the desired BTBT current. Based on the detailed formalism, we build a physics-based compact model that is able to capture the SS, minimum current achievable at any given temperature, and the temperature-dependence of the transfer characteristics. All TFET device features such as negative differential resistance (NDR), superlinear ON current, and the drain control over the channel potential are captured through physical parameters. Our model a) matches closely with TFET experiments, b) captures the material and structural parameters that influence the TAT, and c) allows predictions of what trap density is needed to see subthermal switching.



▲ Figure 1: A schematic of a TFET and TAT.



▲ Figure 2: Total current in a homojunction III-V TFET in presence of TAT. The steepest part of the transfer curve is obscured by TAT.

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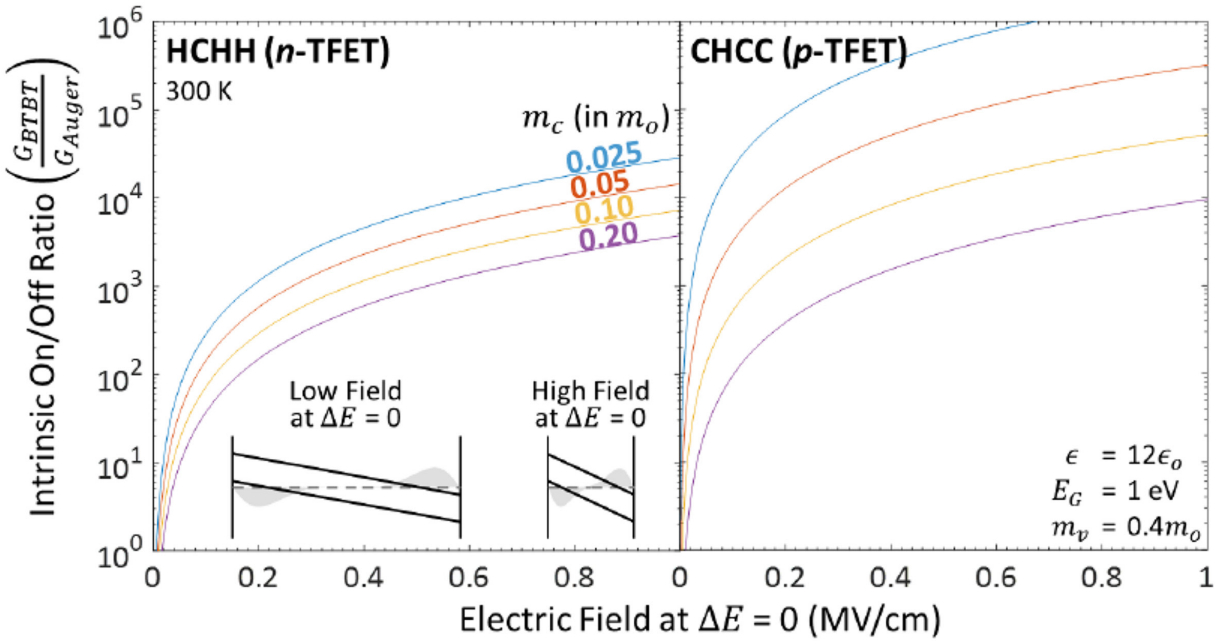
Auger Generation as an Intrinsic Limit to Tunneling Field-Effect Transistor Performance

J. T. Teherani, S. Agarwal, W. Chern, P. M. Solomon, E. Yablonovitch, D. A. Antoniadis
Sponsorship: NSF E3S

Many in the microelectronics field view tunneling field-effect transistors (TFETs) as society's best hope for achieving > 10× power reduction for electronic devices; however, despite a decade of considerable worldwide research, experimental TFET results have significantly underperformed simulations and conventional metal-oxide semiconductor FETs (MOSFETs). To explain the discrepancy between TFET experiments and simulations, we investigate the parasitic leakage current due to Auger generation, an intrinsic mechanism that cannot be mitigated with improved material quality or better device processing. We expose the intrinsic link between the Auger and band-to-band tunneling rates, highlighting the difficulty of increasing one without the other. From this link, we show that Auger generation imposes a fundamental limit on ultimate TFET performance.



▲ Figure 1: Intrinsic on/off ratio of the band-to-band-tunneling (BTBT) and Auger rates at eigenstate alignment ($\Delta E=0$) as a function of the electric field. The BTBT rate decreases dramatically as the field decreases, and therefore, the ratio drops. The relative permittivity (ε) and heavy-hole mass (m_v) do not vary significantly among materials; hence, constant values indicated on the plot are used. A 1-eV band gap is also assumed. The ratio depends linearly on $1/E_G$ so decreasing the band gap by half will double the on/off ratio. The CHCC process is one where an electron-hole pair is spontaneously generated by a high energy electron; the HCHH process is the opposite where an electron-hole pair is generated by a high energy hole. The CHCC process (dominant in p-TFETs with high n-doping) gives a much better on/off ratio because the Auger generation rate is much lower for the CHCC process due to the light electron mass. The inset shows the energy-band diagram for two structures with different body thicknesses at $\Delta E=0$. The thinner structure requires a higher electric field to align the bands, which results in an improved on/off ratio due to increased BTBT at high fields. The electric field at $\Delta E=0$ will also be dependent on the doping profile and electrostatics of the device, in addition to body thickness.

Simulation Study of the Performance of Negative Capacitance Field-Effect Transistors Using a Physics-Based Compact Model

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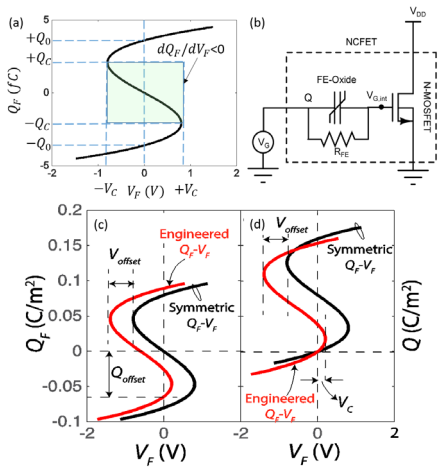
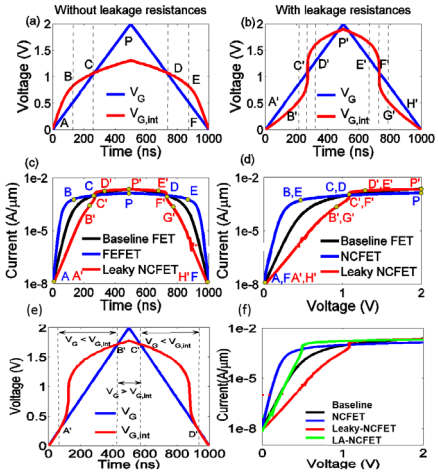
Sponsorship: NSF NEEDS, ONR, LEAST, SRC STARnet Center, MARCO, DARPA

There is an increasing need for semiconductor logic devices that can operate at scaled power supply voltage in digital computing systems for overall energy efficiency in electronics. A fundamental limitation on the scaling of supply voltage in CMOS technology is the Boltzmann limit of 60 mV/decade on the sub-threshold swing (SS) of field-effect transistors (FETs). The concept of negative capacitance (NC) FETs (NCFETs) has been proposed to overcome this limitation by using a capacitor with a ferroelectric material (FE-oxide), connected in series with the gate dielectric of a regular MOSFET. The underlying mechanism for sub-60 mV/decade operation of a NCFET is the passive amplification of the gate voltage at the interface between the FE-oxide and the semiconductor channel yielding steep-SS as the ferroelectric NC state cancels the equivalent of all the positive capacitances in NCFETs.

The FE -oxide capacitor with Q-V characteristics showing the NC-regime (where dQ_F/dV_F <0) in Figure 1-a is connected in series with the gate of a regular MOSFET to constitute the NCFET shown in Figure 1b. Simulations are conducted to study the performance of the NCFET by using the MVS-model calibrated against Intel 45-nm NFET connected to the FE-oxide capacitor as shown, including the scenario of FE-leakage through R_{FE}. Leakage shifts the Q-V characteristics by Q_0, stabilizing the FE-oxide in the positive-capacitance (PC) state, with the unintended consequence of decreasing the NCFET performance versus baseline MOSFETs. Work function engineering of the external and internal metal gates to shift the Q-V characteristics by V_{offset} as shown in Figure 1c-d restores the advantage of leaky-NCFETs in terms of steeper SS by stabilizing the FE-oxide close to the NC-regime (V_{offset}, Q_{offset}). Transient simulations for the triangular gate voltage on the NCFETs for leaky and non-leaky scenarios in Figure 2a-b show that the NC-state in segments AC and DF results in steeper-SS in the NCFET transfer characteristics versus baseline FETs, as Figure 2c-d shows. Leakage results in PC in the sub-threshold regime of the NCFET (in segments A'C' and H'F') yielding degraded SS. Leakage-aware design by work function engineering preserves lower SS along with higher I_{on} as seen in Figure 2e-f. The NCFET model implemented in Verilog-A can be a useful tool to design NCFET-parameters (t_{FE}, V_{offset}) and evaluate circuit-level performance of NCFETs.



▲Figure 1: (a) Q_F-V_F characteristics of a FE-oxide showing the NC-region. (b) The NC-state is stabilized with the gate-oxide of MOSFET forming the NCFET shown. (c)-(d) Leakage shifts the Q-V characteristics by Q_0 pushing it to the PC-state while LA-design by work-function engineering to shift the Q-V curves by V_{offset}, stabilizes the oxide to have charge of Q_{offset} closer to the NC-state.



▲Figure 2: (a)-(b) Internal gate-voltage ($V_{G,int}$) response to a triangular gate voltage in leaky and non-leaky scenarios showing amplification in certain segments. (c)-(d) NCFETs have steeper SS than the baseline while leakage eliminates this advantage. (e)-(f) LA-design preserves the NC-state stability in sub-threshold, yielding steeper SS to some extent and higher I_{on}.

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High Aspect Ratio InGaAs FinFETs with Sub-20 nm Fin Width

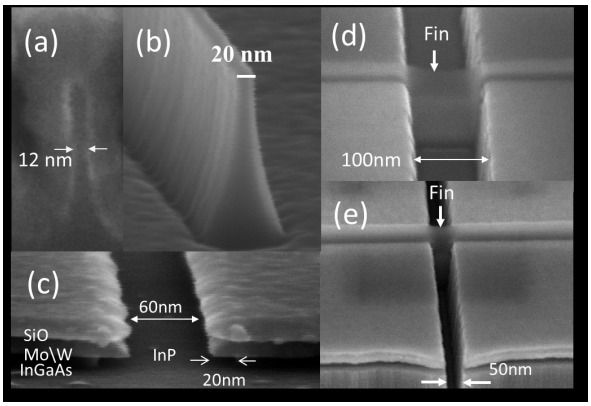
A. Vardi, J. A. del Alamo
Sponsorship: DTRA, NSF E3S, Lam Research

InGaAs is a promising candidate for channel material for CMOS technologies beyond the 10-nm node. In this dimensional range, only high aspect-ratio (AR) 3D transistors with a fin or nanowire configuration can deliver the necessary performance. Impressive fin- and nanowire-based InGaAs FinFET prototypes have recently been demonstrated. However, to date, InGaAs FinFETs with fin widths below 30 nm and channel aspect ratio better than unity have yet to be demonstrated. Furthermore, the channel sidewall slopes demonstrated so far are typically lower than 80°. At the point of insertion in a sub-10-nm node, InGaAs FinFETs with sub-10-nm fin widths and steep sidewalls will be required.

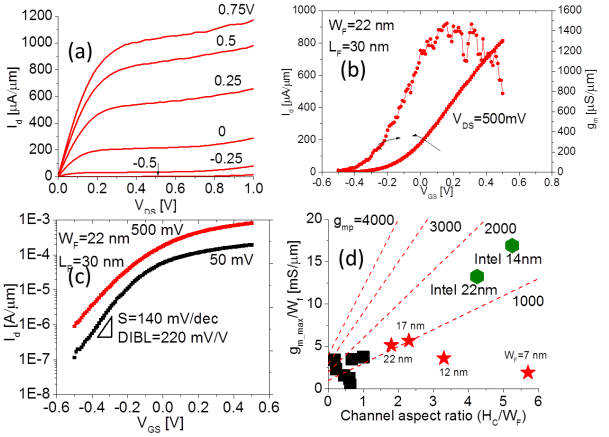
In this work, we present the first self-aligned InGaAs FinFETs with sub-20-nm fin width, high channel aspect ratio (H_c=40 nm), vertical sidewalls, gate lengths as short as 20 nm, and CMOS-type manufacturability. We use a top-down process based on reactive-ion etching (RIE) and digital etch. Our transistors are the most aggressively scaled InGaAs FinFETs to date.

The process is illustrated in Figure 1 and follows a flow developed for self-aligned planar InGaAs quantum-well MOSFETs. SEM images of sub-20-nm fin test structures are shown in Figures 1(a) and (b). Low-resistivity Mo is first sputtered as contact metal (R_{sh}=5 Ω/□), followed by SiO_2 CVD. The gate pattern is defined by E-beam lithography. The SiO_2 and Mo layers are then etched by RIE. After RIE mesa isolation, the top n^+ InGaAs cap is wet-etched in a well-controlled manner (see Figure 1(c)). Fins are then patterned using 40-nm-thick HSQ and E-beam lithography and RIE etched (see Figure 1(d)-(e)). This yields fins as narrow as 20 nm with an aspect ratio of 8. The fins are highly vertical in the top ~70 nm (Figure 1(b)). Gate dielectrics composed of 0.5 nm of Al_2O_3 and 2.5 nm HfO_2 are deposited by ALD. Sputtered Mo is used as gate metal and patterned by RIE. The device is finished by via opening and pad formation. In this process, the HSQ that defines the fin etch is kept in place. This feature makes our FinFETs double-gate transistors with carrier modulation only on the sidewalls.

The electrical characteristics of a device with W_f=22 nm L_g=30 nm (AR= H_c/W_f=1.8) are shown in Figure 2(a)-(c). Well-behaved characteristics and good sidewall control are obtained. R_{on} is 170 Ω·μm, and a peak transconductance, g_m, of 1400 μS/μm is obtained at V_{DS}=0.5 V. This value is comparable to the highest g_m obtained so far in InAs FinFETs with W_f=40 nm (AR=0.23). Figure 2 (s) shows a benchmark plot comparing normalized g_m per fin footprint of InGaAs FinFETs realized to date as well as commercial Si FinFETs.



▲ Figure 1: SEM image of self-aligned InGaAs FinFET. (a) cross section of gated fin, (b) stand-alone fin test structure, (c) gate area after recess, and (d) and (e) 100- nm and 50-nm gate length devices, respectively, after fin etch.



▲ Figure 2: (a) output, (b) transfer and (c) subthreshold characteristics of self-aligned InGaAs FinFET with L_g=30 nm and W_f =22 nm. (d) g_m per fin footprint as a function of AR= H_c/W_f for InGaAs (black), this work (red) and Si (green) FinFETs. Trend lines show the physical g_m of equivalent planar device.

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An InGaSb Tri-gate MOSFET

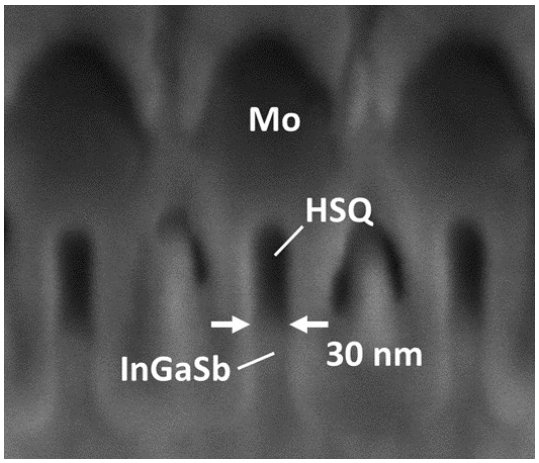
W. Lu, J. A. del Alamo
Sponsorship: Lam Research Corporation, Samsung Electronics

Recently, III-V multi-gate metal-oxide semiconductor field-effect transistors (MOSFETs) have attracted great interest to replace silicon in future CMOS technology. This is due to the III-V semiconductor's outstanding carrier transport properties. Although impressive n-type transistors have been demonstrated on materials such as InAs and InGaAs, research in III-V p-channel devices is lacking. The antimonide system, such as InGaShas the highest hole mobility among all III-V compound semiconductors; its hole mobility can be further improved by applying compressive strain. Therefore, InGaSb is regarded as one of the most promising semiconductors to replace p-channel Si MOSFETs.

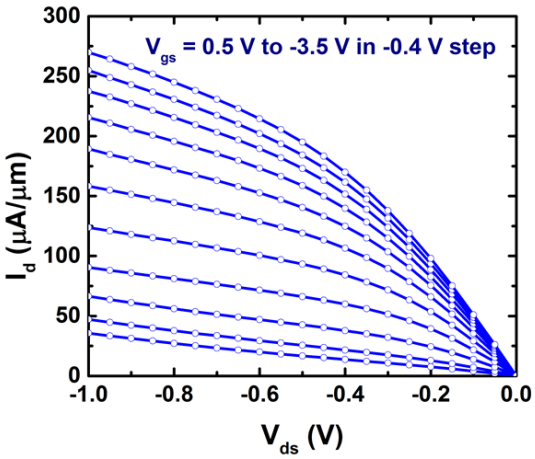
In this work, we have designed and demonstrated the first InGaSb p-channel FinFET. A FinFET is a nonplanar transistor in which the conducting channel sticks out of the wafer top in a similar way as the fin of a shark above the ocean surface. In a FinFET, the gate wraps around the fin, helping to reduce leakage current when the device is OFF and mitigating short-channel effects. The FinFET is the state-of-the-art transistor architecture in current Si CMOS technology and demonstration of III-V FinFETs is imperative.

In order to fabricate an InGaSb FinFET, we have developed two critical technologies. First, a high-aspect ratio dry etching process has been demonstrated. It can produce antimonide-based fins or nanowires as narrow as 15 nm with vertical sidewalls and low sidewall defects. Second, a Si-compatible nickelide ohmic contact scheme has been developed that offers an ultra-low contact resistivity of $3.5 \cdot 10^{-8}$ Ω-cm^2. With the aid of these two technologies, the first InGaSb p-channel FinFET has been fabricated with a narrowest fin width of 30 nm and total fin height of 150 nm, as shown in Figure 1. The output characteristics of a 30-nm wide FinFET with 100-nm gate length are shown in Figure 2. In this transistor, a transconductance, g_m, of 78 μS/μm is obtained. In devices of 100-nm fin width and 100-nm gate length, g_m of 122 μS/μm has been attained. This transconductance is about the same as in the best InGaSb planar MOSFETs. For the first FinFETs in this material system, this is a very encouraging result.

We are currently working on different approaches to achieve smaller device pitch and enhanced device characteristics. In particular, a passivation technology for InGaSb fin sidewalls is of great importance. Our research will be instrumental in mapping the potential of InGaSb for future CMOS nodes.



▲Figure 1: Focused-ion-beam cross-section image of a finished InGaSb FinFET with fin width of 30 nm.



▲Figure 2: Output characteristics of an InGaSb p-channel FinFET with fin width of 30 nm and gate length of 100 nm.

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Si Donor Passivation in InGaAs MOSFETs

X. Cai, J. Lin, J. A. del Alamo
Sponsorship: DTRA, Lam Research Corporation

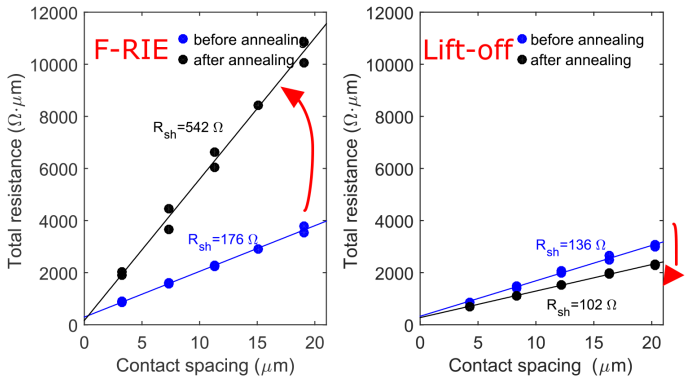
InGaAs is a promising n-channel material candidate for future CMOS technology due to its superior electron transport properties and low-voltage operation. While the process technology and performance of InGaAs metal-oxide semiconductor field-effect transistors (MOSFETs) continues to improve, there is increasing anxiety about the electrical reliability of this device technology. Issues of concern are reactive-ion etching (RIE) damage, ion contamination, radiation damage, trapping, etc. As F-based RIE is important for III-V device processing and F is known to passivate Si donors in n-InAlAs, a common material in InGaAs MOSFET heterostructures, it is important to verify and mitigate this potentially deleterious effect.

To investigate F^- induced donor passivation in our process, we have fabricated transmission line model (TLM) structures on a heterostructure that includes an n-InGaAs/n-InP/n-InAlAs (15/3/3 nm) cap, as shown in Figure 1. We use two different processes. A standard process that is the same as in our InGaAs MOSFET process uses sputtered Mo contacts etched by SF_6/O_2 RIE. In an alternative process, the Mo contacts are lifted-off, and there is no exposure to F.

Figure 2 shows the measurement results of the TLM structures before and after annealing at 350°C for 1 min. The pre-anneal sample prepared by F-RIE exhibits a semiconductor sheet resistance (R_{sh}) of 176 Ω/□, 30% higher than that of the lift-off sample. After annealing, R_{sh} of the lift-off sample decreases somehow, while R_{sh} of the F-RIE sample increases by 3X to 543 Ω/□. This result is consistent with literature findings that during a thermal step, F diffuses and passivates donors in n-InAlAs. Our standard self-aligned InGaAs MOSFET fabrication process includes a 340°C, 15-min thermal step after F-based RIE. Thus, we expect that F passivates Si donors in the n-InAlAs cap layer of the MOSFET and deteriorates device performance. Furthermore, F renders the device unstable as it tends to move around under an electric field.

Our work will be instrumental in enhancing the performance, reliability, and stability of future InGaAs MOSFETs.

▲ Figure 1: Cross-sectional schematic of TLM structure.



▲ Figure 2: TLM resistance versus measured contact distance before and after annealing on (left) samples that have undergone F-based RIE and (right) samples fabricated by lift-off in a F-free process.

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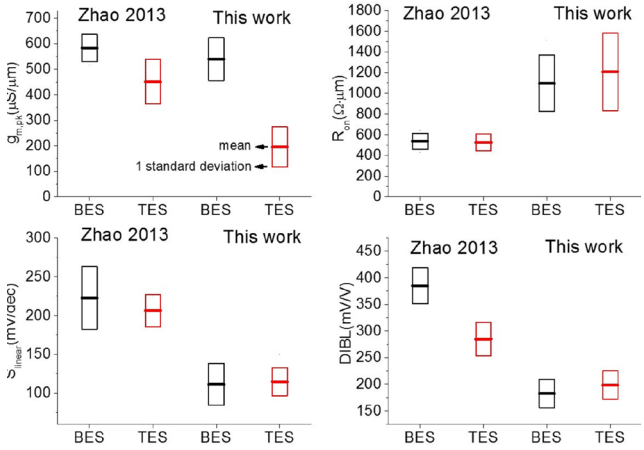
Source/Drain Asymmetry in InGaAs Vertical Nanowire MOSFETs

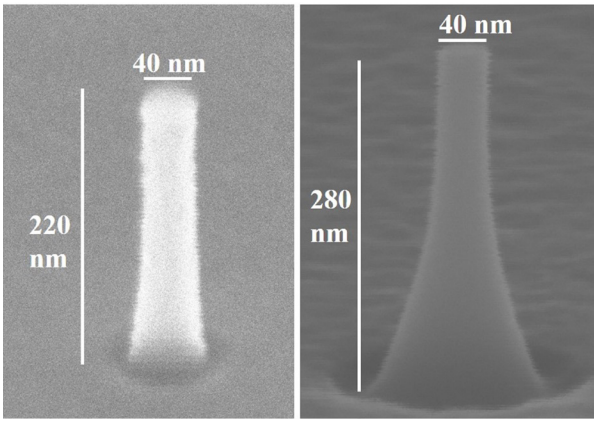
X. Zhao, C. Heidelberger, E. A. Fitzgerald, J. A. del Alamo
Sponsorship: NSF E3S, Lam Research, SRC

CMOS technologies beyond the 5-nm node not only require a highly three-dimensional transistor structure but also benefit from incorporation of new channel materials. InGaAs is considered a promising material candidate while the vertical nanowire MOS field-effect transistor (MOSFET) has been shown to offer better scalability when compared at the circuit level with horizontal nanowire devices. The vertical nanowire InGaAs MOSFET is, therefore, an interesting device technology worth investigating. An intrinsic feature of vertical devices is the asymmetry between source and drain contacts, which is absent in intrinsically symmetric horizontal devices. To date, this source/drain asymmetry has been studied only theoretically.

This work demonstrates InGaAs vertical nanowire MOSFETs fabricated via a top-down approach that achieves state-of-the-art performance in terms of the balance between transport and electrostatics. The much-improved device electrostatics compared to those of an earlier device generation (Further Reading 2) stem mainly from a better oxide/semiconductor interface, enabled by improved atomic layer deposition (ALD) chamber conditioning. These devices and those of an earlier generation have enabled the first experimental study of the impact of source/drain asymmetry in vertical nanowire MOSFETs by comparing device characteristics with bottom electrode as the source (BES) and top electrode as the source (TES). Figure 1 shows key electrical figures of merit measured in both configurations in devices from this work and a previous generation (Further Reading 2). The ON-current characteristics, assessed by the transconductance, differ significantly when swapping source and drain. This is due to the inherently different top and bottom contacts. g_m asymmetry is visible in both the present and previous work. On the other hand, the asymmetry in subthreshold characteristics (notably drain-induced barrier lowering or DIBL), prominent in earlier devices, is eliminated in this work. This lack is explained by simulations that show that diameter non-uniformity along the transport direction leads to asymmetry in electrostatics. The improved InGaAs dry etch technology used in this work delivers a uniform nanowire cross section that improves over prior work, as shown in Figure 2.



▲ Figure 1: Key electrical figures of merit of a number of devices measured in BES and TES configuration from our previous work in 2013 (below) and this work.



▲ Figure 2: Improved NW profile in this work (left) compared to our previous work referenced below (right).

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Fabrication of Test Structures for Measuring Contact Resistance of Vertical Nanowires

D. Choi, J. A. del Alamo
Sponsorship: ILJU Academy and Culture Foundation Fellowship, NSF E3S, Lam Research

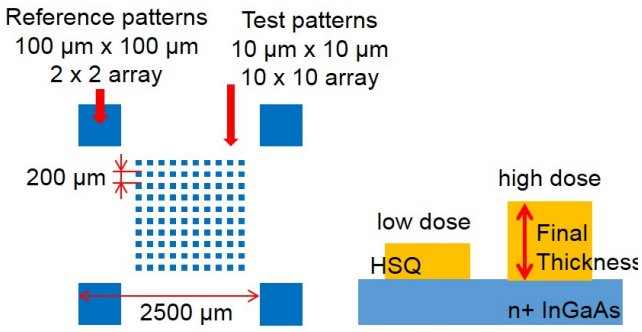
In modern transistors, the contact resistance to the source and drain has been increasing in importance as the device size has been decreasing. Although the traditional technique to measure contact resistance in planar devices, the transmission line method (TLM), is well developed, a similar technique for vertical nanowire (VNW) transistors, which are under intense investigation as next generation devices, does not exist. Our research aims to address this need.

Our test structure concept is based on a top-down nanowire fabrication approach. Once the nanowire has been etched, we need to form a thin insulating spacer on the surrounding field while preserving a clean nanowire sidewall. We are investigating hydrogen silsesquioxane (HSQ) to make this possible. The basic idea is that because HSQ is a negative electron-beam (e-beam) resist, adjusting the e-beam dose can control the final thickness after development.

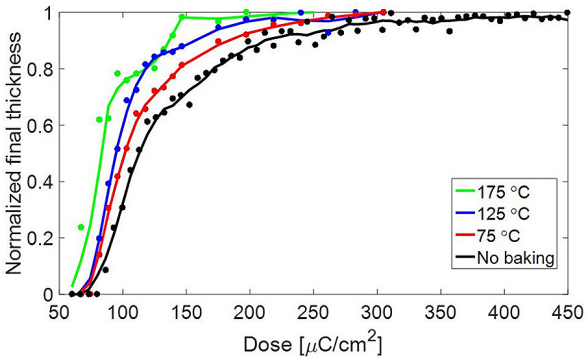
To explore this concept, we have performed e-beam dose test experiments using HSQ on n+ InGaAs. The e-beam lithography pattern consists of a ten-by-ten array of test squares and a two-by-two array of reference squares (left in Figure 1). In each test pattern, the e-beam dose is increased from one end to the other.

An example of the final thickness of HSQ as a function of e-beam dose is shown in Figure 2 (black). For HSQ, FOX 16 (HSQ from Dow Corning) is used after mixed with methyl isobutyl ketone in a 2:1 ratio. The final thickness of HSQ in the exposed area increases as e-beam dose increases, and the film is hardened, as expected (right in Figure 1). Beyond a dose of around 300 μC/cm², the entire film thickness is hardened, and its final thickness saturates to the original thickness of the HSQ film. The threshold dose beyond which the final HSQ thickness is finite is about 80 μC/cm². The threshold dose is the criterion for sensitivity of HSQ; as the threshold dose increases, the sensitivity decreases.

The results of this calibration experiment suggest that to control the final thickness of HSQ through the e-beam dose, the linearly dependent portion of Figure 2 between about 80 μC/cm² to 300 μC/cm² should be used. Also, to control the final thickness easily, the slope of the linear portion of the curve needs to be reduced. We have explored processing conditions that enable this reduction. For example, Figure 2 shows data for various temperatures of a baking step after e-beam lithography. As the baking temperature increases, the slope increases, which is undesirable. We are currently exploring other process parameters to obtain improved thickness control of HSQ films. This technique should allow the fabrication of insulating layers of controlled thickness at the bottom of etched nanowires.



▲ Figure 1: Left: Test and reference patterns fabricated in this work. Right: Illustration of final thickness dependence of HSQ after low and high e-beam dose and subsequent development.



▲ Figure 2: Effect of temperature of baking after e-beam lithography on the final thickness of HSQ normalized to its initial value.

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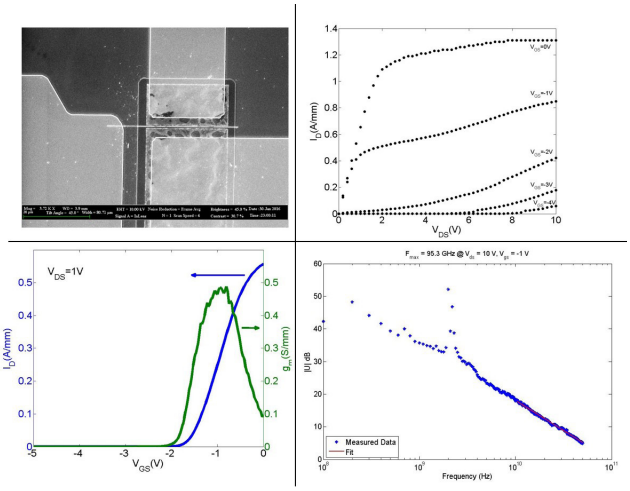
Gallium Nitride Low-Voltage Devices and Technology Development for GaN Circuits

D. Piedra, T. Palacios
Sponsorship: Lincoln Laboratory, Masdar Institute of Science and Technology

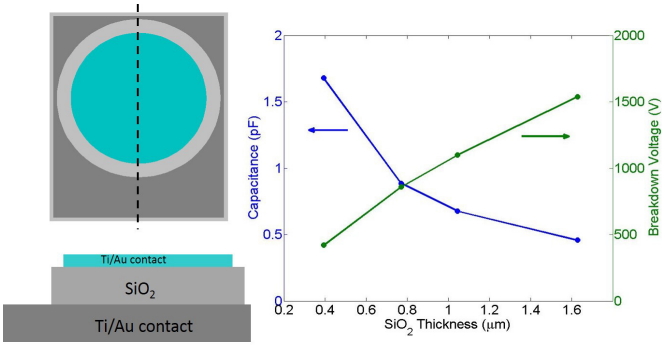
Gallium nitride has found an active avenue in the application spaces of RF and power electronics for mid- to high-voltage areas. However, a somewhat unexplored area is that of low-voltage power electronics, where silicon, due to its high integration density, low cost, and years of technological maturity, still reigns supreme. In this project, we explore, through modeling and experimentation, the design space of low-voltage power electronics and gauge the feasibility of using GaN for such applications. We will see the limitation, which may restrict performance in this space, and examine what improvements would need to be made to have the biggest impact on device performance for low-voltage switching.

Using empirical results from devices designed for RF applications, we model to see if such devices could be competitive with Si low-voltage devices and to determine potential problems or limitations. The initial test device was an InAlGaN/GaN HEMT grown on SiC substrate. The fabricated devices had Lg=90 nm and an array of different gate widths.

Finally, we have fabricated and tested structures to satisfy the requirements of the passive components. We have fabricated capacitors using the dielectrics that are to be used in the device process as passivation or interlayer dielectric layers and confirmed that the employed thickness can meet capacitance and breakdown requirements. Also, an initial batch of thin film resistors has been fabricated from evaporated NiCr metal showing a resistivity of 36Ω/sq.



▲Figure 1: InAlGaN/GaN HEMT with Lg=90 nm and F_{max}=95.3 GHz. This device will serve as the initial test device to obtain empirical measurements on which to build the model for a low-voltage switching device.



▲Figure 2: Test SiO_2 capacitors fabricated out of the device passivation and interlayer dielectric layers.

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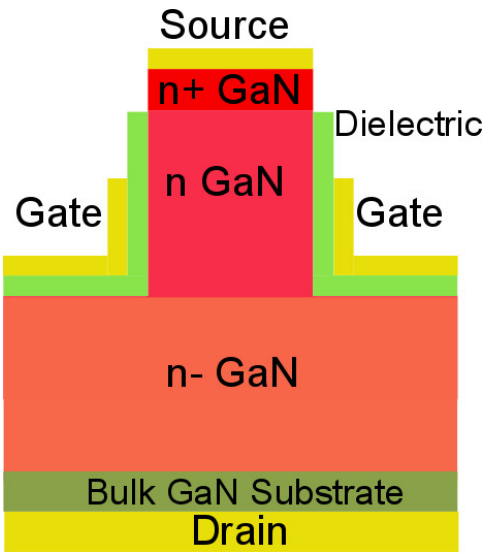
Vertical GaN Power Transistors on Bulk GaN Substrate

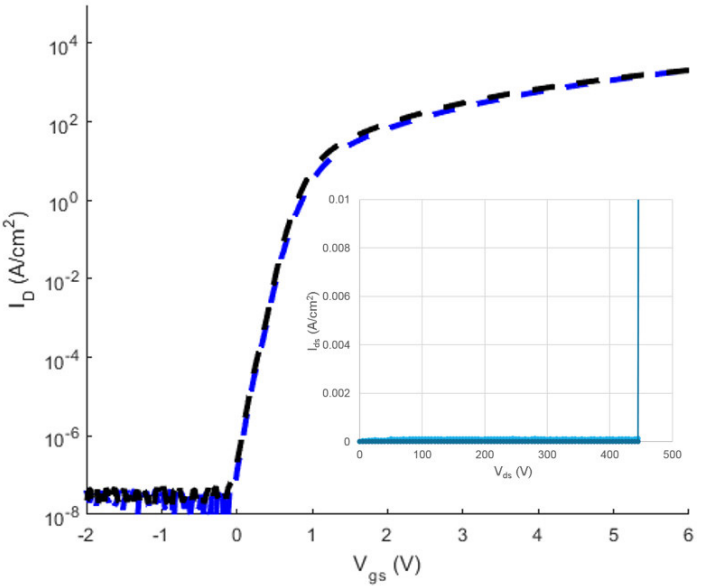
M. Sun, T. Palacios
Sponsorship: ARPA-E SWITCHES

The ideal power switch combines a high breakdown voltage and a low on-resistance, R_{on}. Gallium nitride, GaN, due to its high critical field and electron mobility, has superior R_{on} compared to Si for a given breakdown voltage. Now lateral GaN transistors on Si substrates, with operating voltage less than 650 V, are commercially available. The main drawback of the lateral geometry is, however, that the transistor area is proportional to the breakdown voltage. In addition, numerous material interfaces are exposed to high electric fields. For higher-voltage high-current applications, the device size increases dramatically. A vertical device would significantly reduce the die size, as this size would not depend on the breakdown voltage.

The most studied vertical GaN transistor, the current aperture vertical electron transistor (CAVET), has made significant progress in performance, but it still faces great challenges. The CAVET structure requires a p-doped current- blocking layer buried in the n-doped GaN layer. Activating the p-dopant magnesium in GaN has been found very challenging. Also, it needs a high-quality regrowth of the AlGaN/GaN layer, making it expensive. Our work has developed a novel vertical Junction Field Effect Transistor (JFET) structure to address the challenge mentioned above. As shown in Figure 1, the current flows from the drain to source vertically through a sub-micron-channel, which is surrounded by the metal gate pads. Below the threshold voltage, the channel electrons are depleted due to the work-function difference between the gate metal and GaN. Figure 2 shows the transfer characteristics of the new vertical GaN JFET with channel length 0.4 μm. The current on/off ratio is ~ 10^{11}. The device shows a 0.5-V threshold voltage, defined at $I_{on}/I_{off} = 10^5$. The subthreshold swing of the device is less than 100 mV/dec. The hysteresis is very small, which demonstrates the excellent material quality of the wet etched sidewall. The VFET broke down at V_d = 450 V measured at V_{gs} = 0 V.



▲ Figure 1: Structure of a Vertical GaN JFET on bulk GaN substrate.



▲ Figure 2: Transfer IV characteristics of a vertical GaN JFET with 0.4-μm channel length. The drain voltage is 10 V. The inset figure shows the breakdown curve at V_{gs} = 0 V.

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Origin of Off-State Leakage in GaN Vertical Power Diodes

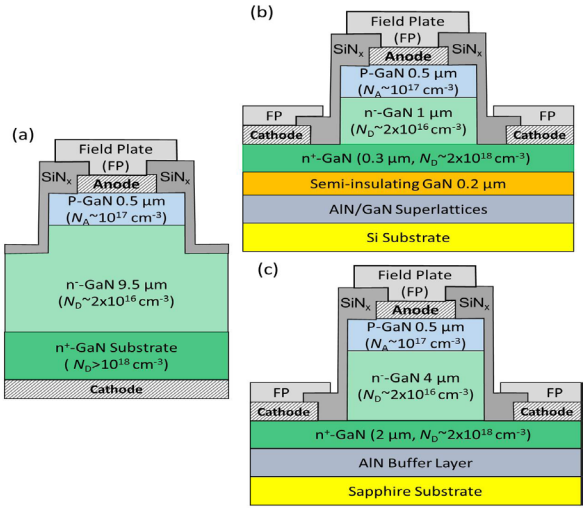
Y. Zhang, M. Sun, T. Palacios
Sponsorship: ARPA-E SWITCHES

GaN transistors and diodes are excellent candidates for high-power electronics. Currently, both lateral and vertical GaN devices are being considered. Specifically, vertical devices have attracted increased attention, due to several potential advantages over lateral devices: 1) higher breakdown voltage (BV) without enlarging chip size, 2) superior reliability, and 3) enhanced thermal performance. Recently, high-performance GaN vertical devices have been demonstrated on GaN, sapphire and Si substrates with over 3.7 kV BV and lower leakage than GaN lateral devices.

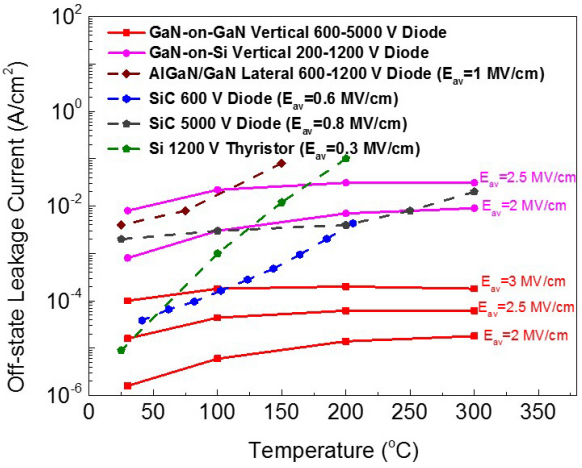
Off-state leakage current is a key factor determining the device BV, power circuit loss and, potentially, reliability. However, the physical mechanisms and the design space of the leakage current in GaN vertical devices are still unknown.

In this work, we fabricated GaN vertical diodes on different substrates and then unveiled the leakage mechanism by analytical analysis and TCAD simulation. Finally, the design space of leakage current in GaN vertical devices was derived and benchmarked with GaN lateral, Si, and SiC devices.

GaN vertical p-n diodes were fabricated on GaN, sapphire, and Si substrates with similar doping levels in p-GaN and n-GaN drift layers (Figure 1). To identify the bulk leakage mechanism, correlations between leakage current I and the average electric field in the drift layer (E_{av}) were studied. According to the I *vs.* E_{av} relationship, variable-range-hopping through dislocations was identified as the main off-state leakage mechanism for GaN vertical diodes on different substrates. The behavior of leakage current for vertical devices as a function of dislocation density and electric field was derived by TCAD simulations, after careful calibration with experimental and literature data. The designed GaN vertical diodes demonstrate 2-4 orders of magnitude lower leakage current while supporting 3-5 times higher electric field, compared to GaN lateral, Si and SiC devices (Figure 2).



▲ Figure 1: Schematic of GaN vertical p-n diodes on (a) GaN, (b) Si, and (c) sapphire substrates, fabricated at MIT MTL.



▲ Figure 2: Off-state leakage current vs. temperature of the designed GaN-on-GaN vertical diodes and GaN-on-Si vertical diodes, benchmarked with the reported lateral GaN diodes, SiC 600 V and 5000 V diodes, and Si 1200 V thyristors.

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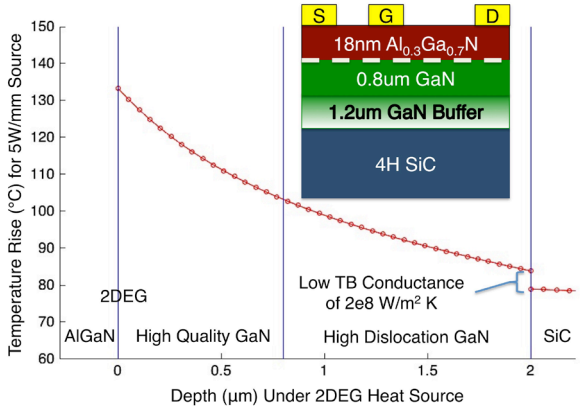
Near-Junction Thermal Management in GaN HEMTS via Wafer Bonding

R. M. Radway, T. Palacios
Sponsorship: Masdar Institute of Science and Technology

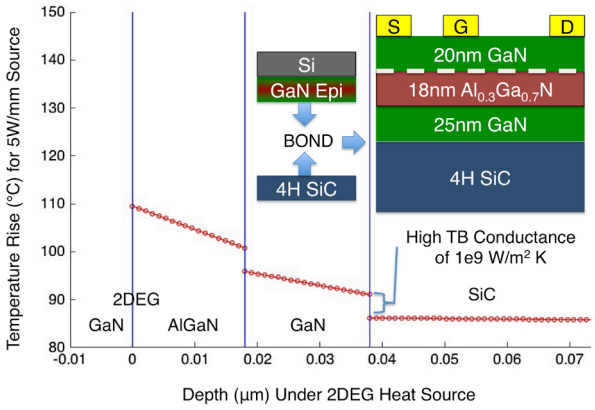
Gallium nitride (GaN)-based high electron mobility transistors (HEMTs) offer excellent performance for use in power conversion, high-frequency power amplifiers, and radar applications. However, operating temperatures effectively limit output power to 5W/mm from the reported maximum of 40W/mm. Thermal management is, therefore, critical for reliable high-power use. Our current research focuses on developing effective thermal models and scalable fabrication techniques to aid in solving these thermal management problems in GaN HEMT design.

Using an analytical solution for temperature rise in multilayered epitaxial structures, we evaluated several standard GaN-on-silicon, GaN-on-silicon carbide (SiC), and GaN-on-diamond epitaxial structures as well as novel structures formed via waferbonding. Going beyond structure, we modeled thermal conductivity reduction and thermal-boundary resistances for the materials in question. In determining these parameters, we considered non-classical effects due to scale and material quality. Phonon mean free path reduction due to diffuse boundary scattering decreases thermal conductivities of thin epitaxial layers. We calculated thermal-boundary resistances using a diffuse mismatch model, but these values are highly dependent on interfacial material quality; interfaces between low-quality material near growth origination will have higher resistivities than those further from nucleation due to GaN crystal dislocations caused by lattice mismatch. These constraints suggest that thermally optimal interfaces are formed by directly bonding high-quality materials from the final layers of epitaxial growth to thermally conductive substrates such as SiC (Figure 2).

We examined several designs based on GaN-SiC direct bonding, etching away of poor material and interfaces, and subsequent device fabrication on the high-quality material remaining. The novel structure shown below improved thermal performance compared to a standard epitaxial structure (Figures 1 and 2). We are currently researching methods for wafer bonding of GaN and SiC to achieve this efficient design. Plasma surface activation shows promise, and we are focused on using these bonding techniques for device fabrication, with the end goal of experimental verification of simulated improvements.



▲ Figure 1: GaN-on-SiC structure grown via MBE; simulated temperature rise of vertical locations under the right edge of gate with device dissipation 5W/mm.



▲ Figure 2: Novel GaN-on-SiC structure fabricated via wafer bonding; simulated temperature rise of vertical locations under the right edge of gate with device dissipation 5W/mm.

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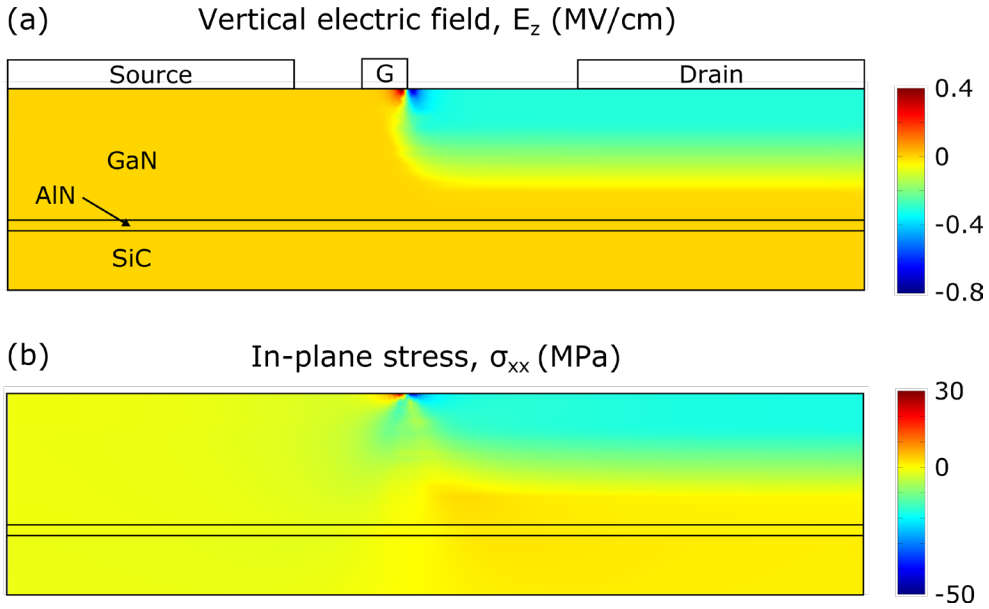
Impact of the Inverse Piezoelectric Effect on Micro-Raman Thermography in GaN HEMTs

K. R. Bagnall, E. N. Wang
Sponsorship: MIT/MTL Gallium Nitride (GaN) Energy Initiative, SMART LEES

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are one of the most promising compound semiconductor technologies for solid-state high-frequency power amplifier (PA) and high-voltage power conversion applications. However, the high power densities present in GaN HEMTs often lead to high channel temperatures, which must be accurately characterized and managed to maximize device reliability and performance. Over the last fifteen years, micro-Raman thermography has emerged as one of the most reliable and popular techniques for measuring the channel temperature in GaN HEMTs with high spatial (~1 μm) and temporal (~10 ns) resolution.

Despite the many advantages of micro-Raman thermography, temperature measurements based on the change in Raman peak position associated with the Stokes (phonon emission) process are also affected by the thermoelastic and inverse piezoelectric (IPE) effects. A number of studies have shown that using the pinched-off state as the unpowered reference for micro-Raman thermography effectively removes the impact of IPE-induced strain/stress. Yet quantitative values of the strain, stress, and electric field components derived from micro-Raman spectroscopy measurements of GaN HEMTs biased in the pinched-off state disagree in sign and order of magnitude with those predicted by electro-mechanical modeling.

Using both electro-mechanical device modeling and very high precision micro-Raman spectroscopy, we are investigating the response of the Raman spectrum of the GaN buffer in GaN HEMTs to strain, stress, and electric field induced in the pinched-off state. Thus far, our work has shown that experimental data from previous studies predict the in-plane stress and vertical electric field to be an order of magnitude larger than our electro-mechanical model. We believe that these discrepancies can be resolved by considering the impact of the electric field on the optical phonon frequencies apart from the IPE effect, which we aim to demonstrate experimentally for the first time.



▲ Figure 1: (a) Vertical electric field and (b) in-plane stress predicted by a semiconductor device electro-mechanical model of a GaN HEMT under bias in the pinched-off state. The vertical electric field component in the gate-drain access region is negative, resulting in a compressive in-plane stress.

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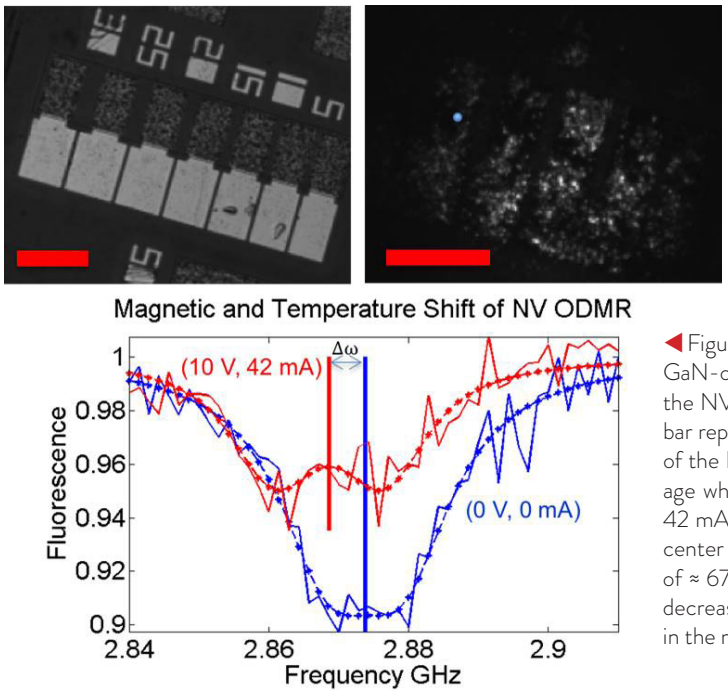
Imaging Current Distributions and Temperature Profiles in GaN HEMTs using Nitrogen Vacancy Centers in Nanodiamonds

C. Foy, K. R. Bagnall, M. E. Trusheim, A. Lauri, E. N. Wang, D. R. Englund
Sponsorship: EFRC Center for Excitonics, NSF

Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are a leading solid-state technology for microwave power amplifiers for a range of applications. However, the high power densities in GaN HEMTs often lead to electronic junction temperatures in excess of 200 ˚C. Such high temperatures accelerate device degradation. In this work, we introduce a wide-field temperature and magnetic measurement technique with simple instrumentation and calibration procedures for GaN electronics characterization. This technique is based on nanoscale spin-based thermometry using NV centers in nanodiamonds.

NV centers, under ambient conditions, enable optically detected magnetic resonance (ODMR) and can provide sub-wavelength imaging. These properties allow the NV to make highly localized simultaneous measurements of temperatures and magnetic fields. Such measurements are accomplished by determining the NV's ground state spin electron levels, which respond to the changes in the NV's local magnetic and thermal environment. Determining the position of these electron spin sublevels is accomplished by measuring the ODMR spectra on standard microscopes.

We deposited NVs onto the surface of an ungated GaN-on-sapphire HEMT so that they are within ~30 nm of the HEMT channel. In Figure 1 we measure the magnetic field and temperature across an NV by applying the model described previously and observe an increase of 67 ˚C and 3.4 G as 10 V and 42 mA are applied across the ungated GaN HEMT. These wide-field temperature measurements allow us to determine the location and value of the peak junction temperature of the GaN-on-sapphire HEMT. The current density distribution is then subsequently calculated from the magnetic field distribution. NV centers offer robust, wide-field temperature and current measurements with simple instrumentation and are a promising addition to the repertoire of thermal and magnetic imaging.



◀Figure 1: Top Left: Bright field image of a series of ungated GaN-on-sapphire HEMTs. Top Right: Fluorescence image of the NV centers on top of the ungated GaN HEMTs. The scale bar represents 100 μm in both images. Bottom: ODMR curves of the NV located at the point marked in the fluorescence image when the device is unpowered (blue curve) and 10 V and 42 mA are applied (red curve). The change in frequency of the center of the ODMR curve ($\Delta\omega$) represents a temperature rise of ≈ 67 °C across the NV center. Further, the broadening and decrease in amplitude of the distribution represent an increase in the magnetic field of 3.4 G across the NV.

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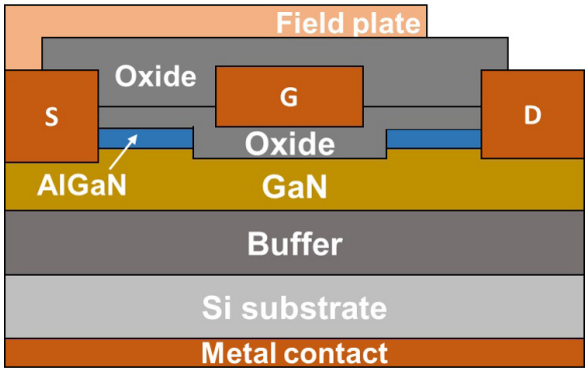
Negative-Bias Temperature Instability in GaN Power Field-Effect Transistors

A. Guo, J. A. del Alamo
Sponsorship: MIT/MTL Gallium Nitride (GaN) Energy Initiative, NDSEG Research Fellowship

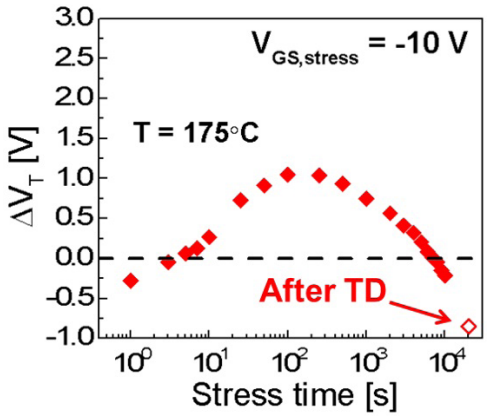
Gallium nitride (GaN) field-effect-transistors (FETs) are promising for replacing silicon in power electronics. For high-voltage applications, GaN-high electron mobility transistors with insulated-gate (GaN MIS-HEMTs) are especially attractive because the added insulator suppresses gate leakage and allows for larger gate swing, both essential for high-voltage performance. However, reliability issues surrounding GaN MIS-HEMTs are major roadblocks for technology commercialization. For example, threshold voltage (V_T) instability as a result of negative gate stress at elevated temperature (referred to as negative-bias temperature instability, or NBTI) is a serious concern. NBTI is studied in silicon transistors but much less well understood in GaN MIS-HEMTs. Addressing this issue is challenging because the many layers and interfaces of a MIS-HEMT structure make identifying the physical origin of NBTI difficult. Here, we study GaN metal-oxide-semiconductor FETs (MOSFETs) (Figure 1), which allow us to focus on stability issues associated with the oxide and the oxide/GaN interface.

We used a benign characterization scheme, also utilized in our earlier studies on positive-bias temperature instability (PBTI). We carried out experiments with gate stress ($V_{GS,stress}$) between -1 V and -70 V, stress time (t_{stress}) between 1 and 10,000 seconds, and temperature (T) between -40°C and 175°C. Our study shows that NBTI in GaN MOSFETs progresses through three regimes. Figure 2 shows this progression. A device was subjected to $V_{GS,stress}$ = -10 V at T = 175°C for 10,000 s. As t_{stress} increases, V_T first shifts negative, then positive, and then negative again. At the end, we see a negative V_T shift that is non-recoverable after thermal detrapping.

After many detailed experiments, we identified three mechanisms responsible for V_T shift of GaN MOSFETs due to NBTI. Under low-stress (regime 1), a small, negative V_T shift that is completely recoverable is observed. This shift can be modeled using a well-established oxide-trapping model. We then conclude that electron detrapping from pre-existing oxide traps is likely to be responsible for this shift. For mid-stress (regime 2), a recoverable positive V_T shift is observed. We attribute this behavior to trapping in the GaN channel. The high vertical electrical field in the channel under the gate edges causes electron trapping in deep levels within the GaN band gap, which appears as a temporarily increased doping level. For high-stress (regime 3), there is an additional negative V_T shift that is non-recoverable and that is accompanied by permanent subthreshold swing degradation. These observations strongly suggest the generation of interface states. Our findings should be instrumental in understanding the instability of GaN MIS-HEMTs.



▲ Figure 1: GaN MOSFET structure studied in this work.



▲ Figure 2: Stress time evolution of ΔV_T for GaN MOSFETs with SiO_2/Al_2O_3 as gate dielectric for $V_{GS,stress}$ = -10 V at 175°C. Filled symbols are the total ΔV_T extracted 1 sec after stress, and open symbol are the non-recoverable ΔV_T after a thermal detrapping (TD) step.

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Progressive Breakdown in High-Voltage GaN Field-Effect Transistors

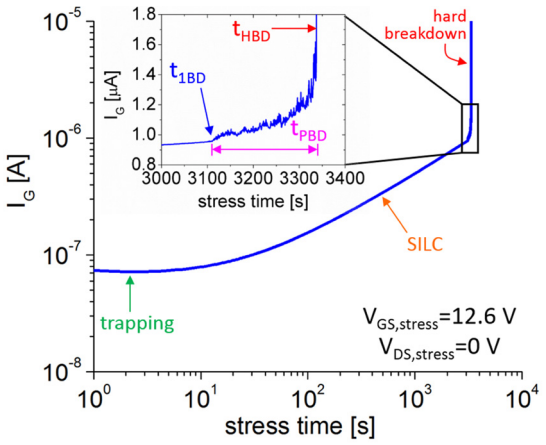
S. Warnock, J. A. del Alamo
Sponsorship: Texas Instruments

As the demand for more energy efficient electronics increases, GaN field-effect transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN power transistors are ready for commercial deployment. One of the concerns is gate dielectric reliability as a result of high-voltage stress. In particular, after prolonged high-voltage gate bias stress, the dielectric will suffer from catastrophic breakdown beyond which the transistor is no longer operational.

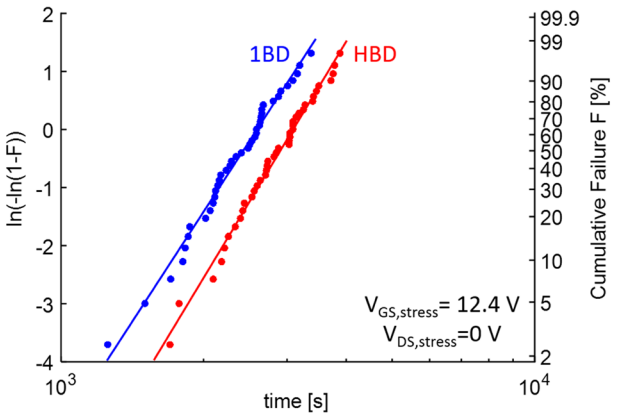
Our research is directed to providing fundamental understanding behind the physics of time-dependent dielectric breakdown (TDDB) of the gate dielectric in GaN metal-insulator-semiconductor high-electron-mobility transistors (MIS-HEMTs), the most promising transistor structure for power electronics. We focus here in particular on a regime of breakdown known as progressive breakdown, or PBD. As this condition at times takes place soon before the complete breakdown of the gate dielectric, studying PBD could provide valuable insight into the hard breakdown (HBD) physics. Figure 1 shows the evolution of the gate current, I_G, in a typical constant-voltage TDDB experiment. We can observe first a decrease in current due to trapping and then an increase in what is known as stress-induced leakage current (SILC). The inset shows that near the final catastrophic breakdown (or HBD), I_G becomes noisy, a condition known as progressive breakdown (PBD). The time at which the noise appears is denoted as time-to-first-breakdown, t_{1BD}.

Figure 2 shows the statistical distribution of both hard breakdown and first breakdown in a number of transistors. TDDB statistics are typically shown on a Weibull plot, where F is the cumulative device failure for a given time. The nearly parallel slopes for t_{1BD} and HBD suggest the two have a common physical origin.

Through experiments such as these, we hope to gain an understanding of the fundamental mechanisms behind dielectric breakdown as well as build models that allow us to predict device lifetime under realistic operating conditions.



▲ Figure 1: Gate current as function of stress time during constant $V_{GS,stress}$ TDDB experiment. FET is held at $V_{GS,stress}$=12.6 V until device breaks down. $V_{DS,stress}$=0 V. Inset shows detail of I_G evolution right before HBD. Clear onset of noise in I_G marks the start of PBD.



▲ Figure 2: Weibull plot of t_{1BD} and t_{HBD}. $V_{GS,stress}$=12.4 V, $V_{DS,stress}$=0 V. Nearly parallel statistics for t_{1BD} and HBD suggest a unified degradation mechanism.

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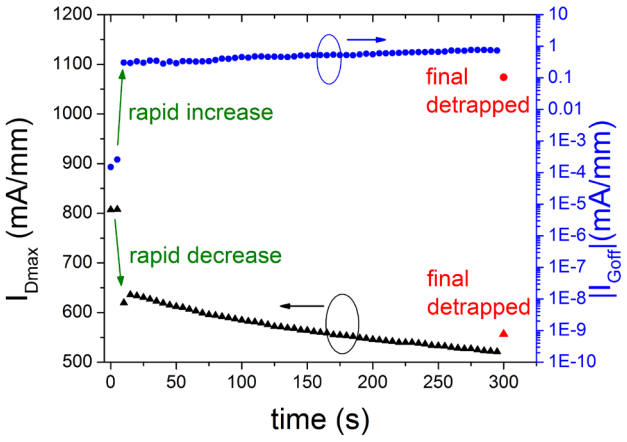
Gate Stack Degradation of InAlN/GaN HEMTs for RF Applications

Y. Wu, J. A. del Alamo
Sponsorship: National Reconnaissance Office

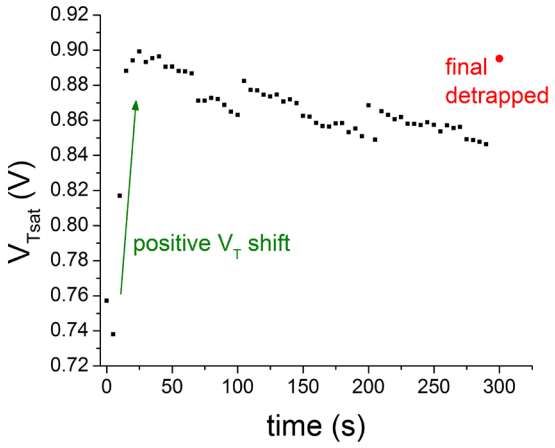
First demonstrated in the 1990s, GaN transistors have become commercially available in recent years. Compared with other commonly used materials such as Si and GaAs, GaN devices can operate at higher voltages and frequencies, thus enabling significant improvements in power efficiency and a dramatic reduction in size.

In contrast to the conventional GaN HEMT with AlGaN as barrier layer, the use of an InAlN barrier yields, for the same layer thickness, a higher spontaneous polarization-induced charge at the barrier/GaN interface. This enables aggressive barrier thickness scaling and therefore greater gate length scaling. As a result, InAlN/GaN HEMTs are extremely promising for very high frequency applications. However, unlike the better understood AlGaN/GaN system, the dominant degradation mechanisms in InAlN/GaN HEMTs are not well established. Our project aims to study the leading degradation modes of InAlN/GaN HEMTs under different stress conditions with the ultimate goal of constructing models to predict device lifetime.

After exploring various stress conditions, we have identified a common pattern of degradation in which a significant increase in gate leakage current takes place together with a drain current decrease (see Figure 1). Further study revealed two degradation mechanisms at play: one is responsible for the rapid degradation of gate and drain currents (first few seconds in Figure 1) as well as a positive shift of threshold voltage (first few seconds in Figure 2). Pure thermal stress experiments (not shown here) have led us to believe that the rapid degradation could be caused by gate sinking, essentially a reaction at the gate metal/semiconductor interface that reduces the Schottky barrier height. In transmission electron microscopy images of stressed devices, we have also observed the appearance of a disordered region in the semiconductor channel under the gate metal, which is consistent with our hypothesis. A second degradation mechanism is responsible for the longer-term continued degradation of the currents (Figure 1) as well as the negative shift of V_T (Figure 2). This mechanism could be trapping and/or the creation of new traps.



▲ Figure 1: Evolution of I_{Dmax} (@ V_{DS} = 4 V, V_{GS} = 2 V) and I_{Goff} (@ V_{DS} = 0.1 V, V_{GS} = -2 V) under high-power stress. During the first few seconds, a rapid drain current decrease and a gate current increase occur. Following this, device degradation continues at a much slower rate.



▲ Figure 2: Evolution of threshold voltage under high-power stress. An initial increase takes place within the first few seconds. After that, V_T shifts in the negative direction.

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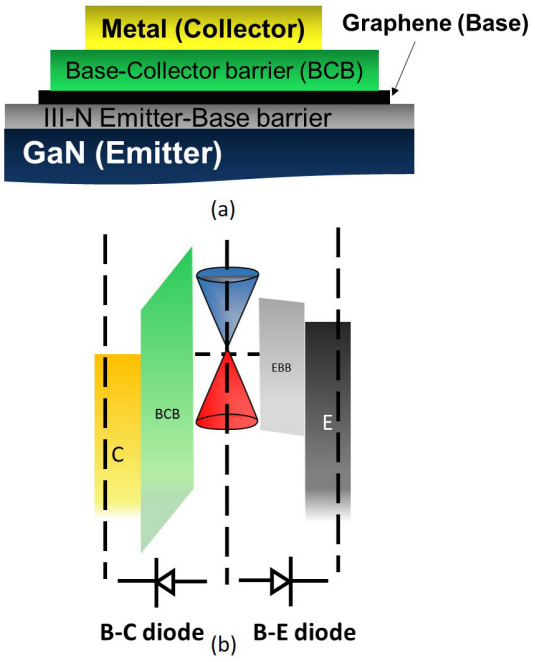
Characterization of Graphene/GaN Heterojunction Diodes for Graphene-on-GaN Hot Electron Transistor

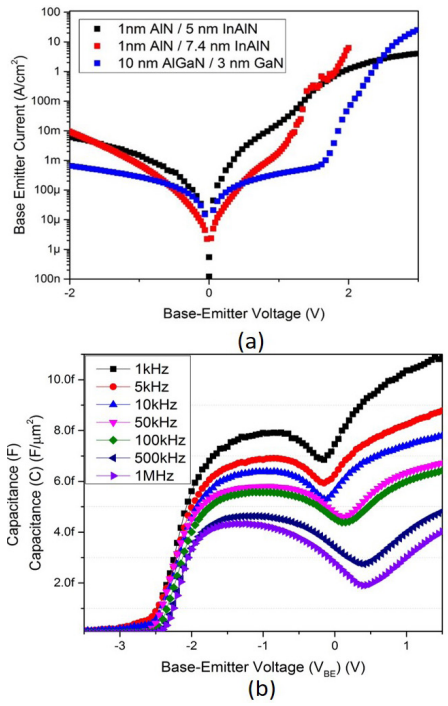
A. Zubair, A. Nourbakhsh, J. Y. Hong, J. Kong, M. Dresselhaus, T. Palacios
Sponsorship: U.S. Army Research Office

Hot electron transistors (HETs) are promising devices that may enable high-frequency operation that currently CMOS cannot provide. In an HET, carrier transport is due to injection of hot electrons from an emitter to a collector, which is modulated by a base electrode. Therefore ultra-thin base electrodes are needed to facilitate ultra-short transit time and high performance for a THz operation range. In this regard, graphene, the thinnest conductive membrane in nature, is considered the best candidate for the base material in HETs.

We previously demonstrated a vertical graphene-on-GaN HET with a record current density and current saturation. Nevertheless, the device showed a relatively high turn-on voltage due to relatively thick barrier. To reduce the turn-on voltage and enhance the tunneling current, a thinner emitter-base barrier is needed. In this work, we use a 1 nm/ (5 nm or 7.4 nm) AlN/InAlN heterostructure instead of the 15 nm/3 nm AlGaN/GaN barrier that was used previously. The current-voltage characteristics show that the turn-on voltage decreases significantly with barrier thickness (Figure 2 (a)). The measured current density (~10 A/cm² at 2V) in the modified graphene-GaN HET is comparable to the values reported in the literature for all-GaN HETs. Our capacitance-voltage (C-V) study of graphene/AlN/InAlN/GaN structures shows good interface between graphene and AlN/InAlN barrier. The C-V measurement (Figure 2(b)) shows a clear transition from depletion to accumulation for a typical GaN-based capacitor. The valleys at the accumulation region correspond to the graphene quantum capacitance, which is in series with the barrier capacitance. The presence of this feature indicates strong Fermi-level modulation in graphene near its Dirac point.



▲Figure 1: (a) Schematic cross section of a typical graphene-on-GaN hot electron transistor. (b) Qualitative energy band diagram of an HET showing base-emitter and base-collector diode components.



▲Figure 2: (a) Base-emitter transport characteristics of graphene/GaN heterojunction diode for different barrier thickness. (b) Capacitance-voltage characteristics of graphene/GaN heterojunction.

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Monolayer MoS_2 FETs with Sub-10-nm Channel Formed by Directed Self-Assembly

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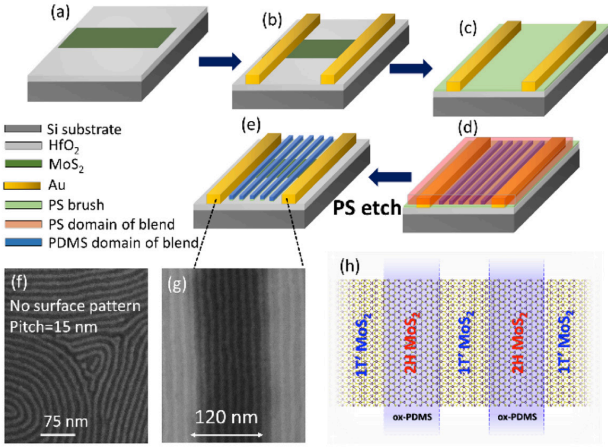
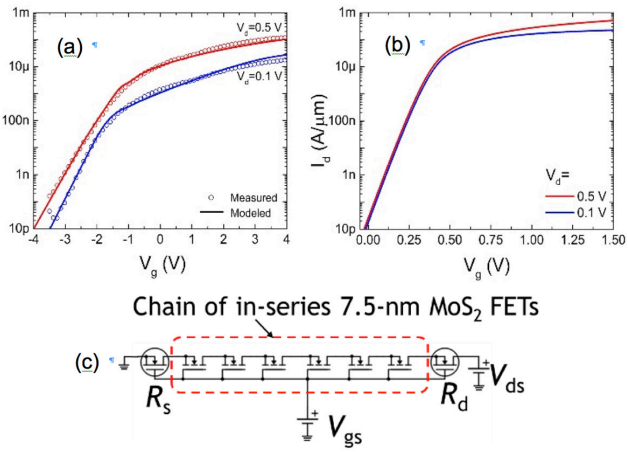
Sponsorship: ONR, U.S. Army Research Office

2D crystals of layered transition metal dichalcogenides such as molybdenum disulfide (MoS_2) are ideal candidates for aggressive miniaturization of field-effect transistors (FETs) to the single-digit-nanometer scale. Beyond having a large bandgap, chemical stability, and compatibility with CMOS processes, this class of materials can benefit from their atomically thin body with dangling-bond-free surfaces. Because of this and their ultra-small body thickness, the transistor subthreshold swing (SS) and drain-induced barrier-lowering (DIBL) coefficient in such films can be significantly smaller than for conventional thin-body semiconductors. In particular, monolayer-MoS_2 (ML-MoS_2), because of its bandgap of 1.8 eV yields high I_{on}/I_{off} ratio FETs, while its low dielectric constant, ε_s = 4-7, and atomically thin body, t ≈ 0.7 nm, facilitate the reduction of characteristic scaling length.

We previously reported a 15-nm channel length MoS_2 FET using monolayer graphene as the source/drain (S/D) contacts. Here, by exploiting the semiconducting to metallic phase transition in MoS_2, we demonstrate a 7.5-nm transistor channel length by patterning of ML-MoS_2 in a periodic chain of homojunction semiconducting- (2H) and metallic-phase (1T') MoS_2 regions. The 2H- to 1T'-phase transition occurs by exposing 2H-MoS_2 to *n*-butyl lithium solution. Sub-10-nm 1T'/2H MoS_2 patterning is achieved by directed self-assembly of block copolymers (BCP: PDMS/polystyrene) technique, as shown in Figure 1. Figure 2 shows the transfer characteristics of the MoS_2 transistor chain at different V_d values and the model fit to the data using the MIT Virtual Source model (MVS). The transistor chain shows I_{on}/I_{off} ≈10^6 with I_{off} ≈100 pA/μm. Modeling of the resulting characteristics reveals that the 2H/1T' MoS_2 homojunction has a resistance of 75 Ω.μm while the 2H-MoS_2 exhibits low-field mobility of ~8 cm^2/V.s and carrier injection velocity of ~10^6 cm/s.



▲Figure 1: (a-e) Schematics depicting the different steps of the DSA of BCP on MoS_2 FETs. (f, g) SEM images show PDMS lines with 15-nm pitch after polystyrene etch on surfaces with no guide pattern as well as surfaces with Au lines as directional guides. (h) Schematic short channel FET comprised of a 2H-MoS_2 channel contacted to two adjacent metallic 1T'-MoS_2 regions forming S/D contacts.



▲Figure 2: (a) Id-Vg of a 6-transistor array at different V_d values and MVS fit of the experimental data. (b) Performance prediction of a single transistor with a double-gate structure, EOT of 0.5 nm, and with the same device parameters but assuming excellent contact resistance (R_s=R_d=100 Ω.mm). Threshold voltage is adjusted to +0.5V for this plot. (c) Circuit configuration used MVS modeling.

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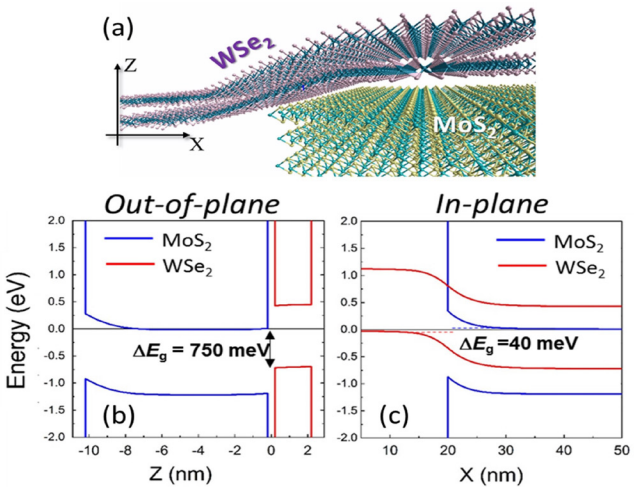
A MoS_2/WSe_2 van der Waals Heterojunction Tunnel Diode

A. Nourbakhsh, A. Zubair, M. S. Dresselhaus, T. Palacios
Sponsorship: U.S. Army Research Office, ONR

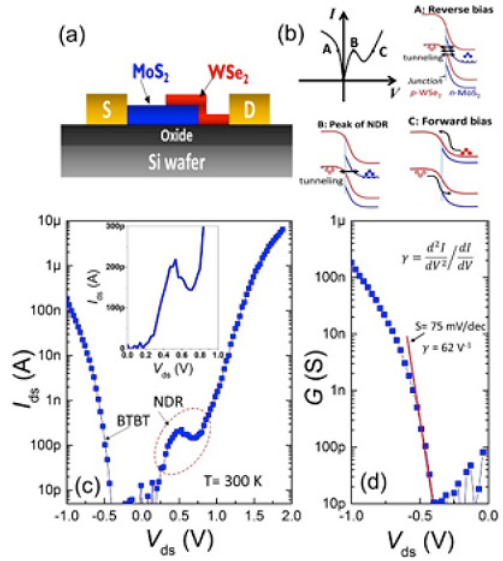
Two-dimensional (2D) crystals based on atomically thin films of layered semiconductors, such as the family of transition metal dichalcogenides (MX_2: MoS_2, WSe_2, $SnSe_2$, etc.), offer an attractive platform for various optoelectronic applications. The unique crystal properties of atomically thin 2D crystals make them particularly attractive for heterojunction devices, which can potentially overcome some of the problems that conventional heterostructure devices face. A very promising field of application for van der Waals (vdW) heterostructures of 2D crystals is as band-to-band tunneling (BTBT) devices for low-power applications. Such vdW heterostructures can benefit from atomically sharp interfaces and no dangling bonds. These features are crucial for tunneling devices that suffer from impurities and interfacial defects.

To obtain a better understanding of BTBT in MoS_2/WSe_2 hetero-diode, the energy band diagram of the MoS_2/WSe_2 heterostructure was calculated and compared in the out-of-plane and in-plane directions to evaluate the possibility of BTBT in different regions and directions (Figure 1). The results show that the effective heterojunction bandgap at the edge of the overlapped region of *n*-MoS_2 and *p*-WSe_2 in the horizontal direction is significantly smaller than their bandgap in the overlapped region, in the out-of-plane direction (40 meV *vs.* 750 meV). These results indicate that the BTBT occurs dominantly at the edge rather than, as is commonly believed, the overlapped region of the MoS_2/WSe_2 heterojunction.

Next, a MoS_2/WSe_2 heterodiode was designed and fabricated. We observe, for the first time, room-temperature negative differential resistance (NDR) in a heterodiode comprised of 2nm-WSe_2 stacked on 10-nm MoS_2. The presence of NDR is attributed to the lateral BTBT at the edge of the MoS_2/WSe_2 heterojunction. The diode shows an average conductance swing voltage of 75 mV/dec with a high curvature coefficient of 62 V^{-1} (Figure 2). This work represents the remarkable potential of 2D crystals-based heterostructures for high-performance tunneling devices.



▲ Figure 1: (a) Schematic of a MoS_2/WSe_2 heterostructure. (c) Calculated band diagrams of 10 nm-MoS_2/ 2 nm-WSe_2 heterojunctions in the out-of-plane and in-plane directions. The WSe_2 charge density is $5\times10^{18}/cm^3$, the MoS_2 charge density is $1\times10^{19}/cm^3$, and the MoS_2/WSe_2 gap is 4 Å, assuming the vdW gap between the two films.



▲ Figure 2: (a) Schematic of a MoS_2/WSe_2 hetero- diode (b) Schematic band diagrams of a MoS_2/WSe_2 junction at different bias regimes. (c) Absolute current, I_{ds}, and (d) conductance, $G=I_{ds}/V_{ds}$, versus V_{ds} of a 10-nm MoS_2/2 nm WSe_2 heterodiode. The inset in (c) shows $I_{ds}-V_{ds}$ at the NDR region with a linear scale.

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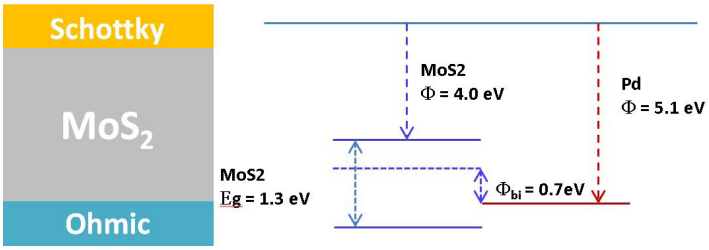
MoS_2-Based Two-Dimensional Radio Frequency Rectifiers

X. Zhang, J. Grajal de la Fuente, U. Radhakrishna, A. Zubair, A. Nourbakhsh, X. Ling, X. Ji, L. Zhou, J. Kong, M. Dresselhaus, T. Palacios
Sponsorship: ARL

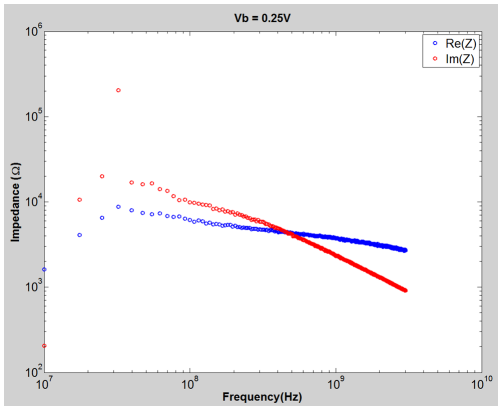
The development of autonomous flexible electronic systems is still not possible, even though thin-film electronics have experienced rapid progress recently. One of the key missing components is a flexible rectifier that can operate fast enough to enable wireless communication and RF energy harvesting. The critical frequency for these applications is 2.45 GHz, since our smart phones, GPS, Bluetooth, Wi-Fi, and many other communication systems all utilize this radio frequency. In this work, we are developing a MoS_2-based Schottky diode rectifier and improving its cut-off frequency to GHz range.

The cutoff frequency of a Schottky diode can be determined by $f_T = 1/2p*R_s*C_j$, where R_s is the series resistance and C_j is the junction capacitance. Figure 1 illustrates the structure of our MoS_2 device structure. Both Au and Pd exhibit n-type behavior as MoS_2 metal contacts. Gold deposited at high vacuum is good for Ohmic contact, while the Pd metal enables Schottky contact with MoS_2 with a built-in potential around 0.7 eV. The band alignment diagram of MoS_2 and Pd metal contacts is also illustrated in Figure 1.

To study the high frequency performance of the MoS_2 Schottky diode, we did S-parameter measurements by using a vector network analyzer. The S parameter of the diode was converted to Z-parameter and the real/imaginary part of the diode impedance was plotted in Figure 2. The cutoff frequency can be determined by the crossing point of the Re{Z} and Im{Z} curves. At a forward bias of 2.5V, the cutoff frequency can reach ~500MHz (Figure 2). The equivalent circuits of the internal part of a MoS_2 Schottky diode can be modeled as a junction resistance R_s in shunt with a junction capacitance C_j. At radio frequency, the impedance of the junction capacitance $1/jwC_j$ will roughly "short" the impendence of R_j. Therefore, at radio frequency, the series resistance R_s, instead of R_j, is the most significant limiting factor.



▲ Figure 1: Illustration of MoS_2 device structure and band alignment diagram.



▲ Figure 2: The real (red dots) and imaginary (blue dots) part of the impedance of the MoS_2 diode. The cutoff frequency f_T can be determined by the crossing point of the Re{Z} and Im{Z}.

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Control of Heating Dynamics in Superconducting Thin-Film Niobium Nitride Nanowires by Resistive Shunting

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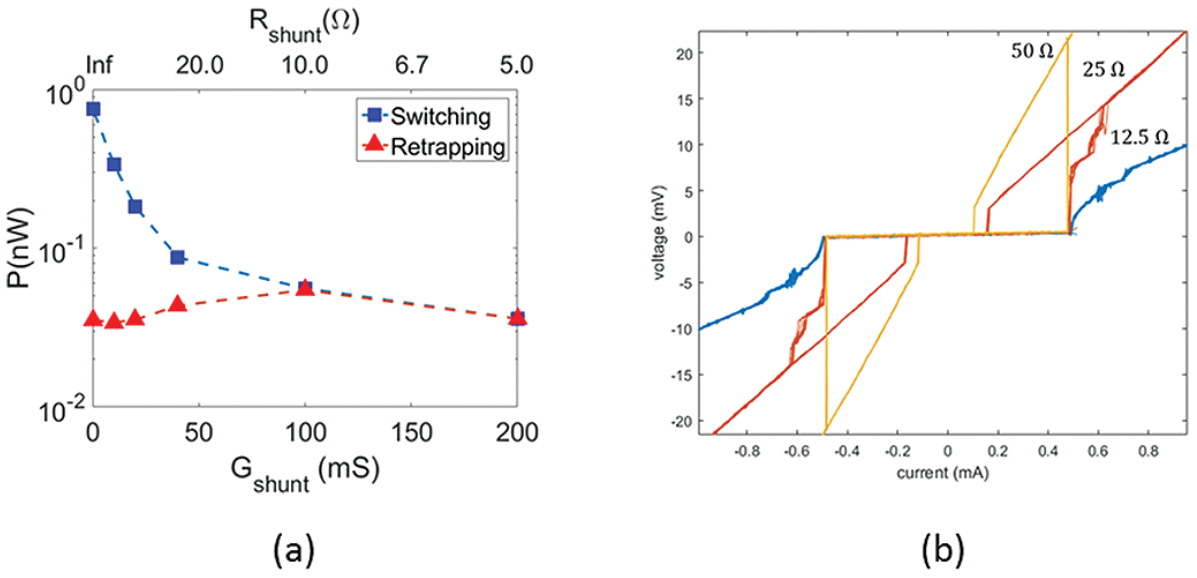
Sponsorship: IARPA, AFOSR, NSF, Intel

We have demonstrated the use of resistive shunting on thin-film NbN nanowires to control the heating dynamics of a three-terminal superconducting device. The nanocryotron (nTron) is a T-shaped device consisting of a channel, which can be switched from the superconducting state to the normal state by the injection of hot quasiparticles from the gate through the channel once the gate current exceeds the critical current density. Unlike Josephson junctions, this device can be fabricated from a single thin-film layer, produces large output voltages (>100 mV), and offers a third terminal for gate modulation, which can be triggered by a single flux quantum input. However, the heating dynamics of the nTron limit its speed and power efficiency while also preventing precise control of the phase difference between its terminals.

To overcome these limitations, we have investigated the impact of resistive shunting on thin-film NbN constrictions as a model for controlling the thermal dynamics of the nTron. Using the RCSJ model to approximate the phase-slip center in these superconducting nanowires as a weak link, we have simulated the suppression of hysteresis that results from increased damping of the constriction as the magnitude of shunt resistance decreases. We also evaluated the change in Joule heating power at the time of switching to demonstrate the decrease in hotspot formation caused by the diversion of bias current to the shunt. Experimentally, we have confirmed these results and characterized the change in switching and retrapping current distributions to determine the appropriate shunt resistance needed to preserve coherence in the resistive state. Extending this knowledge to the nTron could change its operation from a Joule-heated state governed by hotspots to a non-hysteretic, coherent mode controlled by single vortex crossings. We expect to use our results for applications such as reading out the discrete number of fluxons in a superconducting loop for single-flux quantum logic.



▲ Figure 1: (a) Simulated switching and retrapping power of a shunted nanowire. Power at switching decreases with decreasing shunt resistance. (b) Experimentally observed suppression of hysteresis as a function of shunt resistance for thick-film NbN (R_{sheet} = 59 Ω/square). Full suppression is seen at R_s = 12.5 Ω.

FURTHER READING

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