Electronic Devices: Transistors; Memory, Magnetic, and Superconducting Devices

Efficient Device and Integrated Circuit Statistical Modeling and Extraction Using a Bayesian Inference Framework

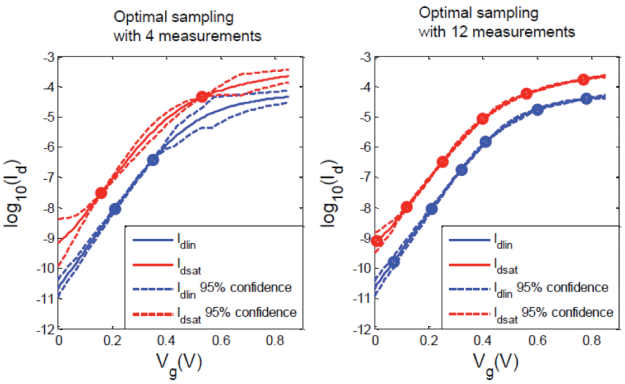
L. Yu, I. Elfadel, D. A. Antoniadis, D. S. Boning
Sponsorship: Masdar Institute/MIT Cooperative Program

Variability modeling and extraction in advanced integrated circuit technologies is a key challenge to ensure robust circuit performance as well as high manufacturing yield. We have developed an efficient framework for device and circuit variability modeling and extraction by combining ultra-compact transistor and timing models with Bayesian extraction methods. The compact models used here include the MIT virtual source (MVS) MOSFET model and a recent analytical model for gate timing characterization. Based on statistical extensions of these models, we propose algorithms for three applications that greatly reduce the time and cost required for measurement of on-chip test structures and characterization of library cells.

A critical problem in design for manufacturability (DFM) is to build statistically valid prediction models of circuit performance based on a small number of measurements taken from a mixture of on-chip test structures. Towards this goal, we have developed a technique named physical subspace projection to transfer a mixture of measurements into a unique probability space spanned by the MVS parameters. We search over MVS model parameter combinations to find those with the maximum probability by extending the expectation-maximization (EM) algorithm and iteratively solve the resulting maximum a posteriori (MAP) estimation problem. Finally, we develop a process shift calibration technique to estimate circuit performance by combining SPICE simulation and very few new measurements.

We further develop the parameter extraction algorithm to enable us to accurately extract all current-voltage (I-V) parameters given limited and incomplete I-V measurements, applicable to early technology evaluation and statistical parameter extraction. An important step in this method is the use of MAP estimation, where past measurements of transistors from various technologies are used to learn the *a priori* distribution and its uncertainty matrix for the parameters of the target technology. We then utilize Bayesian inference to facilitate extraction of *a posteriori* estimates for the target technologies using only a very small set of additional measurements. The proposed extraction approach can also be used to characterize the statistical variations of MOSFETs, with the significant benefit that some constraints required by the backward propagation of variance (BPV) method are relaxed. We study the lower bound requirement for number of transistor measurements to extract the full set parameters from a compact model, and propose an efficient algorithm for selecting the optimal measurement biases by minimizing the average output measurement uncertainty (Figure 1).

Finally, we have developed a flow to enable computationally efficient statistical characterization of delay and slew in standard cell libraries. We utilize a novel ultra-compact, analytical model for gate timing characterization. Instead of exploiting the sparsity of the regression coefficients of the process space with a reduced process sample size, we exploit correlations between different input vectors using a Bayesian learning algorithm, enabling us to estimate the parameters of the aforementioned timing model using past library characterizations along with a very small set of additional simulations.



▲ Figure 1: Confidence intervals on Idlin and Idsat estimates for transistor compact model fitting, as a function of optimally selected measurement voltage bias points.

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Impact of Intrinsic Channel Scaling on InGaAs Quantum-Well MOSFETs

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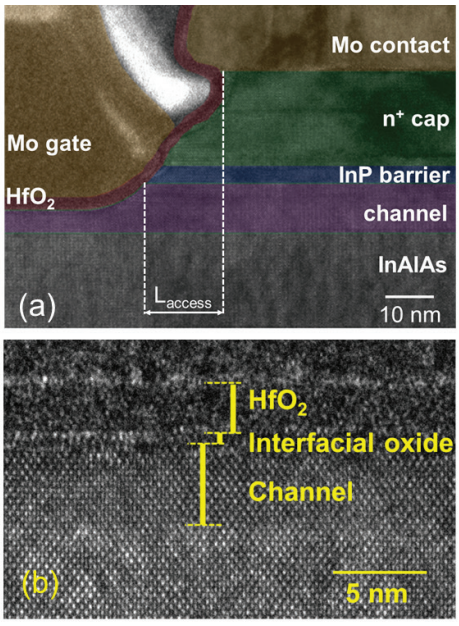
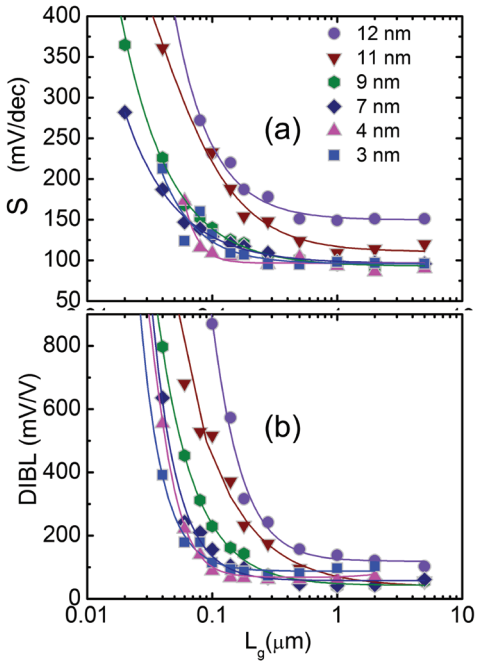
Sponsorship: Defense Threat Reduction Agency, E3S STC, Singapore-MIT Alliance, SMART

InGaAs is a promising candidate as an n-type channel material for future CMOS due to its superior electron transport properties. We have developed a novel self-aligned recessed-gate fabrication process for scaled InGaAs quantum-well MOSFETs (QW-MOSFETs). The fabrication sequence yields precise control of all critical transistor dimensions. Figure 1 (a) shows a cross-sectional transmission electron microscopy (TEM) image of the transition region between the intrinsic channel on the left and the extrinsic region on the right in a finished device. The contact is very close to the gate with an access region length (L_{access}) of 15 nm. Figure 1 (b) shows that a uniform channel and a flat surface are obtained in the intrinsic portion of the device. The channel is 7 atomic monolayers thick, which agrees with our targeted channel thickness for this device of 4 nm and showcases the excellent control accuracy of our process.

Our precise fabrication technology has allowed us to carry out a detailed scaling study of these devices. It is found that a thick channel is beneficial for ON-state figures of merit including transconductance and ON resistance. However, a thin channel is beneficial for OFF-state metrics such as subthreshold swing (S) and drain-induced barrier lowering (DIBL). S and DIBL in Figure 2 follow classic scaling behavior: they are both independent of gate length (L_g) for long L_g but degrade rapidly as L_g scales down beyond a certain value. The onset of S and DIBL degradation occurs at longer gate lengths for devices with thicker t_c. The InGaAs QW-MOSFET shown here is at the limit of scaling around L_g=50 nm, which indicates the need for appropriate transistor redesign and advanced 3D device architectures to deliver further progress.



▲Figure 1: (a) TEM cross-section of a finished InGaAs QW-MOSFET around the edge of the gate. The access region (L_{access}) is indicated. (b) High-resolution TEM (HRTEM) cross-section of the intrinsic region.



▲Figure 2: Experimental S and DIBL as a function of gate length (L_g) for channel thickness t_c =3 nm to 12 nm.

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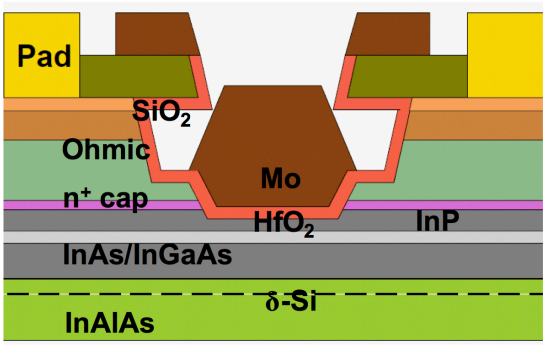
Electrical Reliability of InGaAs MOSFETs

X. Cai, J. Lin, J. A. del Alamo
Sponsorship: Defense Threat Reduction Agency

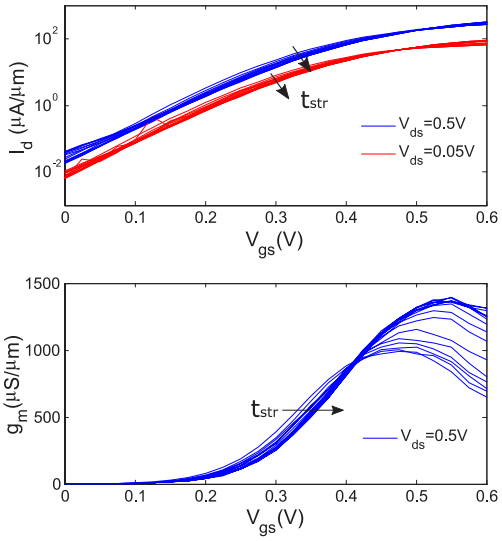
InGaAs is a promising n-channel material candidate for future complementary metal–oxide–semiconductor (CMOS) technology due to its superior electron transport properties and low voltage operation. While the process technology and performance of InGaAs metal–oxide–semiconductor field-effect transistors (MOSFETs) continue to improve, there is increasing research interest in developing fundamental understanding behind the electrical reliability of this device technology. Several recent studies have observed threshold voltage shifts and transconductance changes under various voltage stress conditions. Understanding, modeling, and mitigating these effects is of great relevance.

To understand the impact of voltage stress on InGaAs MOSFETs and its physical origin, we have developed an automated stress-characterization measurement scheme. A constant bias is applied to the device and periodically interrupted for I-V characterization. This allows us to study the evolution of device behavior during stress. After reaching the total stress time, the voltage stress is removed and I-V measurements are taken periodically to study the device recovery. A thermal step is used to restore the device to its initial condition before applying a different stress condition.

The InGaAs quantum-well MOSFETs used in this study are fabricated by a self-aligned gate-last process. The gate insulator is 2.5-nm HfO_2, deposited by atomic layer deposition (ALD) at 250°C. Figure 1 shows the cross section schematic of a typical device. Figure 2 shows the evolution of subthreshold and transfer characteristics of a device during stress at V_{gs}=1 V and V_{ds}=0 V at room temperature. As stress time increases, the threshold voltage shifts positively and the peak transconductance increases. Contrary to most other studies, where the transconductance is observed to degrade, we have observed a 40% enhancement of the peak transconductance at the end of the two-hour stress period. Understanding the physical mechanism behind this transconductance enhancement will allow us to explore options to stabilize the device and furthermore might provide us with process technology suggestions to improve device performance.



▲Figure 1: A cross-sectional schematic of the InGaAs MOSFET used in this study.



▲Figure 2: Evolution of subthreshold (top) and transfer characteristics (bottom) during stress at V_{gs}=1 V and V_{ds}=0 V for two hours at room temperature.

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A New Emission-Diffusion Virtual Source Field-Electron-Transmitter Model

S. Rakehja, M. Lundstron (Purdue U.), D. A. Antoniadis
Sponsorship: National Science Foundation NEEDS program

A new physics-based compact model valid from drift-diffusive to ballistic carrier transport regimes was implemented in close collaboration with Professor Lundstrom of Purdue University. This model, called the virtual-source emission-diffusion (VSED) model, is similar to the ED model for Schottky barriers but incorporates the metal-oxide semiconductor electrostatics. The VSED model provides a description of the current at any drain bias without empirical fitting and predicts the injection velocity of carriers (device on-current). The VSED model is fully consistent with the MIT Virtual Source model and is applicable to both long- and short-channel devices using only a few physical parameters such as long-channel mobility and thermal velocity. The accuracy of the VSED model was demonstrated by comparison with measured I-V data of III-V HEMTs and Si extremely thin SOI (ETSOI) devices. The model physics and experimental calibration of the VSED model were presented at IEDM, 2014.

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A Second-Generation Virtual Source Field Electron Transmitter Model

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Sponsorship: National Science Foundation NEEDS program

An improved virtual source (VS) model is developed that builds upon the original MIT Virtual Source (MVS) model but incorporates the effects of (i) carrier degeneracy on thermal velocity and mean free path of carriers, (ii) drain-bias dependence of gate capacitance and virtual-source charge, and (iii) non-linear channel-access resistance on gm-degradation at high drain currents in the channel.

It is well known that both the thermal velocity and the mean free path of carriers increase with an increase in carrier concentration. While the basic MVS model required an artificially lower effective carrier mass, for its presumed constant carrier velocity, in order to match the measured drain currents in InGaAs HEMT devices, the MVS 2.0 model allows for the virtual source injection velocity of carriers to increase with V_{gs}, permitting a higher and more realistic effective mass of carriers. Furthermore, in the basic MVS model, the VS charge is not influenced by non-equilibrium transport conditions in the channel, and essentially the gate capacitance of the device is assumed to be independent of the drain bias. This assumption is too simplistic for quasi-ballistic devices where the negative momenta of the VS charge distribution are primarily supplied by the drain contact in near-equilibrium transport ($V_{ds} \approx 0V$) and are missing in non-equilibrium transport (high V_{ds}). The VS charge model in MVS 2.0 is updated to capture the effect of non-equilibrium transport. The charge model also includes the quantum-mechanical correction to the gate-channel capacitance due to the finite separation of the charge centroid from the semiconductor-insulator interface. Finally, the non-linearity of channel-access resistances that is responsible for the reduction in the transconductance, $gm = \partial I_D/\partial V_g$, of the III-V HEMT devices for high drain currents has been included in MVS 2.0 by modeling the source and the drain channel-access resistances as non-linear voltage-dependent resistances. Even though the basic MVS model has fewer fitting parameters and can fit the experimental data well, it does not capture the essential physics of the nanotransistor in presence of non-equilibrium transport, carrier degeneracy, and access-region non-linearity, and therefore MVS 2.0 is superior in this respect.

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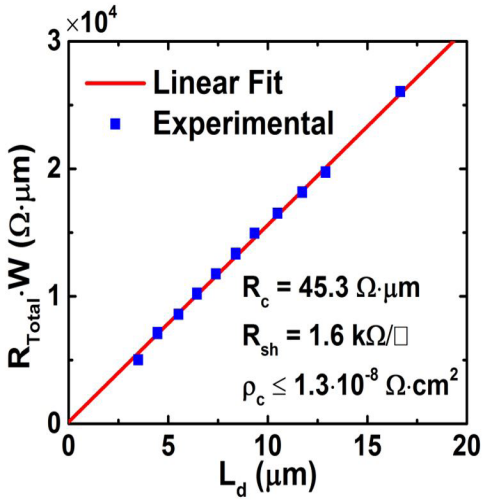
Nano-Scale Ohmic Contacts for p-InGaSb MOSFETs

W. Lu, J. A. del Alamo
Sponsorship: Samsung

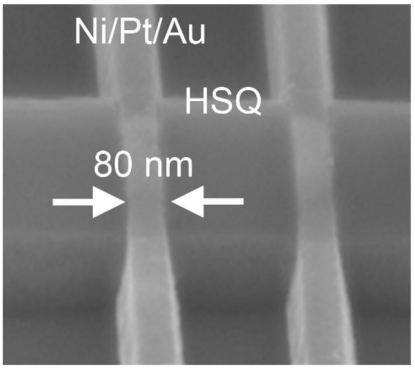
In the last few years, III-V compound semiconductors have emerged as promising channel materials for future scaling of CMOS technology. As high-performance InGaAs n-MOSFETs have been successfully demonstrated, it is critical to find a p-type counterpart with comparable characteristics. Among all III-V materials, the antimonide system, such as p-InGaSb, is the best candidate because of its outstanding hole mobility and the substantial enhancement in transport characteristics that is made possible by introducing compressive strain. To make p-InGaSb MOSFETs feasible in future technology, many challenges need to be addressed. One of the main limiting issues is the lack of a low-resistance nano-scale ohmic contact technology. This lack severely restricts the performance that can be achieved.

In this project, we are investigating process technologies that will allow us to demonstrate ultralow resistance nano-scale p-type ohmic contacts for sub-10 nm InGaSb MOSFETs. We have designed a novel p^+-InAs/InAsSb bilayer capping structure that addresses the deffectivity issues of conventional InAs caps and significantly improves the contact resistance. We are conducting a systematic study of various ohmic contact schemes and contact formation conditions. To date, we have fabricated Ni/Pt/Au ohmic contacts with a contact resistance as low as 45 Ω·μm, corresponding to a record contact resistivity of $1.3 \cdot 10^{-8}$ Ω·cm². Figure 1 shows the resistance data obtained by a circular transmission line model (CTLM) of the Ni contacts. To investigate nano-scale ohmic contacts, we also fabricated Ni nano-transmission line model (nano-TLM) test structures, which allow accurate measurement of ultralow contact resistivity in nano-contacts. Figure 2 shows an SEM image of a typical nano-TLM structure. For the smallest fabricated contact length of 80 nm, an average contact resistivity of $5.2 \cdot 10^{-8}$ Ω·cm² was extracted. In addition, we have fabricated Ni/Ti/Pt/Al ohmic contacts with a contact resistivity of $4.1 \cdot 10^{-8}$ Ω·cm². This is the first demonstration of Si-compatible contacts with ultralow contact resistivity.

We are working toward further improvement of the ohmic contact technology, through innovations such as strained contacts and fin-contacts, and trying to reduce the contact resistivity to the 10^{-9} Ω·cm² range. Our future goal is to demonstrate high performance InGaSb p-type MOSFETs and study fundamental transport phenomena in these transistors.



▲ Figure 1: Electrical measurements on a CTLM with Ni/Pt/Au ohmic contacts on a p^+-InAs/InAsSb cap structure after 3 min 350 °C annealing.



▲ Figure 2: SEM image of a Ni/Pt/Au nano-TLM test structure, with 80-nm contact length, 130-nm contact spacing, and 1-μm width.

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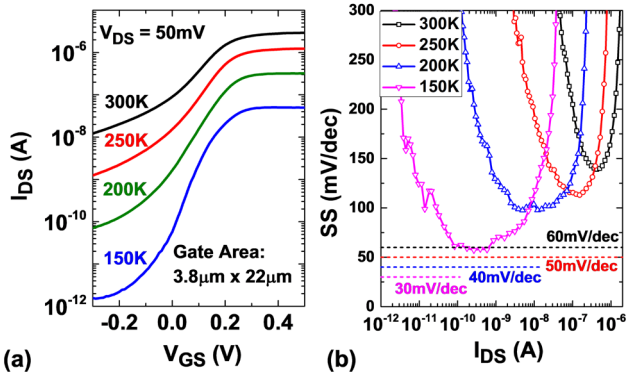
Effects of Drain-Side Thermal Barriers in InGaAs/GaAsSb Quantum-Well Tunnel-FETs

T. Yu, J. T. Teherani, D. A. Antoniadis, J. L. Hoyt
Sponsorship: National Science Foundation

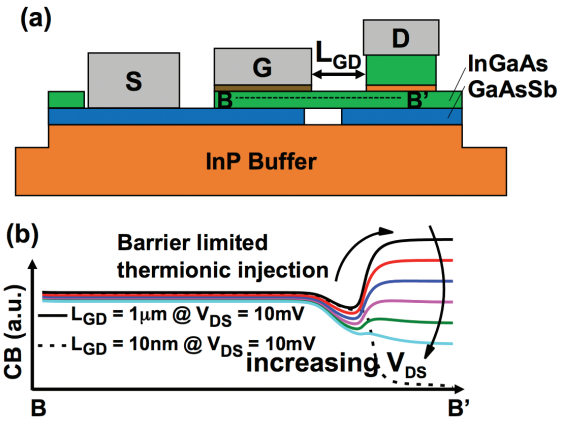
The recent downscaling of the supply voltage (V_{DD}) becomes limited in the conventional CMOS technology and tunnel-FETs (TFETs) have attracted much attention as potential candidates for future low power applications However, the non-idealities of the devices must be fully understood. In this work, temperature dependent measurement was performed to investigate the operation characteristics of the first InGaAs/GaAsSb quantum-well TFETs (QWTFETs) with tunneling taking place between two quantum-wells. Specifically, the drain-side thermal barrier in the ungated region is limiting the device performance.

Figure 1 shows the transfer characteristics and corresponding subthreshold swing (SS) of a QWTFET with gate dimension of L_g = 3.8μm, W_g = 22μm at V_{DS} = 0.05V at 150 K to 300 K. Significantly improved SS_{min} = 58 mV/decade and SS_{eff} = 80 mV/decade (I_{DS} from 10 pA to 10 nA) at 150 K are observed. One limiting factor in the device SS is the high-k/InGaAs interface traps. Since the traps in the conduction band, where TFETs are operated, do not freeze out at low temperature, the SS at 150 K is still not close to the thermal limit of 30 mV/decade. The OFF current is another major factor limiting the SS where the leakage current decreases substantially, exhibiting slightly improved SS compared with the thermal limit.

Figure 1 (a) also shows that the ON-current of the device at low drain bias degrades as the temperature decreases, which is caused by the decreased thermionic emission over a parasitic barrier in the current path. The location of the current barrier is at the drain side of the ungated region. TCAD simulation of the conduction band profile along the cutline B-B' in Figure 2 (a) shows that the barrier is present near the drain for small V_{DS} (Figure 2 (b)), which restricts the electron flow. To eliminate this barrier, the lightly doped region must be shortened. The simulation result with L_{GD} = 10 nm is also shown in Figure 2 (b).



▲ Figure 1: (a) I_{DS}-V_{GS} curves of the TFET from 150 to 300 K at low V_{DS}. The OFF-state leakage current is dramatically decreased at 150 K. (b) Subthreshold swing (SS) versus drive current from 150 to 300 K. SS ~ 60 mV/decade over more than one decade of I_{DS}, and SS_{eff} = 80 mV/decade is achieved at 150 K.



▲ Figure 2: A physical analysis for the InGaAs/GaAsSb vertical TFET in the ON-state. (a) A simplified schematic view; (b) InGaAs conduction band diagram parallel to the gate (B-B') simulated at V_{GS} = 0.5 V with varying V_{DS}.

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Modeling of Parasistic Trap-Assisted Tunneling in Tunnel Field-Effect Transistors

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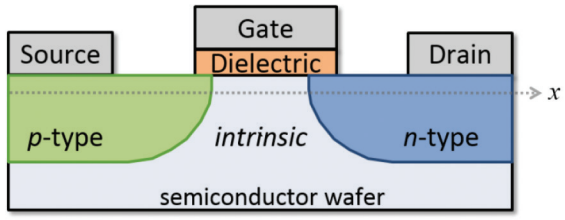
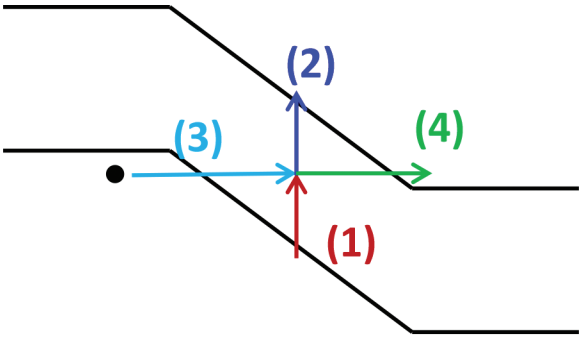
* Denotes equal contribution
Sponsorship: National Science Foundation Center for Energy Efficienct Electronics Science (E3S)

Tunnel field-effect transistors (TFETs), schematic shown in Figure 1, are currently being investigated because they are theoretically able to switch more steeply with gate voltage than the 60 mV/dec (room T) thermal limit of metal-oxide field effect transistors (MOSFETs), potentially enabling lower power electronics. The improvement of the switching steepness allows for a reduction in the operating voltage, V, and hence a reduction in power consumption as power scales with ~ V^2. Experimentally, TFETs have been challenged by low current drive and/or switching at rates above the thermal limit inferior to theoretical predictions. TFETs are gated diodes that switch from off to on when the gate aligns the conduction band of the channel to the valence band of the source. This work seeks to investigate parasitic leakage paths from traps–namely interface traps--that have prevented TFETs from delivering sub-60 mV/dec. performance. A gate-controlled parasitic current path through interface states is investigated using a modified Shockley-Reed-Hall (SRH) generation model in an effort to quantify the impact of trap-assisted tunneling on TFET switching behavior. The model consists of either an electron being emitted from the valence band to the conduction band through both tunneling and thermal mechanisms with the assistance of a trap state as shown in Figure 2. Different methods of reducing the impact of traps on the switching behavior will be investiaged to move towards the final goal of demonstrating sub-60 mV/dec. switching experimentally.



▲ Figure 1: A schematic of a tunnel field-effect transistor (TFET).



▲ Figure 2: Band diagram illustrating different mechanisms for trap-assisted-tunneling. The mechanisms are (1) electron capture and (2) electron emission from thermal emission and (3) electron capture and (4) electron emission from tunneling.

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InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs Fabricated by a Top-Down Approach

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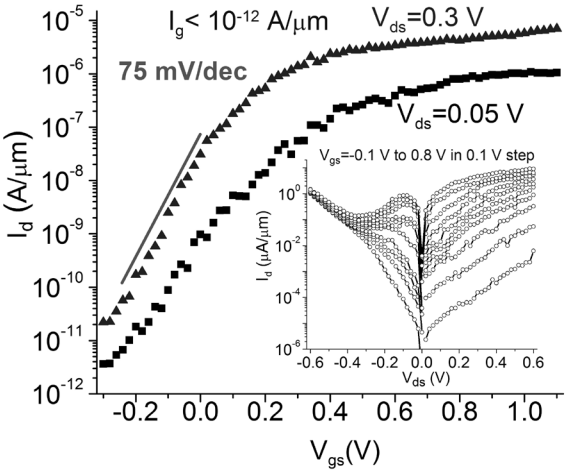
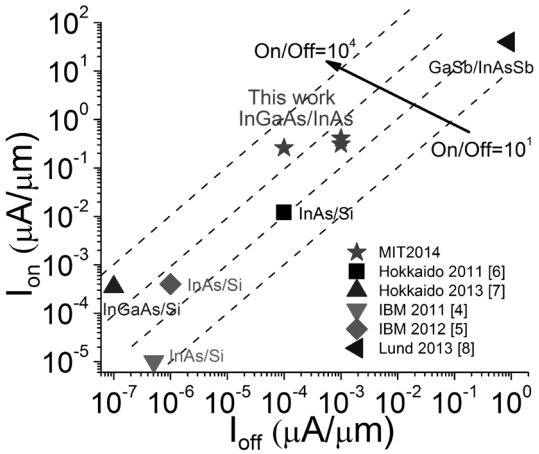
Sponsorship: National Science Foundation Award #093951 (E3S STC)

In light of the increased emphasis on energy efficiency in electronics, the tunnel field-effect transistor (TFET) has become attractive as a logic transistor due to its potential for low voltage operation. In TFETs, InGaAs-based heterojunctions promise a combination of steep slope, high ON-current due to the reduced tunnel barrier height, and a well passivated surface. To enable continued scaling, a nanowire (NW) transistor geometry with a wrapped-around gate is highly favorable due to the effective charge control and its robustness to short-channel effects. Here we demonstrate for the first time InGaAs/InAs heterojunction vertical NW TFETs fabricated via a top-down approach, which is more relevant to manufacturing than existing bottom-up techniques.

In our devices, the tunneling junction consists of a p^+-i $In_{0.53}Ga_{0.47}As$ heterostructure in which a 2 nm i-InAs/8 nm i-$In_{0.7}Ga_{0.3}As$ "notch" has been inserted to reduce the tunnel barrier height and yield steeper subthreshold characteristics and high ON current. We leverage process technology used in our previous InGaAs NW MOSFETs with several key changes, including an improved dry etch process. Figure 1 shows the subthreshold characteristics of a single-NW device with 50-nm diameter. A subthreshold swing of 75 mV/dec averaged over I_d from 10^{-9} to 10^{-7} A/μm is obtained at V_{ds}= 0.3 V. The output characteristics in a semilog scale including the reverse regime are shown in the inset of Figure 1. Clear negative differential resistance is observed for V_{ds}<0 and high V_{gs}, confirming the tunneling nature of device operation in the ON regime. Figure 2 benchmarks I_{on} vs. I_{off} among published vertical NW TFETs based on III-V materials at V_{dd}= 0.3 V (V_{ds}=0.3 V, ΔV_{gs}= 0.3 V). Compared to other III-V NW TFETs, our devices deliver high I_{on} at low I_{off}. These results are testimony to the increased flexibility and precision heterostructure growth that are afforded by a top-down fabrication approach.



▲ Figure 1: Subthreshold and output characteristics in semilog scale (inset) of a 50-nm diameter single-NW TFET. The device has a channel length of 60 nm, and the gate dielectric consists of 2.2 nm of Al_2O_3.



▲ Figure 2: I_{on} vs. I_{off} at V_{dd}=0.3 V (V_{ds}=0.3 V, ΔV_{gs}= 0.3 V) for recently published vertical NW TFETs containing III-V materials. All devices but the present ones are fabricated through bottom-up techniques.

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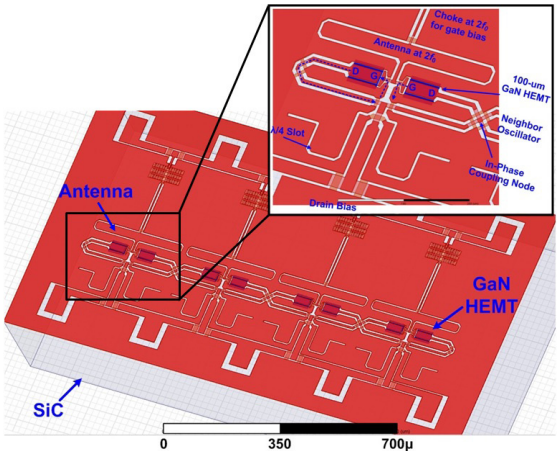
GaN-based High Electron Mobility Transistors for High Power THz Source

S. Rennesson, P. Srivastava, T. Sumitomo, U. Radhakrishna, R. Han, T. Palacios
Sponsorship: Office of Naval Research PECASE, ARO, DARPA DAHI program

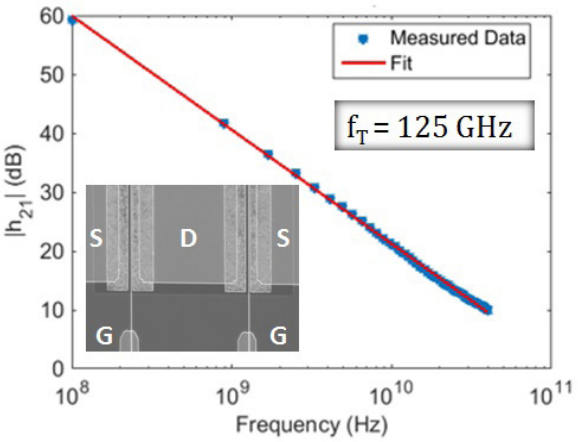
The outstanding properties of gallium nitride (GaN) such as high electron velocity (~ 2.5 × 10^7 cm/s) and high breakdown electric field (~ 3.3 MV/cm) make it an ideal candidate for applications requiring high power at high frequencies where conventional semiconductors, e.g., Si and GaAs, are incapable. Over the last decade, tremendous efforts have been concentrated on high power GaN-based high electron mobility transistors (HEMTs) to operate from the millimeter wave frequency (100 - 300 GHz) towards the THz range (300 GHz – 30 THz). At the moment, focal plane imaging array systems with the current state of high power THz sources are suffering from significant scattering losses.

The goal of this project is to realize and demonstrate energy-efficient high power THz sources by utilizing GaN-HEMTs circuit design and technology platform. The large THz frequency band is challenging to reach via traditional electronic and optical methods. Therefore, there is an immediate need to develop alternative approaches for future applications operating at high power and frequencies. In this project, we have developed a novel circuit design of a high power self-feeding GaN oscillator, which has been modeled to generate the 2nd harmonic ($2f_0$) of a signal with a frequency exceeding 300 GHz (Figure 1).

The standard AlGaN/GaN HEMTs on SiC substrate have been fabricated, using a T-shaped gate with a deep submicron gate length. The device exhibits a current density of >1 A/mm and excellent pinch off characteristics. The extracted transition frequency f_T is about 125 GHz (Figure 2). The electrical models for circuit simulation are undergoing for this device. In order to push further the frequency performances of the HEMTs (> 150 GHz), designs are being carefully optimized, e.g., by reducing the source-to-drain distance to boost the current density, re-designing a T-shape gate with thick top metal for reducing the gate resistance, and optimizing the dielectric stack to reduce the parasitic capacitance.



▲ Figure 1: Prototype of a 180-GHz GaN radiating oscillator array, with 4 elements (8 GaN HEMTs). The zoom-in exhibits the oscillator unit cell and describes the self-feeding oscillation structure with 2nd harmonic ($2f_0$) signal radiation.



▲ Figure 2: Small signal performance of an AlGaN/GaN HEMT-on-SiC substrate with f_T ~ 125 GHz. The inset presents a top view of the device with L_g = 80 nm and width = 2x100 μm.

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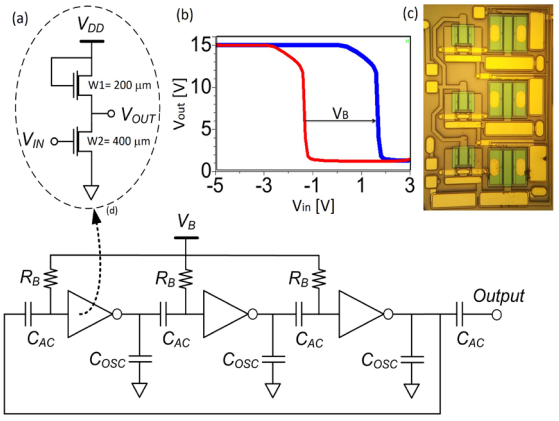
Study of Phase Noise in GaN-Based Ring Oscillators

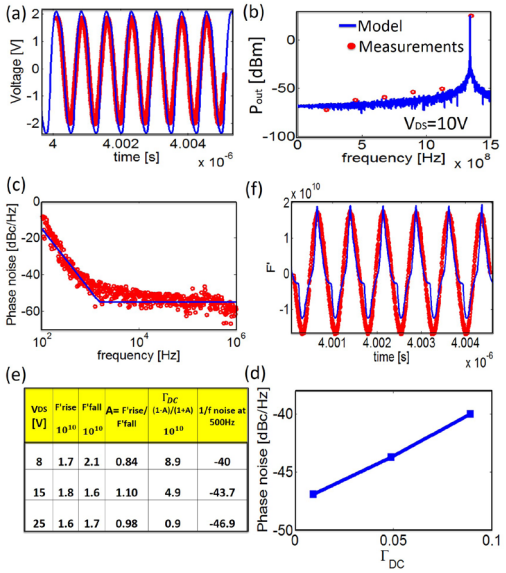
U. Radhakrishna, P. Choi, D. A. Antoniadis
Sponsorship: Singapore-MIT Alliance for Research and Technology LEES program, National Science Foundation NEEDS program, MIT/MTL GaN Energy Initiative

Modeling GaN-based HEMTs has gained considerable attention in recent years because of superiority in high-power and high-frequency performance, making them the key candidate for RF applications. The design requirements of GaN-based RF circuits motivate GaN-compact device models to include accurate description of device small signal, large signal and noise performances. The design of oscillators that are used in GaN-based microwave monolithic integrated circuits as voltage-controlled oscillators in the receiver stage and in wired-communication as clock sources requires the modeling of phase noise or jitter.

Prior works on the physics-based MIT Virtual Source GaNFET (MVSG) model demonstrated its physical grounding along with its usefulness in RF circuits design. This work demonstrates the usefulness of the MVSG model in the design of GaN- based oscillators. The model with its accurate representation of small- and large-signal device characteristics along with RF- and low-frequency noise behavior can be used for the design of oscillators with the desired frequency response including the close-in phase noise performance. The MVSG model is benchmarked against device terminal DC-, small-signal S-parameter-, and noise figure measurements and is used to design a 3-stage GaN pseudo-invertor ring oscillator, delivering 21 dBm at 1.4 GHz. It is found that the MVSG model provides accurate estimation of large-signal device-switching behavior along with the device-flicker (1/f) noise-dominated phase noise. The dependence of phase noise level on the DC component of the impulse sensitivity function (ISF) is confirmed using the model and measurements. In this work, the physics of carrier charge and transport in a GaN-HEMT along with device-level noise is translated into functional RF-circuit elements using the MVSG model.



▲Figure 1: Capability of MVSG model to capture the device phase noise and large signal behavior can be studied simultaneously using an RO circuit. (a) The absence of E-mode devices requires a pseudo-inverter topology using a drain-gate connected FET. (b) The voltage transfer characteristic (VTC) shows a transition at negative input voltage (V_{in}) (red) due to the negative threshold voltage of depletion mode GaN HEMTs. To shift the transition to a positive V_{in} (blue), a negative gate bias (V_B) through R_B and ac-coupled capacitor (C_{AC}) is required. (c) The die micrograph image and (d) the 3-stage RO schematic with V_B, ac-coupled capacitor are also shown.



V_{DS} [V]	F^2_{rise} 10^{10}	F^2_{fall} 10^{10}	$A = F^2_{rise}/F^2_{fall}$	Γ_{DC} $(1-A)/(1+A)$ 10^{10}	1/f noise at 500Hz
8	1.7	2.1	0.84	8.9	-40
15	1.8	1.6	1.10	4.9	-43.7
25	1.6	1.7	0.98	0.9	-46.9

▲Figure 2: (a) Time domain waveforms and (b) frequency spectrum of output voltage of RO are shown. (c) Phase noise spectrum is compared to simulation with flicker noise model capturing phase noise ($1/f^3$) spectral levels and corner frequencies accurately. (d) $1/f^3$ is found to be proportional to DC component of ISF (Γ_{DC}), which depends on derivative of output node waveforms (i.e., rising and falling edge slopes); it can be captured by model as shown. (e) Table shows Γ_{DC} calculated from ISF at different V_{DD}. (f) Linear relationship between $1/f^3$ noise level at 500 Hz offset frequency and Γ_{DC} can be verified from model and measurements.

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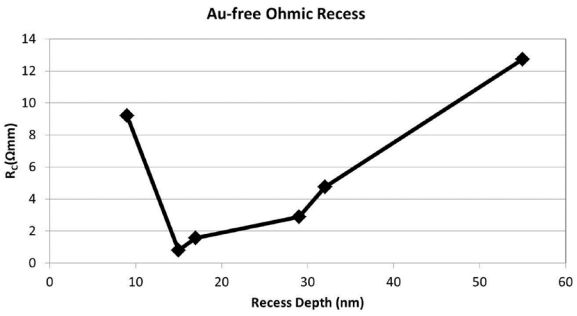
Process Development for GaN/SOI Heterogeneous Integration

D. Piedra, S. Rennesson, T. Palacios
Sponsorship: DARPA DAHI Program

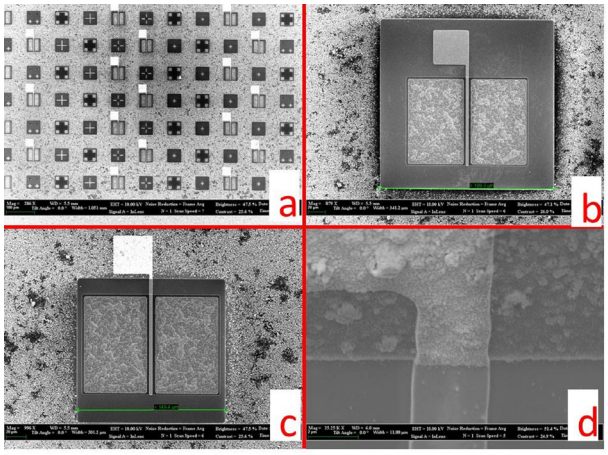
Silicon complementary metal–oxide–semiconductor (CMOS) technology has been at the forefront of the microelectronics revolution, benefiting from years of process development allowing for advances in device scaling and integration density. However, deeply scaled Si CMOS faces challenges in high-voltage and high-power density applications. The monolithic heterogeneous integration of GaN devices with Si CMOS in the power amplifier and power conversion stages would allow performance unachievable by Si alone. The approach taken in this project is to grow AlGaN/GaN structures in patterned windows on an 8" SOI wafer. This paper focuses on the development of high electron mobility transistors (HEMTs) that are then fabricated in the GaN windows using Si compatible process technology.

One of the key technologies to develop for CMOS process compatibility is a gold (Au) free ohmic contact technology. Excellent device performance has been reported in GaN HEMTs using Au-based ohmic contacts. However, for successful heterogeneous integration, the GaN HEMT ohmic contats must be processed without gold. The process flow currently consists of etching a recess in the ohmic pattern by reactive ion etching, followed by sputtering a metal stack of Ti/Al, patterning the ohmic contacts, etching the metal stack, and finally annealing the patterned metal at 550˚C. As seen in our results (Figure 1), the contact resistance is extremely sensitive to the recess depth.

In parallel to our development of Au-free ohmic contacts, we have processed devices in the GaN windows of different sizes and shapes (square or rectangle). Both HEMT and Van der Pauw squares were processed (Figure 2) to measure a full suite of device and material characteristics including breakdown voltage, current collapse, Hall mobility, and carrier concentration.



▲ Figure 1: GaN HEMT contact resistance as a function of ohmic recess depth.



▲ Figure 2: Scanning electron microscope image taken from the processed GaN on patterned SOI wafers.
2a) array of HEMTs. 2b) HEMT in 200x200μm^2 window.
2c) HEMT in 150x150μm^2 window.
2d) gate pad coverage of the window edge step.

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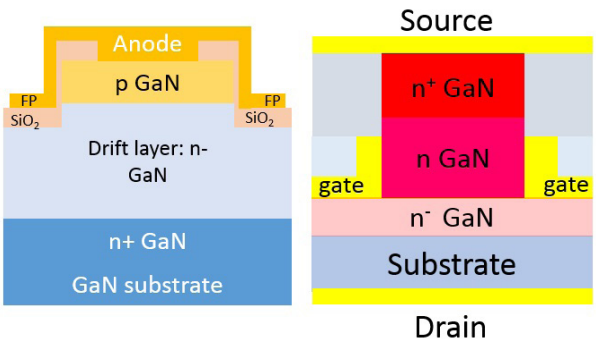
Vertical Transistors and Diodes on Bulk GaN Substrates

M. Sun, Y. Zhang, T. Palacios
Sponsorship: ARPA-E Switches Program

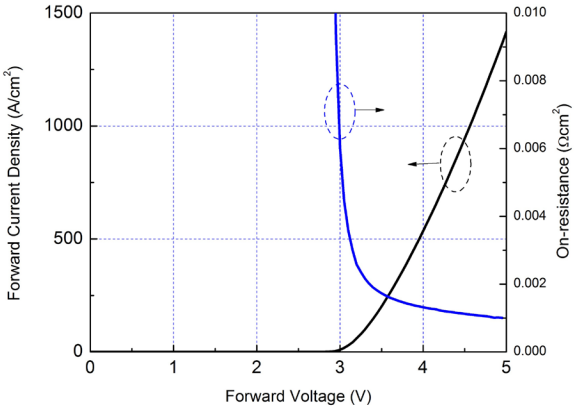
New opportunities for higher efficiency power electronics have emerged with the development of GaN. However, most GaN discrete devices demonstrated to date have had relatively low current ratings in addition to high cost. Recent research results indicate that advances in new materials could substantially accelerate progress towards GaN devices that achieve both higher current ratings and functional cost parity with silicon-based devices. Vertical device architectures for GaN power semiconductor transistors could substantially reduce cost and increase current densities. Our group has been working to develop new fabrication technologies to reduce the cost of vertical PIN diodes and transistors.

In the vertical PIN diodes fabricated at MTL, the mesa etch was performed in an ICP-RIE system by using Cl_2/BCl_3 gas. A wet etch was followed to achieve a smooth etching sidewall to reduce sidewall leakage. Ni/Au metal was annealed in oxegen ambien to form ohmic contacts with p-GaN. A field plate was made to reduce peak electric field at the device edge. The cathode electrode was formed on the rear surface of the device. An on resistance of 1 $m\Omega cm^2$ was achieved on these diodes with a breakdown voltage more than 700 V. The leakage current of the diodes is below 10^{-7} A/cm^2, significantly lower than GaN devices on foreign substrates.

A conventional current aperture vertical electron transistor (CAVET) requires the regrowth of the AlGaN/GaN access region, which significantly increases the cost of the device. In addition, it is very difficult to have highly insulating current blocking layers between the access region and the drain drift region, which makes it very difficult to increase the breakdown voltage in these devices. To solve these problems, we have proposed a new vertical GaN JFET structure that uses a top-down fabrication technology based on dry etching. No regrowth is needed, therefore lowering the cost and complexity.



▲ Figure 1: Cross-sectional view of vertical GaN PIN diode (right) and vertical GaN JFET.



▲ Figure 2: Forward characteristics of vertical GaN PIN diode.

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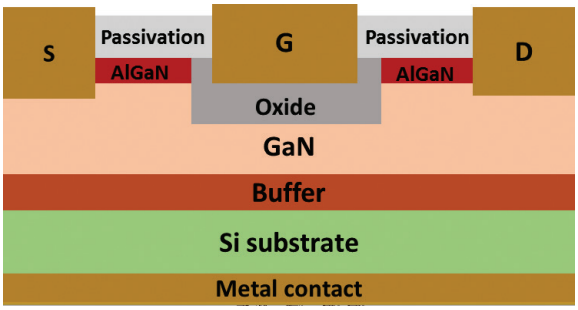
Positive-Bias Temperature Instability in GaN Power Field-Effect Transistors

A. Guo, J. A. del Alamo
Sponsorship: NDSEG Research Fellowship

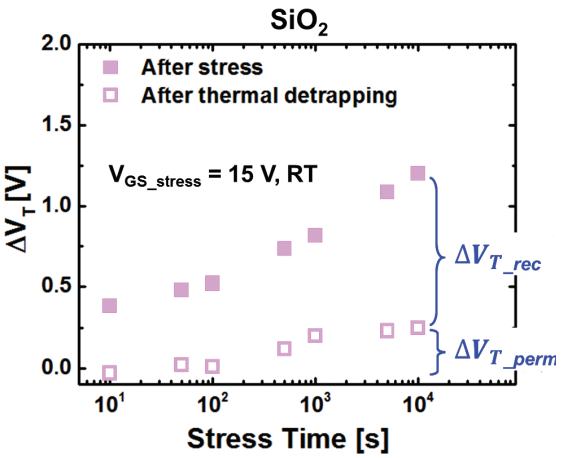
Galium nitride (GaN) is a promising material for replacing silicon in power switching applications. Recently, GaN-high electron mobility transistors with insulated-gates (GaN MIS-HEMT) have attracted much attention because they offer high current, low gate leakage and high breakdown voltage, all desirable for power transistors. However, GaN MIS-HEMTs suffer from threshold voltage (V_T) instability after prolonged high-voltage stress at high temperature (usually referred to as bias temperature instability, or BTI). It is challenging to address this issue because the many layers and interfaces of a MIS-HEMT structure make it difficult to identify the physical origin of BTI. In this work, we study the positive-bias temperature instability (PBTI) in a simpler GaN metal-oxide-semiconductor field-effect-transistor (MOSFET) (Figure 1). This structure allows us to focus specifically on stability issues associated with the oxide and the oxide/GaN interface.

We developed a benign process to characterize the devices before, during, and after stress experiments. In a typical experiment, we first characterize a device and identify a "stable" initial state as a reference for subsequent stress/recovery experiments. The PBTI stress phase consists of a series of stress segments of increasing stress voltage (V_{GS_stress}>0), stress time (t_{stress}) and temperature (T). During stress, a device is subject to a constant positive gate stress with other terminals grounded. Immediately after each stress segment, we evaluate the evolution of V_T and subthreshold swing (S) through repeated, short I_D-V_{GS} sweeps. At the end of each segment, the device is reinitialized by a thermal baking step, and a complete I_D-V_{GS} characterization is performed.

We studied PBTI in GaN MOSFETs with SiO_2 as the gate dielectric. We carried out experiments with V_{GS_stress} between 5 and 15 V, t_{stress} between 10 and 10,000 seconds and T at -40˚C, room temperature (RT) and 75˚C. We found that V_T shifts are positive and increase with V_{GS_stress}, t_{stress} and T. In all studied devices, this V_T shift is completely recoverable after $V_{GS\_stress} \leq 10$ V and T ≤ RT but only partially recoverable after V_{GS_stress} = 15 V. Figure 2 shows the stress time evolution of ΔV_T for V_{GS_stress} = 15 V at RT. In all cases, we are able to model the recoverable portion of ΔV_T using a well-established oxide trapping model. We conclude that the recoverable ΔV_T is due to electron trapping in pre-existing oxide traps and the non-recoverable ΔV_T is due to the creation of interface states at the oxide/GaN interface. Our findings are consistent with PBTI studies for silicon and other material systems.



▲ Figure 1: GaN MOSFET structure studied in this work.



▲ Figure 2: Stress time evolution of ΔV_T for GaN MOSFETs with SiO_2 as gate dielectric for V_{GS_stress} = 15 V at RT. Filled symbols are the total ΔV_T extracted 1 sec after stress, and open symbols are the non-recoverable ΔV_T after a thermal bake. ΔV_{T_rec} stands for recoverable ΔV_T, and ΔV_{T_perm} stands for non-recoverable or permanent ΔV_T.

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Oxide Breakdown in High-Voltage GaN Field-Effect Transistors

S. Warnock, J. A. del Alamo
Sponsorship: Texas Instruments

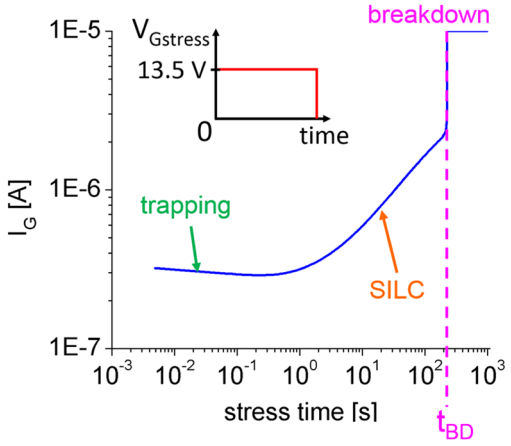
As the demand for more energy-efficient electronics increases, GaN field-effect transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN power transistors are ready for commercial deployment. One of the concerns is gate oxide reliability as a result of high-voltage stress. In particular, after prolonged high-voltage gate bias stress, the oxide will suffer from catastrophic breakdown beyond which the transistor is no longer operational.

Our research is directed to providing fundamental understanding behind the physics of time-dependent dielectric breakdown (TDDB) of the gate oxide in GaN metal-insulator-semiconductor high electron-mobility transistors (MIS-HEMTs). We leverage a rich body of work that has been performed on silicon MOSFETs with regards to TDDB.

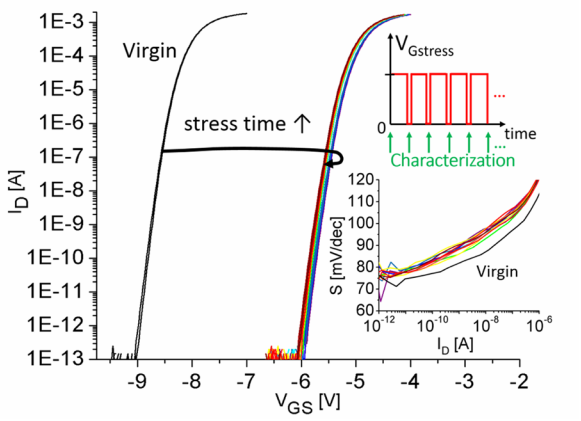
Figure 1 shows the evolution of the gate current I_G in a classic TDDB experiment in a GaN MIS-HEMT. Here, we hold a high positive gate bias until breakdown occurs, which we can observe as the sudden jump in gate current, I_G, around 225 s. Through this experiment, we can observe first a decrease in current due to trapping and then an increase in what is known as stress-induced leakage current, SILC. This increase results from the generation of defects in the oxide. The observed characteristics in Figure 1 constitute fairly classic TDDB behavior.

Experiments such as the one in Figure 1 give limited information about oxide degradation during stress. A richer picture emerges if we perform a similar experiment where the stress is periodically paused to measure the subthreshold characteristics of the device, as shown in the inset of Figure 2. This figure reveals a large positive shift in the threshold voltage followed by a small negative shift as the experiment progresses. We also observe a fixed immediate degradation in the subthreshold swing S that suggests interface state generation early in the stress experiment. The change in direction of V_T, as well as the degradation in S, both occur in the same regime where we see the appearance of SILC in Figure 1.

Through experiments such as these, we hope to gain an understanding of the fundamental mechanisms behind oxide breakdown as well as build models that allow us to predict device lifetime under realistic operating conditions.



▲ Figure 1: Gate leakage current as a function of stress time during a constant $V_{Gstress}$ TDDB experiment at room temperature. The FET is held at V_G=13.5 V until the device breaks down. V_{DS}=0 V.



▲ Figure 2: Subthreshold characteristics at V_{DS}=0.1 V, for a TDDB experiment at $V_{Gstress}$=13.5 V. I-V characterization is performed every 30 s. The insets describe the experimental procedure and the degradation of the subthreshold swing S.

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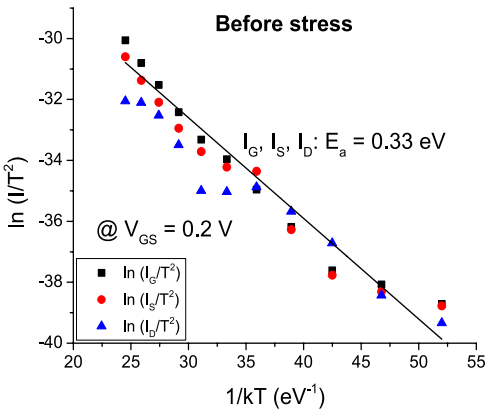
Permanent Degradation of InAlN/GaN HEMTs under High-Power Stress

Y. Wu, J. A. del Alamo
Sponsorship: National Reconnaissance Office

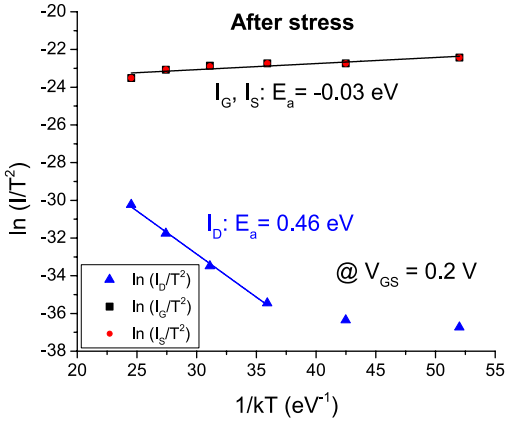
First demonstrated in the 1990s, GaN transistors have started to become commercially available in recent years. GaN is the technology of choice for high-power applications in electronic warfare, radar, satellites, cable TV, and cellular mobile communications. Compared with other commonly used materials such as Si and GaAs, GaN devices can operate at higher voltages and frequencies, thus enabling significant improvements in power efficiency and dramatic reduction in size.

In contrast with the conventional GaN HEMT with AlGaN as barrier layer, the use of an InAlN barrier yields, for the same layer thickness, a higher spontaneous polarization-induced charge at the barrier/GaN interface. This enables aggressive barrier thickness scaling and therefore gate length scaling. As a result, InAlN/GaN HEMTs, are extremely promising for very high-frequency applications. However, unlike the better understood AlGaN/GaN system, degradation mechanisms in InAlN/GaN HEMTs are not well established. Our project aims to study the leading degradation modes of InAlN/GaN HEMTs under different stress conditions with the ultimate goal of constructing models to predict device lifetime.

We are studying the degradation of InAlN/GaN MIS-HEMTs under prolongued biasing in the OFF, semi-ON, and ON-states. Negligible device degradation takes place in both OFF and Semi-ON states, which is in drastic contrast to the AlGaN/GaN structure known to be vulnerable to semi-ON-state stress. Under ON-state high-power stress, however, InAlN/GaN HEMTs can undergo significant permanent degradation, which is reflected in a decrease in the saturation drain current, an increase in gate leakage current, and degradation of other important figures of merit. With further exploration, we have found that both high voltage and high current are necessary to induce significant device degradation. This suggests something more than just an electric-field-driven degradation mechanism. Also, a close examination of the terminal currents of a degraded device reveals the appearance of a gate-to-source leakage path of a unique character, as illustrated in Figures 1 and 2. Before stress (Figure 1), all three terminal currents demonstrate thermionic field emission dominated behavior whereas after stress (Figure 2), the gate and source currents suggest ohmic conduction while the drain current still maintains the signature of a virgin device. This strongly suggests a degradation mechanism that affects the source side of the device instead of the drain side, which is where the high electric field is present. We are currently studying this puzzling behavior in more detail.



▲ Figure 1: Arrhenius plot for I_D, I_G, and I_S of a virgin InAlN/GaN HEMT at V_{GS}= 0.2 V and V_{DS}=0 V. All three terminals show thermionic-field-emission dominated current with an activation energy of 0.33 eV.



▲ Figure 2: Arrhenius plot for I_D, I_G, and I_S after high-power stress for the same device as in Figure 1. The currents are measured at V_{GS}= 0.2 V and V_{DS}=0 V. The drain current maintains the signature of a virgin device while the gate and source currents have drastically increased and changed character.

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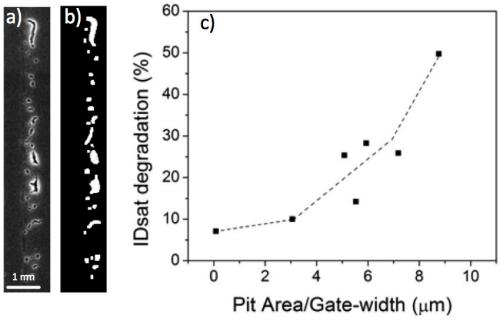
Reliability of AlGaN/GaN HEMTs on Silicon

W. A. Sasangka, G. J. Syaranamual, C. L. Gan, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology

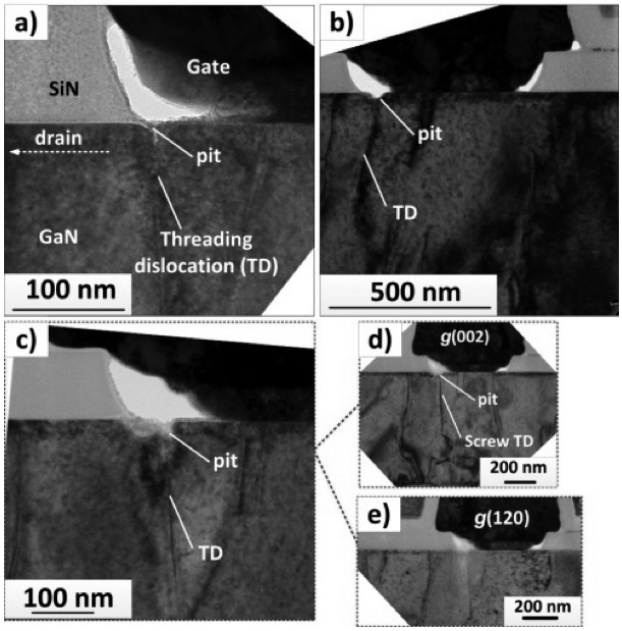
Integration of AlGaN/GaN high electron mobility transistors (HEMTs) on the silicon platform is attractive for many reasons. Having both high-power-high-frequency AlGaN/GaN HEMTs and established Si complementary metal-oxide semiconductor (CMOS) devices in a single chip would open up many new applications. It would also allow cost-effective large-scale fabrication of complex system by building on existing silicon technology and infrastructure, including the use of 300 mm wafers. However, market adoption of such a technology is still limited due to concerns about HEMT device reliability.

Due to its high lattice mismatch, epitaxial growth of AlGaN/GaN on silicon substrates results in a very high threading dislocation density (~10^9/cm^2). This is one to two orders of magnitude higher than the typical threading dislocation density of AlGaN/GaN grown on SiC or sapphire. The threading dislocation density significantly affects the electrical degradation of the devices. However, correlations with physical degradation mechanisms are still unclear. Past work has established a correlation between electrical degradation and physical degradation, in the form of pits that appear in the GaN capping layer and AlGaN layer along gate edges where high electric fields exist. The mechanism of pit formation has been associated with the presence of water, which, even in the presence of SiN passivation layers, leads to electrochemical oxidation of aluminum and gallium oxide.

We have investigated the role of threading dislocations in pit formation during stressing of AlGaN/GaN on Si high electron mobility transistors under high reverse bias. Upon stressing, the drain current saturation ($I_{D\text{-saturation}}$) decreases over time. The amount of $I_{D\text{-saturation}}$ degradation correlates well with pit formation at the gate-edge, where the electric field is the highest. Using a transmission electron microscope weak-beam technique, it was found that pits tend to nucleate at threading dislocations that have a screw component, even when these dislocations are at locations away from the gate-edge. An explanation based on an electrochemical oxidation model has been proposed.



▲ Figure 1: a) Top view SEM image of a device with pits. b) After image processing using Image J software, pits are indicated in white. This allows pixel computation of the pit area. c) $I_{D\text{-saturation}}$ degradation as a function of pit area/gate-width.



▶ Figure 2: a) to c). Cross-sectional TEM images of stressed devices before metal removal, taken along the [210] zone axis. Pits are seen to form at locations away from E_{max} (the gate edge). d). Image of sample c) taken using a weak beam technique at *g* (002). e) Image of sample c) taken using a weak beam technique at *g* (120).

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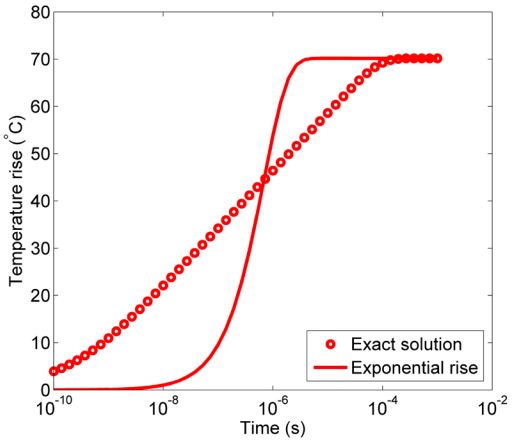
Transient Thermal Dynamics of GaN High Electron Mobility Transistors

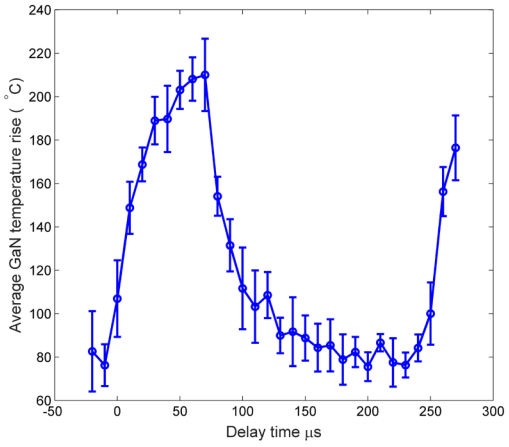
K. R. Bagnall, E. N. Wang
Sponsorship: MIT/MTL GaN Energy Initiative, Singapore-MIT Alliance for Research and Technology LEES program

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are one of the most promising compound semiconductor technologies for high-frequency communication and high-voltage power conversion applications. In particular, the high critical electric field, electron concentration, and electron mobility enable GaN HEMTs to have a lower on-resistance than transistors based on silicon with the same breakdown voltage. However, the high power density present in GaN HEMTs for radio-frequency (RF) and power switching applications results in high channel temperatures due to self-heating and degradation in device performance and lifetime. Although self-heating in GaN HEMTs has been studied comprehensively with modeling and experimental approaches, much of this work has focused on steady state conditions. In this work, we are developing analytical models for transient thermal dynamics in GaN HEMTs as well as experimentally characterizing devices with time-resolved micro-Raman thermography.

Transient power dissipation resulting in a time-dependent channel temperature occurs in many contexts in which GaN HEMTs are utilized: pulse mode radar, cellular base stations, and switch mode power converters. To facilitate design and packaging of GaN HEMTs for these applications, we have developed a semi-analytical thermal model for the transient temperature rise in multi-layer HEMT structures based on Fourier series expansions and numerical Laplace transforms. Like our previous work on steady state thermal modeling, this model provides rich physical insight, e.g., identifying the dominant thermal time constants associated with multi-dimensional heat diffusion over several length scales. As Figure 1 shows, we have demonstrated that a single time constant, often assumed to be ~1 µs for typical GaN HEMTs, poorly represents the transient temperature response by underestimating the channel temperature rise for times ~100 ns. To validate this modeling, we are developing an experimental setup based on time-resolved micro-Raman spectroscopy to measure the GaN buffer temperature with ~1-µm spatial, 10 °C temperature, and 20-ns time resolution. We have successfully implemented this technique and measured the transient temperature rise of GaN-on-sapphire ungated HEMTs subject to pulsed power dissipation as shown in Figure 2. This combination of computationally-efficient thermal modeling and rigorous experimental characterization can lead to greater understanding of transient thermal dynamics of GaN HEMTs to improve reliability and performance.



▲ Figure 1: Modeled transient temperature response of a 100-µm silicon slab representing a GaN-on-Si HEMT structure. An exponential function with a single time constant significantly underestimates the temperature at times less than ~1 µs.



▲ Figure 2: Temperature of GaN-on-sapphire ungated HEMT measured by time-resolved micro-Raman spectroscopy. A pulsed power dissipation of 4 W/mm was applied for 75 µs, and the device was allowed to cool for 175 µs.

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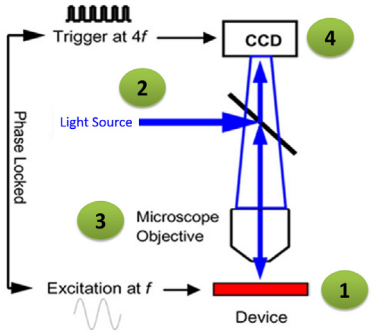
Thermal Characterization of GaN HEMTs via Photo-Thermal Reflectance Thermography

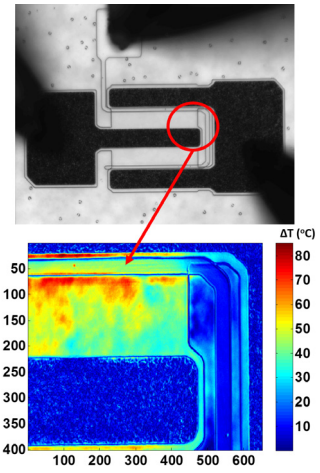
B. Barabadi, K. R. Bagnall, Y. Zhang, T. Palacios, E. N. Wang
Sponsorship: MIT/MTL GaN Energy Initative, MIT-Singapore SMART LEES Program

Gallium nitride- (GaN) based high electron mobility transistors (HEMTs) have gained a significant amount of interest over the last few years for their excellent electrical properties, high efficiencies, and high power densities for both power electronics and radio-frequency applications. However, these high power densities result in high channel temperatures and temperature gradients that induce thermo-elastic stresses, formation of defect sites, and many other degradation mechanisms that substantially affect the performance and reliability of GaN HEMTs. Therefore, it is important to develop reliable tools for thermal characterization of GaN HEMTs. Temperature measurement in these devices, however, is extremely challenging due to the requirement of high spatial resolution, the geometrical complexities, and the variety of materials present (metals, semiconductors, and insulators). As previously demonstrated, the extremely high temperature profile in a GaN HEMT occurs in a region (~0.5 to 1 μm) over which the dissipated power density is very high (~10^{10} W/m^2). In fact, the state of the art thermal measurement techniques are simply incapable of capturing this highly localized temperature profile of the devices being tested. Our objective is to develop a reliable approach to detect thermal phenomena with nanoscale spatial resolution (below 500 nm) under various input powers that can significantly affect the performance of GaN-based devices.

To have a comprehensive understanding of thermal management in GaN devices, we have utilized photo-thermal reflectance thermography, a well-established technique that is fully optical and noncontact. Thermoreflectance imaging has several advantages over the currently available high resolution techniques: it provides a thermal map of the device, and it also provides surface measurements, which is crucial due to the unique geometries of transistors. The schematic of the setup is shown in Figure 1. By choosing the appropriate illumination wavelength, we have achieved a spatial resolution of 0.3 μm for gated and ungated AlGaN/GaN structures on different substrates. We have also improved the photo-thermal reflectance setup by developing a new calibration method and optimizing the temperature measurement procedure to obtain a reliable and accurate map of the temperature profiles for various input powers. Figure 2 (a) shows an optical image of a two-finger GaN HEMT on SiC during thermal measurements. The device was biased at voltages ranging from 0 to 25 V. Figure 2 (b) demonstrates a representative temperature profile at the interface of AlGaN/GaN close to the gate for the case in which the device is biased at 20 V and the gate voltage is 1 V. As can be seen, the temperature rise of up to 80 °C occurs in a considerably localized area (less than 2 μm) adjacent to the gate, where power densities are significantly high. This work helps us to better understand the structural and thermal changes in GaN HEMTs, the formation of defect cites, and their relation to temperature through high-resolution thermal imaging.



▲Figure 1: Schematic of thermal-reflectance setup (adapted from third reading).



◀Figure 2: -(a) Optical image of a two-finger GaN HEMT during measurements, (b) temperature profile in a zoomed-in view of the device.

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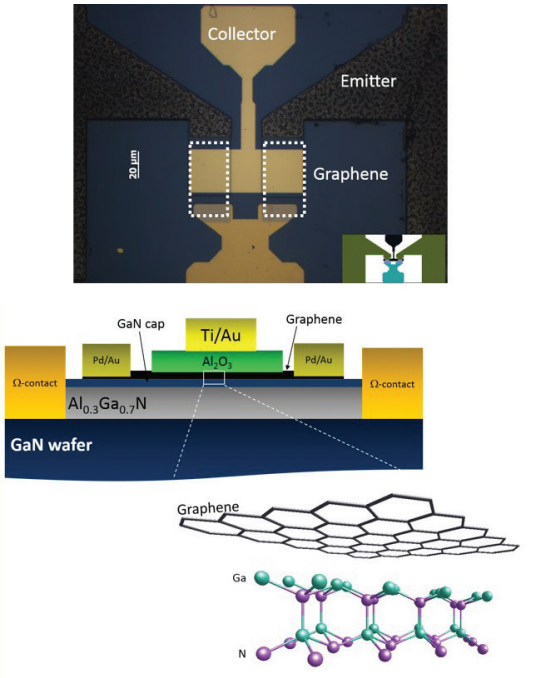
Vertical Graphene-on-GaN Hot Electron Transistor

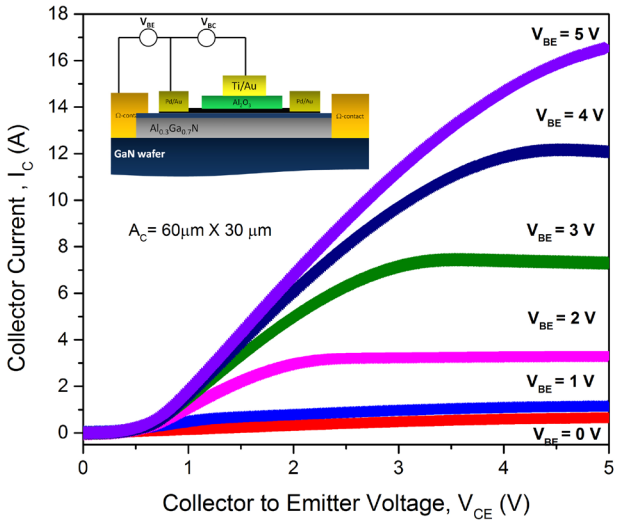
A. Zubair, Y. Song, J. Kong, M. Dresselhaus, T. Palacios
Sponsorship: Army Research Office

Two-dimensional materials have been extensively studied as promising candidates for future high-speed electronics. The very high room-temperature carrier mobility, saturation velocity, and thermal conductivity of graphene make it an attractive candidate for high frequency electronics. Although remarkable RF performance has been demonstrated in lateral graphene transistors, their performance is still limited by lack of current saturation caused by the absence of bandgap in graphene. At the same time, III-nitride heterostructure ($Al_xGa_{1-x}N$/GaN) high electron mobility transistors (HEMTs) are promising for high frequency and high-power operation (due to wide bandgap and high critical field), but their intrinsic current gain cutoff frequency is limited by smaller electron saturation velocity. The integration of graphene and GaN in a single vertical hot electron transistor can utilize the potentials of both materials systems in high frequency electronics, overcoming the limitations present in lateral transistors.

In this work, we design and fabricate a novel vertical graphene transistor, a majority-carrier device where a monolayer graphene base is sandwiched between a metal collector and an AlGaN/GaN heterojunction emitter (Figure 1). The transport characteristics of first device prototype (Figure 2) exhibits very promising current density (~kA/cm²), current gain (α~50%), and moderate on-off ratio (~300). The measured current density is the highest among all the graphene-based hot electron transistors reported so far in the literature. Simulations further support the notion that with proper optimization of the materials and device structure, the proposed transistor can be a promising candidate for future high frequency applications.



▲ Figure 1 Optical image and schematic diagram of graphene-on-GaN graphene base transistor. Emitter contact to the two-dimensional electron gas in GaN/AlGaN heterojunction consists of a Ti/Al/Ni/Au.



▲ Figure 2 Common-emitter characteristics of the fabricated hot electron transistor at different base to emitter voltages (V_{BE} -0-5 V), showing high current density.

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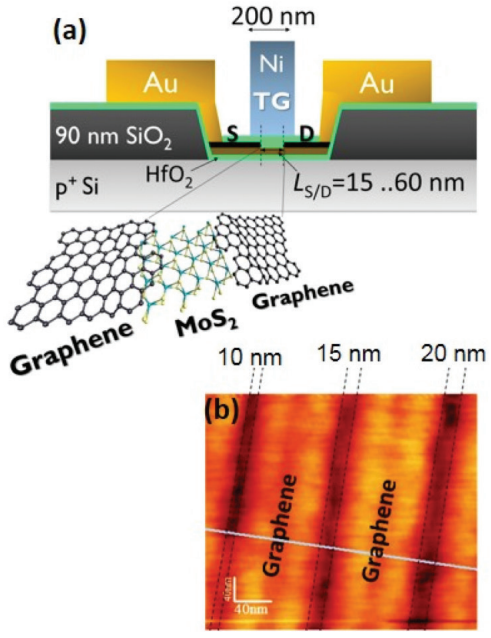
High Performance 15-nm Channel Length Double-Gate MoS_2 Field-Effect Transistor

A. Nourbakhsh, A. Zubair, T. Palacios
Sponsorship: Office of Naval Research PECASE, Army Research Laboratory

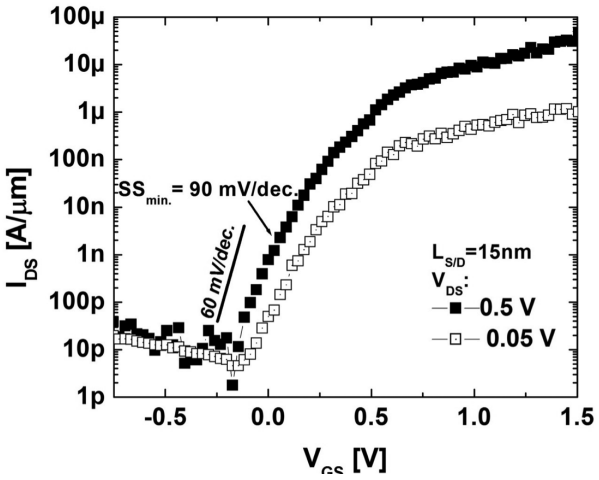
Mono- and multiple layers of molybdenum disulphide (MoS_2) have great potential in device applications because of the large bandgap, thermal stability, high carrier mobility, and compatibility with CMOS processes. Field-effect transistors (FETs) built on a few layers of MoS_2 are effectively ultra-thin body FETs (UTB-FETs), which have an optimized structure to reduce short channel effects. Also, the heavier effective mass of MoS_2 compared with Si allows the transistors to have an increased drive current when benchmarked against UTB-silicon transistors at their scaling limit.

In this work, we demonstrate the fabrication and electrical characteristics of a double-gate MoS_2 FET using single-layer graphene (SLG) as the source/drain (S/D) contacts and a record channel length of 15 nm. A 3-nm MoS_2 thin film was transferred onto a p-doped silicon substrate covered with 10 nm of HfO_2 as the back gate. Subsequently, the SLG was transferred onto the MoS_2 layer. SLG has metallic properties with two-dimensional ballistic electronic transport. A 15-nm polymethyl methacrylate (PMMA) trench was patterned on the SLG followed by selective etching of the SLG, creating a 15-nm slit that defined the S/D channel. After PMMA removal, 10 nm of HfO_2 and 50 nm of Ni were deposited onto the channel as the top gate. Figure 1 shows a schematic of the device and an atomic force microscopy (AFM) image of sub-20-nm-wide graphene slits.

The MoS_2 FET had an on/off ratio of greater than 10^6 with an on-current of ~50 μA/mm and minimum subthreshold slope of 90 mV/dec at drain-voltage V_{DS}= 0.5 V (Figure 2). To the best of our knowledge, this MoS_2 transistor has the shortest operating channel length of any MoS_2 transistor demonstrated to date. Without significant optimization, this transistor already performs as well as much larger state-of-the-art silicon-on-insulator transistors in many aspects. The high on/off ratio indicates that further scaling is possible.



▲Figure 1: (a) Schematic of the short channel double-gate MoS_2 FET using SLG as the S/D contacts. (b) An AFM image showing 10-, 15-, and 20-nm graphene slits.



▲Figure 2: The transfer characteristics of the 15-nm channel length double-gate MoS_2 FET at V_{DS} = 0.05 and 0.5 V.

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A Diamond:H/MoO_3 MOSFET

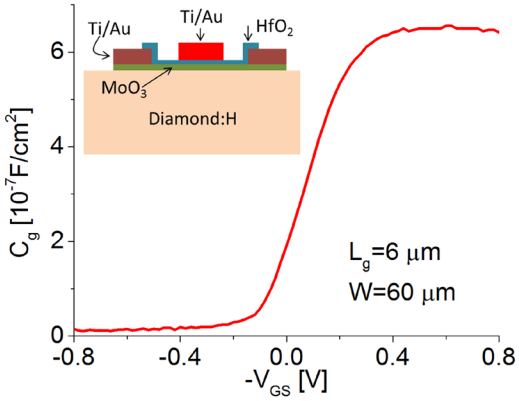
A. Vardi, M. Tordjman (Technion), R. Kalish (Technion), J. A. del Alamo
Sponsorship: Donner Endowed Chair, MIT-Technion Fellowship

Diamond is widely considered the ultimate semiconductor material for the realization of solid-state microelectronic devices. This is due to its unique combination of outstanding mechanical, electrical, and thermal properties, such as extreme hardness, high breakdown electric field, very high thermal conductivity, and high intrinsic carrier mobility at room temperature. Progress in the realization of diamond-based electronic devices has been hampered by the lack of suitable acceptors and donors with low activation energies. This drawback has been partially overcome through the discovery of "surface transfer doping," in which hydrogenated diamond (D:H) is exposed to different surface acceptors with high work function. Charge transfer between the hydrogen-passivated diamond surface and the absorbed species takes place and results in a highly conductive sheet of holes at the diamond sub-surface. The surface transfer doping system that has been most studied consists of D:H exposed to H_2O molecules. However, a major difficulty of the D:H/H_2O system is the gradual desorption of H_2O that occurs at even moderate temperatures (<200˚C). Recently, MoO_3 has been shown to exhibit excellent transfer doping properties with D:H, yielding the highest yet reported areal hole density (up to $1x10^{14}$ cm^{-2}) and showing temperature stability up to at least 350˚C. This makes this system attractive for D:H-based electronic devices. Here, we present the first demonstration of a D:H/MoO_3 transfer-doped MOSFET.

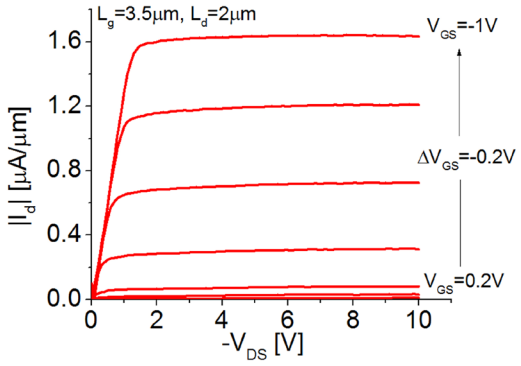
A schematic cross section of our transistor is shown in the inset of Figure 1. The starting substrate is a commercially available 3x3x0.5 mm^3 type IIa (001)-oriented single-crystal diamond. Surface hydrogenation was accomplished by exposure to pure hydrogen plasma in a CVD reactor. This was followed by thermal deposition of 4 nm of MoO_3. Device fabrication starts with mask definition for ohmic contacts followed by Ti/Au evaporation and liftoff. We used 10 nm of HfO_2 deposited by ALD as gate dielectric. Using flowable oxide (FOX) as a mask, the HfO_2 and MoO_3 films are defined by RIE. Following a standard photolithography step, a Ti/Au gate was lifted off.

Capacitance-voltage and current-voltage characteristics of a typical device are shown in Figure 1 and Figure 2, respectively. They both indicate classic p-type MOSFET behavior. High contact resistance limit the device performance, however, this can be mitigated by removing the MoO_3 under the S/D contacts (inset of Figure 1).

Although the results are modest, they clearly indicate the robustness of this new semiconductor heterostructure system, as no special measures were taken to protect the D:H interface during the process, which included several thermal steps up to 200C. Our work rekindles the hope for a future diamond electronics technology with unprecedented performance and robustness.



▲ Figure 1: Capacitance-voltage characteristics at 1 MHz of a typical device. Inset: transistor cross-section schematic.



▲ Figure 2: Output characteristics of L_g=3.5 μm Diamond:H/MoO_3 p-type MOSFET.

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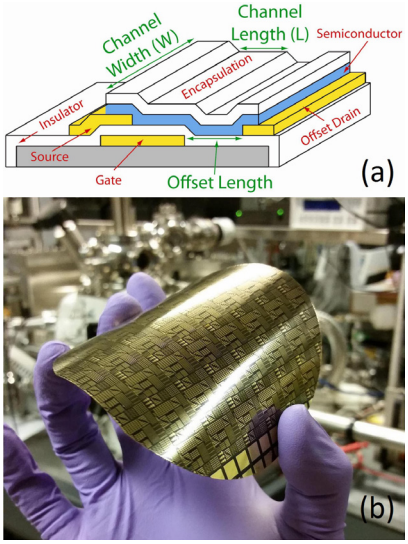
High-Voltage Organic Thin Film Transistor

A. Shih, M. A. Smith, A. I. Akinwande
Sponsorship: DARPA

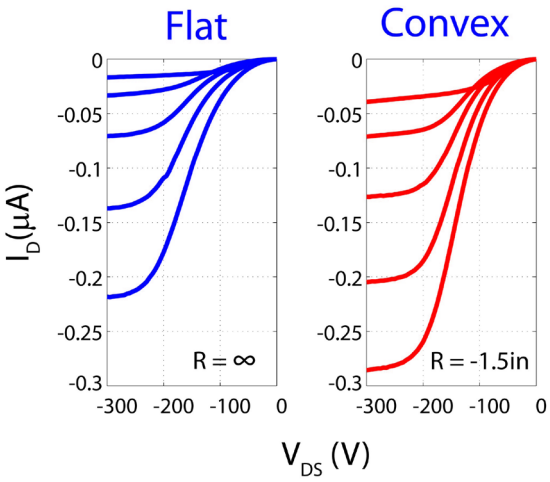
Organic-based thin film transistors (OTFTs) have been identified as excellent candidates for flexible electronics due to the weak van der Waals forces between small molecules. OTFTs can be applied to develop wearable electronics such as artificial skin or sensor-enhanced prosthetics to introduce ubiquitous electronics and sensors on curved surfaces and to create novel compact systems such as a portable x-ray imager. However, enabling truly ubiquitous electronics through OTFTs demands not only a high performance, but also a wide range of operating voltages. Specifically, there are many applications that demand a high operating voltage beyond that capable of a typical thin film transistor. For example, ferroelectric liquid, electrophoretic or electro-optic displays, digital x-ray imaging, poly-Si cold cathodes, and other sophisticated integrated microelectromechanical systems (MEMS) all require large operating voltages to function.

In this work, we are developing a high-voltage organic thin film transistor (HVOTFT) based on the organic semiconductor pentacene ($C_{22}H_{14}$), operable at several hundreds of volts. The design of the pentacene-based HVOTFT is shown in Figure 1 (a). We have employed a bottom contact architecture along with organic compatible dielectrics Parylene-C and BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$), the latter being a high-k material. The pentacene is then thermally evaporated on top of the contacts to form the active thin film (10-20 nm thick). The key design structure is to introduce an ungated region in series with the traditional gated region. The gated region allows for standard transistor switching behavior, while the ungated region enables the high voltage operation by acting as a resistor.

The device has been successfully fabricated on glass substrates as well as on flexible polyimide wafers, as shown in Figure 1 (b). Currently, devices exhibit excellent performances with charge carrier mobility of ~0.01 $cm^2/V•s$, flexibility tolerance up to 1.5 in radius of curvature, and operating voltages beyond 300 V, as shown in Figure 2. Although the devices do exhibit short channel and impeded charge injection into the gated region, recent efforts such as the addition of a field plate above the interface of the gated and ungated regions have proven promising.



▲Figure 1: (a) Cross sectional view of the high-voltage organic thin film transistor. (b) OTFTs made on flexible polyimide substrates.



▲Figure 2: High-Voltage Output Characteristics of HVOTFTs before and after flexure at a 1.5 in radius of curvature. The channel length is 10 μm with a 20 μm ungated region. The channel width is 20 μm. V_{GS} is stepped from 0 V to -20 V in -5 V increments.

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Characterization of $SrRuO_3$ and TaO_x Resistive Switching Memory Devices by Scanning Tunneling Microscopy

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Sponsorship: MIT, National Science Foundation Center for Material Science Research, Forschungszentrum Jülich

Resisitive switching random access memory (Re-RAM) or memristive devices are considered contenders to become the next generation of information storage technology. Re-RAM devices are attractive compared to the current state-of-the-art flash devices due to their lower power consumption, high scalability, simple architecture, faster switching times (under sub-nanoseconds) and longer data retention. Although the technology is highly promising, the switching mechanisms are far from being well understood, thereby limiting the optimization of the Re-RAM device materials. The fundamental questions that need to be addressed on the switching mechanism of these devices include the effects of a strong electric field on defect creation and defect transport and the electronic structure. The inaccessibility of buried oxide films to several characterization techniques also makes the investigations of switching mechanisms more challenging.

In this work, we have induced and characterized localized electronic switching phenomenon under the electric field of the scanning tunneling microscope (STM) tip in a non-contact mode on electronically conducting and insulating oxides, $SrRuO_3$ and TaO_x, respectively. The advantage of this approach is that the switching can be studied at the local level, without necessitating a top electrode that buries the oxide. Localized area-wise switching is demonstrated in both oxides, in an area as small as 25 nm^2 in $SrRuO_3$. Scanning tunneling microscopy in spectroscopy mode provides electronic structure information, allowing us to characterize the switching process in-situ by a single experiment, which was not possible previously. The work highlights the use of tunneling microscope for characterizing diverse memory devices to understand the defect transport mechanisms under applied electric fields and variable oxygen partial pressure.

Carbon Nanotube Network using Silicon Oxide Non-Volatile Switches

A. D. Liao, P. T. Araujo, M. S. Dresselhaus
Sponsorship: Department of Energy

As mobile electronic devices become more prevalent in society, the need for compact and densely packed non-volatile memory (NVM) continues to grow. As flash memory fast approaches its scaling and power limits, other promising NVM technologies are being developed. Among these, resistive random access memory (RRAM) has gained popularity in industry because it utilizes materials that are in common use in semiconductor processing. These metal-insulator-metal (MIM) memory cells operate by switching the insulator between a high resistive state (HRS) and low resistive state (LRS). Whereas the switching mechanism to the LRS is well understood as oxygen atoms being removed from the lattice to form a conductive filament bridging the electrodes, there is not a complete consensus on the switching mechanism to return the MIM device to its HRS. It is known, however, that the type of metal used to contact the insulator may influence this switching mechanism. Furthermore, while it is typical to use a metal oxide7-9 (e.g., AlO_x, HfO_x, TiO_x) in the MIM cell, recently it was discovered that even silicon oxide could be switched between an HRS and an LRS.

In this study, we demonstrate a non-volatile switch that utilizes carbon nanotube networks to electrically contact a conductive nano-crystal Si filament in SiO_2. We sweep a voltage across the device until the CNT network undergoes Joule breakdown, creating a physical gap within the network. While the gap within an individual CNT network may vary from ~10 – 40 nm, the minimum gap size between different networks fluctuates by ± 3 nm. To prevent premature breakdown from oxidation, all measurements are performed in a vacuum (10^{-5} Torr). After the initial breakdown of the network, we observe a coalescence induced mode (CIM) at ~1860 cm^{-1} in the Raman spectrum, which is characteristic of linear *sp* hybridized carbon chains. We note that the temperature needed to induce the coalescence of CNTs is ~2000 K. After breaking the CNT network, we sweep the voltage back to zero where we observe a sudden increase in current at a voltage ~ 50 – 80 % of the breakdown voltage. We can reliably switch the device multiple times between high and low resistive states. Each time we are able to heal the conductivity, in some cases up to ~50 % of its original value. During the reset to the low resistive state, thermal modeling indicates that the filament reaches temperatures of ~600 ˚C, the oxidation temperature of carbon. From this, we conclude that the carbon-oxygen interaction between the CNTs and SiO_2 are responsible for switching the device to a high resistive state.

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Driving Stage for SFQ Circuits using a Single Nanocryotron

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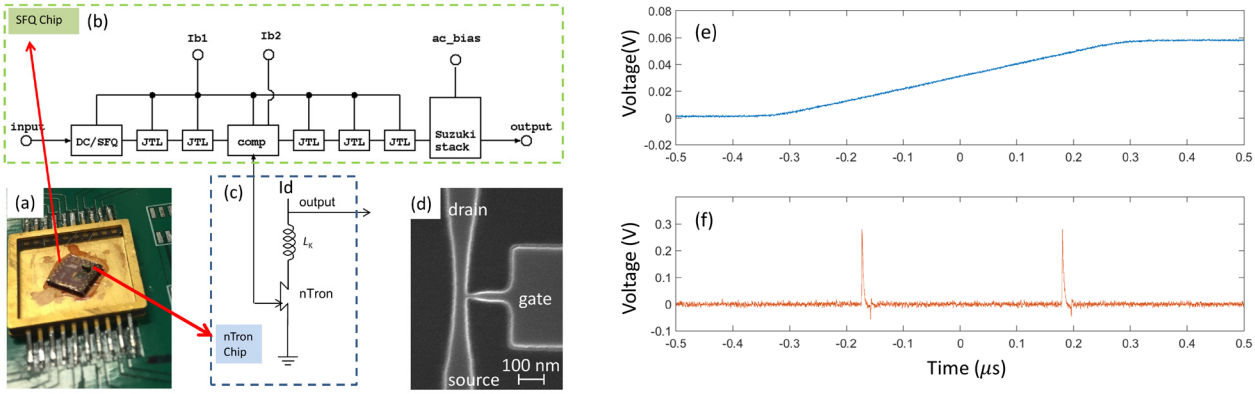
Sponsorship: IARPA, National Science Foundation, Air Force Office of Scientific Research, NASA

Superconducting single-flux-quantum (SFQ) suffers from poor driving capability due to the very low impedance of Josephson junctions. Here, we report a driving stage for rapid single-flux-quantum (RSFQ) circuits using a single nanocryotron (nTron) that may provide new SFQ circuit solutions including compact, energy-efficient word-line drivers for superconducting memory. In this work, we present experimental results of a hybrid circuit, as shown in Figure 1a-1d, showing the translation of a single SFQ pulse to a high-amplitude nTron output pulse, equivalent to 1,000 Φ_0. The SFQ chip had a Josephson comparator that split the output pulse into two. One pulse went to a Suzuki stack for reference monitoring, while the other one fed into the gate of an nTron. The gate width was designed as 40 nm and the channel width as 80 nm (Figure 1d) to maximize the nTron sensitivity.

We measured the dependence of the nTron output on the input of the DC/SFQ converter at 4.2 K. A pulse (Figure 1e) was input to the DC/SFQ block to generate SFQ pulses at its rising edge. The nTron channel was biased at 9 μA, below its critical current of 12 μA. The nTron pulses (Figure 1f), which were 0.45 mV in amplitude and 10 ns wide on a 50 Ω load, were amplified for readout by commercial room-temperature RF amplifiers. When an SFQ pulse was created on the comparator by increasing the DC/SFQ input, we observed both an nTron pulse and a step from the reference Suzuki stack. As the DC/SFQ input increased linearly to generate additional SFQ pulses with a fixed period, the output pulses of nTron showed the same period.

This hybrid interface circuit has a foot-print of only 1 μm² for the sensitive area, is DC-powered, triggered by a single SFQ pulse, offers high output impedance as well as high gain and input isolation. Therefore, it is very attractive for advanced SFQ circuit designs and even enables new circuit solutions such as compact energy-efficient memory word line drivers for superconducting memories.



▲ Figure 1: Hybrid circuit using an nTron to read out SFQ pulses. (a) Test board of the hybrid circuit. The nTron chip (1 mm × 0.5 mm) is glued on top of the SFQ chip (5 mm × 5 mm). (b, c) Schematic diagrams for the SFQ chip and the nTron chip. The output SFQ pulses are from the comparator, which also output pulses to the Suzuki stack for monitoring the SFQ pulses. (d) SEM image of an nTron gate. The gate width is 20 nm. (e) Input pulses to the DC/SFQ. On the rising edge, the current pulse generates two SFQ pulses. (f) nTron output pulses. Each SFQ pulse generated on the rising edge of the DC/SFQ input is successfully read out by the nTron.

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Modeling Superconducting Nanowire Circuits

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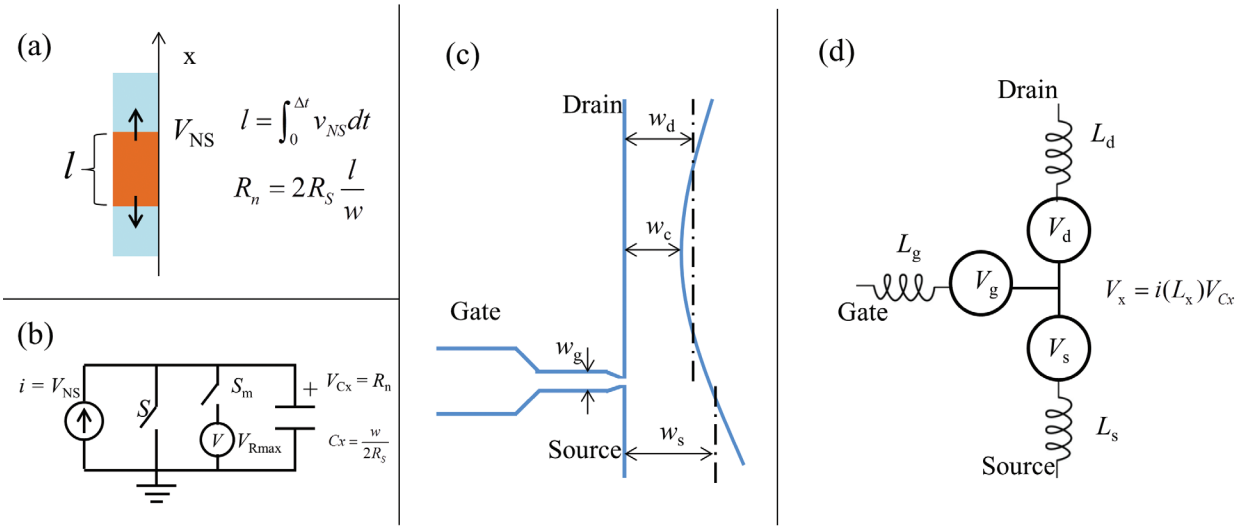
Sponsorship: Air Force Office of Scientific Research, IARPA, iQuise, National Science Foundation, NASA

In this work, we have demonstrated SPICE (Simulation Program with Integrated Circuit Emphasis) models for superconducting nanowire single-photon detectors (SNSPDs) and superconducting nanowire cryotrons (nTrons). We have also designed several circuits which were simulated and optimized by using these models.

To simulate the electro-thermal dynamics of an SNSPD after it switched from superconducting state to resistive/normal state, as shown in Figure 1a, we calculated the velocity of the superconducting-normal boundary v_{NS} which varied over time and current. This calculation was then expressed into a circuit model (Figure 1b). For modeling an nTron which had three terminals (Figure 1c), as shown in Figure 1d, we took each of the three terminals as a superconducting nanowire which had an independent dynamic process based on its geometry and current. The switching conditions in which a gate pulse can trigger the channel were determined by experimental results.

Based on these SPICE models, we simulated several circuits using superconducting nanowires to improve the device performance. We will first show a pulse amplifier using an nTron to read output pulses from an SNSPD. A coupling network with an inductor shunted to ground was used to let the fast-rising edge of the SNSPD pulses trigger an nTron, while decoupling the two devices during the current recovery, to prevent the nanowires from latching. The signal-to-noise ratio of detection pulses was increased, suppressing timing jitter from voltage noise, because the SNSPD pulses were amplified. Additionally, the nTron amplifier worked as a buffer and isolated the SNSPD from the following processing circuits. Then, we extended the single-nTron amplifier to a differential amplifier using a pair of inversely biased nTrons. Thus, if two SNSPD pulses fed into the differential amplifier, the time interval between them could be detected through the pulse-width of the differential output. If the two SNSPD pulses were split from a single SNSPD with a modulated delay, the pulse-width of the differential output could be used as a time-tag to the detector. Thus, such circuits can be used in a time multiplexing SNSPD array for on-chip quantum optics.



▲ Figure 1: SPICE modeling of an nTron. (a) Modeling the growth of a nanowire by tracing the superconducting-to- insulating boundary. (b) Equivalent circuit of a nanowire. (c) Geometry of an nTron. Each port of the nTron is simplified in a nanowire with uniform width. (d) Equivalent circuit of an nTron with three nanowires in different widths, inductance, and bias conditions.

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Magnetic Domain Wall Logic Devices

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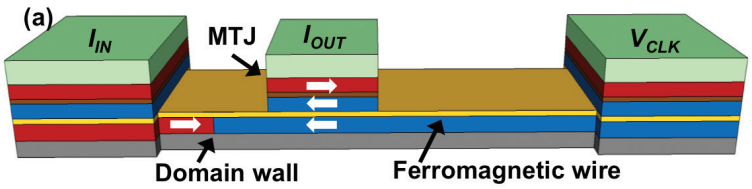
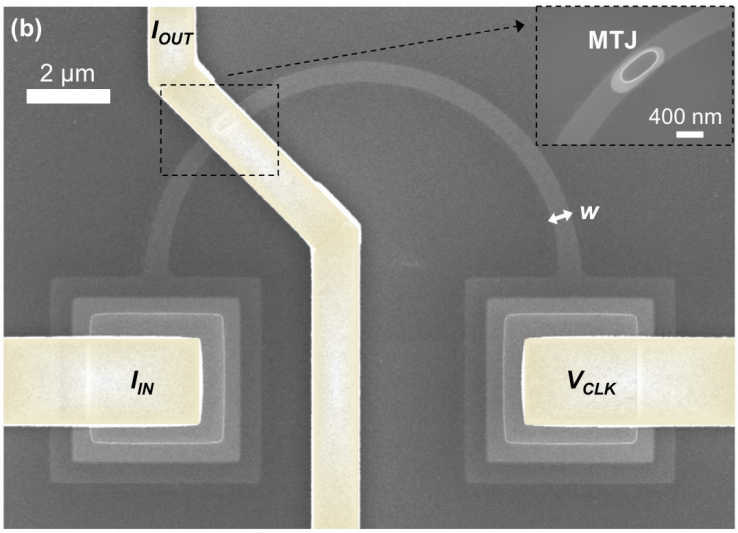
We are working on building logic devices that encode information in a magnetic domain walls. A cartoon of the DW-Logic device is shown in Figure 1. Domain wall motion can operate at very low switching voltages, making magnetic logic a promising contender for more energy efficient computing.

Information is stored in a single transverse domain wall in a CoFeB wire, with magnetization fixed on the wire ends using IrMn antiferromagnetic pinning. The domain wall is translated by a current, and information is read out by a MgO magnetic tunnel junction (MTJ).

We are working on simulations of the device performance, which show that these logic devices have a complete set of Boolean operations and scale to switching energies and voltages below those of CMOS. Our integrated micromagnetics-SPICE model predicted switching energies in IMA devices down to 3×10^{-16} J using 0.1 mV V_{dd} and in PMA devices down to 3×10^{-18} J using 0.003 mV V_{dd}. We are also exploring the magnetic and electrical properties of device prototypes, shown in Figure 2.



◀ Figure 1: Cartoon of magnetic logic device.



▶ Figure 2: Scanning electron micrograph of a logic device prototype.

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