MICROSYSTEMS TECHNOLOGY LABORATORIES
ANNUAL RESEARCH REPORT 2015

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

MIT

MTL 2015

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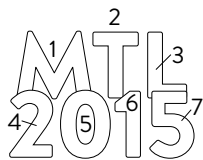
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RESEARCH ABSTRACTS

Foreword

The 2015 Annual Report of the Microsystems Technology Laboratories highlights the research and educational activities of faculty, staff, students, postdocs and visitors associated with MTL during MIT Fiscal Year 2015.

MTL's mission is to foster world-class research, education and innovation at the nanoscale. Nanoscale science and technology can help solve some of the world's greatest problems in areas of energy, communications, water, health, information and transportation, among others. As showcased in this report, MTL's activities encompass integrated circuits, systems, electronic and photonic devices, MEMS, bio-MEMS, molecular devices, nanotechnology, sensors and actuators, to name a few. MTL's research program is largely interdisciplinary. MTL's facilities are open to the entire MIT community and the outside world. Over 600 MIT students and postdocs from 19 different Departments, Laboratories or Centers carried out their research in MTL's facilities in the last fiscal year.

To accomplish its mission, MTL manages a set of experimental facilities in Bldgs. 39 and 24 that host in excess of 150 processing and analytical tools. We strive to provide a flexible fabrication environment that is capable of long-flow integrated processes that yield complex devices while presenting low-barrier access to fast prototyping of structures and devices for a wide range of users. Our fabrication capabilities include diffusion, lithography, deposition, etching, packaging and many others. Our lab can handle substrates from odd-shaped small pieces to 6-inch wafers. The range of materials continues to expand beyond Si and Ge to include III-V compound semiconductors, nitride semiconductors, carbon-based materials, polymers, glass, organics and others.

MTL also manages an information technology infrastructure that supports state-of-the-art computer-aided design (CAD) tools for device, circuit and system design. Together with a set of relationships with major semiconductor manufacturers, this provides access for our users to some of the most advanced commercial integrated circuit processes available in the world today.

MTL could not accomplish its mission without the vision, commitment and generosity of a number of companies that comprise the Microsystems Industrial Group (MIG). The MIG supports the operation of MTL's facilities but it also advises the faculty on research directions, trends and industrial needs. The list of current MIG members can be found in the Acknowledgement section of this report.

In the Fall of 2014, we celebrated the 30th anniversary of the creation of MTL. From an initial emphasis on semiconductors and electronics, over the 30 years of its life, the technologies that underpin MTL's activities and their domains of application have greatly expanded. The 2015 Annual Report is the broadest in scope to date with abstracts describing research on nanoscale transistors, medical devices, microfluidics, organic lasers and perovskite photovoltaics, among many exciting research projects.

The research activities described in these pages would not be possible without the dedication and passion of the fabrication, IT and administrative staff of MTL. Day in and day out, they strive to support MTL users in the pursuit of their goals. They do this in an unassuming manner. Their names do not usually end up in the research papers, but that does not diminish the significance of their contributions. To them and to all of you who support in your own way the activities of MTL, a most sincere thank you!

Jesús A. del Alamo
Director, Microsystems Technology Laboratories
Donner Professor, Department of Electrical Engineering and Computer Science
August 2015

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Circuits and Systems for Information Processing, Communications, Multimedia, Energy Management, and Sensing

12-bit 250MS/s CMOS Pipelined Analog-to-Digital Converter
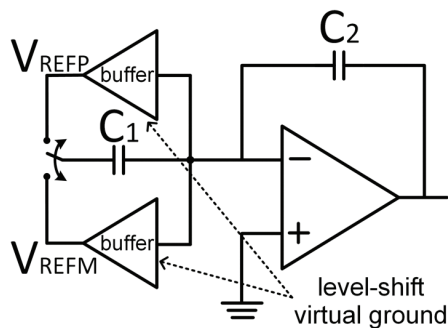
H. H. Boo, H.-S. Lee, D. S. Boning
Sponsorship: Masdar Institute / MIT Cooperative Program

The virtual ground reference buffer technique is introduced as a solution to improve the feedback factor of a closed-loop circuit and is demonstrated in a high performance pipelined CMOS analog-to-digital converter (ADC) prototype. The technique enhances the performance of switched-capacitor circuits by improving the feedback factor of the op-amp without affecting the signal gain. The bootstrapping action of level-shifting buffers relaxes op-amp performance requirements in unity-gain bandwidth, noise, open-loop gain, and offset compared with conventional circuits. The improvements substantially reduce the design complexity and the power consumption of the op-amps in applications such as ADCs.
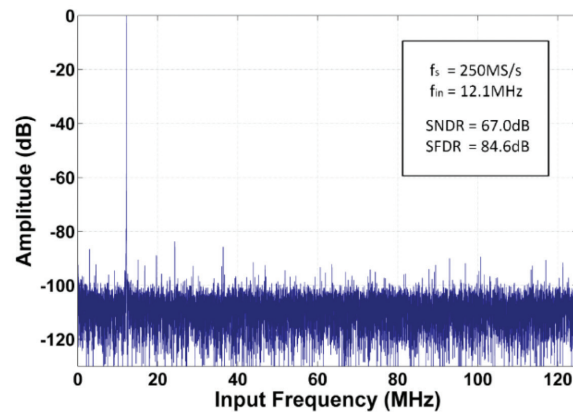
The proposed virtual ground reference buffer technique in its charge-transfer phase is shown in Figure 1. Similarly to conventional pipelined ADC circuits, C_2 flips around the op-amp and C_1 is driven by either the positive or negative reference voltage. Here, however, the reference voltages are referenced to the virtual ground node instead of the system ground, and they are generated by level-shifting the virtual ground potential. Assuming an ideal buffer, any change in the virtual ground node voltage is reflected at the output of the buffer, effectively bootstrapping C_1 away. Therefore, the C_1 capacitance is removed from the feedback network of the op-amp, resulting in an ideal unity feedback factor independent of the signal gain. The unity feedback factor improves the closed-loop bandwidth and op-amp noise referred to the ADC input by a factor of the signal gain compared with the conventional circuit. Also, op-amp open-loop gain and offset requirements are reduced by a factor of the signal gain.

The proof-of-concept chip was fabricated in 65 nm CMOS technology. Figure 2 shows the output spectra with input frequencies of 12.1MHz at the sampling rate of 250MS/s. SNDR of 67.0dB (10.84-b ENOB) and SFDR of 84.6dB are achieved. The DNL and INL are within -0.86/+0.52 LSB and -0.90/+1.08 LSB, respectively. The chip operates from a 1.2V power supply and consumes 49.7mW at 250MS/s.

▲ Figure 1: Proposed virtual ground reference buffer technique.

▲ Figure 2: Measured spectrum from f_{in}= 12.1MHz and f_s = 250MS/s

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Time-Interleaved A/D Converters

D. P. Kumar, H.-S. Lee
Sponsorship: Masdar Institute of Science and Technology

The demand for high-resolution and high-accuracy A/D converters in communication systems continues to increase. To raise the sampling rates to the GHz range in a power-efficient manner, time-interleaving is an essential technique whereby N A/D channels, each operating at a sampling frequency, f_s, are used to achieve an effective conversion speed of Nf_s, as illustrated in Figure 1.

While time-interleaving enables higher conversion rates in a given technology, mismatch issues such as gain, offset, and sampling clock skew errors between channels degrade the overall A/D performance. Of these issues, sampling clock skew between channels is the biggest problem in high-speed and high-resolution, time-interleaved A/D as errors due to sampling clock skew become more severe for higher input frequencies. A few sources of sampling clock skew between channels exist. Mismatches in the sampling clock path and logic delays are the most obvious. Input signal routing mismatch and RC mismatch of the input sampling circuits also cause sampling clock skew. Previous calibration techniques employ either analog and digital timing adjustment or digital calibration of output data. The timing adjustment requires an adjustable delay resulting in increased sampling jitter, which cannot be compensated by calibration. The digital calibration of output data requires complex interpolation.

In this research, we are developing a simpler calibration algorithm for sampling clock skew correction whereby the input signal delay is adjusted by controlling the resistance of the input sampling network. The variable time-constant of the input sampling network will result in a linear delay of the input signal if the RC time constant of the input sampling network is much greater than $1/f_{in,max}$, where $f_{in,max}$ is the maximum input signal frequency. This sampling method allows for finely tuned timing-skew corrections, and the impact on noise or power consumption of the system is negligible. A prototype 12-bit, 200MS/s, 4-way time-interleaved A/D implementing the proposed correction technique was taped out in a 65-nm LP CMOS process and is currently being characterized.
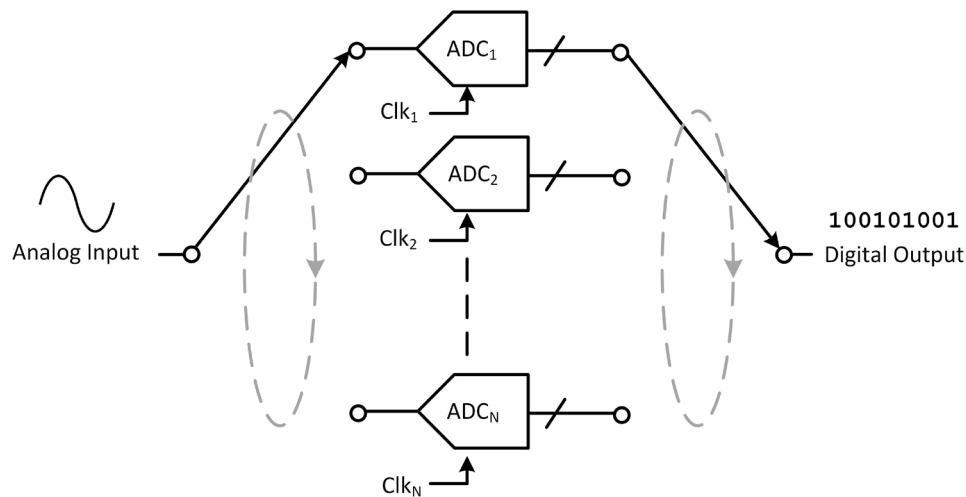
▲ Figure 1: Block diagram of a time-interleaved (TI) A/D converter.

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# A Flash ADC with a Reduced Number of Comparators

X. Yang, S. Bae, H.-S. Lee
Sponsorship: MIT/MTL GaN Energy Initiative, Office of Naval Research, Samsung

High-speed and low-resolution flash analog-to-digital converters (ADCs) are widely used in applications such as 60-GHz receivers, series links, and high-density disk drive systems, as well as in quantizers in delta-sigma ADCs. In this project, we propose a flash ADC with a reduced number of comparators by means of interpolation. One application for such a flash ADC is a GaN/CMOS hybrid delta-sigma converter. The GaN first stage exploits the high-voltage property of the GaN while the CMOS backend employs high-speed, low-voltage CMOS. This combination may achieve an unprecedented SNR/bandwidth combination by virtue of its high input signal range and high sampling rate. One key component of such an ADC is a flash ADC. To take advantage of the high signal-to-thermal-noise ratio of the proposed system, the quantization noise must be made as small as possible. Therefore, a high-speed, 8-bit flash ADC is proposed for this system. Figure 1 shows the block diagram of the ADC architecture. Sixty-five comparators are used to achieve the 6 most

significant bits (MSBs). Sixty-four interpolators are inserted between the comparators to obtain two extra bits. The input capacitance of this design is only ¼ of the conventional 8-bit flash ADC. Therefore a higher operating speed can be achieved. We introduced gating logic so that only one interpolator is enabled during operation, which reduces power consumption significantly. A high-speed, low-power comparator with low noise and low offset requirements is a key building block in the design of a flash ADC. We chose a two-stage dynamic comparator, as in Figure 2, because of its fast operation and low power consumption. With the scaling of CMOS technology, the offset voltage of the comparator keeps increasing due to greater transistor mismatch. A popular offset cancellation technique is to digitally control the output capacitance of the comparator. However, this technique reduces the speed of the comparator because of the extra loading effect. In this project, we also propose a novel offset compensation method that eliminates the speed problem.
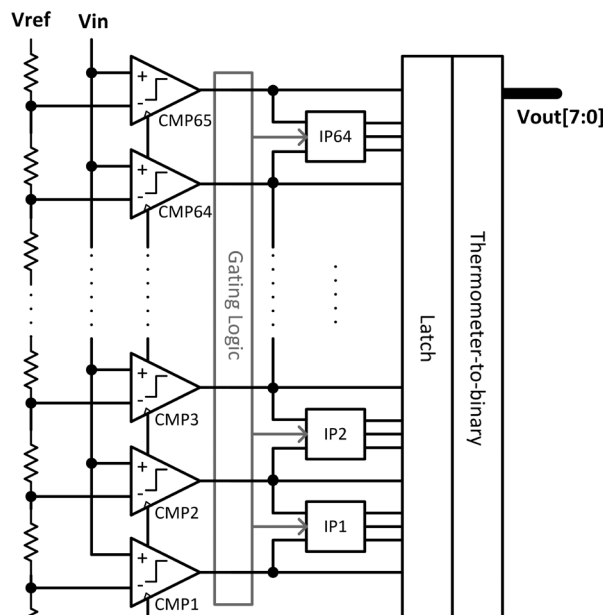
▲ Figure 1: Flash ADC architecture, with 65 comparators and 64 2-bit interpolaters.
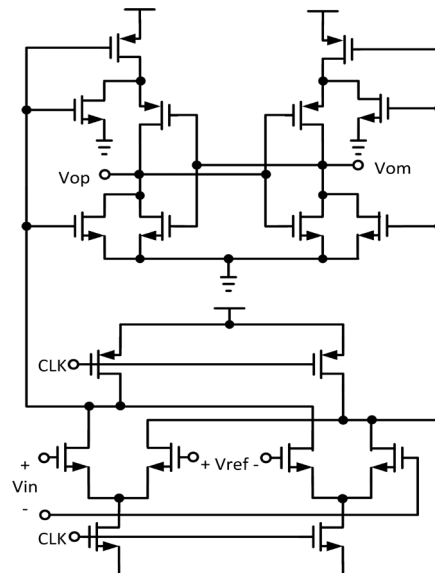
▲ Figure 2: Schematic of the two-stage dynamic comparator.

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Continuous-Time Delta-Sigma Modulator for Next-Generation Wireless Applications

D.-Y. Yoon, H.-S. Lee
Sponsorship: MediaTek, Inc., Korea Foundation for Advanced Studies

As wireless communication technology is rapidly advancing, new wireless applications are continuously developed. Figure 1 shows each application space and the required dynamic range. The new wireless applications demand wide bandwidth (≥50 MHz) and high resolution (≥14 bits) data converters. A continuous-time (CT) delta-sigma modulator (ΔΣM) is suitable for the demanding new wireless applications due to its high-resolution, wide-bandwidth, and low-power characteristics. In addition, a CT ΔΣM provides an inherent anti-aliasing property. Several state-of-the-art CT ΔΣMs reported recently achieved signal bandwidths greater than the 50 MHz appropriate for the next generation wireless communication. However, the resolution and power consumption still need to be improved.

This project focuses on the design of a CT ΔΣM, specifically for modern wireless communication applications. Quantization noise is suppressed aggressively by increasing the effective order of a noise transfer function (NTF) of a ΔΣM, instead of increasing the order of a loop filter, to mitigate a stability requirement. To increase the effective order of an NTF, the proposed CT ΔΣM is implemented based on a 2-loop sturdy multi-stage noise-shaping (SMASH) architecture, previously reported in a DT ΔΣM. Figure 2 shows the block diagram of the proposed CT SMASH ΔΣM. With a wider signal bandwidth, the proposed CT SMASH ΔΣM provides a better quantization noise suppression capability than the original DT SMASH ΔΣM by canceling the quantization noise from the first loop, not simply   shaping it. The CT SMASH ΔΣM is implemented with several circuit techniques appropriate for high operation speed. These circuit techniques allow the proposed CT ΔΣM to achieve performance metrics for modern wireless communication applications. As a result, the prototype fabricated in 28 nm CMOS achieves DR of 85 dB, peak SNDR of 74.6 dB, SFDR of 89.3 dBc, and Schreier FOM of 172.9 dB over a 50 MHz bandwidth at a 1.8 GHz sampling frequency.
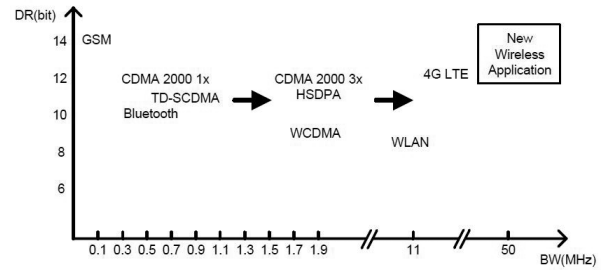
▲ Figure 1: Dynamic range and bandwidth requirements of ADCs in wireless applications.
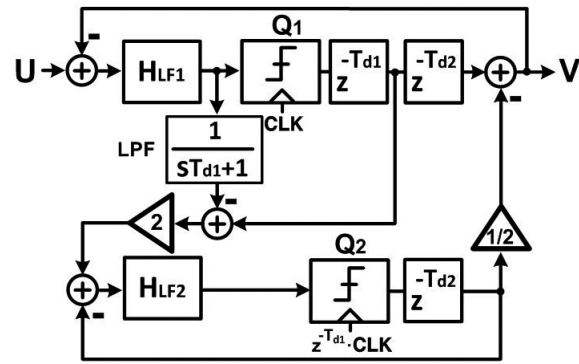
▲ Figure 2: Block diagram of a CT SMASH ΔΣM.

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Ultra High-Performance GaN-on-Silicon Analog-to-Digital Converters

S. Chung, X. Yang, H.-S. Lee
Sponsorship: MIT/MTL GaN Energy Initiative, Office of Naval Research

In this research, we investigate ultra high-performance analog-to-digital converters (ADCs) for diverse emerging applications including personal communication, health care, and an optical backbone network. The low supply voltage of deeply scaled complementary metal oxide semiconductor (CMOS) transistors limits the dynamic range of ADC input signals, thus becoming a fundamental barrier to the performance of silicon ADCs. Recently, high-electron-mobility transistors based on gallium-nitride (GaN HEMTs) are reported with many advantages over the existing compound semiconductor technologies. Operating GaN HEMTs at a very high voltage (30+ V) allows much higher signal-to-noise ratio (SNR) in ADCs than that of CMOS ADCs at given power consumption. A hybrid technology, which monolithically integrates GaN HEMTs with Si-CMOS transistors (GaN-on-Si), will take advantage of both technologies, enabling revolutionary mixed-signal performance (Figure 1). We focus on the design of unprecedentedly high-performance ADCs in a GaN-on-Si hybrid technology (Figure 2). As the first step, we have been developing an over-100-dB SNR GaN sampler for a GaN/Si hybrid pipeline ADC. In addition, we have been investigating the design of a high voltage GaN operational amplifier for a continuous-time delta-sigma ADC with a very high dynamic range.

In the last year, we designed two different GaN track-and-hold (T/H) circuits. The first 250-MS/s T/H was fabricated in a commercial GaN foundry where transistors are optimized for power applications with either low leakage or high gain. These device choices necessitated a two-stage sampler design. The second design operates at a higher speed, 1-GS/s. This circuit was fabricated in a GaN technology that was developed at MTL. This technology offered higher f_t at a lower breakdown voltage. Innovative design techniques allowed a single-stage sampler for a higher sampling rate while avoiding the reverse overvoltage and leakage issues.
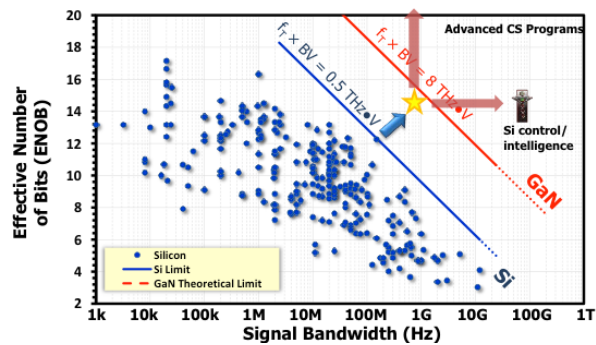
▲ Figure 1: Revolutionary ADC performance expected from the monolithic GaN-on-Si integration [Raman 2012].
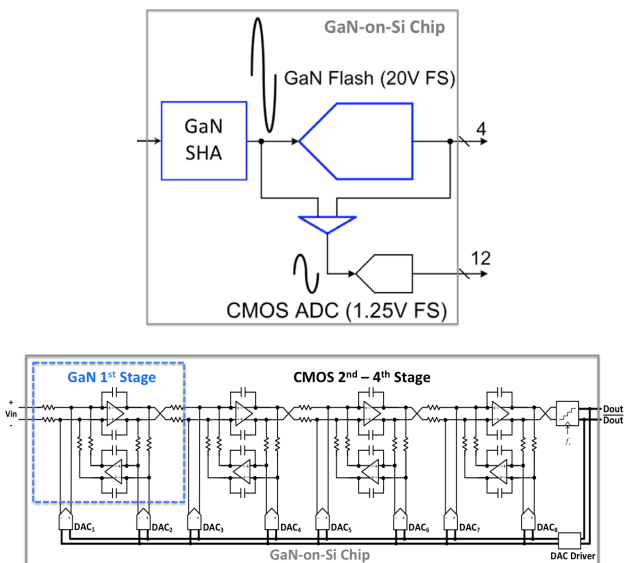
▲ Figure 2: High-performance ADC architecture in GaN-on-Si hybrid technology: (top) pipeline architecture for wide bandwidth. (bot) continuous-time delta-sigma architecture for high dynamic range.

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High-Efficiency, Low-Leakage RF Transmitters for Low Duty Cycle Applications

A. Paidimarri, N. Ickes, A. P. Chandrakasan
Sponsorship: Shell, Texas Instruments

With the convergence of ever-improving wireless and energy management technologies, Internet-of-things (IOT) devices for home, industrial, and environmental monitoring have brought significant improvements to lifestyle, safety, and efficiency. Despite these advancements, energy efficiency remains a significant bottleneck, leading to short device lifetimes. This work focuses on RF transmitter optimizations in ultra-low duty cycle applications such as machine vibration monitoring, where time constants of wear and tear are long (hours to days). In this scenario, it is just as important to optimize the leakage power as it is to optimize on-performance.

Figure 1 shows the complete block diagram of our Bluetooth low-energy (BLE) transmitter. It operates from a 0.68V supply, where both the switching losses and leakage power are reduced. RF circuits that need a higher voltage for improved efficiency (for example high-Q tunable capacitors) are powered by a voltage doubler that generates 1.2V. In order to have large communication range, the power amplifier is designed

for an output power of +10dBm. A resonant input drive and inductive biasing of the output help achieve high efficiency. The chip also includes a crystal oscillator, PLL, and digital baseband.

Most blocks in the system are power-gated with high-V_T thick-oxide power switches. The on-performance of the switches is improved by turning them on strongly with the 1.2V supply, while the off-leakage is strongly cut off though negative V_{GS} biasing. In order to avoid efficiency penalty due to power switches in the PA, which is the most power-hungry component in the system, the negative biasing is applied to the thin-oxide PA device itself. This achieves significant leakage reduction (up to 100×, as shown in Figure 2) without efficiency degradation. The negative voltage of −0.2V is generated by a charge pump and associated oscillator (Figure 1). The design achieves 43.7% system efficiency generating +10.9dBm, and leakage power of 370pW, for an on/off ratio of 7.6×10⁷. This transmitter architecture could enable sub-nW IOT devices.
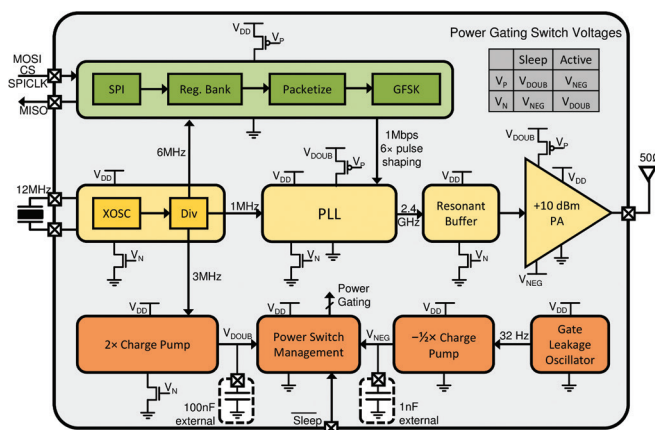
▲ Figure 1: Block diagram of the BLE transmitter. It shows the digital baseband; RF signal chain including crystal oscillator, PLL, and PA; and leakage management blocks including negative V_{GS} generating charge pump and a 32-Hz oscillator.
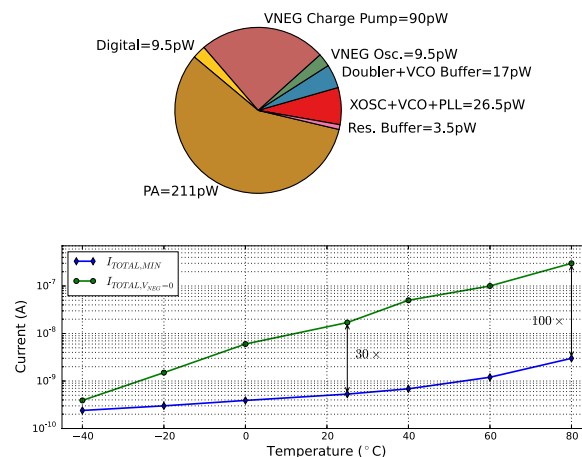
▲ Figure 2: Some leakage measurement results. The pie chart shows the distribution of leakage in various blocks. The total leakage is 370pW. The lower graph shows a 30 to 100× leakage reduction due to the negative V_{GS} biasing technique.

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# Broadband Inter-Chip Link Using Terahertz Wave on Dielectric Waveguide

J. Holloway, R. Han
Sponsorship: Office of Naval Research, MIT Lincoln Laboratory

The development of data links between different microchips of an on-board system have encountered a speed bottleneck due to the excessive transmission loss and dispersion of the traditional inter-chip electrical interconnects. Although high-order modulation schemes and sophisticated equalization techniques are normally used to enhance the speed, they also lead to significant power consumption. Silicon photonics provide an alternative path to solve the problem, thanks to the excellent transmission properties of optical fibers. However, the existing solutions are still not fully integrated (e.g., off-chip laser sources are needed) and require process modification to the mainstream CMOS technologies.

In this project, we aim to utilize a modulated Terahertz (THz) wave to transmit broadband data. Similar to the optical link, the wave is confined in dielectric waveguides, with sufficiently low loss (~1dB for 10-cm length) and bandwidth (>100GHz) for board level signal transmission (Figure 1). In commercial CMOS/BiCMOS platforms, we have previously demonstrated high-power THz generation with modulation, frequency up-conversion, and phase-locking capabilities. In addition, a room-temperature Schottky-barrier diode detector (in 130-nm CMOS) with <10pW/Hz$^{1/2}$ sensitivity (antenna loss excluded) is also reported. The proposed data link will leverage these blocks in order to achieve > 100Gbps/waveguide transmission rate with sub pJ/bit energy efficiency. Our current efforts are focused on the design of a chip-to-fiber THz coupler. Different from previous couplers (<140 GHz) using off-chip antennas, our THz coupler can be implemented entirely with the metal backend of a CMOS process, and does not require any post processing (such as wafer thinning). The structure is also fully shielded, so that there is no THz power leakage into the silicon substrate. Conventional on-chip radiators using ground shield work are resonance type (e.g., patch antenna) and only have <5% bandwidth. In comparison, our design is based on a traveling-wave, tapered structure, and exhibits <3dB insertion loss across a ~60-GHz bandwidth (Figure 2).

(a)

(b)

(c)
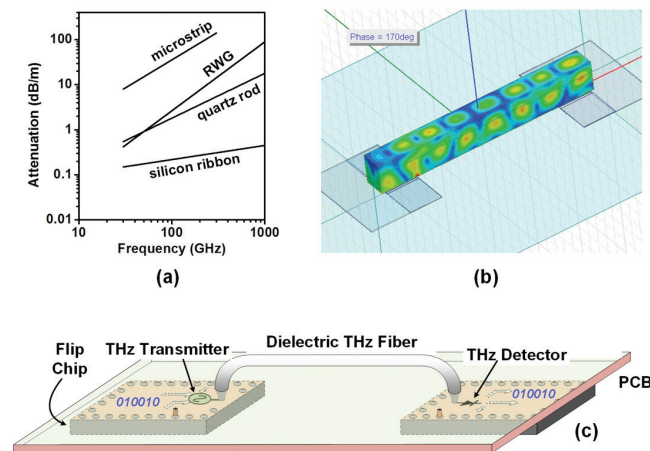
▲ Figure 1: A conceptual illustration of the inter-chip link using THz waveguide (bottom), typical attenuation of various waveguides [1] (top left) and the simulated field of the wave coupled from a chip to a dielectric waveguide (ε_r=6).
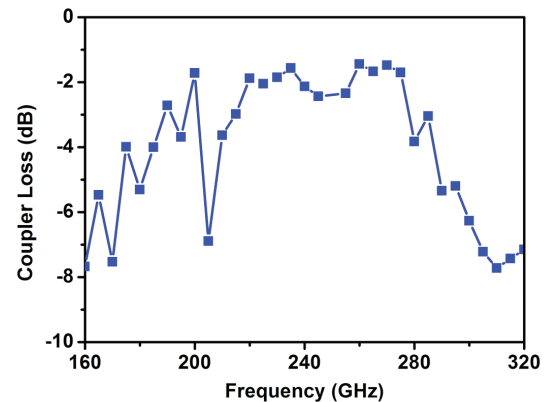
▲ Figure 2: The simulated loss of the proposed on-chip coupler design. The bandwidth for <3dB loss is ~60 GHz.

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Monolithic GaN-MMIC MEMS-Based Oscillators

B. Bahr, L.C. Popa, D. Weinstein
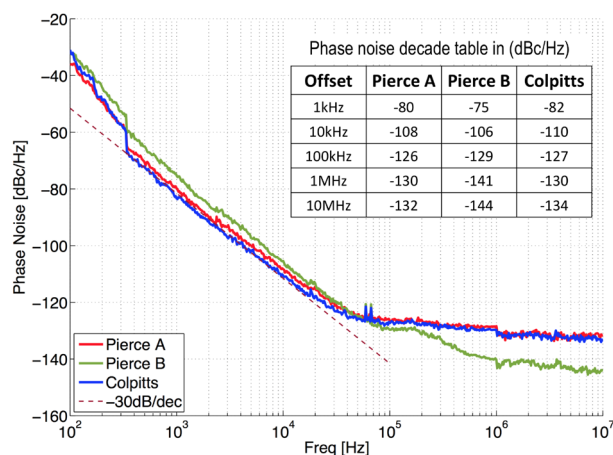Sponsorship: DARPA DAHI Program, DARPA UPSIDE Program

Low phase noise oscillators are critical components in the front end of any communication system. Due to an ever-growing demand for higher data rates and reduced size, weight, and power consumption, efforts to integrate high-Q GHz frequency MEMS resonators with standard circuit technologies have grown dramatically. This work is the first demonstration of a single-chip 1 GHz closed-loop monolithic MEMS-based oscillator circuit implementing both passive and active devices in a standard GaN-MMIC platform, which is a growing technology for various RF front-end applications.

Colpitts and Pierce oscillators were designed and fabricated alongside GaN MEMS Lamb-mode resonators operating at 1 GHz on the same die to realize monolithically integrated GaN-MEMS oscillators. Figure 1 shows an optical photo of the monolithic Colpitts oscillator, including the MEMS GaN resonator. 2DEG resistors and MIM capacitors incorporated into the standard MMIC process were used for passive components. Fabrication of the oscillator circuit, including the monolithic MEMS resonator and the active HEMT core was carried out in MIT Microsystems Technology Laboratories. Figure 2 shows the measured phase noise of both Colpitts and Pierce oscillators. With power consumption of 1.5 mW, both oscillator topologies out-perform state of the art oscillators of comparable sized devices, a direct result of the significant reduction of parasitics afforded by monolithic integration as well as the high quality factor of the MEMS resonator.
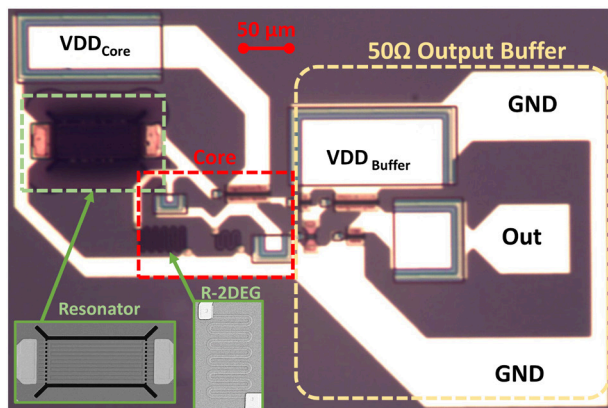
▲ Figure 1: Monolithic Colpitts GaN-MEMS oscillator, showing lamb-mode resonator, 2DEG resistor as well as the core circuit.

Phase noise decade table in (dBc/Hz)			
Offset	Pierce A	Pierce B	Colpitts
1kHz	-80	-75	-82
10kHz	-108	-106	-110
100kHz	-126	-129	-127
1MHz	-130	-141	-130
10MHz	-132	-144	-134

▲ Figure 2: Measured phase noise performance of the Pierce and Colpitts oscillators, both operating at 1GHz .

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Vertical Noise Coupling Mitigation in 3D-IC Using a Solenoid Inductor

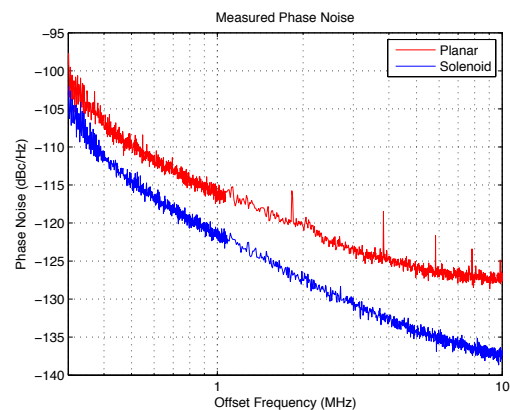G. Yahalom, A. Wang, A. P. Chandrakasan
Sponsorship: MediaTek

Three-dimensional integrated circuits (3D-IC) have the potential to meet the demand for higher system performance and data rates, while avoiding the increase in cost of scaled CMOS technologies The ability to stack multiple dies vertically will allow integration of complex systems in a small footprint with short, low-parasitic interconnects. Previous work has shown power and bandwidth benefits of 3D stacking for integrating logic and memory. Designing in three dimensions opens up new possibilities for system- and block-level design; however, care must be taken due to challenges arising from thermal distribution, mechanical stress, power integrity, and signal integrity.

In this work we explore integration of logic devices with RF circuits. Such coexistence may be hindered due to inductive and capacitive coupling between the tiers. Here, a vertical solenoid inductor in 3D-IC is presented to improve the quality factor of the structure and minimize coupling between tiers. The potential coupling between stacked die tiers is shown in Figure 1 for different inductor structures. The bottom tier die contains signal lines that emulate part of a high-speed digital clock tree. Directly above the clock lines, two different integrated inductor structures were fabricated: the proposed solenoid and a conventional planar structure as a reference design. The planar inductor utilizes the top metal layer and has a patterned ground shield. The solenoid inductor uses the through silicon vias themselves as part of the inductor structure and the redistribution layers on both the top and bottom die tiers. The measured phase noise of two voltage-controlled oscillators using these inductors is plotted in Figure 2. The higher inductance and lower resistance of the solenoid results in a ~70% higher quality factor and lower phase noise. Furthermore, the planar inductor exhibits spurs due to an adjacent low-frequency digital clock, whereas the solenoid does not exhibit spikes due to the clock.
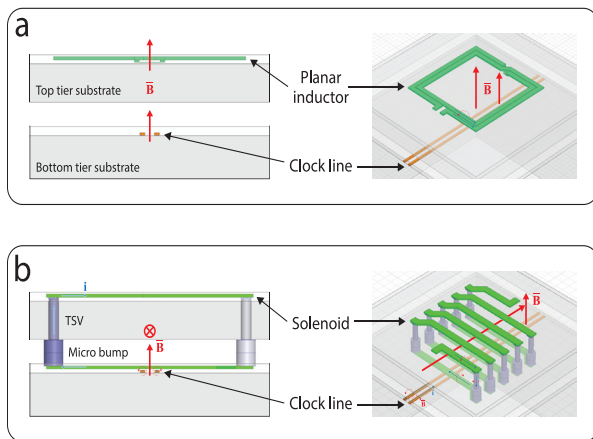
▲ Figure 1: Illustration of 3D-IC stack with clock lines, (a) planar and (b) solenoid inductor structures, along with current directions and magnetic field lines (figure not to scale).

▲ Figure 2: Phase noise measurement of planar (red) and solenoid (blue) inductor-based voltage- controlled oscillators with the presence of an on-chip low speed digital clock.

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Energy and Area-Efficient Hardware Implementation of HEVC Inverse Transform and Dequantization

M. Tikekar, V. Sze, A. P. Chandrakasan
Sponsorship: Texas Instruments, National Science Foundation

High Efficiency Video Coding (HEVC) achieves a 50% reduction in bit-rate over Advanced Video Coding (H.264/AVC) at the same visual quality. A key feature of HEVC is the use of large 16×16 and 32×32 inverse discrete cosine transforms (IDCTs), a new 4×4 inverse discrete sine transform, and high-precision 4×4 and 8×8 IDCTs. However, this new feature raises several challenges for hardware implementations which we have addressed in our work.

Designing for all the transform sizes (4×4 - 32×32) requires complex control as they need different cycle counts. We developed a pipelining scheme to process all sizes with at least 2 pixels/cycle throughput. Further, we use zero-column skipping to increase throughput by 63%. Zero-column skipping also decreases the number of signal transitions, which reduces energy by 30%.

The large and high-precision transforms have 8× higher computational complexity, which affects both area and energy. To address the area problem, a Multiple Constant Multiplication-based method had previously

been proposed. We improved the energy efficiency of the design by 17% using data-gating at the cost of 4% area.

The HEVC inverse transform needs a 16 kbit transpose memory as compared to 1 kbit for H.264/AVC. The large transpose memory needs to use static random access memory (SRAM), which is denser but slower and less flexible than registers that are used for H.264/AVC. We used a combination of 4 single-port SRAMs and a small register cache to achieve the desired throughput in a small area.

We implemented the inverse transform and dequantization engine in TSMC 40 nm CMOS. The design, shown in Figure 1, has an area of 126 kgates and energy consumption of 11.9 pJ/pixel. Energy consumption depends on the data being processed. We observed that large transforms typically contain more zeros. Our zero-column skipping method exploits this observation to process the large transforms with better energy efficiency as seen in Table 1.
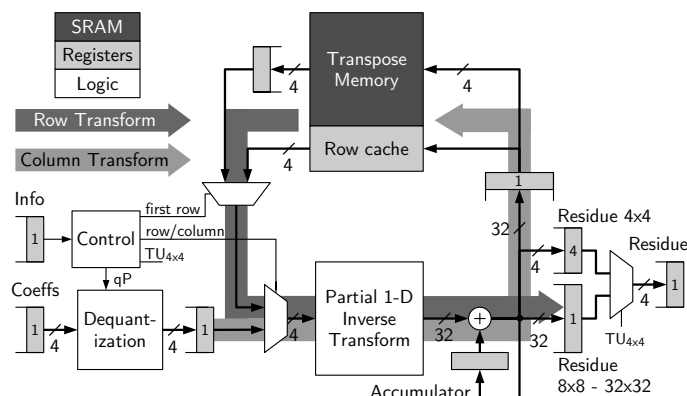
▲ Figure 1: Architecture of inverse transform and dequantization engine.

Transform size	Fraction of zeros in data	Energy (pJ/pixel)
4×4	85.0%	9.7
8×8	95.5%	11.4
16×16	97.6%	12.6
32×32	99.5%	12.2

▲ Table 1: Exploiting the higher fraction of zeros in large transform to improve energy efficiency.

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A Navigation Device with 3-D Computer Vision Processor for Visually Impaired People

D. Jeon, N. Ickes, P. Reina, I. Ananthabhotla, H. C. Wang, D. L. Rus, A. P. Chandrakasan
Sponsorship: Andrea Bocelli Foundation, Texas Instruments

Computer vision is an emerging area for mobile systems, and there is an increasing need for various applications such as autonomous navigation, gesture recognition, and face identification. In this project, we seek to build a 3-D vision processor targeting multiple applications that achieves good reconfigurability and energy efficiency. We first take a navigation device for the visually impaired as a primary application since it requires various processing algorithms such as surface normal calculation and region growing. The proposed processor will be demonstrated as a core processing part of the entire navigation system.

The portable navigation system processes depth image data captured by a Time-of-Flight camera to detect obstacles in front and inform the user of safe areas to walk (Figure 1). The system must operate for at least few hours relying on a small battery, making the power consumption a key design constraint. We are implementing a low-power computer vision processor by exploring multiple design spaces ranging from algorithmic optimization and architecture improvement to maximize energy efficiency. We also focus on developing algorithms to save LED illumination power since it can easily outweigh energy savings from the processor. The algorithm will dynamically tune configurations of the ToF camera such as illumination power and refresh rate based on sensory inputs.

Another important direction of our research is miniaturization of the navigation system. The navigation device must be in a small form factor so that it is not easily noticeable for social reasons. We are developing a customized system consisting of an image sensor and peripheral ICs of a ToF camera, FPGA chip and the proposed ASIC vision processor. The system will directly process data captured by on-board ToF camera and detect safe walkable areas. This information will be transferred via Bluetooth to an external haptic array, which gives vibratory feedback to the user.
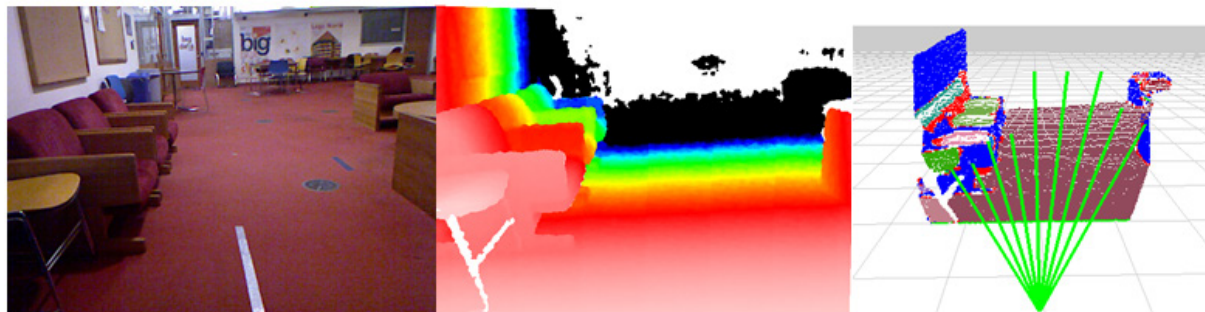
▲ Figure 1: Original color (left) and depth image (center) captured by RGB-D camera. Processed depth image reveals possible obstacles with different colors and provides walkable distance in different directions (right).

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Energy-Efficient Hardware for Multi-Modal Object Detection

A. Suleiman, Z. Zhang, V. Sze
Sponsorship: Texas Instruments, DARPA

Object detection is needed in many embedded applications, such as surveillance, advanced driver assistance systems (ADAS), consumer electronics, and robotics. Real-time and high throughput are necessary for applications such as ADAS and unmanned aircraft vehicles (UAV) to allow more time for course corrections in case of quick changes in the environment. On the other hand, high-resolution images enable early detection by having enough pixels to identify objects at a distance. Finally, in both navigation and portable devices, energy-efficient object detection is desirable because of the energy-limited battery. In this project, a dedi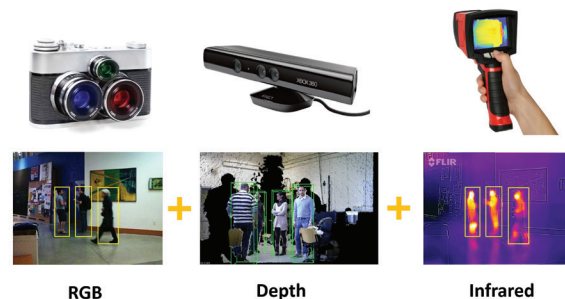cated application-specific integrated circuit (ASIC) is implemented for histogram of oriented gradients (HOG)-based object detection. Unlike most existing low-power hardware object detectors, this architecture supports multi-scale detection for robustness as shown in Figure 1. The image pyramid is generated on the fly, resulting in 3x more pixels to process. HOG features are then extracted for each scale and classified with a support vector machine (SVM). This detection system can process 1080 HD videos at 60 fps, supporting 12 scales per frame, and consuming only 45.3 mW using 45-nm silicon-on-insulator (SOI) complementary metal–oxide–semiconductor (CMOS) technology.

Our next step is to leverage multi-modality to further boost the detection accuracy. These additional sources, shown in Figure 2, complement the visual red-green-blue (RGB) data and hence enable a vision system to function under challenging but important environments like dark scenes. It has been demonstrated in the literature that these sensors can significantly boost the performance of object detection and recognition systems. However, unlike RGB cameras, the output of these sensors is noisy, low in resolution, and sometimes incomplete. Therefore, it is important to properly process and fuse them with RGB data. We are investigating solutions to these challenges from both algorithmic and hardware perspectives. In the end, we expect to deliver a robust object detection system working on multiple sources in different environments while still delivering energy-efficient, real-time, and high-throughput processing.

▲ Figure 1: SVM template for pedestrian detection is shown. The template is used to process each level of the image pyramid, hence detecting pedestrians with different sizes/distances in the scene.

▲ Figure 2: RGB, depth, and infrared images captured from different sensors for pedestrian detection. By fusing them correctly, we can enhance the robustness and performance of our detector.

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A Deeply Pipelined CABAC Decoder for High Efficiency Video Coding Supporting Level 6.2 High-Tier Applications

Y.-H. Chen, V. Sze
Sponsorship: MIT

High Efficiency Video Coding (HEVC) is expected to be the mainstream video compression standard for the next decade. This promise is based on the fact that HEVC provides 2x higher coding efficiency than the current mainstream standard H.264/AVC. However, in addition to supporting high coding efficiency, high throughput is also needed for higher resolutions and frame rates. The key component comes down to the context adaptive binary arithmetic coding (CABAC) entropy decoder, which is a well-known throughput bottleneck due to its highly serial processing algorithm. Low CABAC throughput not only restricts the throughput of the whole HEVC decoder but also limits the room for decoder to trade off throughput for low-power operation using voltage scaling.

This work aims to develop an implementation that maximizes the throughput of an HEVC CABAC decoder. Leveraging CABAC throughput improvement features introduced by HEVC can address two design aspects: high clock rate and multi-bin per cycle decoding. First, high clock rate is achieved by using a 5-stage deeply pipelined architecture as shown in Figure 1. This design reaches 2.2x higher clock rate than the 2-stage architecture adopted by many previous works. To reduce stalls caused by serial feedback dependencies in CABAC, state prefetch logic and latch-based context memory are proposed. The clock rate reaches 1.6 GHz after place-and-route using an IBM 45-nm SOI process, and the impact of stalls is reduced to only 12%. Second, this work adopts separate finite state machines that can decode at most one context-coded bin or two bypass bins per cycle. This feature benefits the decoding of high bit-rate and high demanding bitstreams as shown in Figure 2. The design reaches up to 1.06 bin/cycle for common test sequences and thus achieves throughput up to 1696 Mbin/s, which is sufficient to decode in real-time high-tier video bitstreams at level 6.2 (8K Ultra-HD at 120 fps).

▲ Figure 1: Block diagram shows proposed HEVC CABAC decoder architecture. It consists of two finite state machines (CTX-FSM and BPS-FSM), FSM selector, context selector (CS), context memory (CM), bitstream parser (BP), arithmetic decoder (AD), and de-binarizer (DB). The architecture is deeply pipelined for high-throughput processing.

▲ Figure 2: Performance of proposed HEVC CABAC decoder design, as measured in average bins/cycle, increases linearly with percentage of bypass bins in bitstreams. Since high bitrate (and high performance demanding) bitstreams usually contain more bypass bins, this result proves that performance of our design improves with bitrate of bitstreams.

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Towards High-Performance Bufferless NoCs with SCEPTER

B. K. Daya, L. S. Peh, A. P. Chandrakasan
Sponsorship: Center for Future Architectures

In the many-core era, the network on-chip (NoC) is playing a larger role in meeting performance, area, and power goals. However, the network, especially the buffers, consumes a significant portion of the total power consumption: The MIT SCORPIO NoC connects 36 tiles and expends 18% of the tile power; the Intel TeraFLOPS chip network connects 80 tiles and expends 30% of the total power. Proposals have advocated bufferless NoCs to reduce the NoC power consumption; however, a performance wall has been reached so that high throughput performance has not been extracted.

We present SCEPTER (Single-Cycle Express Path Traversal for Efficient Routing), an NoC architecture that pushes towards high-performance bufferless NoCs. We lower the average network latency of bufferless NoCs by leveraging single-cycle multihop traversals across the network. Thus, even if the flit is sent in a non-preferred direction, a single-cycle path can be potentially traversed, bringing the flit closer to its destination even along non-minimal routes. SCEPTER intelligently prioritizes between flits in the router pipeline, bypassing from faraway, and waiting in the network interface to be injected. It adaptively routes flits in a livelock-free manner while maximizing opportunities to zoom along virtual express paths by opportunistically bypassing. Figure 1 displays an example where a multihop bypass path is preset by Flit A, with the use of switch setup requests (SSRs). Since Flit A is deflected along another direction at node 10, Flit B can either follow the preset bypass path or not. Figure 2 shows the router pipeline and bypass path. When Flit B arrives, a check is performed on whether Flit B's destination quadrant ID (QID) matches that of the preset bypass path. In this example, it matches and Flit B is able to traverse the path in one cycle to reach node 4.

For a 64-node network, we demonstrate an average 62% reduction in latency and an average 1.3x higher throughput over a baseline bufferless NoC for synthetic traffic patterns, with comparable performance to a single-cycle multihop buffered mesh network with 6 flit buffers, per input port, in each router. Early post-synthesis results in IBM 32-nm SOI technology show an average 31% lower area and 33% lower power than optimized buffered router baselines.

▲ Figure 1: The SCEPTER single-cycle multihop traversals allow multiple hops to be traversed by presetting the crossbar switched. At time T0, Flit A's SSR is sent along a path to the destination node. At time T2, at node 10, Flit A and Flit B contend for output port East. Flit B wins; at time T4 it arrives at node 11 and traverses the preset path to node 4.

▲ Figure 2: The SCEPTER router uses the latches between the pipeline stages to hold the flit's information, as no buffers exist. Thus, even if a flit cannot be routed to its desired output port, it must be deflected along another direction/output port. When a flit arrives, a simple check is performed to see if the bypass path is enabled for this cycle. Subsequently, a check determines whether this flit's destination quadrant ID matches that of the SSR that preset the bypass path. If it matches, the flit skips the first two pipeline stages and traverses the crossbar and link.

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Energy-Efficient SRAM using Data-Dependency

C. Duan, A. P. Chandrakasan
Sponsorship: DARPA, National Science Foundation

Embedded static random access memories (SRAMs) are critical components in the design of modern system-on-chips (SoCs). As the capabilities of many digital electronic devices continue to improve, the need for both large and low-power on-chip storage grows in parallel. In IC implementations for various applications, SRAMs occupy a disproportionate amount of total die area and total power consumption. Despite recent progress enabling the low-power operation of digital system blocks at low supply voltages, robust SRAM operation still requires a high operating voltage to guarantee reliability in worst-case scenarios including extreme process, temperature, and/or voltage conditions. Consequently, SRAM has recently become the current bottleneck for further power reduction in many systems and thus necessitates creative energy- and area-efficient solutions. To develop novel approaches to SRAM energy savings, application-specific data features are to be explored in harmony with state-of-the-art techniques such as voltage scaling. Highly correlated data, introduced intuitively as data with repeated or similar values, has been shown via proof of concept to help memory make predictions, reduce bit-line switching, and ultimately save energy wasted on reading redundant and/or predictable information. Existing data-dependent designs, however, are limited by their narrow applicability as well as significant overhead in area and/or latency. In this work, we propose to address said limitations by first examining inherent data-accessing features of several targeted applications. New bit-cell and architectural-level techniques will be investigated to support low-power SRAM operation. The remaining work focuses on the circuit-level implementation of these developments and the construction of a test chip in 28 nm FD-SOI process.

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Energy-Efficient SRAM Design in 28-nm FDSOI Technology

A. Biswas, A. P. Chandrakasan
Sponsorship: STMicroelectronics, DARPA

As CMOS scaling continues to the sub-32 nanometer regime, the effects of device variations become more prominent. This is very critical in static random access memories (SRAMs), which use very small transistor dimensions to achieve high memory density. The conventional six-transistor (6T)-based SRAM bit-cell, which provides the smallest cell-area, fails to operate at lower supply voltages (Vdd). This failure is due to the significant degradation of functional margins as the supply voltage is scaled down. However, Vdd scaling is crucial in reducing the energy consumption of SRAMs, which is a significant portion of the overall energy consumption in modern micro-processors. Energy saving in SRAM is particularly important for battery-operated applications, which run from a very constrained power-budget.

This work focuses on energy-efficient 6T SRAM design in a 28-nm Fully Depleted Silicon-On-Insulator (FDSOI) technology. Significant savings in energy per access of the SRAM can be achieved by Vdd scaling. Different read and write assist techniques are evaluated to improve the minimum SRAM operating voltage (Vdd,min). The different techniques are compared based on various metrics, e.g., energy-overhead, area-overhead, etc. Techniques are proposed to reduce the energy-overhead of different assist methods.

It has been recently shown that correlation in data can be exploited to reduce energy consumption of SRAMs. Applications such as motion estimation in video processing access the same data for multiple read cycles before writing a new data. Sinangil et al. proposed a 10T bit-cell that used data prediction to reduce bit-line switching energy. However, it incurs a significant area overhead due to 10 transistors required to implement the bit-cell. In this work we investigate techniques to incorporate data-prediction in 6T-based SRAM design to benefit from higher density while still saving energy.

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New AC-DC Power Factor Correction Architecture Suitable for High Frequency Operation

S. Lim, D.M. Otten, D. J. Perreault
Sponsorship: ARPA-E, Texas Instruments

We present a novel ac-dc power factor correction (PFC) power conversion architecture for a single-phase grid interface. The proposed architecture has significant advantages for achieving high efficiency, good power factor, and converter miniaturization, especially in low-to-medium power applications. The architecture enables twice-line frequency energy to be buffered at high voltage with a large voltage swing, enabling reduction in the energy buffer capacitor size, and elimination of electrolytic capacitors. While this architecture can be beneficial with a variety of converter topologies, it is especially suited for system miniaturization by enabling designs that operate at high frequency (HF, 3 – 30 MHz). Moreover, we introduce circuit implementations that provide efficient operation in this range. The proposed approach is demonstrated for an LED driver converter operating at a (variable) HF switching frequency (3 – 10 MHz) from 120 Vac, and supplying a 35 Vdc output at up to 30 W. The prototype converter achieves high efficiency (92 %) and power factor (0.89) and maintains good performance over a wide load range. Owing to architecture and HF operation, the prototype achieves a high "box" power density of 50W/ in3 ("displacement" power density of 130W/ in3), with miniaturized inductors, ceramic energy buffer capacitors, and a small-volume EMI filter.
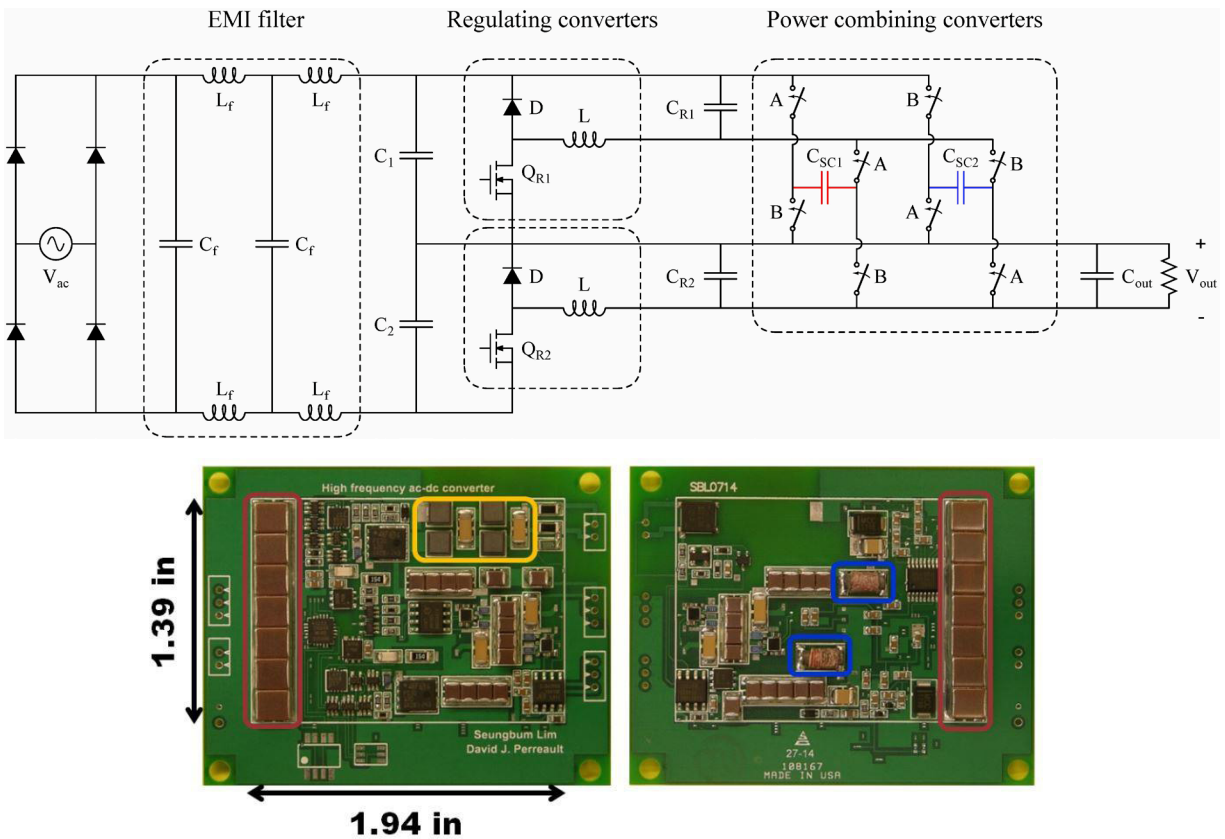
▲ Figure 1: The prototype converter, implemented on a 1.94 in(x), 1.39 in(y), 0.22 in(z) printed circuit board. This figure shows the front and back side of the PCB.

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A High-Power-Density Wide-Input-Voltage-Range Isolated DC-DC Converter with a Multi-Track Architecture

M. Chen, K. K. Afridi, S. Chakraborty, D. J. Perreault
Sponsorship: Texas Instruments, CICS

This project investigates a multi-track power conversion architecture that splits charge into multiple voltage domains and delivers power through multiple tracks, as illustrated in Figure 1. The multi-track architecture reduces the voltage ratings on devices, reduces the voltage regulation stress of the system, improves the component utilization, and reduces the sizes of passive components. The architecture also leverages the complementary strengths of switched-inductor, switched capacitor, and magnetic isolation circuits and gains mutual benefits from the way they are merged. This architecture is suitable to applications that require both isolation and wide-input-voltage range. Compared to a conventional two-stage design, its regulation stage and isolation stage are merged, leading to a hybrid-switched capacitor- magnetics structure that reduces the energy that is "reprocessed" by the two-stages. An 18V-80Vin, 5Vout, 15A, 800 kHz, isolated dc-dc converter has been built and tested to verify the effectiveness of this architecture. It has a power density of 453 W/inch³ and a peak efficiency of 91.3%. This power density is 3x higher than the power density of the state-of-the-art commercial converters. A picture of the prototype converter is shown in Figure 2.

The proposed multi-track power conversion architecture is one embodiment of a group of generalized distributed power conversion techniques. Comparison of the multi-track power conversion architecture with conventional centralized power conversion architecture can demonstrate and theoretically quantify the advantages of distributed power conversion.
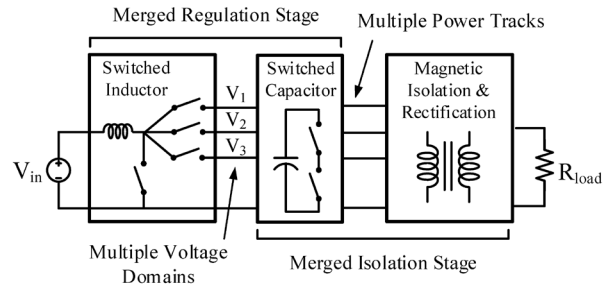
▲ Figure 1: The proposed multi-track power conversion architecture comprising multiple voltage domains and multiple power tracks. Its regulation and isolation stage are merged to reduce the energy that is "re-processed" by the two-stages.
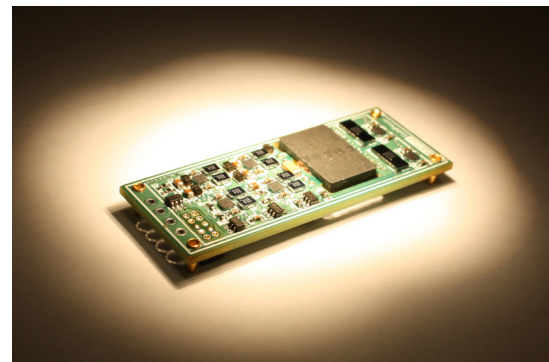
▲ Figure 2: A picture of the high-power-density wide-input-voltage-range isolated multi-track converter.

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A Systematic Approach to Modeling Impedances and Current Distribution in Planar Magnetics

M. Chen, S. A. Pavlick, M. Araghchini, K. K. Afridi, J. H. Lang, C. R. Sullivan, D. J. Perreault
Sponsorship: Texas Instruments, CICS

Planar magnetic components using printed-circuit board (PCB) windings are attractive due to their high repeatability, good thermal performance and usefulness for realizing intricate winding patterns. An example planar magnetic structure is shown in Figure 1. To enable higher system integration at high switching frequency, more sophisticated methods that can rapidly and accurately model planar magnetics are needed. This project develops a systematic approach to modeling impedances and current distribution in planar magnetics based on a lumped circuit model named the *Modular Layer Model* (MLM). Stacked PCB layers are modeled as repeating modular impedance networks, with additional modular impedances representing the magnetic core, air gaps and vias. The model captures skin and proximity effects and enables accurate predictions of impedances, losses, stored reactive energy, and current sharing among windings. The MLM can be used to simulate circuits incorporating planar magnetics, to visualize the electromagnetic fields, and to extract parameters for magnetic models by simulations, among many other applications. The modeling results are checked with results of previous theories and finite-element-modeling approaches, with good matching presented. A group of planar magnetic devices, including transformers and inductors with various winding patterns, are prototyped and measured to validate the proposed approach and clarify the boundaries of its applicability.

A software that can generate SPICE netlists based on planar magnetics geometry information has been developed and is accessible by emailing the authors. The user interface of the current version of the software is shown in Figure 2.
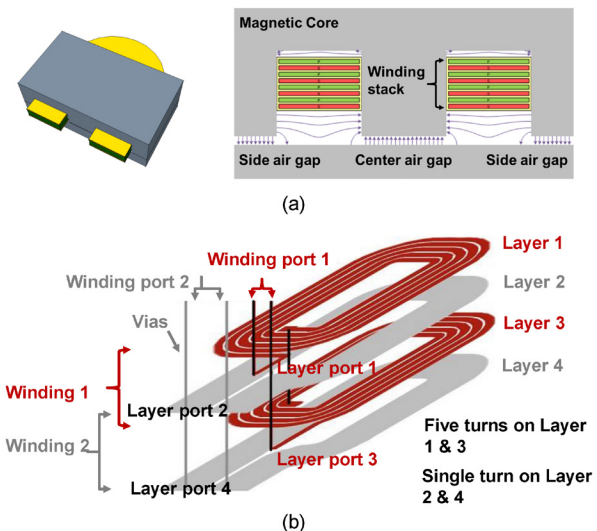
▲ Figure 1: (a) Cross-sectional view of a planar magnetic structure. It comprises a magnetic core, a winding stack, and a set of possible air gaps. (b) Winding stack of an example two-winding, four-layer transformer with 10:1 turns ratio.
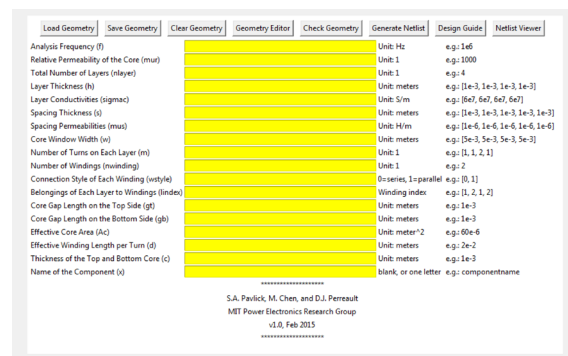
▲ Figure 2: A magnetic geometry to SPICE netlists conversion tool – M2Spice.

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Investigating Magnetic Materials for Power Conversion at High Frequency

A. J. Hanson, J. Belk, C. R. Sullivan, D. J. Perreault
Sponsorship: Lockheed Martin

Magnetic components (inductors and transformers) are typically the largest and most lossy components in power converters. While increasing converter switching frequencies can reduce the required size of passive components, size reductions achievable through frequency increases are often limited by magnetic material constraints for components where core loss is a major consideration, such as in transformers and resonant inductors. Nevertheless, recent research has made significant advances in miniaturized power electronics operating in the high (HF) and very high frequency (VHF) ranges (3-300 MHz), well above typical modern designs operating from hundreds of kilohertz to a few megahertz.

While such advances have been substantial, the design of power magnetics is still not fully understood or optimized, especially in the HF range (3-30 MHz) where use of low-permeability RF magnetic materials can play a valuable role. In part, this lack of understanding owes to a lack of data regarding HF magnetic materials. Magnetic materials are typically characterized for power loss; however, such data are simply not available for most magnetic materials above a few megahertz, hindering the design of magnetics at these frequencies.

Additionally, the modeling and evaluation methods for magnetic components must be adapted in the HF range.

Great efforts have been made to model magnetic core loss and winding loss, but holistic design and evaluation remain incomplete. For example, the commonly used Performance Factor (a FOM for magnetic materials) assumes that, in a magnetic component to be designed, winding loss is not a function of frequency, which often is not true in the HF range.

Our research is extending both the empirical data and the evaluation methods necessary for magnetics design in power converters operating above a few MHz. Using HF measurement techniques (Figure 1), we have gathered large-signal core loss data for a variety of commercially available materials; these data show room for significant improvements in power conversion by moving to the HF range. We have also developed an extension to the popular Performance Factor to include HF effects (Figure 2), allowing material comparison even at frequencies where the traditional Performance Factor is inapplicable. Our results suggest that significant improvements in performance are possible through operation at HF using commercially available magnetic materials. Performance Factor and Modified Performance Factor facilitate understanding of the implications of these data for selecting an operating frequency and understanding its benefits.
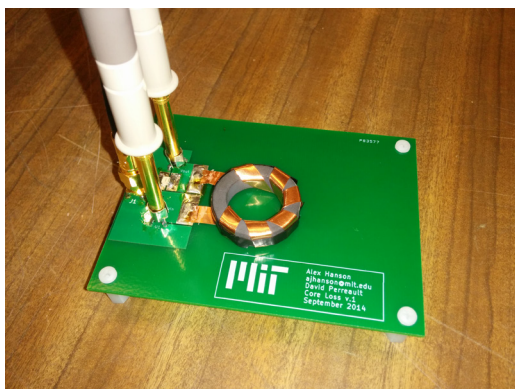
▲ Figure 1: Test setup with a representative magnetic core-under-test (CUT). Core loss measurements at HF require advanced techniques compared to similar characterization in the typical ~100 kHz range.
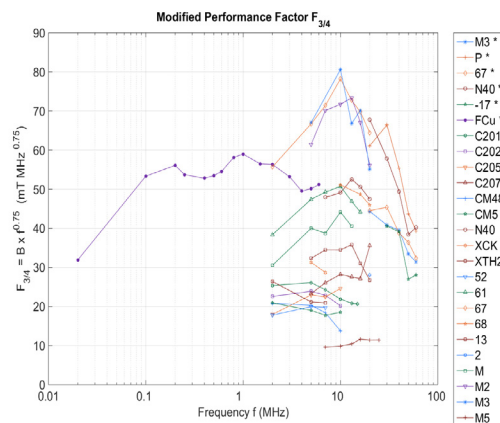
▲ Figure 2: Plot of Modified Performance Factor for materials characterized in this investigation, compared with materials designed for lower frequencies. The theoretical modification correctly accounts for HF effects on loss.

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Energy-Efficient Wireless Power Transmitters and Receivers

N. Desai, T. Yeh, T. Palacios, A. P. Chandrakasan
Sponsorship: Foxconn, MIT/MTL GaN Energy Initiative

The ability to transfer power wirelessly to a device greatly enhances the convenience of using portable electronics in daily life. Even though far-field radiative transfer of power remains an elusive goal owing to regulatory and/or safety concerns, near-field wireless charging using coupled inductor coils has been receiving a lot of attention over the past few years. However, these systems still need to address issues such as standardization and energy efficiency to be deployed on a wide variety of commercial devices.

Losses in coupled-inductor systems arise primarily due to highly imperfect ($k < 0.1$) coupling between the transmitter and receiver coils and small magnetizing inductance of the air core, which results in a lot of reactive energy sloshing back and forth. Compensating the reactances of the coils using a resonant network can address this problem. However, to keep component sizes reasonably small, this technique implies operation in the several MHz-range, which leads to higher transistor switching losses. To address this issue, we designed a soft-switched (Class E), resonant transmitter that uses a GaN switch to reduce switching losses on the input of the switch (Figure 1). Results showed a 5% improvement in efficiency just by using a GaN switch over a silicon switch for similar (~ 10 W) transmit power levels.

Another interesting area of research concerns wirelessly charging wearable electronics. As the functionality of these devices grows, they will need multiple bursts of energy over the course of a day from an energy-constrained source such as a cellphone or tablet. This makes maximizing the end-to-end system efficiency very important. The efficiency is a strong function of the load impedance, coupling and other circuit parameters. The load impedance presented by a battery varies across its charging cycle, while the coupling coefficient is a dynamic parameter in a scenario where the user holds the cellphone over the fitness tracker to charge it. We are designing integrated circuits on the receiver side to track these changing conditions and adapt accordingly to maintain maximum efficiency operation.
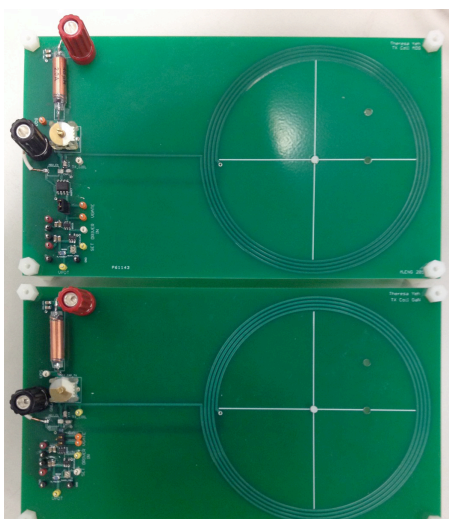
▲ Figure 1: Design of a zero-voltage switched (ZVS) wireless power transmitter with Si FET (top) and GaN FET (bottom). Due to lower input switching losses with the GaN switch, the transmitter on the bottom reduces losses by 5%.

▲ Figure 2: Using a cellphone to provide a burst of energy to a wearable device such as a fitness tracker can typically charge it within a few minutes.

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Picowatt Timer for Energy-Constrained, Battery-Less Systems

P. M. Nadeau, A. Paidimarri, A. P. Chandrakasan
Sponsorship: Texas Instruments, TSMC University Shuttle Program, NSERC

Energy harvesting presents an attractive option for powering wireless Internet-of-things devices; however, the most ubiquitous of sources, such as indoor lighting, ambient RF, system vibration, or body heat, all garner an extremely limited amount of average power. With a recent demonstration of harvesting as low as 1 nW of average power, there is a need to design always-on circuits, such as the wake-up timer, to take advantage of these weak sources.

This abstract presents the design of wake-up timer that consumes 4.2 pW of power for 18 Hz of oscillation (0.23 pJ/cycle). The design features a dynamic 3-stage architecture, duty-cycled current-source, and low operating voltage (0.6 V) enabled by a voltage boost circuit. The circuit details are shown in Figure 1. M1 precharges C1 to V_{dd}, and M6 precharges C2 to ground. Then, at the beginning of a timing cycle, I_{bias} linearly discharges C1 until M5 begins charging C2 and turns on M3. The positive feedback generated by M5 and M3 quickly flips the cell, generating a sharp edge to subsequent logic, such as inverter I1. A three-stage design provides all of the control signals necessary to precharge and trigger the timing of each stage in sequence.

Since I_{bias} should ideally remain stable across voltage and temperature, it is generated by a current source referenced to an on-chip resistor, which is then duty-cycled to save power. At the beginning of operation, M7 is enabled by a boosted voltage for a short period of time so that the current reference can set I_{bias} to the desired level. Then, M7 is disabled, and I_{bias} is fixed by the analog voltage stored on C3. A refresh of the voltage on C3 is performed periodically to compensate for the leakage current through M7, which serves to discharge this voltage over time.

Measurements of the system are shown in Figure 2. The design has scalable performance across 2 orders of magnitude in frequency and power by adjusting the I_{bias} current. Performance versus V_{dd} is also assessed, and the power consumption follows near square-law (e.g., proportional to CV^2f) dependence up to 1.8V, owing to the benefit of the positive regeneration in eliminating short-circuit currents. The figure also shows the performance of the track-and-hold scheme. Refreshing the I_{bias} current every 400 s leads to an average power consumption of 2.2 pW for the reference circuit (overall 4.2 pW for the system) and a ±2% variation in the generated frequency.

▲ Figure 1: Circuit diagram of the timer system showing the current reference and interconnection of the stages (top), and detailed circuit for one stage (bottom).
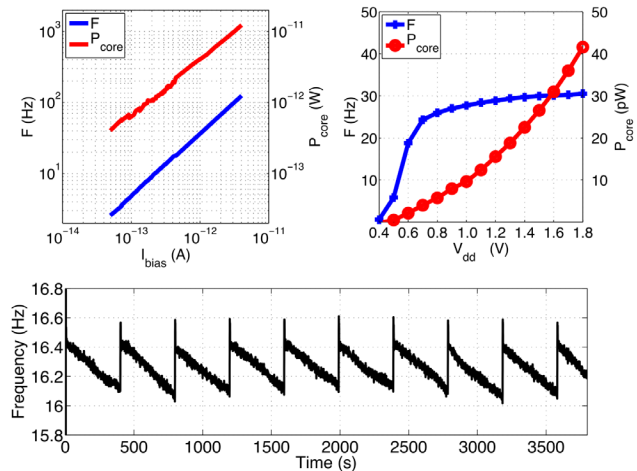
▲ Figure 2: Measurements of timer system including performance vs. I_{bias} (top-left), vs. supply voltage (top-right), and performance when integrated with the track-and-hold scheme (bottom).

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Solar Energy Harvesting System with Integrated Battery Management and Startup using Single-Inductor and 3.2 nW Quiescent Power

D. El-Damak, A. P. Chandrakasan
Sponsorship: TSMC University Shuttle Program, Texas Instruments Fellowship for Women in Microelectronics

Energy harvesting systems have allowed the autonomous operation of ultra-low power devices for implantable and wearable applications. Since the power sources available in our surroundings are intermittent, extreme energy-efficiency of the power management circuits is required. Thus, this work presents an energy harvesting system with 3.2 nW of quiescent power for solar-based applications. Figure 1 shows the chip's top-level architecture. The IC integrates the converter switch matrix with the associated configuration logic and drivers, voltage reference, current reference, startup, regulation, and battery management circuits. It can supply a 1V regulated voltage rail, V_{LOAD}, and charge a battery, V_{BAT} using a single 47μH inductor. The switch matrix supports three main configurations in addition to the startup: (a) Boost1: from the solar harvester V_{IN} to V_{LOAD}, (b) Boost2: from V_{IN} to V_{BAT}, and (c) Buck: from V_{BAT} to V_{LOAD}, which is used when the power available from the solar cell is insufficient to keep the 1V output regulated. The control circuit is designed in an asynchronous fashion that scales the effective switching frequency of the converter with the level of the power transferred. The on-time of the converter switches adapts dynamically to the input and output voltages for peak-current control and zero-current switching. The chip operates efficiently with input power that ranges from 10 nW to 1 μW. Figure 2 shows the micrograph of the fabricated chip with an active area of 2.2x1.1 mm². For input power of 500 nW, the proposed system achieves an efficiency of 82%, including the control circuit overhead, while charging a battery at 3 V from 0.5 V input. In buck mode, it achieves a peak efficiency of 87% and maintains efficiency greater than 80% for output power of 50 nW-1μW with input voltage of 3 V and output voltage of 1 V.
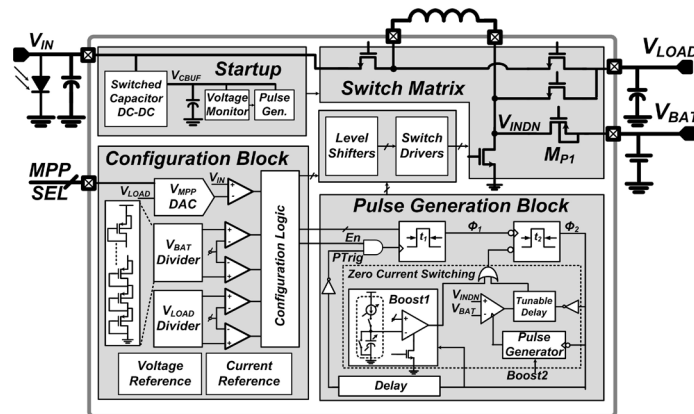
▲ Figure 1: Top level architecture of the system.
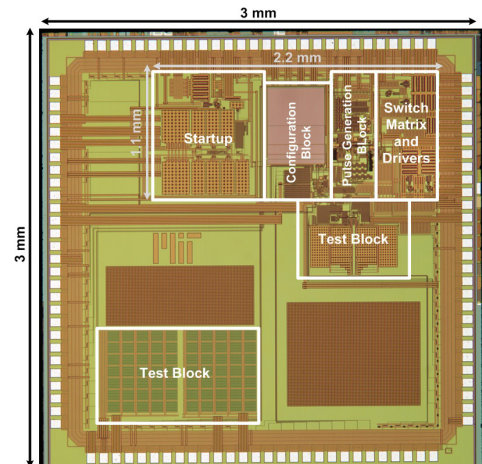
▲ Figure 2: Chip micrograph.

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Authentication Tags for Supply Chain Integrity

C. Juvekar, H.-M. Lee, A. P. Chandrakasan, J. Kwong (Texas Instruments)
Sponsorship: Texas Instruments, Denso

Counterfeiting is a major problem in commodity markets. A global supply chain exacerbates this problem by making it even harder to maintain the integrity of the components due to the sheer diversity of suppliers. In fact, most counterfeit components make it into the supply chain despite the best effort of the suppliers simply because the suppliers lack the capability to detect them. DARPA has proposed the Supply Chain Hardware Integrity for Electronics Defense (SHIELD) program to address these concerns.

In this project, we implement the concept of electronic fingerprinting to a wide range of components (Figure 1). To achieve this goal we are building integrated tags that act as cryptographically unique identifiers for both electronic and mechanical components. Our tags satisfy the goals of low cost and secure operation through a combination of protocol, circuits, and technology innovation.

We leverage unique technology features provided by our fabrication partner (Texas Instruments) to build authentication circuits that can operate reliably in the presence of intermittent powering. A dynamic on-chip key memory ensures added protection against conventional side-channel as well as more advanced semi-invasive imaging attacks. To preserve the small form factor and facilitate stand-alone operation, we have integrated wireless power and telemetry circuits with on-chip passives. This enables low-cost system integration on account of zero off-chip components. Finally we have developed a custom cryptographic challenge-response protocol that allows the server to securely authenticate the tag and maintain seamless synchronization with our key storage.

We envision that the tag will be used in conjunction with a server that maintains a database of valid issued tags. To validate the authenticity of purchased components, a user would scan the affixed tag using a handheld scanner and run a challenge response protocol to match cryptographic information stored on the tags with the server database (Figure 2).
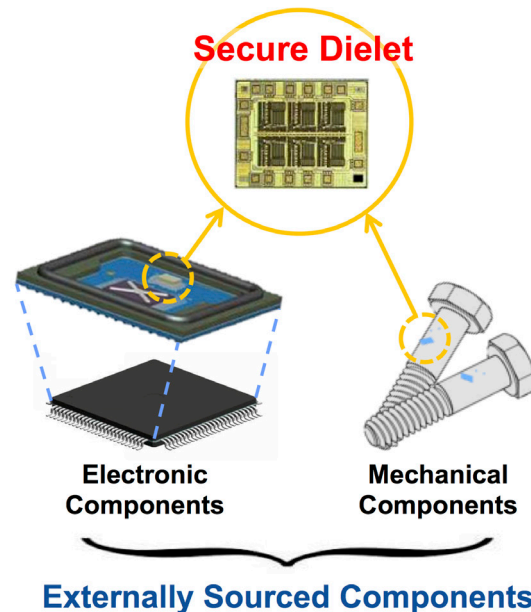
▲ Figure 1: Common stand-alone authentication tags that can be attached to various electronic and mechanical components
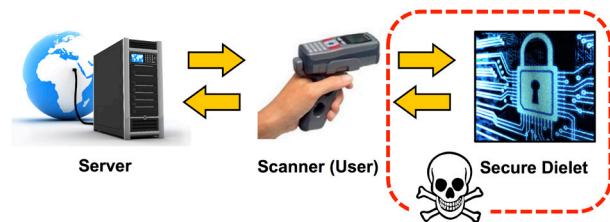
▲ Figure 2: Illustration of a complete authentication system that includes the tag, handheld scanner, and server database. Our tags protect against physical and side-channel attacks on the tag.

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Low-Power Sensor Interfaces for Wireless Sensor Nodes

F. M. Yaul, A. P. Chandrakasan
Sponsorship: Shell, Texas Instruments

Sensor interface circuits found in wireless sensor nodes (WSNs) typically comprise a low-noise amplifier (LNA), analog signal conditioning circuits, an analog-to-digital converter (ADC), and a digital signal processor (DSP) to extract information from the signals. These blocks are shown in Figure 1. Reducing system power consumption allows for increased sensor node lifetime, which is especially important for nodes that are difficult to physically access. Examples include medical implants and pipeline monitoring nodes.

One component of this project has been an ADC which takes advantage of low signal activity in order to save power. Since low signal activity is common to many sensor signals, the ADC can save power in a broad range of applications. This work introduces an altered successive approximation (SA) algorithm called LSB-First SA, which is designed to reduce the number of bitcycles per conversion, given a good initial guess of the value of the sample. Figure 2 depicts the ADC's response to an ECG input signal and demonstrates the ADC's ability to save power and perform 10-bit conversions in just 3.7 bitcycles/sample on average when the signal is only varying by 1.2 LSBs/sample on average.

Current work on this project involves exploring power reduction techniques in the LNA and DSP blocks, as well as investigating ways to exploit structure in the signal information to save power in the overall system.
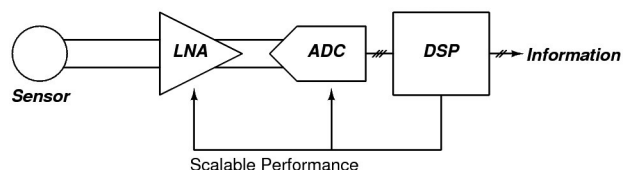
▲ Figure 1: Block diagram of signal-to-information chain. Based on the structure of the information, the performance of the analog front-end may be scaled to save power.
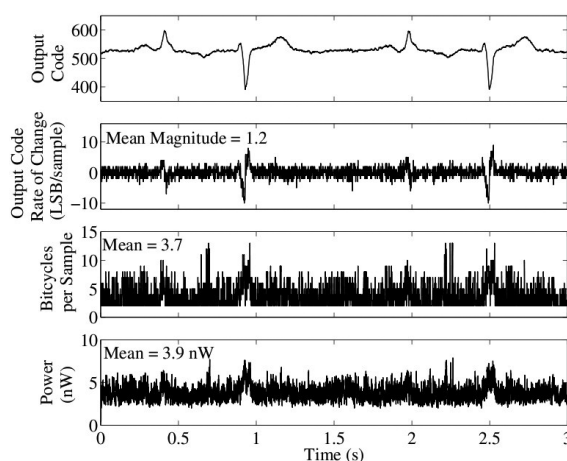
▲ Figure 2: ADC response to ECG test input signal with f_S = 1 kHz and V_{DD} = 0.5 V, demonstrating the ADC's low leakage and data-dependent energy consumption.

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A Graphene-CMOS Hybrid Sensor for Thermal Imaging

S. Ha, A. Hsu, Y. Lin, M. Hempel, C. Mackin, J. Kong, T. Palacios, A. P. Chandrakasan
Sponsorship: Center for Integrated Circuits and Systems, Institute for Soldier Nanotechnologies

CMOS image sensors are widely used in digital multi-media applications thanks to their mature production technology; the performance ramps up every year with denser integration, better noise suppression, adjustable dynamic range, and lower power. However, the band gap of silicon fundamentally limits the absorption spectrum to the visible and near-infrared light (λ < 1100nm). To overcome the physical limitation of a Si photodetector in longer wavelength detection, we employ a tunable ambipolar graphene-based thermocouple. With an integrated graphene-based thermocouple array, the hybrid IR image sensor can detect the long-wavelength infrared spectrum that is used in security cameras and medical thermal imaging and in spectroscopy for chemistry and astronomy. Furthermore, the present sensing platform solves critical issues in manufacture of conventional IR sensors and enables expanded applications such as a high-speed and high-resolution IR imager and a hyperspectral IR imaging IC.

First, a Si CMOS readout chip using commercially available 0.18-um technology was designed. The readout circuit consists of pixel transimpedance amplifiers, row-column multiplexers, and parallel column analog-to-digital converters (ADCs). The layout design of the chip required careful considerations on the post-fabrication process to ease the graphene integration processes, or at least make them possible, including standard ebeam lithography, metalization, etching, and graphene transfer steps. For instance, the pixel amplifier and signal paths occupy only the small portion of each 50-um x 50-um pixel area, leaving over 60% of the area empty and flat to enable fabrication of back gate electrodes for the graphene thermocouple and high-yield graphene transfer. Secondly, the graphene-integrated readout chip was fabricated as shown in Figure 1. Figure 2 shows a closer look at the fabricated on-chip graphene thermocouple pixel. An electrostatically induced graphene p-n junction of graphene generates a thermoelectric voltage in response to IR light absorption. The terminals of the thermocouple are connected to the M6 pillars of the pixel amplifier input; the signal is amplified and converted into 8-bit codes. In the testing setup, an off-chip processor renders the data in 2D image.
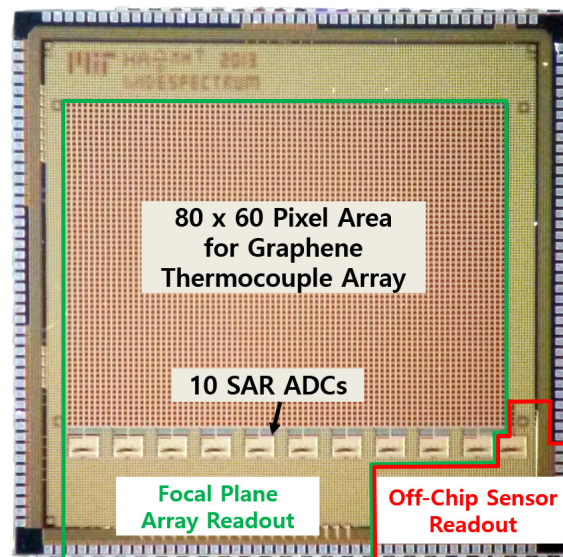
▲ Figure 1: The integrated readout IC for graphene-CMOS hybrid IR imager consists of an array of 80 x 60 graphene thermocouples and pixel amplifiers in the center area and row and column selection logic, current sources, column amplifiers, and ADCs in the periphery to ease the fabrication.
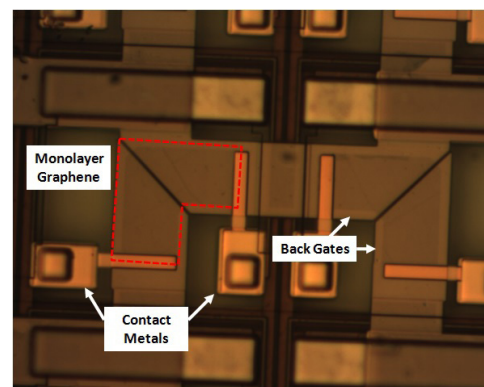
▲ Figure 2: Top view of the pixels with graphene thermocouples connected to the pixel amplifier inputs. The monolayer graphene sheet is biased by two metal gates embedded in the dielectric layer.

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Electronic Devices: Transistors; Memory, Magnetic, and Superconducting Devices

Efficient Device and Integrated Circuit Statistical Modeling and Extraction Using a Bayesian Inference Framework

L. Yu, I. Elfadel, D. A. Antoniadis, D. S. Boning
Sponsorship: Masdar Institute/MIT Cooperative Program

Variability modeling and extraction in advanced integrated circuit technologies is a key challenge to ensure robust circuit performance as well as high manufacturing yield. We have developed an efficient framework for device and circuit variability modeling and extraction by combining ultra-compact transistor and timing models with Bayesian extraction methods. The compact models used here include the MIT virtual source (MVS) MOSFET model and a recent analytical model for gate timing characterization. Based on statistical extensions of these models, we propose algorithms for three applications that greatly reduce the time and cost required for measurement of on-chip test structures and characterization of library cells.

A critical problem in design for manufacturability (DFM) is to build statistically valid prediction models of circuit performance based on a small number of measurements taken from a mixture of on-chip test structures. Towards this goal, we have developed a technique named physical subspace projection to transfer a mixture of measurements into a unique probability space spanned by the MVS parameters. We search over MVS model parameter combinations to find those with the maximum probability by extending the expectation-maximization (EM) algorithm and iteratively solve the resulting maximum a posteriori (MAP) estimation problem. Finally, we develop a process shift calibration technique to estimate circuit performance by combining SPICE simulation and very few new measurements.

We further develop the parameter extraction algorithm to enable us to accurately extract all current-voltage (I-V) parameters given limited and incomplete I-V measurements, applicable to early technology evaluation and statistical parameter extraction. An important step in this method is the use of MAP estimation, where past measurements of transistors from various technologies are used to learn the *a priori* distribution and its uncertainty matrix for the parameters of the target technology. We then utilize Bayesian inference to facilitate extraction of *a posteriori* estimates for the target technologies using only a very small set of additional measurements. The proposed extraction approach can also be used to characterize the statistical variations of MOSFETs, with the significant benefit that some constraints required by the backward propagation of variance (BPV) method are relaxed. We study the lower bound requirement for number of transistor measurements to extract the full set parameters from a compact model, and propose an efficient algorithm for selecting the optimal measurement biases by minimizing the average output measurement uncertainty (Figure 1).

Finally, we have developed a flow to enable computationally efficient statistical characterization of delay and slew in standard cell libraries. We utilize a novel ultra-compact, analytical model for gate timing characterization. Instead of exploiting the sparsity of the regression coefficients of the process space with a reduced process sample size, we exploit correlations between different input vectors using a Bayesian learning algorithm, enabling us to estimate the parameters of the aforementioned timing model using past library characterizations along with a very small set of additional simulations.
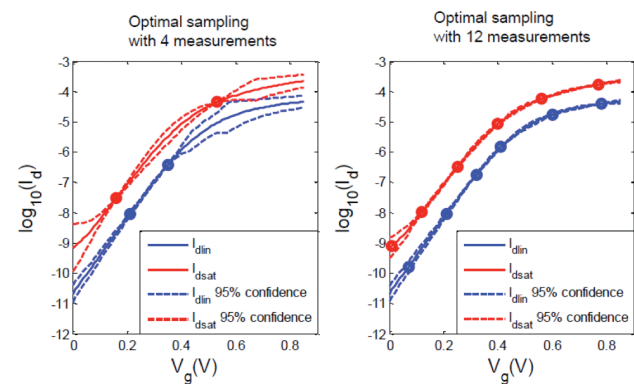
▲ Figure 1: Confidence intervals on Idlin and Idsat estimates for transistor compact model fitting, as a function of optimally selected measurement voltage bias points.
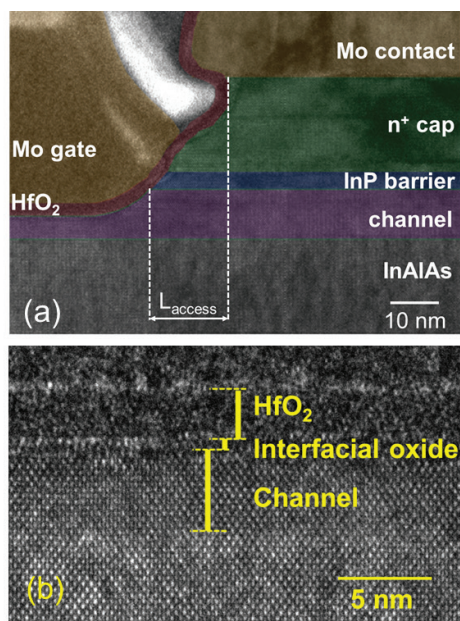
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Impact of Intrinsic Channel Scaling on InGaAs Quantum-Well MOSFETs

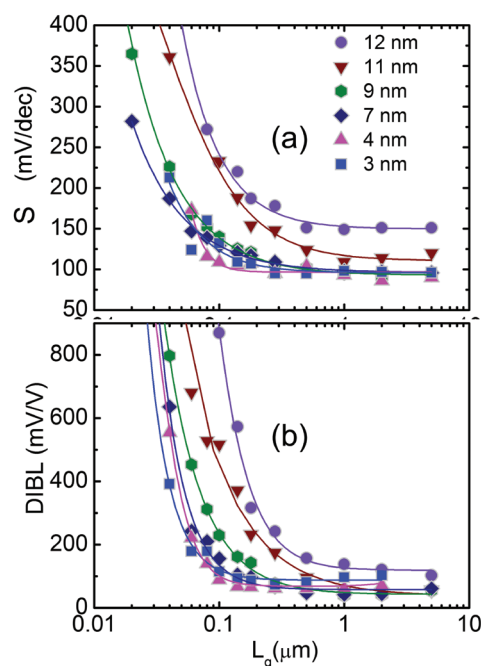J. Lin, D. A. Antoniadis, J. A. del Alamo
Sponsorship: Defense Threat Reduction Agency, E3S STC, Singapore-MIT Alliance, SMART

InGaAs is a promising candidate as an n-type channel material for future CMOS due to its superior electron transport properties. We have developed a novel self-aligned recessed-gate fabrication process for scaled InGaAs quantum-well MOSFETs (QW-MOSFETs). The fabrication sequence yields precise control of all critical transistor dimensions. Figure 1 (a) shows a cross-sectional transmission electron microscopy (TEM) image of the transition region between the intrinsic channel on the left and the extrinsic region on the right in a finished device. The contact is very close to the gate with an access region length (L_{access}) of 15 nm. Figure 1 (b) shows that a uniform channel and a flat surface are obtained in the intrinsic portion of the device. The channel is 7 atomic monolayers thick, which agrees with our targeted channel thickness for this device of 4 nm and showcases the excellent control accuracy of our process.

Our precise fabrication technology has allowed us to carry out a detailed scaling study of these devices. It is found that a thick channel is beneficial for ON-state figures of merit including transconductance and ON resistance. However, a thin channel is beneficial for OFF-state metrics such as subthreshold swing (S) and drain-induced barrier lowering (DIBL). S and DIBL in Figure 2 follow classic scaling behavior: they are both independent of gate length (L_g) for long L_g but degrade rapidly as L_g scales down beyond a certain value. The onset of S and DIBL degradation occurs at longer gate lengths for devices with thicker t_c. The InGaAs QW-MOSFET shown here is at the limit of scaling around L_g=50 nm, which indicates the need for appropriate transistor redesign and advanced 3D device architectures to deliver further progress.

▲ Figure 1: (a) TEM cross-section of a finished InGaAs QW-MOSFET around the edge of the gate. The access region (L_{access}) is indicated. (b) High-resolution TEM (HRTEM) cross-section of the intrinsic region.

▲ Figure 2: Experimental S and DIBL as a function of gate length (L_g) for channel thickness t_c =3 nm to 12 nm.

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# Electrical Reliability of InGaAs MOSFETs

X. Cai, J. Lin, J. A. del Alamo

InGaAs is a promising n-channel material candidate for future complementary metal–oxide–semiconductor (CMOS) technology due to its superior electron transport properties and low voltage operation. While the process technology and performance of InGaAs metal–oxide–semiconductor field-effect transistors (MOSFETs) continue to improve, there is increasing research interest in developing fundamental understanding behind the electrical reliability of this device technology. Several recent studies have observed threshold voltage shifts and transconductance changes under various voltage stress conditions. Understanding, modeling, and mitigating these effects is of great relevance.

To understand the impact of voltage stress on InGaAs MOSFETs and its physical origin, we have developed an automated stress-characterization measurement scheme. A constant bias is applied to the device and periodically interrupted for I-V characterization. This allows us to study the evolution of device behavior during stress. After reaching the total stress time, the voltage stress is removed and I-V measurements are taken periodically to study the device recovery. A thermal step is used to restore the device to its initial condition before applying a different stress condition.

The InGaAs quantum-well MOSFETs used in this study are fabricated by a self-aligned gate-last process. The gate insulator is 2.5-nm HfO_2, deposited by atomic layer deposition (ALD) at 250°C. Figure 1 shows the cross section schematic of a typical device. Figure 2 shows the evolution of subthreshold and transfer characteristics of a device during stress at V_{gs}=1 V and V_{ds}=0 V at room temperature. As stress time increases, the threshold voltage shifts positively and the peak transconductance increases. Contrary to most other studies, where the transconductance is observed to degrade, we have observed a 40% enhancement of the peak transconductance at the end of the two-hour stress period. Understanding the physical mechanism behind this transconductance enhancement will allow us to explore options to stabilize the device and furthermore might provide us with process technology suggestions to improve device performance.
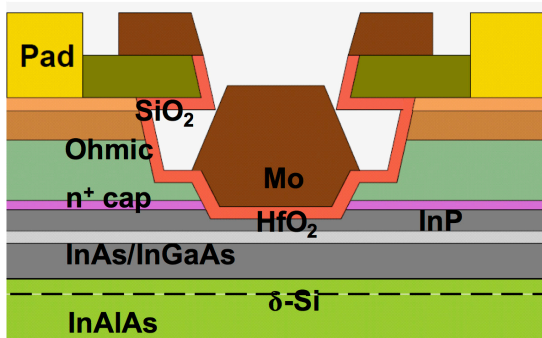
▲ Figure 1: A cross-sectional schematic of the InGaAs MOSFET used in this study.
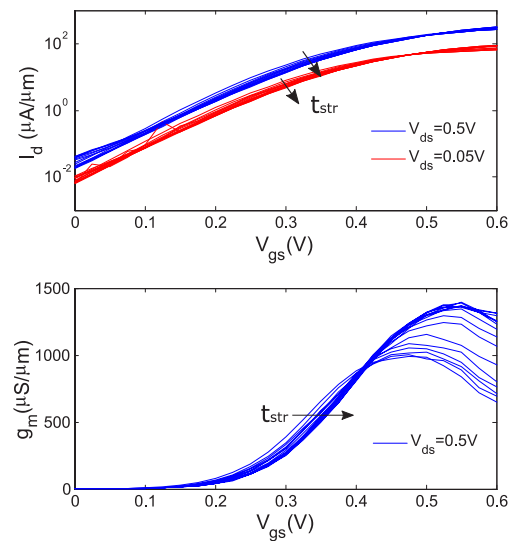
▲ Figure 2: Evolution of subthreshold (top) and transfer characteristics (bottom) during stress at V_{gs}=1 V and V_{ds}=0 V for two hours at room temperature.

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A New Emission-Diffusion Virtual Source Field-Electron-Transmitter Model

S. Rakehja, M. Lundstron (Purdue U.), D. A. Antoniadis
Sponsorship: National Science Foundation NEEDS program

A new physics-based compact model valid from drift-diffusive to ballistic carrier transport regimes was implemented in close collaboration with Professor Lundstrom of Purdue University. This model, called the virtual-source emission-diffusion (VSED) model, is similar to the ED model for Schottky barriers but incorporates the metal-oxide semiconductor electrostatics. The VSED model provides a description of the current at any drain bias without empirical fitting and predicts the injection velocity of carriers (device on-current). The VSED model is fully consistent with the MIT Virtual Source model and is applicable to both long- and short-channel devices using only a few physical parameters such as long-channel mobility and thermal velocity. The accuracy of the VSED model was demonstrated by comparison with measured I-V data of III-V HEMTs and Si extremely thin SOI (ETSOI) devices. The model physics and experimental calibration of the VSED model were presented at IEDM, 2014.

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A Second-Generation Virtual Source Field Electron Transmitter Model

S. Rakehja, M. Lundstron (Purdue U.), D. A. Antoniadis
Sponsorship: National Science Foundation NEEDS program

An improved virtual source (VS) model is developed that builds upon the original MIT Virtual Source (MVS) model but incorporates the effects of (i) carrier degeneracy on thermal velocity and mean free path of carriers, (ii) drain-bias dependence of gate capacitance and virtual-source charge, and (iii) non-linear channel-access resistance on gm-degradation at high drain currents in the channel.

It is well known that both the thermal velocity and the mean free path of carriers increase with an increase in carrier concentration. While the basic MVS model required an artificially lower effective carrier mass, for its presumed constant carrier velocity, in order to match the measured drain currents in InGaAs HEMT devices, the MVS 2.0 model allows for the virtual source injection velocity of carriers to increase with V_{gs}, permitting a higher and more realistic effective mass of carriers. Furthermore, in the basic MVS model, the VS charge is not influenced by non-equilibrium transport conditions in the channel, and essentially the gate capacitance of the device is assumed to be independent of the drain bias. This assumption is too simplistic for quasi-ballistic devices where the negative momenta of the VS charge distribution are primarily supplied by the drain contact in near-equilibrium transport ($V_{ds} \approx 0V$) and are missing in non-equilibrium transport (high V_{ds}). The VS charge model in MVS 2.0 is updated to capture the effect of non-equilibrium transport. The charge model also includes the quantum-mechanical correction to the gate-channel capacitance due to the finite separation of the charge centroid from the semiconductor-insulator interface. Finally, the non-linearity of channel-access resistances that is responsible for the reduction in the transconductance, $gm = \partial I_D / \partial V_g$, of the III-V HEMT devices for high drain currents has been included in MVS 2.0 by modeling the source and the drain channel-access resistances as non-linear voltage-dependent resistances. Even though the basic MVS model has fewer fitting parameters and can fit the experimental data well, it does not capture the essential physics of the nanotransistor in presence of non-equilibrium transport, carrier degeneracy, and access-region non-linearity, and therefore MVS 2.0 is superior in this respect.

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# Nano-Scale Ohmic Contacts for p-InGaSb MOSFETs

W. Lu, J. A. del Alamo
Sponsorship: Samsung

In the last few years, III-V compound semiconductors have emerged as promising channel materials for future scaling of CMOS technology. As high-performance In-GaAs n-MOSFETs have been successfully demonstrated, it is critical to find a p-type counterpart with comparable characteristics. Among all III-V materials, the antimonide system, such as p-InGaSb, is the best candidate because of its outstanding hole mobility and the substantial enhancement in transport characteristics that is made possible by introducing compressive strain. To make p-InGaSb MOSFETs feasible in future technology, many challenges need to be addressed. One of the main limiting issues is the lack of a low-resistance nano-scale ohmic contact technology. This lack severely restricts the performance that can be achieved.

In this project, we are investigating process technologies that will allow us to demonstrate ultralow resistance nano-scale p-type ohmic contacts for sub-10 nm InGaSb MOSFETs. We have designed a novel p^+-InAs/InAsSb bilayer capping structure that addresses the deffectivity issues of conventional InAs caps and significantly improves the contact resistance. We are conducting a systematic study of various ohmic contact schemes and contact formation conditions. To date, we have fabricated Ni/Pt/Au ohmic contacts with a contact resistance as low as 45 $\Omega\cdot\mu m$, corresponding to a record contact resistivity of $1.3\cdot10^{-8}$ $\Omega\cdot cm^2$. Figure 1 shows the resistance data obtained by a circular transmission line model (CTLM) of the Ni contacts. To investigate nano-scale ohmic contacts, we also fabricated Ni nano-transmission line model (nano-TLM) test structures, which allow accurate measurement of ultralow contact resistivity in nano-contacts. Figure 2 shows an SEM image of a typical nano-TLM structure. For the smallest fabricated contact length of 80 nm, an average contact resistivity of $5.2\cdot10^{-8}$ $\Omega\cdot cm^2$ was extracted. In addition, we have fabricated Ni/Ti/Pt/Al ohmic contacts with a contact resistivity of $4.1\cdot10^{-8}$ $\Omega\cdot cm^2$. This is the first demonstration of Si-compatible contacts with ultralow contact resistivity.

We are working toward further improvement of the ohmic contact technology, through innovations such as strained contacts and fin-contacts, and trying to reduce the contact resistivity to the 10^{-9} $\Omega\cdot cm^2$ range. Our future goal is to demonstrate high performance InGaSb p-type MOSFETs and study fundamental transport phenomena in these transistors.
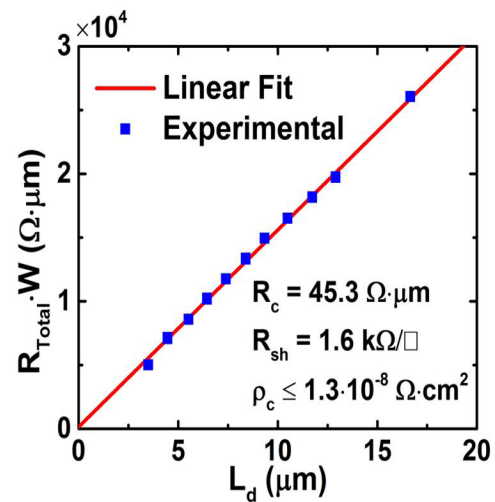
▲ Figure 1: Electrical measurements on a CTLM with Ni/Pt/Au ohmic contacts on a p^+-InAs/InAsSb cap structure after 3 min 350 °C annealing.
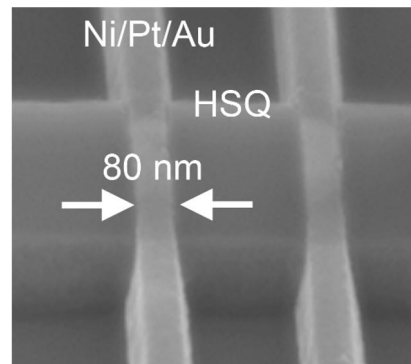
▲ Figure 2: SEM image of a Ni/Pt/Au nano-TLM test structure, with 80-nm contact length, 130-nm contact spacing, and 1-μm width.
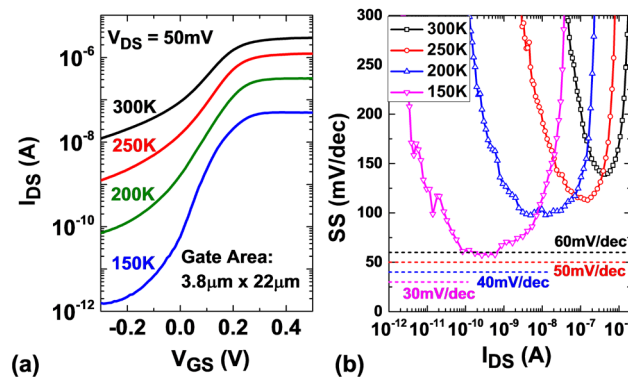
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Effects of Drain-Side Thermal Barriers in InGaAs/GaAsSb Quantum-Well Tunnel-FETs

T. Yu, J. T. Teherani, D. A. Antoniadis, J. L. Hoyt
Sponsorship: National Science Foundation

The recent downscaling of the supply voltage (V_{DD}) becomes limited in the conventional CMOS technology and tunnel-FETs (TFETs) have attracted much attention as potential candidates for future low power applications However, the non-idealities of the devices must be fully understood. In this work, temperature dependent measurement was performed to investigate the operation characteristics of the first InGaAs/GaAsSb quantum-well TFETs (QWTFETs) with tunneling taking place between two quantum-wells. Specifically, the drain-side thermal barrier in the ungated region is limiting the device performance.

Figure 1 shows the transfer characteristics and corresponding subthreshold swing (SS) of a QWTFET with gate dimension of L_g = 3.8µm, W_g = 22µm at V_{DS} = 0.05V at 150 K to 300 K. Significantly improved SS_{min} = 58 mV/decade and SS_{eff} = 80 mV/decade (I_{DS} from 10 pA to 10 nA) at 150 K are observed. One limiting factor in the device SS is the high-k/InGaAs interface traps.

Since the traps in the conduction band, where TFETs are operated, do not freeze out at low temperature, the SS at 150 K is still not close to the thermal limit of 30 mV/decade. The OFF current is another major factor limiting the SS where the leakage current decreases substantially, exhibiting slightly improved SS compared with the thermal limit.

Figure 1 (a) also shows that the ON-current of the device at low drain bias degrades as the temperature decreases, which is caused by the decreased thermionic emission over a parasitic barrier in the current path. The location of the current barrier is at the drain side of the ungated region. TCAD simulation of the conduction band profile along the cutline B-B' in Figure 2 (a) shows that the barrier is present near the drain for small V_{DS} (Figure 2 (b)), which restricts the electron flow. To eliminate this barrier, the lightly doped region must be shortened. The simulation result with L_{GD} = 10 nm is also shown in Figure 2 (b).

▲ Figure 1: (a) I_{DS}-V_{GS} curves of the TFET from 150 to 300 K at low V_{DS}. The OFF-state leakage current is dramatically decreased at 150 K. (b) Subthreshold swing (SS) versus drive current from 150 to 300 K. SS ~ 60 mV/decade over more than one decade of I_{DS}, and SS_{eff} = 80 mV/decade is achieved at 150 K.
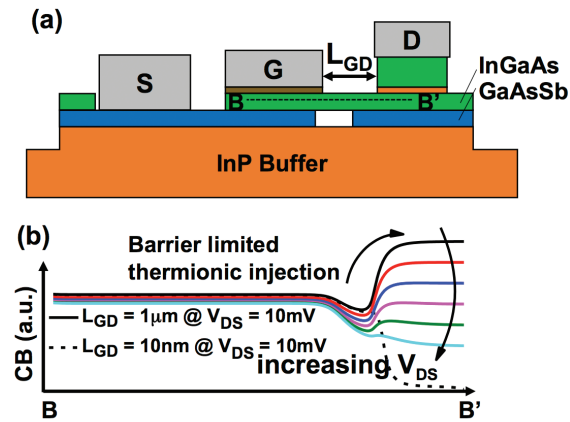
▲ Figure 2: A physical analysis for the InGaAs/GaAsSb vertical TFET in the ON-state. (a) A simplified schematic view; (b) InGaAs conduction band diagram parallel to the gate (B-B') simulated at V_{GS} = 0.5 V with varying V_{DS}.

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Modeling of Parasistic Trap-Assisted Tunneling in Tunnel Field-Effect Transistors

W. Chern*, R. Sajjad*, J. T. Teherani, D. A. Antoniadis, J. L. Hoyt
* Denotes equal contribution
Sponsorship: National Science Foundation Center for Energy Efficienct Electronics Science (E3S)

Tunnel field-effect transistors (TFETs), schematic shown in Figure 1, are currently being investigated because they are theoretically able to switch more steeply with gate voltage than the 60 mV/dec (room T) thermal limit of metal-oxide field effect transistors (MOSFETs), potentially enabling lower power electronics. The improvement of the switching steepness allows for a reduction in the operating voltage, V, and hence a reduction in power consumption as power scales with ~ V^2. Experimentally, TFETs have been challenged by low current drive and/or switching at rates above the thermal limit inferior to theoretical predictions. TFETs are gated diodes that switch from off to on when the gate aligns the conduction band of the channel to the valence band of the source. This work seeks to investigate parasitic leakage paths from traps–namely interface traps--that have prevented TFETs from delivering sub-60 mV/dec. performance. A gate-controlled parasitic current path through interface states is investigated using a modified Shockley-Reed-Hall (SRH) generation model in an effort to quantify the impact of trap-assisted tunneling on TFET switching behavior. The model consists of either an electron being emitted from the valence band to the conduction band through both tunneling and thermal mechanisms with the assistance of a trap state as shown in Figure 2. Different methods of reducing the impact of traps on the switching behavior will be investiaged to move towards the final goal of demonstrating sub-60 mV/dec. switching experimentally.
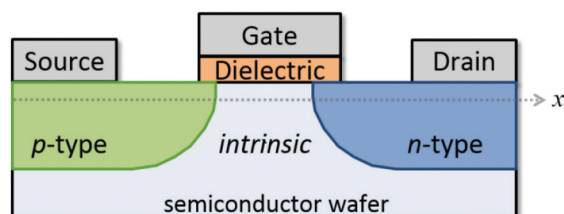
▲ Figure 1: A schematic of a tunnel field-effect transistor (TFET).
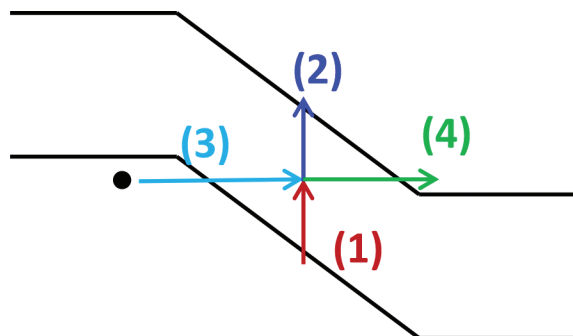
▲ Figure 2: Band diagram illustrating different mechanisms for trap-assisted-tunneling. The mechanisms are (1) electron capture and (2) electron emission from thermal emission and (3) electron capture and (4) electron emission from tunneling.

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InGaAs/InAs Heterojunction Vertical Nanowire Tunnel FETs Fabricated by a Top-Down Approach

X. Zhao, A. A. Vardi, J. A. del Alamo
Sponsorship: National Science Foundation Award #093951 (E3S STC)

In light of the increased emphasis on energy efficiency in electronics, the tunnel field-effect transistor (TFET) has become attractive as a logic transistor due to its potential for low voltage operation. In TFETs, In-GaAs-based heterojunctions promise a combination of steep slope, high ON-current due to the reduced tunnel barrier height, and a well passivated surface. To enable continued scaling, a nanowire (NW) transistor geometry with a wrapped-around gate is highly favorable due to the effective charge control and its robustness to short-channel effects. Here we demonstrate for the first time InGaAs/InAs heterojunction vertical NW TFETs fabricated via a top-down approach, which is more relevant to manufacturing than existing bottom-up techniques.

In our devices, the tunneling junction consists of a p^+-i In$_{0.53}$Ga$_{0.47}$As heterostructure in which a 2 nm i-InAs/8 nm i-In$_{0.7}$Ga$_{0.3}$As "notch" has been inserted to reduce the tunnel barrier height and yield steeper subthreshold

characteristics and high ON current. We leverage process technology used in our previous InGaAs NW MOSFETs with several key changes, including an improved dry etch process. Figure 1 shows the subthreshold characteristics of a single-NW device with 50-nm diameter. A subthreshold swing of 75 mV/dec averaged over I_d from 10^{-9} to 10^{-7} A/µm is obtained at V_{ds}= 0.3 V. The output characteristics in a semilog scale including the reverse regime are shown in the inset of Figure 1. Clear negative differential resistance is observed for V_{ds}<0 and high V_{gs}, confirming the tunneling nature of device operation in the ON regime. Figure 2 benchmarks I_{on} vs. I_{off} among published vertical NW TFETs based on III-V materials at V_{dd}= 0.3 V (V_{ds}=0.3 V, ΔV_{gs}= 0.3 V). Compared to other III-V NW TFETs, our devices deliver high I_{on} at low I_{off}. These results are testimony to the increased flexibility and precision heterostructure growth that are afforded by a top-down fabrication approach.
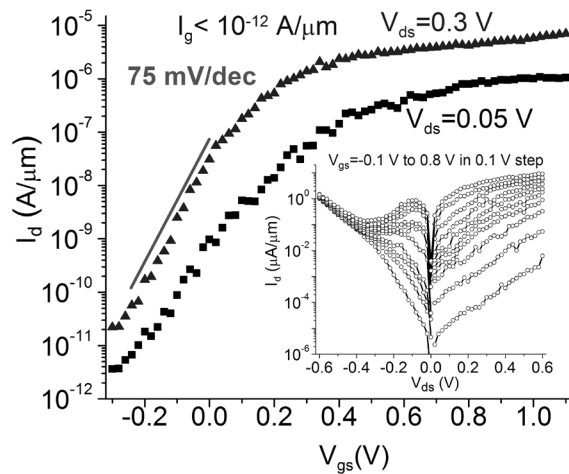
▲ Figure 1: Subthreshold and output characteristics in semilog scale (inset) of a 50-nm diameter single-NW TFET. The device has a channel length of 60 nm, and the gate dielectric consists of 2.2 nm of Al$_2$O$_3$.
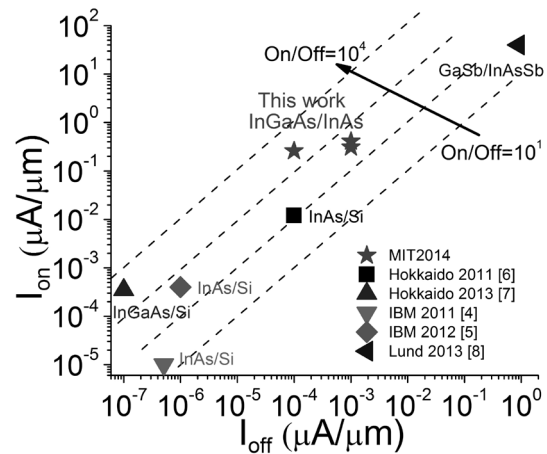
▲ Figure 2: I_{on} vs. I_{off} at V_{dd}=0.3 V (V_{ds}=0.3 V, ΔV_{gs}= 0.3 V) for recently published vertical NW TFETs containing III-V materials. All devices but the present ones are fabricated through bottom-up techniques.

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GaN-based High Electron Mobility Transistors for High Power THz Source

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Sponsorship: Office of Naval Research PECASE, ARO, DARPA DAHI program

The outstanding properties of gallium nitride (GaN) such as high electron velocity (~ 2.5 × 10^7 cm/s) and high breakdown electric field (~ 3.3 MV/cm) make it an ideal candidate for applications requiring high power at high frequencies where conventional semiconductors, e.g., Si and GaAs, are incapable. Over the last decade, tremendous efforts have been concentrated on high power GaN-based high electron mobility transistors (HEMTs) to operate from the millimeter wave frequency (100 - 300 GHz) towards the THz range (300 GHz – 30 THz). At the moment, focal plane imaging array systems with the current state of high power THz sources are suffering from significant scattering losses.

The goal of this project is to realize and demonstrate energy-efficient high power THz sources by utilizing GaN-HEMTs circuit design and technology platform. The large THz frequency band is challenging to reach via traditional electronic and optical methods. Therefore, there is an immediate need to develop alternative approaches for future applications operating at high power and frequencies. In this project, we have developed a novel circuit design of a high power self-feeding GaN oscillator, which has been modeled to generate the 2nd harmonic ($2f_0$) of a signal with a frequency exceeding 300 GHz (Figure 1).

The standard AlGaN/GaN HEMTs on SiC substrate have been fabricated, using a T-shaped gate with a deep submicron gate length. The device exhibits a current density of >1 A/mm and excellent pinch off characteristics. The extracted transition frequency f_T is about 125 GHz (Figure 2). The electrical models for circuit simulation are undergoing for this device. In order to push further the frequency performances of the HEMTs (> 150 GHz), designs are being carefully optimized, e.g., by reducing the source-to-drain distance to boost the current density, re-designing a T-shape gate with thick top metal for reducing the gate resistance, and optimizing the dielectric stack to reduce the parasitic capacitance.
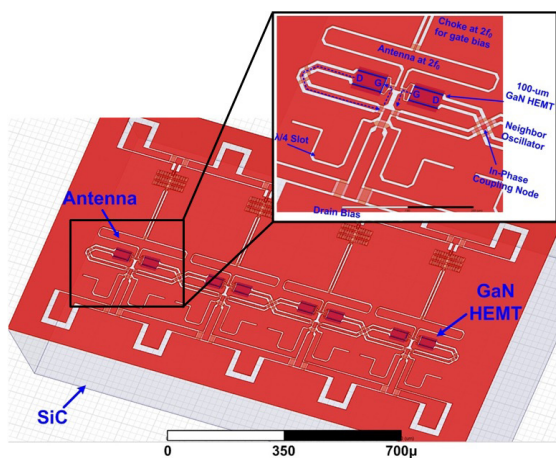
▲ Figure 1: Prototype of a 180-GHz GaN radiating oscillator array, with 4 elements (8 GaN HEMTs). The zoom-in exhibits the oscillator unit cell and describes the self-feeding oscillation structure with 2nd harmonic ($2f_0$) signal radiation.
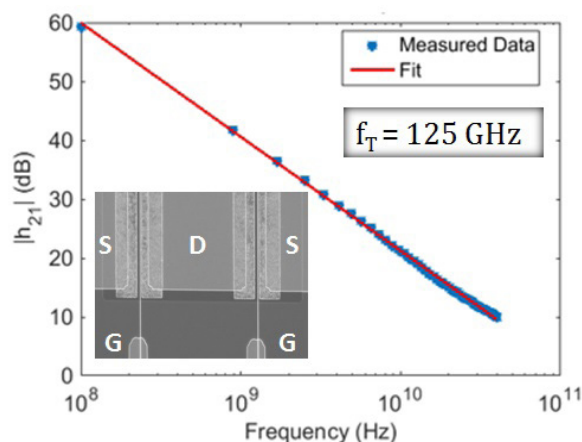
▲ Figure 2: Small signal performance of an AlGaN/GaN HEMT-on-SiC substrate with f_T ~ 125 GHz. The inset presents a top view of the device with L_g = 80 nm and width = 2x100 μm.

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Study of Phase Noise in GaN-Based Ring Oscillators

U. Radhakrishna, P. Choi, D. A. Antoniadis
Sponsorship: Singapore-MIT Alliance for Research and Technology LEES program, National Science Foundation NEEDS program, MIT/MTL GaN Energy Initiative

Modeling GaN-based HEMTs has gained considerable attention in recent years because of superiority in high-power and high-frequency performance, making them the key candidate for RF applications. The design requirements of GaN-based RF circuits motivate GaN-compact device models to include accurate description of device small signal, large signal and noise performances. The design of oscillators that are used in GaN-based microwave monolithic integrated circuits as voltage-controlled oscillators in the receiver stage and in wired-communication as clock sources requires the modeling of phase noise or jitter.

Prior works on the physics-based MIT Virtual Source GaNFET (MVSG) model demonstrated its physical grounding along with its usefulness in RF circuits design. This work demonstrates the usefulness of the MVSG model in the design of GaN-based oscillators. The model with its accurate representation of small- and large-signal device characteristics along with RF- and low-frequency noise behavior can be used for the design of oscillators with the desired frequency response including the close-in phase noise performance. The MVSG model is benchmarked against device terminal DC-, small-signal S-parameter-, and noise figure measurements and is used to design a 3-stage GaN pseudo-invertor ring oscillator, delivering 21 dBm at 1.4 GHz. It is found that the MVSG model provides accurate estimation of large-signal device-switching behavior along with the device-flicker (1/f) noise-dominated phase noise. The dependence of phase noise level on the DC component of the impulse sensitivity function (ISF) is confirmed using the model and measurements. In this work, the physics of carrier charge and transport in a GaN-HEMT along with device-level noise is translated into functional RF-circuit elements using the MVSG model.
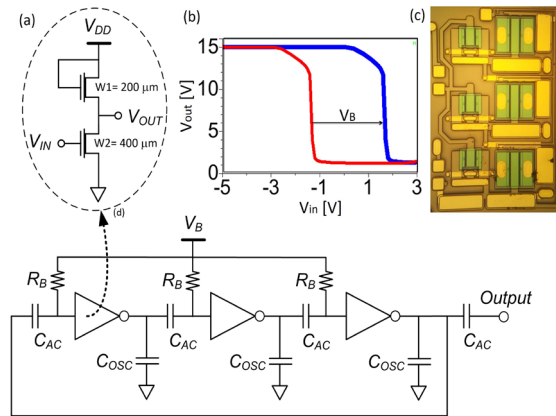
▲ Figure 1: Capability of MVSG model to capture the device phase noise and large signal behavior can be studied simultaneously using an RO circuit. (a) The absence of E-mode devices requires a pseudo-inverter topology using a drain-gate connected FET. (b) The voltage transfer characteristic (VTC) shows a transition at negative input voltage (V_{in}) (red) due to the negative threshold voltage of depletion mode GaN HEMTs. To shift the transition to a positive V_{in} (blue), a negative gate bias (V_B) through R_B and ac-coupled capacitor (C_{AC}) is required. (c) The die micrograph image and (d) the 3-stage RO schematic with V_B, ac-coupled capacitor are also shown.

▲ Figure 2: (a) Time domain waveforms and (b) frequency spectrum of output voltage of RO are shown. (c) Phase noise spectrum is compared to simulation with flicker noise model capturing phase noise ($1/f^3$) spectral levels and corner frequencies accurately. (d) $1/f^3$ is found to be proportional to DC component of ISF (Γ_{DC}), which depends on derivative of output node waveforms (i.e., rising and falling edge slopes); it can be captured by model as shown. (e) Table shows Γ_{DC} calculated from ISF at different V_{DD}. (f) Linear relationship between $1/f^3$ noise level at 500 Hz offset frequency and Γ_{DC} can be verified from model and measurements.

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# Process Development for GaN/SOI Heterogeneous Integration

D. Piedra, S. Rennesson, T. Palacios
Sponsorship: DARPA DAHI Program

Silicon complementary metal–oxide–semiconductor (CMOS) technology has been at the forefront of the microelectronics revolution, benefiting from years of process development allowing for advances in device scaling and integration density. However, deeply scaled Si CMOS faces challenges in high-voltage and high-power density applications. The monolithic heterogeneous integration of GaN devices with Si CMOS in the power amplifier and power conversion stages would allow performance unachievable by Si alone. The approach taken in this project is to grow AlGaN/GaN structures in patterned windows on an 8" SOI wafer. This paper focuses on the development of high electron mobility transistors (HEMTs) that are then fabricated in the GaN windows using Si compatible process technology.

One of the key technologies to develop for CMOS process compatibility is a gold (Au) free ohmic contact technology. Excellent device performance has been reported in GaN HEMTs using Au-based ohmic contacts. However, for successful heterogeneous integration, the GaN HEMT ohmic contats must be processed without gold. The process flow currently consists of etching a recess in the ohmic pattern by reactive ion etching, followed by sputtering a metal stack of Ti/Al, patterning the ohmic contacts, etching the metal stack, and finally annealing the patterned metal at 550°C. As seen in our results (Figure 1), the contact resistance is extremely sensitive to the recess depth.

In parallel to our development of Au-free ohmic contacts, we have processed devices in the GaN windows of different sizes and shapes (square or rectangle). Both HEMT and Van der Pauw squares were processed (Figure 2) to measure a full suite of device and material characteristics including breakdown voltage, current collapse, Hall mobility, and carrier concentration.
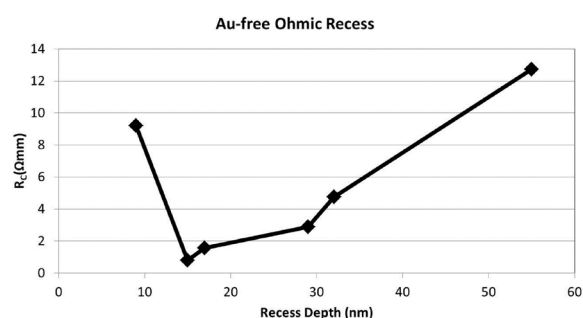
▲ Figure 1: GaN HEMT contact resistance as a function of ohmic recess depth.
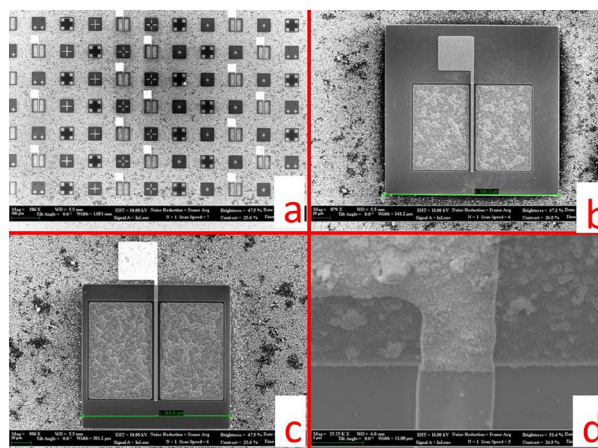
▲ Figure 2: Scanning electron microscope image taken from the processed GaN on patterned SOI wafers.
2a) array of HEMTs. 2b) HEMT in 200x200μm² window.
2c) HEMT in 150x150μm² window.
2d) gate pad coverage of the window edge step.

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Vertical Transistors and Diodes on Bulk GaN Substrates

M. Sun, Y. Zhang, T. Palacios
Sponsorship: ARPA-E Switches Program

New opportunities for higher efficiency power electronics have emerged with the development of GaN. However, most GaN discrete devices demonstrated to date have had relatively low current ratings in addition to high cost. Recent research results indicate that advances in new materials could substantially accelerate progress towards GaN devices that achieve both higher current ratings and functional cost parity with silicon-based devices. Vertical device architectures for GaN power semiconductor transistors could substantially reduce cost and increase current densities. Our group has been working to develop new fabrication technologies to reduce the cost of vertical PIN diodes and transistors.

In the vertical PIN diodes fabricated at MTL, the mesa etch was performed in an ICP-RIE system by using Cl_2/BCl_3 gas. A wet etch was followed to achieve a smooth etching sidewall to reduce sidewall leakage. Ni/Au metal was annealed in oxegen ambien to form ohmic contacts with p-GaN. A field plate was made to reduce peak electric field at the device edge. The cathode electrode was formed on the rear surface of the device. An on resistance of 1 mΩcm² was achieved on these diodes with a breakdown voltage more than 700 V. The leakage current of the diodes is below 10^{-7} A/cm², significantly lower than GaN devices on foreign substrates.

A conventional current aperture vertical electron transistor (CAVET) requires the regrowth of the AlGaN/GaN access region, which significantly increases the cost of the device. In addition, it is very difficult to have highly insulating current blocking layers between the access region and the drain drift region, which makes it very difficult to increase the breakdown voltage in these devices. To solve these problems, we have proposed a new vertical GaN JFET structure that uses a top-down fabrication technology based on dry etching. No regrowth is needed, therefore lowering the cost and complexity.
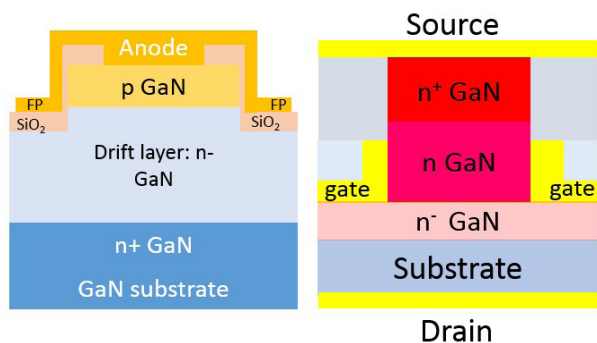
▲ Figure 1: Cross-sectional view of vertical GaN PIN diode (right) and vertical GaN JFET.
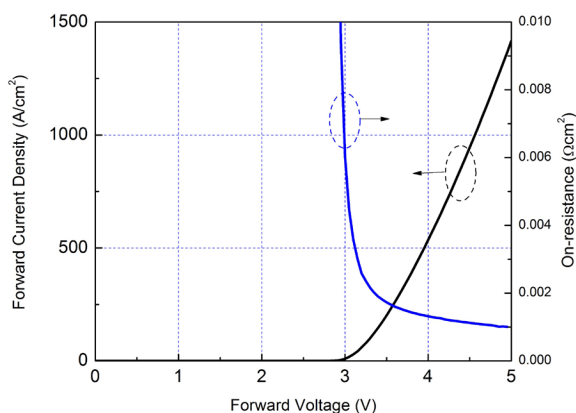
▲ Figure 2: Forward characteristics of vertical GaN PIN diode.

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Positive-Bias Temperature Instability in GaN Power Field-Effect Transistors

A. Guo, J. A. del Alamo
Sponsorship: NDSEG Research Fellowship

Galium nitride (GaN) is a promising material for replacing silicon in power switching applications. Recently, GaN-high electron mobility transistors with insulated-gates (GaN MIS-HEMT) have attracted much attention because they offer high current, low gate leakage and high breakdown voltage, all desirable for power transistors. However, GaN MIS-HEMTs suffer from threshold voltage (V_T) instability after prolonged high-voltage stress at high temperature (usually referred to as bias temperature instability, or BTI). It is challenging to address this issue because the many layers and interfaces of a MIS-HEMT structure make it difficult to identify the physical origin of BTI. In this work, we study the positive-bias temperature instability (PBTI) in a simpler GaN metal-oxide-semiconductor field-effect-transistor (MOSFET) (Figure 1). This structure allows us to focus specifically on stability issues associated with the oxide and the oxide/GaN interface.

We developed a benign process to characterize the devices before, during, and after stress experiments. In a typical experiment, we first characterize a device and identify a "stable" initial state as a reference for subsequent stress/recovery experiments. The PBTI stress phase consists of a series of stress segments of increasing stress voltage (V_{GS_stress}>0), stress time (t_{stress}) and temperature (T). During stress, a device is subject to a constant positive gate stress with other terminals grounded. Immediately after each stress segment, we evaluate the evolution of V_T and subthreshold swing (S) through repeated, short I_D-V_{GS} sweeps. At the end of each segment, the device is reinitialized by a thermal baking step, and a complete I_D-V_{GS} characterization is performed.

We studied PBTI in GaN MOSFETs with SiO_2 as the gate dielectric. We carried out experiments with V_{GS_stress} between 5 and 15 V, t_{stress} between 10 and 10,000 seconds and T at -40°C, room temperature (RT) and 75°C. We found that V_T shifts are positive and increase with V_{GS_stress}, t_{stress} and T. In all studied devices, this V_T shift is completely recoverable after $V_{GS\_stress} \leq 10$ V and T $\leq$ RT but only partially recoverable after V_{GS_stress} = 15 V. Figure 2 shows the stress time evolution of ΔV_T for V_{GS_stress} = 15

V at RT. In all cases, we are able to model the recoverable portion of ΔV_T using a well-established oxide trapping model. We conclude that the recoverable ΔV_T is due to electron trapping in pre-existing oxide traps and the non-recoverable ΔV_T is due to the creation of interface states at the oxide/GaN interface. Our findings are consistent with PBTI studies for silicon and other material systems.
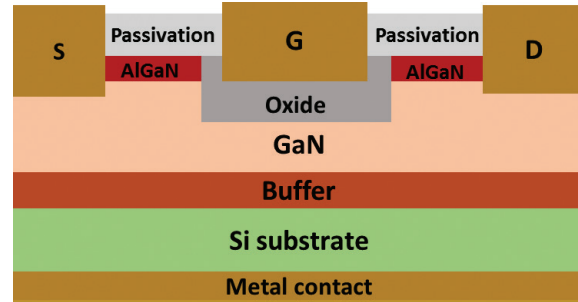
▲ Figure 1: GaN MOSFET structure studied in this work.
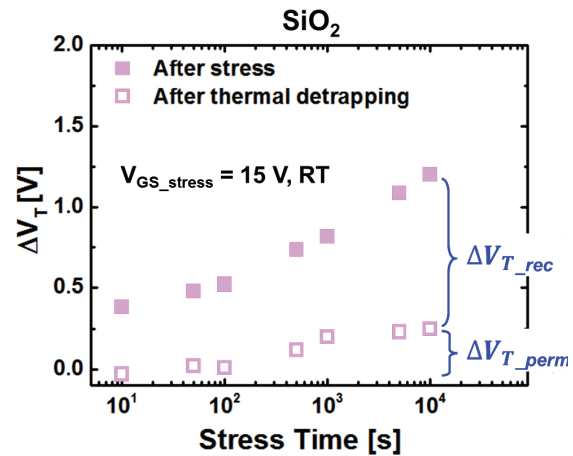
▲ Figure 2: Stress time evolution of ΔV_T for GaN MOSFETs with SiO_2 as gate dielectric for V_{GS_stress} = 15 V at RT. Filled symbols are the total ΔV_T extracted 1 sec after stress, and open symbols are the non-recoverable ΔV_T after a thermal bake. ΔV_{T_rec} stands for recoverable ΔV_T, and ΔV_{T_perm} stands for non-recoverable or permanent ΔV_T.

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Oxide Breakdown in High-Voltage GaN Field-Effect Transistors

S. Warnock, J. A. del Alamo
Sponsorship: Texas Instruments

As the demand for more energy-efficient electronics increases, GaN field-effect transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN power transistors are ready for commercial deployment. One of the concerns is gate oxide reliability as a result of high-voltage stress. In particular, after prolonged high-voltage gate bias stress, the oxide will suffer from catastrophic breakdown beyond which the transistor is no longer operational.

Our research is directed to providing fundamental understanding behind the physics of time-dependent dielectric breakdown (TDDB) of the gate oxide in GaN metal-insulator-semiconductor high electron-mobility transistors (MIS-HEMTs). We leverage a rich body of work that has been performed on silicon MOSFETs with regards to TDDB.

Figure 1 shows the evolution of the gate current I_G in a classic TDDB experiment in a GaN MIS-HEMT. Here, we hold a high positive gate bias until breakdown occurs, which we can observe as the sudden jump in gate current, I_G, around 225 s. Through this experiment, we can observe first a decrease in current due to trapping and then an increase in what is known as stress-induced leakage current, SILC. This increase results from the generation of defects in the oxide. The observed characteristics in Figure 1 constitute fairly classic TDDB behavior.

Experiments such as the one in Figure 1 give limited information about oxide degradation during stress. A richer picture emerges if we perform a similar experiment where the stress is periodically paused to measure the subthreshold characteristics of the device, as shown in the inset of Figure 2. This figure reveals a large positive shift in the threshold voltage followed by a small negative shift as the experiment progresses. We also observe a fixed immediate degradation in the subthreshold swing S that suggests interface state generation early in the stress experiment. The change in direction of V_T, as well as the degradation in S, both occur in the same regime where we see the appearance of SILC in Figure 1.

Through experiments such as these, we hope to gain an understanding of the fundamental mechanisms behind oxide breakdown as well as build models that allow us to predict device lifetime under realistic operating conditions.
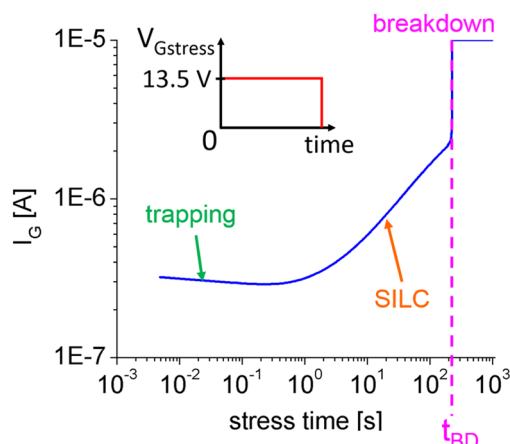
▲ Figure 1: Gate leakage current as a function of stress time during a constant $V_{Gstress}$ TDDB experiment at room temperature. The FET is held at V_G=13.5 V until the device breaks down. V_{DS}=0 V.
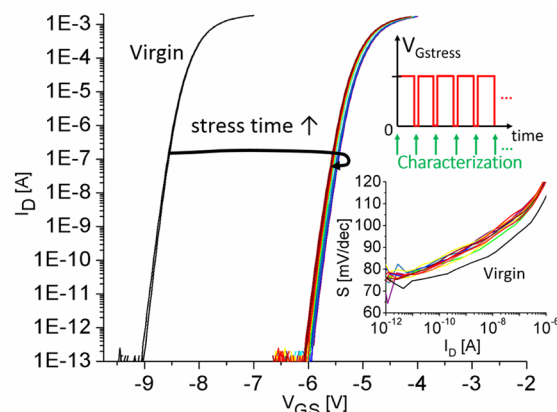
▲ Figure 2: Subthreshold characteristics at V_{DS}=0.1 V, for a TDDB experiment at $V_{Gstress}$=13.5 V. I-V characterization is performed every 30 s. The insets describe the experimental procedure and the degradation of the subthreshold swing S.

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Permanent Degradation of InAlN/GaN HEMTs under High-Power Stress

Y. Wu, J. A. del Alamo
Sponsorship: National Reconnaissance Office

First demonstrated in the 1990s, GaN transistors have started to become commercially available in recent years. GaN is the technology of choice for high-power applications in electronic warfare, radar, satellites, cable TV, and cellular mobile communications. Compared with other commonly used materials such as Si and GaAs, GaN devices can operate at higher voltages and frequencies, thus enabling significant improvements in power efficiency and dramatic reduction in size.

In contrast with the conventional GaN HEMT with AlGaN as barrier layer, the use of an InAlN barrier yields, for the same layer thickness, a higher spontaneous polarization-induced charge at the barrier/GaN interface. This enables aggressive barrier thickness scaling and therefore gate length scaling. As a result, InAlN/GaN HEMTs, are extremely promising for very high-frequency applications. However, unlike the better understood AlGaN/GaN system, degradation mechanisms in InAlN/GaN HEMTs are not well established. Our project aims to study the leading degradation modes of InAlN/GaN HEMTs under different stress conditions with the ultimate goal of constructing models to predict device lifetime.

We are studying the degradation of InAlN/GaN MIS-HEMTs under prolonged biasing in the OFF, semi-ON, and ON-states. Negligible device degradation takes place in both OFF and Semi-ON states, which is in drastic contrast to the AlGaN/GaN structure known to be vulnerable to semi-ON-state stress. Under ON-state high-power stress, however, InAlN/GaN HEMTs can undergo significant permanent degradation, which is reflected in a decrease in the saturation drain current, an increase in gate leakage current, and degradation of other important figures of merit. With further exploration, we have found that both high voltage and high current are necessary to induce significant device degradation. This suggests something more than just an electric-field-driven degradation mechanism. Also, a close examination of the terminal currents of a degraded device reveals the appearance of a gate-to-source leakage path of a unique character, as illustrated in Figures 1 and 2. Before stress (Figure 1), all three terminal currents demonstrate thermionic field emission dominated behavior whereas after stress (Figure 2), the gate and source currents suggest ohmic conduction while the drain current still maintains the signature of a virgin device. This strongly suggests a degradation mechanism that affects the source side of the device instead of the drain side, which is where the high electric field is present. We are currently studying this puzzling behavior in more detail.
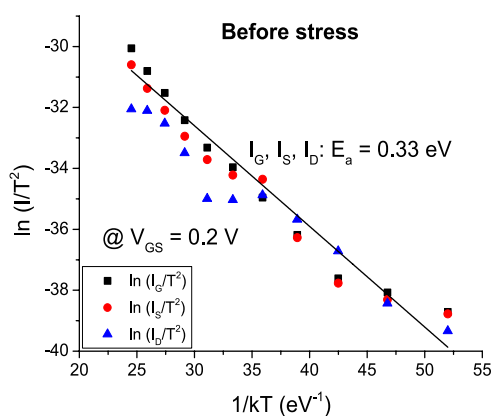
▲ Figure 1: Arrhenius plot for I_D, I_G, and I_S of a virgin InAlN/GaN HEMT at V_{GS}= 0.2 V and V_{DS}=0 V. All three terminals show thermionic-field-emission dominated current with an activation energy of 0.33 eV.
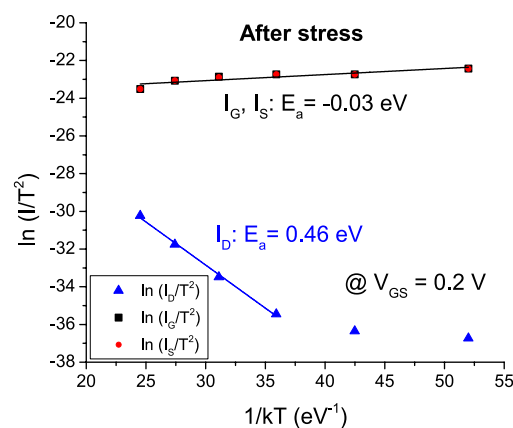
▲ Figure 2: Arrhenius plot for I_D, I_G, and I_S after high-power stress for the same device as in Figure 1. The currents are measured at V_{GS}= 0.2 V and V_{DS}=0 V. The drain current maintains the signature of a virgin device while the gate and source currents have drastically increased and changed character.

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Reliability of AlGaN/GaN HEMTs on Silicon

W. A. Sasangka, G. J. Syaranamual, C. L. Gan, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology

Integration of AlGaN/GaN high electron mobility transistors (HEMTs) on the silicon platform is attractive for many reasons. Having both high-power-high-frequency AlGaN/GaN HEMTs and established Si complementary metal-oxide semiconductor (CMOS) devices in a single chip would open up many new applications. It would also allow cost-effective large-scale fabrication of complex system by building on existing silicon technology and infrastructure, including the use of 300 mm wafers. However, market adoption of such a technology is still limited due to concerns about HEMT device reliability.

Due to its high lattice mismatch, epitaxial growth of AlGaN/GaN on silicon substrates results in a very high threading dislocation density ($\sim 10^9$/cm^2). This is one to two orders of magnitude higher than the typical threading dislocation density of AlGaN/GaN grown on SiC or sapphire. The threading dislocation density significantly affects the electrical degradation of the devices. However, correlations with physical degradation mechanisms are still unclear. Past work has established a correlation between electrical deg-radation and physical degradation, in the form of pits that appear in the GaN capping layer and AlGaN layer along gate edges where high electric fields exist. The mechanism of pit formation has been associated with the presence of water, which, even in the presence of SiN passivation layers, leads to electrochemical oxidation of aluminum and gallium oxide.

We have investigated the role of threading dislocations in pit formation during stressing of AlGaN/GaN on Si high electron mobility transistors under high reverse bias. Upon stressing, the drain current saturation ($I_{D-saturation}$) decreases over time. The amount of $I_{D-saturation}$ degradation correlates well with pit formation at the gate-edge, where the electric field is the highest. Using a transmission electron microscope weak-beam technique, it was found that pits tend to nucleate at threading dislocations that have a screw component, even when these dislocations are at locations away from the gate-edge. An explanation based on an electrochemical oxidation model has been proposed.
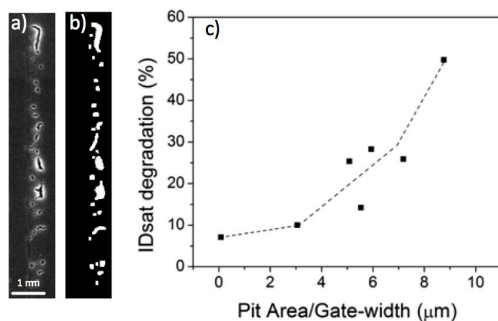
▲ Figure 1: a) Top view SEM image of a device with pits. b) After image processing using Image J software, pits are indicated in white. This allows pixel computation of the pit area. c) $I_{D-saturation}$ degradation as a function of pit area/gate-width.

▶ Figure 2: a) to c). Cross-sectional TEM images of stressed devices before metal removal, taken along the [210] zone axis. Pits are seen to form at locations away from E_{max} (the gate edge). d). Image of sample c) taken using a weak beam technique at g (002). e) Image of sample c) taken using a weak beam technique at g (120).
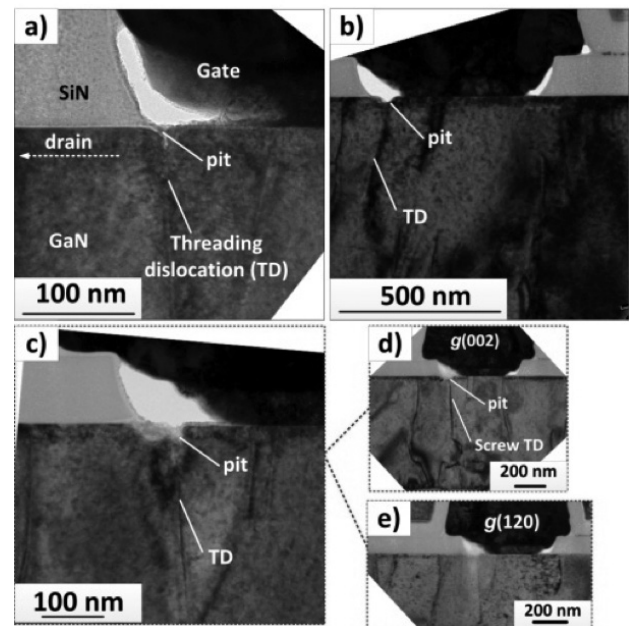
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# Transient Thermal Dynamics of GaN High Electron Mobility Transistors

K. R. Bagnall, E. N. Wang
Sponsorship: MIT/MTL GaN Energy Initiative, Singapore-MIT Alliance for Research and Technology LEES program

Gallium nitride (GaN) high electron mobility transistors (HEMTs) are one of the most promising compound semiconductor technologies for high-frequency communication and high-voltage power conversion applications. In particular, the high critical electric field, electron concentration, and electron mobility enable GaN HEMTs to have a lower on-resistance than transistors based on silicon with the same breakdown voltage. However, the high power density present in GaN HEMTs for radio-frequency (RF) and power switching applications results in high channel temperatures due to self-heating and degradation in device performance and lifetime. Although self-heating in GaN HEMTs has been studied comprehensively with modeling and experimental approaches, much of this work has focused on steady state conditions. In this work, we are developing analytical models for transient thermal dynamics in GaN HEMTs as well as experimentally characterizing devices with time-resolved micro-Raman thermography.

Transient power dissipation resulting in a time-dependent channel temperature occurs in many contexts in which GaN HEMTs are utilized: pulse mode radar, cellular base stations, and switch mode power converters. To facilitate design and packaging of GaN HEMTs for these applications, we have developed a semi-analytical thermal model for the transient temperature rise in multi-layer HEMT structures based on Fourier series expansions and numerical Laplace transforms. Like our previous work on steady state thermal modeling, this model provides rich physical insight, e.g., identifying the dominant thermal time constants associated with multi-dimensional heat diffusion over several length scales. As Figure 1 shows, we have demonstrated that a single time constant, often assumed to be ~1 µs for typical GaN HEMTs, poorly represents the transient temperature response by underestimating the channel temperature rise for times ~100 ns. To validate this modeling, we are developing an experimental setup based on time-resolved micro-Raman spectroscopy to measure the GaN buffer temperature with ~1-µm spatial, 10 °C temperature, and 20-ns time resolution. We have successfully implemented this technique and measured the transient temperature rise of GaN-on-sapphire ungated HEMTs subject to pulsed power dissipation as shown in Figure 2. This combination of computationally-efficient thermal modeling and rigorous experimental characterization can lead to greater understanding of transient thermal dynamics of GaN HEMTs to improve reliability and performance.
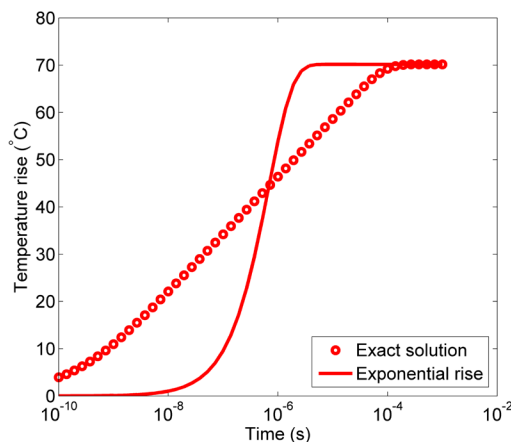
▲ Figure 1: Modeled transient temperature response of a 100-µm silicon slab representing a GaN-on-Si HEMT structure. An exponential function with a single time constant significantly underestimates the temperature at times less than ~1 µs.
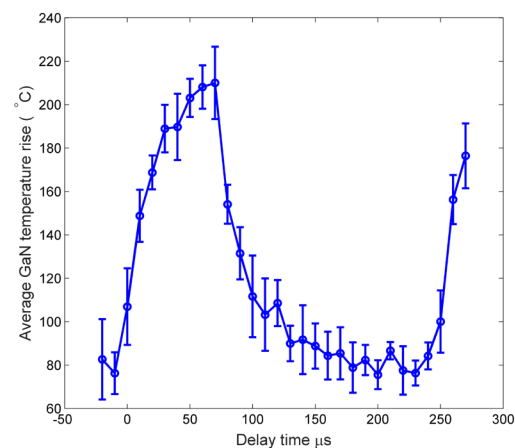
▲ Figure 2: Temperature of GaN-on-sapphire ungated HEMT measured by time-resolved micro-Raman spectroscopy. A pulsed power dissipation of 4 W/mm was applied for 75 µs, and the device was allowed to cool for 175 µs.

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# Thermal Characterization of GaN HEMTs via Photo-Thermal Reflectance Thermography

B. Barabadi, K. R. Bagnall, Y. Zhang, T. Palacios, E. N. Wang
Sponsorship: MIT/MTL GaN Energy Initative, MIT-Singapore SMART LEES Program

Gallium nitride- (GaN) based high electron mobility transistors (HEMTs) have gained a significant amount of interest over the last few years for their excellent electrical properties, high efficiencies, and high power densities for both power electronics and radio-frequency applications. However, these high power densities result in high channel temperatures and temperature gradients that induce thermo-elastic stresses, formation of defect sites, and many other degradation mechanisms that substantially affect the performance and reliability of GaN HEMTs. Therefore, it is important to develop reliable tools for thermal characterization of GaN HEMTs. Temperature measurement in these devices, however, is extremely challenging due to the requirement of high spatial resolution, the geometrical complexities, and the variety of materials present (metals, semiconductors, and insulators). As previously demonstrated, the extremely high temperature profile in a GaN HEMT occurs in a region (~0.5 to 1 µm) over which the dissipated power density is very high (~10^{10} W/m^2). In fact, the state of the art thermal measurement techniques are simply incapable of capturing this highly localized temperature profile of the devices being tested. Our objective is to develop a reliable approach to detect thermal phenomena with nanoscale spatial resolution (below 500 nm) under various input powers that can significantly affect the performance of GaN-based devices.

To have a comprehensive understanding of thermal management in GaN devices, we have utilized photo-thermal reflectance thermography, a well-established technique that is fully optical and noncontact. Thermoreflectance imaging has several advantages over the currently available high resolution techniques: it provides a thermal map of the device, and it also provides surface measurements, which is crucial due to the unique geometries of transistors. The schematic of the setup is shown in Figure 1. By choosing the appropriate illumination wavelength, we have achieved a spatial resolution of 0.3 µm for gated and ungated AlGaN/GaN structures on different substrates. We have also improved the photo-thermal reflectance setup by developing a new calibration method and optimizing the temperature measurement procedure to obtain a reliable and accurate map of the temperature profiles for various input powers. Figure 2 (a) shows an optical image of a two-finger GaN HEMT on SiC during thermal measurements. The device was biased at voltages ranging from 0 to 25 V. Figure 2 (b) demonstrates a representative temperature profile at the interface of AlGaN/GaN close to the gate for the case in which the device is biased at 20 V and the gate voltage is 1 V. As can be seen, the temperature rise of up to 80 °C occurs in a considerably localized area (less than 2 µm) adjacent to the gate, where power densities are significantly high. This work helps us to better understand the structural and thermal changes in GaN HEMTs, the formation of defect cites, and their relation to temperature through high-resolution thermal imaging.
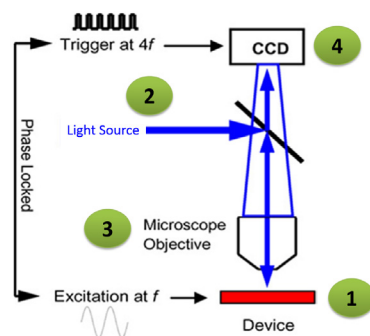
▲ Figure 1: Schematic of thermal-reflectance setup (adapted from third reading).
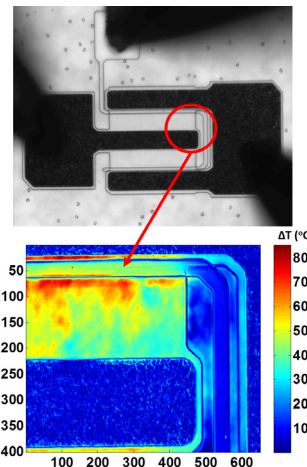
◄ Figure 2: -(a) Optical image of a two-finger GaN HEMT during measurements, (b) temperature profile in a zoomed-in view of the device.

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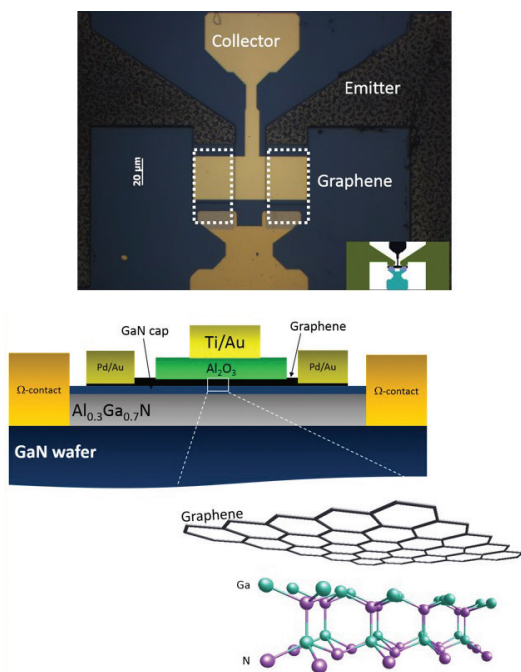
Vertical Graphene-on-GaN Hot Electron Transistor

A. Zubair, Y. Song, J. Kong, M. Dresselhaus, T. Palacios
Sponsorship: Army Research Office

Two-dimensional materials have been extensively studied as promising candidates for future high-speed electronics. The very high room-temperature carrier mobility, saturation velocity, and thermal conductivity of graphene make it an attractive candidate for high frequency electronics. Although remarkable RF performance has been demonstrated in lateral graphene transistors, their performance is still limited by lack of current saturation caused by the absence of bandgap in graphene. At the same time, III-nitride heterostructure ($Al_xGa_{1-x}N$/GaN) high electron mobility transistors (HEMTs) are promising for high frequency and high-power operation (due to wide bandgap and high critical field), but their intrinsic current gain cutoff frequency is limited by smaller electron saturation velocity. The integration of graphene and GaN in a single vertical hot electron transistor can utilize the potentials of both materials systems in high frequency electronics, overcoming the limitations present in lateral transistors.

In this work, we design and fabricate a novel vertical graphene transistor, a majority-carrier device where a monolayer graphene base is sandwiched between a metal collector and an AlGaN/GaN heterojunction emitter (Figure 1). The transport characteristics of first device prototype (Figure 2) exhibits very promising current density (~kA/cm²), current gain (α~50%), and moderate on-off ratio (~300). The measured current density is the highest among all the graphene-based hot electron transistors reported so far in the literature. Simulations further support the notion that with proper optimization of the materials and device structure, the proposed transistor can be a promising candidate for future high frequency applications.

▲ Figure 1 Optical image and schematic diagram of graphene-on-GaN graphene base transistor. Emitter contact to the two-dimensional electron gas in GaN/AlGaN heterojunction consists of a Ti/Al/Ni/Au.
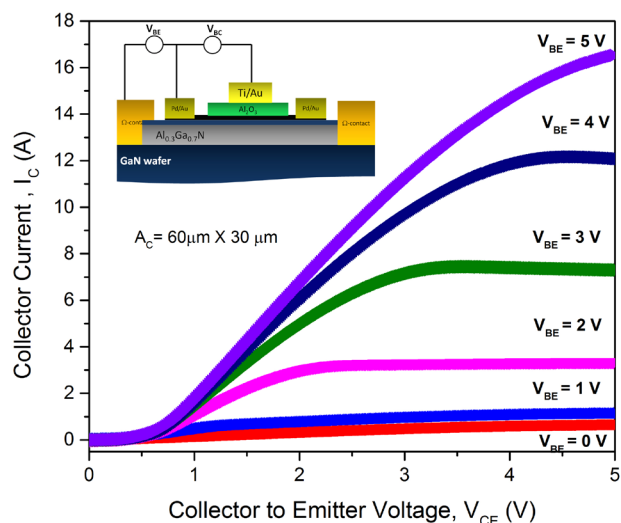
▲ Figure 2 Common-emitter characteristics of the fabricated hot electron transistor at different base to emitter voltages (V_{BE} -0-5 V), showing high current density.

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High Performance 15-nm Channel Length Double-Gate MoS$_2$ Field-Effect Transistor

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Sponsorship: Office of Naval Research PECASE, Army Research Laboratory

Mono- and multiple layers of molybdenum disulphide (MoS$_2$) have great potential in device applications because of the large bandgap, thermal stability, high carrier mobility, and compatibility with CMOS processes. Field-effect transistors (FETs) built on a few layers of MoS$_2$ are effectively ultra-thin body FETs (UTB-FETs), which have an optimized structure to reduce short channel effects. Also, the heavier effective mass of MoS$_2$ compared with Si allows the transistors to have an increased drive current when benchmarked against UTB-silicon transistors at their scaling limit.

In this work, we demonstrate the fabrication and electrical characteristics of a double-gate MoS$_2$ FET using single-layer graphene (SLG) as the source/drain (S/D) contacts and a record channel length of 15 nm. A 3-nm MoS$_2$ thin film was transferred onto a p-doped silicon substrate covered with 10 nm of HfO$_2$ as the back gate. Subsequently, the SLG was transferred onto the MoS$_2$ layer. SLG has metallic properties with two-dimensional ballistic electronic transport. A 15-nm polymethyl methacrylate (PMMA) trench was patterned on the SLG followed by selective etching of the SLG, creating a 15-nm slit that defined the S/D channel. After PMMA removal, 10 nm of HfO$_2$ and 50 nm of Ni were deposited onto the channel as the top gate. Figure 1 shows a schematic of the device and an atomic force microscopy (AFM) image of sub-20-nm-wide graphene slits.

The MoS$_2$ FET had an on/off ratio of greater than 10^6 with an on-current of ~50 μA/mm and minimum subthreshold slope of 90 mV/dec at drain-voltage V$_{DS}$= 0.5 V (Figure 2). To the best of our knowledge, this MoS$_2$ transistor has the shortest operating channel length of any MoS$_2$ transistor demonstrated to date. Without significant optimization, this transistor already performs as well as much larger state-of-the-art silicon-on-insulator transistors in many aspects. The high on/off ratio indicates that further scaling is possible.
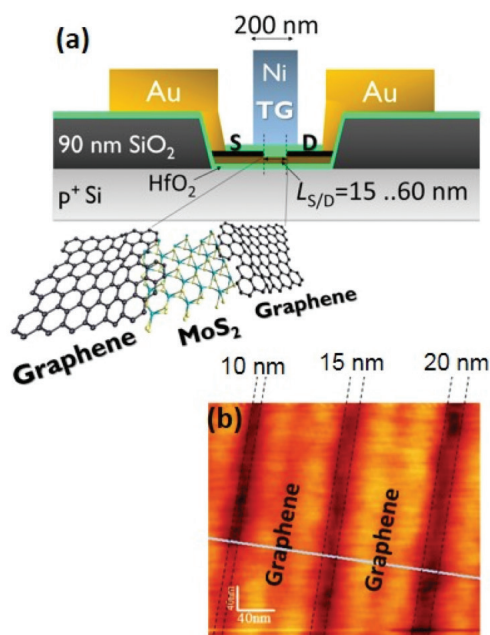
▲ Figure 1: (a) Schematic of the short channel double-gate MoS$_2$ FET using SLG as the S/D contacts. (b) An AFM image showing 10-, 15-, and 20-nm graphene slits.
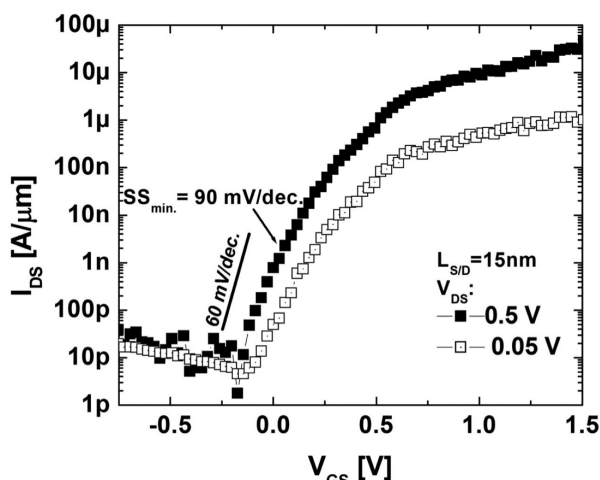
▲ Figure 2: The transfer characteristics of the 15-nm channel length double-gate MoS$_2$ FET at V$_{DS}$ = 0.05 and 0.5 V.

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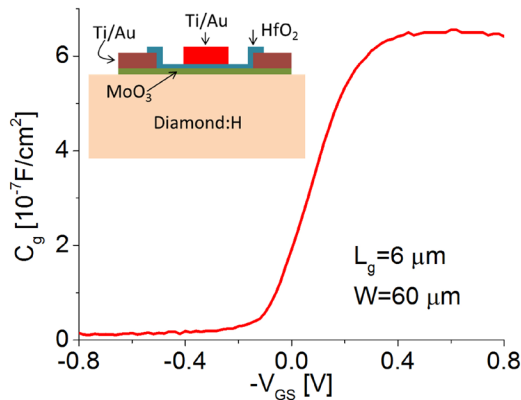
A Diamond:H/MoO$_3$ MOSFET

A. Vardi, M. Tordjman (Technion), R. Kalish (Technion), J. A. del Alamo
Sponsorship: Donner Endowed Chair, MIT-Technion Fellowship

Diamond is widely considered the ultimate semiconductor material for the realization of solid-state microelectronic devices. This is due to its unique combination of outstanding mechanical, electrical, and thermal properties, such as extreme hardness, high breakdown electric field, very high thermal conductivity, and high intrinsic carrier mobility at room temperature. Progress in the realization of diamond-based electronic devices has been hampered by the lack of suitable acceptors and donors with low activation energies. This drawback has been partially overcome through the discovery of "surface transfer doping," in which hydrogenated diamond (D:H) is exposed to different surface acceptors with high work function. Charge transfer between the hydrogen-passivated diamond surface and the absorbed species takes place and results in a highly conductive sheet of holes at the diamond sub-surface. The surface transfer doping system that has been most studied consists of D:H exposed to H$_2$O molecules. However, a major difficulty of the D:H/H$_2$O system is the gradual desorption of H$_2$O that occurs at even moderate temperatures (<200°C). Recently, MoO$_3$ has been shown to exhibit excellent transfer doping properties with D:H, yielding the highest yet reported areal hole density (up to 1x10^{14} cm^{-2}) and showing temperature stability up to at least 350°C. This makes this system attractive for D:H-based electronic devices. Here, we present the first demonstration of a D:H/MoO$_3$ transfer-doped MOSFET.

A schematic cross section of our transistor is shown in the inset of Figure 1. The starting substrate is a commercially available 3x3x0.5 mm^3 type IIa (001)-oriented single-crystal diamond. Surface hydrogenation was accomplished by exposure to pure hydrogen plasma in a CVD reactor. This was followed by thermal deposition of 4 nm of MoO$_3$. Device fabrication starts with mask definition for ohmic contacts followed by Ti/Au evaporation and liftoff. We used 10 nm of HfO$_2$ deposited by ALD as gate dielectric. Using flowable oxide (FOX) as a mask, the HfO$_2$ and MoO$_3$ films are defined by RIE. Following a standard photolithography step, a Ti/Au gate was lifted off.

Capacitance-voltage and current-voltage characteristics of a typical device are shown in Figure 1 and Figure 2, respectively. They both indicate classic p-type MOSFET behavior. High contact resistance limit the device performance, however, this can be mitigated by removing the MoO$_3$ under the S/D contacts (inset of Figure 1).

Although the results are modest, they clearly indicate the robustness of this new semiconductor heterostructure system, as no special measures were taken to protect the D:H interface during the process, which included several thermal steps up to 200C. Our work rekindles the hope for a future diamond electronics technology with unprecedented performance and robustness.

▲ Figure 1: Capacitance-voltage characteristics at 1 MHz of a typical device. Inset: transistor cross-section schematic.
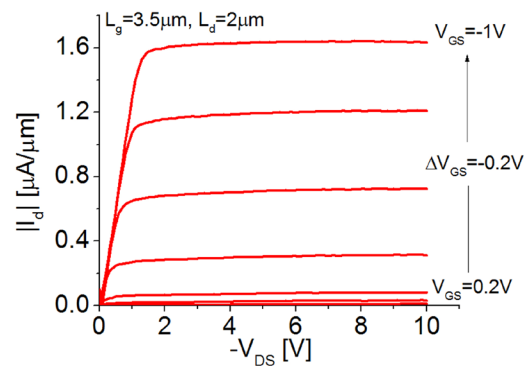
▲ Figure 2: Output characteristics of L$_g$=3.5 µm Diamond:H/MoO$_3$ p-type MOSFET.

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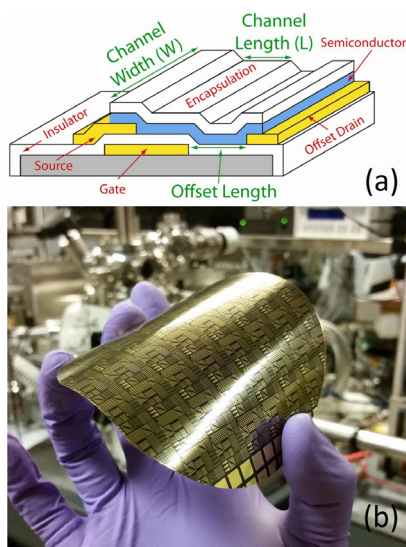# High-Voltage Organic Thin Film Transistor

A. Shih, M. A. Smith, A. I. Akinwande
Sponsorship: DARPA

Organic-based thin film transistors (OTFTs) have been identified as excellent candidates for flexible electronics due to the weak van der Waals forces between small molecules. OTFTs can be applied to develop wearable electronics such as artificial skin or sensor-enhanced prosthetics to introduce ubiquitous electronics and sensors on curved surfaces and to create novel compact systems such as a portable x-ray imager. However, enabling truly ubiquitous electronics through OTFTs demands not only a high performance, but also a wide range of operating voltages. Specifically, there are many applications that demand a high operating voltage beyond that capable of a typical thin film transistor. For example, ferroelectric liquid, electrophoretic or electro-optic displays, digital x-ray imaging, poly-Si cold cathodes, and other sophisticated integrated microelectromechanical systems (MEMS) all require large operating voltages to function.

In this work, we are developing a high-voltage organic thin film transistor (HVOTFT) based on the organic semiconductor pentacene ($C_{22}H_{14}$), operable at several hundreds of volts. The design of the pentacene-based HVOTFT is shown in Figure 1 (a). We have employed a bottom contact architecture along with organic compatible dielectrics Parylene-C and BZN ($Bi_{1.5}Zn_1Nb_{1.5}O_7$), the latter being a high-k material. The pentacene is then thermally evaporated on top of the contacts to form the active thin film (10-20 nm thick). The key design structure is to introduce an ungated region in series with the traditional gated region. The gated region allows for standard transistor switching behavior, while the ungated region enables the high voltage operation by acting as a resistor.

The device has been successfully fabricated on glass substrates as well as on flexible polyimide wafers, as shown in Figure 1 (b). Currently, devices exhibit excellent performances with charge carrier mobility of ~0.01 cm²/V•s, flexibility tolerance up to 1.5 in radius of curvature, and operating voltages beyond 300 V, as shown in Figure 2. Although the devices do exhibit short channel and impeded charge injection into the gated region, recent efforts such as the addition of a field plate above the interface of the gated and ungated regions have proven promising.

▲ Figure 1: (a) Cross sectional view of the high-voltage organic thin film transistor. (b) OTFTs made on flexible polyimide substrates.
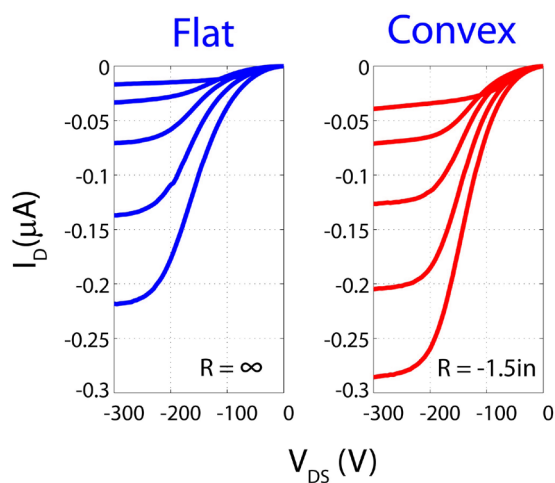
▲ Figure 2: High-Voltage Output Characteristics of HVOTFTs before and after flexure at a 1.5 in radius of curvature. The channel length is 10 µm with a 20 µm ungated region. The channel width is 20 µm. V_{GS} is stepped from 0 V to -20 V in -5 V increments.

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Characterization of SrRuO$_3$ and TaO$_x$ Resistive Switching Memory Devices by Scanning Tunneling Microscopy

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Sponsorship: MIT, National Science Foundation Center for Material Science Research, Forschungszentrum Jülich

Resisitive switching random access memory (Re-RAM) or memristive devices are considered contenders to become the next generation of information storage technology. Re-RAM devices are attractive compared to the current state-of-the-art flash devices due to their lower power consumption, high scalability, simple architecture, faster switching times (under sub-nanoseconds) and longer data retention. Although the technology is highly promising, the switching mechanisms are far from being well understood, thereby limiting the optimization of the Re-RAM device materials. The fundamental questions that need to be addressed on the switching mechanism of these devices include the effects of a strong electric field on defect creation and defect transport and the electronic structure. The inaccessibility of buried oxide films to several characterization techniques also makes the investigations of switching mechanisms more challenging.

In this work, we have induced and characterized localized electronic switching phenomenon under the electric field of the scanning tunneling microscope (STM) tip in a non-contact mode on electronically conducting and insulating oxides, SrRuO$_3$ and TaO$_x$, respectively. The advantage of this approach is that the switching can be studied at the local level, without necessitating a top electrode that buries the oxide. Localized area-wise switching is demonstrated in both oxides, in an area as small as 25 nm^2 in SrRuO$_3$. Scanning tunneling microscopy in spectroscopy mode provides electronic structure information, allowing us to characterize the switching process in-situ by a single experiment, which was not possible previously. The work highlights the use of tunneling microscope for characterizing diverse memory devices to understand the defect transport mechanisms under applied electric fields and variable oxygen partial pressure.

Carbon Nanotube Network using Silicon Oxide Non-Volatile Switches

A. D. Liao, P. T. Araujo, M. S. Dresselhaus
Sponsorship: Department of Energy

As mobile electronic devices become more prevalent in society, the need for compact and densely packed non-volatile memory (NVM) continues to grow. As flash memory fast approaches its scaling and power limits, other promising NVM technologies are being developed. Among these, resistive random access memory (RRAM) has gained popularity in industry because it utilizes materials that are in common use in semiconductor processing. These metal-insulator-metal (MIM) memory cells operate by switching the insulator between a high resistive state (HRS) and low resistive state (LRS). Whereas the switching mechanism to the LRS is well understood as oxygen atoms being removed from the lattice to form a conductive filament bridging the electrodes, there is not a complete consensus on the switching mechanism to return the MIM device to its HRS. It is known, however, that the type of metal used to contact the insulator may influence this switching mechanism. Furthermore, while it is typical to use a metal oxide7-9 (e.g., AlO_x, HfO_x, TiO_x) in the MIM cell, recently it was discovered that even silicon oxide could be switched between an HRS and an LRS.

In this study, we demonstrate a non-volatile switch that utilizes carbon nanotube networks to electrically contact a conductive nano-crystal Si filament in SiO_2. We sweep a voltage across the device until the CNT network undergoes Joule breakdown, creating a physical gap within the network. While the gap within an individual CNT network may vary from ~10 – 40 nm, the minimum gap size between different networks fluctuates by ± 3 nm. To prevent premature breakdown from oxidation, all measurements are performed in a vacuum (10^{-5} Torr). After the initial breakdown of the network, we observe a coalescence induced mode (CIM) at ~1860 cm^{-1} in the Raman spectrum, which is characteristic of linear sp hybridized carbon chains. We note that the temperature needed to induce the coalescence of CNTs is ~2000 K. After breaking the CNT network, we sweep the voltage back to zero where we observe a sudden increase in current at a voltage ~ 50 – 80 % of the breakdown voltage. We can reliably switch the device multiple times between high and low resistive states. Each time we are able to heal the conductivity, in some cases up to ~50 % of its original value. During the reset to the low resistive state, thermal modeling indicates that the filament reaches temperatures of ~600 °C, the oxidation temperature of carbon. From this, we conclude that the carbon-oxygen interaction between the CNTs and SiO_2 are responsible for switching the device to a high resistive state.

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Driving Stage for SFQ Circuits using a Single Nanocryotron

Q. Zhao, A. N. McCaughan, A. E. Dane, K. K. Berggren, T. Ortlepp

Superconducting single-flux-quantum (SFQ) suffers from poor driving capability due to the very low impedance of Josephson junctions. Here, we report a driving stage for rapid single-flux-quantum (RSFQ) circuits using a single nanocryotron (nTron) that may provide new SFQ circuit solutions including compact, energy-efficient word-line drivers for superconducting memory. In this work, we present experimental results of a hybrid circuit, as shown in Figure 1a-1d, showing the translation of a single SFQ pulse to a high-amplitude nTron output pulse, equivalent to 1,000 Φ_0. The SFQ chip had a Josephson comparator that split the output pulse into two. One pulse went to a Suzuki stack for reference monitoring, while the other one fed into the gate of an nTron. The gate width was designed as 40 nm and the channel width as 80 nm (Figure 1d) to maximize the nTron sensitivity.

We measured the dependence of the nTron output on the input of the DC/SFQ converter at 4.2 K. A pulse (Figure 1e) was input to the DC/SFQ block to generate SFQ pulses at its rising edge. The nTron channel was biased at 9 µA, below its critical current of 12 µA. The nTron pulses (Figure 1f), which were 0.45 mV in amplitude and 10 ns wide on a 50 Ω load, were amplified for readout by commercial room-temperature RF amplifiers. When an SFQ pulse was created on the comparator by increasing the DC/SFQ input, we observed both an nTron pulse and a step from the reference Suzuki stack. As the DC/SFQ input increased linearly to generate additional SFQ pulses with a fixed period, the output pulses of nTron showed the same period.

This hybrid interface circuit has a foot-print of only 1 µm² for the sensitive area, is DC-powered, triggered by a single SFQ pulse, offers high output impedance as well as high gain and input isolation. Therefore, it is very attractive for advanced SFQ circuit designs and even enables new circuit solutions such as compact energy-efficient memory word line drivers for superconducting memories.
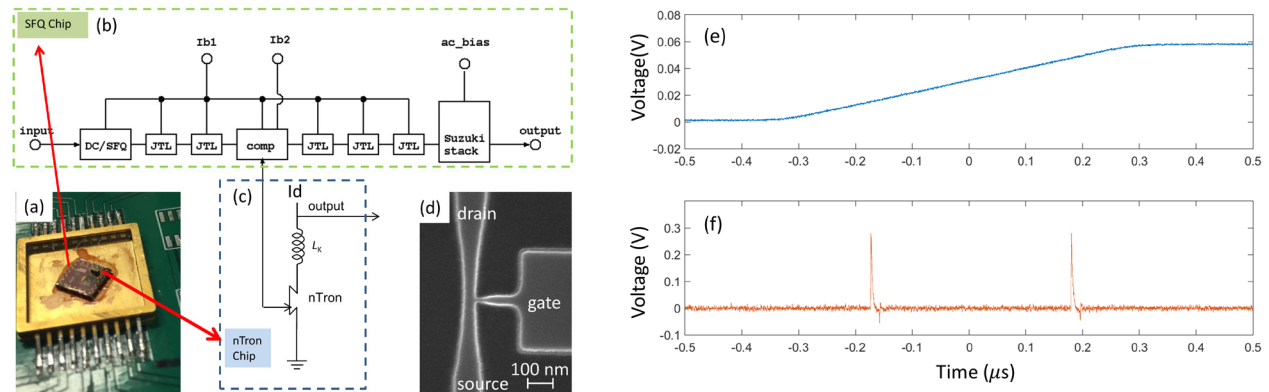
▲ Figure 1: Hybrid circuit using an nTron to read out SFQ pulses. (a) Test board of the hybrid circuit. The nTron chip (1 mm × 0.5 mm) is glued on top of the SFQ chip (5 mm × 5 mm). (b, c) Schematic diagrams for the SFQ chip and the nTron chip. The output SFQ pulses are from the comparator, which also output pulses to the Suzuki stack for monitoring the SFQ pulses. (d) SEM image of an nTron gate. The gate width is 20 nm. (e) Input pulses to the DC/SFQ. On the rising edge, the current pulse generates two SFQ pulses. (f) nTron output pulses. Each SFQ pulse generated on the rising edge of the DC/SFQ input is successfully read out by the nTron.

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Modeling Superconducting Nanowire Circuits

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Sponsorship: Air Force Office of Scientific Research, IARPA, iQuise, National Science Foundation, NASA

In this work, we have demonstrated SPICE (Simulation Program with Integrated Circuit Emphasis) models for superconducting nanowire single-photon detectors (SNSPDs) and superconducting nanowire cryotrons (nTrons). We have also designed several circuits which were simulated and optimized by using these models.

To simulate the electro-thermal dynamics of an SNSPD after it switched from superconducting state to resistive/normal state, as shown in Figure 1a, we calculated the velocity of the superconducting-normal boundary v_{NS} which varied over time and current. This calculation was then expressed into a circuit model (Figure 1b). For modeling an nTron which had three terminals (Figure 1c), as shown in Figure 1d, we took each of the three terminals as a superconducting nanowire which had an independent dynamic process based on its geometry and current. The switching conditions in which a gate pulse can trigger the channel were determined by experimental results.

Based on these SPICE models, we simulated several circuits using superconducting nanowires to improve the device performance. We will first show a pulse amplifier using an nTron to read output pulses from an SNSPD. A coupling network with an inductor shunted to ground was used to let the fast-rising edge of the SNSPD pulses trigger an nTron, while decoupling the two devices during the current recovery, to prevent the nanowires from latching. The signal-to-noise ratio of detection pulses was increased, suppressing timing jitter from voltage noise, because the SNSPD pulses were amplified. Additionally, the nTron amplifier worked as a buffer and isolated the SNSPD from the following processing circuits. Then, we extended the single-nTron amplifier to a differential amplifier using a pair of inversely biased nTrons. Thus, if two SNSPD pulses fed into the differential amplifier, the time interval between them could be detected through the pulse-width of the differential output. If the two SNSPD pulses were split from a single SNSPD with a modulated delay, the pulse-width of the differential output could be used as a time-tag to the detector. Thus, such circuits can be used in a time multiplexing SNSPD array for on-chip quantum optics.
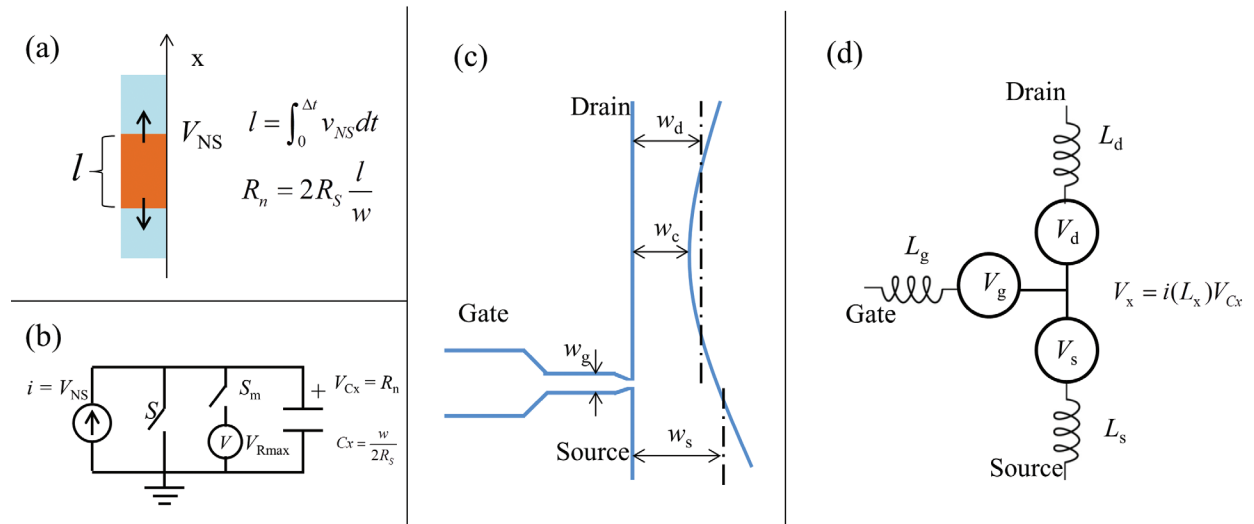
▲ Figure 1: SPICE modeling of an nTron. (a) Modeling the growth of a nanowire by tracing the superconducting-to-insulating boundary. (b) Equivalent circuit of a nanowire. (c) Geometry of an nTron. Each port of the nTron is simplified in a nanowire with uniform width. (d) Equivalent circuit of an nTron with three nanowires in different widths, inductance, and bias conditions.

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Magnetic Domain Wall Logic Devices

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We are working on building logic devices that encode information in a magnetic domain walls. A cartoon of the DW-Logic device is shown in Figure 1. Domain wall motion can operate at very low switching voltages, making magnetic logic a promising contender for more energy efficient computing.

Information is stored in a single transverse domain wall in a CoFeB wire, with magnetization fixed on the wire ends using IrMn antiferromagnetic pinning. The domain wall is translated by a current, and information is read out by a MgO magnetic tunnel junction (MTJ).

We are working on simulations of the device performance, which show that these logic devices have a complete set of Boolean operations and scale to switching energies and voltages below those of CMOS. Our integrated micromagnetics-SPICE model predicted switching energies in IMA devices down to 3×10^{-16} J using 0.1 mV V_{dd} and in PMA devices down to 3×10^{-18} J using 0.003 mV V_{dd}. We are also exploring the magnetic and electrical properties of device prototypes, shown in Figure 2.
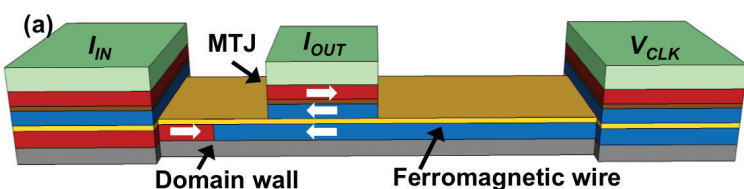
Figure 1: Cartoon of magnetic logic device.
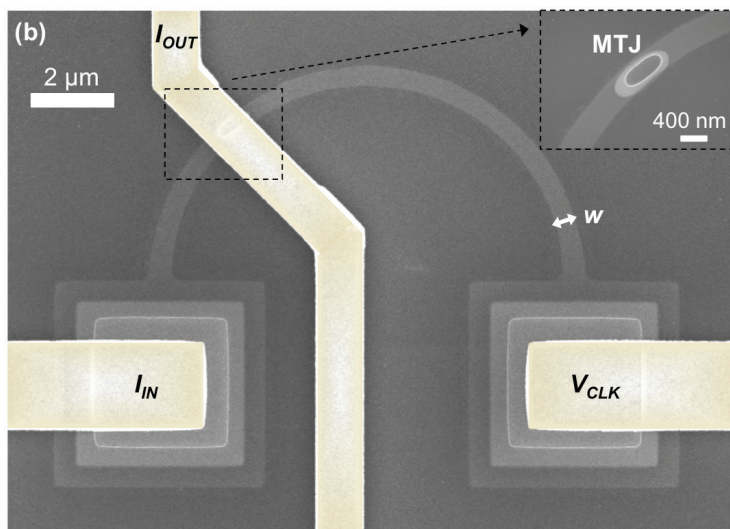
Figure 2: Scanning electron micrograph of a logic device prototype.

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Energy: Photovoltaics, Energy Harvesting, Energy Storage

15.7% Efficient 10-μm-Thick Crystalline Silicon Solar Cells

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Sponsorship : SunShot Initiative, Department of Energy

As the cost of crystalline silicon solar cell modules has steadily declined in recent years, the proportion of the module cost attributable to silicon has remained stubbornly high, accounting for 30% - 40% of the total. One promising approach to cutting the silicon cost component of solar modules is utilizing new manufacturing strategies such as epitaxial silicon growth on porous silicon or direct wafering to reduce the volume of silicon used in a photovoltaic cell. This strategy in particular has sparked a flurry of research addressing an impediment to the realization of ultrathin crystalline silicon cells: how to maintain competitively high efficiencies while shrinking the volume of silicon available to absorb incident photons. We overcome this challenge by incorporating a light-trapping nanostructure into an ultrathin silicon film, resulting in a substantial advance in short-circuit current and efficiency over previous efforts. We demonstrated experimentally that an inverted nanopyramid light-trapping scheme for a 10-μm-thick c-Si thin-film can achieve 15.7% energy conversion efficiency and 34.5 mA/cm² short-circuit current using a periodic inverted nano-pyramids structure. We have also demonstrated experimentally that even random texturing can lead to good light-trapping characteristics. To reach the high efficiencies necessary for a commercial product, we also constructed a multi-physics optimization tool incorporating both optical absorption and electronic carrier collection to understand in detail the loss mechanisms of the devices, including incomplete photonic absorption, contact recombination, surface recombination, and Schottky-Read-Hall and Auger recombination. Our model predicts that a 10-μm-thick thin-film c-Si solar cell can have an efficiency approaching 20% as the electronic properties are improved.

	Device A	Device B	Planar
Voc (mV)	589	593	555
Jsc (mA/cm²)	33.9	34.5	24.6
FillFactor (%)	78.5	75.2	76.8
Efficiency (%)	15.7	15.4	10.5
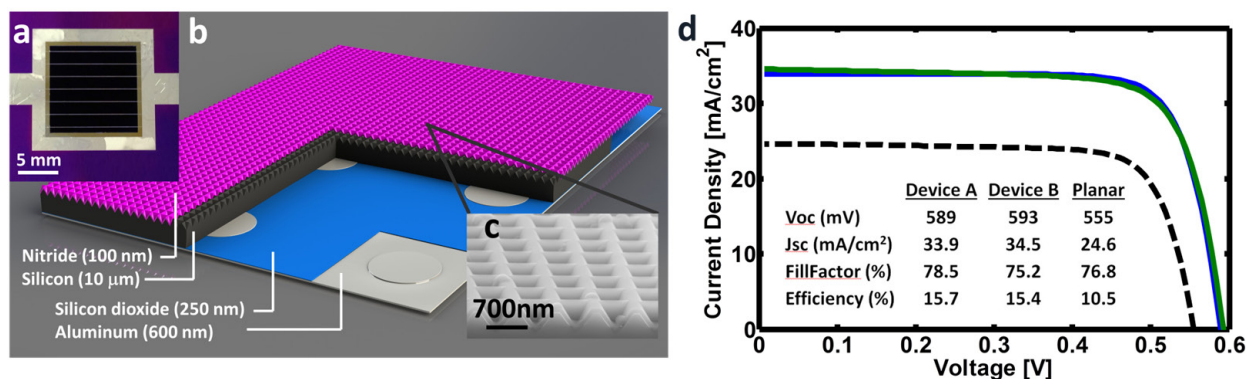
▲ Figure 1: 15.7% Efficient 10-μm-thick crystalline silicon solar cells using periodic nanostructures. (a) The top view of the solar device with an active area of 1cm x 1cm. (b) The schematic of structures. (c) Scanning electron microscope image of 700-nm-pitch inverted nano-pyramids light-trapping structure. (d) Performance (Current-voltage curves) of the solar devices and a planar (untextured) reference device.

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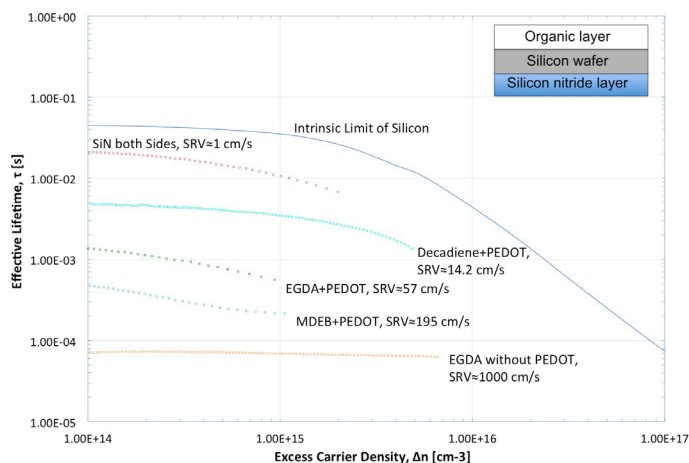
Surface Passivation of Silicon using Organic Molecules

M. L. Castillo, B. Reeja-Jayan, K. K. Gleason, T. Buonassisi
Sponsorship: EniPower

Many advanced silicon device architectures including photovoltaics and integrated circuits require excellent surface passivation. To combine the functionality of polymers with the robustness of silicon technology, we are exploring the direct passivation of silicon with organic molecules. Organic molecules offer a wide range of tunability in size and electronic dipoles and open up new materials for passivation beyond conventional inorganic dielectrics. We use initiated chemical vapor deposition (iCVD) and oxidative chemical vapor deposition (oCVD) to graft these organic molecules on <100> oriented p-type silicon wafers (B-doped, 80–120 ohm-cm, 750±25 μm thickness). We have observed surface recombination velocities (SRV) of minority carriers as low as 14.2 cm/s and minority carrier lifetimes as high as 4.8 ms, as shown in Figure 1.

We prepared the silicon wafer samples with a silicon nitride passivation layer on the back and an organic passivation layer on the front. In preparation for the silicon nitride passivation, samples went through a Radio Corporation of America (RCA) clean, which is a standard set of wafer-cleaning steps required immediately before any high-temperature process step, to remove organics, the native oxide, and any remaining extrinsic ions. Then, a 900-Å-thick layer of silicon nitride was deposited at a temperature of 400°C using an Applied Materials Centura 5300 Dielectric Chemical Vapor Deposition (DCVD) tool. After the silicon nitride passivation, we etched the samples in hydrofluoric acid for 2 minutes to remove the native oxide and obtain Si-H on the surface (the densified silicon nitride layer was minimally affected). The samples were then immediately transferred into the (iCVD) chamber (see the ethylene glycol diacetate (EGDA) passivation process in Figure 2 (a)). Finally, poly(3,4-ethylenedioxythiophene) (PEDOT) was deposited via oCVD in another chamber (see Figure 2 (b)). After the organic passivation process, minority-carrier lifetime was measured using a Sinton WCT-120 apparatus. The effective lifetime of various organic passivated layers measured using this tool is shown in Figure 1. Improvement of the quality of the surface passivation of silicon using organic molecules is critical to improving the efficiency of these devices. The combination of PEDOT and decadiene passivation on silicon has resulted in the best surface-passivation quality, as shown in Figure 1.

▲ Figure 1: Effective minority-carrier lifetime(s) of various organic surface passivation layers on silicon and corresponding surface recombination velocity (cm/s) of minority carriers.
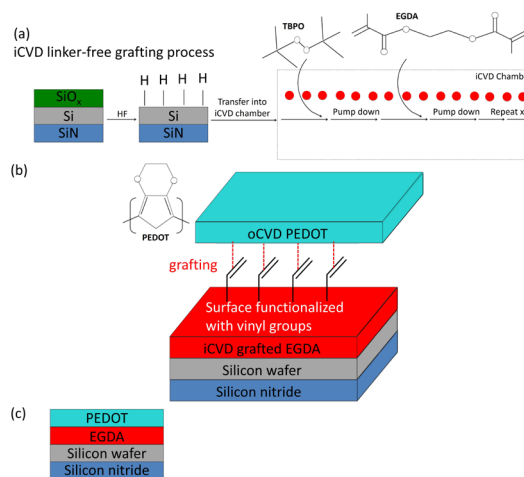
▲ Figure 2: PEDOT on EGDA surface passivation on silicon process via (a) iCVD linker-free grafting process in reactor (Yang, 2013) and (b) oCVD PEDOT layer grafts to vinyl bonds on iCVD grafted EGDA. (c) Example of final device after passivation.

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# Utilization of BaSnO₃ and Related Materials Systems for Transparent Conducting Electrodes

M. Campion, H. L. Tuller

Efficient transparent electrode materials are vital for applications in smart window, LED display, and solar cell technologies. These materials must possess a wide band gap for minimal optical absorption in the visible spectrum while maintaining a high electrical conductivity. Tin-doped indium oxide (ITO) has been the industry standard for transparent electrodes, but the use of the rare element indium has led to a search for better material alternatives. BaSnO₃ represents a promising alternative due to its high electron mobility and resistance to property degradation under oxidizing conditions, but the mechanisms by which processing conditions and defect chemistry affect the final material properties are not well understood.

This work seeks to better understand the relationships among processing, defect chemistry, and material properties of BaSnO₃, in order to better establish the consistent and controllable use of BaSnO₃ as a transparent electrode. To accomplish these goals, methods such as in situ resistance and impedance monitoring during annealing will be applied. In addition, a variety of novel methods such as the *in situ* monitoring of optical transmission (shown in Figure 1) during annealing and the *in situ* monitoring of resistance during physical vapor deposition will be utilized to investigate BaSnO₃. Direct measurements of the key constants for the thermodynamics and kinetics of oxidation in donor-doped BaSnO₃ will be experimentally determined for the first time. This increase in understanding will provide a predictive model for determining optical properties, carrier concentrations, and electron mobilities in BaSnO₃, which may be become increasingly important due to its high electron mobility, high temperature stability, and favorable crystal structure.
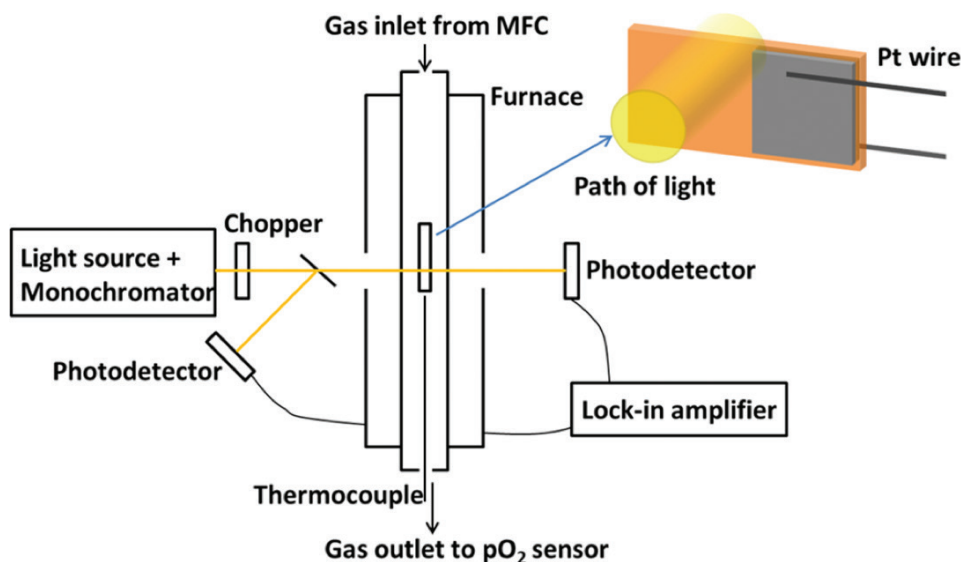
▲ Figure 1: Schematic of experimental setup to be used for simultaneous in situ measurement of the optical transmission and electrical conductivity of thin film BaSnO3 samples during annealing under controlled atmosphere and temperature.

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Ink-Jet Printing of Organic-Inorganic Halide Perovskites for Solar Photovoltaics

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Sponsorship: Eni

Remarkable optical and electronic properties, coupled with solution low temperature process-ability and environmental abundance of the precursor materials, have garnered increased attention to the hybrid organic-inorganic, metal halide perovskites as an attractive material alternative for solar photovoltaics.

Low internal losses and efficient carrier transport were demonstrated, and as a result high open-circuit voltages and solar power conversion efficiencies were realized. To achieve large-scale deployment, however, emerging thin-film technologies must achieve high efficiencies using high-throughput manufacturing techniques. Inkjet printing of hybrid organic-inorganic perovskites (e.g., $CH_3NH_3PbI_3$) offers a promising approach for low-cost, scalable manufacturing of future thin-film solar cells.

We are currently investigating the effect of the key printing parameters and precursor solution chemistries on the $CH_3NH_3PbI_3$ film formation, thickness, morphology and homogeneity as well as corresponding photovoltaic performances. Solution engineering allowed control over the evaporation rate and the surface tension gradient, therefore enabling fabrication of dense, continuous films with controlled morphology, as depicted by SEM (Figure 1). Preliminary devices exhibit V_{oc} of 0.86V, J_{sc} of 3.7-6 mA/cm2 and η of 3-5%. Further understanding of surface chemistry and wetting behavior are essential for fabrication of efficient photovoltaic devices.
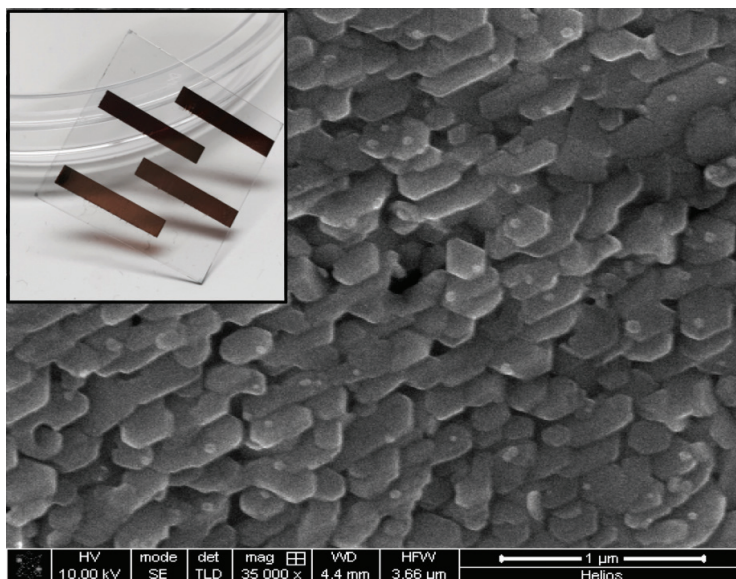
▲ Figure 1: SEM micrograph of ink-jet printed $CH_3NH_3PbI_3$ thin film. Inset: Photograph of the $CH_3NH_3PbI_3$ film on 1" glass substrate, demonstrating mask-less patterning approach.

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Open-Circuit Voltage Deficit, Radiative Sub-Bandgap States, and Prospects in Quantum Dot Solar Cells

C.-H. M. Chuang, A. Maurano, R. E. Brandt, G. Weon Hwang, J. Jean, T. Buonassisi, V. Bulović, M. G. Bawendi
Sponsorship: Samsung Advanced Institute of Technology

Quantum dot (QD) solar cell based on near-infrared active PbS QDs is an emerging technology that could fulfill the goal of efficient solar energy harvesting at low cost. In addition to the tunable bandgap covering the optimal bandgap ranges for solar cells, PbS QD solar cells can be fabricated with simple solution processes in air at room temperature and exhibit excellent air-stability for over 150 days. However, despite these advantages, the highest efficiency reported so far is still considerably lower than the expected performance for a material with this bandgap range. In this work, we present a comprehensive analysis of our recently developed air-stable PbS QD solar cells with a certified power conversion efficiencies of 8.6%. We elucidate the carrier recombination mechanisms and the origins of the large open-circuit voltage (V_{OC}) deficit, which is a primary limitation in present QD solar cells. In particular, we show evidence for the presence of radiative sub-bandgap states and the filling of these states in working devices under different operating conditions. We conclude that the performance and V_{OC} of current QD solar cells is mainly limited by these sub-bandgap states rather than the interfaces between QD and other materials. Based on these findings and perspectives on the recent progress of QD solar cells, we discuss future prospects for QD solar and suggest potential routes to improving these devices.
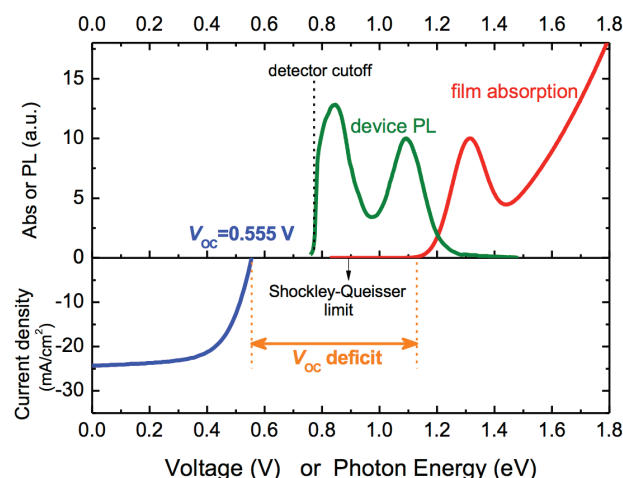
▲ Figure 1: Upper panel: absorption spectra and photoluminescence (PL) spectra of a PbS QD solar cell. Lower panel: J–V characteristics of the certified 8.6%-efficient QD solar cell. The device shows a peak of sub-bandgap emission and a large V_{OC} deficit.
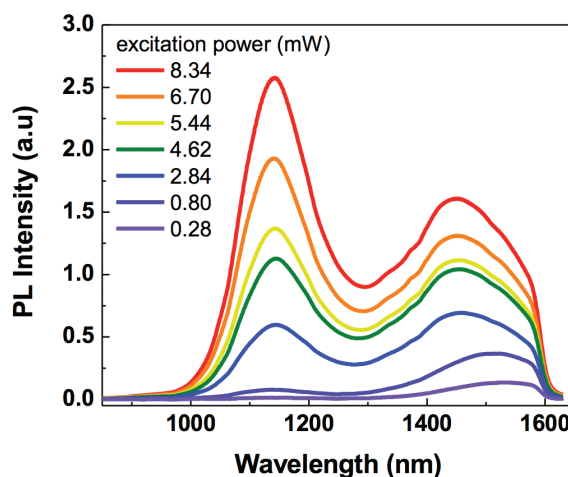
▲ Figure 2: Power-dependent PL spectra of a PbS QD solar cell. The relative intensity of the band-edge emission and sub-bandgap emission changes with excitation power. The progressive blueshift of the sub-bandgap emission is consistent with the sub-bandgap state-filling from deeper states.

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Control of the Fermi Level of Lead Sulfide Quantum Dots through Ligand Steric Interactions

P. R. Brown, V. Bulović

The electronic properties of lead sulfide colloidal quantum dots (PbS QDs) can be controlled through modification of the QD surface chemistry via ligand exchange, and recent work from our group has applied ultraviolet photoelectron spectroscopy (UPS) and density functional theory (DFT) to explain the influence of ligand-induced energy-level modification on record-efficiency QD photovoltaics. Control over the QD doping type and doping level is also an important factor in the design of efficient QD photovoltaics. Here, we show that by modifying the steric bulk of sulfur-containing ligands bound to the PbS QD surface, the Fermi level of the QD-ligand complex measured by UPS can be predictably tuned over a range of 0.6 eV within the QD bandgap. As shown in Figure 1, bulkier ligands result

in a Fermi level close to the QD conduction band (signifying n-type behavior), while smaller ligands result in a Fermi level close to the middle of the QD bandgap (signifying intrinsic behavior). This trend is expected given the ionic nature of lead sulfide: an excess of electron-rich lead atoms (realized here using bulky ligands with low relative sulfur content) should lead to n-type doping, while a balanced lead-sulfide ratio (realized here using small sulfide ligands that can effectively passivate the excess lead on the QD surface) should lead to intrinsic behavior. These results identify ligand steric interactions as an important contributor to the stoichiometry and electronic properties of PbS QDs, and as a broadly adjustable parameter in the design of efficient QD optoelectronic devices.
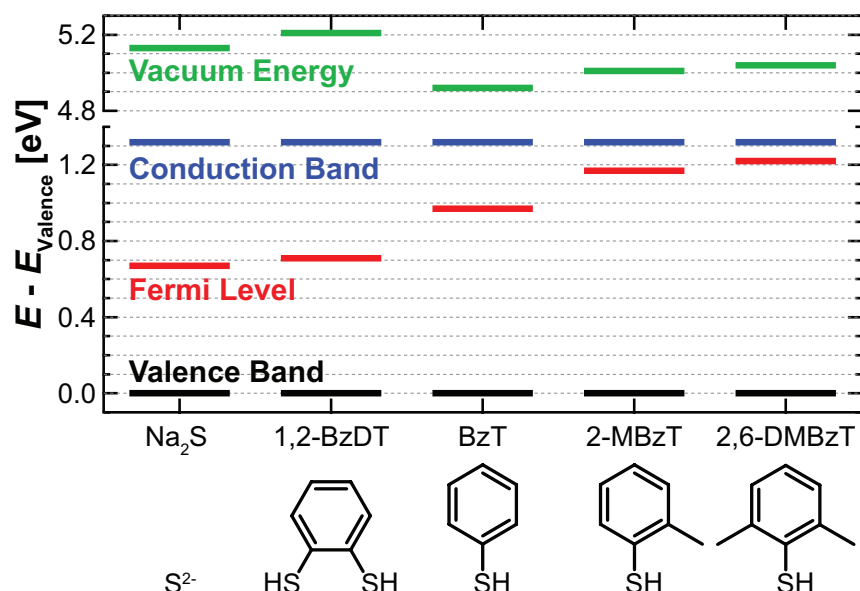
▲ Figure 1: Energy levels of lead sulfide colloidal quantum dots (excitonic absorption peak in solution of λ = 963 nm) derived from ultraviolet photoelectron spectroscopy and absorption spectroscopy, for five different chemical ligand treatments: sodium sulfide (Na_2S), 1,2-benzenedithiol (1,2-BzDT), benzenethiol (BzT), 2-methylbenzenethiol (2-MBzT), and 2,6-dimethylbenzenethiol (2,6-DMBzT). The chemical structures of the corresponding ligands are shown below the x-axis.

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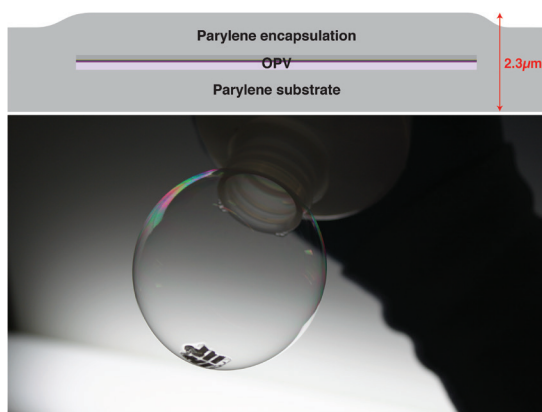
In Situ Vapor-Deposited Parylene Substrates for Ultra-Thin, Lightweight Organic Solar Cells

J. Jean, A. Wang, V. Bulović
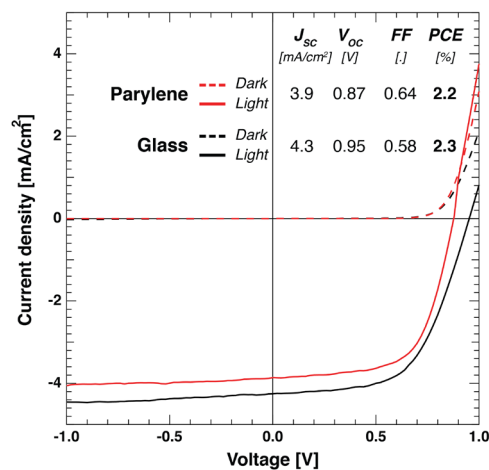Sponsorship: Eni-MIT Solar Frontiers Center

Solar photovoltaics (PV) are among the few low-carbon energy technologies with the scalability to satisfy global electricity demand. Today's leading silicon and thin-film PV modules are low-cost, efficient, and reliable, but also rigid and heavy (~30 kg for a 300 W module). Restricted module form factor limits potential PV applications and contributes to high non-module costs, which dominate total system cost and hinder deployment. Lightweight and flexible solar cells are possible with emerging thin-film technologies, but only if lightweight and flexible substrates are used. In this work, we introduce an alternative approach for producing thin, lightweight, clean, nanoscale-smooth, and flexible PV substrates and encapsulation layers: *in situ* vapor-phase deposition of transparent polymer membranes.

The most common substrate material today is glass: it presents a flat, smooth, robust surface for cell processing and protects sensitive organic and hybrid materials from exposure to oxygen and water vapor. However, a rigid glass sheet dominates cell weight and thickness. For example, typical organic, perovskite, and colloidal quantum dot solar cells are 600–900 nm thick and weigh 3–5 g/m². In contrast, a typical glass substrate or cover is 3 mm thick and weighs ~8 kg/m², dwarfing the mass of the active layers and constraining specific power for a given cell efficiency.

Here we demonstrate ultra-thin, lightweight, and flexible solar cells that are uniquely built by growing in situ thin polymer films as substrates and fabricating devices on top (Figure 1). For our polymer substrate we use chemical-vapor-deposited poly(chloro-p-xylylene) (parylene-C) films with thicknesses below 1 micron. The solar cells consist of vapor-deposited metal oxides, molecular organic films, and metal electrodes. Encapsulation with parylene-C is similarly performed under vacuum conditions. The entire cell can thus be fabricated without breaking vacuum. In-vacuum processing avoids exposure of substrate surfaces to atmospheric conditions, minimizing contamination and damage risk associated with transportation, handling, and cleaning of ultra-thin substrates. Organic PV cells on parylene exhibit power conversion efficiencies and device yields comparable to cells on glass substrates (Figure 2). These devices are the thinnest (<1 μm) and lightest (3.6 g/m²) solar cells yet demonstrated, with specific powers exceeding 6 W/g, and they illustrate the lower limits of PV substrate thickness and materials use. Solar cells on thin and flexible parylene membranes can be seamlessly adhered onto a variety of solid surfaces, providing for additive solar power on any surface.

▲ Figure 1: Molecular organic solar cells on 1-μm-thick parylene-C. Top: Device structure with thicknesses shown to scale. Bottom: Picture of parylene-based solar cells supported by a soap bubble, highlighting their low weight and conformability.

		J_{sc} [mA/cm²]	V_{oc} [V]	FF [.]	PCE [%]
Parylene	Dark				
	Light	3.9	0.87	0.64	**2.2**
Glass	Dark				
	Light	4.3	0.95	0.58	**2.3**

▲ Figure 2: Current–voltage characteristics in dark and under 100 mW cm⁻² solar illumination for organic solar cells on glass and on parylene substrates.

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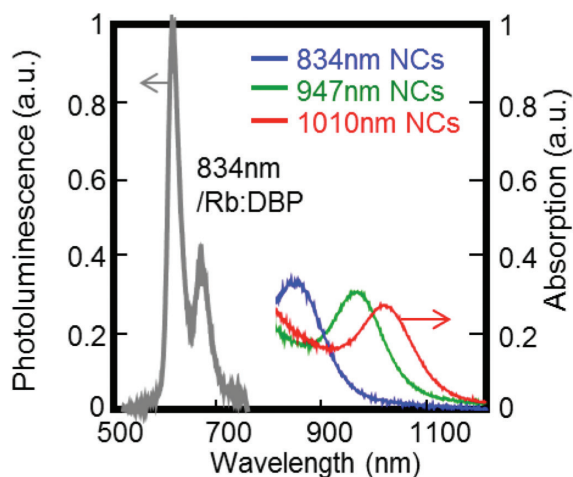
Solid State Triplet-Triplet Annihilation Upconversion

D. N. Congreve, M. Wu, Mark W. B. Wilson, J. Jean, N. Geva, M. Welborn, T. Van Voorhis, V. Bulović, M. G. Bawendi, M. A. Baldo

Despite decades of research, silicon photovoltaics have peaked at power efficiencies of approximately 25%. This loss is largely due to two unavoidable processes: the thermalization of high energy photons and the transmission of low energy photons. Here, we propose a cost effective, straightforward method for increasing photovoltaic power efficiencies past the Shockley Queisser limit. Upconversion is the process of turning two low energy photons into one high energy photon. When applied to silicon, upconversion can add substantial power gains without increasing the complexity of the solar cell. The upconverting layer can be applied to the back of the photovoltaic, capturing un-absorbed photons and returning them to the silicon cell as absorbable ones.

Here, we demonstrate upconversion using colloidal nanocrystals as the sensitizer and the organic material rubrene as the annihilator. The addition of 0.5% of a dopant dye allows for a 20-fold increase in the photoluminescence. The energetics of this process are illustrated in Figure 1. Light is absorbed by the nanocrystals at up to 1000 nm. The nanocrystals generate triplet states which transfer to the rubrene, where they undergo triplet-triplet annihilation to generate a singlet state and fluoresce; Figure 1, grey. The utilization of nanocrystals allows for further reach into the infrared as compared with current state of the art devices. Further, they minimize energy loss in the intersystem crossing process, allowing for a greater energetic difference between absorbed and emitted light. The successful application of upconversion to a silicon solar cell could increase efficiencies from 25% to over 30%.

▲ Figure 1: Energetics of upconversion. The light is absorbed by the nanocrystals (red, green, blue) and converted to triplet states, which transfer to the rubrene. They undergo triplet-triplet annihilation and then fluoresce from the emitter molecule, grey curve.
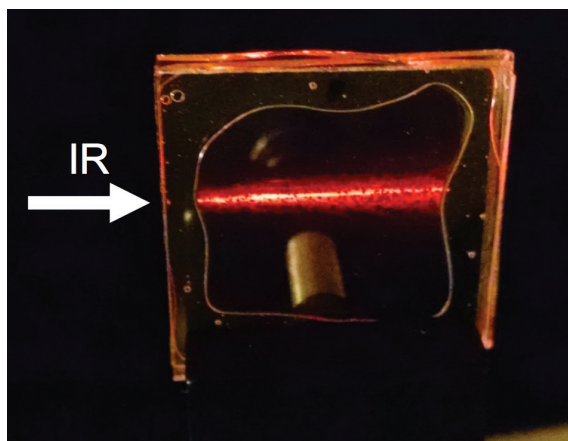
▲ Figure 2: Visible demonstration of upconversion. The sample is excited by an 808 nm laser beam from the left. Red fluorescence from the emitter is observed.

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Thin Film Evaporation from Nanopores and its Applications to Solar Thermal Devices

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Sponsorship: Masdar Institute/MIT Cooperative Program

The continuous growth of demands for energy and clean water, dwindling resources, and the environmental impact of the current techniques that dominate the world's energy market make the need for alternative, renewable sources as prominent as ever. Given solar energy's theoretical energy potential is 89,300 TW only a very small fraction of the available solar energy would be needed to provide our current needs.

In this work, we consider solar thermal energy where the key process is the conversion of light to heat to vapor. The produced vapor could be utilized for the production of electricity or distilled water, etc. Recently, it was shown that as much 80% of absorbed sunlight could be converted to water vapor by using absorptive nanoparticles dispersed in water. It was suggested that localized heating of the nanoparticles allowed the high efficiency conversion and prevented heat from being lost to the surroundings. We have expanded this idea of localized energy absorption and conversion to a concept that may have more practical relevance than a nanofluid. The surface of a nanoporous membrane is coated with a thin layer to absorb the sunlight. Liquid is wicked in via capillarity from the bottom of the membrane and forms a meniscus near the absorbing layer. As light is absorbed, heat is generated in the thin absorbing film near the liquid-vapor interface of the meniscus. Because the meniscus is in a nanopore, the conduction resistance from the pore wall through the liquid to the evaporating interface is small, and the efficient heat transfer of thin film evaporation can be utilized. As the input heat flux varies, the shape of the meniscus changes to increase or decrease the capillary pressure, providing passive pumping of the liquid. Furthermore, the membrane can be thermally insulating to prevent thermal losses to the liquid below.

To study device characteristics and gain a fundamental understanding of evaporation through nanoporous structures, we designed and fabricated a series of nanoporous membranes. Parameters such as pore diameter, porosity, and location of the meniscus within the pore can be varied. An experimental setup to test the evaporation from the membranes has been built (see Figure 1 for image of test fixture and SEM images of membranes), and suitability to different solar thermal devices is considered. We believe this study will provide understanding of solar-driven evaporation with highly localized heating, as well as a fundamental understanding of how parameters such as pore size and location of the meniscus affect evaporation from nanopores, some initial results of which are shown in Figure 2. During tests the input power, evaporation rate, surface temperature, and other parameters are monitored.
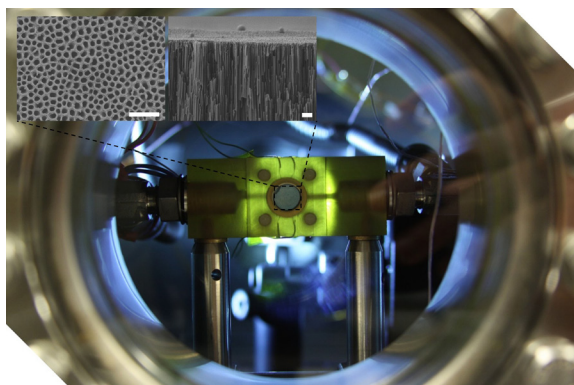
▲ Figure 1: Test fixture seen from a viewport in the experimental vacuum chamber. Insets show SEM images of the anodic aluminum oxide membranes used for evaporation tests. Scale bars: 1μm
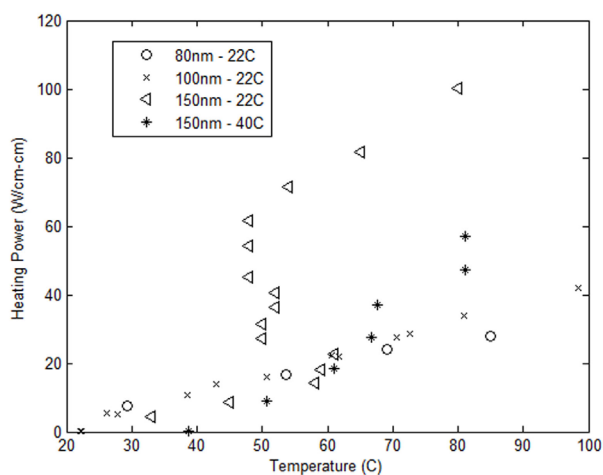
▲ Figure 2: Surface temperature vs. heating power for samples of different pore diameter and different chamber ambient temperatures.

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MEMS Energy Harvesting from Low-Frequency and Low-G Vibrations

R. Xu, S.G. Kim
Sponsorship: MIT-SUTD International Design Center

MEMS-scale vibration energy harvesting has been investigated for more than a decade to enable autonomous systems such as batteryless wireless sensor networks. Toward this goal, a fully assembled energy harvester at a size of a quarter dollar coin should be able to generate robustly about 100 mW continuous power from ambient vibration (mostly less than 100Hz and 0.5g acceleration) with reasonably wide bandwidth (>20%). We are inching close toward this goal in terms of power density and bandwidth, but not in terms of low frequency operations.

Most of the reported vibration energy harvesters use a linear cantilever resonator structure to amplify small ambient vibration. While such structures are easy to model, design and build, they typically have a narrow bandwidth. In contrast, nonlinear resonators have different dynamic response and greatly increase the bandwidth by hardening or softening the resonance characteristic of the beam structure. In addition, it has been found that non-linear resonating stretching beams can extract more electrical energy than linear resonating bending beams can. Our previous research with non-linear resonating stretching energy harvesters achieved 2.0 mW/mm³ power density with >20% power bandwidth. But it was operated with input vibrations of >1 KHz and 4.0 g acceleration, which practically limits the use of this technology, harvesting energy from real environmentally available vibrations. Many believed this is an inherent limitation imposed on the MEMS scale structures.

We approached this problem with a bi-stable nonlinear resonating buckled beam. Compared to mono-stable nonlinear resonance, we found bi-stable resonance could bring more dynamics phenomena to help reduce the operating frequency as well as the g-requirement. Electromechanical lumped model has been built for simulating the dynamics of buckled clamped-clamped beam structure. The two oscillation modes, intra- well and inter-well with respect to the double energy well potential of the bi-stable system, have been predicted. We also found the characteristic spring softening and spring stiffening responses, which were associated with the small-amplitude intra-well and large-amplitude inter-well oscillations respectively. In order to validate the simulated models, a meso-scale prototype has been built and tested on an electromagnetic shaker with controlled and monitored input vibration frequency and amplitude. The testing results verify the theoretical predictions, showing a shifted response of bi-stable configuration, which generates more power than the mono-stable configuration at lower frequencies (Figure 1). Hysteresis also exists when varying the vibration amplitude at fixed frequency, so that at low g input, the bi-stable energy harvesters still generate a significant amount of power (Figure 2). The buckled bi-stable beam structure is believed to solve the last challenge of the MEMS energy harvester at low frequency and low-g input vibrations. The MEMS device will be fabricated soon.
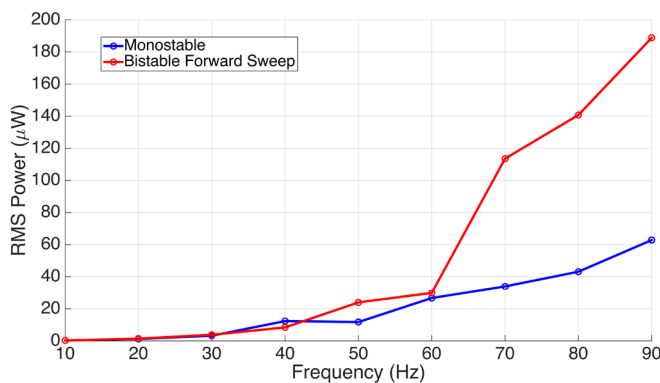
▲ Figure 1: Power frequency responses of mono-stable and bi-stable configurations of the same setup at 3g excitation.
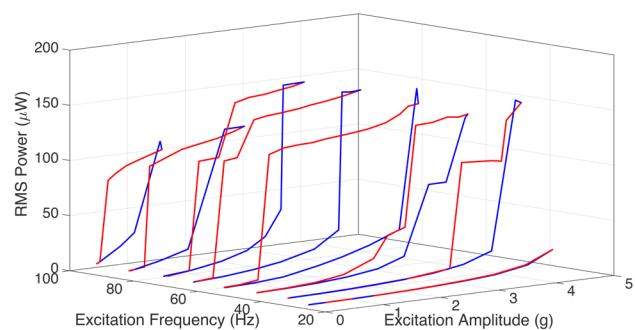
▲ Figure 2: The input acceleration amplitude was swept forward (blue) and backward (red) at fixed frequencies from 30Hz to 100Hz for the same bi-stable system.

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Fabrication of Ruthenium Oxide-Coated Si Nanowire-Based Supercapacitors

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Sponsorship: Singapore-MIT Alliance for Research and Technology

Supercapacitors are electrochemical devices that have high power density and long cycle life. Pseudo-capacitors are a type of supercapacitor that involves reversible surface reduction/oxidiation reactions. Among all the pseudo-capacitive materials, ruthenium oxide is the most promising due to its high specific capacitance, excellent cyclability, and high conductivity. While researchers have been developing supercapacitors based on ruthenium oxide or its composite with other materials such as CNT, there has been little study on ruthenium oxide-Si composite. In earlier work, we demonstrated the feasibility of using metal-assisted chemical etching (MACE) to fabricate Si nanowires for on-chip MOS capacitors. Here we continue using an ordered vertical array of Si nanowires from MACE to fabricate on-chip supercapacitors.

Atomic layer deposition (ALD) is used to deposit ruthenium oxide on silicon nanowires due to its conformal coating on high aspect ratio structures. Moreover, it also provides a precise control of the ruthenium oxide film thickness. As pseudo-capacitive reactions occur at the surface of ruthenium oxide, the high aspect ratio Si nanowire structure coated with ruthenium oxide has a highly accessible ruthenium oxide surface area and thus leads to a high energy storage capacitance. We have developed an ALD process for conformal coating of ruthenium oxide on silicon nanowires generated by MACE. The composite structure shows a coating of well-distributed particles (Figure 1). High-resolution transmission electron microscopy (HRTEM) characterization confirmed that these particles match the lattice of ruthenium oxide. We are currently investigating the electrochemical performance of this composite material using a three-electrode set up. Meanwhile, we are optimizing the ALD process according to the measured electrochemical performance. Our ultimate goal is to fabricate a solid state micro on-chip supercapacitor based on the optimized electrode material (Figure 2).
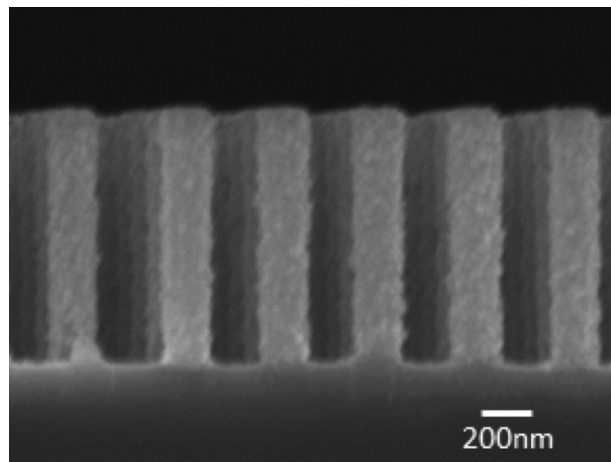
▲ Figure 1: SEM image of an array of Si pillars after ALD of ruthenium oxide.
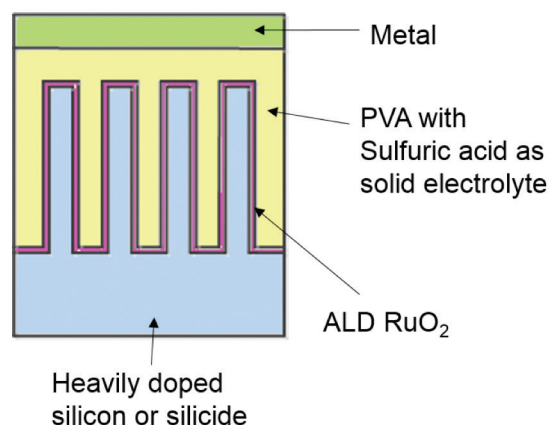
▲ Figure 2: Schematic of the solid state micro on-chip supercapacitor.

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# Materials and Structures for Lithium-Air Batteries

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Sponsorship: Bosch, Skoltech Center for Electrochemical Energy Storage

Lithium-air batteries hold promise for the next generation of electric vehicles and other applications. By reacting oxygen directly with lithium ions to form Li_2O_2 on discharge, they can achieve energy densities 3-5 times higher than current lithium-ion batteries. However, a number of challenges exist for implementing lithium-air batteries, including poor rate capability, poor cyclability, high overpotentials upon charging, and electrode and electrolyte instability. We seek to address these issues by developing new electrode materials and architectures and performing studies of Li_2O_2 formation under various discharge conditions.

Aligned arrays of carbon nanotubes (CNTs) provide ideal conductive scaffolding materials for Li_2O_2 while occupying a small volume fraction and having low mass. CNTs of 5-10 nm in diameter are grown in aligned forests on a catalyst-deposited silicon wafer and delaminated. These free-standing carpets can be placed directly into our cell. We observed nearly ideal gravimetric capacities and high volumetric capacities. However, carbon has been found to decompose in lithium-air cells and promote electrolyte decomposition. These side reactions lead to poor cycling performance and high overpotentials on charge. In order to avoid these effects, we have worked on depositing coating materials such as TiN onto CNTs to chemically passivate the carbon surface (see Figure1). We are able to completely coat the CNTs and are currently working on optimizing conductivity and testing electrochemical performance.

The rate capability of Li-air battery with CNTs cathode is still not satisfying. The current understanding of the mechanism is that Li_2O_2 forms different morphologies at different rates. As an insulator material, Li_2O_2 forms a uniform coating on CNTs at a high rate and passivates the electron transport, leading to a limited capacity. At a low rate, Li_2O_2 forms toroidal particles and results in a much larger capacity. To further understand the discharge product nucleation and growth mechanism and to exploit the full potential of Li-air battery application, we pre-nucleate particles at a low rate and then discharge them at a high rate to try to optimize capacity and void-filling and learn about nucleation and growth mechanisms (see Figure 2).
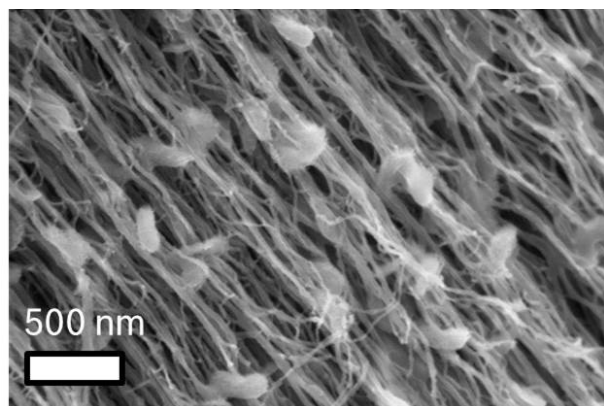
▲ Figure 1: SEM micrograph of toroidal Li_2O_2 formation on CNTs deposited with a coating of TiN.
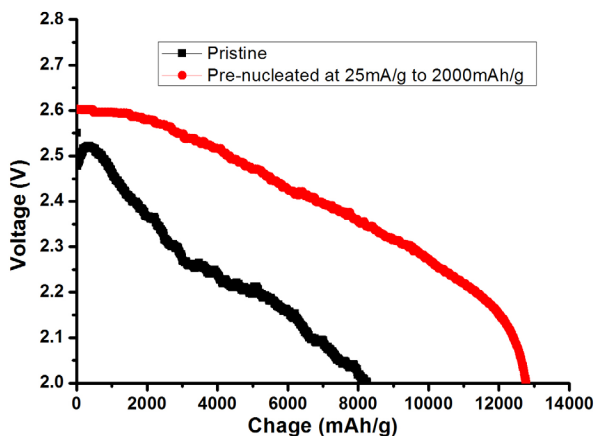
▲ Figure 2: Discharge diagram at 500mA/g of pristine CNTs and CNTs pre-nucleated at 25mA/g to 2000mAh/g.

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Mechanical Stresses in Germanium Thin Film Microbattery Electrodes during Cycling

A. Al-Obeidi, D. Kramer, R. Moenig, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology

A critical component for autonomous microsystems is a reliable energy storage system that can be integrated with on-board energy harvesting and power management systems. One possible energy storage system to meet this demand is lithium-ion thin film microbatteries, which offer high energy storage capacities. For the anode, silicon and germanium offer capacities as high as 3579 A h kg^{-1} and 1384 A h kg^{-1} compared to graphite's theoretical capacity of only 372 A h kg^{-1}. However, use of these materials has been limited by the significant volumetric and structural changes that occur during cycling. In order to explore the relationship between electrochemistry and the mechanical stresses that arise, *in situ* stress measurements on thin film electrodes were conducted.

It was found that the stresses developed in 90 nm thick germanium films were lower than in silicon by roughly one-third (Figure 1) and showed better capacity retention at higher rates. Cycling thicker 170 nm films initially showed similar stress behavior to that of the thinner 90 nm films but showed a significant drop in stress magnitude with cycling. Imaging these cycled films showed that the initially continuous thin film had evolved toward a complex, three-dimensional island structure, which had lower stress (Figure 2). The reduced plastic flow stresses observed in lithium-germanium and the weak dependence on charge-discharge rates correlate with the improved cyclability and reduced rate sensitivity found in germanium electrodes as compared to silicon.
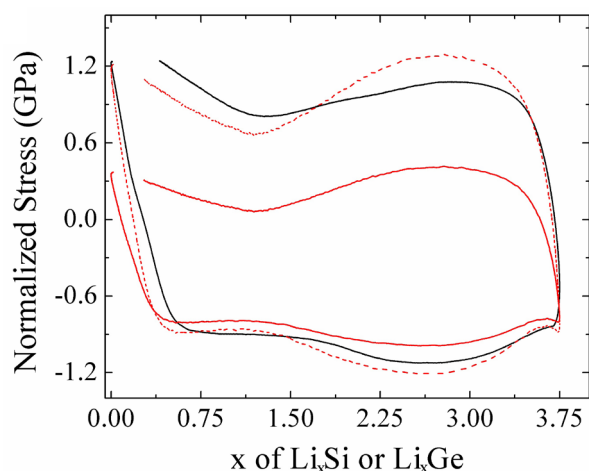
▲ Figure 1: Evolution of stress as a function of anode capacity for silicon and germanium.
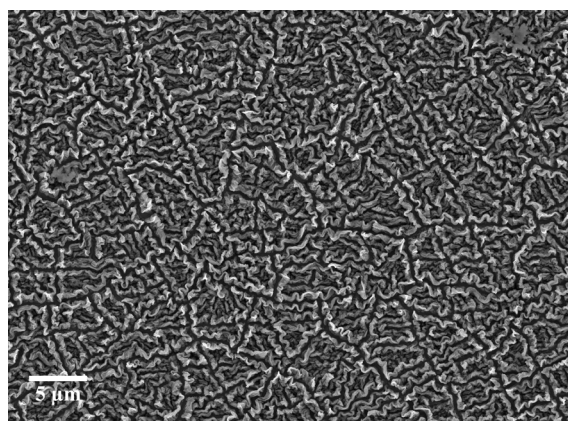
▲ Figure 2: Low magnification SEM image of an extensively cycled 170 nm germanium film.

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Oxygen Exchange Kinetics in Pr_2CuO_4 Thin Film Cathodes: The Role of Doping and Orientation

K. Mukherjee, H. L. Tuller (in collaboration with Y. Hayamizu, S. Istomin)
Sponsor: Skolkovo Foundation

Layered oxide compounds with mixed ionic electronic conductivity are promising candidate materials for cathodes in intermediate-temperature solid oxide fuel cells. There have been reports of anisotropic oxygen ion conductivity in materials with the K_2NiF_4 (T) and Nd_2CuO_4 (T') crystal structures, with facile transport along the rock-salt layers. These material systems also exhibit anisotropic thermal and chemical expansion properties, potentially important for long-term device stability. However, in practice, it is difficult to control the crystal structure, doping and grain orientation independent of each other to understand their effect on cathode performance. Additionally, the lanthanide cuprates exhibit a third phase (T*), a hybrid of the T and T' phases with important implications for the ionic and electronic conductivity.

In this work, we synthesized thin films of Pr_2CuO_4 with varying amounts of Sr and Ce doping using pulsed-laser deposition on single crystal YSZ substrates. Alloys with the same crystal structure and doping but with different film orientations were also successfully synthesized through the use of seed layers on YSZ. Using electrochemical impedance spectroscopy to measure the area-specific resistance, we find a significant improvement in the oxygen surface-exchange rate as a result of both donor and acceptor doping. However, the activation energies are very different, indicative of different rate-determining steps in each case.

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Development of Reversible Solid Oxide Cells: A Search for New Electrode Materials

C. S. Kim, S. R. Bishop, H. L. Tuller
Sponsorship: Skolkovo Foundation

Recent advances in photovoltaic cells have enabled efficient conversion of solar energy to electricity at low cost. However, solar radiation is intermittent, and an efficient means for storage of excess electricity generated during daytime is needed. Electrolysis cells can convert excess electrical energy into chemical fuels via the electrolysis of water (H_2O) or carbon dioxide (CO_2) to hydrogen (H_2) or carbon monoxide (CO), respectively, with the excess stored energy converted back to electricity efficiently by solid oxide fuel cells (SOFCs). A reversible SOFC can operate as an electrolysis cell (Figure 1) during the day and as a fuel cell (Figure 2) at night. While symmetric solid oxide cells with redox stable electrodes have been investigated, their performance is substantially lower than the state-of-the-art SOFCs. In this project, we are investigating new redox stable electrode materials with high mixed (electrical and ionic) conductivity under both highly oxidizing and reducing conditions.

The defect structure and transport properties of new candidate electrode materials are investigated by thermogravimetry, electrical conductivity, and dilatometry as functions of temperature and oxygen partial pressure. Surface kinetics are examined by means of ac impedance spectroscopy of half-cells and symmetric cells fabricated by depositing electrode materials onto electrolytes by pulsed laser deposition. Electrode performance is being correlated with defect and transport models developed on the basis of the collected thermodynamic and kinetic experimental data.
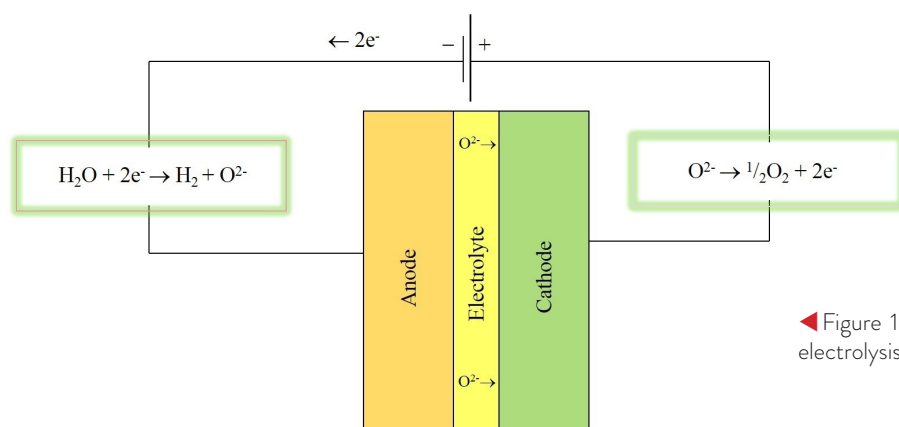
◀ Figure 1: A reaction diagram of a solid oxide electrolysis cell.

$$H_2O + 2e^- \rightarrow H_2 + O^{2-}$$

$$O^{2-} \rightarrow {}^{1}/_{2}O_2 + 2e^-$$
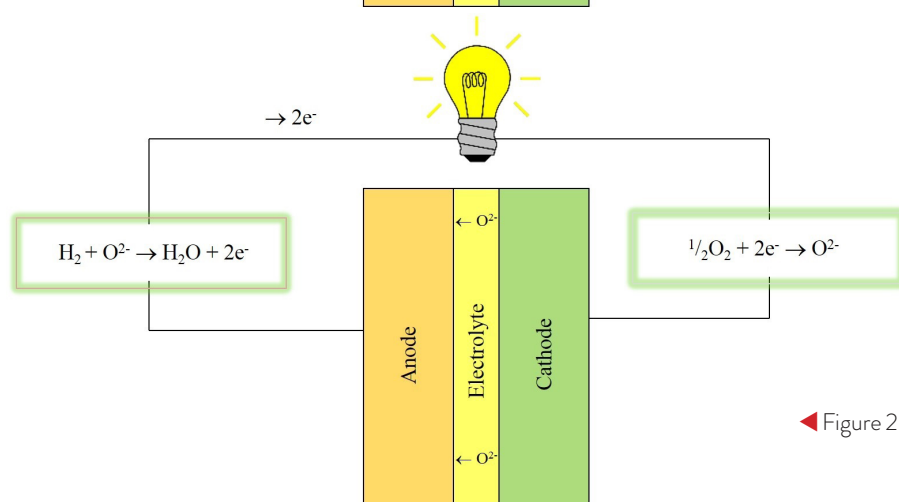
◀ Figure 2: A reaction diagram of an SOFC.

$$H_2 + O^{2-} \rightarrow H_2O + 2e^-$$

$$^{1}/_{2}O_2 + 2e^- \rightarrow O^{2-}$$

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Investigation of Fuel Cell Cathode Performance in Solid Oxide Fuel Cells: Application of Model Thin Film Structures

J. J. Kim, D. Chen, N. Perry, S. R. Bishop, H. L. Tuller
Sponsorship: Department of Energy

An improved fundamental understanding of oxygen nonstoichiometry (δ) and surface exchange kinetics in solid oxide fuel cell (SOFC) cathodes is considered to be critical for achieving enhanced device performance and longevity, especially at reduced operating temperatures. Although numerous research activities have been focused on elucidating the oxygen reduction reaction (ORR) mechanisms at the cathode, their conclusions remain unsatisfactory and controversial. The ORR at mixed conducting oxide thin film cathodes consists of oxygen adsorption, dissociation, charge-transfer, incorporation, and migration of charge carriers. The kinetic parameters associated with the overall ORR, such as the diffusion coefficient (D) and surface exchange coefficient (k), are strongly influenced by δ in the oxides. On the other hand, oxygen defect generation is often associated with valency changes in the transition metal or rare earth ions within the oxides and with corresponding changes in lattice constant (chemical expansion). This expansion may lead to stresses sufficient to support crack initiation and/or delamination, impacting the device's long-term stability. Because many advanced oxide materials used in SOFC experience significant changes in δ during operation at elevated temperatures and under reducing/oxidizing conditions, the ability to diagnose a material's behavior *in situ* is therefore important.

Our group recently demonstrated that δ in $Pr_{0.1}Ce_{0.9}O_{2-\delta}$ (10 PCO) thin films could be reliably derived by utilizing chemical capacitance extracted from electrochemical impedance spectroscopy (EIS) measurements. Furthermore, we have introduced a non-contact optical means for *in situ* recording of transient redox kinetics, as well as the equilibrium Pr oxidation state and, in turn, δ in 10 PCO thin films, by monitoring the change in absorption spectra upon change in pO_2 or temperature. In this study, we are investigating cathode kinetics and nonstoichiometry of two model oxide thin films, $Sr(Ti,Fe)O_{3-\delta}$ (STF) with Ba or La doping and $(Pr,Ce)O_{2-\delta}$ (PCO), by simultaneously utilizing in situ and in operando optical absorption spectroscopy and EIS as a function of temperature, pO_2, and electrical potential. We are also investigating changes in surface chemistry and their impact on electrode impedance by atomic force microscopy (AFM), x-ray photoelectron spectroscopy (XPS), and low-energy ion-scattering spectroscopy (LEIS).

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Fundamental Studies of Oxygen Exchange and Associated Expansion in Solid Oxide Fuel Cell Cathodes

N. H. Perry, J. J. Kim, D. Marrocchelli, S. R. Bishop, H. L. Tuller (in collaboration with B. Yildiz, D. Pergolesi)
Sponsorship: Department of Energy

In order to lower the cost of solid oxide fuel cells (SOFCs), both the low-temperature efficiency and long-term durability need to be improved. Two key areas involving fundamental studies of how fuel cell materials "breathe" oxygen under operating conditions that we are examining are 1) the origin of sluggish oxygen incorporation at the cathode, which often dominates SOFC efficiency losses at low temperatures, and 2) the origin of chemical expansion during oxygen loss from the oxide, which can result in catastrophic mechanical failure of the cell in addition to electro-chemo-mechanical coupling effects. Our recent review article (*Annu. Rev. Mater. Res.*, 44, 2014) highlights the widespread presence of chemical expansion and its consequences across a number of energy conversion and storage devices.

In this work we experimentally and theoretically investigate cathode systems with model geometries (controlled active surface area and diffusion lengths of thin films) and model chemistries (tailored electronic structure, crystal structure, and defect chemistry) to isolate underlying factors controlling the oxygen exchange and expansion behavior. Previous work on fluorite-structured electrodes is being extended to the perovskite families $(Sr,Ba,Ca,La)(Ti,Fe,Co)O_{3-\delta}$ and $(La,Sr)(Ga,Ni)O_{3-\delta}$, using advanced *in situ* X-ray diffraction, optical absorption, thermogravimetric analysis, dilatometry, and electrochemical impedance spectroscopy techniques, defect thermodynamic modeling, and density functional theory calculations. Using this approach we have experimentally confirmed our previous theoretical calculations demonstrating the important role of charge localization in controlling chemical expansion behavior. We have also identified other key factors, such as temperature, crystal symmetry, and oxygen vacancy radii, which impact chemical expansion in perovskites. In related studies, we have demonstrated how chemical substitution affects defect chemistry, electronic structure, and corresponding oxygen exchange rate at the cathode surface. Such information is key to the design of both efficient and durable fuel cell electrodes.

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Photonics, Optoelectronics

Design Method for Optical Phased Arrays that Emit 3D Holograms

J. Zhou, J. Sun, A. Yaacobi, C. V. Poulton, M. R. Watts
Sponsorship: Draper Laboratory

Optical phased arrays have garnered a great deal of research attention due to their potential in communications, imaging, and detection. Recent development in the field has shown optical phased arrays can emit 2D patterns and continuously steer in one dimension. Currently, in microwave phased antenna arrays, high resolution is achieved at the expense of size, power, and cost. These drawbacks can be resolved by moving into the optical domain since it maintains high resolution due to a large array size coupled with small optical wavelength. The next step beyond 1D and 2D work is finding a way to extend these optical arrays to be able to tackle issues requiring 3D imaging. The previous 2D emitting phased arrays have produced outputs in the far field, which allows for only a single plane of focus, limiting it to 2D. The near field, on the other hand, allows for multiple patterns to come into focus at different projection distances, creating the framework for generating a 3D hologram. Digital holography techniques can be used to design phased arrays that generate 3D holograms, expanding their potential. In the past, digital binary holograms have been synthesized by superimposing Fourier transforms of output image planes. In the biomedical field, digital 3D holography has shown the ability to detect more information than traditional radiographs and CT images. Digital holography also opens the possibility for 3D displays and TVs without requiring specialized glasses.

This work presents a design technique that attempts to combine the 2D emitting phased array concept with digital holography to generate phased arrays with the capability to emit arbitrary 3D patterns in the near field. The phased array generation is accomplished by back-propagating desired output planes by using Fresnel diffraction to achieve a single electric field realizable by a phased array (Figure 1). This phased array will then tune its individual antennas to amplitudes and phases to match the previously calculated electric field so that it emits the desired 3D pattern when forward-propagated.

Additional techniques are applied to improve the output quality of the image by adding both a random and curved phase front to the output planes prior to back-propagation (Figure 2). This technique provides a method to tune phased arrays that are capable of generating near field 3D holograms.
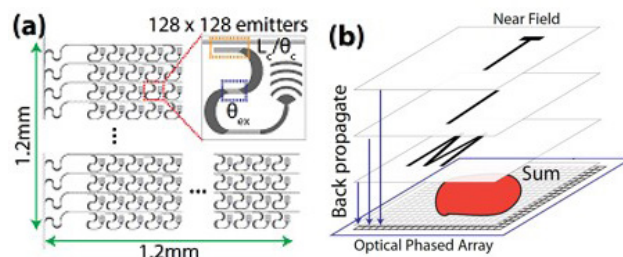
▲ Figure 1: (a) System overview of synthesized and simulated phased array. (b) Concept of 3D hologram design technique by back-propagation of MIT logo.
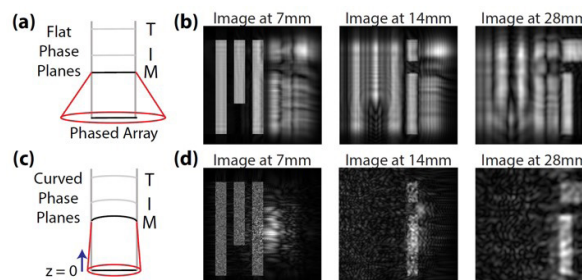
▲ Figure 2: (a) Back-propagated uniform flat phase front field. (b) Output of the phased array emitting "MIT" using back-propagation of the flat phase front. (c) Addition of circular phase front to back-propagate more accurately to the phased array area. (d) Improved output due to the addition of random and circular phase fronts prior to back-propagation.
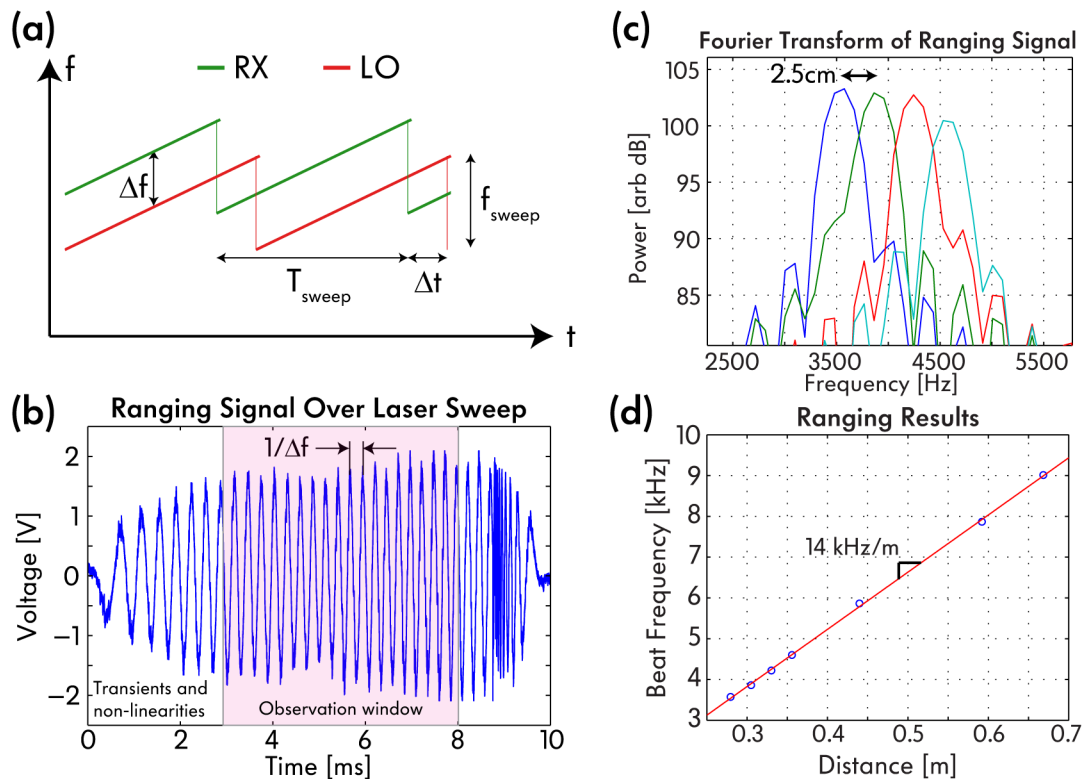
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Integrated LIDAR System Based on Frequency-Modulated Continuous-Wave Detection

C. V. Poulton, D. B. Cole, M. R. Watts
Sponsorship: DARPA MTO

Light detection and ranging (LIDAR) systems have proven useful in autonomous vehicle, urban mapping, and military applications. However, these systems have traditionally been bulky and expensive, along with utilizing mechanical steering, which is not robust in harsh environments. At the moment, high-performance LIDAR systems cost on the order of \$1,000 to \$10,000, which limits its practical applications. Integrated photonics promises a viable path to reduce the cost and form factor of LIDAR systems. The use of standard 300 mm CMOS foundries can reduce the cost of individual chips to under \$10, making LIDAR systems commercially viable for a range of applications. Traditionally, LIDAR systems utilize a time-of-flight measurement technique that requires pulsed lasers with large peak powers, which is difficult to realize in an integrated system.

In this work, we utilize a range detection method based on coherent detection that involves modulating the frequency of a continuous-wave laser (FMCW) and can utilize photodetectors with moderate dark currents. Our recent results have shown ranging measurements with the FMCW method in an integrated optical system consisting of a single-sideband modulator and photodetectors. Edge-coupled waveguides with external collimating optics are used as transmitter and receiver ports. A compact laser diode with modulated injection current for frequency modulation is utilized as an optical input. A distance measurement of 4 m with a range resolution of 2.5 cm is achieved. The addition of large-aperture optical phased arrays will allow for no external optics and beam steering.

▲ Figure 1: (a) Operation of ranging with FMCW; (b) Example ranging signal; (c) Fourier transform of ranging signals showing 2.5 cm resolution; (d) Ranging results showing expected linear fit.

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Fast Stochastic Simulation of Silicon Photonic Devices with Non-Gaussian Correlated Process Variations

T. W. Weng, Z. Zhang, Z. Su, L. Daniel
Sponsorship: National Science Foundation

Silicon photonics has attracted much attention in recent years thanks to its ability to achieve higher bandwidth, its lower power dissipation compared to electrical interconnects, and its compatibility and easy integration with CMOS process. However, because of the high contrast of the refractive index between silicon and silica, silicon-based optical devices are very sensitive to manufacturing process variations; for example, the geometric variations in silicon width and thickness can result in a fluctuation of the effective phase index, leading not only to degraded performance in devices such as directional couplers and ring resonators but also to serious failures at the system level.

Despite some results for nanometer integrated circuits (IC), there is still a lack of efficient uncertainty quantification techniques for silicon photonics. Monte Carlo (MC) has been the mainstream statistical simulation technique in commercial design software. However, it suffers from a slow convergence rate and long simulation time. Recently, fast stochastic spectral methods have been developed based on generalized polynomial chaos expansions to efficiently approximate a stochastic solution. However, one of the major assumptions in the existing publications is that the input parameters describing the process variations are mutually independent, which is not always necessarily true. Therefore, our goal is to quantify the effects of silicon photonic process variations using a non-intrusive polynomial chaos scheme called stochastic collocation (SC). A directional coupler in Figure 1 is used as an example to show the technique works. In practical fabrications, due to tolerances of the fabrication process, the fabricated waveguide width and the gap between two waveguides of a directional coupler are different from chip to chip and wafer to wafer, and the exterior and interior waveguide sidewall positions are assumed to be correlated random parameters. The simulated power coupling coefficients are shown in Figure 2. It is clearly seen that the probability density function of the power coupling coefficients obtained by 10000 samples MC and 81 quadrature points SC are in good agreement; however, the simulation time of SC is far less than MC, which is around 55 times speed-up in this example.
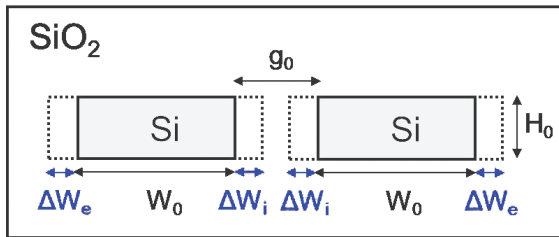
▲ Figure 1: A silicon directional coupler. W_0 and g_0 are the nominal value of the waveguide width and gap. ΔW_e and ΔW_i are exterior and interior waveguide sidewall positions, which are assumed to be correlated.
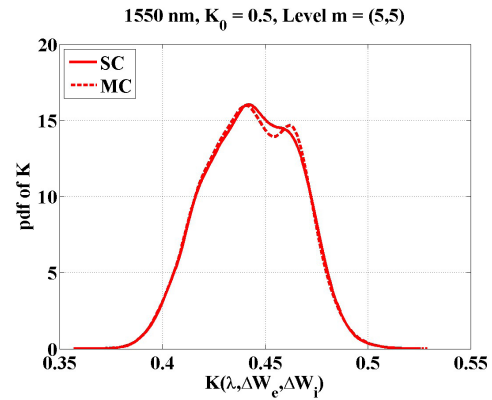
▲ Figure 2: The probability density function of power coupling coefficients of a directional coupler under non-Gaussian process variations. The nominal value is designed to be 0.5 at 1550 nm. The dash line and solid line represent Monte-Carlo simulation and stochastic collocation, respectively.

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# Irradiation Defects in Germanium

C. Monmeyran, N. Patel, A. Agarwal, L. C. Kimerling
Sponsorship: Defense Threat Reduction Agency

Defects in semiconductors, no matter how they arise, control the properties and consequently the performances of a device. Hence, an understanding of bandgap defect states followed by appropriate defect engineering is crucial for obtaining high-performance devices. A systematic study of defects in silicon has been performed, successfully mapping the characteristics of the defect states within the silicon bandgap. But such an investigation has not yet been achieved in germanium, which, in addition to its usage in electronics, is an essential element for Si microphotonics.

^{60}Cobalt (^{60}Co) gamma irradiation is used to uniformly create elemental defects, vacancies, and interstitials in a controlled fashion in Czochralski-grown 10^{15} cm^{-3} Sb-doped germanium. These primary defects and the complexes they form with lattice impurities are then characterized using deep-level transient spectroscopy (DLTS), leading to the measurement of defect concentrations, energetic positions within the bandgap and capture cross-sections. Isochronal and isothermal annealing of the gamma-irradiated-germanium are also performed for 0 to 400 min and from room temperature to 200˚C.

Figure 1 shows a typical DLTS spectrum obtained after ^{60}Co irradiation of Ge, and Figure 2 is the Arrhenius plot corresponding to each peak. The peaks are named according to the apparent activation energies shown in the plot relative to the level position below the conduction band. E_{37} dominates the spectrum and has been reported as the E-center, a vacancy group V impurity complex. The other three defects in this figure, however, have not been systematically reported, and their physical identity remains unknown. The purpose of our study is to gain an insight into the nature of these deep states.
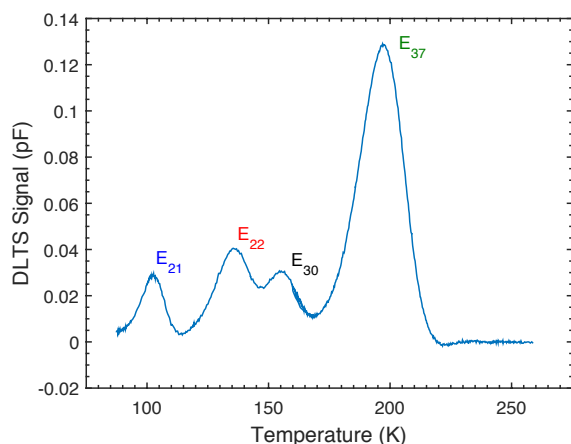
▲ Figure 1: DLTS scan of a room temperature gamma irradiated 10^{15} cm^{-3} Sb-doped Ge at a rate window of 200 s^{-1} with a filling pulse of 500 us, with reverse voltage and pulse voltage of -5 V and 0V, respectively.
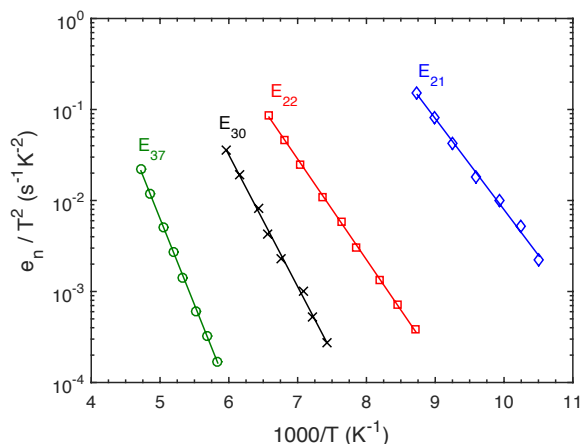
▲ Figure 2: Arrhenius behavior of the observed peaks in irradiated Ge from which the activation energies and capture cross-sections are extracted.
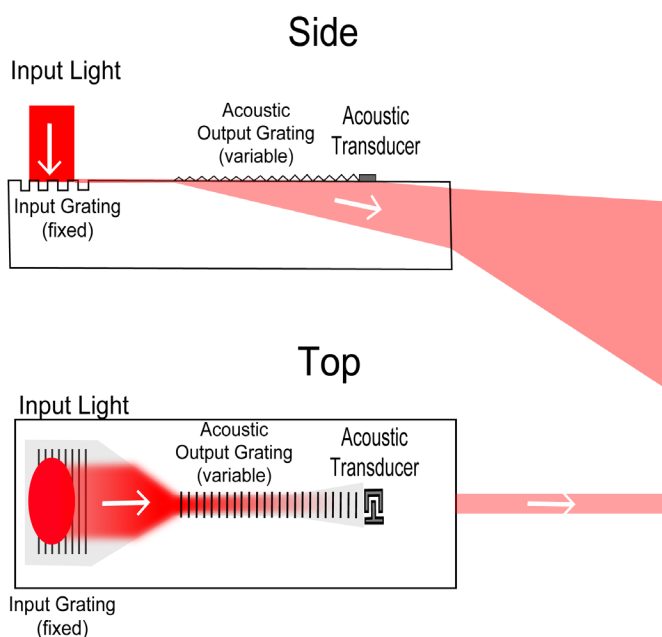
Light Modulators for Holographic Video Displays

V. M. Bove, Jr., S. Jolly, N. Savidis, B. Datta
Sponsorship: MIT Media Lab research consortium, Center for Terrestrial Sensing, AFRL

In this research (a collaboration with Dr. Daniel Smalley of Brigham Young University), we design and fabricate acousto-optic, guided-wave modulators in proton-exchanged lithium niobate for use in holographic and other high-bandwidth displays. Guided-wave techniques make possible the fabrication of modulators that are higher in bandwidth and lower in cost than analogous bulk-wave acousto-optic devices or other spatial light modulators used for diffractive displays and enable simultaneous modulation of red, green, and blue light. In particular, we are investigat-

ing multichannel variants of these devices with an emphasis on maximizing the number of modulating channels to achieve large total bandwidths. To date we have demonstrated multichannel full-color modulators capable of displaying holographic light fields at standard-definition television resolution and at video frame rates. New work aims to make larger direct-view panels based on an extension of this technology and different materials. Figures 1 and 2 show a schematic diagram of our device and an image displayed using it.

◄ Figure 1: Diagram of our modulator (one channel).
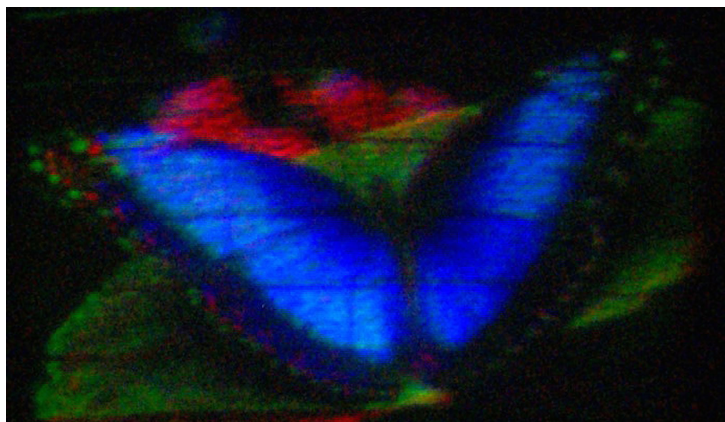
◄ Figure 2: Color holographic image displayed using our modulator.

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Electrically Tunable Organic Vertical-Cavity Surface-Emitting Laser

A. Murarka, W. Chang, A. Wang, J. Lang, V. Bulović
Sponsorship: National Science Foundation Center for Energy Efficient Electronics Science

Development of compact tunable lasing devices, using large-area scalable fabrication techniques, would enable many applications in spectroscopy and remote sensing. Additionally, organic semiconducting thin films can be used as spectrally-broad lasing gain materials, with a demonstrated visible lasing wavelength range of over 100 nm using a single organic guest-host gain medium. However, previously demonstrated frequency-tunable lasing devices have required either complex fabrication techniques, external micro-actuated mirror stages, or manual switching between gain media. Tunable air-gap MEMS microcavity structures offer a scalable, integrated solution, but their conventional fabrication processes are incompatible with solvent- and temperature-sensitive organic gain materials.

We demonstrate an electrically tunable organic laser fabricated using a solvent-free composite membrane transfer technique, which allows us to combine the compact form of a MEMS vertical-cavity surface-emitting laser (VCSEL) with spectrally-broad organic gain media to realize large range tunability in compact laser arrays. The device comprises a composite membrane suspended over cavities in a SU-8 spacer layer atop a distributed Bragg reflector. The suspended membrane incorporates an organic laser gain medium, Alq3:DCM, into the microcavity, and the completed capacitive structure can be electrostatically actuated for dynamic tuning of the optical spectra.

Cavity mode emission and lasing in device arrays is measured using a 400 nm wavelength excitation laser as optical pump. Additionally, bias is applied between the composite membrane and the underlying electrode to deflect the membrane and tune the microcavity length. These devices demonstrate a lasing threshold of 200 µJ/cm², as indicated by the integrated emission intensity and the reduction in the full-width half-max (FWHM) spectral linewidth (Figure 1). Electrical actuation and optical characterization of these devices show reversible lasing mode tuning of 10 nm at 6V bias (Figure 2). The membrane deflection and resulting cavity mode shift vary with the square of the applied voltage, as expected. Optimization of device structure and composition to reduce membrane pull-in effects would allow larger ranges of reversible lasing tunability.
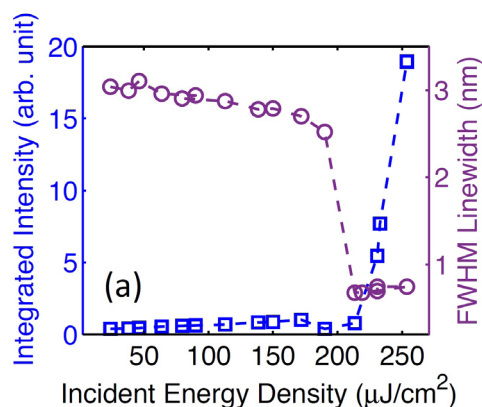
▲ Figure 1: Integrated emission intensity (left axis) and FWHM spectral linewidth (right axis) as a function of estimated excitation energy density. The nonlinear increase in intensity and a sudden decrease in mode linewidth are indicative of a lasing threshold of 200 µJ/cm².
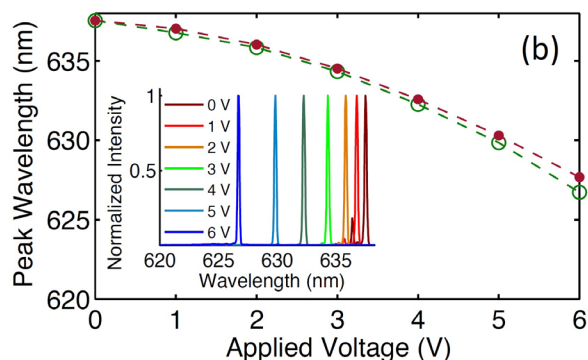
▲ Figure 2: VCSEL wavelength shift under applied bias in two consecutive sweeps shows hysteresis below 1 nm. (inset) Normalized spectra of laser emission at various bias voltages.

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Ultra-Compact Low-Threshold Organic Laser

P. B. Deotare, T. S Mahony, V. Bulović,
Sponsorship: EFRC Center for Excitonics, MIT

Lasing has been reported under photo-excitation in organic dye devices with distributed Bragg reflectors, distributed feedback structures, whispering gallery resonators, photonic bandgap fiber resonators, and 2D photonic crystals. However, no demonstration of an electrically pumped organic laser has yet been reported. The major limiting factor is attributed to singlet-triplet annihilation leading to unfeasible threshold current densities. A possible way to tackle this problem is to lower the threshold by controlling the device optical properties.

Here, we try to achieve this by controlling the quality factor/mode volume (Q/V) and/or spontaneous emission factor (β), using a photonic crystal nanobeam cavity (PCNC). Lasing was observed with a threshold of 4.2 µJ/cm² when pumped using femtosecond pulses of λ = 400 nm wavelength light. We also modeled the dynamics of the laser and show good agreement with the experimental data. The devices are fabricated using a top-down approach, which will assist in scalability during manufacturing. These lasers are the smallest organic lasers to be reported, and their waveguide geometry enables on-chip integration with potential application in data communication.

We anticipate that the results will be the launching pad for further work towards achieving an electrically pumped organic laser as well as open up new research areas in optomechanics (due to a suspended structure) and integrated on-chip photonics (due to waveguide geometry) for applications in motion sensing, biochemical sensing and data communication.
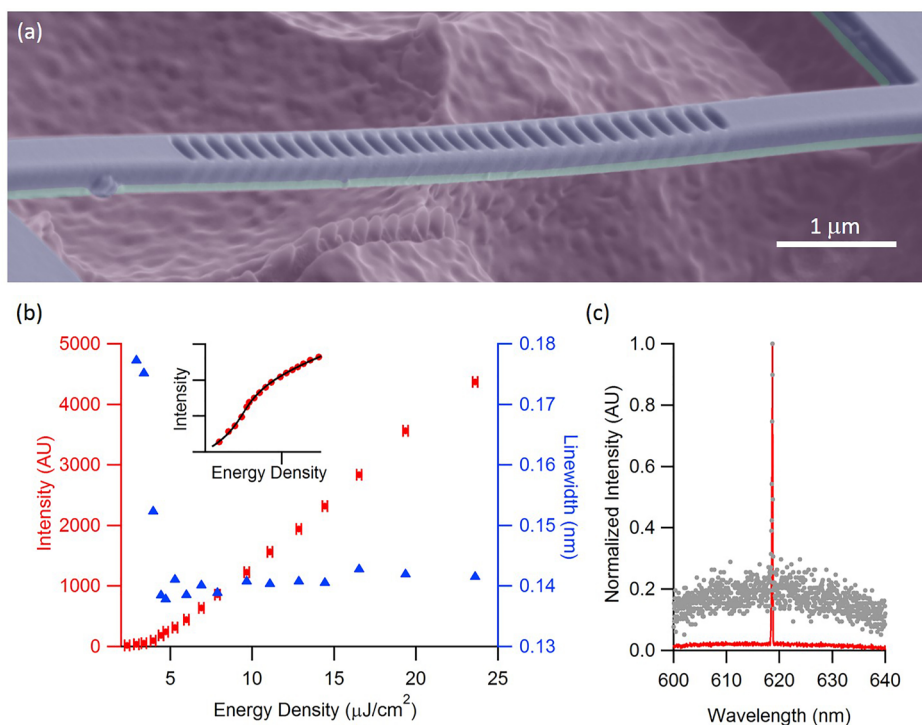
▲ Figure 1: (a) SEM image of the fabricated device. (b) Red filled circles denote the output intensity of the optical mode for various absorbed input pulse energy densities. Blue triangles show the corresponding linewidth of the mode. Linewidth narrowing at threshold is observed as a confirmation for lasing. Inset shows log-log plot of the experimental intensity data. The solid line is the numerical fit to the data. (c) Output spectrum of device below (gray line) and above (red line) threshold.

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# Integrated Mid-infrared Laser Based on an Er-doped Chalcogenide Microresonator

Z. Han, L. Zhang, L. C. Kimerling, A. M. Agarwal

Mid-infrared (mid-IR) represents a wavelength range that remains less explored in many optics and photonics branches, e.g., in integrated photonics. Recently, significant research effort has been made to develop passive, active and nonlinear integrated devices in the mid-IR. One key benefit of a monolithically integrated mid-IR device is that it enables compact, potentially energy-efficient and cost-effective systems for sensing, signal processing, and communications. For such systems, an integrated on-chip laser source is critical.

The invention of quantum cascade lasers (QCLs) represents a revolutionary development in this area. However, near the short-wavelength end of the mid-IR range, around 2~4 µm, the availability of QCLs is quite limited. Another technical approach to lasing in the mid-IR, which has also experienced great advances recently, is rare-earth-doped fiber lasers. Bulk Er^{3+}-doped GLS shows mid-IR photoluminescence emission at 3.6 µm through the transition between $^4F_{9/2}$ and $^4I_{9/2}$ energy levels. The correlated pumping wavelength is 0.66 µm, which can be realized by a semiconductor laser.

In this work, we numerically demonstrate the feasibility of building a planar room-temperature low-pump-power integrated mid-IR laser, enabled by a high-Q microresonator. Essentially, the cavity acts as a microring resonator at the signal wavelength in the mid-IR range and is similar to a whispering gallery microdisk resonator at the pump wavelength. With a gap of 100 nm, designs with different coupling lengths (L_C) are simulated. A joint consideration of Q factor (at lasing wavelength) and power enhancement factor (at pumping wavelength, $\eta = P_{ring}/P_{bus}$) reveals an optimal L_C of 0.6 µm, $\eta = 50.64$ and $Q = 2.2 \times 10^5$. Threshold power is 7.6 µW, and slope efficiency is 10.26%.
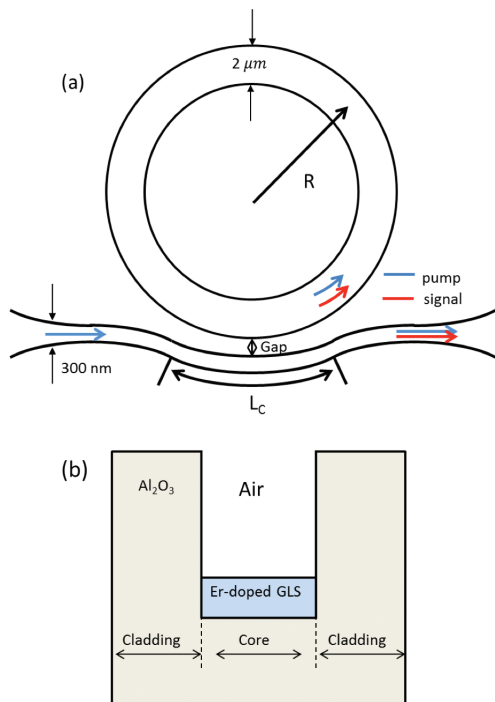
▲ Figure 1: (a) Device configuration of a high-Q microresonator-based mid-IR laser, which consists of a ring resonator with a curved bus waveguide. (b) Cross section of a chalcogenide waveguide that is in an Al_2O_3 trench.
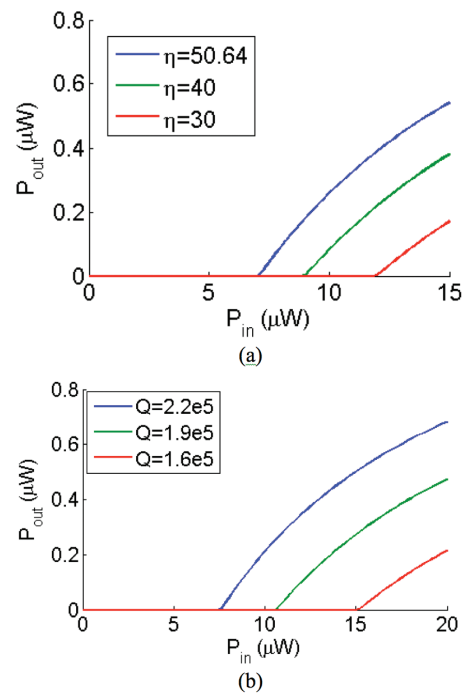
▲ Figure 2: Predicted lasing performance for gap=100 nm and LC=0.6 µm (a) The influence of the power enhancement on the lasing threshold, and (b) the influence of the cavity Q-factor are shown.

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# Design and Manufacture of Bio-Inspired Light-Emitting Optical Micro-Cavities

C. Chazot, Y. Kim, M. Kolle
Sponsorship: MTL, MISTI

Optical micro-cavities are structures confining light in a small volume by resonant circulation. They can be constructed from two reflective surfaces sandwiching a gain medium to create light-emitting devices and lasers. The quality factor, representing the ratio between the number of round trips that a photon takes in the cavity and the cavity losses, determines the maximum attainable light amplification.

We design and manufacture optical micro-cavities containing light-emitting organic dyes, which were inspired by a structure found on the wings of the *Papilio blumei* butterfly. In the micro-cavities described here, individual reflectors consist of concave half-spherical metal surfaces with 1 µm-to-10 µm diameter topped by a Bragg reflector (Figure 1a). Given their micro-scale dimensions, the cavities support a variety of optical resonances in the visible spectrum (Figure 1b). The cavities' bottom reflector is formed from gold or silver with broadband reflectivity. The second light-confining mirror, a flat Bragg reflector, provides high reflectivity for a selected spectral range. The amplifying medium consists of an organic dye stabilized in a polymer matrix.

The manufacturing of the micro-cavities combines a set of procedures, including the assembly of a colloidal template (Figure 1c), the formation of cavities by electro-deposition of metal in the template's interstitial spaces (Figure 1d), template removal, solvent-based spin-casting of the organic dye, and the creation of a Bragg reflector using chemical vapor deposition. The cavities represent periodically arranged micro-scale light sources (Figure 1e) with potential to be selectively switched on and off. Furthermore, they show interesting optical behaviors such as spectral selectivity, polarization rotation effects, and emission in a broad range of angles. The cavities will be incorporated into microfluidic devices and lab-on-chip assemblies to provide localized chemical sensing and precise cell imaging for applications in microbiology.
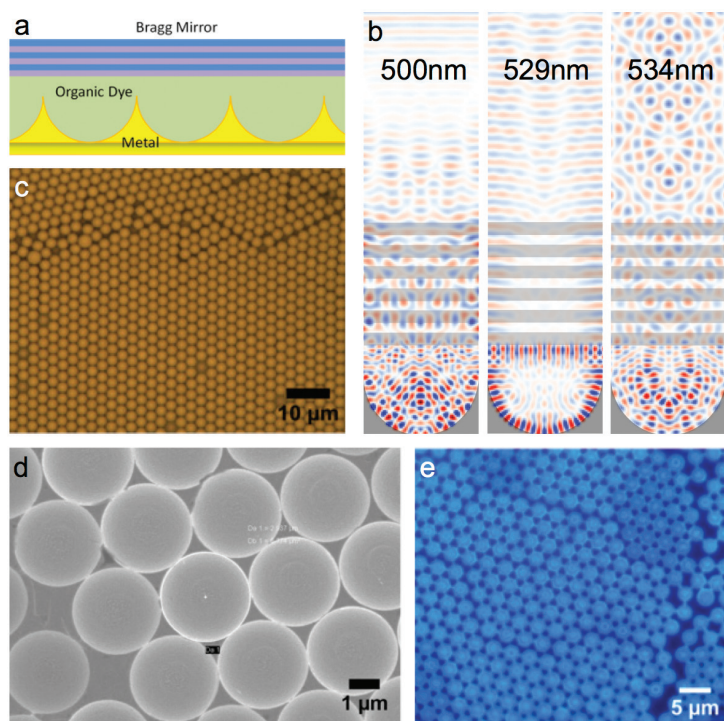
◄ Figure 1: a) Schematic of the resonance cavity layout. b) Finite-Difference-Time-Domain simulations of light fields in the cavities for different light wavelengths marked in the image. c) A monolayer of colloidal particles that serves as a template for the formation of the cavities by electro-deposition. d) Half-spherical gold cavities after electro-deposition and removal of the template. e) Optical micrograph of fluorescing organic dye in the optical cavities.

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Enhancement of Colloidal Quantum Dot Luminescence through Photonic Crystal Cavity Modes

T. S. Mahony, P. B. Deotare, V. Bulović
Sponsorship: National Science Foundation, Department of Energy Center for Excitonics

Colloidal quantum dots are semiconductor nanocrystals that can be used as bright light emitters. Their size tunability allows them to emit across the visible spectrum and has enabled their use in LED displays. They are also promising materials for use in generating optical gain for laser applications. Lasing using colloidal quantum dots has been demonstrated using VCSEL and DFB structures, but neither of these devices forms a compact structure, a desirable attribute for an on-chip laser. We are designing a compact laser with a waveguide geometry suitable for an integrated photonic architecture, and we hope to show a further reduction of lasing threshold in our devices.

To create such a laser, we can separate the design process into two pieces: cavity design and fabrication process. The cavity design follows the guidelines found in the literature for creating a deterministically high quality factor nanobeam photonic crystal cavity. These cavities can achieve a theoretical quality factor (Q) of 10^5-10^6 with a mode volume approaching the limit of a cubic half wavelength. Nanobeam photonic crystal cavities are suspended structures that have been demonstrated even for very low index contrast systems such as polymers.

The design of the cavity depends on our ability to create nano-patterned suspended structures of quantum dots. Though demonstrations of nano-patterned quantum dots can be found in the literature, none have been suspended. To overcome this challenge, we mix our quantum dots into a solution with PMMA. We spin coat these solutions on a silicon substrate, leaving behind a thin composite film of PMMA-QDs. At high weight fractions we found that the quantum dots are thermodynamically driven to phase separate from the PMMA, but at low weight fractions, they remain embedded within the polymer matrix. We confirmed our findings by SEM images taken of the surface of devices shown in Figure 1. These films are then patterned with ebeam lithography and undercut to create suspended structures.

We measure the photoluminescence of the cavity structures under pulsed optical excitation. As Figure 2 shows, we observe significant enhancement in the photoluminescence of the quantum dots through the cavity modes. By fitting these peaks to Lorentzian lineshapes, we can estimate the Qs of each mode to be about 1800; however, for the spectra we took, these Q's were limited by the spectrometer resolution. We are hopeful that under power-dependent optical measurements, these cavities will demonstrate the characteristics of lasing.
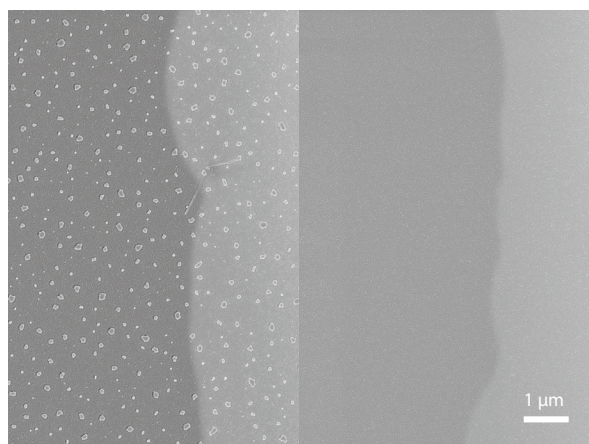
▲ Figure 1: SEM image showing the surfaces of films with a weight ratio of 15:1 PMMA:QDs on the left and 150:1 on the right. We see that the quantum dots phase separate from the PMMA at higher weight fractions.
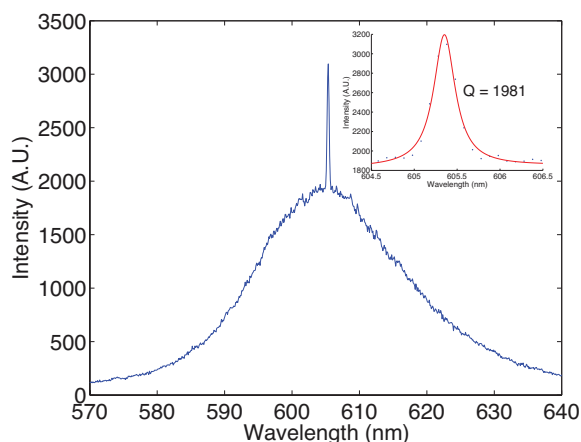
▲ Figure 2: Photoluminescence spectrum of a representative device showing enhanced emission through the cavity mode. Inset: Fit of the cavity mode emission spectrum yields a quality factor of 1981.

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Inkjet Printing High-Resolution Patterning of Quantum Dot-LEDs

G. Azzellino, G. J. Supran, V. Bulović

The high luminescence efficiency and uniquely size-tunable color of solution-processable semiconducting colloidal quantum dots (QDs) highlight their potential for use as both optically- and electrically-excited luminophores in energy-efficient, substrate-independent, high-color-quality solid-state lighting and thin-film display technologies. Recent advances in the design of electrically-driven QD-LEDs have seen their external quantum efficiencies approach 20%, comparable to those of phosphorescent organic LEDs.

We demonstrate high-resolution patterning of quantum dot light-emitting devices (QD-LEDs) by using the droplet-on-demand inkjet printing of colloidal QDs. By tailoring the solvents of QD solutions and by modifying the surface energy of the layer underlying the printed QD films, we obtain "coffee-stain"-free QD structures. We also introduce a surface treatment, applied before printing, which allows us to shrink the lateral dimensions of droplets. In our demonstrations we shrink the size of printed QD features down to 10 μm, using single-droplet prints. With the latest generation of "hybrid" QD-LED architectures, we show that both visible- and near infrared-emitting QD-LEDs can be patterned, with pixel areas defined by these single printed droplets. This approach definitely paves the way to the high-resolution QD-LED displays.

Inkjet printing offers a new, largely unexplored technique for room temperature, maskless pattering of QD-LEDs, yet inkjet printing is often hampered by the formation of "coffee-stains," which can be difficult to overcome solely through optimization of the driving voltage waveform of the printer-head. Here, solvent tailoring enables "coffee-stain"-free, smooth, and uniform inkjet-printing of QD pixels. Since the technique relies on tailoring the solvent, not the solute, it is readily translatable to most QD solutions.
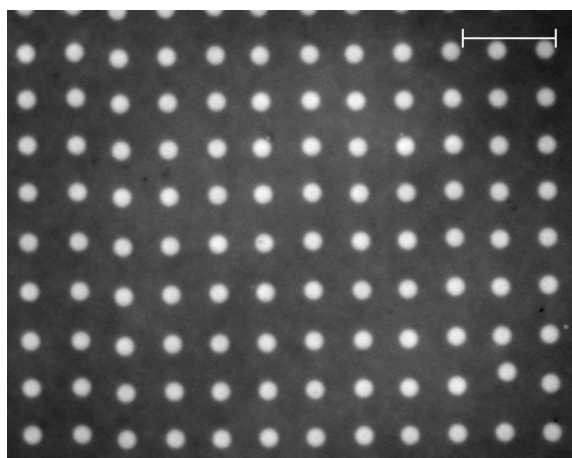
▲ Figure 1: Optical profilometry of an array of infra-red core-shell PbS quantum dots inkjet-printed onto pre-treated ZnO (scale bar is 50 µm).
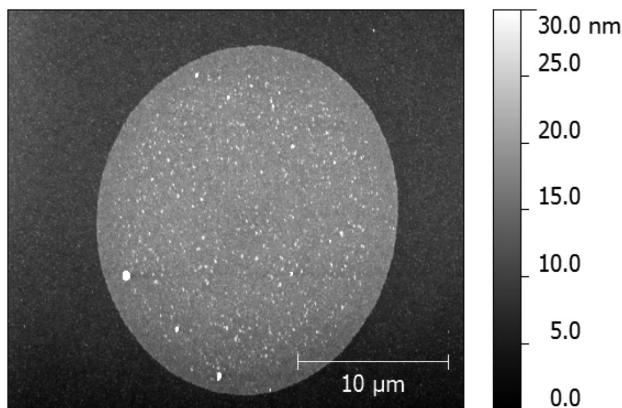
▲ Figure 2: AFM topography of a "coffee stain"-free droplet of core-shell PbS onto pre-treated ZnO.

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# Transport of Charge Transfer States in Organic Blends

P. B. Deotare, W. Chang, E. Hontz, D. N. Congreve, P. D. Reusswig, B. Modtland, M. E. Bahlke, V. Bulović, T. Van Voorhis, M. A. Baldo
Sponsorship: EFRC Center for Excitonics, MIT

The dynamics of charge transfer (CT) states, bound combinations of an electron and a hole on separate molecules are perhaps the most controversial topic in organic semiconductor devices. CT states, which mediate efficient generation of free charges, are bound in many systems. Consequently, there has been debate over whether charge generation requires mediation by "hot" (non-equilibrium) CT states. Recent studies, including the 2014 Nature Materials paper by Vandewal et al., have shown that the CT states do not need to be hot to efficiently generate photocurrent. These results only deepen the mystery over the generation of photocurrent in such devices. The central question is now: if they are not hot, then what are the dynamics of CT states?

Here, we present the first direct imaging of CT states. Contrary to expectations, we find that the CT states diffuse, and the transport mechanism seems to be neither the conventional Förster nor Dexter process. Rather, it seems to be a novel exciton-stretching transport analogous to an "inchworm" motion, where the state moves through the blend by repeatedly extending and then contracting into a new position at the donor-acceptor interface.

Given the short exciton lifetimes characteristic of bulk heterojunction organic solar cells, this work confirms the potential importance of CT state transport, suggesting that CT states are likely to diffuse farther than the Frenkel exciton in many donor-acceptor blends. Since donor-acceptor blends typically exhibit rapid conversion from excitons to CT states, it is possible that CT state diffusion distances in many organic devices exceed that of the initial exciton, highlighting the potential importance and impact of CT state transport on device performance. This work will significantly advance the understanding of CT state dynamics with practical implications for organic optoelectronics.
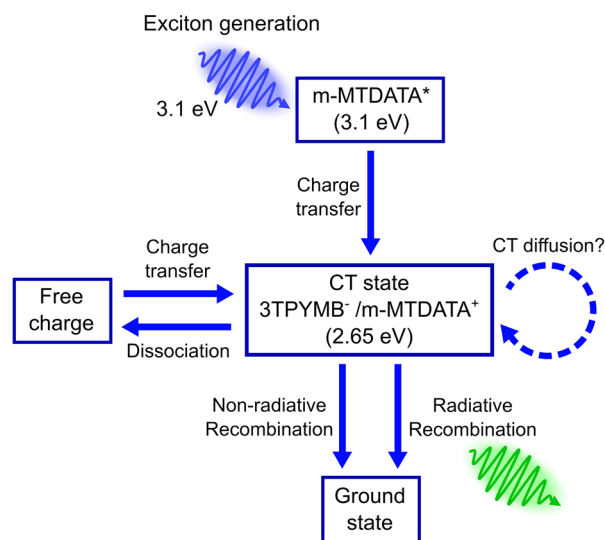
▲ Figure 1: *m*-MTDATA/3TPYMB Charge transfer blend. Schematic of charge transfer state dynamics.
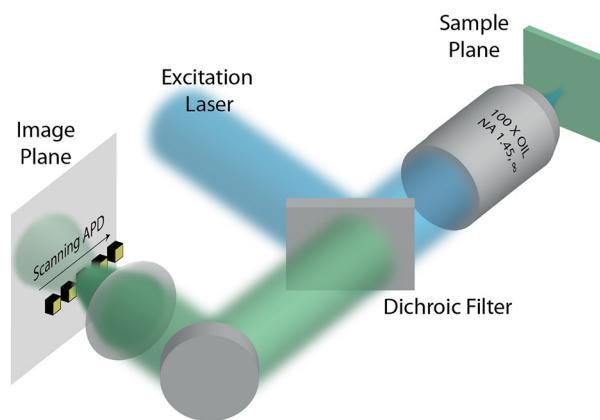
▲ Figure 2: Diffusion imaging. Setup schematic of the optical microscope with a scanning detector for diffusion imaging measurements.

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Quantum-Spillover Enhanced Surface-Plasmonic Absorption at the Interface of Silver and High-Index Dielectrics

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Sponsorship: National Science Foundation, AFOSR

Surface plasmons (SPs), known as collective oscillations of conduction electrons at a metal-dielectric interface, have attracted interest for several decades. Nanomaterials that strongly absorb visible light through plasmonic effects could be very important for solar-energy devices. It is normally assumed that classical theory, with prescribed frequency-dependent bulk permittivities, reliably captures the SP properties. Quantum effects, despite their academic interest, are usually considered to have negligible effect in practical systems.

We demonstrate an unexpectedly strong surface-plasmonic absorption at the interface of silver and high-index dielectrics. We show, from first-principles, that due to the lowered metal-to-dielectric work-function at such interface, conduction electrons display a drastic quantum spillover, causing the interfacial electron-hole pair production to become the predominant dissipation channel (Figure 1). The theoretical prediction is supported experimentally by the electron-energy loss spectroscopy and ultraviolet-visible spectrophotometry (Figure 2). This finding can be of fundamental importance in understanding and designing quantum nano-plasmonic devices, which utilize metal-high-index contacts.
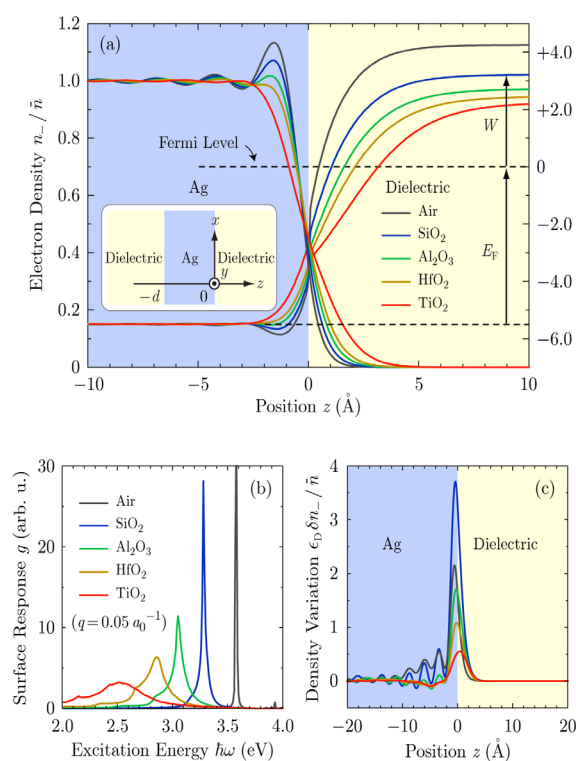
▲ Figure 1: (a) Calculated ground-state electron-density profiles and effective-potential profiles for silver in contact with varied dielectrics. (b) Calculated dynamic surface response. (c) Calculated induced density variation.
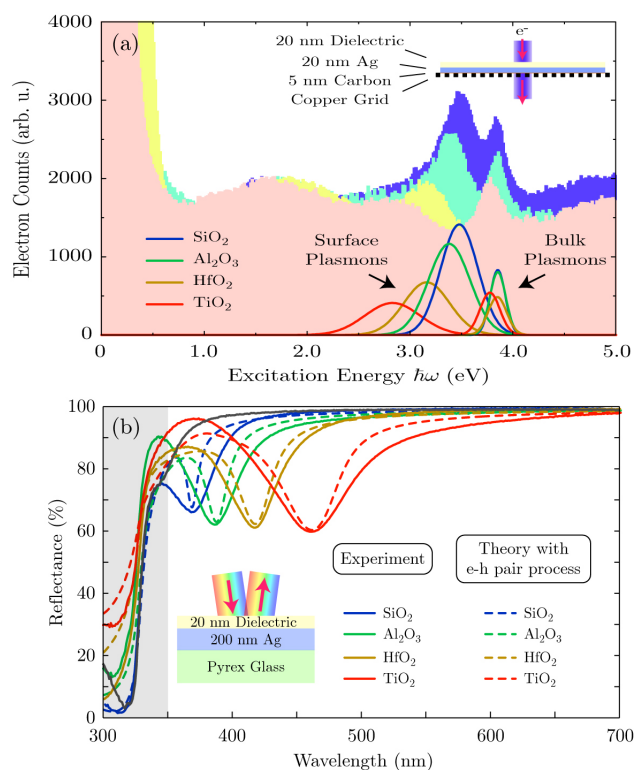
▲ Figure 2: (a) Electron energy-loss spectra for 20 nm dielectrics on 20 nm silver. (b) Experimentally measured and theoretically calculated reflection spectra for 20 nm dielectrics on 200 nm silver. The grey curve is the measured reflectance of the bare 200 nm silver as a reference.

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# Integrated Graphene-Based Photonic Devices

R. Shiue, J. Goldstein, C. Peng, D. Efetov, D. Englund
Sponsorship: Office of Naval Research

Graphene is a single-atom-thick 2D material consisting of a single layer of graphite. Its high carrier mobility, extremely broadband and uniform optical properties, high surface area, CMOS compatibility, and potentially low cost of manufacture make it a promising material for optoelectronic applications (among many others). In particular, graphene's high mobility and extremely fast carrier dynamics make it suitable for applications that require high speed operation, e.g., telecommunications, where digital signals must be modulated onto light using optical modulators and detected using photodetectors. Typically, these optical signals use wavelengths of around 1550 nm, which coincides with the absorption minimum of glass optical fibers. We aim to demonstrate fast, CMOS-compatible waveguide-integrated graphene-based photodetectors and modulators that outperform the state-of-the-art germanium photodetectors and silicon modulators in terms of speed and, ideally, size.

Previously, we reported a waveguide-integrated graphene photodetector (shown in Figure 1) with a high responsivity of up to 0.1 A/W and a bandwidth of above 20 GHz at zero bias operating at wavelengths between 1450 and 1590 nm. In this device, the gold contacts pin the Fermi level of the graphene channel, which, being a 2D material, has a very low density of electronic states. The gold contacts create a jump in the Fermi level near the contacts, which in turn yields a jump in the graphene's Seebeck coefficient. Combining the Fermi level profile with the electron temperature bump from the absorption of light passing through the waveguide, we obtain a measurable thermoelectric voltage, just as in a thermocouple. We are continuing to improve upon these types of devices and to combine them in optical networks.

More recently, we demonstrated an optical reflection modulator involving a silicon photonic crystal cavity transferred on top of a boron nitride (BN)-graphene-BN-graphene-BN stack (a so-called Van der Waals heterostructure) as shown in Figure 2. In this device, a voltage applied between the two graphene layers shifts their Fermi levels, preventing them from absorbing light below a certain frequency due to Pauli blocking. The photonic crystal cavity on top of the graphene "sandwich" supports an optical mode that overlaps with the graphene sheets, allowing absorption of the mode to be controlled by the input voltage. This device shows a 3.2-dB modulation depth and a cutoff frequency of 1.2 GHz.
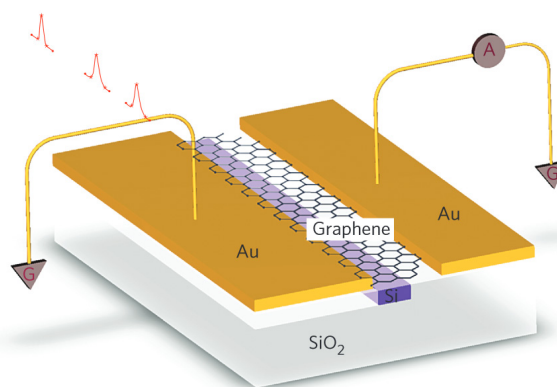
▲ Figure 1: This graphene photodetector's photoresponse is caused mainly by the photothermoelectric effect, whereby charge carriers heated by the absorbed radiation interact with a nonuniform Seebeck coefficient to generate a photovoltage.
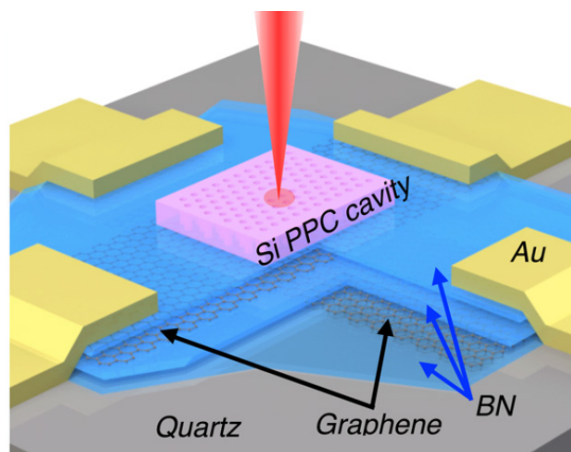
▲ Figure 2: This image depicts a graphene-based reflection modulator. Applying a voltage between the two graphene sheets changes their optical absorption, while a photonic crystal cavity concentrates light in the vicinity of the sheets.

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# Free-Space Coupled Superconducting Nanowire Single-Photon Detectors for Mid-IR Optical Communications

F. Bellei, A. P. Cartwright, A. McCaughan, A. E. Dane, F. Najafi, K. K. Berggren
Sponsorship: Office of Naval Research, IARPA

Mid-IR optical communication represents an important technology for naval and astronomical applications. A transmission window in the atmosphere at 10-um-wavelength (λ) allows mid-IR light to travel unperturbed for hundreds of kilometers. In addition, optical communication based on single-photon transmitters and receivers enables secured, high-speed, and low-power communication protocols if the receiver can detect more than 30% of the signal from the transmitter at a data rate of 100 Mbit/s. The superconducting nanowire single-photon detector (SNSPD) is the only existing technology that combines high-speed with single-photon sensitivity in the mid-IR; in order to couple more than 30% of the signal from the transmitter in the mid-IR, free-space optics is necessary. Our goal is to design an experimental apparatus that maximizes the mid-IR light coupled in free-space to an SNSPD.

Figure 1 shows a prototype of a cryogenic system that we designed and built with free-space optical access that couples on the detector more than 50% of the light from a source at λ = 1550 nm, dampens the vibration amplitude at the sample stage to < 400 nm, and has the potential for multiple channel communication. Commercially available cryostats could not meet those characteristics or were either too expensive or based on cryogens. We tested an SNSPD with an active area of 8 × 7.3 µm² at λ = 1550 nm, and we extrapolated from data that 56.5% of the light from the source hit the detector. An SNSPD can easily be fabricated with an active are of 10 × 10 µm², which would allow us to couple 76% of the light. Figure 2 shows the oscillation in the count rate of the detector that we used to extrapolate the vibration amplitude of the stage. Knowing the dimensions of the SNSPD and the beam diameter, we extrapolated vibration on the order of 400 nm.

This cryogenic system will be upgraded to work at mid-IR wavelength and to host 4 separate communication channels. Our coupling demonstration was performed at λ = 1550 nm because of our familiarity at that wavelength. Moving to mid-IR optics should simply be a matter choosing lenses with the correct focal length to allow high coupling on the SNSPD. The use of free-space components allows us to add multiple channels at the transmitter without changing the optics. Based on this idea, we will upgrade from single channel to four channels to improve the data rate capabilities of the system.
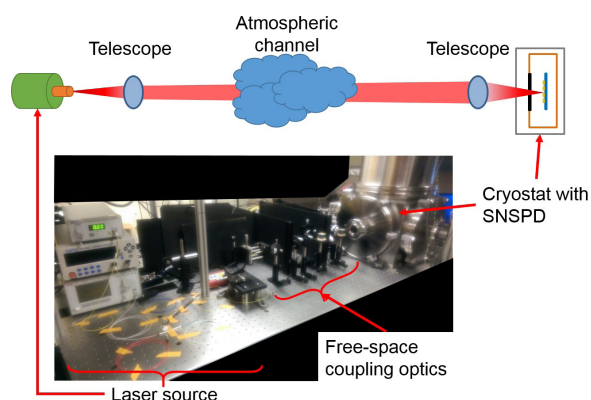
▲ Figure 1: Free-space coupled mid-IR optical communication system. On the top, we show a schematic of the final system for long distance communication. On the bottom, we show a picture of the prototype that we built and that operates at λ = 1550 nm.
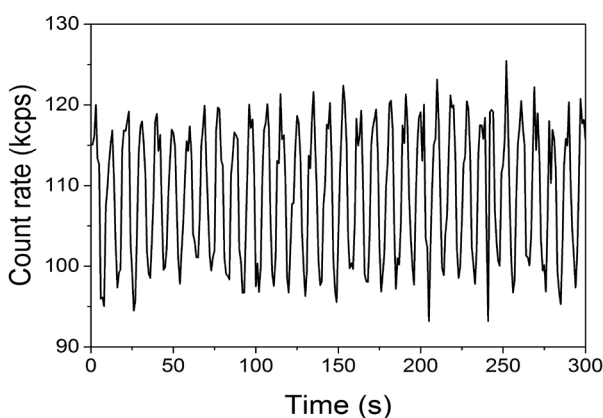
▲ Figure 2: Count rate from an 8×7.3 µm² area NbN SNSPD as a function of time. The signal beam was positioned at 4.6 µm from the center of the detector.

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Measuring the Timing Jitter of WSi SNSPDs with Integrated nTron Readout

A. Dane, Q. Zhao, A. McCaughan, F. Marsili, A. Beyer, M. Shaw, K. K. Berggren
Sponsorship: NASA Space Technology Research Fellowship, iQUISE National Science Foundation

Superconducting nanowire single photon detectors (SNSPDs) based on tungsten silicide (WSi) have been used to demonstrate the highest reported system detection efficiency at 1550 nm with a single device. However, WSi devices lag behind niobium nitride (NbN) SNSPDs in terms of timing performance, as both the reset time and the timing jitter are one order of magnitude larger in WSi than in NbN devices. WSi SNSPDs have higher jitter than NbN devices due to their lower switching current and lower signal-to-noise ratio (SNR). In order to decrease the jitter of WSi SNSPDs, a nano-cryroton (nTron) could be used to increase the output signal after photodetection and thus reduce jitter. The nTron is a three-terminal superconducting device that allows a small gate current to switch a channel current that is orders-of-magnitude larger. The reduction of the jitter of NbN SNSPDs using NbN nTrons has been demonstrated recently.

We designed and fabricated SNSPDs and nTrons on a single layer of 5-nm-thick WSi deposited on SiO_x. We used electron-beam lithography with hydrogen silsesquioxane resist to fabricate devices. This process was shown to yield superconducting WSi devices, and we have demonstrated that the addition of a DC bias current at the nTron gate can strongly suppress the switching current of the nTron channel as shown in Figure 2. Additionally, an off-chip coupling circuit was designed and built to couple the SNSPD output signal into the nTron gate. We used an electro-thermal model of superconducting nanowires contained in SPICE circuit simulation software to design the coupling circuit and ensure that both the SNSPD and the nTron could self-reset while operating at full speed. This work should enable the reduction of noise-related-jitter in WSi SNSPD systems via readout with integrated nTrons.
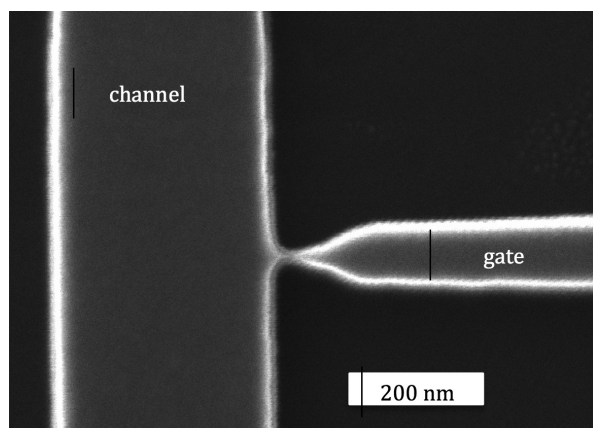
▲ Figure 1: Helium ion microscope image of WSi nTron fabricated by electron beam lithography. Current sourced into the nTron gate from the right can cause the narrow superconducting section that connects the gate and channel to switch to the normal state. Joule heating in this region reduces the channel's ability to carry current and can lead to switching.
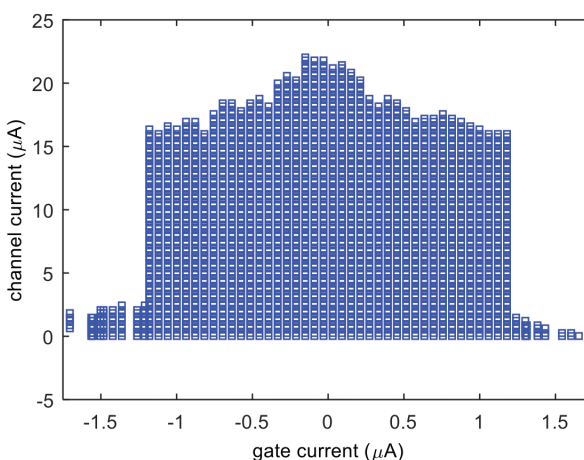
▲ Figure 2: The zero voltage state of the superconducting IV curves of a WSi nTron channel, as a function of the gate current. The channel switching current is strongly suppressed as the gate current is increased above 1.2 microamperes.

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# Ionic Conduction Studies in TlBr Radiation Detector Materials

S. N. Cook, S. R. Bishop, H. L. Tuller (in collaboration with S. Payne, A. Conway, K. Shah)
Sponsorship: Domestic Nuclear Detection Office, Lawrence Livermore National Laboratory, Radiation Monitoring Devices, Inc.

Detection of high-energy radiation (e.g., γ-rays) is key in nuclear non-proliferation strategies. When a wide-band gap semiconductor detector intercepts a γ-ray, electron-hole pairs are formed, resulting in an increase in electrical conductivity, facilitating their detection. As in any photodetecting device, sensitivity is maximized if the conductivity in the non-illuminated (dark) state is very low. While current semiconductor-based technologies require cooling to very low temperatures, adding to cost and reducing portability, TlBr is an attractive detector material given its low room temperature dark conductivity, as well as its high mass density, leading to high radiation absorption. In TlBr the dominant conduction mechanisms when non-illuminated are ionic. This ionic conduction therefore presents itself as a source of leakage current during operation and its minimization is valuable to produce higher performance detectors. A schematic illustrating operation and the presence of the leakage current is shown in Figure 1.

In this project, we characterize the ionic conduction properties of TlBr, dopant association, and exsolution using impedance spectroscopy. Through doping techniques, we have determined that TlBr is primarily a Schottky type ionic conductor, meaning that Tl and Br move through the material by vacancy motion. These measurements have led us to predict a doping strategy to minimize dark conductivity. We take advantage of the detailed defect model that we have established in the investigation of the origin of this long-term performance degradation and its relation to electrode chemistry.
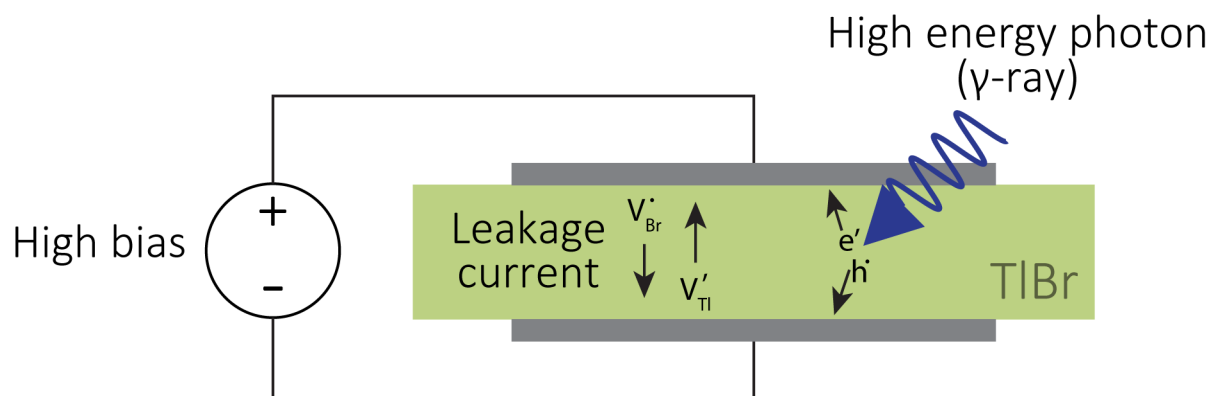
▲ Figure 1: The operating principle of TlBr radiation detectors showing the ionic species contributing to current leakage.

# MEMS, Field-Emitter, Thermal, Fluidic Devices

A Tabletop Deep Reactive Ion Etching System for MEMS Development and Production

P. A. Gould, M. D. Hsing, K. K. Gleason, M. A. Schmidt
Sponsorship: MTL

A general rule of thumb for new semiconductor fabrication facilities (fabs) is that revenues from the first year of production must match the capital cost of building the fab itself. With modern fabs routinely exceeding $1 billion to build, this rule serves as a significant barrier to entry for groups seeking to commercialize new semiconductor devices aimed at smaller market segments that require a dedicated process. To eliminate this cost barrier, we are working to create a suite of tools that will process small (~1") substrates and cost less than $1 million. This suite of tools, known colloquially as the 1" Fab, offers many advantages over traditional fabs. By shrinking the size of the substrate, we can realize substantial savings in material usage, energy consumption, and, most importantly, capital costs. This substantial reduction in capital costs will drastically increase the availability of semiconductor fabrication technology and enable experimentation, prototyping, and small-scale production to occur locally and economically.

The first 1" Fab tool we have developed is a deep reactive ion etcher (DRIE). DRIE tools are used to create highly anisotropic, high aspect-ratio trenches in silicon—a crucial element in many MEMS processes that will benefit from a 1" Fab platform. A labeled image and rendering of the 1" Fab DRIE is shown in Figure 1. The modularized design of our DRIE system can be easily adapted to produce other plasma-based etching and deposition tools (like PECVD and RIE). Using the switched-mode Bosch Process, the 1" Fab DRIE system currently can achieve silicon etch rates up to 6 μm/min with vertical sidewall profiles, an estimated photoresist selectivity greater than 50:1, and etch depth non-uniformity to less than 2% across the substrate. Several examples of anisotropic etches performed with our system are included in Figure 2. Presently, we are working to refine the mechanical design of the system and optimizing recipes for high-aspect ratio etching.
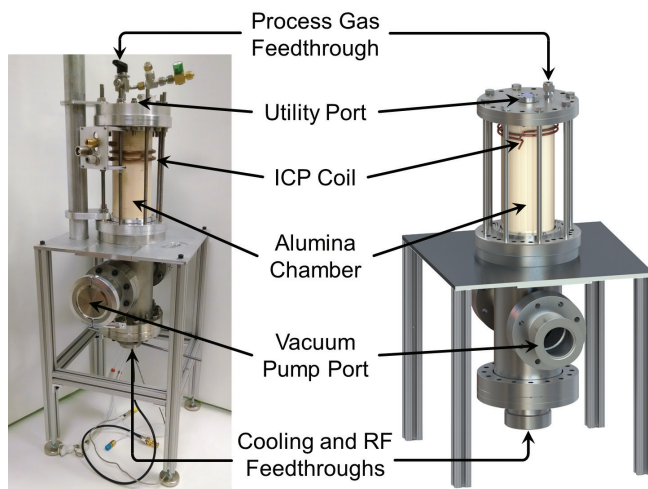
▲ Figure 1: View of the basic components of the 1" Fab DRIE system.
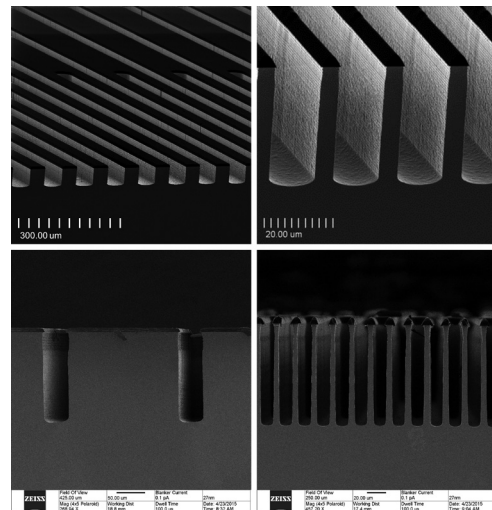
▲ Figure 2: Examples of anisotropic etches performed using the Bosch Process in the 1" Fab DRIE.

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# A Miniature MEMS Vacuum Pump with Curved Electrostatic Actuation

E. Newton, H. Li, M. A. Schmidt
Sponsorship: DARPA

Portable sensing devices such as microscale mass spectrometers need vacuum pumping to lower samples at atmospheric pressure to the desired measurement pressure range. Further improvements for MEMS accelerometers, gyros, and other resonant sensors require internal pressures as low as a few microtorr, which is possible only with active vacuum pumping. While these pressures are easily achieved using macroscale vacuum pumps, the larger pumps are not portable, negating the benefits gained from making small, low-power sensors in the first place. To realize the full potential of portable sensors, a chip-scale vacuum pump needs to be developed.

We are developing what is to our knowledge the first two-stage MEMS displacement pump with integrated electrostatic actuation. Two pump stages, along with an efficient layout that minimizes dead volume and a new actuation scheme, should enable it to reach pressures below 30 Torr. Actuation is achieved by electrostatically zipping a thin flexible membrane down onto a stiff curved electrode. This actuator topology allows for large displacements and large forces at relatively low voltages (< 100 V). An image of a fabricated two-stage micropump is shown in Figure 1 below.

We have developed two methods for producing curved electrodes in MEMS devices: 1) hot air trapped during wafer bonding expands with enough pressure to plastically deform a thin silicon membrane and 2) strain induced when epoxy cures can pull a membrane into a curved shape. We have demonstrated that we can reliably and repeatably zip a thin membrane using these curved electrodes at low voltages and we have mapped out how the critical voltage depends on the deformation magnitude and the oxide thickness. Finally, we have developed models to predict the extent of plastic deformation and the onset of pullin for these curved electrostatic electrodes. A comparison of the model and experimental data is shown in Figure 2 below.
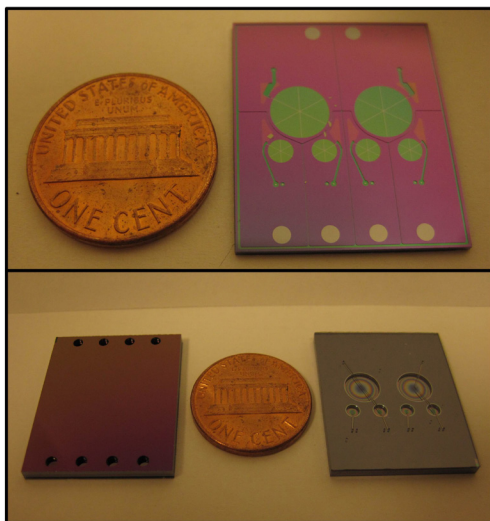
▲ Figure 1: Microfabricated two-stage vacuum pump. Top and bottom views of the pumps are shown (bottom), as are internal fluidic connections (top).
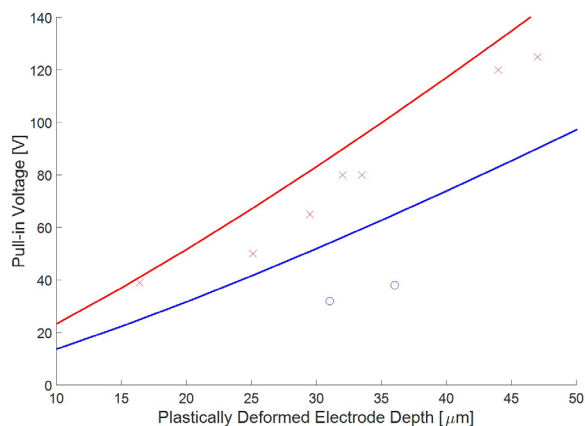
▲ Figure 2: Pull-in voltages for 6-mm-diameter curved electrodes with a 25-μm-thick zipping membrane. Data are shown for a 0.1-μm gap (blue) and a 0.5-μm gap (red).

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# Additive Manufacturing of Three-Dimensional Microfluidics

L. F. Velásquez-García
Sponsorship: DARPA

In many cases, microfluidics are manufactured in clean-rooms using semiconductor industry processes and materials, making them fairly expensive to produce. In addition, the device architecture is often a compromise between what should be made based on modeling and what can be made based on the planarity and thickness/depth limitation of most microfabrication processes. Moreover, a change of any of the in-plane features of the design typically requires the fabrication of one or more new lithography masks, incurring substantial costs and time delays. A manufacturing technology that can circumvent these difficulties without sacrificing device performance would greatly extend the kind of devices that can be made and the kind of commercial applications beyond research, high-end products, and large-volume products that can satisfied by microfluidic chips.

Additive manufacturing is a group of layer-by-layer fabrication methods that use a computer file to generate solid objects. Additive manufacturing started as a visualization tool of passive, mesoscaled parts; however, given the recent improvements in the resolution capabilities and cost of commercial 3D printers, additive manufacturing has recently been explored as a fabrication technology that could address the complexity of certain microsystems, e.g., microfluidics.

We are exploring the use of stereolithography to manufacture freeform microfluidics with three-dimensional hydraulic networks with features (range of dimensions, aspect ratio, morphology) that would be very hard to make using standard microfabrication processing. Stereolithography is an additive fabrication process that uses a computer file (Figure 1) to manufacture structures based on spatially controlled solidification of a liquid resin by photo-polymerization. For example, we have developed fabrication process flows for the creation of three-dimensional structures that can be used as multiplexed, externally fed electrospray emitter arrays (Figure 2); these structures have a minimum feature size and emitter density comparable to reported single-crystal silicon multiplexed electrospray devices. Current work focuses on exploring the resolution limits and capabilities of the 3D printing process, as well as in demonstrating working microfluidic chips.
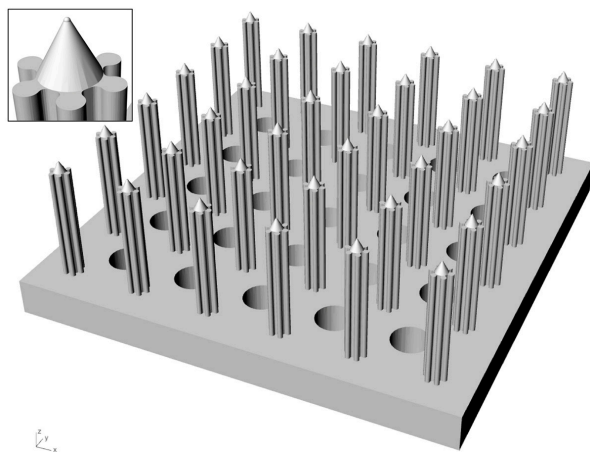
▲ Figure 1: Computer-aided design file of a monolithic array of 36 micro-sharpened, high aspect-ratio columns with lateral striations on top of a perforated plate and close-up of the side view of a tip.
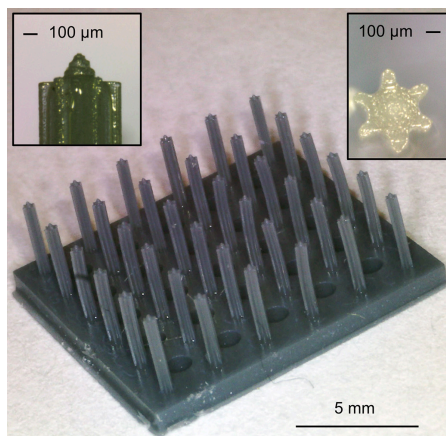
▲ Figure 2: A monolithic array of 36 3D-printed, micro-sharpened, high aspect-ratio columns with lateral striations on top of a perforated plate with close-up of the side view of a tip and top view of one of the columns. The structure could be used as a multiplexed externally fed electrospray source.

FURTHER READING

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Piezoelectric Nonlinearity in GaN Lamb Mode Resonators

S. Wang, L. Popa, D. Weinstein
Sponsorship: National Science Foundation, DARPA DAHI

This paper reports on the measurement of nonlinearity in GaN Lamb mode resonators subjected to power levels between 10 and +10 dBm. In these devices, nonlinearity manifests itself as both frequency shift ($\Delta f/f$ of 60-128 ppm) and change in motional impedance ($\Delta Rm/Rm$ of 13-33%). In this work, we decouple the contributions from self-heating and strain-induced piezoelectric nonlinearity to $\Delta R/R$, and conclude that strain-induced change in piezoelectric coefficients $\Delta e31$ and $\Delta e33$ is the dominant cause of $\Delta R/R$, accounting for 31% of the total 33% observed shift. The result is consistent with 2nd order nonlinear coefficients previously derived analytically.

Whether for use in radio filters or in frequency references, the MEMS resonator's capability to handle large RF power is crucial for system performance. It is therefore important to understand any nonlinearity in piezoelectric MEMS resonators. Studies have shown that self-heating is a primary contributor to frequency shift in AlN Lamb mode resonators. In this paper, we show that GaN Lamb mode resonators (Figure 1) are subject not only to frequency shift (Δf) from self-heating, but also to an increase in motional impedance (ΔRm) with increasing power levels due to a significant nonlinearity in piezoelectric coefficients (Figure 2). After ruling out these two factors, we conclude that the amplitude-induced $\Delta e31$ and $\Delta e31$ are the dominant contribution to ΔRm, consisting about 31% of the total 33% change.

The paper also concludes that self-heating is the main cause of frequency shift and nonlinearity in piezoelectric coefficient will dominate IIP3 (the input power at the third-order intercept point), an importance specification for weakly nonlinear devices in RF communication
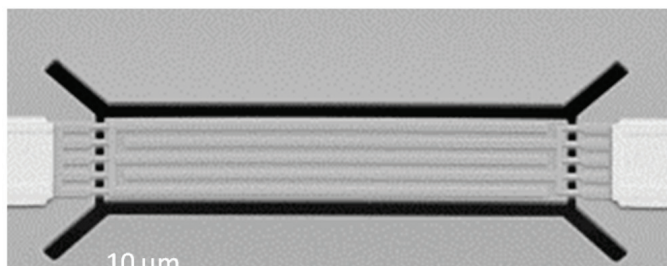
Figure 1: SEM of GaN Lamb mode resonator under study. This corresponds to Device 2 in Figure 3.
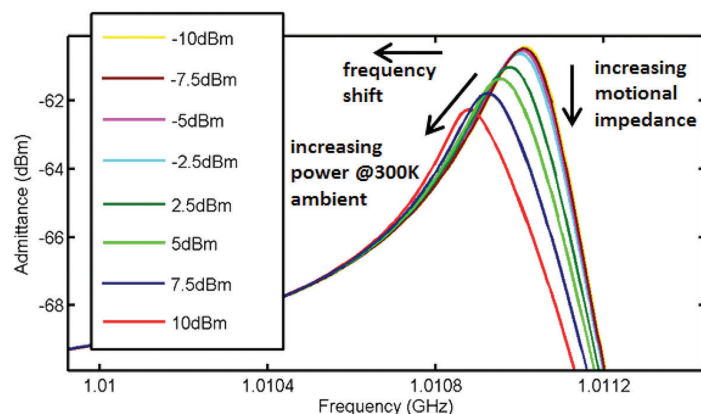
Figure 2: 1-port frequency response of GaN Lamb mode resonator, showing frequency drop and motional impedance increase with increasing power levels.

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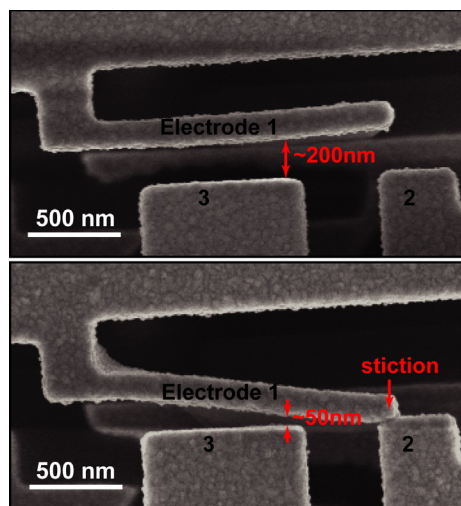
Controlled Fabrication of Nanoscale Gaps using Stiction

F. Niroui, E. M. Sletten, P. B. Deotare, A. I. Wang, T. M. Swager, J. H. Lang, V. Bulović
Sponsorship: National Science Foundation Center for Energy Efficient Electronics Science

As dimensions are continuously scaled down to achieve devices with higher performance and novel principles, developing methods for the controlled fabrication of nanogaps is important for enabling functional devices. Nanogaps are particularly critical for advancements in nanoelectromechanical systems (NEMS) and molecular electronics. Various methods of fabricating such gaps have been reported in the literature. However, these approaches are developed mainly for two-terminal devices, involve multiple processing steps, and commonly lack robustness, thus limiting their applications.

In this work we present an approach to controlled fabrication of nanoscale gaps through use of stiction, i.e., permanent adhesion between device components, an otherwise common mode of failure in electromechanical systems. In this scheme, laterally actuated cantilevers are patterned through electron beam lithography in polymethyl-methacrylate (PMMA). During the wet-developing process, the cantilever (labeled Electrode 1 in Figure 1) undergoes deflection due to the capillary forces, permanently adhering (stiction) to the opposing structure (Electrode 2). The deflection and stiction promote formation of nanogaps, smaller than originally patterned, between the cantilever and opposing electrode. Lastly, gold (Au) is evaporated onto the substrate defining the metallic electrodes onto the PMMA structures. The Au evaporation further reduces the gap size depending on the thickness of the film. The extent of deflection and its profile can be controlled through balancing the surface adhesive forces by altering the device geometry such that desired widths are achieved. The tunability of the gap size through device design is shown in Figure 2, where relative placement of the electrode with respect to the point of stiction defines the widths of the gap achieved. Furthermore, through modifications of device design, the nanogaps can be optimized to be electromechanically tunable or filled with molecular layers making them suitable for applications in tunneling electromechanical switches, nanoelectromechanical systems, and molecular electronics.

▲ Figure 1: Stiction induced through capillary forces during the fabrication process promotes formation of nanogaps smaller than patterned through the lithography process.
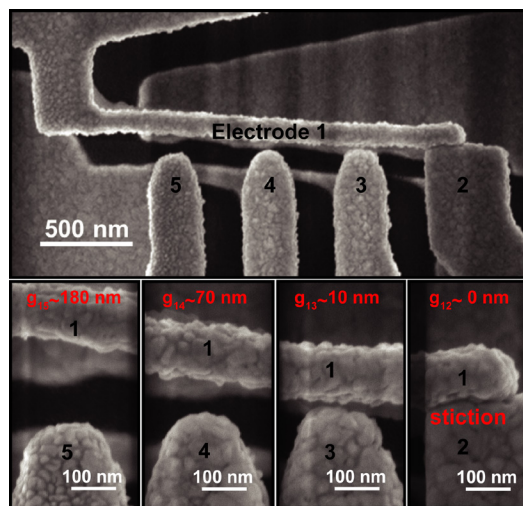
▲ Figure 2: Optimizing device architecture and electrode placement relative to the point of stiction allows achievement of nanogaps with controlled width.

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# Printed MEMS Membrane Electrostatic Microspeakers

A. Murarka, J. Jean, J. Lang, V. Bulović
Sponsorship: National Science Foundation Center for Energy Efficient Electronics Science

This work reports the fabrication and operation of electrostatic microspeakers formed by contact-transfer of 125-nm-thick gold membranes over cavities patterned in a micron-thick silicon dioxide (SiO_2) layer on a conducting substrate. Upon electrostatic actuation, the membranes deflect and produce sound. Additionally, membrane deflection upon pneumatic actuation can be used to monitor pressure. The microspeaker fabrication process reported enables fabrication of MEMS diaphragms without wet or deep reactive-ion etching, thus obviating the need for etch-stops and wafer-bonding. This process enables monolithic fabrication of multiple completely enclosed drum-like structures with non-perforated membranes to displace air, in both individual-transducer and phased-array geometries.

We characterized the mechanical deflection of the gold membranes using optical interferometry. The membranes show a repeatable peak center deflection of 121±13 nm across gaps of ~25 microns at 1 kHz sinusoidal actuation with 60 V peak-to-peak amplitude and a 30 V DC bias (Figure 1). The acoustic performance of the microspeakers is characterized in the free field. Sound pressure level of the microspeaker increases with frequency at 40 dB/decade (Figure 2), indicating that its sound pressure output is proportional to the acceleration of its diaphragm, as expected in the spring-controlled regime for free field radiation. The microspeaker consumes 262 µW of real electric power under broadband actuation in the free field and outputs 34 dB(SPL/Volt) of acoustic pressure at 10 kHz drive. The silicon wafer substrate (~500 µm thick) dominates the total thickness of the microspeakers; the active device thickness is less than 2 µm. These thin microspeakers have potential applications in hearing aids, headphones, and large-area phased arrays for directional sound sources.
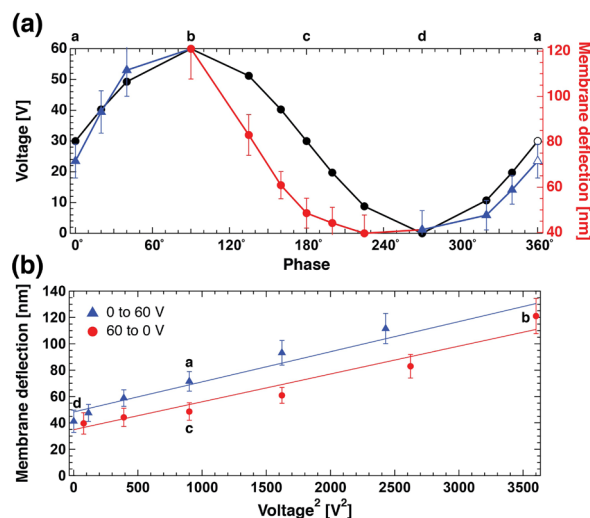
▲ Figure 1: Deflection profiles of gold membrane suspended over cavities, obtained via optical interferometry during 1 kHz AC actuation. Center deflections of this membrane over 83 cavities as functions of time were extracted from the profiles and averaged to yield a single deflection time function. That time function and corresponding applied voltage are plotted. (a) Applied voltage (black) and averaged peak membrane deflection (red and blue) are shown as functions of time. (b) Membrane deflections are plotted against square of applied voltage with time as a parameter. Points labeled a-b-c-d-a in (b) indicate position of corresponding points on the periodic deflection and voltage waveforms in (a).
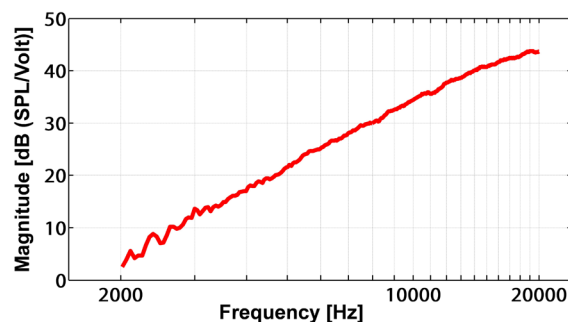
▲ Figure 2: Acoustic frequency response, from 2 kHz to 20 kHz, of a gold membrane microspeaker, 12.5 mm^2 in area. Magnitude of transfer function, $|T_{pv}|$, from driving voltage amplitude to sound output measured by the microphone is converted to decibels using 20 µPa as reference pressure, i.e., magnitude plotted is $20\log_{10}(|T_{pv}|/20\mu Pa)$.
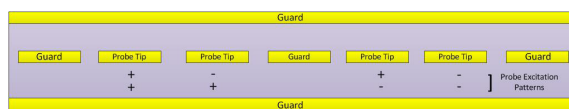
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Electromagnetic Imaging of Nanostructures

R. Kumar, T. Hamer, D. L. Trumper, J. H. Lang
Sponsorship: Lincoln Laboratory

This objective of this project is to develop a system to perform high bandwidth, subsurface, electromagnetic imaging of microfabricated devices. The intent is to simultaneously detect surface topologies, buried conductors/insulators, and doped regions. The proposed system promises to offer very high measurement bandwidth, enabling rapid measurement of large areas with high resolution which is critical to the time-efficient scanning of complex semiconductor wafers.
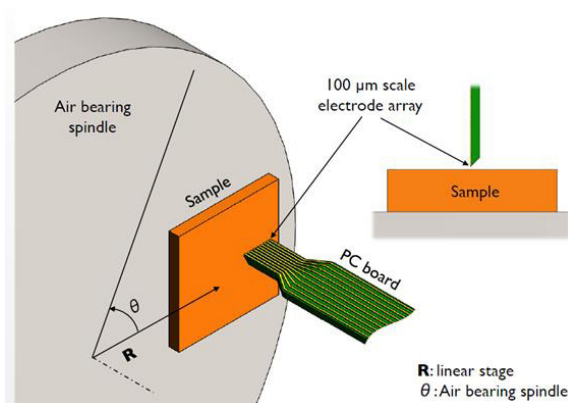
Our imaging approach is based on high-frequency impedance measurements through an array of electrodes capacitively coupled to a microfabricated device. As the electrode array is scanned over the device surface, the resulting impedance variations will be measured and transformed into a 3D tomographic map of the near-surface spatial distributions of the sample permittivity and conductivity. Also, nonlinearities in the current/voltage relationship of P-N junctions allow detection of the dopant boundaries by measuring the harmonic distortion. We plan to drive the electrodes with GHz excitation frequencies, and maintain the electrode array at a submicron flying height above the semiconductor surface. High excitation frequencies are necessary for the electric field generated from the sensor array to penetrate the silicon substrate in sufficient depth, thereby being coupled to the sub-surface features.

The imaging system will consist of a MEMS probe head, precision mechatronics, and RF electronics. The probe head will be fabricated from an array of gold electrodes that will be sandwiched between guard electrodes to prevent stray fields from interfering with the capacitance measurement; see Figure 1 for details. These probes will then fan out back to a vector network analyzer (VNA) which measures the impedance of each probe tip at high frequencies (0.5 GHz – 6 GHz). Different excitation patterns may applied from the VNA to the gold probes to control the depth of penetration of the electric fields into the nanostructure to be imaged. RF electronics will be used to mitigate losses at high frequencies while guarding against unwanted stray electric fields. Finally, an inversing imaging algorithm will be developed to compute a final image from the measured impedance data.

For the experimental setup, the test sample is mounted onto an air bearing spindle and the probe will be placed perpendicularly to the sample, as in Figure 2. Next, the spindle is rotated at a predefined angular velocity and the change in impedance, as the probe tip passes over the test sample, is measured by the RF equipment. After the data is collected, it is processed using the inverse imaging algorithm to output a map of the material composition of the test structure.

▲ Figure 1: Cut away, side view of MEMS probe head. Details the different excitation patterns applied to each probe tip and the placement of the guards to avoid interference of fringing fields.

▲ Figure 2: Diagram of the experimental setup detailing the placement of the probe head in relation to the sample.

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# Purification of High Salinity Brine by Multi-Stage Desalination via Ion Concentration Polarization (ICP)

B. Kim, V. S. Pham, J. Han
Sponsorship: ARPA-E

There is an increased need for the desalination of high concentration brine (> TDS 35,000ppm) efficiently and economically, either for the treatment of produced water from shale gas/oil development, or minimizing the environmental impact of brine from existing desalination plants. Although electro-membrane desalination (e.g., electrodialysis) has been underestimated and considered as a limited technology for brackish water treatment, we have found its multiple advantages for brine treatment. Based on our earlier works (Figure 1) showing better salt removal and energy efficiency than conventional electrodialysis (ED), we demonstrates technical and economic viability of ion concentration polarization (ICP) electrical desalination for the high saline water treatment by adopting a novel multi-stage operation. According to our analysis with a miniaturized microfluidic platform (Figure 2a), one can achieve competitive water cost (~$1/bbl) of highly concentrated brine desalination by optimizing the energy use by adopting the strategy of incremental, multi-stage salt removal in electrical desalination (Figure 2b). We also demonstrate that ICP desalination has the advantage of removing both salts and diverse suspended solids simultaneously, and of less susceptibility to membrane fouling/scaling, which is a significant challenge in any membrane processes.
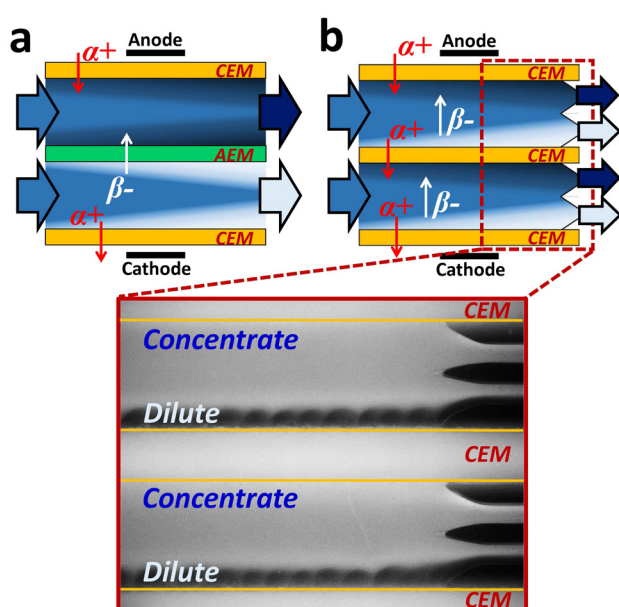
▲ Figure 1: Schematic view of electrical membrane desalination. (a) (ED) and (b) (ICP) desalination with fluorescent image. Red and white arrows indicate the movement of cation $\alpha+$ and anion $\beta-$ by electric field, respectively. Bright and dark regions in schematic figures represent ion-depleted and ion-enriched region, respectively; the fluorescent image shows an opposite contrast.
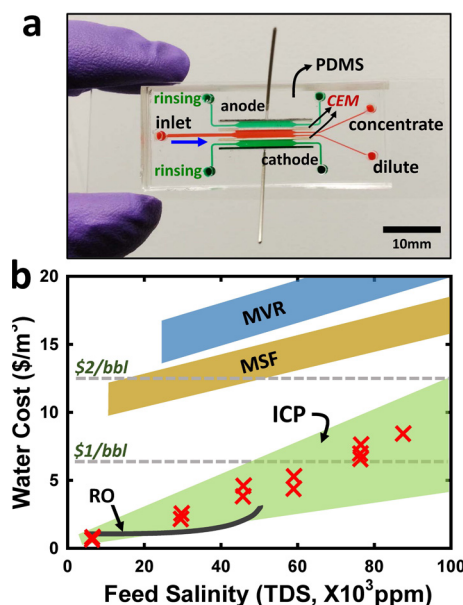
▲ Figure 2: (a) Photo of PDMS-based microfluidic ICP desalination device and (b) Cost analysis of ICP desalination. 12 red X denote results of ICP desalination based on the experiments with fixed recovery of 0.5 and 70-75% salt removal ratio from various feed salinity (5,800-87,700 mg/L of TDS, equivalent to 0.1-1.5M NaCl solution), where most flowback and some produced water range.

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# Enhanced Flow Boiling in Microchannels via Incorporated Surface Structures

Y. Y. Zhu, D. S. Antao, D. W. Bian, E. N. Wang
Sponsorship: Masdar Institute of Science and Technology, Battelle Memorial Institute, Air Force Office of Scientific Research

The increasing power densities in various electronic devices including concentrated photovoltaics, power electronics, and laser diodes pose significant thermal management challenges for the electronics industry. The use of two-phase microchannel heat sinks to cool high-performance electronic devices is attractive because they harness the latent heat of vaporization to dissipate high heat fluxes in a compact form factor. However, the challenges with such a scheme are associated with flow instability and the need to increase the critical heat flux (CHF), which is the highest heat flux the device is capable of dissipating before heat transfer failure.

Recently, incorporating micro/nanostructures onto the surfaces of the microchannels has opened up new opportunities for performance enhancement. Here we investigate the role of surface microstructures on flow boiling heat transfer in microchannels. We designed and fabricated microchannels with well-defined silicon micropillar arrays (heights of ~25 μm, diameters of 5-10 μm and pitches of 10-30 μm) on the bottom heated channel wall. The design decouples thin film evaporation and nucleation by promoting capillary flow on the bottom heated surface while facilitating nucleation from the sidewalls. The structured surface microchannels showed significantly reduced temperature and pressure drop fluctuation. Visualization of the flow indicates that the micropillar surface can promote capillary flow and enhance flow stability and heat transfer by maintaining a stable annular flow, which resulted in high-performance thin film evaporation and an enhanced critical heat flux. The fabricated devices achieved significantly enhanced heat transfer coefficient (40%) compared to that without micropillars, and a maximum CHF value of 720 W/cm² was achieved on a structured surface microchannel (diameters of 5 μm and pitches of 15 μm). The experimental results suggest that capillary flow can be maximized without introducing large viscous resistance when the microstructure geometry is optimized. This work is a first step towards guiding the design of stable, high-performance two-phase microchannel heat sinks.
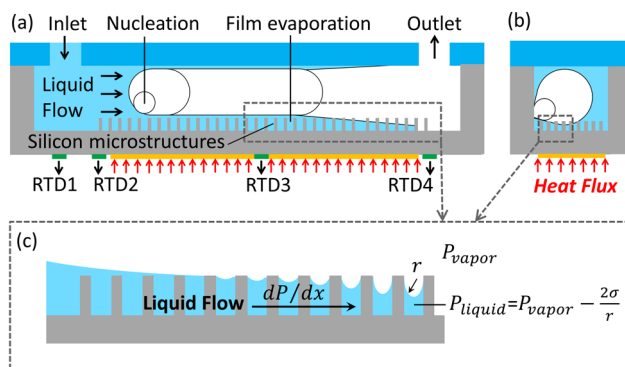
▲ Figure 1: Schematic of microchannel heat sink design with micropillars on the heated surface. (a) Side view, (b) cross-section view, and (c) magnified view of the liquid film forming menisci that create capillary pressure gradient to help drive the liquid flow. The equation that describes the liquid pressure under a meniscus is the Young-Laplace equation, where σ is the surface tension of the liquid, γ is the radius of curvature of the local meniscus, and P_{liquid} and P_{vapor} are the local pressure of the liquid and vapor, respectively.
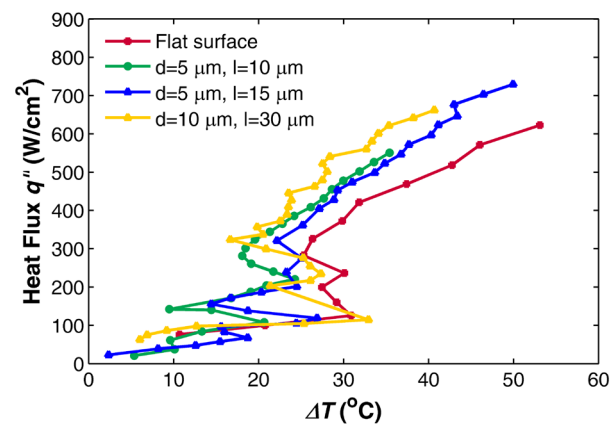
▲ Figure 2: Heat transfer performance characteristics of the microchannel. Heat flux q" vs. microchannel backside surface temperature rise ΔT. The maximum point on each curve indicates the critical heat flux, which is the highest heat flux the device is capable of dissipating before heat transfer failure. Error bars for q" were approximately ±1%. Error bars for ΔT were approximately ±3.5 °C for the structured devices and grew with the heat flux due to the increasing temperature oscillations (±3.5 °C to ±11 °C) for the smooth surface microchannel.

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Experimental Characterization of Thin-Film Evaporation from Silicon Micropillar Wicks

S. Adera, D. S. Antao, R. Raj, E. N. Wang
Sponsorship: Office of Naval Research with Mark Spector as program manager, National Science Foundation Graduate Research Fellowship Program

To the credit of Moore's Law, the exponential rise in the number of transistors in a single chip, the increase in clock speed and functionality, and the continual overall size reduction in device architecture of electronic devices have generated concentrated heat loads in excess of 100 W/cm². Furthermore, this heat flux is projected to exceed 300 W/cm² in a few years [1] creating a thermal management challenge. While enhanced air convection cooling strategies have done the job in the past, direct extension of the state-of-the-art air cooling technology is inadequate to remove heat loads in excess of 100 W/cm². As a result, novel thermal management solutions such as thin-film evaporation [2] that utilize the latent heat of vaporization as the working fluid changes phase from liquid to vapor are required to mitigate this thermal management challenge.

In this work, we have experimentally characterized thin-film evaporation from silicon micropillar wicks. The micropillars were created using contact photolithography and deep-reactive ion etching. For integrated testing and measurement, a thin-film heater and microsensors were incorporated using e-beam evaporation and acetone lift-off. The microsensors measure local temperature while the heater emulates the heat generated in electronic devices. The experiment was conducted in a vacuum chamber and de-ionized water was passively transported to the evaporator surface *via* capillary-wicking (Figure 1). The water was syphoned into the microstructured surface from the surrounding reservoir in response to the input heat flux. Steady state thin-film evaporation in the absence of nucleate boiling was demonstrated. The liquid meniscus recedes and the microstructured surface dries out when the capillary wicking mechanism cannot deliver sufficient liquid to sustain the evaporation by overcoming viscous losses. Dryout heat fluxes of ≈46 W/cm² were dissipated at 19°C superheat (Figure 2) over a 1cm×1cm microstructured area and the effects of micropillar wick geometry were captured through systematic study. Experimental results show that the dryout heat flux scales with micropillar wick thickness. Furthermore, for a given micropillar wick thickness, an optimum pillar diameter and spacing is identified which maximizes the capillary-limited evaporation dryout heat flux. Our study provides mechanistic understanding of the liquid transport and heat transfer processes of thin-film evaporation from well-defined micropillar wicks.
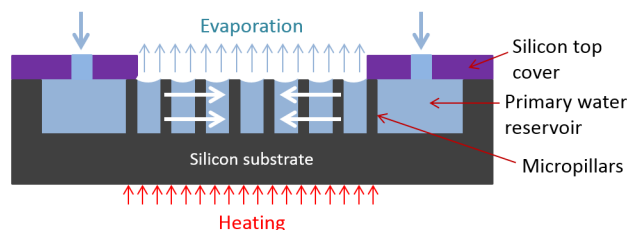
▲ Figure 1: Schematic of device concept. Variation in the liquid meniscus shape from edge of microstructured area to the center creates a pressure gradient that can be used for transporting liquid passively *via* capillary-wicking. Liquid is delivered to the microstructured area by overcoming the viscous loss. When the viscous loss exceeds the capillary pressure, a dry island is created at the center of the microstructured area which grows radially outwards. Liquid lost through evaporation from top liquid-vapor interface is replenished at the base of the micropillar wick.
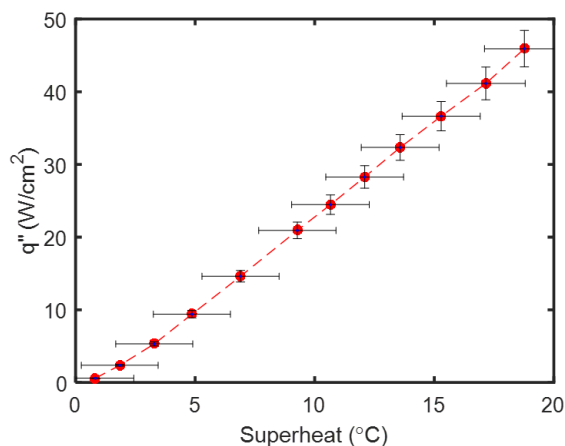
▲ Figure 2: Heat flux as a function of superheat. Last data point is the dryout heat flux beyond which the rate of evaporation exceeds the amount of water delivered *via* capillary-wicking.

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Elementary Framework for Cold Field Emission: Emission from Quantum-Confined Emitters

A. A. Patterson, A. I. Akinwande
Sponsorship: DARPA, National Science Foundation GRFP

Cold field emission is the emission of electrons from a metal at T=0K, induced by an electrostatic field. Field emitted current density (ECD) is traditionally predicted with the Fowler-Nordheim (FN) equation, which assumes a bulk, planar, metal emitter. Due to the enhancement of a static electric field at highly curved surfaces (lightning rod effect), the conventional strategy for increasing the ECD is to fabricate ever smaller and more highly-curved emitter tips. However, for suitably small field emitters, the effects of quantum confinement (QC) at the emitter tip may play a significant role in determining the total ECD since the specific shape of a quantum system determines the its electronic wave functions and distribution of energy levels. In order to study the competing effects of a reduced electron supply due to QC and increased electron transmission probability from local field enhancement, our previously developed elementary framework for cold field emission has been reformulated to treat emission from non-planar surfaces of QC metal emitters.

The framework was employed to derive ECD equations for emission from the planar surface of a normally unconfined (NU) 1D cylindrical nanowire (CNW) and the curved side of a normally confined (NC) 1D CNW, which are illustrated in Figure 1. The energy level spacing, energy level degeneracy, and transverse zero-point energy unique to each emitter geometry led to certain geometries producing larger ECDs than others under equivalent conditions. The close energy level spacing and lack of a transverse zero-point energy in the NC CNW geometry led to exceptionally large ECD peaks, an average ECD that exceeded the FN limit at typical values of E_F, and an increasing trend in the ECD with decreasing emitter dimensions in the presence of field enhancement, which is shown in Figure 2. These results suggest that highly curved emitter geometries may be ideal for emission from the standpoint of not only tip electrostatics, but also the electron supply. Current work includes the application of the framework to more realistic emitter tip geometries, such as paraboloids, and the development of an analogous framework for emission from non-planar, quantum-confined semiconductor emitters.
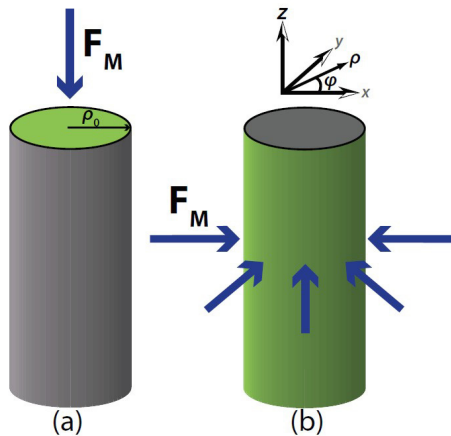
▲ Figure 1: Emission from a (a) normally unconfined 1D cylindrical nanowire emitter and a (b) normally confined 1D cylindrical nanowire emitter. ρ_0 is the emitter radius, F_M is the applied electric field, and e^- are the emitted electrons.
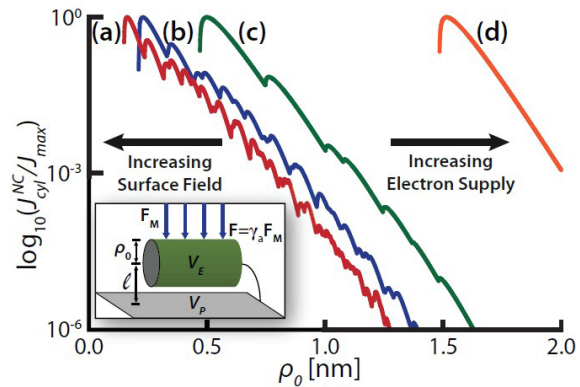
▲ Figure 2: In the presence of local field enhancement, the normalized ECD from the NC CNW emitter J^{NC}_{cyl}/J_{max} increases as a function of decreasing emitter radius ρ_0, for Fermi energy values of (a) 10 eV, (b) 5 eV, (c) 1 eV, and (d) 0.1 eV. The increasing electric field at the emitter surface increases electron transmission probability more rapidly than QC reduces the spatial density of electrons available to tunnel as ρ_0 decreases.

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# High-Throughput Manufacturing of Nanofibers using Planar Arrays of Microfabricated Externally Fed Emitters

P. J. Ponce de Leon, F. A. Hill, L. F. Velásquez-García
Sponsorship: DARPA

Electrohydrodynamic jetting occurs when a strong electric field is applied to the free surface of a conductive liquid; the process can uniformly produce ion plumes, fine aerosol droplets, or continuous fibers with submicron diameters, i.e., nanofibers, depending on the properties of the liquid used and the ionization conditions. Nanofabrication via electrohydrodynamic jetting has received attention as a promising candidate for production of nanostructures because of its ability to create nano-thick films of high quality at lower temperature than standard solid-state processing. A key advantage of electrospinning, i.e., electrohydrodynamic jetting of nanofibers, over other fiber generation methods is its versatility in producing fibers of arbitrary length from a range of materials including polymers, metals, ceramics, and semiconductors. The applications of electrospun nanofibers include dye-sensitized solar cells, scaffolds for tissue engineering, electrodes for ultracapacitors, and separation membranes.

We created a technology for high-throughput generation of polymer nanofibers using planar arrays of microfabricated externally fed electrospinning emitters. Devices with emitter density as high as 25 emitters/cm^2 (Figure 1) deposit uniform imprints comprising fibers with diameters on the order of a few hundred nanometers using solutions of dissolved polyethylene oxide in water and ethanol as working fluid (Figure 2). We measured mass flux rates as high as 417 g/hr/m^2, i.e., 4x the reported production rate of leading commercial free-surface electrospinning sources. Throughput increases with increasing array size at constant emitter density, showing that the design can be scaled up with no loss of productivity. The largest measured mass flux resulted from arrays with larger emitter separation operating at larger bias voltages, indicating the strong influence of electrical field enhancement on the performance of the devices. Inclusion of a ground electrode surrounding the array tips helps control the spread of the imprints over large distances.
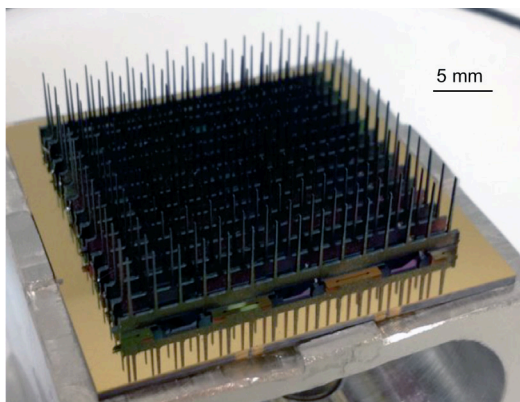
▲ Figure 1: An array of 15×15 externally fed electrospinning emitters (25 emitters/cm^2). From P. Ponce de Leon et al., Nanotechnology, vol. 26, no. 22, 225301 (10 pp.), June 2015.
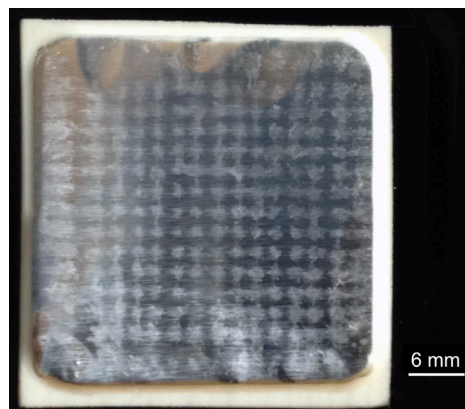
▲ Figure 2: Collector imprints from an array of 225 emitters (25 emitters/cm^2). From P. Ponce de Leon et al., Nanotechnology, vol. 26, no. 22, 225301 (10 pp.), June 2015.

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Optimization of the Morphology of Arrays of Nano-Sharp, Photon-Triggered Silicon Field Emitters to Maximize their Total Current Emission

C. D. Dong, M. E. Swanwick, P. D. Keathley, F. X. Kärtner, L. F. Velásquez-García
Sponsorship: DARPA

Femtosecond ultrabright cathodes with spatially structured emission are a critical technology for applications such as free-electron lasers, tabletop coherent x-ray sources, and ultrafast imaging. State-of-the-art UV photocathodes have several disadvantages: (i) they need to be fabricated, stored, and operated in ultra-high vacuum and (ii) producing high current pulses reduces their lifetime due to the rapid degradation of the low workfunction material. Cathodes based on photon-triggered field emission, i.e., tunneling of electrons due to the interaction of high-intensity optical pulses with field enhancing structures, are a promising technology to bypass these shortcomings. We recently reported batch-fabricated photon-triggered field emission cathodes composed of massively multiplexed arrays of nano-sharp high-aspect-ratio silicon pillars; the devices are made using standard complementary metal-oxide semiconductor batch fabrication processes, are stored at atmospheric conditions, and can be operated at lower vacuum levels than standard photocathodes with no degradation. The devices are capable of pC-level emission with multi-kHz repetition, greatly increasing the total emitted charge per pulse compared to single-emitter sources. Through experiment and simulations, this work explores the optimization of the total electron yield of ultrafast photon-triggered field emission cathodes composed of arrays of nanosharp, high-aspect-ratio, single-crystal silicon pillars by varying the emitter pitch and height.

Arrays of 6-nm-tip-radius silicon emitters with emitter densities between 1.2 and 73.9 million tips.cm^{-2} and emitter height between 2.0 µm and 8.5 µm were characterized using 35-fs 800-nm laser pulses (Figure 1). Of the devices tested, the arrays with emitter pitch equal to 2.5 µm produced the highest total electron yield; arrays with larger emitter pitch suffer area sub-utilization; and in devices with smaller emitter pitch, the larger emitter density does not compensate for the smaller per-emitter current due to the electric field shadowing that results from the proximity of the adjacent tips (Figure 2). Experimental data and simulations suggest that 2-µm-tall emitters achieve practical optimal performance as shorter emitters have visibly smaller field factors due to the proximity of the emitter tip to the substrate, and taller emitters show marginal improvement in the electron yield at the expense of greater fabrication difficulty.
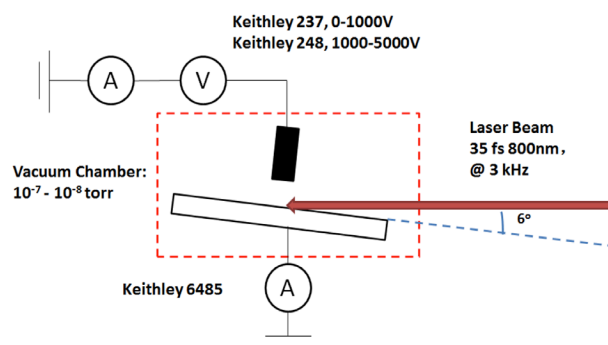
▲ Figure 1: Schematic of the experimental apparatus used to characterize the photon-triggered silicon field emitter arrays.
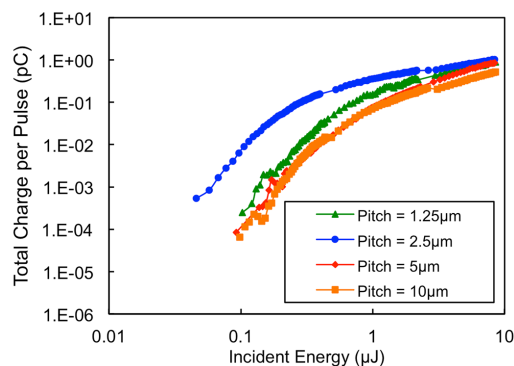
▲ Figure 2: Total emitted charge per pulse vs. incident laser pulse energy for devices with emitter pitch equal to 1.25 µm, 2.5 µm, 5 µm, and 10 µm and emitter height equal to 8.5 µm. From C. Dong et al., Nanotechnology, vol. 26, no. 26, 265202 (11pp), 2015.

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# Advanced X-Ray Sources for Absorption Imaging of Low-Z Materials

A. Basu, M. E. Swanwick, A. A. Fomani, L. F. Velásquez-García
Sponsorship: DARPA

X-rays are widely used in applications such as healthcare, airport security, crystallography, spectroscopy, and microfabrication. The development of miniaturized X-ray sources could satisfy applications where the target areas are small or where the smaller dimensions and lighter weight of the X-ray source enable desirable capabilities such as portability. For example, compact X-ray sources can revolutionize computerized tomography (CT) by making possible the implementation of a system with multiple X-ray sources that provides a wide range of information without the need to implement a rotating gantry.

A field emission cathode is an attractive alternative to a conventional thermionic cathode as an electron source in a portable X-ray source because of the lower vacuum it requires to operate, its faster response, and its resilience to traces of reactive gases. Field emission cathodes use high-surface electric fields on the emitter tip surface to narrow the potential barrier that traps electrons in the material, allowing electrons to quantum tunnel into vacuum. Miniaturization and multiplexing of field emitters result in nanostructured field-emitter arrays capable of high-current emission at a low (< 150 V) voltage. The field emitters used in our X-ray source are capable of generating mA-level dc currents even when operated continuously for many hours. High-current cathodes make it possible to capture images in a short time, which helps to reduce any blurriness of the image due to movement of the sample. X-rays generated from a target anode can be catego-rized as either bremsstrahlung or fluorescent. On the one hand, bremsstrahlung X-rays span the entire energy range of the bombarding electrons with the maximum energy being determined by the voltage applied to the anode. On the other hand, fluorescent X-rays are characteristic of the target material and appear as specific sharp peaks in the X-ray spectrum. While bremsstrahlung X-rays give rise to low-contrast polychromatic images, fluorescent X-rays could be used to produce quasi-monochromatic, high-contrast images.

For over four years our group has developed advanced field-emission-enabled, near-monochromatic X-ray sources capable of imaging soft tissue structures. Our latest development is a portable X-ray source (200 cm^3 chamber size) with a reflection anode composed of a copper rod coated with a molybdenum thin film and a field emission cathode (Figure 1). A 25 l/s portable ion pump keeps the chamber base pressure at approximately 10^{-8} Torr. At an anode bias voltage of 35 kV, the X-ray source maximizes the percentage of photons with 17.8 keV, which corresponds to the Kα peak of Mo; these X-rays are energetic enough to go through air without significant attenuation (~95% transmission) but are of low-enough energy to generate high-contrast absorption images when interacting with soft tissue. Using the X-ray source, we obtained absorption images of ex-vivo samples captured on a CsI scintillator operated in fluoroscopic mode (Figure 2). Features as low as 160 µm were visible in the images.
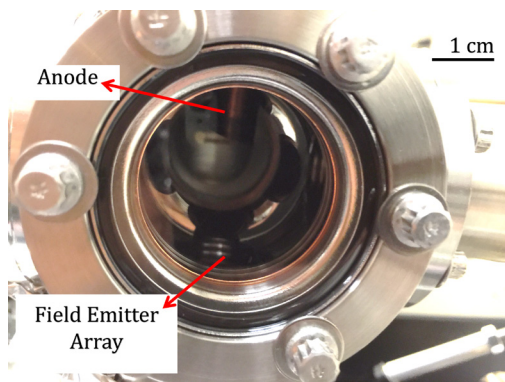
▲ Figure 1: The inside of the X-ray chamber as seen through a glass port. The field emitter array is hidden from view
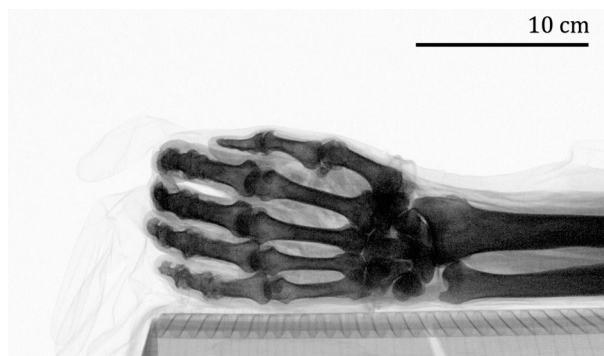
▲ Figure 2: Absorption X-ray image of ex vivo human hand captured with anode bias voltage equal to 35 kV and cathode current of 250 µA for 60 seconds of exposure time.

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A Field Emission-Based Ultra-High Vacuum Pump for Cold-Atom Interferometry Systems

A. Basu, M. A. Perez (ColdQuanta, Inc.), L. F. Velásquez-García
Sponsorship: DARPA

The discovery of magneto-optical trapping of alkali metal vapors in the late 1980s generated a strong interest in developing miniaturized atomic clocks and sensors based on cold alkali atom interferometry. Chip-scale, high-precision atomic sensors can be used in a great variety of exciting applications including fundamental scientific discovery (e.g., general relativity and geophysics), inertial navigation (e.g., gyroscopes and accelerometers), and geological survey (e.g., magnetometers and gravimeters). Cold-atom interferometry needs ultra-high vacuum (UHV, pressure < 10^{-9} Torr) to operate; therefore, portable cold-atom sensors require miniaturized UHV pump technology compatible with alkali vapor that operates at low power. Standard UHV ion pumps, which use high magnetic fields to increase the ionization probability, are not ideal to maintain vacuum in a chip-scale atomic sensor because the intensity of the magnetic field increases with the reduction in size of the pump and because the magnetic field of the pump can alter the quantum states of the laser-cooled atoms, leading to incorrect measurements. A better alternative is to use an electron source to provide a surplus of electrons to increase the ionization probability, eliminating the need for a magnetic field. A field emission electron source is a good choice for that because, unlike state-of-the-art thermionic cathodes, they do not require high temperature to operate, which makes them compatible with the reactive alkali environment inside atomic vapor cells.

We preliminarily demonstrated a magnetic-less ion pump design (Figure 1) that uses field electron emission to create a self-sustained plasma within a 200 cm³ vacuum chamber. A silicon-based, nanostructured, self-aligned, gated field emitter array (FEA) is used as electron source. Two electrodes, both consisting of structural rings wrapped with titanium wire, are placed above the FEA and biased at voltages that enable collection of either electrons or ions. The ion collector is the getter of the pump, capturing the ions both physically (bombardment) and chemically (chemisorption). The apparatus has a rubidium dispenser for releasing the alkali metal vapor inside the chamber, and the chamber is connected to an external pump system capable of maintaining a base pressure of ~10^{-8} Torr within the chamber. The performance of the field emission cathode did not deteriorate due to the presence of Rb at pressures as high as 7×10^{-6} Torr. The pump performance is shown in Figure 2. An initial rise in pressure (due to electron scrubbing) was followed by a 25% drop in pressure (from 4.0×10^{-7} Torr to 3.0×10^{-7} Torr) when the ion current was increased from 0 to 0.5 nA (by increasing the bias on the negatively charged ion collector). Current work focuses on the optimization of the electron impact ionization process to improve pumping performance.
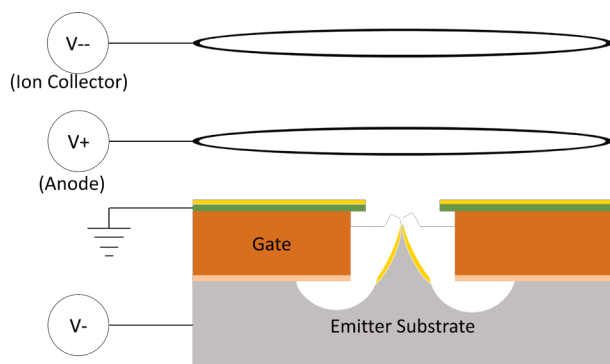
▲ Figure 1: Schematic of the pump architecture. The FEA is represented by a single emitter tip; the anode and ion collectors are ring-shaped structures.
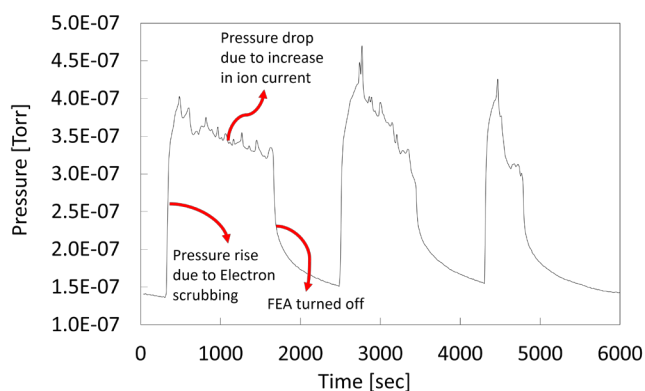
▲ Figure 2: Chamber pressure vs. time. From "Nanostructured Silicon Field Emitter Array-Based High-Vacuum Magnetic-Less Ion Pump for Miniaturized Atomic Spectroscopy Sensors," *Transducers 2015*, Anchorage AK, June 2015.

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Biological, Medical Devices and Systems

**Biological, Medical Devices and Systems**

A Portable Bioimpedance Spectroscopy Measurement System for Congestive Heart Failure Management

M. Delano, C. G. Sodini
Sponsorship: Medical Electronic Device Realization Center, Analog Devices

An estimated five million people are currently diagnosed with congestive heart failure (CHF) in the United States, with over 400,000 new diagnoses annually. Almost one in two patients will be readmitted to the hospital within four to six months of discharge. Readmissions can occur when the patient becomes fluid-overloaded due to poor medication and/or diet compliance, among other reasons. Up to 50% of these early re-admissions may be prevented if symptoms are recognized early enough and medication and diet compliance improve.

CHF is frequently associated with significant fluid retention in the lungs and legs. Bioimpedance techniques can be used to estimate the fluid levels in a patient non-invasively. These measurements have been shown to be predictive of heart failure decompensation up to 14 days before an event occurs We have developed a portable bioimpedance system that can measure body impedance from 1 kHz to 1 MHz. The system uses the magnitude-ratio and phase-difference detection (MRPDD) method to calculate the magnitude and phase of the measured impedance (see Figure 1). The system is enclosed in aluminum box (see Figure 2) and can be used with four co-axial cables. Each co-axial cable is actively driven by a screen driver circuit that reduces stray capacitance from the cables. Data from the device can be sent directly to a computer or transmitted over bluetooth (with lid off). The device has been characterized with RC networks and is being validated in healthy volunteers.
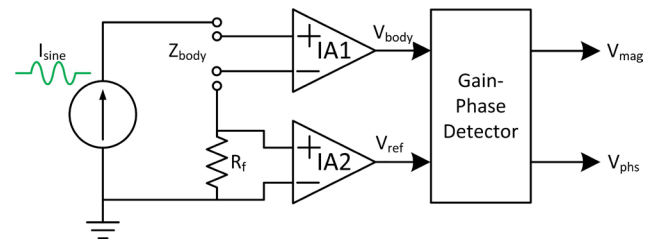
▲ Figure 1: A schematic overview of the MRPDD method. A fixed sinusoidal current is driven through the body and a sense resistor The voltage is amplified and measured by a Gain-Phase Detector chip (AD8302).
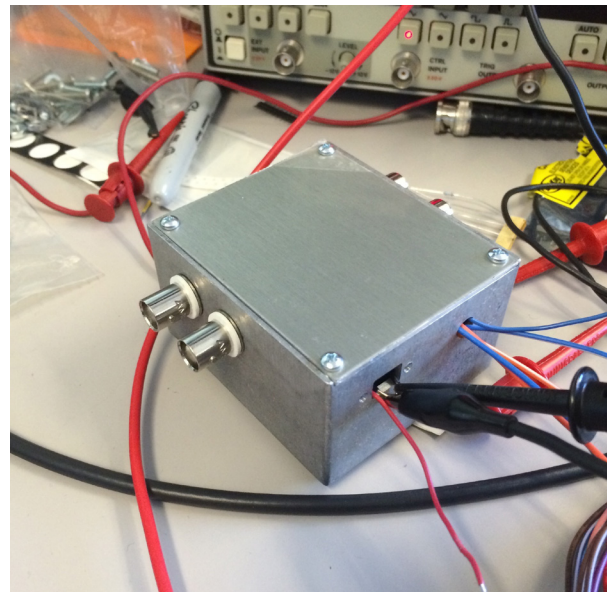
▲ Figure 2: The portable bioimpedance spectroscopy measurement system inside the enclosure.

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Subdermal Implantable EEG Recorder and Seizure Detector

B. Do Valle, C. G. Sodini
Sponsorship: Center for Integrated Circuits and Systems

Epilepsy is a common chronic neurological disorder that affects about 1% of the world population. Although electroencephalogram (EEG) has been the chief modality in the diagnosis and treatment of epileptic disorders for more than half a century, long-term recordings (more than a few days) can be obtained only in hospital settings. Many patients, however, have intermittent seizures occurring far less frequently. Patients cannot come into the hospital for weeks in order for a seizure to be captured on EEG—a necessary prerequisite for making a definitive diagnosis, tailoring therapy, or even establishing the true rate of seizures.

This work aims to address this need by proposing a subdermal, implantable, eight-channel EEG recorder and seizure detector. The system will be implanted behind the patient's ear, as shown in Figure 1. It has two modes of operation: diagnosis and seizure counting. In the diagnosis mode, EEG is continuously recorded and transmitted to an external device. In the seizure-counting mode, the system uses a novel low-power algorithm to track the number of seizures a patient has over a given time period, providing doctors with a reliable count to help determine medication efficacy. This mode is especially important given the severity of antiepileptic drugs' side-effects.

An application-specific integrated circuit (ASIC) that implements the EEG recording and seizure detection algorithm was designed and fabricated in a 0.18 µm CMOS process. The ASIC, shown in Figure 2, includes eight EEG channels and was designed to minimize the system's power and size. The result is a power-efficient analog front end that requires 2.75 µW per channel in diagnosis mode and 0.84 µW per channel in seizure-counting mode. Both modes have an input referred noise of approximately 1.1 µVrms. The seizure detection algorithm has a sensitivity of 98.5%, a false alarm rate of 4.4 per hour, and a detection delay of 9.1 seconds. It consumes only 0.45 µW, which is over an order of magnitude less power than comparable algorithms.
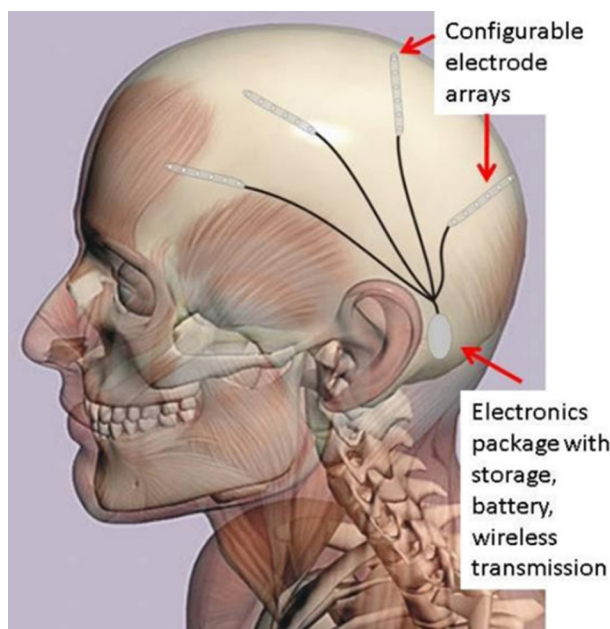
▲ Figure 1: Implanted EEG system showing the location of the electronic package and electrodes.
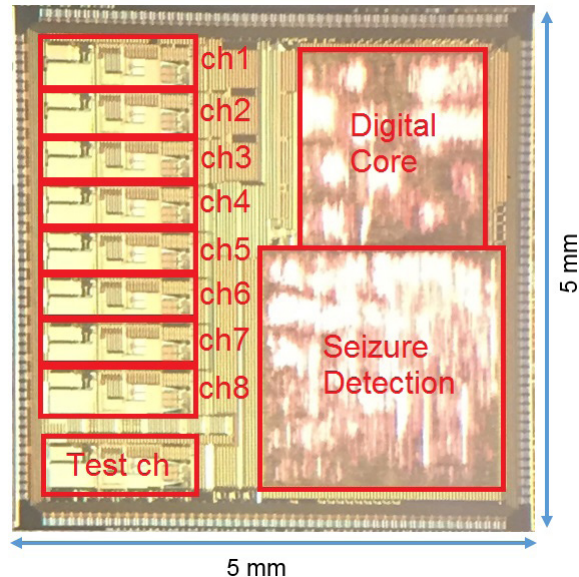
▲ Figure 2: Die micrograph of the ASIC with circuit blocks labeled.

Continuous and Non-Invasive Blood Pressure Monitoring using Ultrasound

J. Seo, H.-S. Lee, C. G. Sodini
Sponsorship: Samsung Fellowship, Center for Integrated Circuits and Systems

An arterial blood pressure (ABP) waveform provides valuable information for treating cardiovascular diseases. The ABP waveform is usually obtained through a pressure transducer connected to an arterial catheter. Although this method is considered the gold standard, its disadvantage is invasive nature. The invasive nature not only increases various patients' risks but makes the usage of the ABP waveform for cardiovascular studies expensive. Therefore, reliable non-invasive ABP waveform estimation has been desired for a long time by medical communities. In that sense, medical ultrasound is an attractive imaging modality because it is inexpensive, free of radiation, cuff-less, and suitable for portable system implementation.

The proposed ultrasonic ABP monitoring is achieved by observing the pulsatile change of the cross-sectional area and identifying the elastic property of the arterial vessel, represented by the pulse wave velocity (PWV, the propagation speed of a pressure wave along an arterial

tree) with a diastolic blood pressure measurement as a baseline. The PWV can be estimated by obtaining a flow-area plot and then measuring the slope of a linear part in the flow-area plot during a reflection-free period (e.g., the early systolic stage).

A prototype ultrasound device is designed to obtain both a blood flow waveform and a diameter waveform simultaneously to implement the proposed technique, shown in Figure 1. Clinical testing was conducted on nine healthy human subjects to demonstrate the feasibility of the proposed technique, which was previously tested in a phantom setup. Figure 2 presents a pressure waveform comparison between an ABP waveform obtained at a left middle finger and an estimated ABP waveform at the left common carotid artery from this method. The comparison shows good agreement although some degree of discrepancy is expected due to different measurement sites.
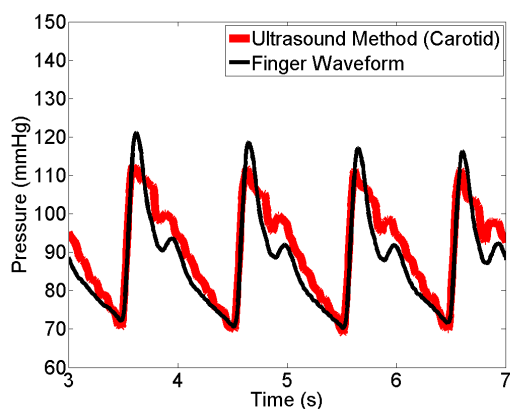
▲ Figure 1: A prototype PCB board design. The board drives ultrasound transducers, receives echoes, and process the voltage signal to implement the proposed method. The board is capable of streaming data to the PC over USB 2.0 interface with sufficient data rate for real-time data acquisition. The device has a portable form factor (14.7 cm×13.2 cm).
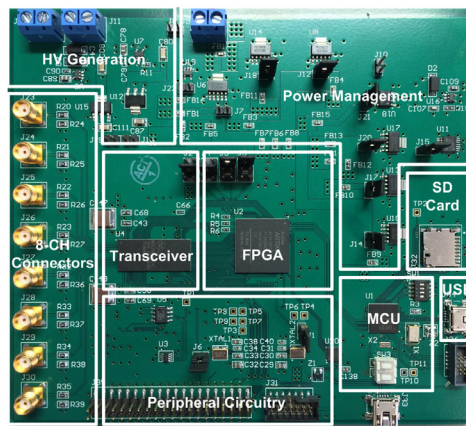
▲ Figure 2: Comparison of two blood pressure waveforms assuming diastolic blood pressures are constant over major arteries. An estimated carotid ABP waveform shows less augmented shape than the finger waveform as the finger waveform is more affected by pressure wave reflection from peripheries.

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Body-Coupled Communication and Implants

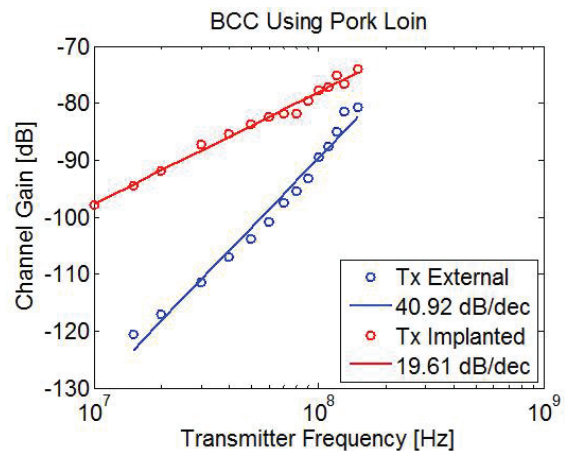G. S. Anderson, C. G. Sodini
Sponsorship: Google

Body-coupled communication (BCC) is achieved by creating a potential difference in one area of the body and sensing the resulting attenuated potential difference in another area of the body. To do this, the transmitter and receiver each have two electrodes that electrically connect to the body's conductive tissues beneath the epidermis. These connections can be formed either capacitively or galvanically. A capacitive link consists of the electrode forming one plate of a parallel plate capacitor while the conductive tissues form the other plate. A galvanic link is formed by directly putting the electrode or wire in the conductive tissue.

For an implant to communicate to a device outside the body using BCC, the channel utilizes both galvanic and capacitive links (capacitive for the device outside the body and galvanic for the implant). To test if this is possible a pork loin was used to simulate the conductive tissue of the body (see Figure 1). First, both the transmitter's and receiver's electrodes were connected to the pork loin using cardboard spacers between the pork loin and the electrodes, ensuring that both the transmitter and receiver would be capacitively coupled to the conductive tissue in the pork loin. Next the transmitter's output was connected to two alligator clips that were inserted into the pork-loin while the receiver was connected capacitively as before. This configuration simulates an implanted transmitter that is galvanically coupled to the conductive tissue, communicating with a receiver that is capacitively coupled. The results, shown in Figure 2, validate the predictions of the body model detailed in the further reading below.

▲ Figure 1: A setup to test implants talking to devices outside the body using BCC.

▲ Figure 2: BCC channel measurements.

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Development of a Transcranial Doppler Ultrasound System

S. J. Pietrangelo, H.-S. Lee, C. G. Sodini
Sponsorship: MEDRC, Maxim Integrated

The central objective of critical care for patients affected by traumatic brain injury (TBI), cerebrovascular accident (i.e., stroke), and other neurovascular pathologies is to monitor patient state and provide suitable medical intervention to mitigate secondary injury and aid in recovery. Transcranial Doppler (TCD) sonography is a specialized Doppler ultrasound technique that allows characterization of blood flow from the basal intracerebral vessels. While several non-invasive cerebrovascular diagnostic modalities exist, including positron emission tomography (PET), computed tomography (CT), and magnetic resonance angiography (MRA), the use of TCD sonography is highly compelling for certain diagnostic needs due to its safety in prolonged studies, high temporal resolution, modest capital equipment costs, and relative portability.

Despite a growing list of potential diagnostic applications, several constraints – notably operator dependent measurement results, bulky instrumentation, and the need for manual vessel location – have generally confined the use of TCD ultrasound to highly-specific clinical environments (e.g., neurocritical care units and vascular laboratories). This project seeks to develop a low-power miniaturized TCD ultrasound system for measuring blood flow velocity at the middle cerebral artery (MCA) in support of continuous cerebrovascular monitoring.

The TCD ultrasound system shown in Figure 1 employs multi-channel transceiver electronics and a two-dimensional transducer array to enable steering of the ultrasound beam. Electronic beamformation allows for algorithmic vessel location and tracking, thereby obviating the need for manual transducer alignment and operator expertise. Figure 2 illustrates a conceptual TCD system for wearable, autonomous monitoring of cerebrovascular state.

▲ Figure 1: TCD ultrasound electronics and transducer array.
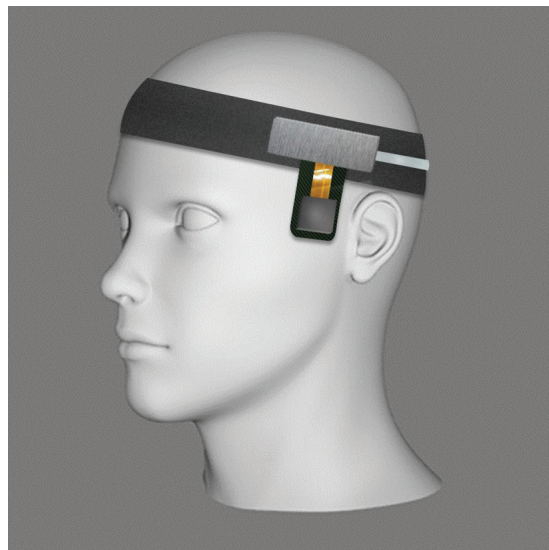
▲ Figure 2: Concept of a wearable TCD monitoring system with integrated ultrasound electronics.

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Stretchable Touch and Finger Position Sensors Molded into a Cloth Glove

M. D'Asaro, V. Bulović, J. H. Lang
Sponsorship: National Science Foundation Engineering Research Center for Sensorimotor Neural Engineering

The NSF Center for Sensorimotor Neural Engineering (CSNE) is working to reanimate a paralyzed human hand by recording and decoding motor intent from electrodes implanted in the brain and driving a spinal cord stimulator to induce the intended hand motion. To receive sensory feedback the user will wear a glove with integrated pressure and shear sensors, the data from which will be used to drive another set of implanted electrodes. This work aims to create a suitable sensing glove.

The glove will have pressure and shear sensors in the fingertips to restore the user's sense of touch plus finger position sensors to restore the user's intuition of finger position. For such a glove to be comfortable, the sensors and interconnects need to be small and compliant (flexible and stretchable). The sensors also need to be durable yet inexpensive to manufacture and replace when the glove wears out. To meet these requirements, sensors made from silicone rubber (PDMS) doped with carbon black (CB) are being explored. CB/PDMS is an inexpensive flexible and stretchable "smart material" that responds to mechanical deformation by increasing in resistance, thus forming a sensor. Fingertip pressure is sensed with a disk of CB/PDMS in the middle of the fingertip while finger curling is measured with a strip of CB/PDMS along the back of the finger, as in Figure 1. To electrically connect to the sensing CB/PDMS, a higher concentration CB/PDMS with added ~5 μm silver particles is used as a stretchable strain-insensitive conductor. Both materials can be molded directly into the nylon fabric of a commercial glove and adhere well.

Testing results from the pressure sensor are shown in Figure 2. Qualitative results from the finger curl sensor are encouraging. CB/PDMS shear sensors have been fabricated and tested but not yet integrated into a glove.
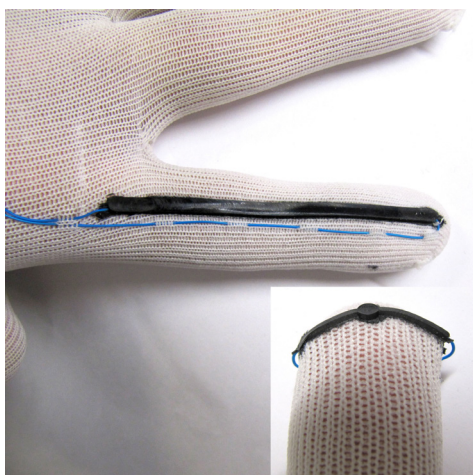
▲ Figure 1: Nylon glove with stretchable finger flex sensor molded into the back of the index finger. The inset shows a fingertip pressure sensor made with the same technology.
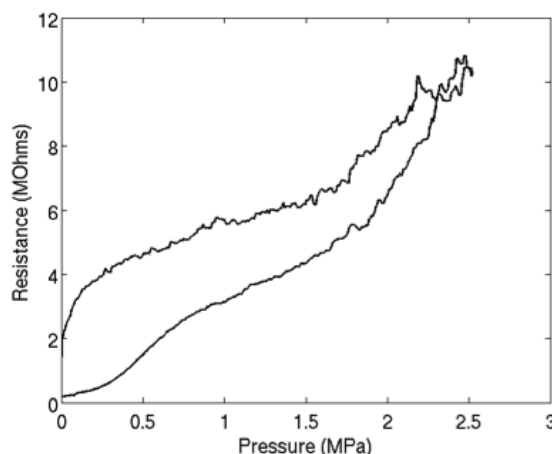
▲ Figure 2: Resistance of the fingertip pressure sensor versus applied pressure. The device is very sensitive, if hysteretic and nonlinear.

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Piezoelectric Micro-machined Ultrasonic Transducer Array for Medical Imaging

K. M. Smyth, C. G. Sodini, S.-G. Kim
Sponsorship: Medical Electronic Device Realization Center, Analog Devices

Diagnostic medical ultrasound imaging is becoming increasingly widespread because it is relatively inexpensive, portable, compact, and non-invasive compared to other diagnostic scanning techniques. However, commercial realization of advanced imaging trends will require cost-effective, large-scale arrays of miniaturized elements, which are expensive to fabricate with the current bulk piezoelectric transducers. At high volume, micro-fabricated transducers based on micro-electromechanical (MEMS) technology are an array-compatible and low-cost option.

The piezoelectric micro-machined ultrasonic transducer (pMUT) is a promising alternative to previously proposed capacitive MUT devices since it does not suffer from electrostatic transduction limitations, including potentially unsafe high bias voltage, and non-linearity. With more effective transformation via the piezoelectric effect, pMUTs have already demonstrated viability for deep penetration imaging via high acoustic pressure output. However, insufficient modeling has produced pMUT devices that often fall short of predictions, resulting in low electromechanical coupling and reduced bandwidth. With an improved modelling framework and optimization, pMUT based arrays have the potential for efficient low-power, high-pressure operation necessary for wearable applications.

Based on a high force output figure of merit, a 31-mode, lead zirconate titanate (PZT) -based pMUT plate cell design is selected. Our previous work developed and validated an analytical, electro-acoustic model of the single cell through experiment and finite element simulation. By leveraging and building on the validated single-cell model, we further optimized parallelized multi-cell elements to achieve high acoustic power and power efficiency. These elements are incorporated into 1D arrays (Figure 1) to demonstrate basic beamforming and image collection capabilities of a pMUT-based ultrasound system.

Current work focuses on fabrication of the pMUT arrays (Figure 2) using common micro-fabrication techniques including a PZT sol-gel deposition process. Work on model scaling to larger multi-cell systems and implementation of supporting electrical drive and receive circuits is also ongoing.
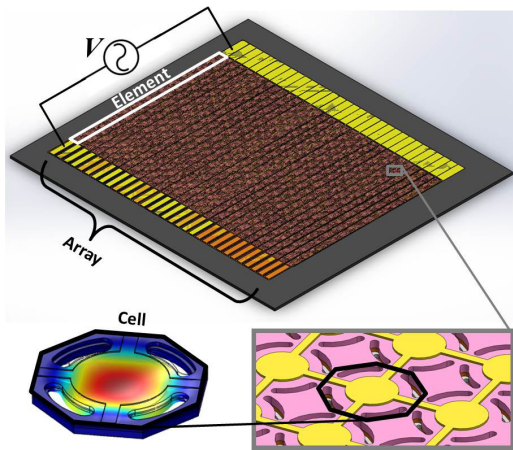
▲ Figure 1: Rendering of 1D pMUT array (top) where each element consists of many small pMUT cells (bottom right). Deflection of single cell based on piezo-acoustic finite element model simulated in COMSOL (bottom left).
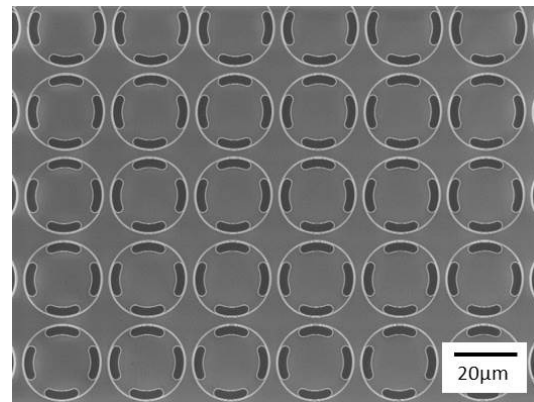
▲ Figure 2: Scanning electron microscope image of partially completed pMUT cells currently undergoing fabrication.

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Weighing Nanoparticles in Solution at the Attogram Scale

S. Olcum, N. Cermak, S. C. Wasserman, K. S. Christine, H. Atsumi, K. R. Payer, W. Shen, J. Lee, A. M. Belcher, S. N. Bhatia, S. R. Manalis
Sponsorship: ARO, CIMIT

Physical characterization of nanoparticles is required for a wide range of applications. Nanomechanical resonators can quantify the mass of individual particles with detection limits down to a single atom in vacuum. However, applications are limited because performance is severely degraded in solution. Suspended nanochannel resonators (SNRs) have opened up the possibility of achieving vacuum-level precision for samples in the aqueous environment, and a noise equivalent mass resolution of 27 attograms in 1-kHz bandwidth was previously achieved. We report on a series of advancements that have improved the resolution by more than 30-fold, to 0.85 attograms in the same bandwidth, approaching the thermomechanical noise limit and enabling precise quantification of particles down to 10 nm with a throughput of more than 18,000 particles per hour (Figure 1). We demonstrate the potential of this capability by comparing the mass distributions of exosomes produced by different cell types (Figure 2) and by characterizing the yield of self-assembled DNA nanoparticle structures.
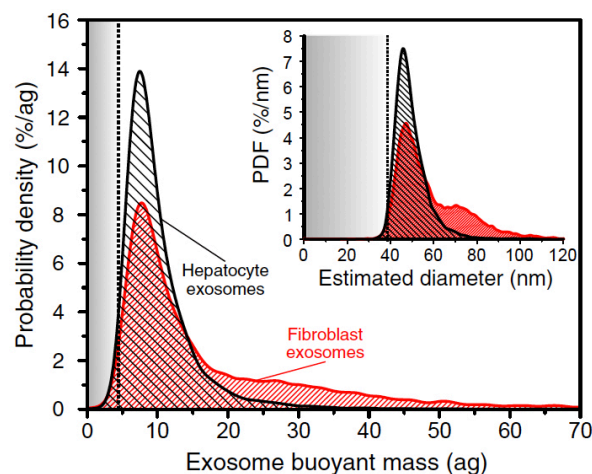
▲ Figure 1: Simplified schematic of SNR system; a positive-feedback loop keeps SNR in oscillation. An optical lever detects cantilever deflection, a photodetector circuit converts laser deflection to a voltage signal, a field programmable gate array (FPGA) delays the photodetector signal while also measuring oscillation frequency, and an amplifier drives the integrated piezoceramic actuator with the FPGA signal. Delay and oscillation amplitude are controlled by the FPGA to achieve minimum frequency noise. An oven-controlled crystal oscillator is used as clock source for the FPGA.
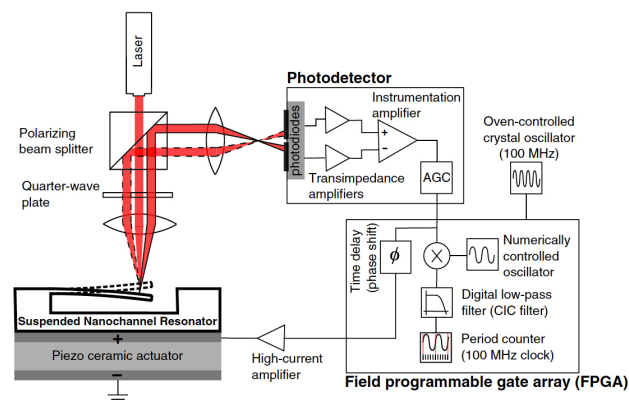
▲ Figure 2: Buoyant mass measurements of exosomes derived from different cell types. Buoyant mass distributions (kernel density estimates) of fibroblast-derived (red) and hepatocyte-derived (black) exosomal vesicles. Some 7,100 fibroblast exosomes and 9,600 hepatocyte exosomes are weighed using SNR in 65-min and 76-min experiments, respectively. Vertical dotted line depicts limit of detection as close to 5 ag. (Inset) Estimation of exosome diameter assumes spherical shape and constant exosome density of 1.16 g/mL throughout populations. Vertical dashed line indicates corresponding limit of mass detection as 39 nm.

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Microfluidic Blood Sorting for Improved Blood Quality over Prolonged Storage

C. Yu, S. Huang, H. W. Hou, J. Han
Sponsorship: Singapore-MIT Alliance for Research and Technology, DARPA Dialysis Like Therapeutics

Blood transfusion is one of the most common lifesaving medical therapies. According to the Food and Drug Administration regulation, refrigerated red blood cells (RBCs) can be stored up to 42 days. However, significant loss of RBC deformability typically occurs after 3 weeks of storage time due to ATP and 2,3-diphosphoglycerate (DPG) depletion. As a result, prolonged blood storage raises concerns of compromised blood quality and rapid RBC clearance post transfusion. However, studies suggest that not all stored RBCs are unfit for transfusion: only a subpopulation of transfused stored RBCs were rapidly cleared in mice, and the remaining transfused stored RBCs stayed in circulation in the same way as transfused fresh RBCs.

In our previous work, a novel microfluidic platform was employed to assess changes in human RBC deformability over prolonged storage periods. Banked RBCs were analyzed using a microfluidic deformability cytometer consisting of repeated bottleneck structures (Figure 1). Significant stiffening was observed between 21 and 28 days of storage (Figure 2a). For blood stored more than 4 weeks, a deformability-based microfluidic sorting device was applied to mechanically purify the old stored blood by enriching and separating the less deformable subpopulations. It was found that the side outlet was able to collect significantly stiffer and more fragile RBC subpopulations (Figure 2b).

To investigate whether there is a clinical benefit to transfusing the more deformable subpopulations of old stored blood, we aim to build a mouse model to assess the post-transfusion survival rate after surgery. As a result, the deformability-based cell sorter was optimized for efficient margination of mice blood. The channel length, channel aspect ratio, and outlet bifurcation of the deformability-based cell sorter were varied as well as the flow rate to achieve satisfactory stiff cell removal. By optimizing our technology and building an in-vivo model to elucidate the clinical benefit of removing the less deformable RBC subpopulation, we believe we can extend blood's shelf life and minimize transfusion-related risks associated with blood storage lesions.
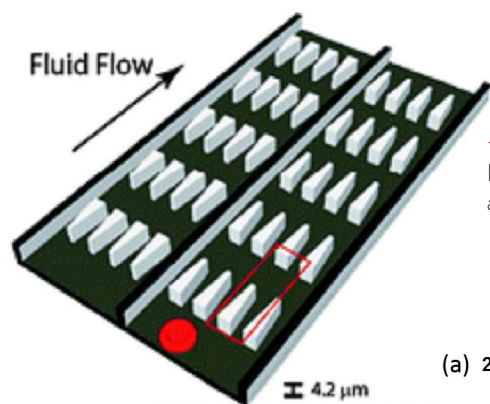
Figure 1: Schematic of the deformability cytometer. Driven by hydraulic pressure, RBCs undergo repeated and extensive deformation in the channel.

Figure 2: (a) Changes in RBC over prolonged storage time. (b) RBC deformability after margination device sorting.
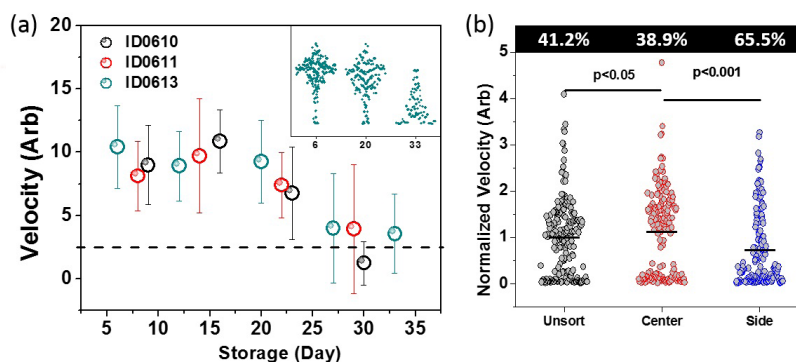
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Single-Cell Study on the Role of ADAM17 in Cancer Drug Resistance

L. Wu, A. M. Claas, D. A. Lauffenburger, J. Han
Sponsorship: Biosystems & Micromechanics IRG, Singapore-MIT Alliance for Research and Technology

Pericellular protease activity, a key component of autocrine signaling, is known to impact the microenvironment of individual cells. Mounting evidence exists for the significant implications of ADAMs, a typical kind of pericelluar protease, in various pathologic settings. However, resulting from the broad substrate specificity of ADAMs, there is a debate over the role of ADAMs in the development of cancer drug resistance. On one hand, the elevated protease-mediated shedding of growth factor ligands have been observed in some resistant cancer cells and shown to be responsible for their resistance by activating an alternative pathway to bypass the specific blockage of the original drug. On the other hand, ADAM proteases shed receptor tyrosine kinases (RTKs) from cell surfaces in addition to growth factor ligands. In cancer cells treated with kinase inhibitors, the activity levels of ADAMs are low, and thus the subsequent RTK shedding is also reduced, leading to RTK accumulation on cell surface. The accumulated RTKs have been shown to enhance the downstream activation of compensatory kinase signaling and confer resistance against specific kinase inhibition. Therefore, it is likely that the variability in ADAM activity of individual cells might have an impact on whether and through which mechanisms each cancer cell can develop resistance to certain drugs. Single-cell measurement of ADAM protease activity is essential to verify this hypothesis.

We have recently developed a microfluidic platform for single-cell measurement of pericellular protease activity. As Figure 1 shows, the designed platform consists of two pieces: a microwell-patterned piece for cell culture (bottom piece) and a 2-layer piece (top piece) acting as an actuatable lid. During each measurement, assay buffer containing FRET-based protease substrate would be introduced into the flow chamber formed between these two pieces. The control channel would then be pressurized to confine substrate and cells within individual microwells. Time-lapse fluorescence imaging would monitor the fluorescence generated by protease-mediated substrate cleavage in real time. Besides, our approach of protease measurement does not require lysis of target cells, which allows us to interrogate the same alive target cell repeatedly to study its temporal behavior upon drug challenge and correlate its protease response with other drug-induced cellular phenotypes, such as morphology, migration, and survival. In the current on-going study, we are utilizing this microfluidic platform to measure the single-cell protease activity distribution of a cancer cell population at different time points across the resistance development process. The evolution profile of single-cell protease activity would offer prospect for studying the role of pericelluar protease in cancer drug resistance.
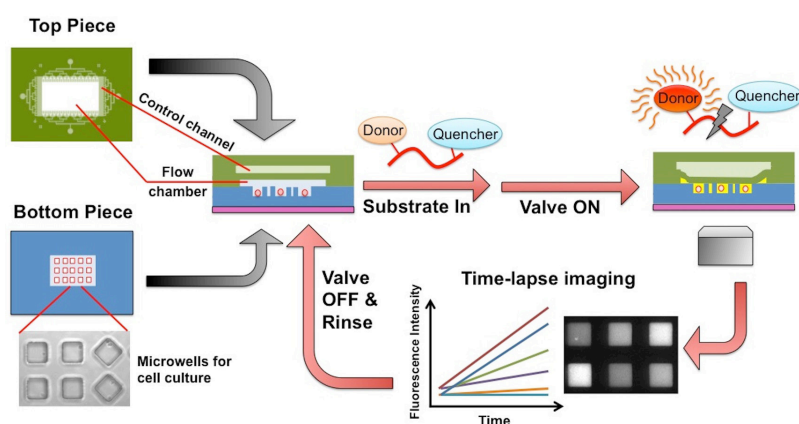
◀ Figure 1: Schematic of single-cell protease assay platform and assay procedure. Upon assembly of top and bottom pieces, assay buffer containing FRET-based substrate is introduced to each microwell via flow chamber, followed by pressurizing control channel to isolate microwells into discrete compartments. Time-lapse fluorescence imaging provides measurement of protease-mediated substrate cleavage. At end of assay, cell-loaded microwell array could be rinsed with fresh assay buffer for subsequent repeated measurements.

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A Nanofluidic Device for Size-Based Protein Concentration and Separation

S. H. Ko, J. Han
Sponsorship: DARPA

Size-based separation of proteins (e.g. sodium dodecyl sulfate polyacrylamide gel electrophoresis (SDS-PAGE) (is widely used to check the purity of protein drugs in the pharmaceutical industry and to ensure the lack of toxic impurities (e.g., protein aggregates). Liquid gel electrophoresis has been automated in a microfluidic platform but still requires polymeric sieving matrices that can increase technical complexity, preventing implementation of truly portable, on-site drug purity and efficacy tests. We have designed a single-step, one-inlet-one-outlet protein analysis device to both concentrate and separate proteins based on size. This system is simple and straightforward to operate; it enhances the detection sensitivity, matching or exceeding that of the standard technique.
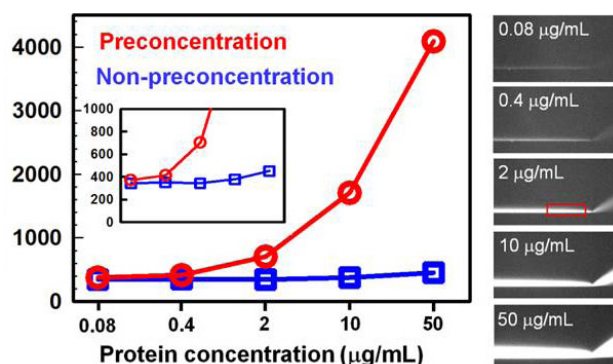
Our design relies on angled nanofilters and enables both protein concentration and separation with a simple one-step introduction of analytes. Each molecule with a certain size has its own distinct trajectory determined by a configurational entropic barrier. Proteins are first manipulated to form a narrow, concentrated band, followed by size-based separation for analysis (Figure 1). The key innovation here is the integrated concentration region, which not only defines the "launching band" for protein separation but also carries out significant concentration to improve the overall detection sensitivity, even in a thin nanofluidic channel (~100 nm).

To check the enhancement of detection sensitivity, we measured the limit of detection (LOD) and concentration factor with different concentrations of a protein (BSA). Figure 2 shows that LOD (80ng/mL) and concentration factor (~100 fold) were achieved. This is a higher detection sensitivity than the silver staining method (1~10ng of protein required per ~10μL loading volume).

We have designed and implemented a new nanofilter system, which would allow simultaneous continuous-flow preconcentration and separation. The efficiency and purpose of the device are determined by only geometry design, such as nanochannel depth, angle, nanofilter period, and inlet width. In addition, unlike previously developed nanofluidic sieving devices, this device enables effective separation and detection for low concentration biomolecules, opening the possibility for its use as a substitute for SDS-PAGE. We believe the device demonstrated here can be used as a point-of-care drug (biologics) efficacy monitoring system, due to its operational simplicity, robustness (no chemical degradation of gels), and minimal sample use (~1 nL of sample volume). The high detection sensitivity of the system could enable detection of low-level impurities in biological drugs that can lead to significant toxicity in patients. In addition, similar systems can be used to measure activity (binding affinity) of the biological drugs as well.

▲ Figure 1: Demonstration of five proteins separation (each protein concentration: 66 μg/mL. SDS-denatured proteins). Fluorescence profiles are measured along white dotted line.

▲ Figure 2: Quantification of LOD and preconcentration factor with different concentration proteins (0.08 μg/mL ~ 50μg/mL).

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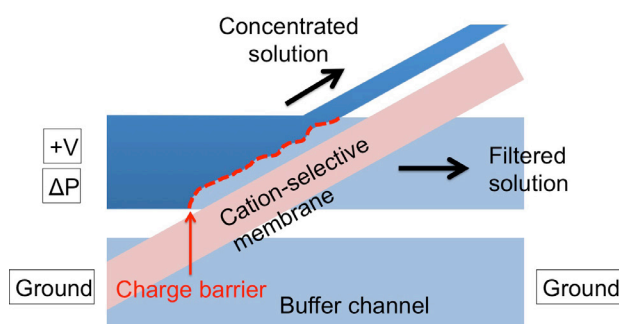# Continuous Biomolecule Preconcentration Using Ion Concentration Polarization

T. Kwon, S. H. Ko, J. Han
Sponsorship: DARPA, Samsung Scholarship

A number of research groups have developed polydimethylsiloxane (PDMS) microfluidic biosensor chips in the past decade. The main advantages of these microfluidic chips include disposability, relatively low cost, and low sample volumes. Preconcentration of target samples can enable faster reaction between target and sensing molecules and improve detection sensitivity of biosensor devices.

In this context, our group demonstrated an enzymatic assay with faster reaction rate and high detection sensitivity in a plug-type concentrator using ion concentration polarization (ICP). When potential difference is applied across an ion-selective membrane, ions are enriched in cathodic side while they are depleted in anodic side. Then, as described in Figure 1, charged molecules cannot pass through this depletion region (charge barrier), and we can concentrate charged molecules by applying pressure-driven and/or electroosmotic flows. However, in the plug-type concentrator, downstream processing of concentrated samples is limited, and selective concentration of either target or sensing molecules to study reaction kinetics was impossible. Kwak et al. demonstrated a continuous-flow preconcentrator based on ICP. In the future, by utilizing the concept of the continuous preconcentrator, we plan to develop a novel enzyme assay chip capable of continuous preconcentration of target samples.

◀ Figure 1: Continuous preconcentration of charged molecules in the microfluidic channel. The charge barrier is formed near cation-selective membrane with voltage difference applied. The concentrated solution is diverted to the upper narrow channel..

▶ Figure 2: The example of continuous preconcentration of charged molecules. Negatively charged fluorescein isothiocyanate (10 ug/mL) was continuously preconcentrated in the microfluidic channel.
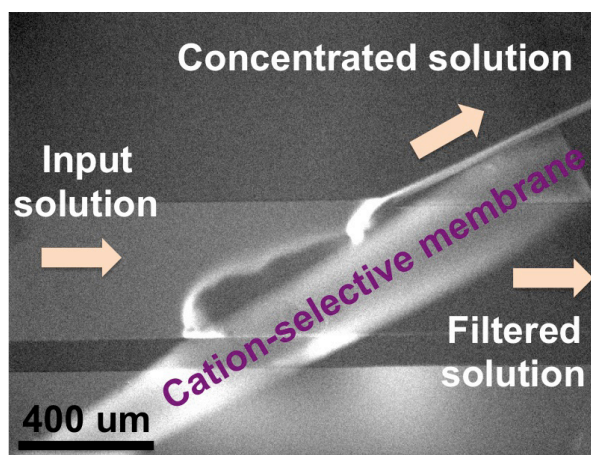
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# Microfluidic Cell Pairing for Studying Immunity

B. Dura, J. Voldman
Sponsorship: Frank Quick Faculty Research Innovation Fellowship

The immune system is tasked with mounting and maintaining protective responses against a wide range of threatening conditions. An effective response requires direct cell-cell interactions, where the ligation of immunoreceptors together with co-stimulatory and co-inhibitory molecules initiates a signaling cascade that promotes immune cell activation and governs a diverse set of developmental (selection, proliferation, differentiation, etc.) and functional immune responses (cytolysis, cytokine secretion, antibody production, etc.). Methods to study these immune cell interactions, however, suffer from limited throughput and a lack of control over cell pairing. Moreover, conventional assays generally depend on bulk co-cultures where the ambiguous nature of cell-cell interactions (number of interacting partners, duration and timing of contacts, etc.) obscures the interpretation of results.

To address these shortcomings, we developed a microfluidic cell-pairing platform that captures and pairs hundreds of lymphocytes using a deterministic back-and-forth cell-loading procedure (Figure 1a-d). This technique creates homogeneously defined one-to-one interactions with enduring contacts, simultaneous timings, and identical contact durations, thereby preventing any variation that would have been otherwise introduced into responses due to the differences in interaction parameters, as would occur in bulk co-cultures. Controlled initiation of interactions further enable examination of the immune cell interaction dynamics from the very onset. The soluble environment around the cell pairs can be controlled by media exchange without disturbing cellular interactions, which enables sequential probing of cell pairs through on-chip stimulation, staining, and fixation protocols. Using these features, we demonstrated, for the first time, dynamic pairwise-correlated measurements over hundreds of cell pairs at the single-cell level in a single experiment (Figure 1e). We further used our devices to monitor early activation dynamics and molecular events during lymphocyte activation, to track cellular response histories upon sequential stimulation, and to characterize the relationship between lymphocyte receptor affinities and early activation dynamics in two lines of melanoma antigen TRP1-specific transnuclear mouse models. Together, our data establish the microfluidic cell pairing platform as a valuable tool for investigation of cell–cell interactions in immunology.
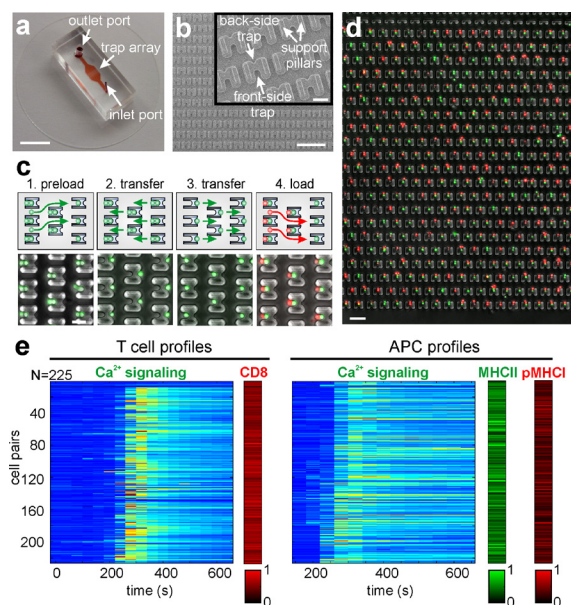
◀ Figure 1: Microfluidic device for immune cell pairing. (a) Image of microfluidic cell-pairing device. Channels and trap array are red. (b) SEM image of cell trap array. (c) Four-step cell loading and pairing protocol. (d) Overlaid phase contrast and fluorescence images show primary mouse lymphocytes stained with DiI (red) and DiO (green) membrane dyes paired in traps. (e) Interaction profiles of OT-I CD8 T cell–APCs compiled over 225 pairs showing raw data set including calcium mobilization and expression of CD8 (T cell), MHCII (APC), and pMHCI (APC) surface molecules. Cell pair responses were arranged based on T-cell calcium responses, i.e., non-responders vs. responders. Response profiles corresponding to non-responder T cells are separated from responders using black line. Range for calcium heat maps: 0 (low)—2.5 (high) where blue indicates low calcium, red indicates high. Scale bars: (a) 5 mm, (b) 100 μm, 20 μm (inset), (d) 50 μm.

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# Iso-Dielectric Separation of Cells and Particles

H. W. Su, L. Liu, J. Voldman
Sponsorship: DARPA

The development of new techniques to separate and characterize cells with high throughput has been essential to many of the advances in biology and biotechnology over the past few decades. We are developing a novel method for the simultaneous separation and characterization of cells based upon their electrical properties. This method, iso-dielectric separation (IDS), uses dielectrophoresis (DEP, the force on a polarizable object) and a medium with spatially varying conductivity to sort electrically distinct cells while measuring their effective conductivity (Figure 1). It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis to concentrate cells and particles to the region in a conductivity gradient where their polarization charge

vanishes. Recently, we have applied IDS to characterize electrical profile of leukocytes for monitor sepsis. One challenge in characterizing blood cells is that the cells change their state very quickly. Delay between blood draw and analysis could introduce inaccuracy. To address this problem, we have started building a portable IDS system for real-time monitoring of cells (Figure 2a). We have designed a circuit board to generate electrical signal with sufficient voltage and current output to drive IDS system (Figures 2b & 2c). A microcontroller such as Arduino or Raspberry Pi will communicate with the DDS and the gain amplifier, allowing control of the voltage and frequency of the signal.
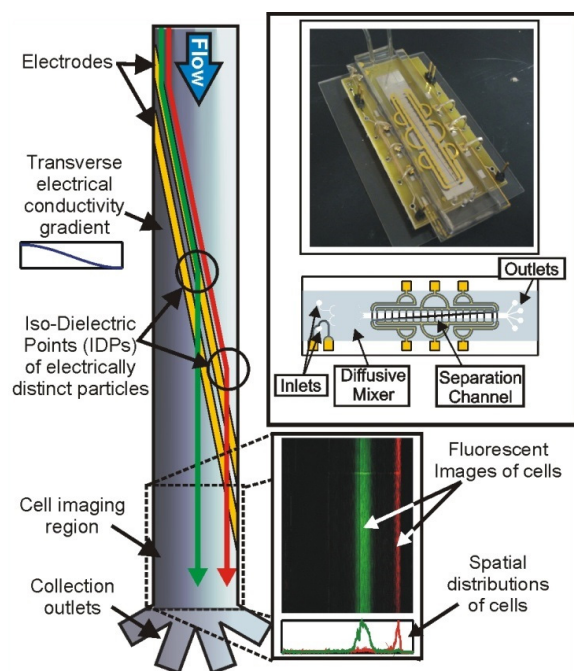
▲ Figure 1: IDS microfluidic device used to measure electrical properties of the cells. The spatial conductivity gradient makes cells with different electrical properties pass through the electrodes at different positions (isodielectric point - IDP).
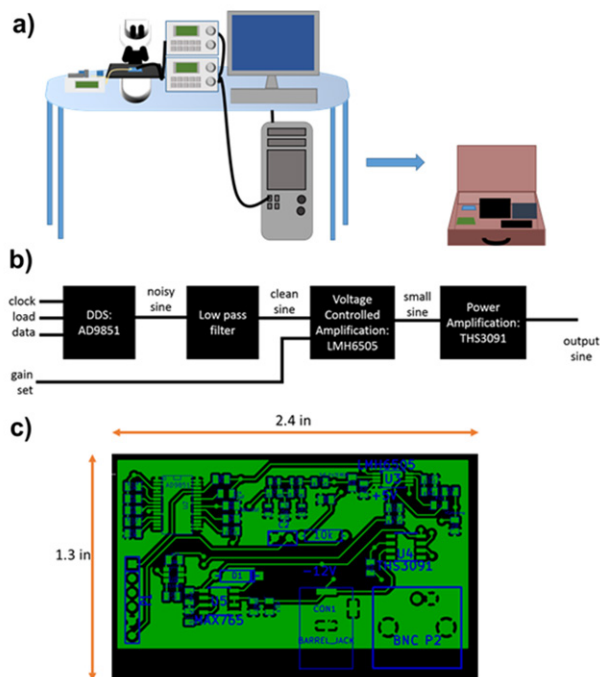
▲ Figure 2: Development of portable IDS system. (a) The goal is to replicate the components of the IDS system and fit into a suitcase. (b) Block diagram of signal generator for the electrical system of the portable IDS. (c) PCB layout of the electrical system.

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# Cell-Based Sensors for Measuring Impact of Microsystems on Cell Physiology

S. Varma, J. Voldman
Sponsorship: National Institutes of Health

The use of microsystems to study and manipulate cells has grown significantly over the past years. With this increase in usage, however, there is also a growing concern regarding the impact of microsystems on cell physiology. Specific molecular biology assays used to examine this concern are typically challenging to implement in microsystem environments. This difficulty limits device users to phase microscopy-based assessments which although convenient, can only convey gross-level physiology, and are non-specific to cell stresses. To this end, we have developed cell-based sensors that emit fluorescence when specific cell stress pathways are activated in microenvironments. This approach does not require large cell numbers, additional reagents, or sophisticated measurement equipment. Additionally, this live-cell assay now allows for quantifiable monitoring of specific cell stress pathway activations through the convenience of fluorescence microscopy (Figure 1A).

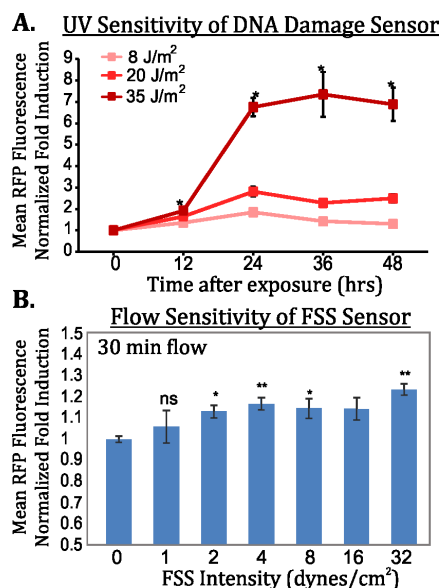Using an easy-to-culture and commonly used NIH3T3 cell line, we developed three types of cell-sensors. Specifically, we created a sensor to assess DNA damage in microsystems, which fluoresces in red (RFP) when the relevant p53-p21 DNA damage pathway is activated. To assess cell stress due to electro-thermal effects, we re-engineered our existing heat shock pathway sensor to express RFP as the activation color. Similarly, we have created a novel fluid shear stress (FSS) cell-sensor for quantifying physiological stresses due to ubiquitously found fluid flows in microsystems. In this case RFP turns on when FSS initiates transcription of a mechanosensitive protein: Early Growth Factor-1 (EGR-1). We verified the functionality of all sensors by chemical induction of their respective pathway and noted RFP induction through microscopy (Figure 1B). We further validated sensor response to its relevant physical stressors: DNA damage sensor to UV (Figure 2A) and EGR-1 sensor to FSS (Figure 2B). We successfully measured the mean fold induction of RFP fluorescence (MFIR) through flow cytometry, verifying sensor utility. With these sensors, the microsystems community can now easily measure stress activation within their device environments and design systems best suited for cell health.
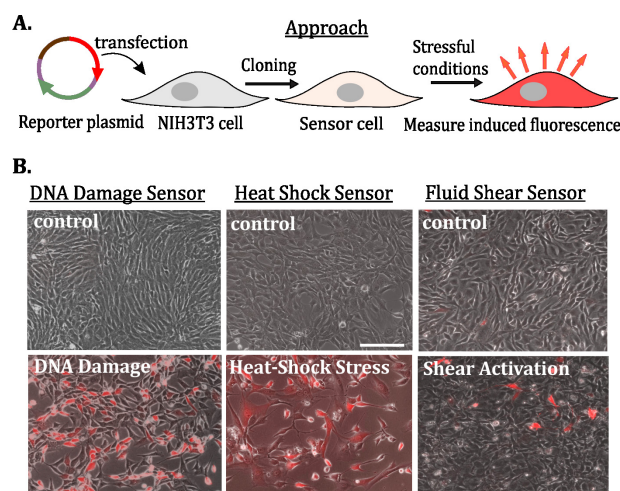
▲ Figure 1: A. Approach to creating and using cell sensors. B. Chemical stressors cause respective sensors to fluoresce (lower panels): DNA damage caused by 4 h treatment of methyl methanesulfonate, heat shock caused by 30 min of arsenite treatment, and FSS pathway activation by 24 h of phorbol 12-myristate 13-acetate treatment. Scale: 100 μm.

▲ Figure 2: Sensor activations through physical stressor exposures. A. UV exposures increase MFIR dynamics for DNA damage sensor. B. Relevant fluid shear stress exposures induce dose-dependent MFIR of FSS sensor.

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Microfluidic Electronic Detection of Protein Biomarkers

D. Wu, J. Voldman
Sponsorship: Maxim Integrated

Immunoassays use antibodies to detect protein biomarkers; these assays have a substantial market and significant clinical importance. However, traditional immunoassays are performed in centralized laboratories using optical methods, which mean results take days and assays cannot be highly multiplexed, in turn increasing patient visits and healthcare costs while decreasing healthcare outcomes. We are developing an all-electronic immunoassay with which we can 1) achieve high-throughput, potentially measuring all protein biomarkers in blood samples; 2) reduce cost by taking advantage of the decreasing cost of silicon electronics; and 3) deliver results to patients before they meet with their physicians.

The biosensor is illustrated in Figure 1: samples are loaded into the microfluidic channel, then antigens specifically bind to antibodies on intergidital electrodes, and finally the presence of antigens is captured by capacitance change due to the binding. To immobilize antibodies, the elctrode was modified using self-assembled monolayers and specific binding between biotin and streptavidin. In our last report, we showed that capacitance measurement can indicate specific binding of protein; but instead of their behavior in a standard buffer, the antigens in practice are in serum or blood whose pH and ionic strength varies from person to person. Therefore we studied the influence of pH and ionic strength. The result (Figure 2) shows capacitance change caused by either pH change or ionic strength variation, as specific protein-binding did; the reasons may be that ionic strength variation altered the double layer capacitance, while the pH change altered the charges on proteins. However, different from capacitance change by protein binding, the change by ionic and pH variation is reversible, which means if we bring them to the original value, the capacitance also recovers. This result suggests that as long as we measure the capacitance before and after protein binding in the same buffer, the capacitance change indictes protein binding, but not ionic and pH variation.
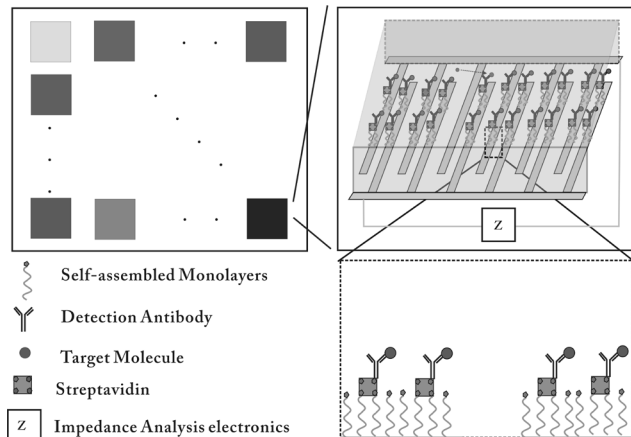
▲ Figure 1: (a) The illustration of multiplexed all-electronic biosensors. (b) The illustration of one pixel of the sensor. (c) The cross section of one pixel.
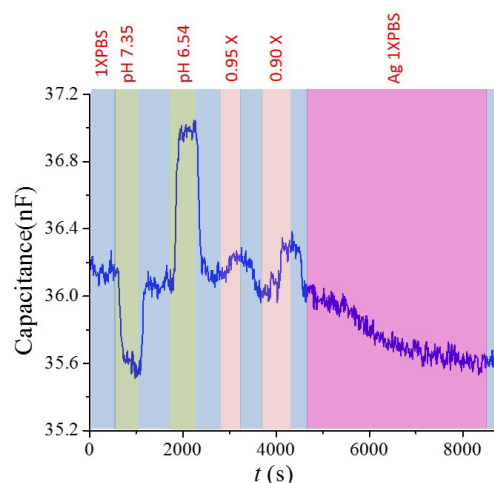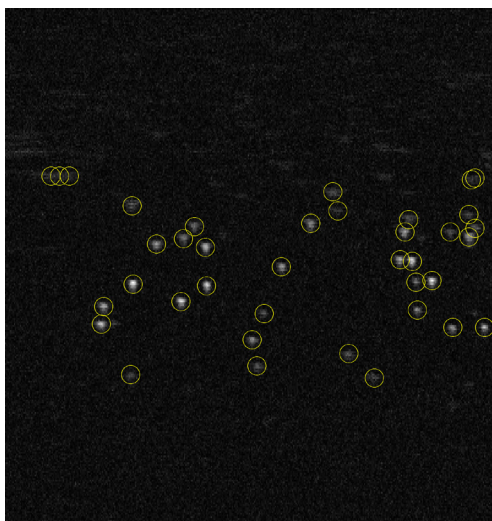

▲ Figure 2: Influence of pH and ionic strength on the sensor signal. The pH of 1X PBS was measured to be 7.04.

Ultrasound-based Cytometry: Absolute Concentration Measurement of Microparticles in Fluid
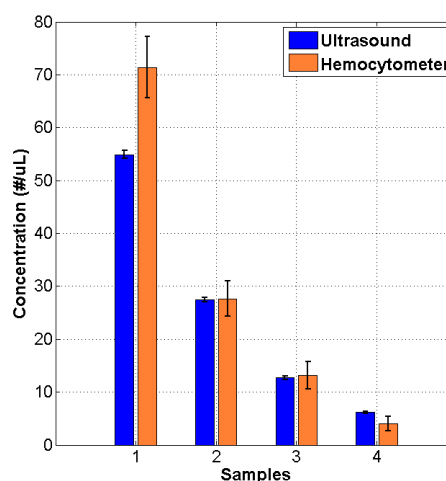
J. H. Lee, B. W. Anthony, D. S. Boning

The ability to measure the concentration of small particles in a medium has a wide range of applications: laboratory instruments that measure cell concentrations in samples, medical tests that measure red blood cell concentration in blood (hematocrit) or white blood cell concentration in body fluids, and even food industry applications such as measuring yeast concentration in beer and wine. The noninvasiveness of ultrasound makes it especially attractive for medical application. When ultrasound frequency is sufficiently high that the wavelength is similar to the size of the scatterer and the sample is dilute, individual scatterers can be distinguished in the image. While the number of scatterers can be simply counted (Figure 1), quantifying the volume being analyzed by the image is challenging because the exact slice thickness of the image is unknown.

The proposed method estimates the slice thickness of the image by extracting the spread of individual scatters from an ultrasound image generated with a mechanically scanned disk single element transducer. Since a circular transducer has identical azimuthal and elevation beam shape, the resulting slice profile of a linearly scanned transducer is identical to the azimuthal beam shape. The method estimates the beam shape from the spread function of each scatterer, which is a combined result of the transducer point spread function and properties of the scatterer such as size and acoustic impedance. The concentration measurement using the proposed method is compared to the hemocytometer in Figure 2.

▲ Figure 1: B-mode image of 10-um polystyrene particles suspended in distilled water acquired with a linearly scanned 75-MHz spherically focused transducer.

▲ Figure 2: Concentration measurement result comparison between the ultrasound-based method and the hemocytometer. Our proposed method shows good agreement with the existing methods.

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Electrochemical Sensors for Monitoring Secreted Cardiac Markers from a Heart on a Chip

D.-J. Kim, S. R. Shin, Y. S. Zhang, A. Silvestri, T. Kilic, J. Aleman, H. Alhadrami, R. Riahi, M. R. Dokmeci, A. Khademhosseini
Sponsorship: Defense Threat Reduction Agency

Microfluidic organs-on-a-chip platforms are finding promising applications both in drug screening studies as well as in fundamental biological investigations. Microscale bioreactors as shown in Figure 1(a) are designed to incorporate organoid constructs for long-term cell culture periods in which the organoids are intended to recapitulate the counterparts in the human body. The microenvironment of the bioreactors needs to be monitored to assess the functionality of the organoids. Since biomarker secretion is correlated with many cell functions or dysfunctions, micro-scale analytical tools enabling real-time monitoring and quantitative detection of proteins in vitro is of great importance. It is believed that microfabrication techniques can be utilized to create these microscale biochemical sensors, which can be connected to the microfluidic bioreactors for sensing in small volumes with high precision. Electrochemical biosensors have numerous attractive features including their miniature size, scalability, ease of use, wide sensitivity range, and outstanding selectivity. Here, an electrochemical sensing module was developed and evaluated for detection of secreted biomarkers from cardiac organoids. Immobilization methods were developed with covalent bonding to create stable immobilization of receptors such as antibodies and aptamers onto the surfaces of electrodes. Furthermore, processes for re-generating the surfaces of electrodes were devised to achieve continual monitoring using these devices.

The microelectrodes were integrated into the microfluidic chips as shown in Figure 1(b). The fabrication of microfluidic chips included a valve layer fabricated from PDMS by replica molding against a SU-8 master, which was bonded to a 40-µm-thick PDMS membrane using air plasma. The fluidic layer was similarly fabricated and bonded with the valve layer, sandwiching the membrane in between. The microelectrode was then bonded with the fluidic layer where the detection area was inside the sensing chamber. A bubble trap was also added to the chip on top of the sensing chamber to capture and remove the bubbles from the system. The working electrode (WE), counter electrode (CE), and reference electrode (RE) were wire-bonded for external connection with a potentiostat. The electrochemical impedance spectroscopy (EIS) was employed as the measurement technique. The surface of the microelectrode was functionalized with aptamers against creatine kinase (CK)-MB prior to detection. The attachment of CK-MB at different concentrations to the microelectrode surface resulted in corresponding charge transfer resistance and showed a linear standard curve from the range of 0.01-100 ng/mL, as shown in Figure 2.
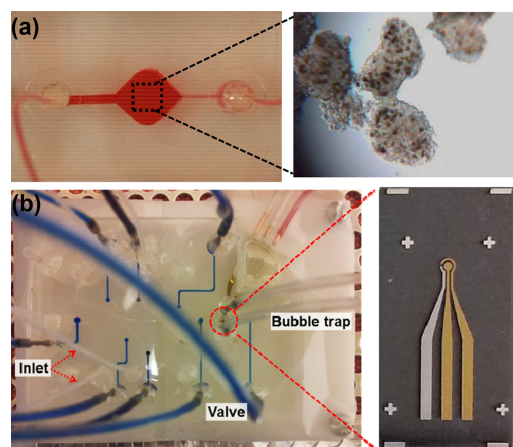
▲ Figure 1: (a) A microscale bioreactor for culturing cardiac organoids. (b) Electrochemical sensors integrated with the microfluidic chip and the photograph of the fabricated microelectrodes.
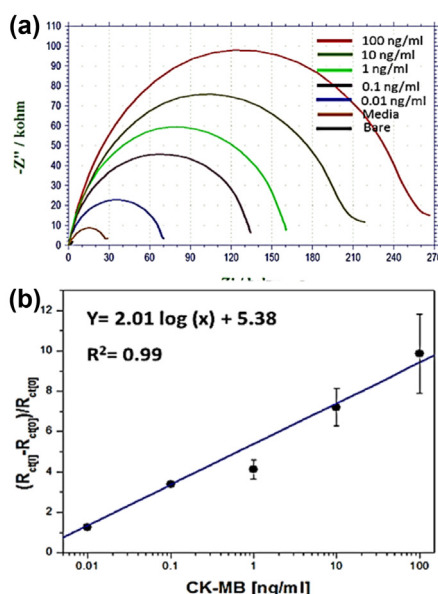
◀ Figure 2: (a) Nyquist plots of impedance spectra and (b) reference curve for CK-MB antigens obtained from $\Delta Rct/Rct(0)$ measurements captured via electrodes.

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Graphene Field-Effect Transistor Sensors for Quantitative Real-Time Polymerase Chain Reactions

C. Mackin, M. DeFazio, T. Palacios
Sponsorship: Institute for Soldier Nanotechnologies

Real-time polymerase chain reaction (RTPCR) is a fundamental analytical technique with broad applications in the life sciences (Figure 1). State-of-art RTPCR systems currently rely on fluorescent probes along with bulky and expensive optical systems. Previous works have shown that RTPCR may be accomplished without fluorescent probes and optical detection systems through fine-tuned PCR chemistries and chemical detection using ion-sensitive field-effect transistors (ISFETs). This is accomplished by appropriately reducing the amount of buffer concentration such that proton release during the DNA extension phase is able to modify pH. Because proton release results from nucleotide incorporation during the template DNA extension, pH may be directly related to DNA concentration.

We build on these works by employing graphene field-effect transistor (FET) sensors, which exhibit well-known pH sensitivity. Because graphene FETs consist solely of a graphene channel region contacted by metal leads, this method offers the advantages of a greatly simplified fabrication process and potentially lower cost than its MOSFET-based counterparts. We develop an integrated chip capable of DNA amplification and quantitative real-time DNA detection. The chip contains resistive heating elements, a temperature sensor, and graphene-based FET chemical sensors. Graphene FET sensors quantify DNA concentration via Dirac point shifts induced by proton release during nucleotide incorporation (Figure 2).
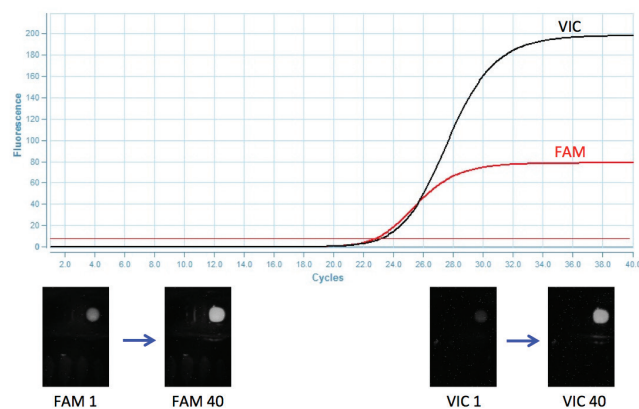
◄ Figure 1: RTPCR experiment using FAM and VIC fluorophores for the detection of a DNA sequence associated with the inability to metabolize clopidogrel, a common antiplatelet medication.

► Figure 2: Graphene FET sensor readouts over the course of an RTPCR experiment for mineral oil baseline (blue), PCR mix with excessive buffer concentration (green), and hypothesized readout for optimized buffer concentration (magenta).
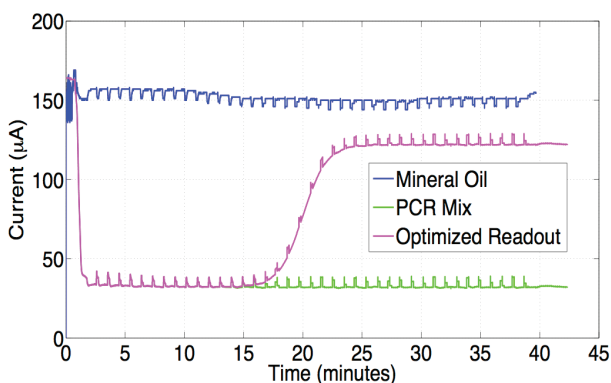
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Chronic, Flexible Electrodes for Interfacing with the Central and Peripheral Nervous System

H. S. Sohal, G. Riggott, E. S. Boyden, R. Desimone
Sponsorship: NIH, McGovern Institute

Micromotion, attributable to the modulus mismatch between the moving brain and electrode materials, is a fundamental phenomenon contributing to generalized electrode failure for chronic brain implants. This failure hampers our ability to dissect neural circuits over chronic experimental paradigms and our ability to produce reliable signals for invasive brain-machine interfaces. We have recently shown that the sinusoidal probe is effective as a chronic implant, providing high-fidelity, stable neural recordings for up to two years with reduced overall gliosis when compared to conventional electrodes (Sohal et al., 2014), perhaps due to its flexibility, and thus intrinsic micromotion-reducing measures. Such measures included a rounded recording tip, a sinusoidal shaft, and a polyimide ball-anchor. The sinusoidal shaft accommodates the brain movement, while the recording sites are anchored in place with the ball anchor. All measures attempt to restrict electrode recording site movement relative to the surrounding brain tissue. The probe is microfabricated out of Parylene-C with WTi recording sites.

The original probe was a proof-of-concept therefore comprised of a limited number of electrode recording sites and restricted to certain lengths. Further, the probes were optimized for chronic recordings in rodents, rather than non-human primates. Now, we have designed and microfabricated the next generation of the sinusoidal probe, substantially increasing the number of recording sites and allowing for multi-depth recording. Lengths of these novel probes, based on the original design, vary from 3-30 mm, allowing for the specific targeting of brain regions in both rodents and non-human primates in highly customizable, 3D arrangements. Further, we have optimized insertion procedures, which may allow for the implantation of more sinusoidal probes using a single carrier, hence minimizing vasculature damage during the insertion process due to repeated brain penetrations. We have also used this process flow to construct differing electrode types for other applications relating to the central and peripheral nervous system in various species.
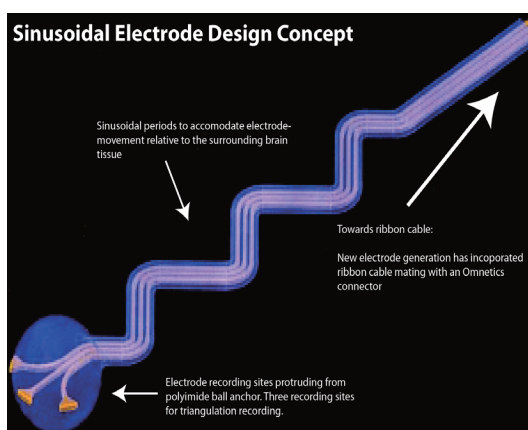
▲ Figure 1: The Flexible Sinusoidal Probe design concept showing the micromotion reducing measures.
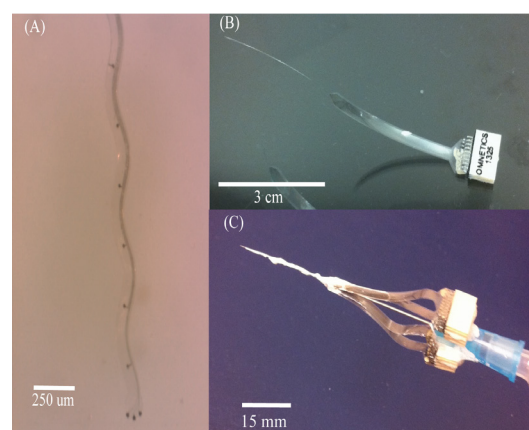
▲ Figure 2: (A) Microfabricated probe, (B) 3-cm-long probe to allow for deep structure targeting, (c) Temporary insertion carrier to allow for the implantation of 4 probes simultaneously with 64 channels of recording

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# Reconfigurable Neural Probes for Chronic Electrical Recording

A. Dighe, U. Froriep, M. Sunshine, A. Ievins, P. Anikeeva, C. Moritz, J. Voldman
Sponsorship: National Science Foundation Center for Sensorimotor Neural Engineering

Chronic interfaces with the nervous system are critical for understanding neurobiology as well as for enabling new technologies that could be used in the treatment of various neurological disorders. A major challenge with current brain-computer interfaces is their inability to reliably record single-unit electrical activity over long periods of time (months) due to tissue reaction to foreign objects in the brain. This tissue reaction consists of a sheath of glial cells that encapsulates a neural probe a few weeks after implantation. Here we describe the design of a new neural probe that aims to bypass the body's immune reaction by changing shape once implanted in the brain, thereby providing the ability to chronically monitor neural activity in vivo.

Our reconfigurable electrode consists of a thin polymer probe whose body can be deflected and locked prior to insertion via a dissolvable glue such as polyethylene glycol (PEG), storing mechanical energy in the device legs (Figure 1a). After inserting into the brain and waiting for the initial glial sheath to form (Figure 1b), the device can be triggered by dissolving the glue, causing the recording tip of the device to penetrate into fresh tissue (Figure 1c). Designing the tip dimensions to be small (7-20 μm) should prevent the formation of an additional glial sheath post-triggering. We have demonstrated successful triggering and electrical recordings from this device in an acute setting in the rodent brain (Figure 2). This technology holds promise for creating chronic interfaces for recording stable neural activity.
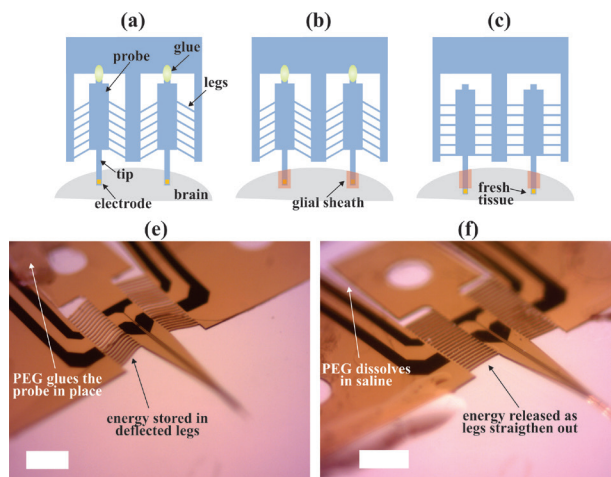
▲ Figure 1: (a) Schematic showing the probe prior to insertion, (b) after glial sheath formation (~weeks), and (c) after dissolving the glue to deploy the probe. (e,f) Photographs of device before and after deployment. Scale bars = 500 μm.
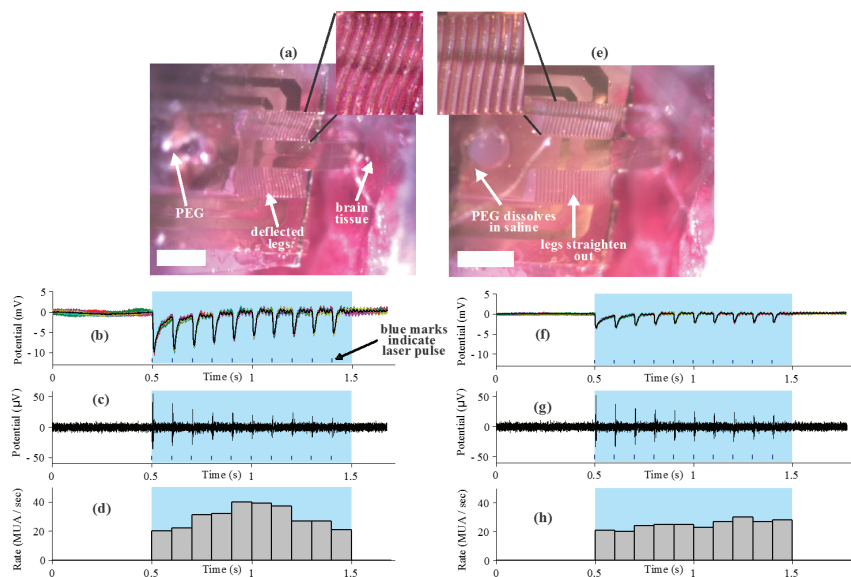
◀ Figure 2: In vivo acute recordings of neural activity in the medial prefrontal cortex of a Thy1-ChR2-YFP optogenetically active mouse. (a) The probe is inserted into the mouse brain (scale bar = 500 μm). (b)-(d) Neural activity is recorded following laser stimulation trains. (e) The probe is deployed. (f)-(h) Neural activity is recorded again in response to the same laser stimulation as in (b)-(d).

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Probing Neural Circuits with Multifunctional Fiber Probes

A. Canales, X. Jia, C. Lu, U. P. Froriep, R. A. Koppes, C. M. Tringides, J. Selvidge, Y. Fink, P. Anikeeva
Sponsorship: National Science Foundation, McGovern Institute for Brain Research, Draper Laboratory

Our ability to understand and map the temporal dynamics of neural circuits associated with fundamental cognitive processes such as learning or decision-making or to treat the neurological conditions such as major depressive disorder or autism are currently limited by the lack of tools capable of adequately addressing and matching the signaling complexity of the brain. Here we describe an entirely new class of flexible polymer-based multimodal neural communication devices that permit simultaneous *in vivo* optical interrogation, drug delivery and electrophysiological recording at high spatial resolution. For the first time we can employ a combinatorial strategy for chemical and optical communication with neural tissue and obtain a concomitant readout of the neural response in a freely moving mouse via a single flexible optoelectronic fiber probe.

The multimaterial fiber probes are produced in a scalable thermal drawing method that involves the fabrication of a macroscopic model, the preform, which is subsequently heated and stretched into many meters of fiber (Figure 1). The resulting fiber has all of the necessary functions built into it and does not require any post processing. Here we fabricated and evaluated multimaterial fibers based solely on polymers (polycarbonate, PC; conductive polyethylene composite, CPE; and cyclic olefin copolymer, COC) or polymer metal composites. We find that our electrodes possess impedance 0.8-2.5 MΩ, waveguides exhibit losses 0.5-2 dB/cm across the visible spectrum, and micro channels can deliver fluids at rates 1-1000 nl/min. Furthermore, our experiments demonstrate the utility of the fiber probes for neural recording, optogenetic stimulation and infusion of neuromodulatory compounds (such as bicuculline, Figure 2) in transgenic mice expressing channelrhodopsin 2 (ChR2) within the brain and spinal cord. Finally, we show that fiber probes produce minimal foreign body response within the surrounding neural tissue. Our results demonstrate the promise of fiber technology in interfacing with the complexity of the mammalian brain while addressing the tissue compatibility and reliability issues.
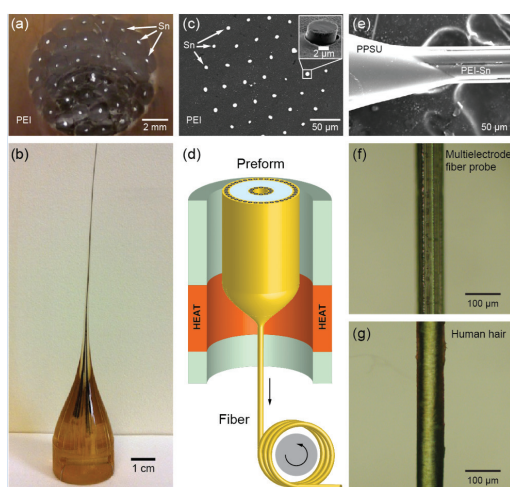
▲ Figure 1: (a) Cross section of a multi-electrode preform. (b) Preform drawn into a fiber. (c) Cross sectional SEM image of a fiber probe produced from preform in (a). (d) An illustration of the drawing process. (e) SEM image of a fiber probe exposed from sacrificial cladding. (f), (g) Micrographs of a 7-electrode fiber probe (f) and a human hair (g).
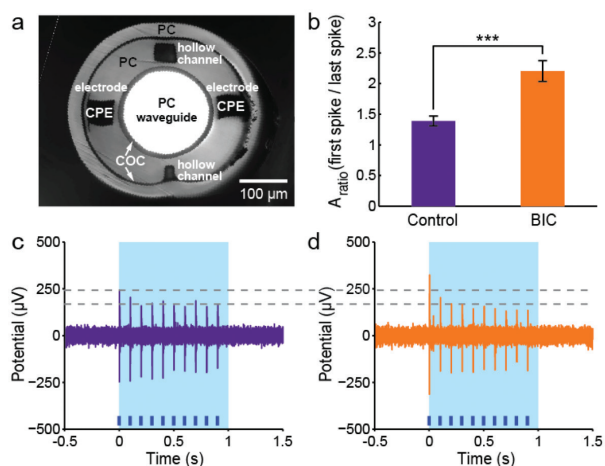
▲ Figure 2: Simultaneous recording, optical stimulation, and drug delivery. (a) Cross section of a multimodal fiber probe with CPE electrodes, PC/COC waveguide, and drug delivery channels. (b) Injection of bicuculline changes the amplitude ratio of the optically evoked first and last spikes in the epoch. (c) Pre-bicuculline epoch. (d) Post-bicuculline epoch.

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Automated Modeling for Large-Scale Arterial Systems

Y.-C. Hsiao, Y. Vassilevski, S. Simakov, L. Daniel
Sponsorship: MIT-Skoltech

Diagnosing medical conditions based on non-invasive (or minimally invasive) measurements requires simultaneous modeling for both (1) local pathological arteries and (2) global arterial networks in order to correlate the available measurements with the actual pathologies. For instance, diagnosing atherosclerosis or an aneurysm requires the detailed understanding of the pressure and flow inside the bifurcation segments. Such information is typically not measurable at pathological sites but may still be attainable if it can be inferred from other measurements. Therefore, it is crucial to develop accurate yet efficient global arterial models such that the correlations between the pathologies and the available measurements can be established. The final diagnosis can be obtained by solving an inverse problem for the pathological parameters, for instance, aneurysm internal diameter, arterial wall thickness, plague stiffness, etc.

For this strategy to be effective, the model for such a large-scale arterial network must be compact, computationally tractable, and field-solver-accurate.

We have proposed an innovative technique to automatically generate nonlinear dynamic models using measurement data or simulations results from partial-differential-equation (PDE) solvers, as shown in Figure 1. The generated models are guaranteed numerically stable, both when simulated alone and when interconnected within a network. This stability enables the hierarchical modeling capability, generating models for local sub-networks, such as branches and bifurcations, and interconnecting them to form a global network. An example of such geometry decomposition is demonstrated in Figure 2. This approach allows full exploitation of artery geometries without compromise due to the shape complexity. In addition, because the entire modeling efforts are subdivided into local model generations, the corresponding finite-element problems for generating training data are at a tractable size. Therefore, the fluid dymamics PDEs, such as viscosity and turbulence, can be fully utilized to capture all types of nonlinearities without simplication.
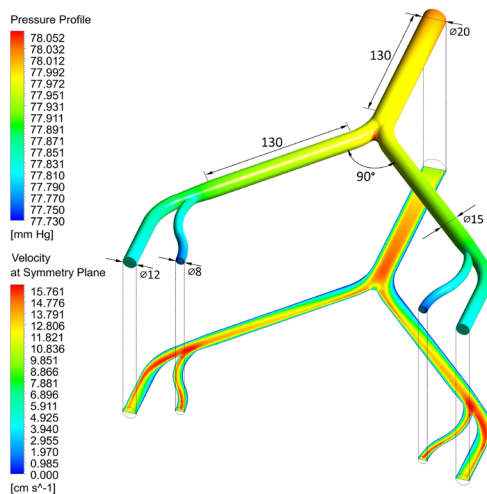
▲ Figure 1: Pressure profile (upper) and velocity profile (lower) of the human abdominal aorta and iliac arteries.
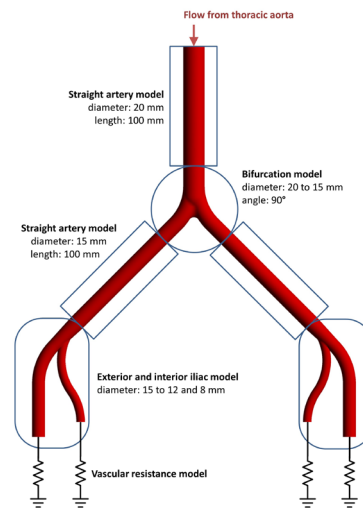
▲ Figure 2: Arterial network decomposition into local models. Each model is automatically generated using our proposed algorithm. The simulation of the overall system is accurate, efficient, and guaranteed numerically stable.

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MARIE: A MATLAB-Based Open Source MRI Electromagnetic Analysis Software

J. Fernández Villena, A. Polimeridis, J. Cruz Serralles, L. Wald, E. Adalsteinsson, J. White, L. Daniel
Sponsorship: National Institute of Health, Skoltech Initiative on Computational Mathematics

MARIE (MAgnetic Resonance Integral Equation suite) is a numerical software platform for comprehensive frequency-domain fast electromagnetic (EM) analysis of MRI systems. The tool is based on a combination of surface and volume integral equation formulations. It exploits the characteristics of the different parts of an MRI system (coil array, shield and realistic body model), and it applies sophisticated numerical methods to rapidly perform all the required EM simulations to characterize the MRI design. The underlying engine of MARIE is based on integral equation methods applied to the different domains that exist in traditional MRI problems (for example, except in interventional cases, the coil and body occupy separate spaces). The natural domain decomposition of the problem allows us to apply and exploit the best modeling engine to each domain. The inhomogeneous human body model is discretized into voxels and modeled by volume integral equation methods. The homogeneous conductors that form the coil design and shield are tessellated into surface triangles, and modeled by surface integral equation methods. Both models are coupled by applying standard dyadic Green functions. Once the models are generated, fast numerical methods are applied to solve the complete system. A set of nested iterative methods with the appropriate preconditioning is used to solve the effect of each port. Fast Fourier Transform techniques exploit the regularity of the voxelized grid and accelerate the matrix vector products. Depending on the different analysis scenarios, some numerical models or tasks can be pre-computed to accelerate the solution, and many strategies are used to reduce either computational time or memory consumption.

The software runs on MATLAB and is able to solve a complex scattering problem in ~2-3 min. on a standard single GPU-accelerated desktop computer. On the same platform it can perform a frequency sweep of a complex coil in ~3-5 min. per frequency point. Furthermore, it can solve the complete inhomogeneous body and coil system in ~5-10 min. per port, depending on the model resolution and error tolerance required. Intended to be a development platform, it includes a simple and intuitive graphical user interface (see Figure 1 for a snapshot) for standard analysis and a set of well-documented scripts to illustrate how to use the core numerical functions to perform more advanced analyses. The underlying numerical routines can be used to generate standard results, such as the B1+, B1- and E maps presented in Figure 2, or to address other relevant problems, such as the generation of ultimate intrinsic SNR and SAR on realistic body models, fast coil design and optimization, and generation of patient-specific protocols, among others.
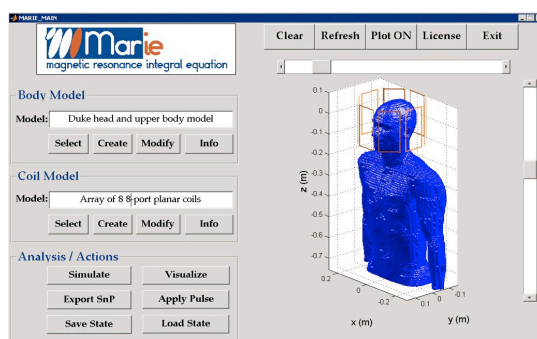
▲ Figure 1: Snapshot of MARIE's graphic user interface with body and coil models loaded, for which the simulation results are shown in Figure 2.
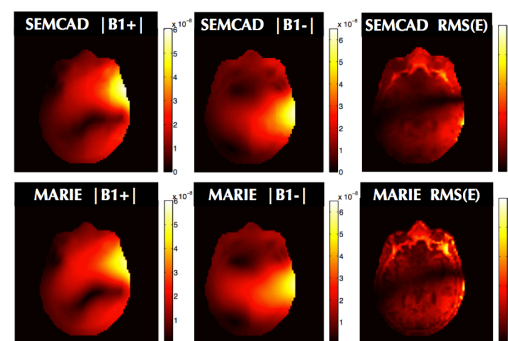
▲ Figure 2: Comparison of the (left) B1+, (center) B1-, and (right) RMS(E) maps for a body model. Top maps are with SEMCAD (SPEAG), bottom with MARIE.

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Nanotechnology, Nanomaterials

Templated Self-Assembly of Block Copolymer Thin Films Under Lithographic Confinement

H. Do, H. Choi, J. Chang, C. A. Ross, K. K. Berggren
Sponsorship: National Science Foundation, Taiwan Semiconductor Manufacturing Company

Physical or chemical templates can direct the self-assembly of block copolymers (BCPs) to achieve well-aligned nanoscale patterns. Complex patterns have previously been demonstrated using a sparse array of lithographically defined and chemically functionalized posts. However, self-assembly of BCPs confined within a topographic template fabricated by electron-beam lithography has not been studied in detail. In this work, we describe how physical confinement affects the self-assembly of cylindrical-phase polystyrene-*b*-polydimethylsiloxane (PS-*b*-PDMS) BCP thin films. This work could lead to a new pattern-generation technique that enables high-throughput pattern generation.

We used an array of square-grid templates fabricated by electron-beam lithography using hydrogen silsesquioxane (HSQ) resist. The patterned substrate was treated with a hydroxyl-terminated PS brush layer. PS-*b*-PDMS block copolymer (45.5 kg/mol) was spin cast on the template and solvent annealed in a 5:1 mixture of toluene and heptane for 3 h at room temperature. The top PDMS layer and PS matrix were removed by CF_4 and O_2 reactive-ion etching, respectively. As shown in Figure 1, PDMS microdomains formed a bar-shaped structure when confined inside a square grid. The bar-shaped structures were randomly aligned to the horizontal and vertical directions because the size of the grid was equal in both directions. In Figure 1(a), 18 structures were aligned horizontally and 18 structures were aligned vertically. As the size of the square was increased, some bar-shaped structures were not fully connected. In Figure 1(b), such defects are visible. One additional bar was formed inside each square compared to the structures in Figure 1(a).

We fabricated a rectangular grid array to control the alignment of the bar-shaped structures. Bar-shaped PDMS structures similar to those shown in Figure 1(a-b) were produced, but now with horizontal alignment. Figures 2(a) and 2(b) show PDMS microdomains confined within a rectangular grid array with aspect ratios of 1.3 and 1.5, respectively. The alignment direction of the bars was preferentially along the horizontal axis resulting in less T-junctions because of the high free-energy penalty associated with forming T-junctions.
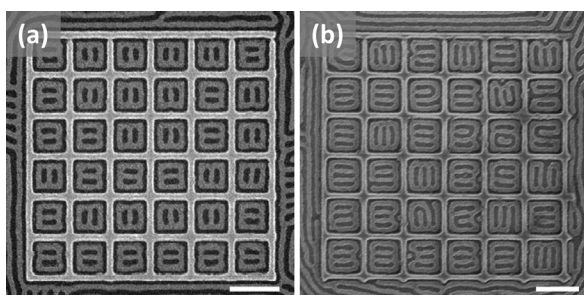
▲ Figure 1: Scanning electron microscope (SEM) images of PDMS microdomains confined inside a square grid array. Size of the square grid was (a) 140 nm and (b) 160 nm. All scale bars are 200 nm in length. (a) The PDMS microdomains formed bar-shaped structures with two T-junctions in each structure. Alignment direction of the structure was random. (b) The PDMS microdomains formed bar-shaped structures with four T-junctions in each structure. Several defects were observed. White lines are oxidized HSQ, and gray lines are oxidized PDMS microdomains.
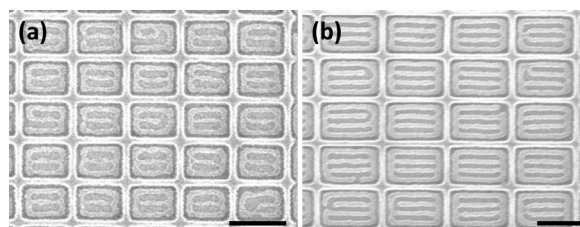
▲ Figure 2: SEM images of PDMS microdomains confined inside a rectangular grid array. Widths of the rectangular grids were (a) 160 nm and (b) 250 nm. All scale bars are 200 nm in length. (a) The PDMS microdomains formed bar-shaped structures that were horizontally aligned. Two T-junctions were formed in each structure. (b) The bar-shaped structures were aligned horizontally, and four T-junctions were formed in each structure. For both cases, the structures were aligned horizontally to reduce the number of T-junctions and therefore minimize free energy. Aspect ratios were (a) 1.3 and (b) 1.5.

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Lithographic Control of Surface and Volume Plasmons in Aluminum

R. G. Hobbs, V. R. Manfrinato, Y. Yang, S. A. Goodman, L. Zhang , D. Su, E. A. Stach, K. K. Berggren
Sponsorship: EFRC Center for Excitonics, Brookhaven National Laboratory, Gordon and Betty Moore Foundation

Aluminum has garnered significant attention as a plasmonic material recently due to the fact that its material properties support surface plasmon (SP) resonances across the entire visible spectrum and deep into the ultraviolet. Moreover, the volume plasmon (VP) resonance in Al has been exploited recently to measure the valence electron density, and by interpolation the material temperature, of an active Al microelectronic device, locally, on the nanoscale. Consequently, the control of plasmonic modes in Al nanostructures is of major interest for applications from nano-optical devices operating in the UV region of the electromagnetic spectrum to nanoscale thermal measurements in active electronic or optoelectronic devices.

In this work we have demonstrated the lithographic control of plasmonic modes in Al nanostructures fabricated by electron-beam lithography (EBL) on ultrathin, 5-10 nm thick SiN_x membranes. We used spatially resolved electron energy-loss spectroscopy (EELS) to map plasmonic modes in Al nanostructures. EELS measurements were performed using the aberration-corrected Hitachi STEM at Brookhaven National Laboratory operating at 200 keV, with an energy-resolution of 400 meV and energy dispersion of 50 meV. We measured the energy and lifetime of SP and VP modes in Al nanodisks as a function of nanodisk diameter, and simulations and models have been shown to accurately reflect the observed relationship between nanodisk diameter and SP/VP characteristics. Figure 1 shows the results of experiments to spatially map surface plasmon excitations in Al nanodisks.
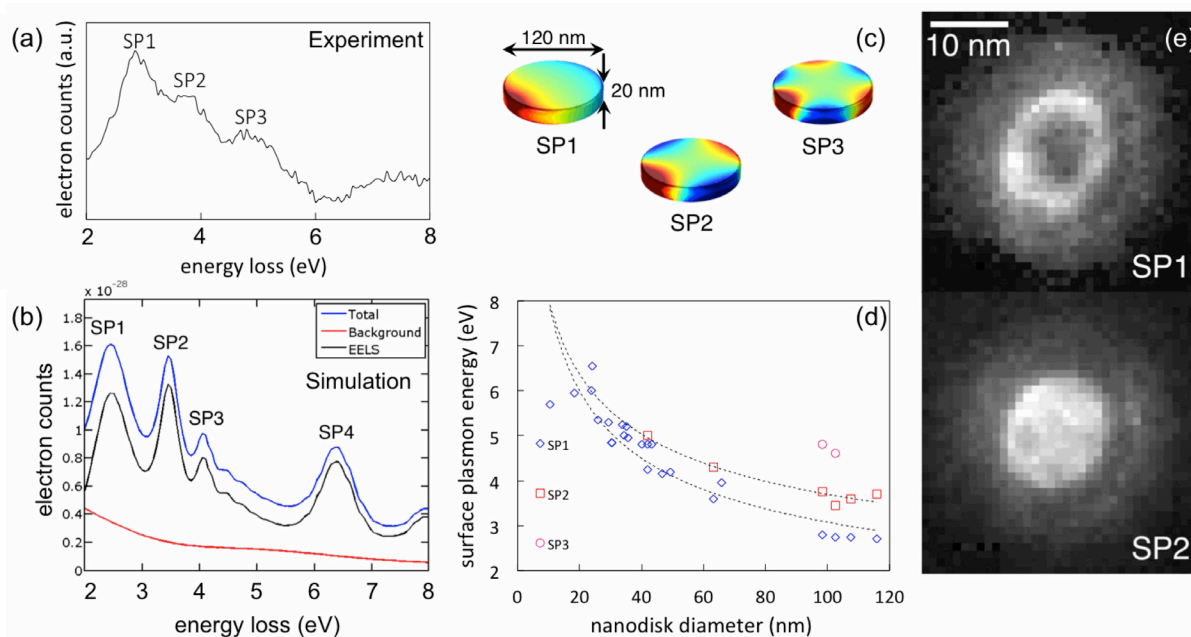
▲ Figure 1: Lithographic control of surface plasmons (SPs) in Al nanodisks. (a) Experimentally measured EEL spectrum for a 120 nm diameter Al nanodisk. The measured spectrum is in excellent agreement with the simulated spectrum in (b). (c) Maps of electric field intensity at the surface of a 120 nm diameter Al nanodisk for the three lowest energy SP modes: SP1, SP2, and SP3, which represent dipolar, quadrupolar, and hexapolar modes, respectively. (d) Plot of SP energy against nanodisk diameter for SP1, SP2, and SP3 surface plasmon modes. (e) EEL maps recorded at energy-loss of SP1 and SP2 modes, respectively, in a 12 nm diameter Al nanodisk.

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Interaction-Free Measurement by Three-Crystal Electron Interferometer

C. S. Kim, Y. Yang, V. R. Manfrinato, R. G. Hobbs, A. Agarwal, K. K. Berggren

Non-destructive imaging of biological samples has been a much sought-after goal in the field of electron microscopy. The quantum electron microscope (QEM) comprising two quantum mechanically coupled electron beams was proposed in 2009 as a means of achieving this goal. A major challenge in the proof of the QEM concept is the demonstration of an interaction-free measurement (IFM) with electrons.

We are investigating a Marton-type electron interferometer (Figure 1(a)) to achieve IFM in a standard transmission electron microscope (TEM). This device consists of three crystal gratings that split and recombine the incident electron beam via diffraction. IFM of an object placed across one of these beams (the sample beam) can be achieved analogous to previously demonstrated IFM with photons in a Mach-Zehnder interferometer geometry.

We used focused gallium ion beam milling (FIB) to fabricate a two-crystal grating from a single silicon crystal monolith. The interferometer has to be precisely aligned due to the short wavelength of the electron (2.5 pm at 200 keV). Using FIB ensures that each grating has the same crystal orientation. We investigated the effect of grating thickness on the fraction of electrons lost through decoherence using electron energy loss spectroscopy. We also fabricated a three-crystal grating structure (Figure 1(b)) as a first step toward the Marton-type interferometer. This structure was used to study diffraction (Figure 1(c)) and interference of the electron beam. We carried out optimization of the interferometer design parameters (diameter of the incident beam, separation between crystal layers) and effects of misalignment (crystal rotation and translation) on the interference fringes.
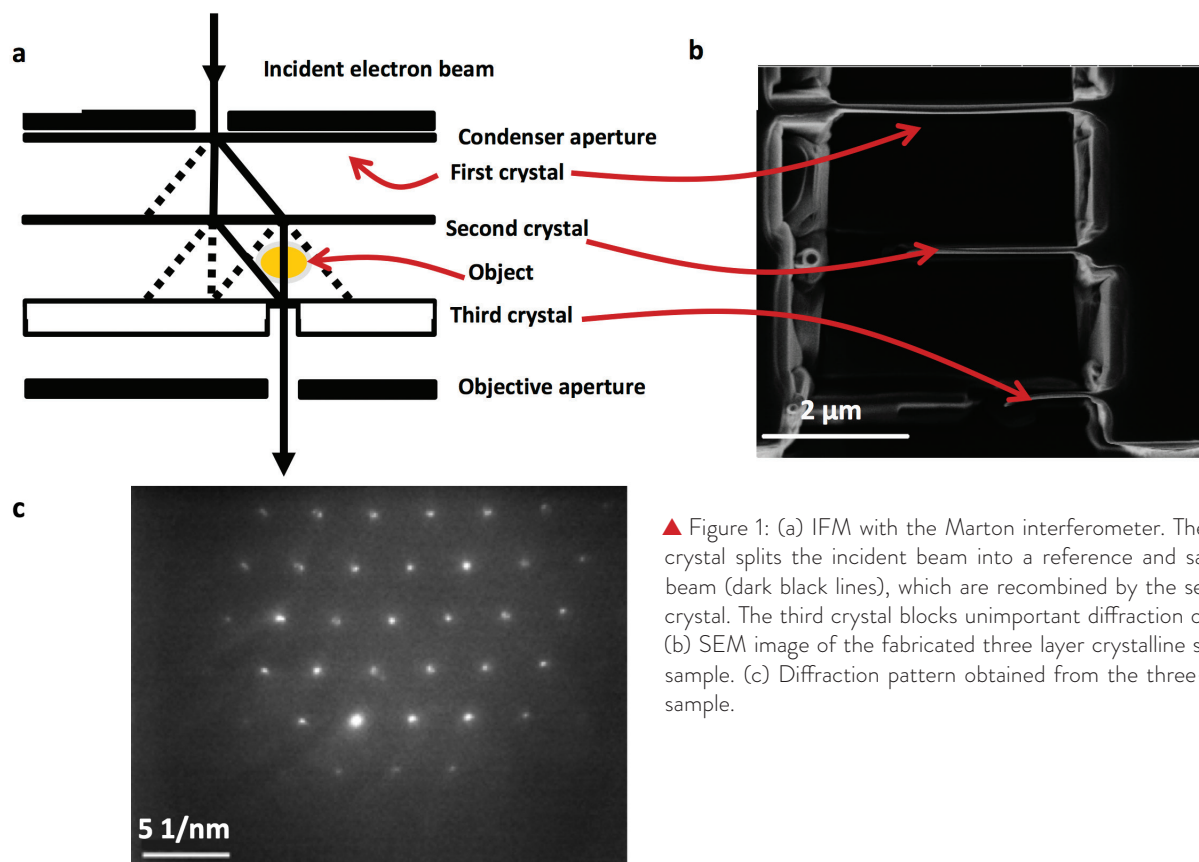
▲ Figure 1: (a) IFM with the Marton interferometer. The first crystal splits the incident beam into a reference and sample beam (dark black lines), which are recombined by the second crystal. The third crystal blocks unimportant diffraction orders. (b) SEM image of the fabricated three layer crystalline silicon sample. (c) Diffraction pattern obtained from the three-layer sample.

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Membrane Nano-Gratings for Electron Diffraction

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Sponsorship: Gordon and Betty Moore Foundation

Nanofabricated electron beam transmission gratings are of interest for a variety of applications, such as electron interferometry, electron holography, and electron vortex beam generation. Compared with natural crystalline samples as electron diffraction "gratings," nano-fabricated gratings provide more flexibility on the control of diffraction angle and orbital angular momentum of diffracted electron beams and can be used with various electron energies. Here we report ~10-nm-thick membrane silicon nitride nano-gratings fabricated with electron beam lithography (EBL) and characterized with electron diffraction in a transmission electron microscope (TEM).

The fabrication process started with silicon nitride membrane (5-20 nm) TEM grids (purchased from *SiMPore Inc.*). Oxygen plasma ashing was applied to clean the membrane and promote resist adhesion. Then, 50 nm poly-methyl-methacrylate (PMMA) electron beam resist was spin-coated on the membrane, and the nano-grating patterns were defined by an Elionix F-125

EBL system. After resist development, CF_4 reactive ion etching (RIE) transferred the pattern to the silicon nitride membrane. Two-dimensional mesh gratings (Figure 1(a)) were fabricated as it allows for large area patterning without delamination issues observed in one-dimensional line gratings. The grating pitch varied from 40 nm to 100 nm, and the patterned area ranged from 2µm to 100µm. Nano-gratings were characterized in a JEOL 2010F TEM operating in high-dispersion diffraction (HDD) mode. Compared to normal electron diffraction mode, HDD mode offered a longer camera length (up to 80 m) and thus a higher magnification to better visualize the diffraction spots located close to the central spot on the diffraction plane. In the diffraction pattern (Figure 1(b)), the diffraction spots' spacing was commensurate with the nano-grating pitch, verifying that these spots were indeed generated by electron diffraction from the nano-gratings.
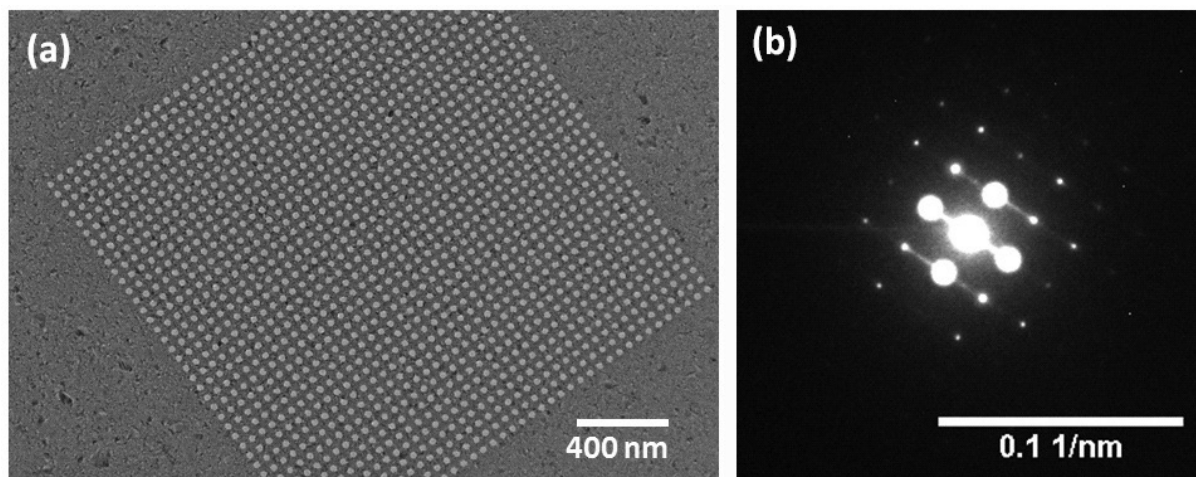
▲ Figure 1: (a) TEM image of a two-dimensional mesh grating patterned on a 10-nm-thick silicon nitride membrane with 10 nm gold coating layer. The grating pitch is 50 nm, and the patterned area is a 2 µm 2 µm square. The purpose of the gold layer is to prevent charging during imaging and diffraction. (b) A high-dispersion diffraction pattern of the mesh nano-grating recorded by JEOL 2010F TEM operating at 200 kV with 80 m camera length.

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Slurry Abrasive Particle Agglomeration Experimentation and Modeling for Chemical Mechanical Planarization

D. S. Boning, J. Johnson
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, Intel

A theoretical modeling approach is developed to predict silica-specific instability in chemical-mechanical polishing (CMP) slurries. In CMP, the formation of large agglomerates such as those seen in Figure 1 is of great concern, as these large particles are associated with high defectivity and poor polish performance. The proposed model describes the complex CMP slurry system as a colloid under high non-linear shear conditions. The model diverges from the classic colloidal models by focusing both on reaction-limited agglomeration (RLA) bounded by silica-specific modes of transitory bonding and on modified DVLO assumptions to include chemical activation and hydrodynamic agglomerate break-up condition evaluation. In order to build physical intuition and predict key model parameters, fundamental experimental studies and novel metrology of agglomerates are performed.

This work finds, in agreement with colloidal and interface science literature, that the specific chemical attributes of *silica* CMP slurry abrasives are the primary drivers of agglomeration, with the secondary being the mechanical application of shear forces (as seen in Figure 2). As a result, we have built both an empirically intuitive and theoretically fundamental model for understanding the behavior of these particles in contrast to other oxide particles, as well as their chemical and hydrodynamic properties under the shear caused by CMP.

▲ Figure 1: SEM of slurry particle agglomerates arising in systematic CMP experiments.

▲ Figure 2: Comparison of model and experimental data for agglomerate growth vs. time, accounting for pH and hydrodynamic break up effects.

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Pad-in-a-Bottle: Planarization with Suspended Polyurethane Beads and a Stiff Counterface
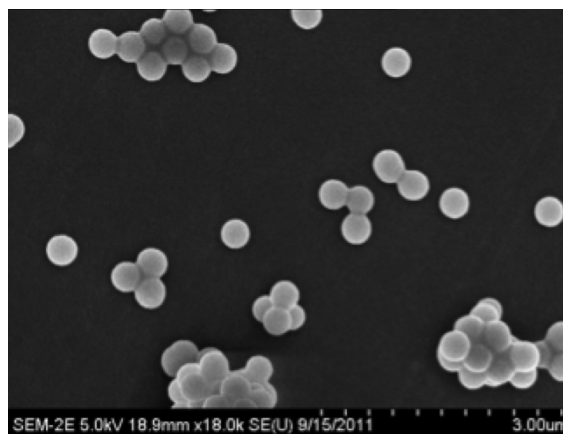
W. Fan, J. Johnson, Y. Zhuang, Y. Sampurno, A. Philipossian, D. S. Boning
Sponsorship: SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

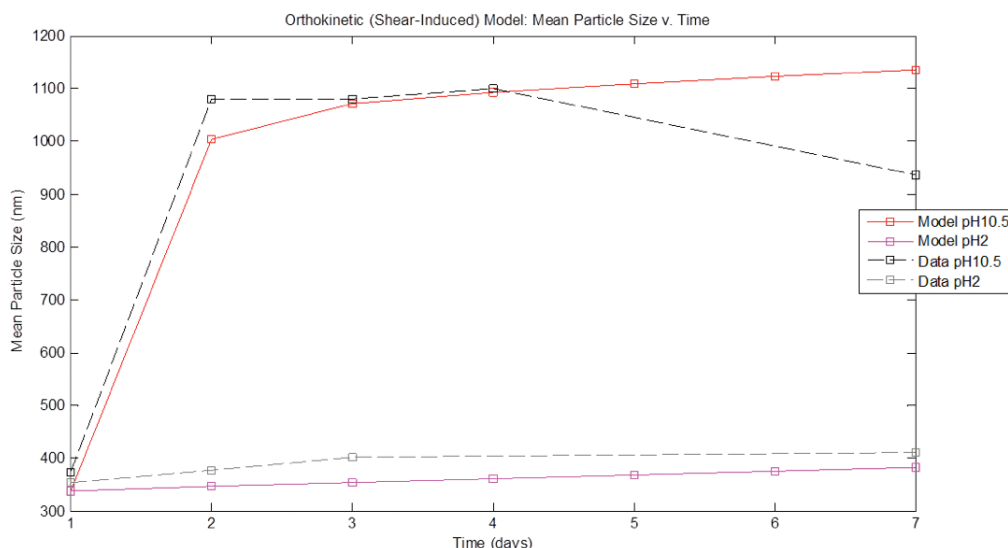"Pad-in-a-bottle" (PIB), an alternative to conventional chemical-mechanical planarization (CMP) is explored. In PIB, a stiff polycarbonate counterface replaces the polyurethane (PU) polishing pad, and 10–50 µm PU beads are used in conjunction with slurry and slurry particles to achieve planarization (Figure 1). Patterned wafer PIB experiments show improved dishing and erosion in STI test wafers. Based on the extraction of a new dual-material PIB model, simulations show that the primary source of reduced dishing and erosion is the use of the stiff counterface as enabled by the compliant beads.

Blanket 200 mm oxide wafers are polished at the University of Arizona on an APD-500 polisher, with 1.2 m/s sliding velocity and 3 to 5 PSI pressures. PU beads with median diameter of 15 and 35 µm are dispersed in Cabot Microelectronics SS25 slurry with surfactant Silsurf. The PU bead content is kept constant at 2 g/L. A polycarbonate counterface with concentric grooves is used. Oxide removal rates up to 150 nm/min are observed. Previous blanket wafer PIB modeling indicates that beads must be stacked (rather than monolayer dispersed) in order to achieve this usable removal rate.

Patterned SKW3-2 STI test wafers are polished using PIB at 5 PSI, for 7 and 10 min in the 15 and 35 µm bead diameter cases, respectively. A new patterned wafer PIB model is fit to measured dishing and erosion (Figure 2). The model accounts for and extracts the following parameters: bead diameter (15 or 35 µm), bead height distribution λ (0.14 µm), bead stacking α (11), effective oxide rate (61 nm/min) and selectivity to nitride (6:1), and counterface Young's modulus (1.6 GPa).

Based on the extracted model, full chip dishing and erosion simulation studies are performed to understand factors that are dominant in achieving dishing/erosion at nitride clear time, compared to conventional CMP. The stiff counterface is found to be most influential in achieving improved within-chip uniformity, as shown in Figure 3.
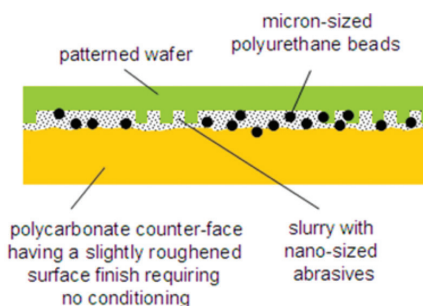
▲ Figure 1: Pad-in-a-Bottle (PIB) CMP with PU beads replacing pad asperities in conventional CMP.
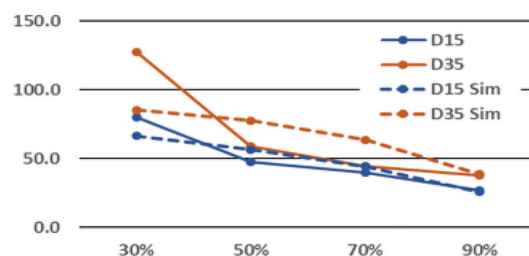
▲ Figure 2: Simulated and experimental dishing (nm) as a function of pattern density.
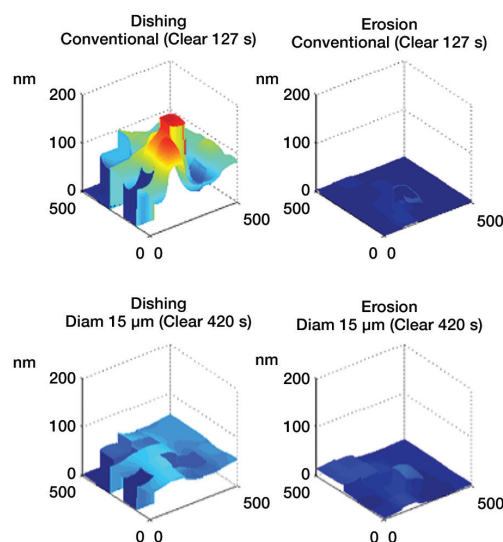
▲ Figure 3: Simulated dishing and erosion across SKW3-2 STI wafer die at nitride clear time: conventional CMP (top) and PIB (bottom).

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Volatile Organic Compounds Sensors based on Oxidative Chemical Vapor Deposition

X. Wang, K. K. Gleason
Sponsorship: Shell

Volatile organic compounds (VOCs) are important hazards in the petroleum industry. Many major hazardous chemicals in refineries are VOCs such as hydrocarbons and alcohol, which may lead to explosions. However, current methods to detect VOCs, such as infrared chemical detectors and transistors, require complicated fabrication methods and high cost. Therefore, it is of great importance to find an economic and efficient way to detect VOCs in refineries. Here, we demonstrate two types of chemical sensors based on oxidative chemical vapor deposition (oCVD) technology. Both chemical sensors utilize the resistance change after exposure to VOCs. The first approach is to tether metal nanoparticles on poly(3,4-ethylenedioxythiohene-co-3-thipheneacetic acid) thin films using wet chemistry. The polymer films are deposited using oCVD (Figure 1 (a)). The sensors respond to acetone/toluene/methanol by modulating the work function of the metal nanoparticles. The second approach is to use oCVD poly(3,4-ethylenedioxythiohene) coated vertically aligned carbon nanotube arrays to detect hydrocarbons. The structure is shown in Figure 1 (b), with the scanning electron microscope (SEM) images in Figure 1 (c). The response of this sensor to n-pentane is demonstrated in Figure 1 (d). Our hypothesis for the sensitivity is that the absorption of non-polar gas molecules in the p-doped conducting polymer layer will decrease the electron hopping rate in the polymer, thus changing the overall resistance. With a simple fabrication method and low cost, our sensors respond to a variety of VOCs with fast and high response.
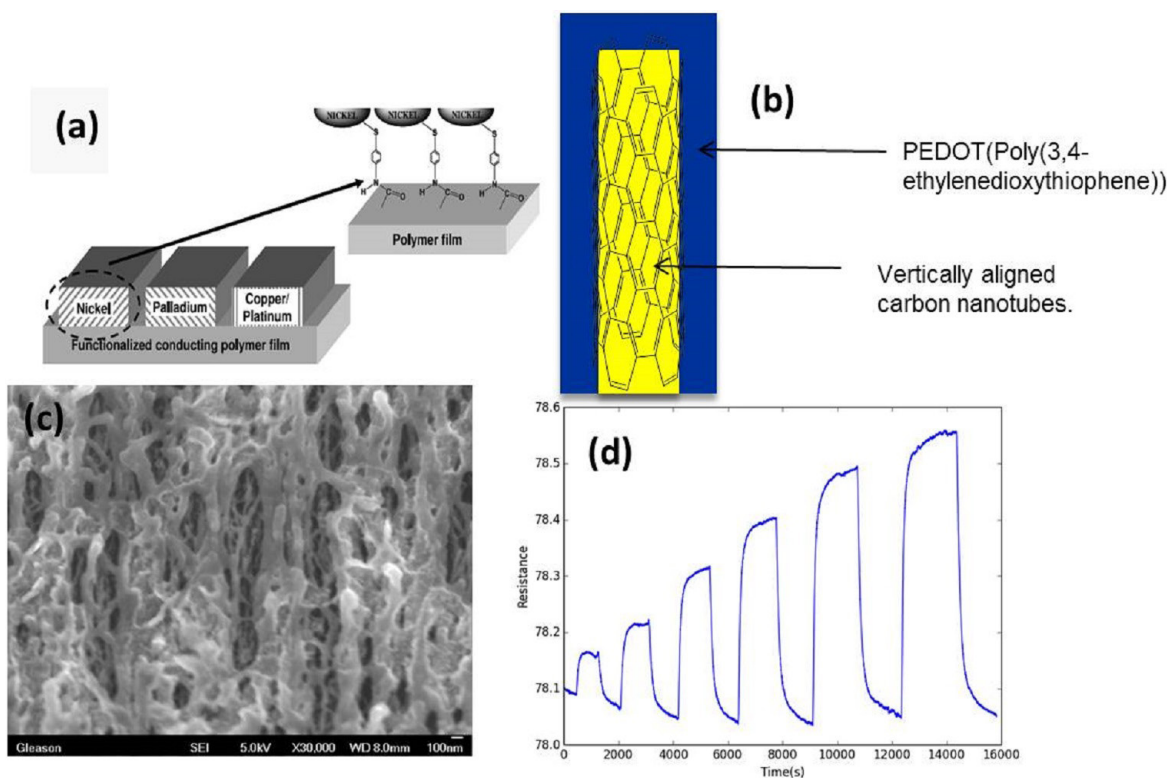
▲ Figure 1 (a) Structure of a metal nanoparticle-copolymer sensor. (b) Structure of polymer-coated carbon nanotube sensor. (c) SEM image of poly(3,4-ethylenedioxythiohene) coated carbon nanotube. (d) Response of the polymer/carbon nanotube sensor to n-pentane vapor ranging from 350 ppm to 7000 ppm.

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Strain-Engineered Manufacturing of Freeform Carbon Nanotube Microstructures

S. J. Park, M. De Volder, H. Zhao, S. Tawfick, A. J. Hart
Sponsorship: DARPA, Air Force Officer of Scientific Research, Office of Naval Research

The skins of many plants and animals have intricate micro-scale surface features that give rise to properties such as directed water repellency and adhesion, resistance to fouling, and camouflage. However, engineered mimicry of these designs has been restrained by the limited capabilities of top-down fabrication processes.

We demonstrate a new technique for scalable manufacturing of freeform microstructures via strain-engineered growth of aligned carbon nanotubes (CNTs). Offset patterning of the CNT growth catalyst and CNT growth rate modification layer is used to locally modulate the CNT growth rate. This patterning causes the CNTs to collectively bend during growth, with exceptional uniformity over large areas (Fig 1a and b). The final shape of the curved CNT microstructures can be designed via finite element modeling (FEM), and using the FEM routine, the internal stress distributions can be calculated to predict structural failure (Figure 1c and d). Because our process is based on an additive chemical synthesis process instead of a subtractive etching and release technique, it enables the direct synthesis of complex microstructures that are perpendicular rather than parallel to the substrate. This result has two major implications: it enables fabrication of closely packed arrays of structures with heterogeneous shapes, and the porosity of the CNT forests enables conformal coating after growth to modify chemical and/or mechanical properties. We demonstrate this latter point by conformal coating of CNT "microtruss" arrays by atomic layer deposition (ALD) and polymer chemical vapor deposition (CVD) which increases their mechanical stiffness without changing the geometry. This process establishes versatile principles for design and manufacturing of complex microstructured surfaces that profit from the mechanical, electrical, and thermal properties of CNTs and can leverage emerging methods for roll-to-roll micro-patterning and CVD.
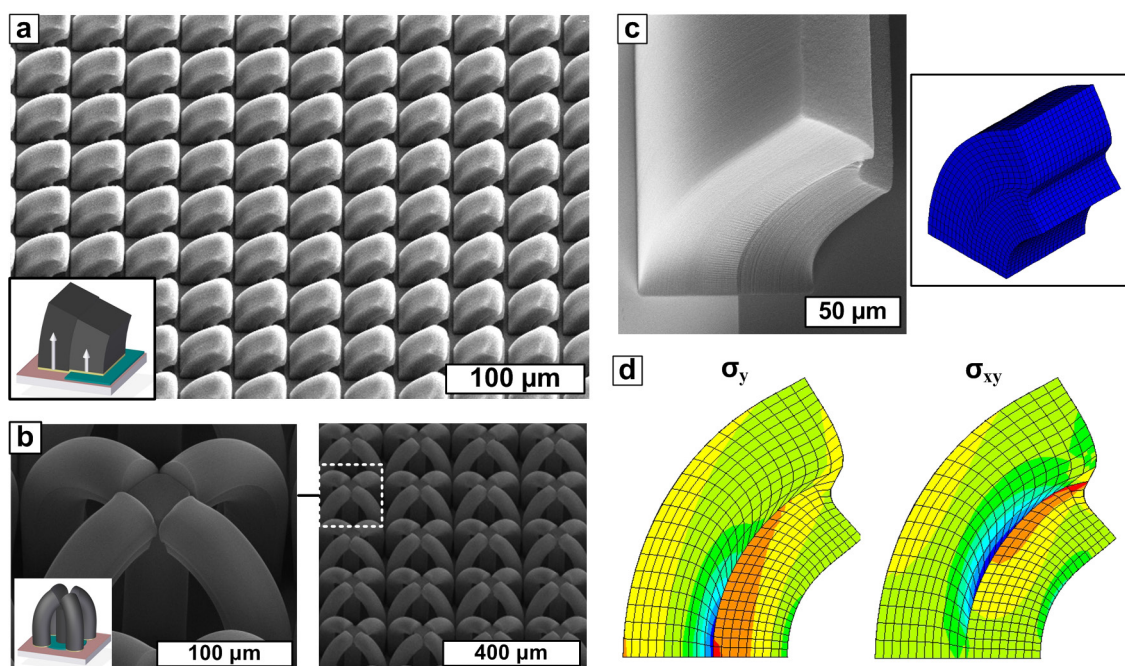
▲ Figure 1: Strain-engineered growth of 3D CNT microstructures by offset patterning of the growth catalyst on a TiN underlayer: (a) curved micropillars; (b) microtrusses. FEM simulation of strain-engineered CNT microstructure growth: (c) visual comparison of an experimentally grown structure and a simulated structure; (d) internal axial and shear stress distribution within the simulated structure.

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Mechanism and Enhanced Yield of Carbon Nanotube Growth on Stainless Steel by Oxygen-Induced Surface Reconstruction

S. W. Pattinson, B. Viswanath, D. N. Zakharov, J. Li, E. A. Stach, A. J. Hart
Sponsorship: Pall Corporation, National Science Foundation, U.S. Department of Energy

It has been previously shown that carbon nanotubes (CNTs) can be grown directly on stainless steel (SS) alloy surfaces because SS natively contains elements that enable CNT growth following exposure to hydrocarbons at elevated temperatures (figure 1). Often CNT growth from SS surfaces has involved the use of acid immersion or oxidation in air to treat the SS surface before hydrocarbon exposure and subsequent CNT growth. However, there is no general understanding of how the surface chemistry and morphology affects the nucleation and growth of CNTs. Through environmental transmission electron microscopy (E-TEM), we observe that CNT growth is enabled by reconstruction of the SS surface following oxygen exposure at the growth temperature, followed by further break-up of the surface upon reduction, and then CNT nucleation and growth after hydrocarbon exposure (figure 2). Using electron energy loss spectroscopy (EELS), we also find that catalyst particles consist of pure iron and iron alloys such as Fe-Cr and Fe-Ni. We use these insights to study CNT synthesis on bulk net-shape porous SS materials, showing that annealing of the SS at 1000°C in air before CVD using an ethylene-based feedstock mixture results in a 70-fold increase in CNT yield. Our findings show how process conditions can be designed for efficient manufacturing of CNT-enhanced stainless steel materials and guide enhanced understanding of CNT growth on additional industrially relevant metal substrates.
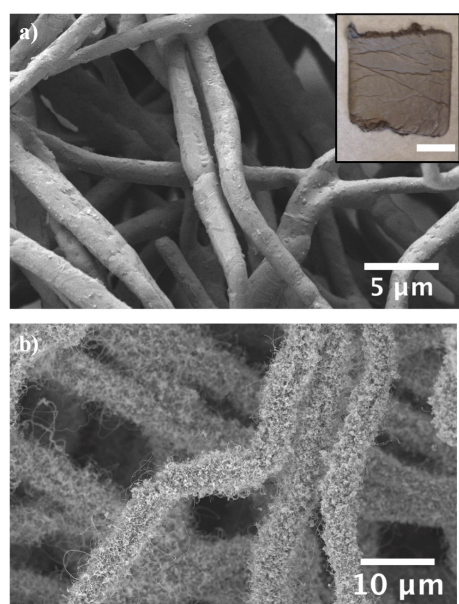
▲ Figure 1: a) SEM image of untreated SS mesh consisting of ~2 µm diameter fibers (inset: optical image with 10 mm scale bar); b) SEM image of 2 µm diameter SS fiber mesh after CNT growth.
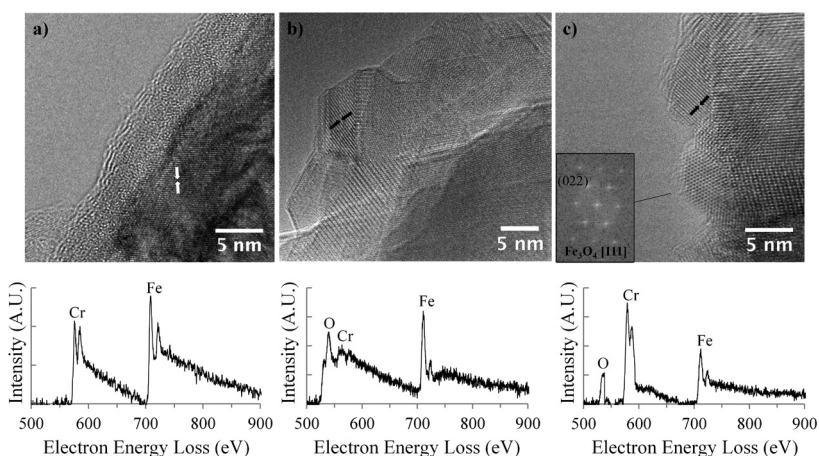
▲ Figure 2: Sequence of high-resolution TEM images and EELS spectra (with linear intensity scale) of an SS 316L surface at a) room temperature in 4×10-7 Torr vacuum (0.20nm spacing is indicated); b) in 40 mTorr oxygen at 500°C (0.34 nm spacing is indicated); c) in 4×10-7 Torr vacuum after venting oxygen but before putting in C_2H_2 and H_2, (0.27 nm spacing is indicated). Image b) was acquired by averaging 13 frames taken using the Gatan K2-IS Direct Electron Detection camera.

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High-Speed Roll-to-Roll CVD of Graphene using a Concentric Tube Reactor

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Sponsorship: National Science Foundation Scalable Nanomanufacturing Program

Continuous and scalable manufacturing techniques are crucial to enable the use of graphene in large-area applications including flexible displays and solar cells. Our group has invented and built a roll-to-roll chemical vapor deposition (CVD) machine using a novel concentric tube design, featuring a thin foil substrate that is wrapped in a helical path around the inner tube and is continuously translated and exposed to the gas atmosphere in the small gap between the concentric tubes. Radial holes in the sidewall of the inner tube enable downstream injection of the carbon source.

Through this decoupled, multi-zone reaction chamber, two sequential treatment atmospheres are seamlessly combined in a controlled thermal environment. Our research highlights the system parameters that lead to optimal quality and coverage of graphene and identifies important tradeoffs between foil translation rate and graphene quality. We demonstrate that graphene films can be produced at a foil translation speed of up to 500 mm/minute in an ethylene/hydrogen atmosphere at ~2 Torr and 1000°C. Nucleation and growth are also shown to depend strongly on substrate preparation, and annealing of the Cu foil in hydrogen prior to growth leads to ~67% increase of the graphene G/D ratio. Additionally, the concentric tube design leads to an ~90% reduction in reaction gas use as compared to typical reactors. Opportunities for further improvement of roll-to-roll graphene manufacturing include enhanced control of pre- and post-treatment atmospheres, and the integration of patterning and transfer methods as well as the integration of additional treatment zones.
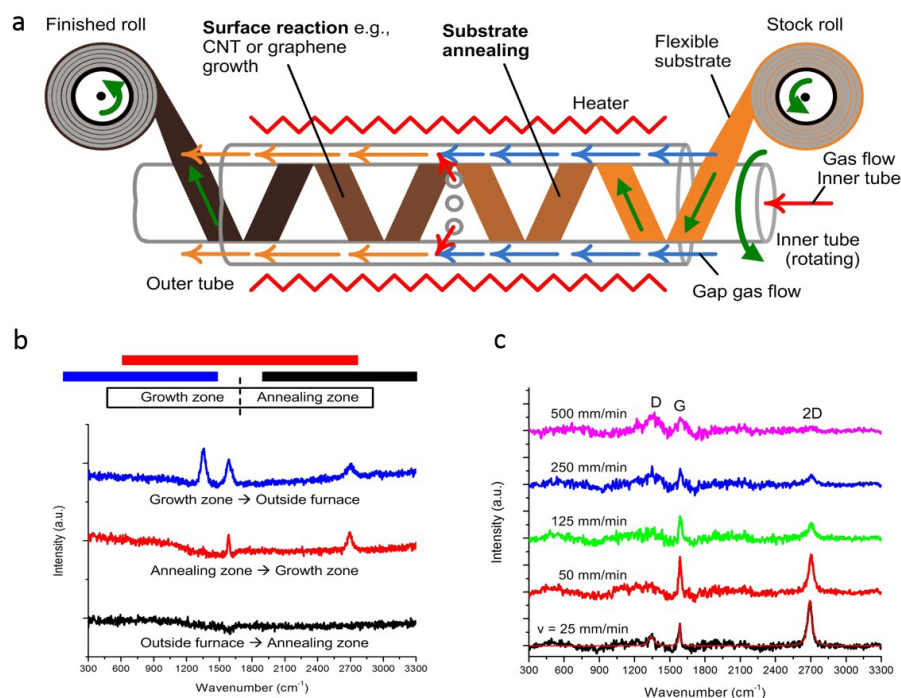
▲ Figure 1: a) Concentric tube reactor with the substrate foil wrapped around the inner tube, which carries the growth gas for the second stage of the reactor. Between the inner and outer tube flows, the gap gas anneals the substrate in the first stage of the reactor and mixes with the growth gas in the second stage. Both stages are located in a tube furnace to provide for the reaction temperature. b) Raman spectra of the substrate at points outside the furnace, in the annealing and growth zone. c) Raman spectra of graphene grown at different translation speeds.

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Modular Robotic System for Photopatterning Large 3D Surfaces

A. Stevens, R. Oliver, L. Chin, A. J. Hart
Sponsorship: National Science Foundation, Massachusetts Institute of Technology

The capability to pattern photosensitive polymers on large curved objects, and to use these patterns to perform traditional micromachining processes, would be an enabling technology for applications including textured mold tooling and integration of electronics with custom medical implants.

Toward this goal, we have designed and built a system comprised of a 6-axis robot and a rotary stage (Figure 1a). A custom-built end effector including a digital light processor, optics, and camera, is mounted to the robot and can be positioned anywhere within a 20x20x20 cm work envelope (Figure 1b). The workpiece is placed on a kinematic mount attached to the rotary stage (Figure 1c). The measured repeatability and accuracy values of the motion system and thus the projected pattern are

20 and 30 microns, respectively. The resolution of the projected light pattern is approximately 1 micron.

The substrate is patterned by digitally triangulating an object with a 3D scanner (Figure 2a) and associating the location of each triangle in the digital space with that in real space. Each triangle is then associated with the computer-applied texture contained within its borders and stored in memory for later projection. The texture is then replicated on the photopolymer-coated substrate by sequentially exposing every triangle in the digital file (Figure 2b, 2c).

We present preliminary demonstrations of functionality by pattern transfer to a metal sphere via etching and by patterning hydrogel microstructures onto a small bone.
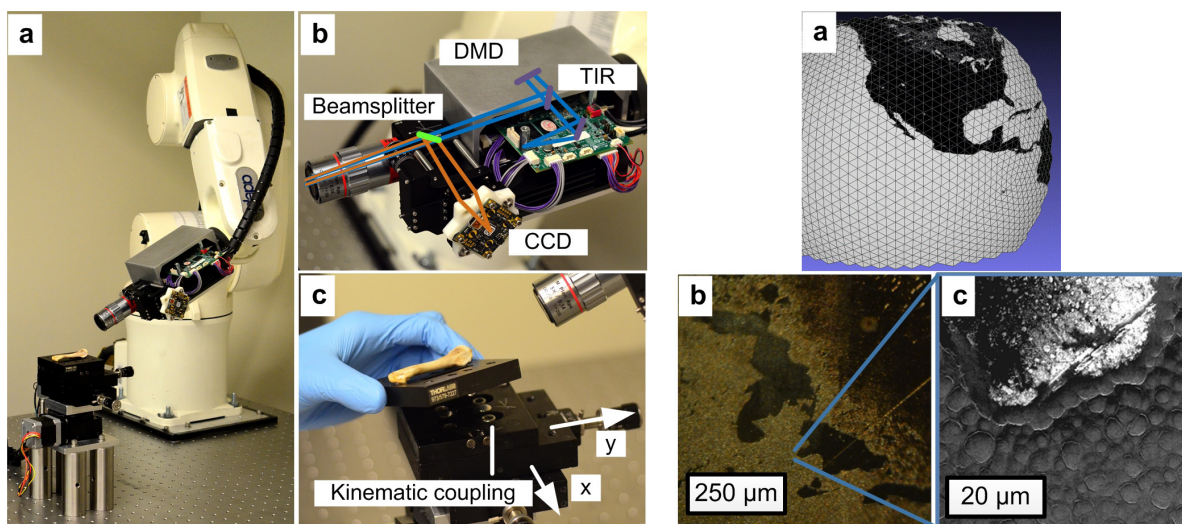
▲ Figure 1 (left): Robotic photopatterning system. a) motion system comprising 6-axis robot and rotary stage; b) custom dynamic-mask projection end-effector; c) bone substrate mounted to kinematic coupling fixture.

▲ Figure 2 (right): Test patterning of a 3D surface. a) triangulation of a spherical surface with applied texture of North America; b) optical micrograph of sphere surface with texture replicated in photopolymer; c) electron micrograph of (b) showing microstructure of photopolymer after development.

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Application of Tungsten as a Carbon Sink for Synthesis of Uniform Monolayer Graphene free of Bilayers/Multilayers

W. Fang, A. Hsu, Y. Shin, Y. Song, T. Palacios, J. Kong
Sponsorship: National Science Foundation

Graphene has attracted great interest because of its exceptional physical properties and enormous potential for various electronic applications. Many synthesis methods have been developed to prepare high-throughput monolayer graphene including mechanical exfoliation, reduction of graphene oxide, SiC thermal decomposition and chemical vapor deposition (CVD). Among them, CVD is one of the most promising approaches because it allows for growth of high-quality large-area graphene, which later on can be easily transferred to arbitrary substrates. Currently, copper is most commonly used as a substrate for the CVD growth of monolayer graphene because of its low carbon solubility. Although the uniformity of graphene grown on copper is greatly improved as compared to that on nickel, small bilayer domains with size of 1~5 μm can still be observed. Moreover, researchers found that bilayer formation is highly dependent on the morphology and impurity of the Cu foil and growth conditions. Therefore, to achieve uniform monolayer graphene, various methods of pre-treating the copper foil have been studied such as etchant cleaning, chemical-electro polishing and many-hour annealing. The size of the bilayers can also be minimized, but not eliminated, by tuning the concentration of hydrogen.

In this work, we focus on graphene growth on Cu enclosures due to asymmetry of carbon delivery between the two surfaces. Our previous works have shown that by using Cu enclosures for growth, high coverage of bilayer graphene can be achieved on the outside surface of the enclosure because carbon inside can diffuse out to form bilayers on the outside. The carbon source diffusion process is driven by the concentration gradient across the copper foil. In this work, we propose that by reversing the direction of the carbon diffusion, we can selectively remove bi-/multi-layers to achieve uniform monolayer graphene. We utilize a tungsten foil, which acts as a carbon sink inside the enclosure.
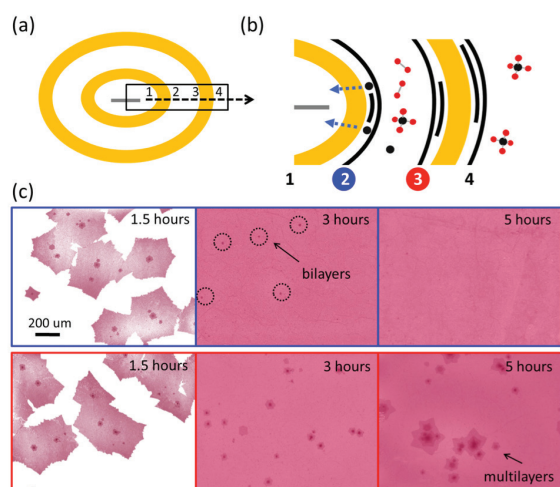
▲ Figure 1: Graphene grown on Cu double enclosures. (a) Schematics of the Cu double enclosures. (b) Growth mechanism for bi-/multi-layer graphene on surface 2 disappear while remains on surface 3. (c) Comparison of graphene grown on the surface 2 and 3 as a function of time.
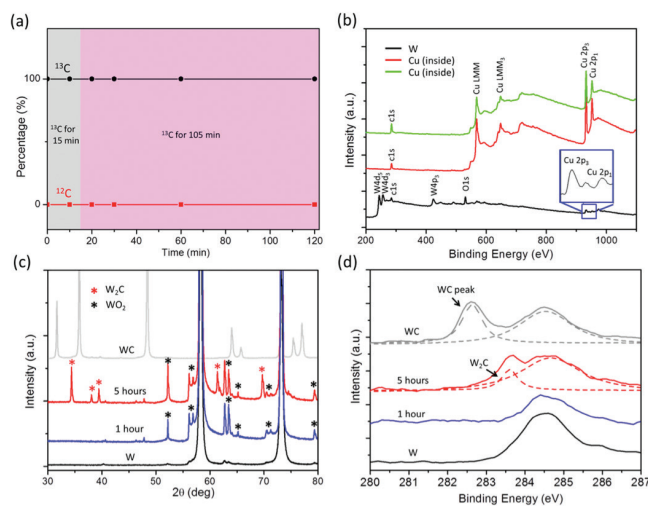
▲ Figure 2. Characterization of the graphene grown on Cu enclosures with tungsten and the composition analysis of the tungsten foil. (a) Percentage of ^{12}C and ^{13}C isotope in monolayer graphene. (b) XPS results and (c) XRD results on as-received tungsten foil (black), tungsten foil after 1-hour (blue) and 5-hour growth (red), and as-received tungsten carbide (grey). (d) Detailed XPS spectrum of C1s.

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Roll-To-Roll Transfer of CVD-Grown Graphene onto Flexible Substrates Using Heated Roll Lamination and Electrochemical Delamination

M. Hempel, T. Palacios, J. Kong
Sponsorship: Eni S.p.A.

Since its extraction in 2004, graphene has attracted tremendous attention due to its unique properties such as single-atom thickness, mechanical strength, and extremely high carrier mobility. Additionally, this material is 98.7% transparent, very flexible, and easily doped. Owing to these characteristics, it is a promising candidate to replace indium-doped tin oxide (ITO) as transparent conductive film in future flexible optoelectronic applications. ITO is brittle and expensive, which makes it not well suited for low-cost optoelectronic devices such as flexible solar cells or displays that could be used in clothing or as electric papers. Driven by this motivation, the goal is to create a scalable technology to produce graphene on flexible, transparent substrates with a sheet resistance below 100 Ω/□ ,which is necessary for the presented applications.

In this work, we developed a setup (see Figure 2) to transfer graphene from copper foil directly onto polyethylene terephthalate (PET) films. A schematic of the setup is depicted in Figure 1. To facilitate the transfer, a graphene/copper strip is first laminated onto the PET film. The PET substrate is coated with a thin ethylene-vinyl acetate (EVA) layer. The heated rollers (130˚C) melt the EVA to create a glue-like layer that bonds the PET film firmly to the graphene. Subsequently, the copper foil is electro-chemically delaminated in a sodium hydroxide bath (1 Mol/l). Applying a voltage between the copper and a platinum counter electrode, that is also submersed the electrolyte bath, generates hydrogen bubbles at the graphene/copper interface that gently separate the copper from the graphene/EVA/PET compound film. Lastly, the rewind stage collects the two films on individual rollers.

So far, we have demonstrated a graphene transfer from copper strips (W 1.2 cm, L 10 cm, H 25 μm) onto PET (75 μm) with a sheet resistance of 5 kΩ/□. In the future, we want to optimize the transfer parameters to lower the sheet resistance to reach the goal stated above and expand the transfer process to be continuous on meter-long substrates.
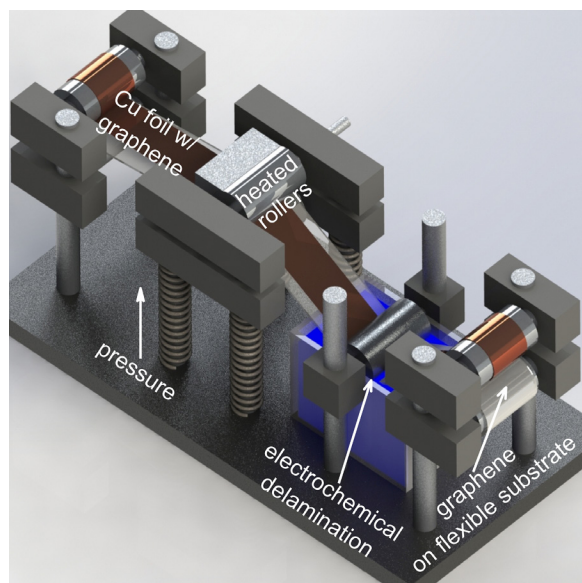
▲ Figure 1: Schematic of developed roll-to-roll transfer setup. First, copper with graphene is laminated onto a PET/EVA substrate using pressure and heat. The copper is then electrochemically delaminated, leaving graphene on the PET/EVA substrate.
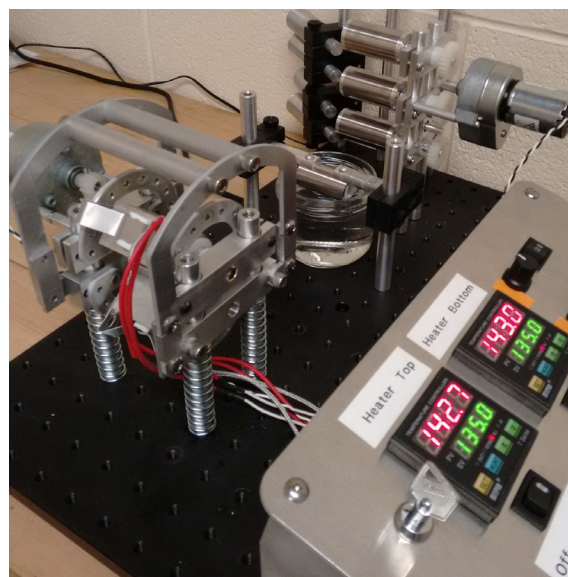
▲ Figure 2: Actual implementation of setup. (Mid-left) lamination unit, (bottom right corner) control panel with temperature and motor speed control, and (top right corner) rewind stage with three rollers for graphene transfer from both copper sides.

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Integration of 2D Materials into 3D Printing

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Sponsorship: NASA, Office of Naval Research PECASE

In recent years, 3D printing has revolutionized how things are made. It is now used in all kinds of rapid prototyping as well as by hobbyists and companies to make finished products and can print not only plastic but also metal, ceramics, and even biological tissue. The next step towards expanding the capabilities of 3D printing technology is to be able to print electronics directly into the 3D structures, as opposed to having to add them in afterwards. Other groups have made some progress in printing conducting inks into and sintering metal onto the 3D structures, and some are working on using pick and place machines to be able to add electronic components directly. Our work seeks to complement this other work by adding the capability to directly print 2D materials such as graphene, MoS_2, and nanoparticle solutions in order to embed complete circuits (e.g., sensors, energy harvesters, or displays) directly into the 3D object.

Two-dimensional materials have showed amazing promise since their discovery, and devices from capacitors to transistors have been demonstrated with graphene, MoS_2 and other 2D-materials. At the same time, nanoparticle inks have also been used to create conductive traces and could potentially prove useful in creating energy storage devices as well. Building on previous work in our group on graphene-based inks and direct printing of graphene-based supercapacitors and strain sensors, this project aims to integrate these technologies into a 3D printer.

The printer we are using is a RepRap Mendel Max 1.5, a fully open-source printer that is relatively inexpensive and readily customizable. Our group has modified the printer hardware to allow for printing of 2D material inks and is working on software to integrate 2D circuits with slices of 3D models. The project aims to print conductive traces and nanoparticle inks including graphene, graphene oxide, and MoS_2 directly into 3D structures made of PLA and other types of plastic.
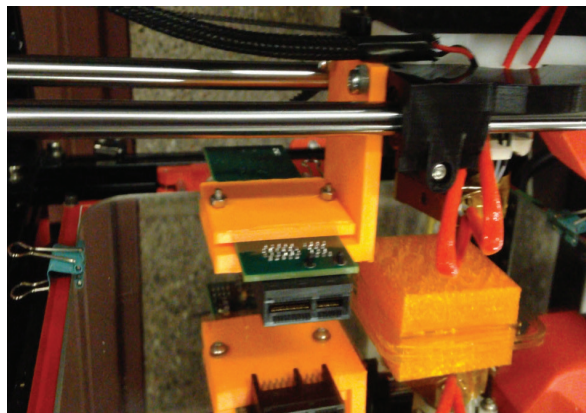
▲ Figure 1: Screenshot from video of the printer printing PLA plastic (right) and graphene oxide ink (left) simultaneously. The green circuit board holds the electronics for the inkjet printerheads that print 2D materials.
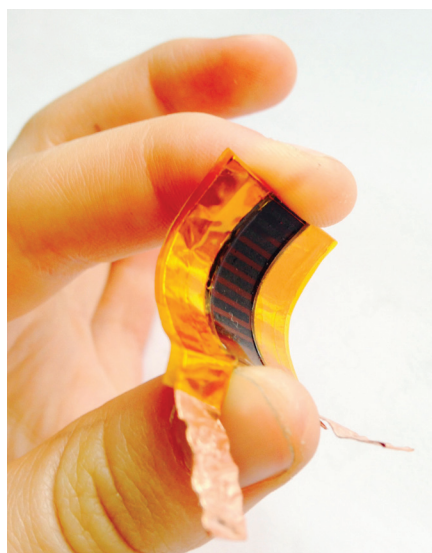
▲ Figure 2: Flexible capacitor made on PET from the laser reduction of graphene oxide. Devices like this could eventually be integrated directly into 3D printed structures for energy storage and delivery.

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Electrospray-Printed 2D Material Humidity Sensors

A. P. Taylor, L. F. Velásquez-García
Sponsorship: Edwards Vacuum

State-of-the-art conductometric gas sensors, based on semiconducting metal oxide films (MOXs), are widely used due to their simplicity and broad applicability to detect many species. However, only a few MOXs show an adequate combination of catalytic activity and thermodynamic stability for gas sensing; these MOXs need to be doped with noble metal nanoparticles to compensate for their poor gas sensitivity, which visibly increases their cost. Fabrication via electrohydrodynamic jetting has recently received attention as a promising candidate for production of low-cost micro- and nanosystems because of its capability to create thin films of high quality without the extreme conditions of standard semiconductor processing (i.e., high vacuum and/or high temperature).

An attractive substitute active material for chemical gas sensing is graphene oxide (GO) because of its high sensitivity to surface adsorbates and compatibility to harsh environments. Thin-film GO sensors have been fabricated with aqueous suspensions of GO flakes using drop casting, air-brush spraying, spin coating, and inkjet printing. Nonetheless, electrospray printing of GO thin-film sensors offers more precise control of the film properties than the other techniques and can also lower production costs through emitter multiplexing. We manufactured GO sensors at low temperatures (< 100 °C) with average layer thickness around 60 nm and characterized their response to humidity in an environmental chamber.

We fabricated devices with multiple electrode configurations on SiO_2-coated Si wafers using contact photolithography and the lift-off technique, and electrosprayed a thin film of GO through a shadow mask onto the electrode structures to form the sensors. We then gold wire-bonded the completed sensor chips into standard IC packages (Figure 1) and placed our GO sensors along with a commercially available humidity sensor (Honeywell HIH-4000) inside an environmental chamber and varied the humidity. A data logger recorded the change in resistance of the GO sensor (Figure 2 top, red curve) and the response of the commercial sensor (Figure 2 top, black curve); the two data sets tracked each other closely. The change in humidity shows a quadratic behavior with the change in resistance of the GO sensor

(Figure 2 bottom) where $\Delta R/R_0 = (R_{1243} - R_0)/R_0$ and $R_0 = 39 k\Omega$. The results were reproducible on different days, and the GO sensors showed no signs of degradation after storage for more than one month.
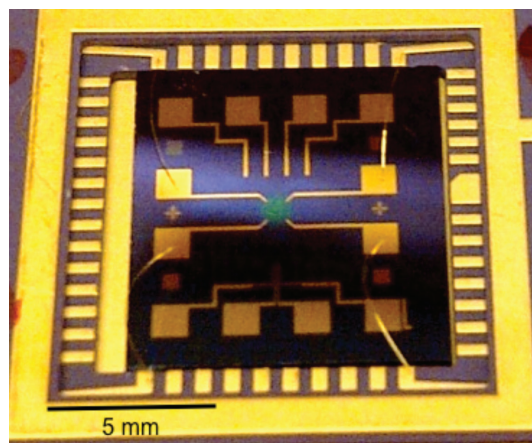
▲ Figure 1: Electrospray-printed GO sensor (greenish dot at center) on top of Au electrodes in the Van der Pauw configuration.
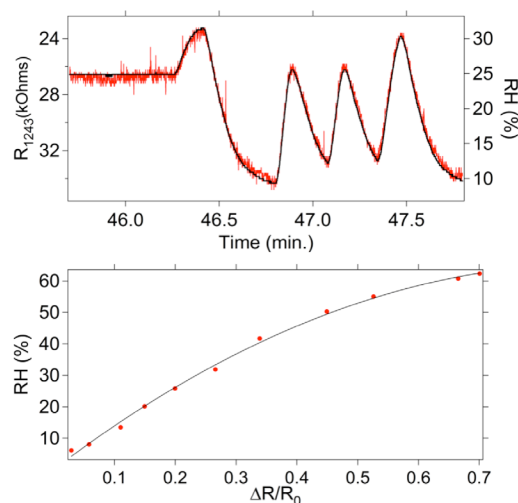
▲ Figure 2: GO sensor response to humidity (red) compared with a commercially available sensor (top) and relative humidity as a function of the sensor response (bottom).

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Quantitative Analysis and Modeling of Templated Solid-State Dewetting of Thin Single-Crystal Ni Films

G. H. Kim, R. V. Zucker, Y. A. Shin, W. C. Carter, C. V. Thompson
Sponsorship: National Science Foundation

Thin films are generally metastable in the as-deposited state and will dewet (agglomerate) when heated. Nanometer-scale films (<100 nm thick) can dewet at temperatures well below the melting temperature of the film, and dewetting occurs while the film remains solid. This phenomenon can limit the use of very thin films in microsystems, but it can also be used to controllably produce complex structures. Dewetting occurs through retraction of the edges of naturally forming holes or at patterned edges of films. In single-crystal films, anisotropy in surface energy and diffusivity drives the dewetting process to result in regular patterns that relate to the crystal symmetry. We are investigating use of anisotropic dewetting as a self-assembly method to generate complex, small, predetermined patterns (Figure 1). A quantitative understanding of dewetting mechanisms is critical for design of self-assembled structures made through dewetting. We studied the Rayleigh-like instability of long strips patterned on single crystal Ni films. These long strips dewet to form wire-like structures, which eventually break-up into islands, similar to the Rayleigh instability of free-standing cylinders. We found that the characteristic spacing of the dewetted islands and the dewetting rate are highly anisotropic and the spacing is dependent on the total surface energy of the wires (Figure 2). Additionally, a kinetic Monte Carlo simulation has been carried out to test our understanding of dewetting mechanisms. This model provides good agreement with experimental observations. We are also developing a three-dimensional phase-field model for dewetting of materials with isotropic and/or anisotropic surface energies.
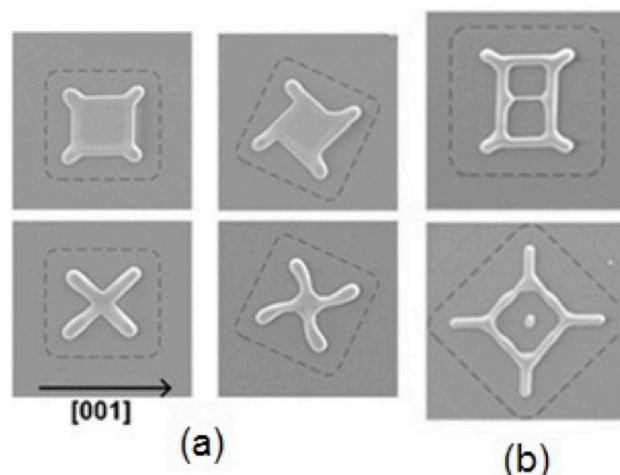
▲ Figure 1: (a) Partially dewetted patches patterned from a (100) film into squares with different in-plane orientations; top is an earlier time than bottom. (b) Dewetting patterns of larger squares.
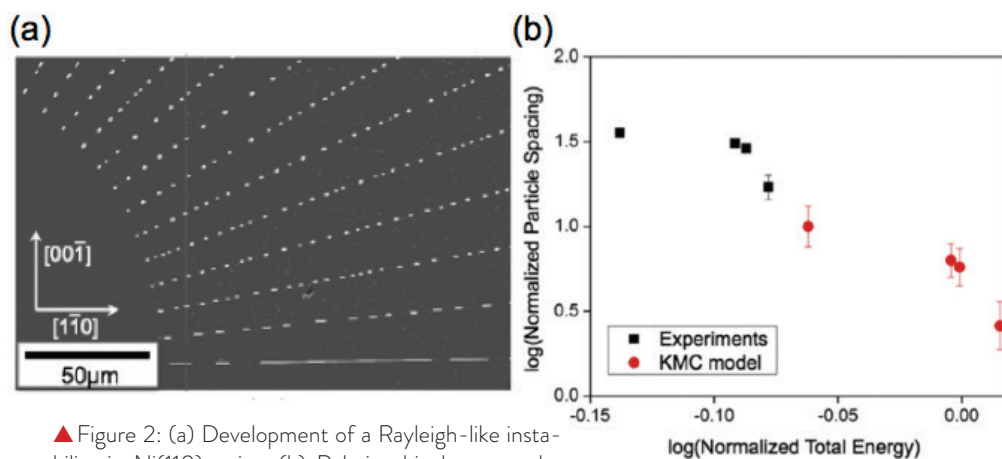
▲ Figure 2: (a) Development of a Rayleigh-like instability in Ni(110) strips. (b) Relationship between the particle spacing as a function of the total surface energy of the wire.

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Metal-Assisted Chemical and Anodic Etching to Form Arrays of Silicon Nanostructures

W. Zheng, C. Q. Lai, P. Lianto, W. K. Choi, C. V. Thompson
Sponsorship: Singapore-MIT Alliance for Research and Technology

Metal-assisted chemical etching (MACE) has been used to fabricate a wide array of semiconductor nanostructures using a room temperature wet etching process. These include arrays of nanowires with diameters down to 20 nm and aspect ratios as high as 220 to 1 (Figure 1). In a typical MACE process, a metal film is deposited on silicon, patterned, and exposed to an etchant consisting of HF and an oxidant (e.g., H_2O_2). The metal catalyzes reduction of the oxidant and provides an electronic hole for oxidation of silicon to form a soluble reaction product. This process causes etching of the Si at the metal/Si interface, and results in the controlled formation of un-etched silicon nanostructures. Beyond this point, the detailed mechanisms of MACE have remained unclear. This lack of knowledge has inhibited extension of the use of this technique to a wider range of semiconductors.

In addition to using the MACE process to fabricate sensors, microbatteries, and supercapacitors (discussed elsewhere), we have carried out basic research on the mechanisms of MACE. In recent work, we etched mechanically supported metal strips to measure the forces that keep the metal and silicon in contact during etching, and identified them as Hamaker forces. We have also shown how these forces depend on the chemistry of the etchant. In addition, we have clarified the role of excess holes in causing porosity in the resulting nanostructures and shown that application of an external electric field can be used to control porosity.

In the past year, we have demonstrated a new electrochemical method for formation of arrays of silicon nanostructures, metal-assisted anodic etching (MAAE). In this process, the etchant consists of HF alone and does not include an oxidant. Holes are supplied through an external circuit, with anodic contact to either the metal or the silicon (Figure 2). In both cases, the metal still catalyzes the etching process and leads to controlled formation of arrays of nanostructures (such as nanowire). This discovery, and its analysis, provide new flexibility in the use of metal catalyzed electrochemical etching, and also provides new insights into the mechanisms of both MAAE and MACE.
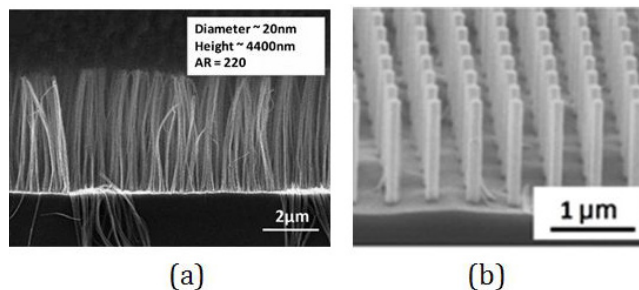
▲ Figure 1: Silicon nanowire array made using MACE with metal films patterned using (a) block copolymer lithography and (b) interference lithography.
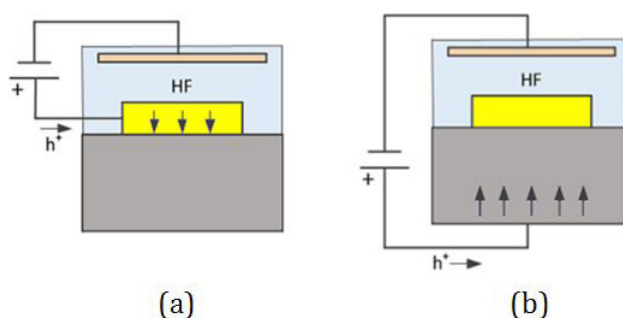
▲ Figure 2: Configurations for metal-assisted anodic etching (MAAE) with (a) anodic contact to the metal, and (b) anodic contact to the silicon.

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Thermal Conductivity Spectroscopy Using Nanostructures

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Sponsorship: S3TEC, Department of Energy

A material's ability to conduct heat is measured by its thermal conductivity. In semiconductors and dielectrics, the predominant heat carriers are quantized lattice vibrations (or phonons), which have a wide range of frequencies and mean free paths (MFPs). The mean free path of each phonon mode decribes the average distance that specific phonon mode travels in between two consecutive scattering events. The thermal conductivity accumulation function describes the fraction of the contribution of phonons with MFPs shorter than a cutoff MFP. The Nanoengineering Laboratory in MIT's Department of Mechanical Engineering hosts a femto-second laser pump-probe system to measure thermal conductivity of bulk materials and thin films, as well as interfacial thermal resistance. Currently, this system is being advanced to measure phonon MFP distributions in different materials.

The idea of probing phonon MFP distribution is based on examining heat transport in the quasiballistic regime that occurs when characteristic heat source sizes are comparable with phonon MFPs. We first observed quasiballistic phonon transport in crystalline sililcon at cryogenic temperatures when the phonon MFPs are longer than the laser beam diameters that determine the size of the heat source. This observation led to the idea of mapping out phonon MFP distributions by systematically changing the size of the heat source. Since phonon MFPs in many materials span sizes from several nanometers to hundreds of microns, one nontrivial challenge is to create nanometer scale heat sources comparable to the phonon MFPs. We fabricated nanostructures, subjected them to laser heating as heat sources, and developed techniques to distribute phonon MFPs in different materials such as GaAs and GaN. Now, we are simplifying the technique using 1D metallic gratings. The metal lines serve as heaters and thermometers. Our experimental observation that when the heat source size is smaller than the phonon MFPs, the classical Fourier heat conduction theory underpredicts the temperature rise also has significant implications for thermal management in microelectronic devices.
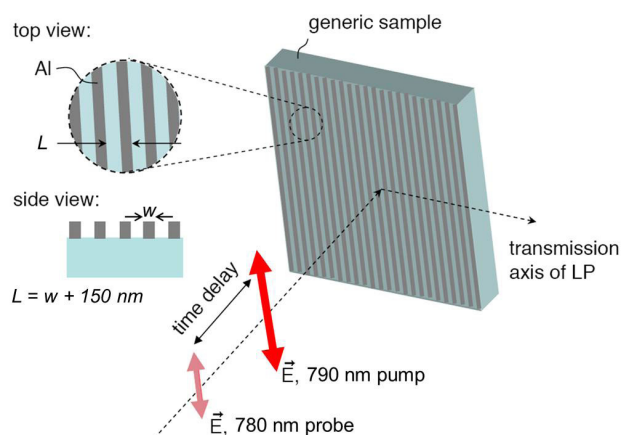
▲ Figure 1: Schematic of our sample structures and experimental technique. The samples are composed of metal grating on top of substrates of interests and are measured by an ultrafast optical time-domain thermoreflectance technique in the RK lab at MIT.
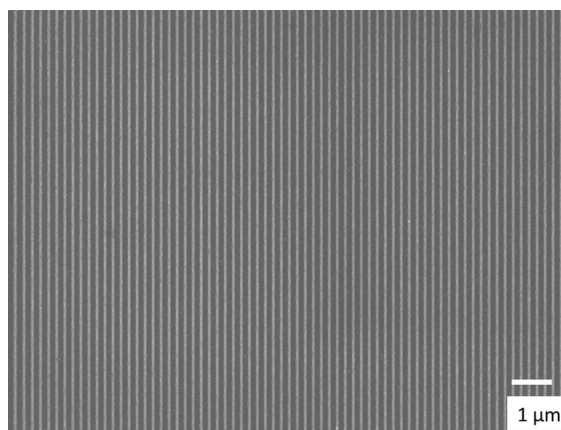
▲ Figure 2: Fabricated 50-nm-wide (period = 200 nm) one-dimensional aluminum metal grating on top of crystalline silicon substrate using the ebeam machine Elionix in the Microsystems Technology Laboratory at MIT.

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Inducing Superconductivity in Semiconducting Atomically Thin Layers

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Sponsorship: CIQM, Ramon Areces Foundation

The combination of semiconducting transition metal dichalcogenides—chemical formula MX_2, with M: Mo, W; and X: S or Se—with modern nanofabrication techniques (exfoliation and van der Waals stacking) has paved the way for the realization of extremely clean two-dimensional electronic systems, so that unprecedented physical properties can now be observed. In particular, the Mo chalcogenides have recently drawn attention due to the occurrence of superconductivity by accumulation of a high density of electrons at their surface. Although the induction of superconductivity has been achieved in bulk crystals and thick flakes, no similar studies in atomically thin layers have appeared. Particularly appealing is the case of single-layer systems where the breaking of the inversion symmetry in single layers in addition to a strong spin-orbit coupling could provide access to the valley degree of freedom within the superconducting state. This access could give rise to exotic phenomena such as unconventional Andreev reflection or superconducting spin valves.

Instrumental to the generation of a high carrier density is the electrical double layer technique, which involves the use of an ionic liquid top gate. However, the use of a liquid imposes several technical challenges. First, it freezes as the device is cooled down, generating mechanical stress. Second, it exhibits a strong chemical reactivity with standard metallic contacts. This problematic prevents the normal characterization of the physical properties down to base temperature. In addition, working on Si/SiO_2 substrates implies the presence of charged surface states and electron/hole puddles. This presence has been found to limit the sample quality and reduce the carrier mobility.

Both problems were tackled by using a new fabrication approach. MoS_2 single layers were exfoliated on top of a thin film of polymer. A layer was selected and transferred onto Au contacts pre-evaporated on an h-BN surface (see Figure 1a). The current strategy improves the performance of the final devices with respect to standard evaporated contacts: it isolates the metal contacts from the chemical corrosion of the liquid; the h-BN provides a defect-free surface; and the polymer film serves as a strain-relieving buffer interface. As a result, the devices

fabricated have been successfully characterized to temperatures below 1 K and exhibit low ohmic contact resistances and maximum Hall mobilities of over 900 cm²/Vs measured at 4 K (see Figure 2).
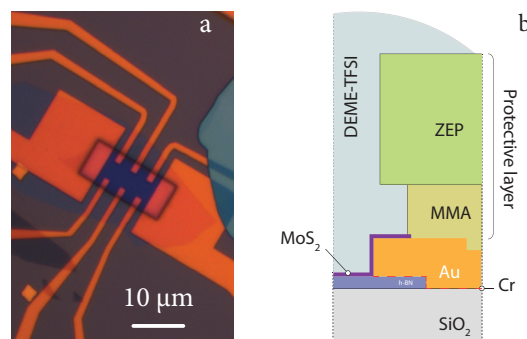
▲ Figure 1: (a) Optical micrograph of a single-layer MoS_2 EDL device. Rectangular frame around device's transport channel is a hole in protective MMA layer. (b) Scheme showing multilayer cross-section of device shown in (a) including ionic liquid (DEME-TFSI).
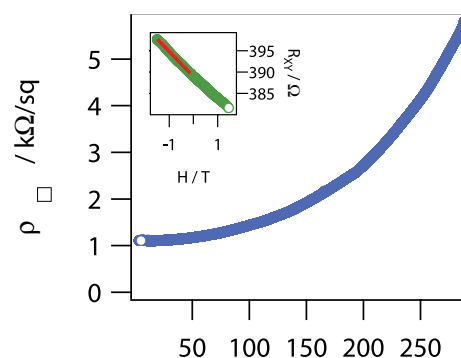
▲ Figure 2: Four-probe transport properties measured at ionic liquid gate voltage V_{ion} = 1.3 V. Inset shows Hall resistance as a function of external applied field. Linear fit provides a mobility of 907.4 cm²/Vs @ 4 K for carrier density of 1×10^{14} cm^{-2}.

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Electrostatic Coupling between Two Surfaces of a Topological Insulator

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Topological insulators have been undergoing intense theoretical and experimental research on the properties of their unique surface electronic states. The presence of bulk carriers has hampered experimental progress, so a large variety of growth techniques and device structures have been implemented in the attempt to access a surface-state dominated regime. For example, quaternary compounds of the form $Bi_{2-x}Sb_xTe_{3-y}Se_y$ have a significantly suppressed bulk contribution to transport and so are good candidates for surface-state dominated transport in nanoscale devices.

Here we report our successful *in situ* identification of two surface states on a single crystal of $Bi_{1.5}Sb_{0.5}Te_{1.7}Se_{1.3}$ as well as clear electric field penetration through the bulk, indicating full bulk suppression and surface-state dominance. In Figures 1a-b we show typical gating characteristics of the resistance. We see two distinct resistance peaks that are modulated by both gate voltages, which is strong evidence for two distinct surface states contributing to the electronic transport of the system. Additionally, this modulation provides evidence for electric field penetration; otherwise, the back-gate electrode could not affect the upper surface state. To understand the motion of the resistance peaks quantitatively, we developed an electrostatic charging model represented in Figure 1c, details of which can be found in the further reading references. Applying this model to the resistance peak allows for a linear transformation from gate voltages to chemical potential and carrier density. Figure 1d is a zoom-in of the motion of the upper surface resistance peak as a function of both gate voltages, and we find an excellent fit of the transport data to independently taken angle-resolved photoemission spectroscopy data of the surface state dispersion (Figure 1e), showing that our system is indeed surface-state dominated.
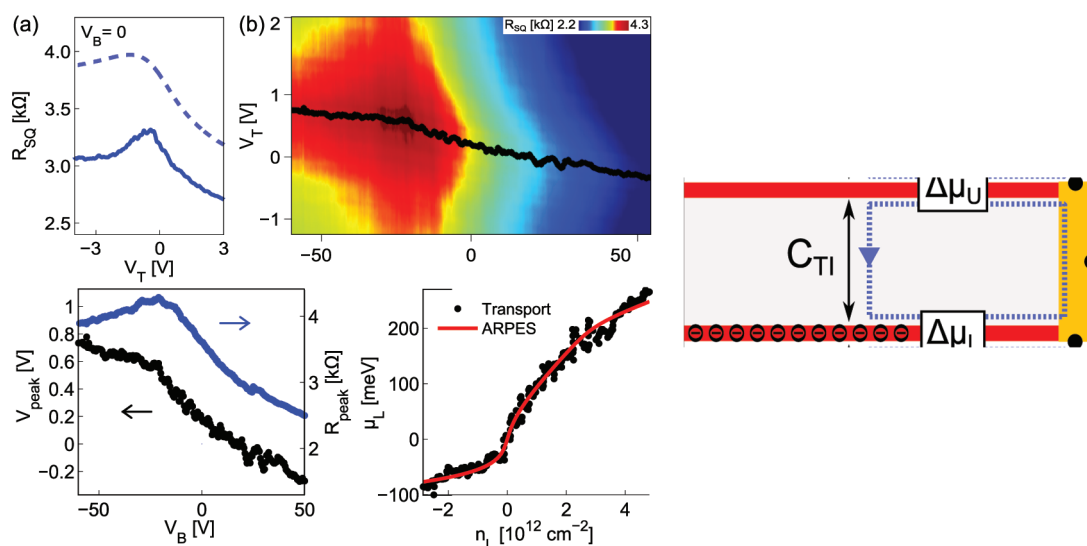
▲ Figure 1: (a) Resistance vs. gate-voltage trace. Solid and dashed lines are at 4K and room temperature, respectively. (b) Resistance vs. top and bottom gate voltages. Black dots mark the upper surface resistance peak. (c) A schematic of the electrostatic charging model. (d) A close-up of the trajectory of the resistance peak from Figure 1b (black) and the resistance along that trace (blue). (e) Fit of transport-extracted dispersion relationship (black) to independently measured spectroscopy (red).

FURTHER READING

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Research Centers

Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Seven faculty members participate in the CICS: Hae-Seung Lee (director), Duane Boning, Anantha Chandrakasan, David Perreault, Charles Sodini, and Vivienne Sze. In September 2014, we welcomed our newest CICS faculty member, Ruonan Han. Prof. Han's research focuses on high frequency circuits and their applications reaching up to the THz ranges. Terahertz wave is opening up tremendous opportunities in non-ionizing medical imaging, biochemical molecule spectroscopy, ultra-high-speed communication, etc. His research group focuses on bridging the THz Gap that is difficult to reach via traditional electronic and optic methods, spanning from electronic device engineering, analog/microwave circuit design, to innovations of system architecture.

CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, biomedical circuits, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy. At present, participating companies include Analog Devices, IBM, Linear Technology, Maxim Integrated, Marvell Technology Group, MediaTek, and Texas Instruments.

CICS's research portfolio includes all research projects that the seven participating faculty members conduct, regardless of source(s) of funding, with a few exceptions.

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research. More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

MIT/MTL Center for Graphene Devices and 2D Systems

Professor Tomás Palacios, Director

The MIT/MTL Center for Graphene Devices and 2D Systems (MIT-CG) brings together, MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional materials.

Graphene and other two-dimensional (2D) materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines thanks to their extreme properties. These materials are the lightest, thinnest, strongest materials we know of, at the same time that they have very rich electronic and chemical properties. For more than 40 years, MIT has led the work on the science and engineering of 2D materials. More recently, since 2011, the MIT-MTL Center for Graphene Devices and 2D Systems (MIT-CG) has played a key role in coordinating most of the work going on at MIT on these new materials, and in bringing together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced technologies and strategies that enable 2D materials, devices and systems to provide discriminating or break-through capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials, to optoelectronics, RF communications and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools and analysis for the creation of a vision for the future of new systems enabled by 2D materials.

Some of the multiple benefits of the Center's membership include complimentary attendance to meetings, Industry Focus days, and webcasting of seminars related to the main research directions of the Center. The members of the Center also gain access to a resume book that connects students with potential employers, as well as to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today's challenges for these materials, devices and systems.

MIT/MTL Gallium Nitride (GaN) Energy Initiative

Professor Tomás Palacios, Director

The MIT/MTL Gallium Nitride (GaN) Energy Initiative (MIT-GaN) is an inter-departmental program that brings together 10 MIT faculty and more than 40 other researchers and industrial partners to advance the science and engineering of GaN-based materials and devices for energy applications.

The GaN Energy Initiative provides a holistic approach to GaN research for energy applications and it coordinates work on the growth, technology, novel devices, circuits and systems to take full advantage of the unique properties of GaN. The GaN Energy Initiative is especially interested in developing new beyond-state-of-the-art solutions to system-level applications in RF power amplification, mixed signal electronics, energy processing and power management, as well as advanced optoelectronics. Most of the work is done on GaN materials and devices that are compatible with Si fabrication technologies, in close collaboration with industrial partners to accelerate the insertion of these devices into systems.

The MIT/MTL Gallium Nitride(GaN)Energy Initiative organizes numerous activities to advance the understanding of GaN materials, technology and devices. Some of these activities include webcast of seminars and annual meetings, as well as joint collaborations with industry partners. The Initiative also elaborates a resume book of graduating students and provides timely access to white papers and pre-prints through its website.

The MIT Medical Electronic Device Realization Center

Professor Charles Sodini, Director

The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will in turn transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personal medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personal medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient's needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry's societal transformation, *Medical Electronic Devices*.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacture devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners' diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure and cerebral blood flow velocity. Since its founding in 2011 MEDRC has grown from two to **five sponsoring companies** with several other companies in serious discussions. There are currently **fifteen MEDRC funded research projects** that are defined by **ten MIT faculty, ten clinicians** and our sponsoring companies supporting approximately **twenty students**. A visiting scientist from a project's sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

In addition to the strong relationship with MTL, MEDRC is associated with MIT's Institute for Medical Engineering and Science, IMES, that has been charged to serve as a focal point for researchers with medical interest across MIT. MEDRC has been able to create strong connections with the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. With the support of MTL and IMES, MEDRC will serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.

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SELECTED PUBLICATIONS

E.R. Meshot, Z. Zhao, W. Lu, A.J. Hart. Self-ordering of small-diameter metal nanoparticles by dewetting on hexagonal mesh templates. *Nanoscale,* 6(17):10106-10112, 2014. http://dx.doi.org/10.1039/C4NR01501K.

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Semiconductor devices. Fabrication and device physics of silicon-based heterostructures and nanostructures. High mobility Si and Ge-channel MOSFETs, nanowire FETs, novel transistor structures, silicon based photovoltaics, and silicon-germanium photodetectors for electronic/photonic integrated circuits.

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SELECTED PUBLICATIONS

W. Chern, P. Hashemi, M. Kobayashi, DG Park, J.L. Hoyt, "Plasma Post-Oxidation for High Mobility Strained-Ge pFETs with Aggressively Scaled High-κ Dielectrics," *ECS Transactions,* vol. 64, no. 6, pp. 329-335, Oct. 2014.

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Lee, J., T. Laoui, and R. Karnik, "Nanofluidic transport governed by the liquid/vapour interface," *Nature Nanotechnology*, 9(4): p. 317-23, 2014.

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SELECTED PUBLICATIONS
J. Chou, S.-G. Kim, "Omnidirectional, spectrally selective, wafer-scale fabricated metallic diectric 2-D photonic crystals for high temperature energy conversion," *Solid-State Sensor and Actuator Workshop*, Hilton Head, SC, 2014.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS
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SELECTED PUBLICATIONS

A. Suleiman, V. Sze, "Energy-Efficient HOG-based Object Detection at 1080HD 60 fps with Multi-Scale Support," in *IEEE International Workshop on Signal Processing Systems (SiPS),* October 2014, pp. 256-261.

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SELECTED PUBLICATIONS
S.T. Boles, C.V. Thompson, O. Kraft, and R. Mönig, "In situ tensile and creep testing of lithiated silicon nanowires," *Applied Physics Letters* 103, p. 263906, 2013, 104, p. 099902, 2014.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

M. E. Swanwick, C. D. Dong, P. D. Keathley, A. Fallahi, F. X. Kärtner, and L. F. Velásquez-García, "Pitch scaling of ultrafast, optically-triggered silicon field emitter arrays," *Technical Digest of the 27th International Vacuum Nanoelectronics Conference (IVNC 2014)*, Engelberg, Switzerland, pp. 69 -70, July 6–10, 2014.

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SELECTED PUBLICATIONS
S. Varma and J. Voldman, "A cell-based sensor of fluid shear stress for microfluidics," *Lab on A Chip,* vol. 15, pp. 1563-73, 2015.

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- **Adrian Grossman** (L. DANIEL)
  PCB design for a Wearable Hydration Sensor.

- **Christopher Klingshirn** (A. AGARWAL)
  Infrared Photoconductive PbTe Film Processing and Oxygen Sensitization

- **Abel Philip** (L. DANIEL)
  MetroExpress: A Platform for Efficient Package Delivery.

- **Jennifer Selvidge** (P. O. ANIKEEVA)
  Characterization and Connectorization of Optoelectronic Neural Probes

- **Nathan Spielberg** (A. J. HART)
  Maskless Photopatterning of Cells in Microfluidic Devices

- **Veronica Szlarzewski** (A. J. HART)
  A Mechanism for Testing the Torsional Mechanics of Origami-Inspired Hinges

- **Christina Tringides** (P. O. ANIKEEVA)
  Materials Selection and Processing for Reliable Neural Interfaces

M.ENG.

- **Chen Dan Dong** (L. F. VELÁSQUEZ-GARCÍA)
  Scaling of Ultrafast Photon-Triggered Field Emission Cathodes Composed of Arrays of Sharpened Single-Crystal Si Pillars

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  Parallel Implementation of Sample Adaptive Offset Filtering Block for Low-Power HEVC Chip

- **Letitia Li** (J. A. DEL ALAMO)
  Switching Circuit Energy Balance in iLabs on Experimental Lab Server Architecture.

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  Reactive DC Magnetrin Sputtering Of Ultrathin Superconducting Niobium Nitride Films

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  Three-Dimensional Nanofabrication By Electron-Beam Lithography And Directed Self-Assembly

- **Yuxuan Lin** (M. S. DRESSELHAUS AND T. PALACIOS)
  Optical Properties of Two-Dimensional Transition Metal Dichalcogenides

- **Damak Maher** (K. K. VARANASI)
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- **Philippa Mothersill** (V. M. BOVE JR.)
  The Form of Emotive Design

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  Parallel Nano-Manufacturing via Electro-Hydrodynamic Jetting from Externally-Fed Emitter Arrays

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  Stealth Dicing Characterization, Optimization, Integration, and Operations Management for Ultra-Thin Stacked Memory Dies

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  Fabrication of Graphene-on-GaN Vertical Transistors

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- **Santiago Alfaro** (V. M. BOVE JR.)
  Digital Synesthesia: Using Mobile Technology and Sensory Substitution to Interact with Our World

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Glossary

MIT ACRONYMS

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
KI	David H. Koch Institute for Integrative Cancer Research
MAS	Program in Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MITEI	MIT Energy Initiative
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
S3TEC	Solid State Thermal Energy Conversion Center
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
⌐ **SMART**	Singapore-MIT Alliance for Research and Technology Center
⌐ **SMART-LEES**	SMART Low Energy Electronic Systems Center
TPP	Technology and Policy Program

OTHER ACRONYMS

AFOSR	Air Force Office of Scientific Research
AFRL	Air Force Research Laboratory
ARL	Army Research Laboratory
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
CUNY	The City University of New York
DARPA	Defense Advanced Research Projects Agency
⌐ **DAHI**	DARPA Diverse Accessible Heterogeneous Integration Program
⌐ **E-PHI**	DARPA Electronic-Photonic Heterogeneous Integration Program
⌐ **MPC**	DARPA Microscale Power Conversion Program
⌐ **MTO**	DARPA Microsystems Technology Office
DOE	Department of Energy

FENA	Center for Functional Engineered Nano Architectonics
GBMF	Gordon and Betty Moore Foundation
IARPA	Intelligence Advanced Research Projects Activity
IEDM	International Electron Devices Meeting (IEEE)
IEEE	Institute of Electrical and Electronics Engineers
ISSCC	International Solid-State Circuits Conference (IEEE)
MASDAR	Masdar Institute of Science and Technology
MRS	Materials Research Society
NASA	National Aeronautics and Space Administration
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
NSRC	Natural Sciences and Engineering Research Council (Canada)
NSF	National Science Foundation
⌐ **CIQM**	NSF Center for Integrated Quantum Materials
⌐ **CSNE**	NSF Center for Sensorimotor Neural Engineering
⌐ **E3S**	NSF Center for Energy Efficient Electronics Science
⌐ **GRFP**	NSF Graduate Research Fellowship Program
⌐ **MRSEC**	NSF Materials Research Science and Engineering Centers
⌐ **NCN-NEEDS**	NSF Network for Computational Nanotechnology - Nano-Engineered Electronic Device Simulation Node
NTU	Nanyang Technological University
NUS	National University of Singapore
ONR	Office of Naval Research
⌐ **DRIFT-MURI**	Design-for-Reliability Initiative for Future Technologies - Multidisciplinary University Research Initiative
SRC	Semiconductor Research Corporation
TSMC	Taiwan Semiconductor Manufacturing Company

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Symbols