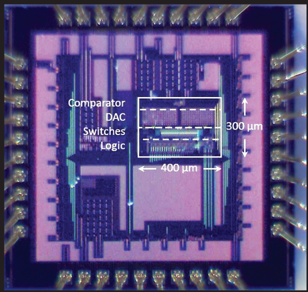

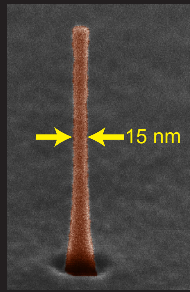

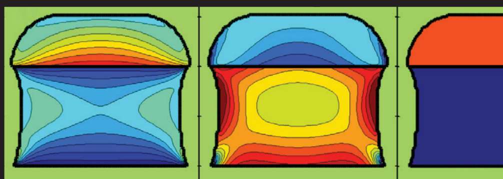

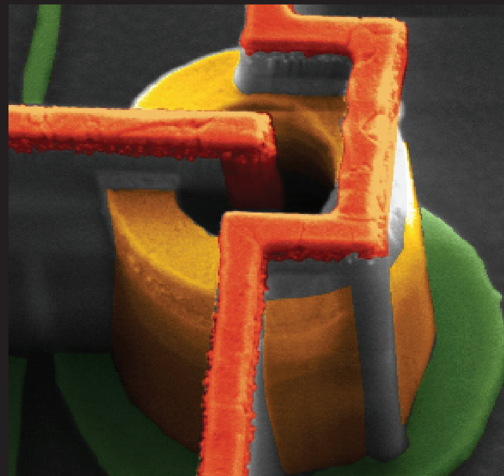

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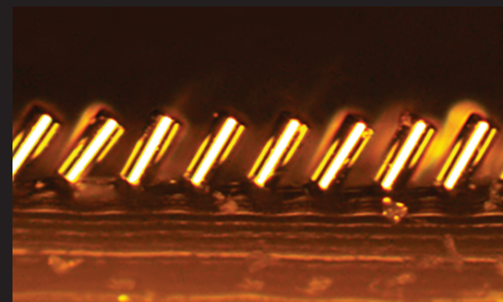

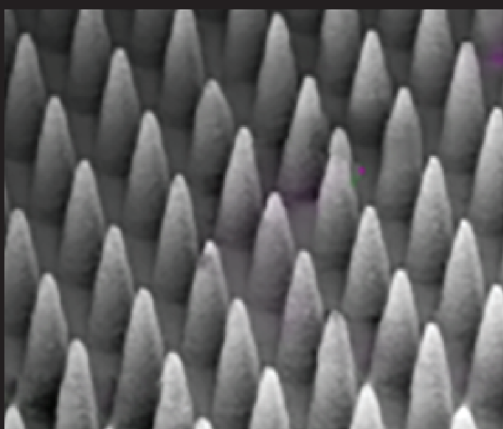

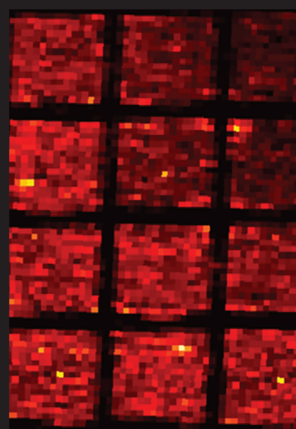

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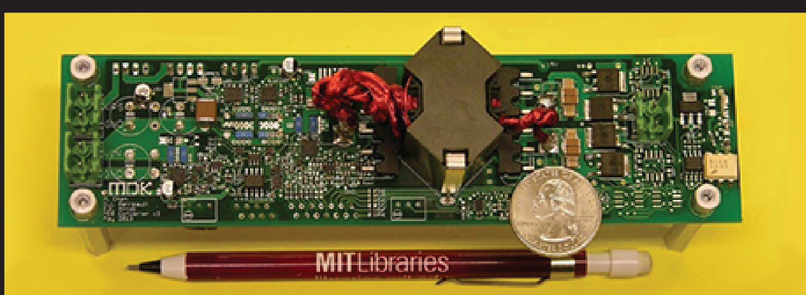

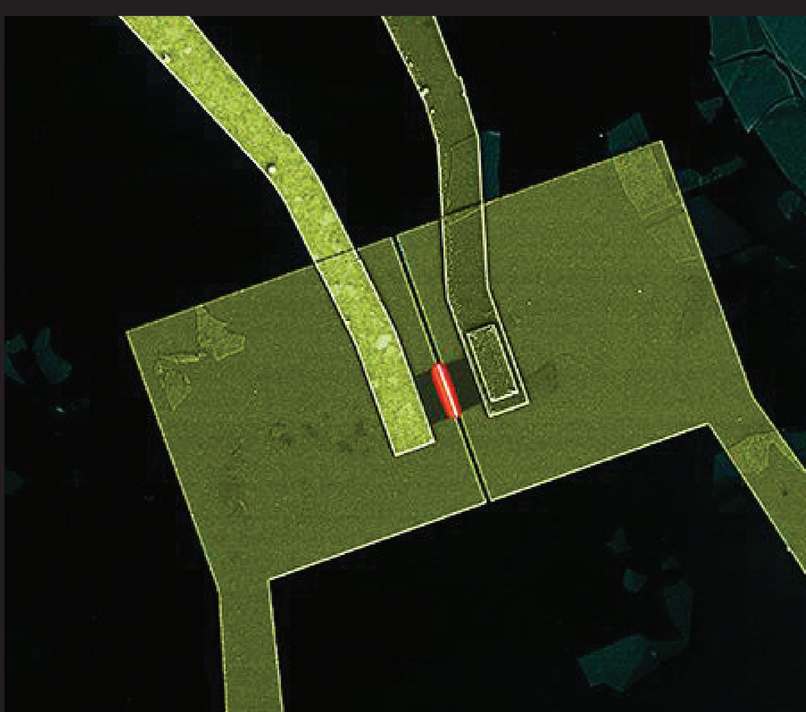

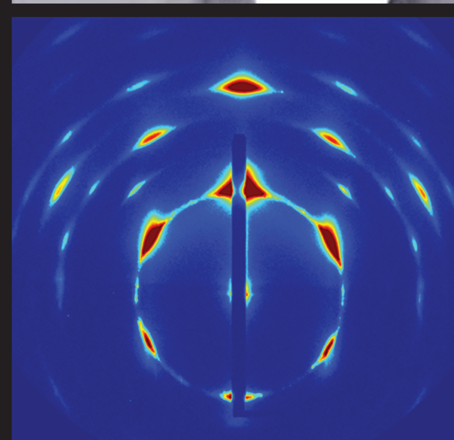

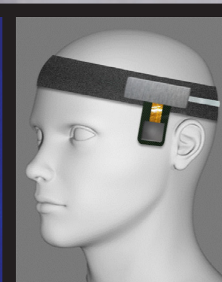

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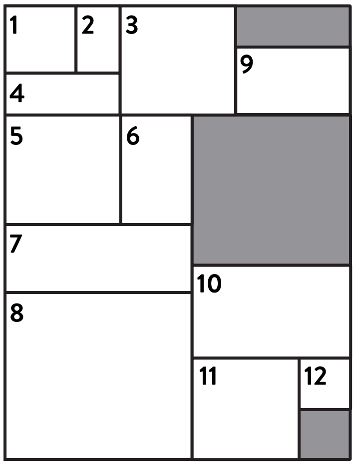

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Foreword

The 2014 Annual Report of the Microsystems Technology Laboratories highlights the research and educational activities of faculty, staff and students associated with MTL during MIT Fiscal Year 2014.

MTL's mission is to foster world-class research and education in Microsystems, broadly construed. As showcased in this report, MTL's activities encompass integrated circuits, systems, electronic and photonic devices, MEMS, bio-MEMS, molecular devices, nanotechnology, sensors and actuators, to name a few. MTL's research program is largely interdisciplinary. MTL's facilities are open to the entire MIT community and beyond. Over 600 MIT students and postdocs from 18 different Departments, Laboratories or Centers carried out their research in MTL's facilities in the last fiscal year.

To accomplish its mission, MTL manages a set of experimental facilities in Bldgs. 39 and 24 that host in excess of 150 processing and analytical tools. We strive to provide a flexible fabrication environment that is at the same time capable of long-flow integrated processes that yield complex devices, as well as low-barrier access to fast prototyping of structures and devices. Our fabrication capabilities include diffusion, lithography, deposition, etching, packaging and many others. Our lab can handle substrates from odd-shaped small pieces to 6-inch wafers. The range of materials continues to expand beyond Si and Ge to include III-V compound semiconductors, nitride semiconductors, carbon-based materials, polymers, glass, organics and others.

MTL also manages an information technology infrastructure that supports state-of-the-art computer-aided design (CAD) tools for device, circuit and system design. Together with a set of relationships with major semiconductor manufacturers, this provides access for our users to some of the most advanced commercial integrated circuit processes available in the world today.

MTL could not accomplish its mission without the vision, commitment and generosity of a number of companies that comprise the Microsystems Industrial Group (MIG). The MIG supports the operation of MTL's facilities but it also provides counsel to the faculty on research directions, trends and industrial needs. The list of current MIG members can be found in the Acknowledgement section of this report.

In the Fall of 2014, we will celebrate the 30th anniversary of the creation of MTL. From an initial emphasis on semiconductors and electronics, over the 30 years of its life, the technologies that underpin MTL's activities and their domains of application have greatly expanded. The 2014 Annual Report is the broadest in scope to date with abstracts describing research on nanofibers, medical devices, microfluidics, photonic phased arrays and quantum dot photovoltaics, among many exciting research projects.

The research activities described in these pages would not be possible without the dedication and passion of the fabrication, IT and administrative staff of MTL. Day in and day out, they strive to help MTL users to accomplish their goals. They do this in an unassuming manner. Their names do not usually end up in the research papers, but that does not diminish the significance of their contributions. To them and to all of you who support, in one way or another, the activities of MTL, a heartfelt thank you!

Jesús A. del Alamo
Director, Microsystems Technology Laboratories
Donner Professor, Department of Electrical Engineering and Computer Science
August 2014

Acknowledgments

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Work centers on the mid-IR (MIR) regime. Although previous silicon microphotonic devices predominantly utilized the NIR range, the MIR regime is extremely interesting for hyperspectral imaging and chem-bio sensing because most chemical and biological toxins have their fingerprints in this range. Work on MIR materials and devices is creating a planar, integrated, Si-CMOS-compatible microphotonics platform to enable on-chip imaging and sensing applications.
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617-253-4693
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617-324-0272
berggren @ mit . edu

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617-253-0931
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Physical properties of organic and organic/inorganic nanocrystal composite thin films and structures, and development of nanostructured electronic and optoelectronic devices. Applications of nanostructured materials in large-scale technologies.
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617-253-7012
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Anantha P. Chandrakasan
Design of digital integrated circuits and systems. Energy efficient implementation of signal processing, communication and medical systems. Circuit design with emerging technologies.
Rm. 38-107
617-258-7619
anantha @ mtl . mit . edu

Gang Chen
Micro- and nanoscale heat transfer and energy conversion with applications in thermoelectrics, photovoltaics, solar-thermal energy to electrical energy conversion, and microelectronics; nano-mechanical devices and micro-electro-mechanical systems; radiation and electromagnetic metamaterials; nanoengineered high thermal conductivity polymers and liquids; and desalination.
Rm. 3-260
617-253-0006
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Luca Daniel
Development of numerical techniques: uncertainty quantification and stochastic integral equation solvers for high dimensional parameter spaces. Parameterized model order reduction for linear and nonlinear dynamical systems. Applications include: nanodevices (CMOS MEMS resonators, silicon photonic devices, analog RF circuits and passives), the human cardiovascular circulatory system, and high resolution parallel transmission Magnetic Resonance Imaging (MRI) systems.
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617-253-2631
luca @ mit . edu

Jesús A. del Alamo
Nanometer-scale compound semiconductor transistor technologies for logic, RF, microwave and millimeter wave and power switching applications. Reliability of compound semiconductor transistors. Technology and pedagogy of online laboratories for engineering education.
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617-253-4764
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Development of scalable semiconductor quantum information processing devices and systems, quantum enhanced sensors, and nanophotonic and electro-optic devices.
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617-324-7014
englund @ mit . edu

Nicholas X. Fang
Nanophotonic and acoustic materials and devices. Physics, nanofabrication, instrumentation.
Rm. 3-435B
617-253-2247
nicfang @ mit . edu

Clifton G. Fonstad, Jr.
Compound semiconductor heterostructure devices and physics. Optoelectronics: laser diodes, photodiodes, quantum effect devices, and optoelectronic integrated circuits. Monolithic heterogeneous integration on Si-CMOS. Multi-waveguide probe arrays for optogenetic brain studies. μ-scale thermophotovoltaics.
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Rm. 36-841
617-253-2290
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Semiconductor devices. Fabrication and device physics of silicon-based heterostructures and nanostructures. High mobility Si and Ge-channel MOSFETs, nanowire FETs, novel transistor structures, silicon based photovoltaics, and silicon-germanium photodetectors for electronic/photonic integrated circuits.
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Circuits and Systems for Information Processing, Communications, Multimedia, and Energy Management

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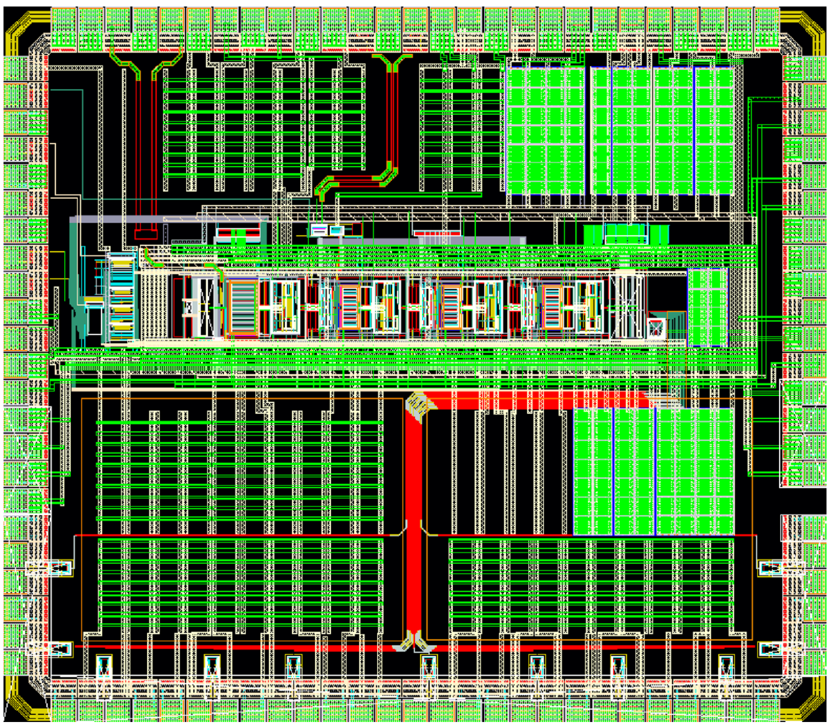
12-bit 330MS/s CMOS Pipelined Analog-to-Digital Converter

H.H. Boo, H.-S. Lee, D.S. Boning
Sponsorship: Masdar Institute of Science and Technology / MIT Cooperative Program

Pipelined ADC architecture is widely applicable as it offers high-resolution and wide-bandwidth data conversions. The scaling of the CMOS devices, however, accompanies lower supply voltage, reduced intrinsic transistor gain, and degraded signal-to-noise ratio (SNR). The op-amp becomes the performance bottleneck as it suffers from low gain, bandwidth, and noise issues. Approaches have been reported in the literature that address these problems by either employing low-performance op-amps and resolving degradations by digital calibrations or proposing new architectures that replace the op-amps.

We propose innovative circuit techniques to relax the op-amp gain, bandwidth, and noise requirements. The approach enables an energy-efficient high resolution and high sampling speed pipelined ADC. A 12-bit, 330MS/s prototype ADC chip is designed in TSMC 65-nm LP. The differential input signal range is 1.5V peak-peak and the ADC consumes 49mW of power with 1.2V power supply at 330MS/s. The full chip layout is shown in Figure 1, and the core area size is $0.56mm^2$. The fabricated prototype is currently being tested.



◀ Figure 1: Full chip layout. The die area is 2.6mm x 2.26mm; the ADC core area is 1.55mm x 0.36mm.

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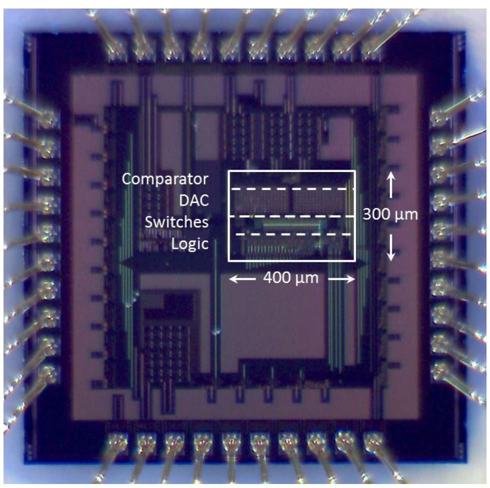
A 10-bit SAR ADC with Data-Dependent Energy Savings Using LSB-First Successive Approximation

F. M. Yaul, A.P. Chandrakasan
Sponsorship: Shell, Texas Instruments

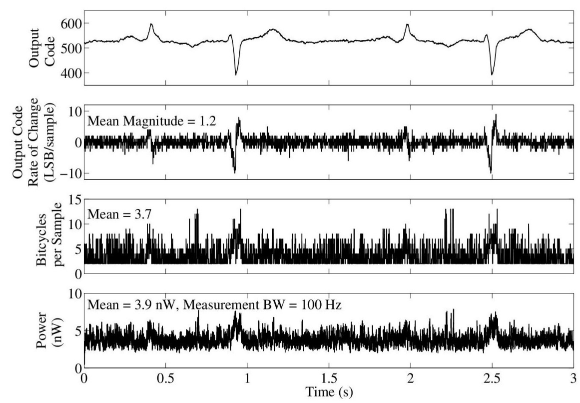
ADCs used in medical and industrial monitoring often transduce signals with short bursts of high activity followed by long idle periods. Examples include biopotential, sound, and accelerometer waveforms. Current approaches to save energy during periods of low signal activity include variable sample rate and resolution ADCs, asynchronous level-crossing ADCs, and application-specific ADCs with non-uniform quantization boundaries or dead-zones.

The motivation for this work is to create an ADC which takes advantage of low signal activity to save power, which can help extend the lifetimes of the medical implants or wireless sensor nodes that they are used in. Since low signal activity is common to many sensor signals, the ADC can save power in a broad range of applications. This work leverages the energy-efficient architecture of the highly-digital successive approximation register (SAR) ADC topology, and introduces an altered successive approximation (SA) algorithm called LSB-First SA, which is designed to reduce the number of bitcycles per conversion, given a good initial guess of the value of the sample. Because low activity signals are the target application, a good initial guess of the current sample is simply the result of the previous sample taken by the ADC. Since each bitcycle uses an analog comparison, a DAC transition, and many logic transitions, bitcycle reduction saves power in all parts of the SAR ADC.

A more detailed description of the algorithm may be found in the references. Figure 1 shows a photo of the 1 mm² silicon die containing the LSB-First SAR ADC. Figure 2 depicts the ADC's response to an ECG input signal and demonstrates the ADC's ability to save power and perform 10-bit conversions in just 3.7 bitcycles/sample on average when the signal varies by only 1.2 LSBs/sample on average.



▲ Figure 1: LSB-first SAR ADC chip micrograph showing twin capacitive DACs, comparator, sampling switches, and LSB-First bitcycling logic.



▲ Figure 2: ADC response to ECG test input signal with f_S = 1 kHz and V_{DD} = 0.5 V, demonstrating the ADC's low leakage and data-dependent energy consumption.

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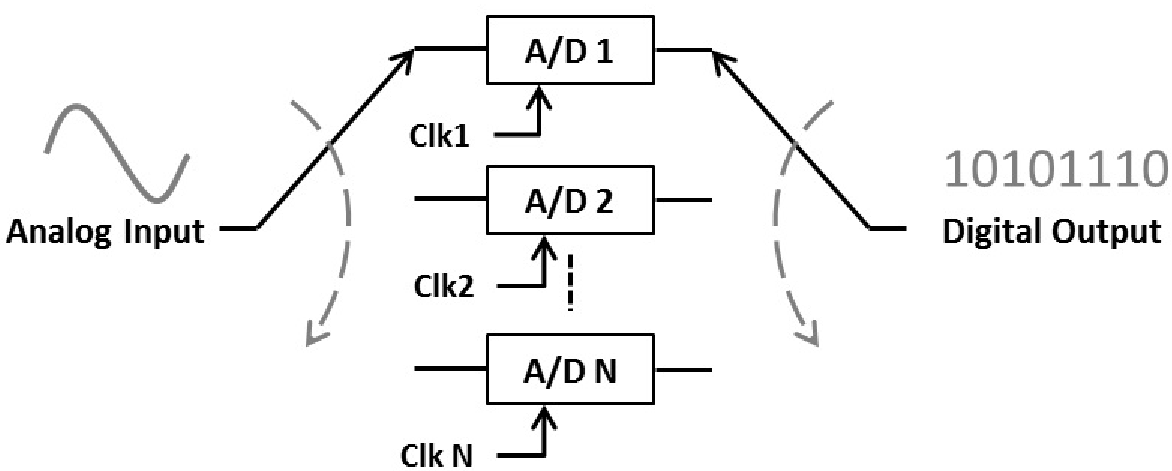
Time-interleaved A/D Converters

D.P. Kumar, H.-S. Lee
Sponsorship: Masdar Institute of Science and Technology

The demand for high-resolution and high-accuracy A/D converters in communication systems continues to increase. To raise the sampling rates to the GHz range in a power-efficient manner, time-interleaving is an essential technique whereby N A/D channels, each operating at a sampling frequency, f_s, are used to achieve an effective conversion speed of Nf_s, as illustrated in Figure 1.

While time-interleaving enables higher conversion rates in a given technology, mismatch issues such as gain, offset, and sampling clock skew errors between channels degrade the overall A/D performance. Of these issues, sampling clock skew between channels is the biggest problem in high-speed and high-resolution, time-interleaved A/D as errors due to sampling clock skew become more severe for higher input frequencies. A few sources of sampling clock skew between channels exist. Mismatches in the sampling clock path and logic delays are the most obvious. Input signal routing mismatch and RC mismatch of the input sampling circuits also cause sampling clock skew. Previous calibration techniques employ either analog and digital timing adjustment or digital calibration of output data. The timing adjustment requires an adjustable delay resulting in increased sampling jitter, which cannot be compensated by calibration. The digital calibration of output data requires complex interpolation.

In this research, we are developing a simpler calibration algorithm for sampling clock skew correction whereby the input signal is delayed by controlling the resistance of the input sampling network. The variable time-constant of the input sampling network will result in a linear delay of the input signal if the RC time constant of the input sampling network is much greater than $1/f_{in,max}$, where $f_{in,max}$ is the maximum input signal frequency. This sampling method allows for finely tuned timing-skew corrections, and the impact on noise or power consumption of the system is negligible. A 12-bit, 240MS/s, 4-way time-interleaved A/D is being taped-out to demonstrate the new calibration scheme.



▲ Figure 1: Block diagram of a time-interleaved (TI) A/D converter.

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High-precision Zero-Crossing/Op-amp Hybrid ADC

M. Markova, H.-S. Lee
Sponsorship: Center for Integrated Circuits and Systems

Technology scaling poses challenges in designing analog circuits because of the decrease in intrinsic gain and reduced swing. An alternative to using high-gain amplifiers in the implementation of switched-capacitor circuits has been proposed that replaces the amplifier with a current source and a comparator. The technique has been generalized to zero-crossing based circuits (ZCBCs). It has been demonstrated but not limited to single-ended and differential pipelined ADCs, with an effective number of bits (ENOB) ranging from 8 bits to 11 bits at sampling rates from 10MS/s to 100MS/s.

The purpose of this project was to explore the use of the ZCBC technique for high-precision ADCs. The goal of the project is a 13-bit pipelined ADC operating at up to 100MS/s. A two-phase hybrid ZCBC operation is used to improve the power-linearity tradeoff of the A/D conversion. The first phase approximates the final output value, while the second phase allows the output to settle to its accurate value. Since the output is allowed to settle in the second phase, the currents through capacitors decay, permitting higher accuracy and power-supply rejection than in standard ZCBCs. Linearization techniques for the ramp waveforms are implemented. Linear ramp waveforms require less correction in the second phase for a given linearity, thus allowing faster operation. We explored techniques for improving linearity beyond using a cascoded current source; these techniques include output pre-sampling and bidirectional output operation. Current steering is used to minimize the overall delay contributing to the first phase error, known as overshoot error. Overshoot error reduction at the end of the first phase improves the linearity requirements of the final phase. We designed a prototype ADC in 1V, 65nm CMOS process to demonstrate the techniques introduced in this work. The prototype ADC achieved 11-bit ENOB at 21MS/s and SFDR of 81dB. The main performance limitations are lack of overshoot reduction in the third pipeline stage in the prototype ADC and mid-range errors, introduced by the bidirectional ramp linearization technique, limiting the attainable output accuracy.

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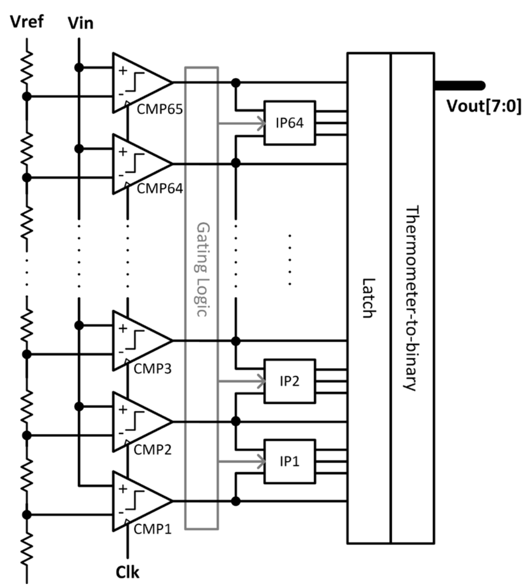
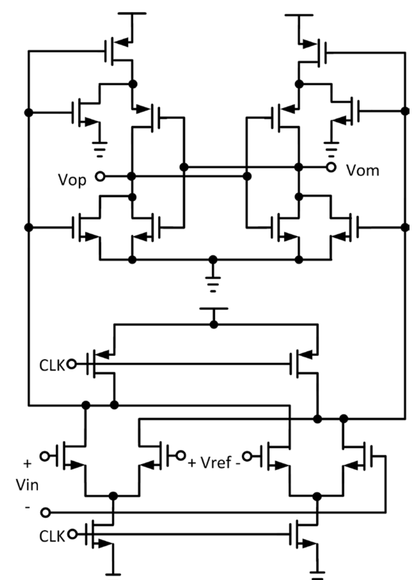
A Flash ADC with Reduced Number of Comparators

X. Yang, S. Bae, H.-S. Lee
Sponsorship: MIT/MTL GaN Energy Initiative, Office of Naval Research, Samsung

High-speed and low-resolution flash analog-to-digital converters (ADCs) are widely used in applications such as 60GHz receivers, series links, and high-density disk drive systems, as well as in quantizers in delta-sigma ADCs. In this project, we propose a flash ADC with reduced number of comparators by means of interpolation. One application for such a flash ADC is a GaN/CMOS hybrid delta-sigma converter. The GaN first stage exploits the high-voltage property of the GaN while the CMOS backend employs high-speed, low-voltage CMOS. This combination may achieve an unprecedented SNR/bandwidth combination by virtue of its high input signal range and high sampling rate. One key component of such an ADC is a flash ADC. To take advantage of the high signal-to-thermal-noise ratio of the proposed system, the quantization noise must be made as small as possible. Therefore, a high-speed, 8-bit flash ADC is proposed for this system. Figure 1 shows the block diagram of the ADC architecture. Sixty-five comparators are used to achieve the 6 most significant bits (MSBs). Sixty-four interpolators are inserted between the comparators to obtain two extra bits. The input capacitance of this design is only ¼ of the conventional 8-bit flash ADC. Therefore a higher operating speed can be achieved. We introduced gating logic so that only one interpolator is enabled during operation, which reduces power consumption significantly. A high-speed, low-power comparator with low noise and low offset requirements is a key building block in the design of a flash ADC. We chose a two-stage dynamic comparator, as in Figure 2, because of its fast operation and low power consumption. With the scaling of CMOS technology, the offset voltage of the comparator keeps increasing due to greater transistor mismatch. A popular offset cancellation technique is to digitally control the output capacitance of the comparator. However, this technique reduces the speed of the comparator because of the extra loading effect. In this project, we also propose a novel offset compensation method that eliminates the speed problem.



▲ Figure 1: Flash ADC architecture, with 65 comparators and 64 2-bit interpolaters.



▲ Figure 2: Schematic of the two-stage dynamic comparator.

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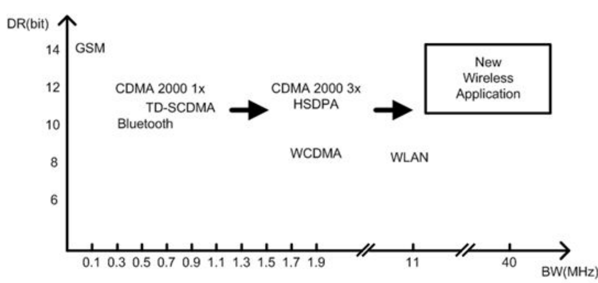
Continuous-time Delta-sigma Analog-to-digital Converters for Application to Multiple-input Multiple-output Systems

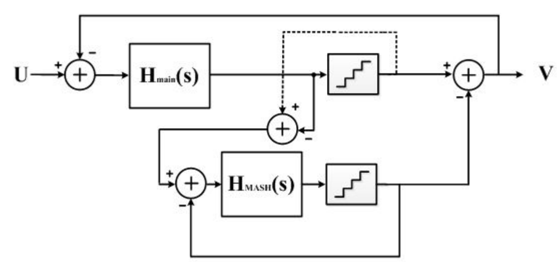
D. Yoon, H.-S. Lee
Sponsorship: MediaTek, Inc.

As wireless communication technology is rapidly advancing, new wireless applications are continuously developed. Figure 1 shows each application space and the required dynamic range. The new wireless applications demand wideband (50 MHz) and high resolution data converters (>14 bits). Delta-sigma (ΔΣ) analog-to-digital converters (ADCs) are best suited for their ability to achieve high resolution. However, the large bandwidth required poses a significant challenge. A ΔΣ ADC can be implemented in either a discrete-time (DT) or a continuous-time (CT) structure. Since DT ΔΣ ADCs require op-amp settling within each half clock period, the gain-bandwidth requirement for the op-amp is extremely high for the sampling rate required for 50MHz bandwidth. The CT ΔΣ ADCs require much lower gain-bandwidth. Thus, CT ΔΣ ADCs can function at a higher sampling frequency and achieve a wider bandwidth compared to DT ΔΣ ADCs. In addition, since the CT ΔΣ ADCs are more power-efficient and have an inherent anti-aliasing property, they are more suitable for the demanding new wireless applications.

This project focuses on the design of CT ΔΣ ADCs, specifically for the application in multiple-input multiple-output wireless receivers. For this application, each CT ΔΣ ADC in a channel must provide wide bandwidth and high dynamic range at low power consumption. The state-of-art CT ΔΣ ADCs fail to come close to either wide-enough bandwidth or high-enough dynamic range for such applications. We are investigating a new type of a CT multi-stage noise-shaping (MASH) ΔΣ ADC based on a DT sturdy-MASH ΔΣ ADC. Figure 2 shows the overall structure of a CT MASH ΔΣ ADC. The main advantage of this new type of CT ΔΣ ADCs is that it does not require digital filters that conventional MASH ΔΣ ADCs need to cancel out the quantization error of the first stage. We have developed several new techniques to make a CT MASH ΔΣ ADC faster, more accurate, and robust. The prototype ΔΣ ADC has been designed and taped out in 28nm CMOS technology.



▲ Figure 1: Dynamic range and bandwidth requirements of ADCs in wireless applications.



▲ Figure 2: Block diagram of a CT MASH ΔΣ ADC.

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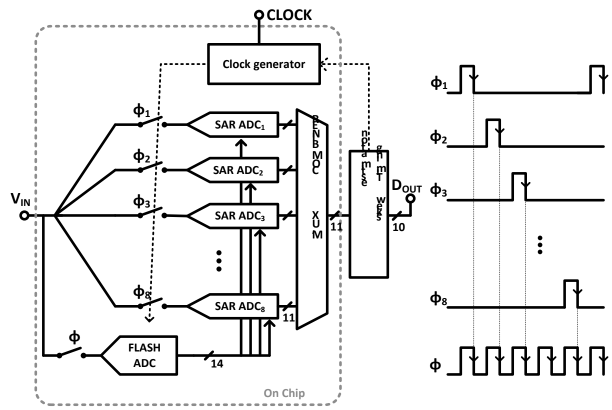
A 10-b, 1GS/s Time-interleaved SAR ADC with a Background Timing Skew Calibration

S. Lee, A.P. Chandrakasan, H.-S. Lee
Sponsorship: Center for Integrated Circuits and Systems, Samsung Fellowship

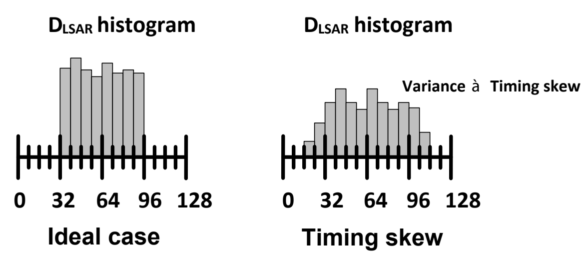
This work presents a time-interleaved (TI) SAR ADC that enables background timing skew calibration without a separate timing reference channel and enhances the conversion speed of each SAR channel. As shown in Figure 1, the proposed ADC incorporates a flash ADC operating at the full sampling rate of the TI ADC. The flash ADC output is multiplexed to resolve MSBs of the SAR channels.

Because the full-speed flash ADC does not suffer from timing skew errors, the flash ADC output is also used as a timing reference to estimate the timing skew of the TI SAR ADCs. However, this work differs from previous works in that no extra channel is required to serve as a timing-skew standard. Figure 2 shows the idea of timing-skew calibration. When the sampling signal of the flash ADC and the sampling signal of the SAR ADC are not aligned due to a timing-skew, the coarse estimation from the flash ADC is inaccurate. To recover the error of the flash ADC, the lower bits of SAR conversion output (D_{LSAR}) go beyond the normal range. Thus, the variance of the DSAR can be used as a measure of the timing-skew. This calibration puts no constraint on the input signal, and the calibration process does not interrupt the normal ADC operation. Thus, this calibration can be run in the background to track variations.

A prototype ADC is designed and fabricated in a 65-nm CMOS process. After background timing skew calibration, 51.4-dB SNDR, 59.1-dB SFDR, and ±1.0 LSB INL/DNL are achieved at 1GS/s with a Nyquist rate input signal. The power consumption is 18.9mW from a 1.0V supply, which corresponds to 62.3fJ/step FoM.



▲ Figure 1: Block diagram of the proposed TI SAR ADC.



▲ Figure 2: Examples of the DLSAR histogram without timing skew (left) and with timing skew (right).

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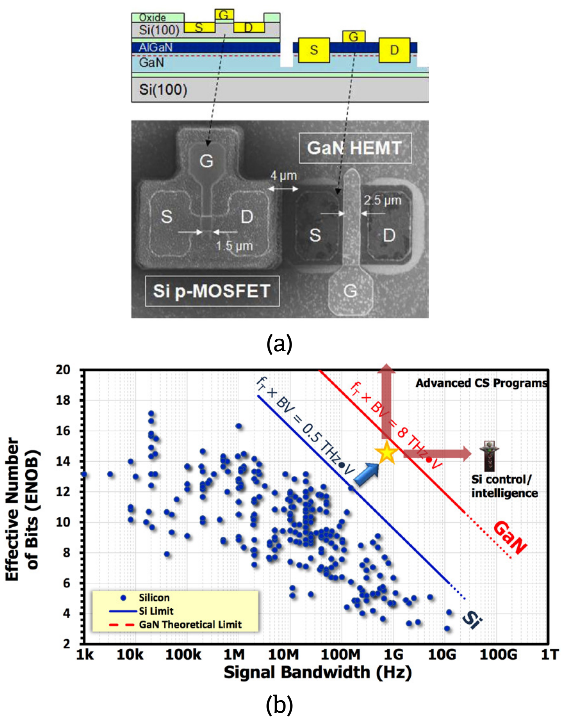
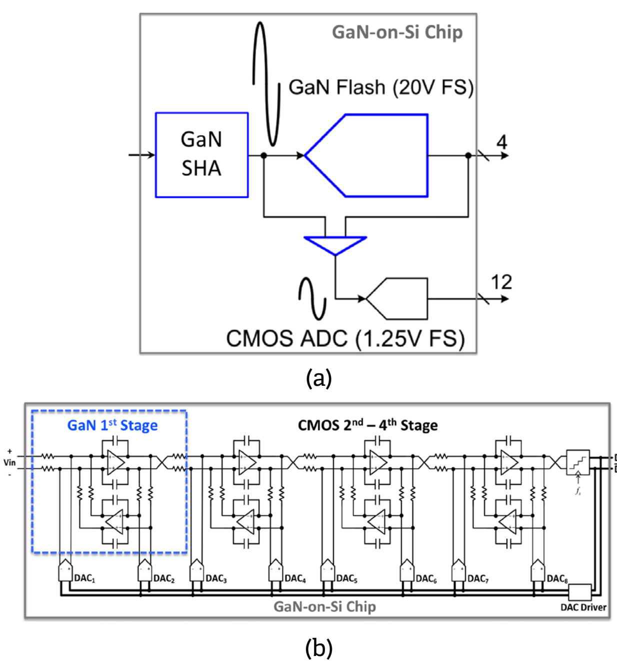
High-performance Analog-to-Digital Converter in GaN-on-Silicon Technology

S. Chung, X. Yang, H.-S. Lee
Sponsorship: MIT/MTL GaN Energy Initiative, Office of Naval Research

Mobile multimedia's coming of age with big data applications has spurred the development of extremely high-performance analog-to-digital converters (ADCs) for diverse emerging applications including personal communication, health care, and optical backbone networks. The low supply voltage of deeply scaled CMOS (complementary metal-oxide semiconductor) transistors limits the dynamic range of ADC input signal and consequently becomes a fundamental barrier to the performance of ADCs' built-in silicon technology. Recently, gallium-nitride-based high-electron mobility transistors (GaN HEMT) are reported to provide many advantages over the existing compound semiconductor technologies. The operation of GaN HEMTs at a very high supply voltage over 30V allows us to surpass the fundamental ADC SNR limit originating from thermal noise and the limited signal range of the silicon technology. Due to the high power and relatively large feature size of GaN HEMTs, a hybrid process technology, which monolithically integrates GaN HEMTs with silicon CMOS transistors on a single wafer (GaN-on-Si), will take advantage of both technologies, enabling revolutionary mixed-signal performance, as Figure 1 shows. Our research focuses on the design of unprecedentedly high-performance ADCs in a GaN-on-Si hybrid technology, as in Figure 2. First, we are developing an over-100-dB SNR GaN sampler to culminate the performance of a GaN-on-Si pipeline ADC. Second, we are investigating a wide-swing GaN operational amplifier design for a continuous-time delta-sigma ADC with a very high dynamic range.



▲ Figure 1: GaN-on-Si technology: (a) Fabricated Si MOSFET and GaN HEMT in a monolithically integrated chip. (b) Revolutionary ADC performance expected from the monolithic GaN-on-Si integration.



▲ Figure 2: High-performance ADC architecture in GaN-on-Si hybrid process technology: (a) pipeline architecture for wide bandwidth. (b) continuous-time delta-sigma architecture for high dynamic range.

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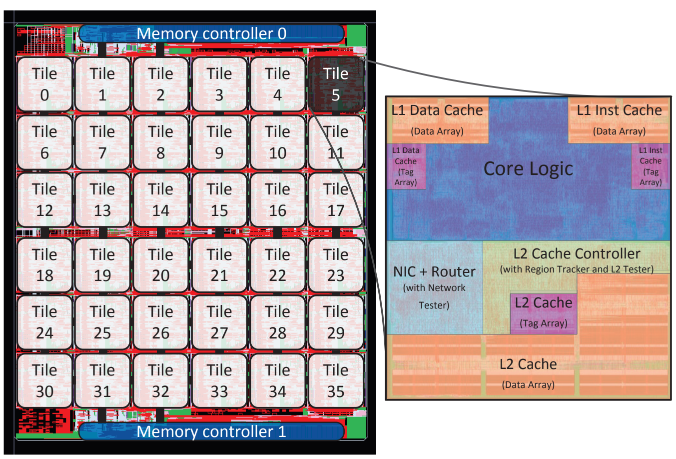
SCORPIO: A 36-core Research Chip Demonstrating Snoopy Coherence on a Scalable Mesh NoC with In-network Ordering

B.K. Daya, C.H.O. Chen, S. Subramanian, W.C. Kwon, S. Park, T. Krishna, J. Holt, A.P. Chandrakasan, L.S. Peh
Sponsorship: Center for Future Architectures (C-FAR), DARPA UHPC Grant (MIT Angstrom)

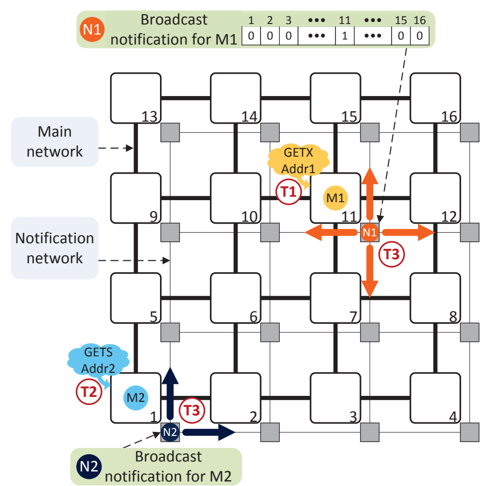
In the many-core era, scalable coherence and on-chip interconnects are crucial for shared memory processors. While snoopy coherence is common in small multicore systems, directory-based coherence is the de facto choice for scalability to many cores, as snoopy relies on ordered interconnects that do not scale. However, directory-based coherence does not scale beyond tens of cores due to excessive directory area overhead or inaccurate sharer tracking. Prior techniques supporting ordering on arbitrary unordered networks are impractical for full multicore chip designs.

SCORPIO, an ordered mesh Network-on-Chip (NoC) architecture with a separate fixed-latency, bufferless network, achieves distributed global ordering. Decoupling message delivery from ordering allows messages to arrive in any order, at any time, yet be correctly ordered. For each message sent on the main network, a notification is broadcast on the bufferless network. Within a fixed number of cycles, all nodes receive notification. Processing the received notification messages according to a consistent ordering rule means that all nodes determine locally the global order for messages in the main network. SCORPIO can plug-and-play with existing multicore IPs with priority to practicality, timing, area, and power. Full-system 36- and 64-core simulations on SPLASH-2 and PARSEC benchmarks show average application runtime reductions of 24.1% and 12.9%, vs. distributed directory and AMD HyperTransport coherence protocols, respectively.

Figure 1 shows SCORPIO in an 11 x 13 mm chip prototype, fabricated in IBM 45-nm SOI technology, comprising 36 Freescale e200 Power Architecture™ cores with private L1 and L2 caches interfacing with the NoC via ARM AMBA, plus two Cadence on-chip DDR2 controllers. The prototype achieves 1 GHz post-synthesis operating frequency (833MHz post-layout), estimated power of 28.8W (768mW per tile) with network consuming 10% of tile area and 19 % of its power.



▲ Figure 1: The 36-core fabricated multicore processor layout with SCORPIO NoC. Each tile contains in-order core, split L1 I/D caches, private L2 cache, L2 region tracker for destination filtering, and SCORPIO NoC components. The core assumes a bus is connected to AMBA AHB data and instruction ports, cleanly isolating it from details of the network and coherence support.



▲ Figure 2: At T1 and T2, cache controllers inject cache miss messages M1 and M2 at cores 11 and 1, respectively. Coherence requests are encapsulated into single flit packets and tagged with IDs of sources; IDs are broadcast to all nodes in main network. At T3, notification messages N1 and N2 corresponding to M1 and M2 are generated and sent to notification network.

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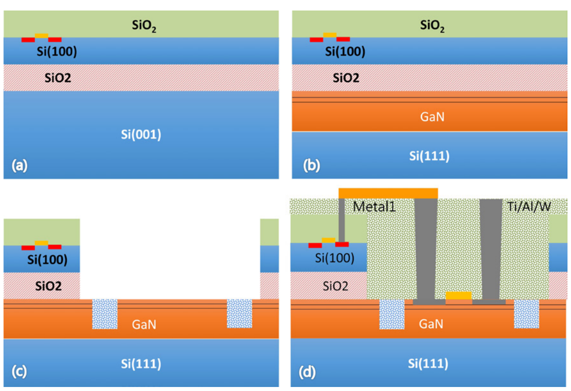
A Case for Leveraging 802.11p for Direct Phone-to-phone Communication

P. Choi, J. Gao, N. Ramanathan, M. Mao, S. Xu, C.C. Boon, S. Fahmy, L.S. Peh
Sponsorship: SMART-LEES program

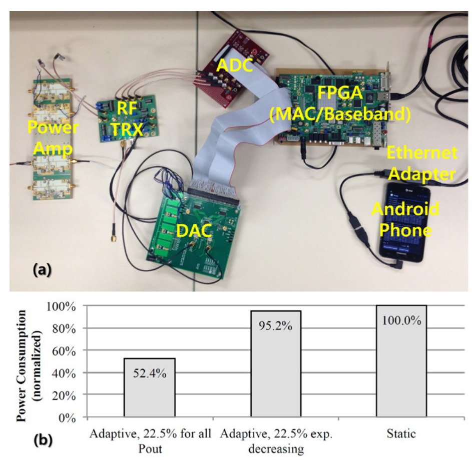
Direct device-to-device communication between phones is readily supported via standards such as ad-hoc 802.11n or WiFi Direct. However, present WiFi standards cannot effectively handle the demands of these applications, due to insufficient range and poor reliability. We make the case for using 802.11p DSRC instead, which has been adopted as a standard for vehicle-to-vehicle communications, providing lower latency and longer range.

This work is the result of collaboration among materials and device researchers, circuits designers, and mobile systems and software architects. Motivated by a novel fabrication process that deposits both III-V and CMOS devices on the same die, we leveraged the GaN HEMT devices to realize the high-power amplifier tailored for adaptive power control and coupled that with a CMOS transmitter. We designed and fabricated an 802.11p-compliant power amplifier and a transmitter on commercial 0.25-µm GaN and 0.18-µm CMOS process, respectively. This combination validates our vision for miniaturized and low-power DSRC chipsets. In our system prototype, the fabricated RF front-end is interfaced with an FPGA board implementing 802.11p digital baseband, connected to Android phones through USB. We use RoadRunner, an Android application to control road congestion, as a representative app requiring significant phone-to-phone communication.

The system consumes 0.02µJ/bit for transmission across 100 m in 64-QAM mode, assuming free space. We demonstrate that application-level power control dramatically reduces power consumption by 47% for our RoadRunner application compared to a case without power control. The 1.98mm^2 die size demonstrates the feasibility of integrating a RF front-end onto smartphones. Our results show that the GaN-CMOS process can realize a 802.11p front-end within the stringent power and area budget of a mobile phone.



▲ Figure 1: Process integration of GaN and CMOS: (a) Fabricated Si devices; (b) Si CMOS/GaN-on-Si wafer realized by two-step bonding technology; (c) GaN window open and device isolation; (d) Monolithically integrated GaN HEMT devices with final metal interconnection of fabricated HEMTs and Si CMOS devices.



▲ Figure 2: (a) Snapshot of the system prototype; (b) Average power consumption of RoadRunner V2V token exchanges with and without adaptive power control.

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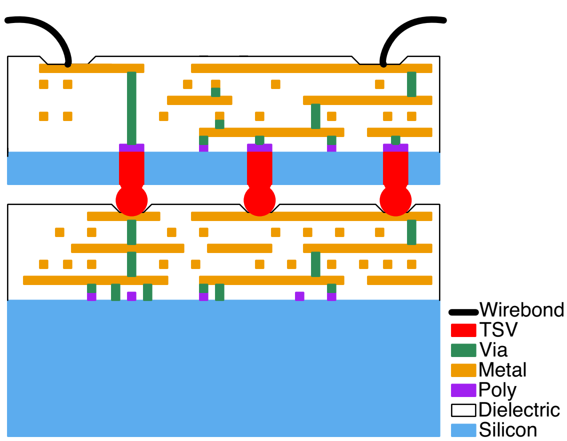
Impact of Digital Clock Tree on LC-VCO Performance in 3D-IC

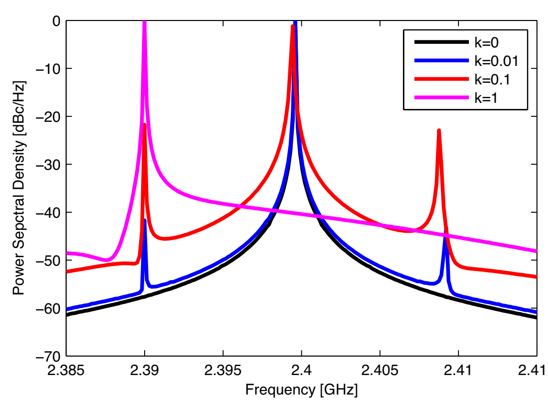
G. Yahalom, A. Wang, A.P. Chandrakasan
Sponsorship: MediaTek, Inc.

As we approach the physical limits of Moore's law and device scaling, there is increasing interest in other directions to achieve higher performance. Functional diversification, dubbed "More-than-Moore," calls us to bring together domains that have traditionally been separated. One of the suggested directions is three-dimensional integrated circuits (3D-IC), allowing the integration of several dies vertically stacked together and connected via through silicon vias (TSV) as shown in Figure 1. This opens up new possibilities for higher levels of integration to create more versatile and robust Systems-in-Package (SiP). Research is currently being done on integration of such elements as logic, memory, RF, power and sensors, showing the potential to reduce area, power, and cost and to increase data bandwidth. These savings can be achieved by the advent of a shorter interconnect with smaller parasitics and new topologies to utilize the three-dimensional structure. To enable these new technologies, we must overcome challenges caused by mechanical and thermal stress as well as power and signal integrity, requiring solutions at the circuit and system levels.

In this work we explore the impact of closely combining a sensitive analog circuit—an LC voltage controlled oscillator (VCO) on one tier with a noisy digital clock tree on the other tier. Such a scheme would likely exist in any communication system consisting of the analog front-end leading to a digital processing back-end. We propose a method to obtain insight into the key parameters that affect coupling between clock lines and the VCO inductor structure. The analysis demonstrates the relation between the structure geometries and relative positions using partial inductance matrices. This analysis enables the design of topologies with minimal coupling. We also demonstrate the impact of such noise coupling on the performance of the VCO as manifested in its output spectrum and its phase noise. A simulation of the output power spectrum of a VCO is shown in Figure 2 for several coupling coefficients. As can be seen, the spurs increase by ~20 dB per decade of increased coupling. If the coupling is close and strong enough, we observe a pulling of the VCO frequency as a result of injection-locking. The techniques proposed to mitigate these effects will allow future development of more complex, highly integrated, front-end systems that bring together RF capability with digital signal processing.



▲ Figure 1: Schematic of Back-to-Face 3D-IC stack structure (not to scale).



▲ Figure 2: Simulation of an LC-VCO output power spectral density affected by various coupling levels from independent digital clock tree.

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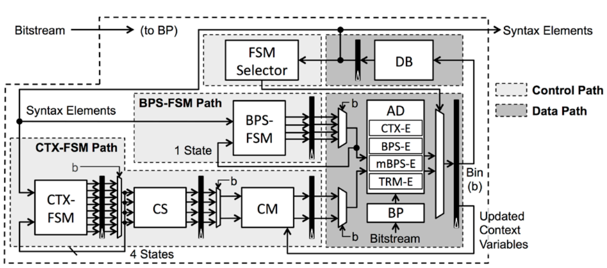
A High-throughput CABAC Decoder Architecture for the Latest Video Coding Standard HEVC with Support of High-level Parallel Processing Tools

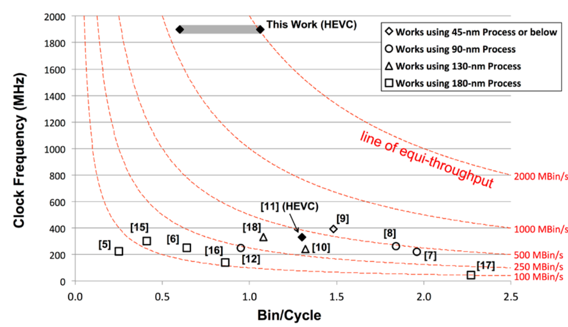
Y.-H. Chen, V. Sze
Sponsorship: MIT

High Efficiency Video Coding (HEVC), developed by the Joint Collaborative Team on Video Coding (JCT-VC) as the latest video compression standard, was approved as an ITU-T/ISO standard in early 2013. Compared to its predecessor, the H.264/AVC standard, HEVC is designed to achieve 2× higher coding efficiency for resolutions up to 4320p (8K Ultra-HD) at 120 fps to support the next decade of video applications. This results in the high-throughput requirements for the context adaptive binary arithmetic coding (CABAC) entropy decoder, which was already a well-known bottleneck in H.264/AVC. To address the throughput challenges, several modifications were made to CABAC during the standardization of HEVC. This work leverages these improvements in the design of a high-throughput HEVC CABAC decoder. It also supports the high-level parallel processing tools introduced by HEVC, including tile and wavefront parallel processing.

The proposed design, as shown in Figure 1, uses a deeply pipelined architecture to achieve a high clock rate. Additional techniques such as the state prefetch logic, latched-based context memory, and separate finite state machines are applied to minimize stall cycles, while multi-bypass-bin decoding is used to further increase the throughput. The design is synthesized in an IBM 45-nm SOI process. At the operating frequency of 1.9 GHz, it achieves throughputs up to 2014 and 2748 Mbin/s under common and theoretical worst-case test conditions, respectively. Figure 2 compares the performances of this design and previous works, including designs for both HEVC and H.264/AVC. The throughput advantage of this work comes from both the proposed architectural techniques and the advance in technology. This design is sufficient to decode in real-time high-tier video bitstreams at level 6.2 (8K Ultra-HD at 120 fps) or main-tier bitstreams at level 6.0 (8K Ultra-HD at 30 fps) for applications requiring sub-frame latency, such as video conferencing.



▲ Figure 1: Block diagram shows proposed HEVC CABAC decoder architecture. It consists of two finite state machines (CTX-FSM and BPS-FSM), FSM selector, context selector (CS), context memory (CM), bitstream parser (BP), arithmetic decoder (AD), and de-binarizer (DB). The architecture is deeply pipelined for high-throughput processing.



▲ Figure 2: Performance of the CABAC decoder is measured in bin/sec, which is the product of clock frequency and average number of decoded bins per cycle. Plot shows results under common test conditions. Compared to previous works in both HEVC and H.264/AVC standards, proposed design has clear throughput advantage.

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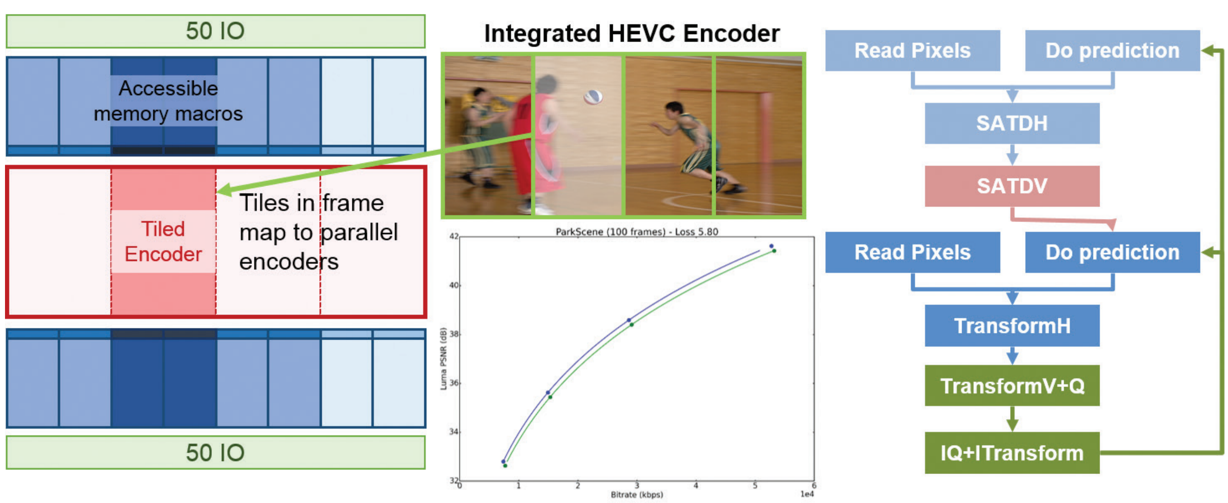
Full HD Integrated Video Encoder for H.265/HEVC

M. Tikekar, C. Juvekar, A.P. Chandrakasan
Sponsorship: Texas Instruments

High-efficiency video coding (HEVC), the latest video standard, uses larger and variable-sized coding units and longer interpolation filters than H.264/AVC to better exploit redundancy in video signals. These algorithmic techniques enable a 50% decrease in bitrate at the cost of increased computational complexity and external memory bandwidth. The added complexity makes building a real-time ASIC encoder a challenging problem. Our work attacks this problem by leveraging new modes of parallelism in HEVC using novel algorithms that are co-designed with the hardware architecture in mind. We target security camera applications where low cost integrated encoders could provide high quality video and still image archival.

Our previous work with HEVC decoders showed that the motion-compensation external memory power is a significant component of the total system's power budget. Since the motion estimation bandwidth for an encoder is typically much greater, we use an on-chip frame buffer to save power. Use of on-chip memory allows for up to 10x bandwidth with 1/10th the power. The disadvantage is the much lower densities. We use the above features of on-chip storage through a 1-frame tiled motion estimator. Tiling is a frame-level parallelism tool introduced in HEVC that allows us to split the frame into rectangular tiles and then encode them independently. Tiles allow us to perform parallel motion estimation on different parts of the frame, making optimum use of the on-chip frame storage.

Intra estimation in HEVC is an equally challenging problem. Coding gain for intra estimation is typically much harder to realize without performing a very computationally intensive optimization. We tackle this problem by developing a new gradient-based intra algorithm that offers 6% coding loss and a 2.5x runtime improvement. We obtain a 2.5% coding gain, preserving the reconstructed pixel feedback in intra estimation by multi-threading across tiles.



▲ Figure 1: Tile architecture for HEVC encoder with 16 on-chip macros to store decoded picture buffer with support of 4 parallel motion estimation engines. Highlighted macros are accessible from current estimation engine.

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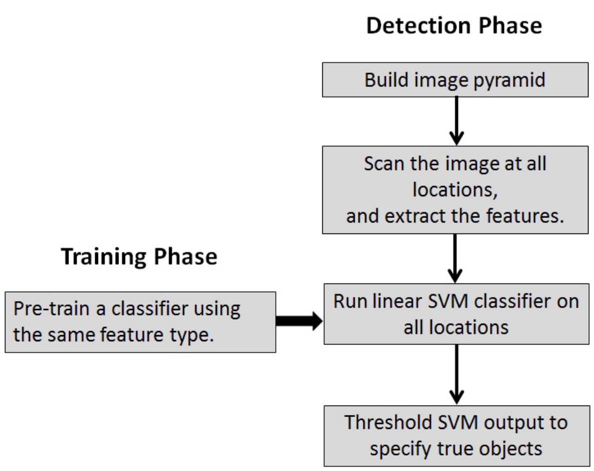
Energy-efficient Hardware for Object Detection

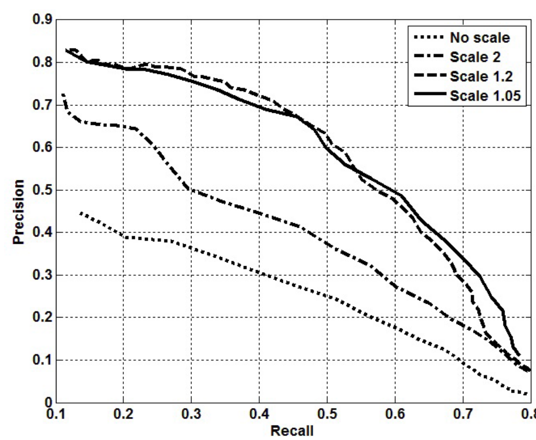
A. Suleiman, V. Sze

Object detection is needed in many embedded vision applications including surveillance, advanced driver assistance systems (ADAS), portable electronics, and robotics. Requirements for these applications include real-time operation, high-resolution image processing, and energy-efficiency, along with accuracy and robustness. For instance, real-time operation with low latency is necessary for applications such as ADAS and autonomous control in unmanned aircraft vehicles (UAV) to enable faster detection and allow more time for course corrections. High throughput (high frame rate) is also essential for fast reactions to quick changes in the environment. On the other hand, high-resolution images enable early detection by having enough pixels to identify objects at a distance. Finally, in both navigation and portable devices, energy-efficient object detection is desirable because of the limited energy available in the battery.

This project aims to develop an efficient implementation of the Histogram of Oriented Gradients (HOG) -based object detection that addresses the throughput and energy requirements, without much degradation in detection accuracy and robustness. This implementation can be achieved through both architectural and algorithmic optimizations. Hardware for object detection faces many challenges, from both complexity and memory points of view. In HOG-based object detection, HOG features are extracted for the entire frame, which is challenging for high-resolution images (e.g., 1080p) under low power constraints. The detection is done using a linear support vector machine (SVM) classifier, which includes a vector dot product requiring large number of multiplications per feature. Another important aspect of object detection is the multi-scale processing, where detection is done on multiple resolutions per frame to detect variably sized objects. This significantly increases the number of pixels being processed per frame, adding complexity to the design. One of the main challenges is to efficiently handle the large amount of computations on pixels and features while adhering to the low area and power requirements of embedded applications.



▲ Figure 1: Flow chart showing the basic steps in object detection algorithms.



▲ Figure 2: Precision-Recall curves for pedestrian detection with HOG using different scaling factors. A scale factor of 1.05 (used in original HOG paper) gives high precision, while not using scales significantly degrades the detection accuracy.

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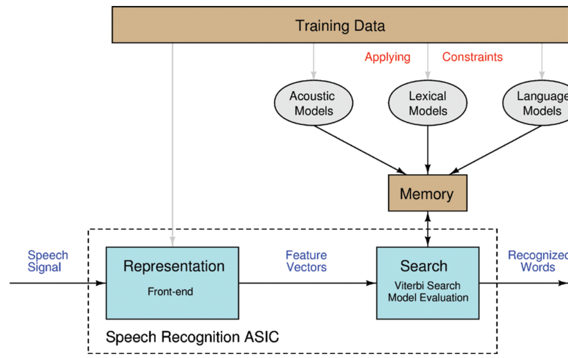
Algorithm and Architecture Enhancements for Hardware Speech Recognition

M. Price, J. Glass, A.P. Chandrakasan
Sponsorship: Quanta Computer, Inc. (Qmulus Project)

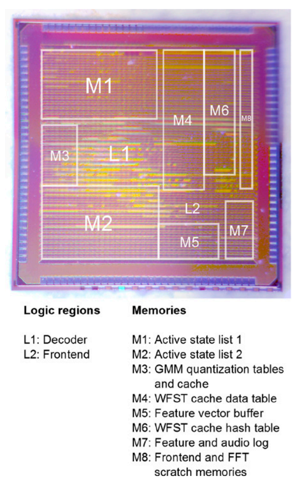
We are developing digital circuits to perform speech recognition within low-power embedded systems. The simplicity, energy efficiency, and scalability of these systems will allow them to substitute for cloud-based speech recognition services in scenarios where Internet connectivity is slow, unreliable, or energetically expensive. The circuits need to recognize speech with a controllable loss of accuracy relative to state-of-the-art software at the desired level of system power consumption.

We have designed an end-to-end (audio in, text out) speech recognition chip that is programmable with industry-standard WFST and GMM models. The chip includes a front-end that transforms audio into the feature representation used by the models and a Viterbi search module that formulates hypotheses based on these features. The weighted finite-state transducer (WFST) is a graph structure providing information about transitions between hidden states in the hidden Markov model (HMM) framework. A Gaussian mixture model (GMM) approximates acoustic observation probabilities.

Evaluating these models takes the bulk of computation and I/O for the chip and is hence the primary target for algorithm and architecture enhancements. GMM memory bandwidth is reduced by a factor of 55 through a combination of caching and parameter compression via Lloyd-Max quantization. A specialized cache for WFST parameters makes memory access more sequential, reducing page access penalties by a factor of 3. A feedback scheme is used to adjust the search pruning threshold dynamically, preventing overflow of limited on-chip memory while accommodating natural variations in search complexity. These techniques were implemented in a 65-nm test chip, which performs real-time speech decoding with a 5,000 word vocabulary. A word error rate of 13.0% is obtained at 50 MHz, with 0.85 V supplies and 6-mW core power consumption.



▲ Figure 1: Architecture of speech recognition system with hardware-accelerated decoder.



Specification	Value
Process	TSMC 65 nm
Die size	2.5 x 2.5 mm
Package	128-pin LQFP
Logic gates	340k (NAND2 equiv.)
SRAM	2.4 Mb
Supply voltage	0.8 – 1.2 V
Power consumption	5 – 23 mW (core)
Clock frequency	40 – 110 MHz
# WFST states	2.9M
# GMMs	4k x 32 Gaussians

▲ Figure 2: Die photo and summarized specifications of speech recognition chip.

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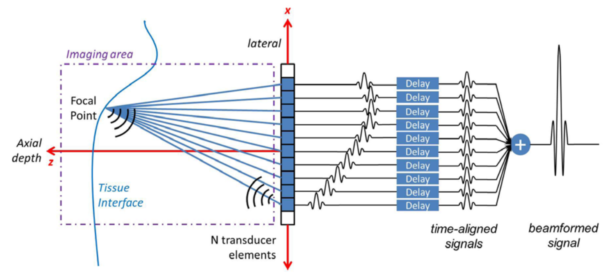
Demonstration Platform for Energy-scalable Ultrasound Beamforming

B. Lam, A.P. Chandrakasan
Sponsorship: SRC/FCRP C2S2, Texas Instruments

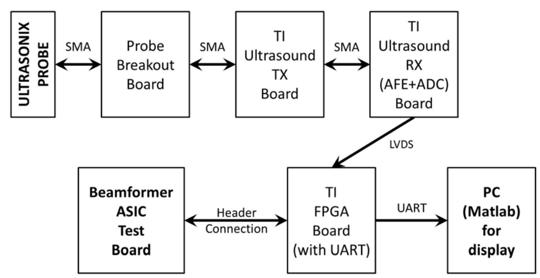
Conventional ultrasound systems employ large arrays of transducer elements to transmit and receive ultrasound waves for image formation. Given the large number of parallel channels, the cables connecting the ultrasound probe to the front-end electronics and back-end processing are necessarily bulky and expensive. With the number of channels supported only to increase (especially with the move to three-dimensional imaging, which requires the use of two-dimensional transducer arrays), miniaturizing the supporting electronics and minimizing the associated power consumption become important next steps in developing next-generation ultrasound imaging systems.

To address this need, previous work in MTL has shown low-power ASIC solutions for analog front-end (AFE) and analog-to-digital converter (ADC) electronics. We designed and fabricated a digital beamforming ASIC using TSMC 65-nm process to demonstrate energy-scalable operation in the digital domain. These three components can potentially comprise a small form factor, low-power, end-to-end solution for two-dimensional beamforming. The beamforming ASIC iteratively processes data from groups of eight transducer channels to form ultrasound images with varying image quality; we analyze the tradeoffs of this scalability .

The system demonstration uses several commercial components in conjunction with the beamforming ASIC to achieve energy scalable two-dimensional imaging. A 128-channel linear transducer probe provided by Ultrasonix Ltd. provides both the transmit and receive paths for analog signals, with the output echo waveforms being iteratively supplied to an eight-channel Texas Instruments AFE and ADC chip. The LVDS (digitized) output of this ASIC is then provided as input to the digital beamforming ASIC, the output of which is sent to a PC via UART for display. Three user-controlled modes of operation allow for a scaling of energy consumption against performance in terms of image quality, with the lower-quality images being used for large feature identification and the high-quality image used for detailed diagnosis.



▲ Figure 1: Graphical representation of beamforming operation.



▲ Figure 2: Block diagram of system demonstration components.

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Self-powered Long-range Wireless Microsensors for Industrial Applications

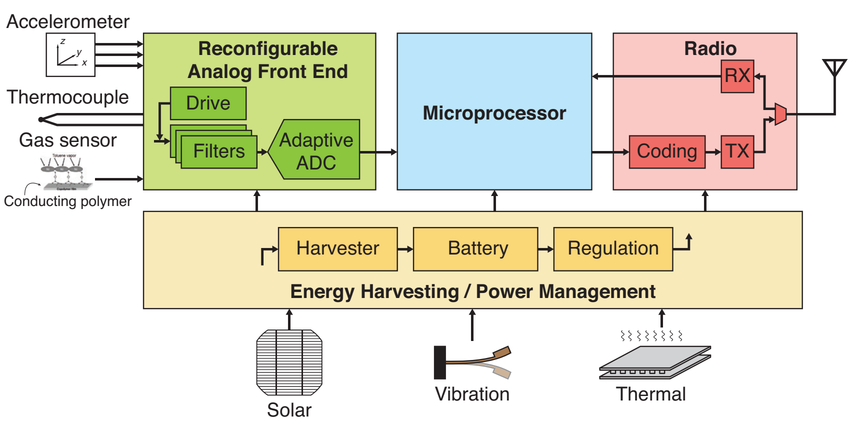
N. Ickes, H. Goktas, P. Iannucci, A. Paidimarri, X. Wang, F. Yaul, H. Balakrishnan, K.K. Gleason, A.P. Chandrakasan
Sponsorship: Shell, Texas Instruments, National Science Foundation

Improved monitoring of industrial equipment through the use of vast networks of small, easily installed, long-lasting, reliable wireless sensor nodes has the potential to increase worker safety, decrease down time, and even minimize unnecessary preventative maintenance. While critical systems are already likely to be highly instrumented and monitored, a large, modern industrial installation (such as an oil refinery, for example) may contain thousands of pumps, fans, motors, and other ancillary equipment that is monitored only through periodic, manual inspections. We are developing wireless microsensors to improve and automate the monitoring of this balance-of-plant equipment.

Figure 1 shows a block diagram of the planned sensor nodes. A reconfigurable analog front end will interface to the sensors themselves. Mechanical failures often develop slowly and can be detected early from abnormal vibrations and temperatures or minor gas leaks. Therefore, while the front end will be adaptable to a variety of sensor types, we will primarily focus on accelerometers and thermocouples, as well as a new conductive polymer sensor for organic vapors, which is also being developed for this project.

Designing an efficient radio and network protocol is another key effort of this project. The target applications will require long-range (at least 100m) communication between the sensor nodes and the base station and high densities (up to 10,000 nodes per base station). We are investigating ways to improve existing protocols by reducing synchronization requirements and incorporating new coding techniques (such as spinal codes), to shift more of the power consumption to the base station, where energy is less constrained.

Once deployed, the sensors must function for up to twenty years without maintenance, so each node will be entirely powered by energy scavenged from its environment. Solar power is an attractive source for sensors deployed outdoors, but we are also investigating vibration and thermal harvesting, as these energy sources are readily available in many industrial applications and would allow sensors to be deployed in much less accessible locations.



◀ Figure 1: Block diagram of the planned sensor node. Optimized, energy-efficient sensor front end and radio components will allow the entire node to be powered from ambient energy harvested from solar, vibration, or thermal sources.

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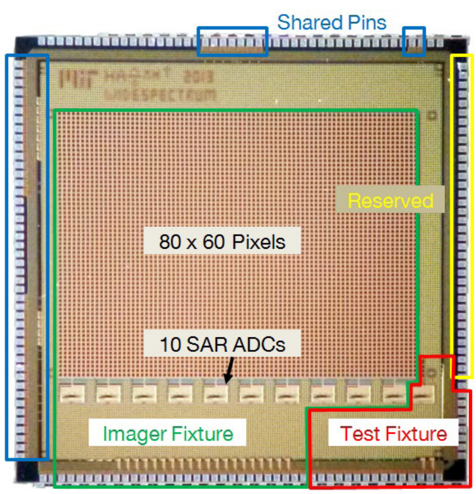
Graphene-CMOS Hybrid Infrared Image Sensor

S. Ha, A. Hsu, T. Palacios, A.P. Chandrakasan
Sponsorship: Center for Integrated Circuits and Systems, Institute for Soldier Nanotechnologies

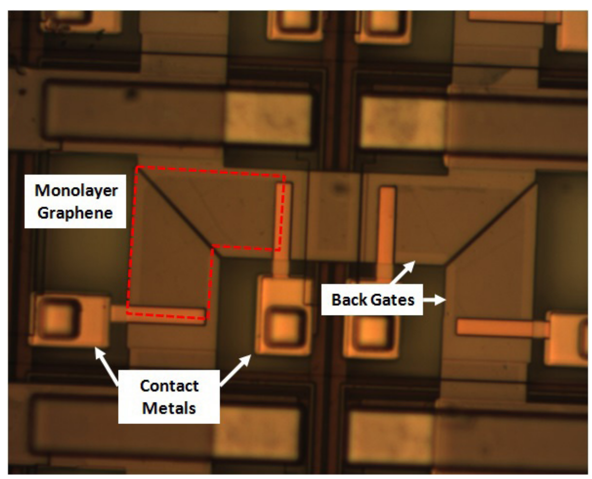
Applications in the mid- and far-infrared spectrum expand from security cameras and medical thermal imaging to spectroscopy for chemistry and astronomy. However, conventional infrared (IR) sensors require high-cost epitaxial growth of InSb or HgCdTe layer for IR absorption, and they also suffer from integration issues and a limited absorption band determined by the epitaxial growth. On the other hand, CMOS image sensors are widely used in digital multimedia applications thanks to their mature production technology, and the performance ramps up every year with denser integration, better noise suppression, adjustable dynamic range, and lower power. However, the band gap of silicon fundamentally limits the absorption spectrum to the visible and near-infrared light (λ < 1100nm).

We develop a graphene-CMOS hybrid sensing platform that solves critical issues in manufacture of conventional IR sensors and enables expanded applications such as a high-speed and high-resolution IR imager and a hyperspectral IR imaging IC. This work presents a prototype chip, with graphene thermocouples fabricated on top of the CMOS IC.

A 5mm x 5mm readout chip is fabricated as shown in Figure 1. The chip is fabricated using commercial 0.18-um technology, but the design considered post-fabrication steps for graphene IR detectors. Each pixel has two contact metal plugs towards the top surface of the chip for ohmic contact to graphene. The pixel area is 50µm x 50µm; a pixel amplifier and signal paths occupy the small portion of each pixel area, leaving over 60% of the area empty and flat. The center area of the chip, 3mm x 4mm, is filled with the 80 x 60 array of the pixels. Sides of the chip are used for the row and column selection logic, current sources, column amplifiers, and ADCs. The layout eases the post-fabrication process, including graphene transfer, by locating the regularly patterned pixel array in the center of the chip and others on the sides. Figure 2 shows the graphene thermocouple fabricated on the chip. Each end of the thermocouple connects to the metal pillar of the pixel amplifier input. An induced p-n junction of graphene generates a thermovoltaic signal in response to IR light; the readout IC amplifies and digitizes it to 8-bit code. Ten parallel ADCs can process data from 4,800 pixels at a rate of 1MB/s.



▲ Figure 1: The readout IC for graphene-CMOS hybrid IR imager is fabricated. The chip is shown before the post-fabrication of graphene thermocouples.



▲ Figure 2: Top view of the pixels with graphene thermocouples connected to the pixel amplifier inputs. The monolayer graphene sheet is biased by two metal gates embedded underneath.

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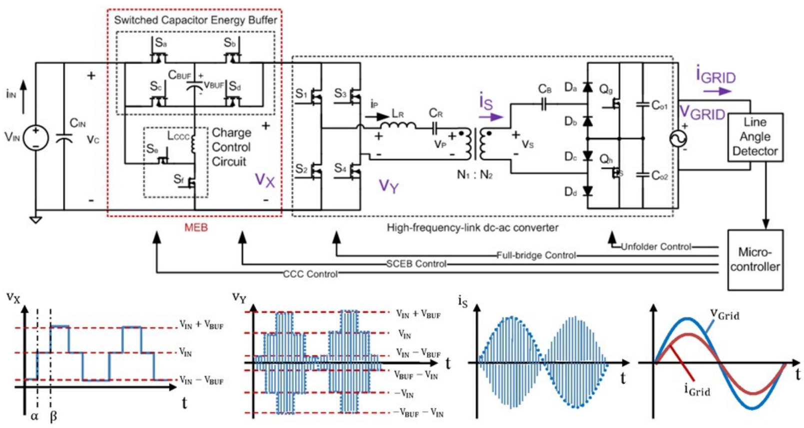
A Multilevel Energy Buffer and Voltage Modulator for Grid-interfaced Micro-inverters

M. Chen, K.K. Afridi, D.J. Perreault
Sponsorship: Enphase Energy

Micro-inverters operating in the single-phase grid from solar photovoltaic (PV) panels or other low-voltage sources must buffer the twice-line-frequency variations between the energy sourced by the PV panel and that required for the grid. Moreover, in addition to operating over wide average power ranges, they inherently operate over a wide range of voltage conversion ratios as the line voltage traverses a cycle. These factors make the design of micro-inverters challenging. This paper presents a Multilevel Energy Buffer and Voltage Modulator (MEB) that significantly reduces the range of voltage conversion ratios that the dc-ac converter portion of the microinverter must operate over by stepping its effective input voltage in pace with the line voltage. The MEB partially replaces the original bulk input capacitor and functions as an active energy buffer to reduce the total size of the twice-line-frequency energy buffering capacitance. The small additional loss of the MEB can be compensated for by the improved efficiency of the dc-ac converter stage, leading to a higher overall system efficiency. The MEB architecture can be implemented in a variety of manners, allowing different design tradeoffs to be made. A prototype micro-inverter incorporating an MEB, designed for 27 V to 38 V dc input voltage, 230 V rms ac output voltage, and rated for a line cycle average power of 70 W, has been built and tested in a grid-connected mode. We show that the MEB can successfully enhance the performance of a single-phase grid-interfaced microinverter by increasing its efficiency and reducing the total size of the twice-line-frequency energy buffering capacitance.



◀ Figure 1: One implementation of the MEB micro-inverter and its conceptual operating waveforms.

▶ Figure 2: Pictures of the prototype MEB based micro-inverter. The layout of the MEB stage (switches and capacitors) is optimized, targeting the highest power density.

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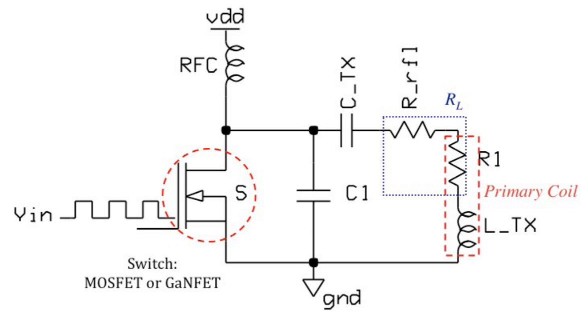
Efficient Wireless Charging with Gallium Nitride FETs

T. Yeh, N. Desai, T. Palacios, A.P. Chandrakasan
Sponsorship: MIT/MTL GaN Energy Initiative, Foxconn

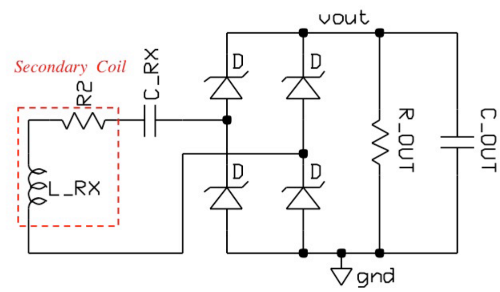
Wireless transfer of power and signals over distances has been rapidly growing. The ability to transfer energy from one device to another without cables improves both the convenience and reliability for consumers. This research focuses on near-field power transfer for ¼ inch up to 1 inch for a device people use in their daily lives: cellphones.

Though wireless charging is more convenient than traditional wired charging methods, it is currently less efficient. This method not only wastes power but also can result in a longer charging time. Reducing the sources of loss in the conversion circuits improves the efficiency of the wireless charging system. In this work, we focus on losses originating from the transistor. We designed and implemented resonant inductive wireless charging systems with different switch implementations to compare efficiencies.

One system utilizes the traditional silicon MOSFET. The other board replaces the MOSFET with a gallium nitride FET (GaNFET), while keeping the circuitry and components as consistent as possible. GaNFETs have many benefits such as lower $R_{ds,on} \times Q_{G,}$ smaller footprints, and potentially higher breakdown voltages. Results show that the GaNFET system has a 5% efficiency gain over the MOSFET system for various distances. The wireless charging systems implemented allow for flexibility in alignment between devices delivering and receiving power and efficiencies in the 30%-50% range.



▲ Figure 1: Transmitter unit. Class E power amplifier used as the DC/RF converter. RF choke provides DC current. S switch is fully either on or off. C1 is shunt capacitor to provide zero voltage turn on. CTX and LTX form the primary tank. LTX is inductance of primary coil; R1 is intrinsic resistance of primary coil.



▲ Figure 2: Secondary unit. A secondary LC tank with full bridge rectifier. LRX is inductance of secondary coil and R2 is intrinsic resistance of secondary coil. CRX adds resonance to circuit for optimal power transfer.

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Efficient Portable-to-Portable Wireless Charging

R. Jin, A.P. Chandrakasan
Sponsorship: Foxconn, TSMC University Shuttle Program

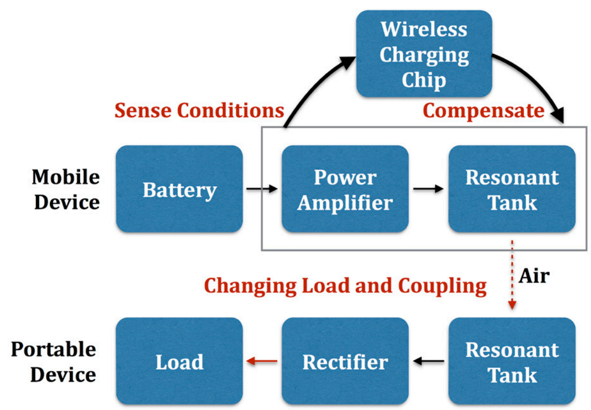
In today's world of ever-increasing low-power portable electronics, from medical implants to wireless accessories, powering these devices efficiently and conveniently is an growing concern. Currently, these devices are recharged by plugging them into individual chargers. This can be an inconvenience for users and contributes to a large amount of electronic waste. Our alternative solution is to wirelessly recharge these lower-power portable devices through a common magnetic link with a higher-power portable device, such as a smartphone. In a typical case, the user moves the smartphone close to the portable device and charges it in a few minutes for a day's use. Such a method is convenient, environmentally friendly, and cheap to implement.

This portable-to-portable wireless charging application differs from conventional charging pad-based systems in that the transmitter battery life is constrained and valuable, so efficiency is key. Also, since both the transmitter and receiver are portable devices, output load and transmitter-to-receiver coupling are constantly changing, which results in dynamic transmitter loading. These changing conditions affect transfer efficiency.

We develop a resonant inductive wireless charging system operating at 6.78 MHz that transfers energy between portable devices with high efficiency. The system includes a custom integrated circuit that senses changing load and coupling conditions while charging and actively adjusts the transmitter circuit to maintain high system efficiency and consistent power levels.

This portable-to-portable wireless charging system is applicable to many kinds of devices. Applications are demonstrated that use a smartphone to wirelessly recharge fitness trackers, cochlear implants, bicycle lights, MP3 players, wireless keyboards, and calculators, charging most devices in 2 minutes for a typical day's use.

▲ Figure 1: Our wireless charging system uses a smartphone to recharge various lower-power portable devices, such as cochlear implants, wireless keyboards, bicycle lights, fitness trackers, and calculators. The smartphone charges most devices in 2 minutes for a typical day's use.



▲ Figure 2: Changing load and coupling conditions impact the transfer efficiency of the wireless charging system. A wireless charging controller chip detects these conditions and actively adjusts the transmitter to compensate. This maintains high efficiency and consistent power levels as conditions change.

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A 28-nm FDSOI Integrated, Reconfigurable, Switched-Capacitor Step-up DC-DC Converter with 88% Peak Efficiency

A. Biswas, Y. Sinangil, A.P. Chandrakasan
Sponsorship: DARPA, STMicroelectronics

The increasing integration of analog, digital and RF circuits in modern Systems-on-Chip (SoCs) has created a demand for a wide range of unique power supplies, to cater to different functionalities. Hence, an on-chip power management unit (PMU) is essential to efficiently convert and deliver these diverse power supplies from a single source. With the progress of CMOS scaling, the nominal supply voltage (V_{dd}) of the transistors has substantially decreased. However, certain functionalities, e.g., non-volatile memory, require voltages that are higher than V_{dd}. On the other hand, applications like energy-harvesting need to boost the source voltage to generate a higher output voltage. Thus, step-up DC-DC converters are an important component in the PMU for these kinds of applications. Fully integrated switched-capacitor- (SC) based DC-DC converters can achieve high conversion efficiency and power density, which are key for on-chip implementation.

To benefit from CMOS scaling, SC converters should utilize core transistors as charge-transfer switches. Core transistors offer lower on-resistance (R_{on}) and capacitance compared to I/O transistors. However, to avoid voltage overstress, core transistors cannot be operated with a gate-to-source/drain voltage of more than V_{dd}. Furthermore, it is desirable to have reconfigurability in the SC converter. It enables the same converter to be efficiently used to generate a wide range of output voltages, rather than using separate converters for each output voltage.

In this work we implement a reconfigurable step-up SC DC-DC converter with 3 conversion ratios of 5/2, 2/1, and 3/2. This converter provides a wide range of output voltage from 1.2V to 2.4V, with a fixed input supply voltage of 1V. The step-up converter has been designed to obviate the need to use high voltage I/O transistors as charge-transfer switches. Additionally, a new topology is proposed for the 5/2 mode, and it improves conversion efficiency by reducing the bottom-plate parasitic loss as compared to a conventional series-parallel topology. The converter (Figure 1) was implemented in a 28-nm FDSOI (fully-depleted SOI) process using only on-chip MOS and MOM (metal fringe) capacitors that require no extra fabrication steps, unlike MIM (metal-insulator-metal) and trench capacitors.

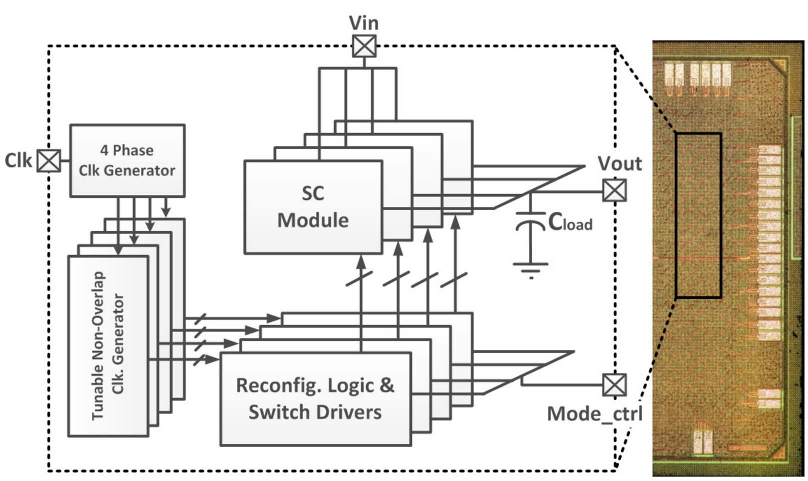

Figure 1: Overall architecture of the integrated, reconfigurable, step-up switched-capacitor DC-DC converter.

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Electronic Devices: Transistors in Si, SiGe, Ge, III-Vs, GaN, and 2D Materials

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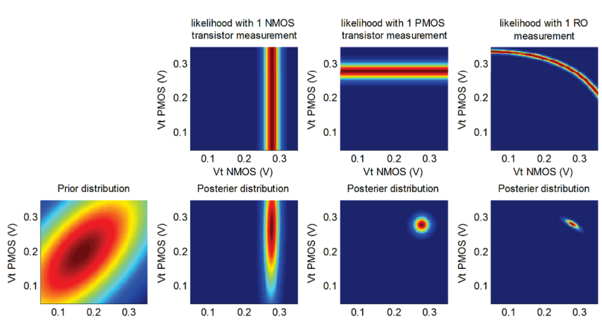
An Efficient Bayesian Framework for Accurate Parameter Extraction from Limited Measurements

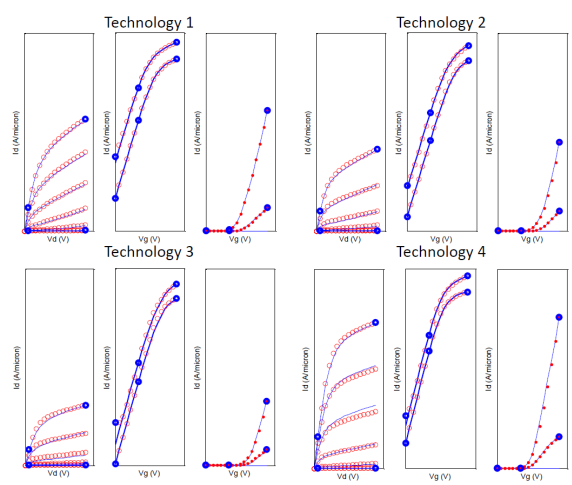
L. Yu, D.A. Antoniadis, D.S. Boning
Sponsorship: MIT/Masdar Institute of Science and Technology

The first of our two projects is to develop methods for application to post-silicon performance estimation using the MIT virtual source mode (MVS) model. We have achieved a new performance estimation algorithm through physical subspace projection and maximum *a posteriori* (MAP) estimation. Our goal is to estimate the distribution of a target circuit performance with an extra-small number of measurement samples from on-chip monitor circuits. The key idea in this work is to exploit the fact that simulation and measurement data are physically correlated under different circuit configurations and topologies. First, different populations of measurements are projected to a subspace expanded by a set of physical variables. The projection is achieved by performing a sensitivity analysis of measurement parameters on subspace variables using the virtual source compact model. Then we develop a Bayesian treatment by introducing prior distributions over these projected variables. MAP estimation is also applied using the prior, as illustrated in Figure 1. The proposed method has been validated by post-silicon measurement of a commercial 28-nm process. An average error reduction of 2x is achieved, which can be translated to a 32x-reduction of the number of data points needed for samples on the same die. A 150x and 70x sample size reduction on training dies is also achieved compared to the traditional least-square training method and least-angle regression method, respectively, without surrendering accuracy

Our second effort is a novel MOSFET parameter extraction method to enable early technology evaluation. The distinguishing feature of the proposed method is that it enables the extraction of an entire set of MOSFET model parameters using limited and incomplete IV measurements from on-chip monitor circuits, as Figure 2 shows. An important step in this method is the use of maximum-a-posteriori estimation where past measurements of transistors from various technologies are used to learn a prior distribution and its uncertainty matrix for the parameters of the target technology. The framework then utilizes Bayesian inference to facilitate extraction using a very small set of additional measurements. The proposed method is validated using various past technologies and post-silicon measurements for a commercial 28-nm process. The proposed extraction could also be used to characterize the statistical variations of MOSFETs with the significant benefit that the constraints required by the backward propagation of variance method are relaxed.



▲ Figure 1: Illustration of sequential Bayesian learning of physical subspace (threshold voltage) from prior and on-chip monitor circuits.



▲ Figure 2: MVS model fitting results in four technologies in the 14-nm to 45-nm generations. Blue circles are fitted measurements using the MAP method; red circles are test measurements for validation.

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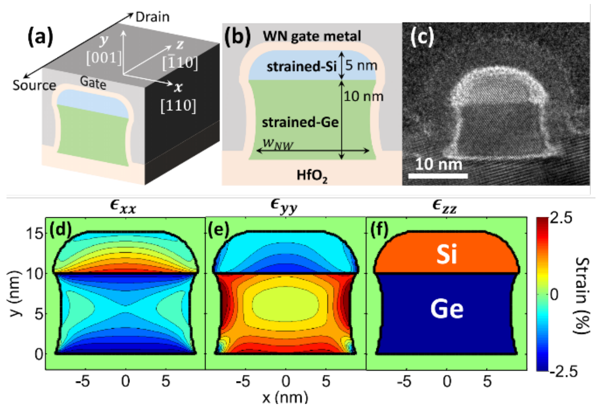
Enhanced Hole Ballistic Velocity in Germanium Nanowire p-MOSFETs Through Asymmetric Strain

J. Teherani, W. Chern, D. Antoniadis, J.L. Hoyt
Sponsorship: NSF Center for Energy Efficient Electronics Science

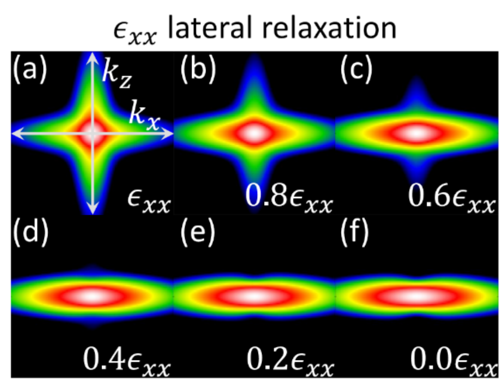
Germanium has the highest hole mobility of any bulk semiconductor, and compressive biaxial strain has been used to increase the Ge hole mobility. Recently, asymmetrically strained Ge nanowire p-MOSFETs exhibiting hole mobility enhancement over biaxially strained structures have been fabricated. This work studies the impact of asymmetric strain on hole ballistic velocity using strain-dependent band structure simulations. Enhanced ballistic velocity translates to higher current drive in nanoscale MOSFETs, which is critical for future CMOS technology.

Figure 1 shows the device structure and simulated strain profiles for the nanowire Ge p-MOSFETs fabricated by Hashemi (details in *Further Reading*). The structure is created through a bond-and-etch-back process that yields compressive biaxially strained Ge (pseudomorphic to $Si_{0.6}Ge_{0.4}$) on HfO_2 dielectric with a tensile strained Si capping layer. The layers are patterned using electron beam lithography to create nanowires. The lateral strain (ε_{xx}) is seen to relax near the sidewall of the nanowire due to the free surface; however, strain along the channel direction (ε_{zz}) remains constant because the device is long in that direction. Lateral strain relaxation increases as the width of the nanowire (w_{nw}) is decreased.

Strain affects the curvature of the valence bands, which impacts the hole effective mass, the hole ballistic velocity, and the valence band density of states. Figure 2 shows the valence band dispersion for bulk Ge with varying lateral strain relaxation. As lateral strain is decreased (from (a) to (f)), the curvature of the valence band in the transport direction (k_z) significantly sharpens, which implies a decrease in the hole effective mass and an increase in the hole ballistic velocity. Analysis of the valence band structure predicts a 2.6× hole ballistic velocity enhancement for 10-nm-wide asymmetrically strained Ge nanowires relative to unstrained Si p-MOSFETs.



▲ Figure 1: (a) 3D schematic of the nanowire structure with crystal Miller directions indicated for the different directions. The *x*, *y*, and *z* correspond to the lateral, vertical, and channel/transport directions. (b) Cross section of the trigate structure. (c) HRTEM of the experimental device. (d-f) Simulated strain profile for w_{nw}=18 nm. The (d) lateral strain ε_{xx}, (e) vertical strain ε_{yy}, and (f) strain along the channel ε_{zz} are shown.



▲ Figure 2: *E*-*k* dispersion for bulk Ge with varying lateral strain. (a) Ge biaxially strained to a $Si_{0.6}Ge_{0.4}$ substrate ($\varepsilon_{xx} = \varepsilon_{zz}$ = -2.4%, ε_{yy} =1.8%). (b-f) is reduced as indicated; ε_{yy} and ε_{zz} are fixed at 1.8 and -2.4%, respectively. The effective mass in the *z*-direction significantly reduces as $|\varepsilon_{xx}|$ is decreased.

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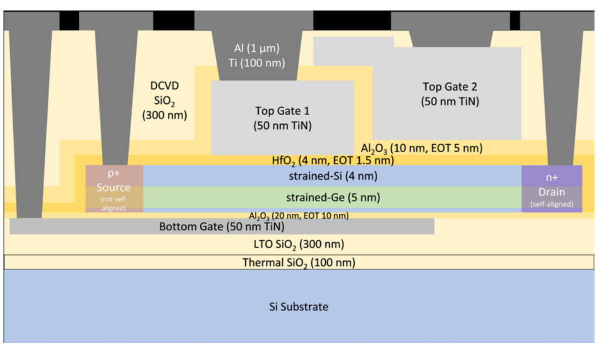
Strained-Si/strained-Ge Heterostructure Bilayer TFETs

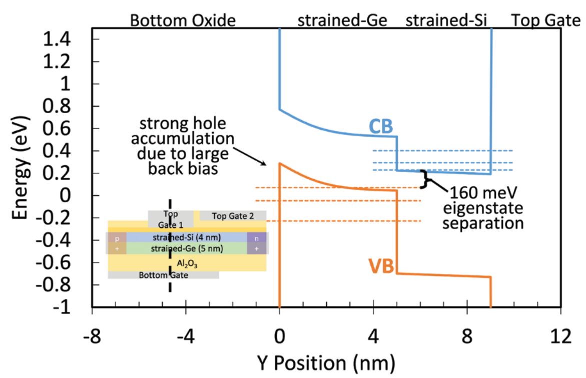
W. Chern, J.T. Teherani, D.A. Antoniadis, J.L. Hoyt
Sponsorship: NSF Center for Energy Efficient Electronics Science

Tunnel field effect transistors (TFETs) are currently being investigated because they can theoretically switch faster than the 60-mV/dec thermal limit of metal-oxide field effect transistors (MOSFETs), potentially enabling lower power electronics. The improvement of the switching steepness allows for a reduction in the operating voltage and hence in power consumption as power scales with ~ V^2. Experimentally, TFETs have been challenged by low current and/or switching at rates above the thermal limit inferior to theoretical predictions. This work explores a structure with multiple independent gates to experimentally investigate electrostatics for TFETs using a strained-Si/strained-Ge heterostructure. This structure has the benefit of an undoped, fully-depleted, thin-body channel for low body capacitance (i.e., improved electrostatic control) and high-κ on Si for low interface trap density required for ideal switching.

We are currently fabricating the bilayer TFET design shown in Figure 1. In this structure, a top and bottom gate overlap to form the tunneling region. The bottom gate serves to electrostatically p-type dope the strained-Ge and provide a conduction path from the source to the channel. Top Gate 1 is used to align the conduction band of the Si to the valence band of the Ge, as shown in Figure 2, to allow tunneling between the two layers, thus turning the device on. The presence of electrons in the Si near the top gate and holes in the Ge near the bottom gate gives this device its name: the bilayer TFET. The second top gate is used to modulate the Fermi level between the gate and drain to cut off potential leakage paths and also allow conduction from the channel to the drain. The device will be used as an experimental testbed to probe the impact of electrostatics and to shed light on design parameters for optimal TFET performance.



▲ Figure 1: Cross-sectional view of final strained-Si/strained-Ge heterostructure bilayer TFET with three independent gates.



▲ Figure 2: Band diagram of strained-Si/strained-Ge heterostructure TFET in the on-state (inset shows band diagram cut taken through the channel). The strained-Ge is under strong hole accumulation when this device is initially turned on.

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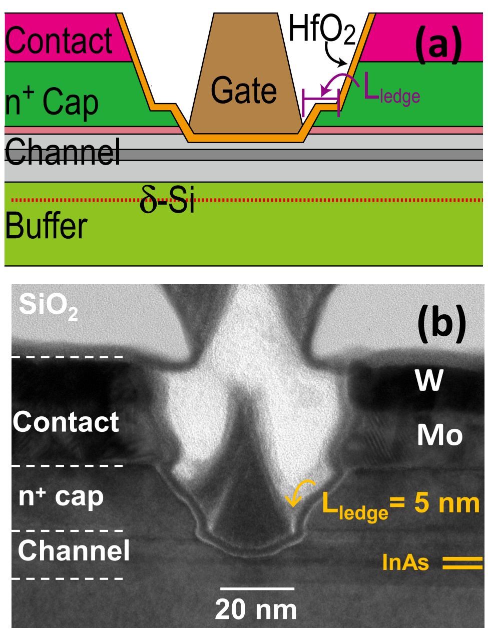
A Self-aligned InGaAs Quantum-well MOSFET Fabricated by a Scalable Tight-pitch Process

J. Lin, D.A. Antoniadis, J.A. del Alamo
Sponsorship: SRC/FCRP MSD, NSF Center for Energy Efficient Electronics Science, Singapore-MIT Alliance, SMART program

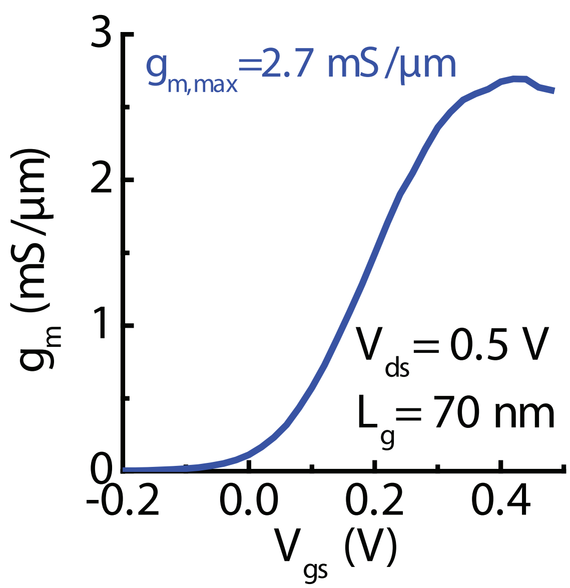
InAs and InGaAs are promising channel material candidates for CMOS applications due to their superior electron transport properties. While great progress has taken place recently in demonstrating III-V MOSFETs, transistors displaying well-balanced electron transport, electrostatic integrity and parasitic resistance together with potential for high device density and tight pitch have yet to be demonstrated. This work demonstrates a novel InGaAS Quantum-well MOSFET (QW-MOSFET) that addresses all these challenges.

The design of the tight-pitch QW-MOSFET is shown in Figure 1 (a). The intrinsic region of the device contains an 8-nm-thick composite channel with an InAs core (2 nm) and two $In_{0.7}Ga_{0.3}As$ cladding layers. The gate insulator is HfO_2 with a thickness of 2.5 nm. To minimize source and drain resistance, this device architecture incorporates a thin, highly conducting "ledge" spanning the access region of the device. The cross sectional transmission electron micrograph (TEM) in Figure 1 (b) shows a finished device with a gate length L_g= 20 nm and very close metal contact spacing. The ledge length is about 5 nm. In the fabrication process, we closely follow CMOS-compatible requirements with the front-end process being *lift-off free*, *Au-free* and *wet-etch free*.

The QW-MOSFETs that we have fabricated exhibit excellent performance. Figure 2 shows transconductance (g_m-V_{gs}) characteristics of an L_g= 70 nm device. A peak g_m of 2.7 mS/mm is obtained at a V_{ds}=0.5 V. This is the highest g_m demonstrated in a III-V MOSFET to date. Using this fabrication process, we have also demonstrate devices with longer ledge length (L_{ledge} = 70 nm). Such a device exhibits well-balanced electrostatics and drive current. This research sheds light on the design and potential of InGaAs transistors for future VLSI applications.



▲ Figure 1: (a) Cross sectional schematic of InGaAs QW-MOSFETs with self-aligned metal contacts. (b) TEM image of a fabricated device with gate length of 20 nm.



▲ Figure 2: Transconductance characteristics of L_g=70 nm MOSFET at V_{ds}=0.5 V. This transconductance is the highest demonstrated in any III-V MOSFET to date.

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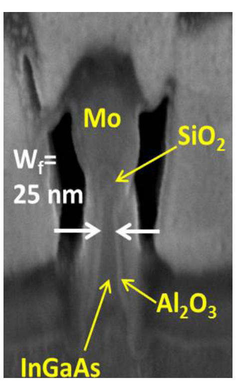
Double-gate InGaAs MOSFET for Fin-sidewall Characterization

A. Vardi, X. Zhao, J.A. del Alamo
Sponsorship: Sematech, Technion-MIT Fellowship, NSF Center for Energy Efficient Electronics Science

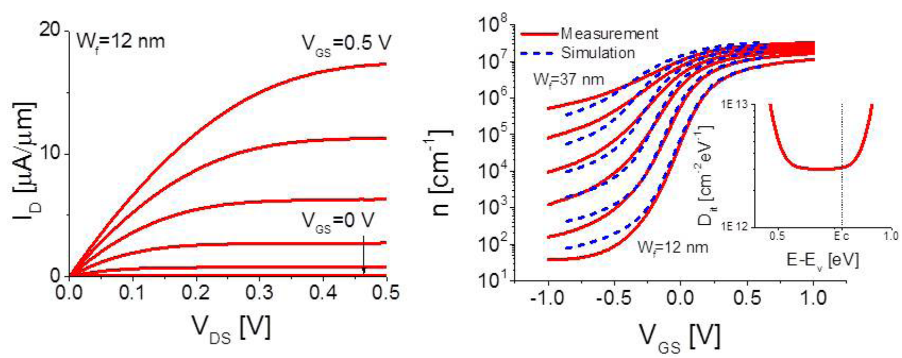
InGaAs has emerged as the most promising n-channel material for sub-10-nm CMOS because of its exceptional electron transport properties. In the sub-10-nm dimensional range, only high aspect-ratio three-dimensional (3D) transistors with a fin or nanowire configuration can deliver the necessary performance and meet the short-channel effects goals. This requirement brings to the fore the need to achieve high quality metal-oxide-semiconductor (MOS) interfaces on the sidewalls of these devices, a topic about which little is known. In this work we fabricate double-gate fin MOSFETs and characterize the sidewall MOS interface of dry-etched InGaAs fins through their subthreshold behavior.

Figure 1 shows a scanning electron microscope (SEM) cross-section of a device. In essence, this is an n-type doped-channel FinFET where the gate acts only on the sidewall surface potential. The starting material consists of an n- type $In_{0.53}Ga_{0.47}As$ active layer on a semi-insulating substrate. A novel reactive-ion etching process that utilizes a $BCl_3/SiCl_4/Ar$ chemistry has been used to define fins as narrow as 20 nm with an aspect ratio of 10. The fins feature smooth sidewalls that are highly vertical in the top ~70 nm. To further smooth the sidewalls, we perform multiple cycles of digital etching. This consists of a self-limited oxidation/wet-etch sequence that reduces the fin width by ~2 nm per cycle. Immediately after digital etching, the sample is loaded into the atomic layer deposition for gate dielectric deposition. Gating from the top facet of the fin is suppressed by leaving in place the SiO_2 hard mask (>25 nm thick) that was used in their patterning. Sputtered Mo is used as gate metal and patterned by reactive ion etching. Evaporated Mo/Ti/Au is used for source and drain contacts and pads. The final step is annealing in forming gas. A typical device consists of 100 fins, 5 mm in length, with fin widths (W_f) ranging from 10 to 40 nm. Output characteristics of a typical device with a fin width of 12 nm are shown in Figure 2, left.

Using mobility data, we extracted the carrier concentration in the fin as a function of gate bias (Figure 2, right). In our devices, once the fin is fully depleted, the ideal value of the subthreshold swing (S) is 60 mV/dec. The softer subthreshold behavior that we observe reveals the presence of interface states (D_{it}) on the fin sidewalls. We have extracted the interface state density across the bandgap by comparing our measurements with Poisson-Schrodinger simulations. A U-shape D_{it} distribution emerges that provides excellent agreement with measurements on transistors over the entire range of fin width. This D_{it} profile is consistent with previous observations on planar MOSFETs. A minimum value of ~3×10^{12} $eV^{-1}cm^{-2}$ close to the conduction band edge is obtained. This value bodes well for the viability of future trigate MOSFETs that do not require a wide bandgap semiconductor barrier layer on the sidewalls.



▲ Figure 1: SEM image of device cross-section.



▲ Figure 2: Left – output characteristics of 12 nm fin width device. Right – measured and simulated carrier concentration as a function of gate voltage for different fin width devices. Inset - interface density of states used in the simulations.

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Nano-scale Metal Contacts for III-V MOSFETs

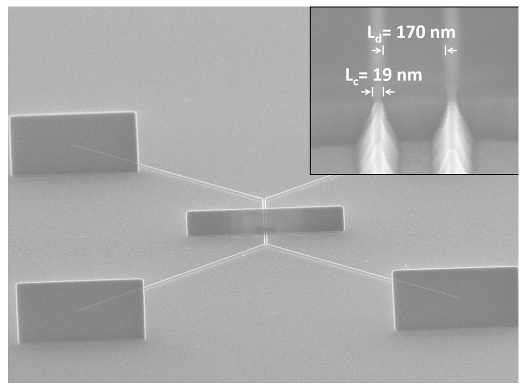
W. Lu, J.A. del Alamo
Sponsorship: SRC/FCRP MSD, SRC, Intel

In the last few years, III-V compound semiconductors have emerged as one of the most promising family of materials to replace silicon in logic applications. Novel III-V MOSFET prototypes with excellent electrical characteristics have been recently demonstrated. In III-V MOSFETs, achieving a low parasitic source resistance remains one of the greatest challenges as it limits the on-state current (I_{on}) of the device. The contact resistance, R_c, is a major component of the source resistance. As transistor scaling continues, the contact resistance is expected to increase quickly as the contact length shrinks. It is therefore urgent to fabricate and accurately characterize high-quality ohmic contacts with contact length smaller than 30 nm.

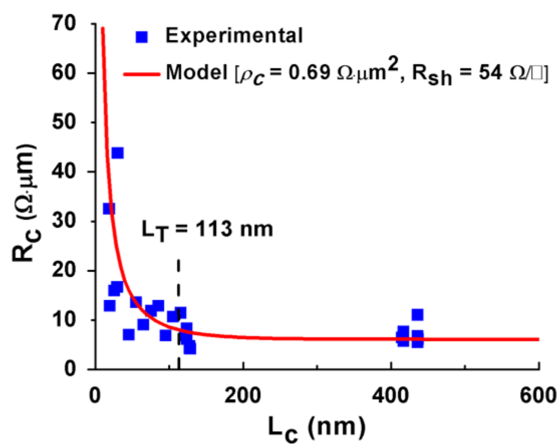
In this work, we develop a novel test structure called a nano-transmission line model (nano-TLM) to study and optimize metal contacts for III-V field-effect transistors. We also demonstrate the nano-TLM structure using a Mo/n$^+$-InGaAs ohmic contact system. We design a metal-first fabrication process and use electron-beam lithography to fabricate nano-TLMs with contact length as small as 19 nm, the smallest contacts we have achieved to date. Figure 1 shows a micrograph of a finished device.

The nano-TLMs are characterized using Kelvin 4-terminal measurements. To extract the contact resistance, the nano-TLM is modeled analytically using a 2-D circuit network. From measurements on many nano-TLM structures, we have extracted an average contact resistivity of 0.69 Ω·µm², the lowest reported value so far at a carrier concentration of 1×10^{19} cm^{-3}. For relatively long contacts (>110 nm), this value corresponds to an extremely small contact resistance of 6.6 Ω·µm. Figure 2 shows the trend of the contact resistance versus contact length. A simple model for the contact resistance does a good job of describing its behavior over the entire range of contact lengths. We experimentally show the fact that the contact resistance blows up at small contact lengths, something that is expected theoretically. This result highlights the critical importance of achieving ultrasmall contact resistance in future scaled MOSFET technologies.

Our research will continue to optimize the contact fabrication to achieve lower contact resistance and further scaling. We are also investigating the contact resistance to the buried channel of a MOSFET. In addition to metal contacts to n-type III-V semiconductors, we are exploring contacts to p-type Sb-based heterostructures for future p-type MOSFET technology.



▲ Figure 1: Nano-TLM test structure to measure the contact resistance of nanoscale contacts to InGaAs. Inset: 19-nm-long Mo contacts to InGaAs.



▲ Figure 2: Contact resistance vs. contact length for nanoscale Mo/n+-InGaAs contacts. The data is consistent with a contact resistivity of 0.69 Ω·µm² and a semiconductor sheet resistance of 54 Ω/□.

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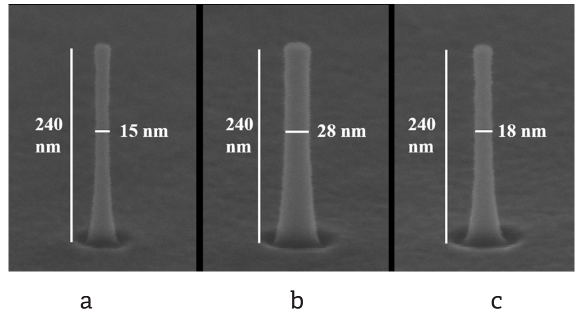
Nanometer-scale Reactive Ion Etching of InGaAs for 3-D III-V MOSFETs

X. Zhao, J.A. del Alamo
Sponsorship: NSF Center for Energy Efficient Electronics Science

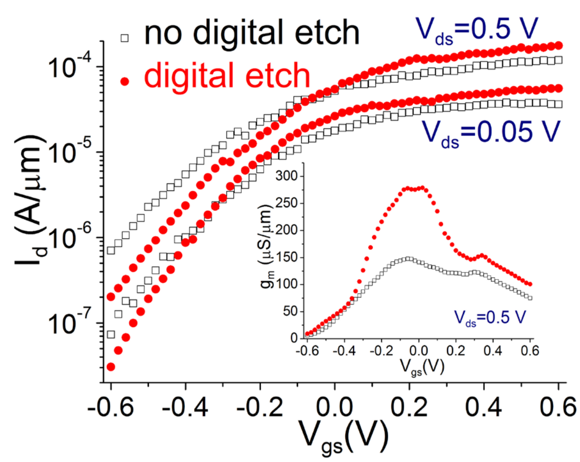
Future complementary metal oxide semiconductor (CMOS) scaling requires novel 3-D device architectures with trigate and nanowire (NW) structures with dimensions in the few-nanometer regime. Recently, InGaAs has emerged as a promising high-mobility channel material candidate to extend the CMOS roadmap. In future 3-D III-V MOS field-effect transistors (MOSFETs) fabricated via a top-down approach, a dry etch process capable of defining nanometer-scale fins and NWs in InGaAs-based heterostructures is essential. We demonstrate for the first time sub-20-nm diameter InGaAs NWs with vertical sidewalls and an aspect ratio greater than 10. A novel inductively coupled plasma-reactive ion-etching (ICP-RIE) technique using $BCl_3/SiCl_4/Ar$ chemistry achieves this result.

RIE is widely employed in the industry to realize precision structures. In-containing compounds are notoriously difficult to etch with Cl-based chemistry. We have successfully solved this problem by carefully optimizing the etching conditions, including substrate temperature, substrate bias power, chamber pressure and gas flows. Figures 1a and 1b show NWs with diameters (D) of 15 and 28 nm, respectively, and an aspect ratio greater than 10 fabricated by our etching technology. The NWs feature low surface roughness and a smooth and vertical sidewall. To mitigate potential dry etch damage just below the NW sidewall, a digital etch (DE) process is used. In our approach, a DE cycle is a two-step process consisting of self-limiting low-power O_2 plasma oxidation followed by diluted H_2SO_4 rinse for oxide removal. Figure 1c shows the same NW as in Figure 1b after 5 cycles of DE.

To demonstrate the suitability of the RIE+DE process to yield high aspect ratio 3D devices, we have fabricated vertical nanowire gate-all-around InGaAs MOSFETs. Figure 2 shows subthreshold and transconductance (g_m) (inset) characteristics of D=30 nm devices with and without DE. Digital etching improves both charge control and transport characteristics by reducing RIE damage. NW-MOSFETs fabricated via our top-down etch techniques match performance of devices fabricated by bottom-up techniques.



▲ Figure 1: (a) 15-nm diameter (D= 15 nm) InGaAs NW defined by optimized RIE technique with aspect ratio over 15. (b) D= 28-nm InGaAs NW fabricated by RIE. (c) Same NW as in (b) after 5 subsequent cycles of digital etch.



▲ Figure 2: Impact of digital etch on subthreshold and transconductance (inset) characteristics of 30-nm diameter gate-all-around InGaAs NW MOSFETs. 30 nm is the final device diameter.

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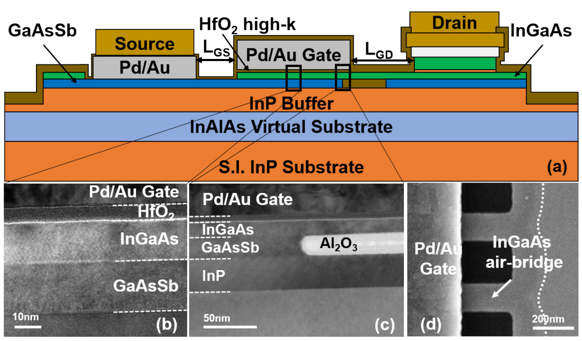
InGaAs/GaAsSb Quantum-well Tunnel-FETs

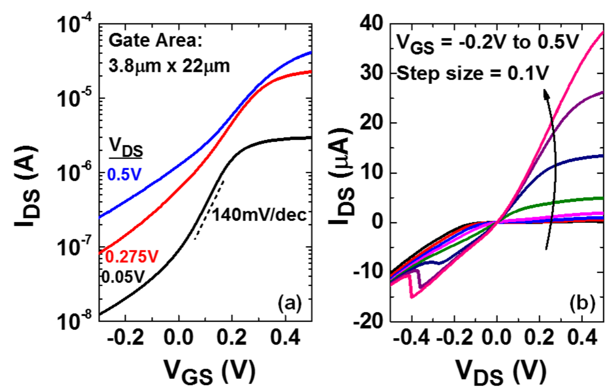
T. Yu, J.T. Teherani, J.L. Hoyt
Sponsorship: National Science Foundation

With the continuing downscaling of modern CMOS technology, integrated circuit power consumption has become one of the most critical issues. This is due to the limit of operation voltage scaling, which originates from the limit of 60mV/dec subthreshold swing (SS) in the conventional MOS devices. Various device structures have been proposed to achieve subthreshold swing below 60mV/dec using novel device physics, including impact ionization, interband tunneling, etc. In particular, tunnel-FETs (T-FETs) have attracted much attention due to their potential of achieving sharp subthreshold behavior, CMOS compatibility, and scalability. Quantum-well T-FETs (QWTFETs) with an ultra-thin heterojunction structure have been proposed to yield sharp turn-on over a wide range of drive currents, and they are one of the potential candidates for future generation low-power technology. We have demonstrated experimental InGaAs/GaAsSb QWTFETs with minimum SS of 140 mV/dec at 300 K.

Figure 1 (a) shows the cross-sectional view of the InGaAs/GaAsSb QWTFET. The self-aligned source recess and air-bridge structure are used in the device to eliminate parasitic tunneling paths in the ungated regions. Figures 1 (b)-(d) are the XTEM and SEM images of the fabricated device with the air-bridge self-aligned to the gate. The transfer and output characteristics of a TFET are plotted in Figures 3 (a) and (b). The minimum (point) SS at low V_{DS} is 140 mV/dec. and the effective SS for I_{DS} from 20 nA to 2 μA is 220 mV/dec. The output characteristics show good saturation for positive V_{DS}, and V_{GS}-dependent negative-differential-resistance (NDR) is clearly seen in the negative V_{DS} region. This is solid evidence of the tunneling nature of the device operation. Two factors have been identified that impact the SS: high OFF current and high D_{it} in the InGaAs conduction band at the HfO_2/InGaAs interface (not shown here). Optimized device structures have been proposed to improve the device performance in the future.



▲ Figure 1: (a) Schematic cross-section view of fabricated $In_{0.53}Ga_{0.47}As$/ $GaAs_{0.5}Sb_{0.5}$ vertical TFET; (b) HR-XTEM of tunneling junction and gate stack in gated region; (c) XTEM at edge of InGaAs air-bridge; (d) Top-view SEM image of InGaAs air-bridge after suspension. The air-bridge is self-aligned to gate, and outline of etched GaAsSb is highlighted.



▲ Figure 2: (a) Transfer and (b) output characteristics of the fabricated TFET with gate dimensions of 3.8 × 22 μm^2.

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High-voltage Vertical GaN Diodes on Si Substrates

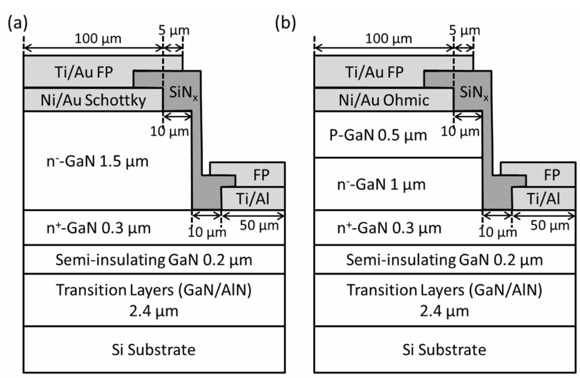
Y, Zhang, M. Sun, D. Piedra, M. Azize, T. Fujishima, T. Palacios
Sponsorship: ARPA-E Switches Program, MIT/MTL GaN Energy Initiative

GaN-based devices are excellent candidates for high-power switching applications. Currently, both vertical and lateral devices are being considered. GaN vertical devices have attracted increased attention recently, due to their potential for sustaining high breakdown voltage (*BV*) without enlarging chip size and their superior thermal performance. However, current GaN vertical devices suffer from the need for expensive GaN substrates, which has become a main obstacle for their development. Lower-cost substrates for GaN vertical devices could significantly reduce the cost of the final device; however, no GaN vertical power devices on Si substrates have been reported so far.

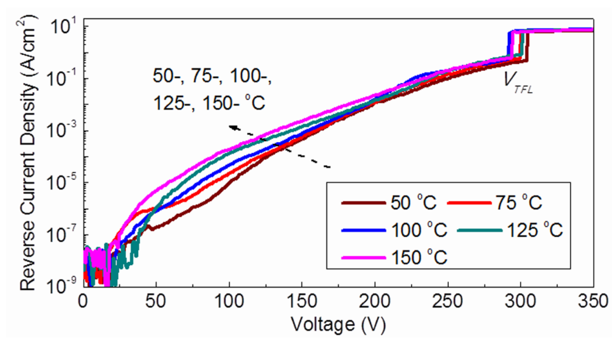
This work demonstrates vertical GaN-on-Si Schottky barrier diodes (SBDs) and p-n diodes for the first time. The structure of the GaN-on-Si vertical SBD and p-n diodes consists of n^--GaN (p-GaN), n^+-GaN, semi-insulating GaN, transition layers, all grown on a 3-inch Si substrate.

Two key processes were developed to suppress the parasitic leakage currents along the etching sidewall and dielectric/GaN interface in the vertical diodes. First, a GaN deep etching process was developed in an inductively coupled plasma reactive ion etching (ICP-RIE) system by using $Cl_2/BCl_3/Ar$ gas system. This deep etching technology achieved a smooth etching sidewall with low sidewall leakage. Second, we used a new technology based on sputtering deposition system and optimized pre-treatment to improve the passivation layer. This technology effectively reduces the surface leakage widely reported previously for traditional passivation using PECVD systems.

By utilizing the above technologies, we have fabricated vertical GaN-on-Si Schottky and p-n diodes. With a total GaN drift layer of only 1.5 μm thick, a breakdown voltage of 205 V was achieved for GaN-on-Si Schottky diodes, and a soft *BV* higher than 300 V was achieved for GaN-on-Si p-n diodes with a peak electric field of 2.9 MV/cm in GaN. The leakage current of our GaN-on-Si vertical diodes (~10^{-2} A/cm^2 at -200 V up to at least 150 °C) is comparable to the state-of-the-art leakage reported for lateral AlGaN/GaN diodes on Si substrates. The high breakdown voltage and low leakage demonstrates the great potential of GaN-on-Si vertical devices for nitride-based power electronics.



▲ Figure 1: Schematic cross sections of GaN-on-Si vertical (a) Schottky and(b) p-n diodes with passivation and filed plate structures.



▲ Figure 2: Reverse *I* -*V* characteristics of the GaN-on-Si vertical p-n diodes at different temperatures, demonstrating a soft breakdown voltage of 300 V.

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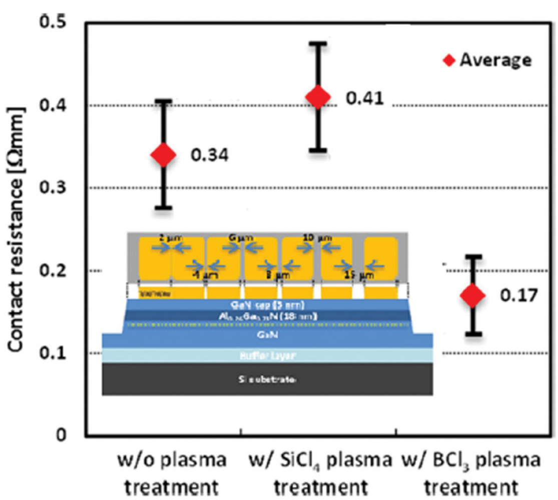
Effect of Surface Pre-treatments on Ohmic Contact Resistance in AlGaN/GaN Transistors

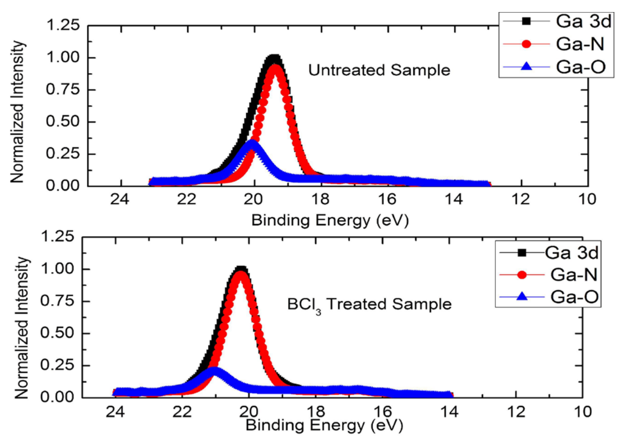
S. Joglekar, T. Fujishima, D. Piedra, H-S. Lee, T. Palacios
Sponsorship: DARPA MPC, MIT/MTL GaN Energy Initiative

GaN-based high electron mobility transistors (HEMTs) have been recently targeted for high-power, high-frequency, and high-temperature operation electronic devices for mobile communication systems, radars, and power electronics because of their high critical breakdown fields, high saturation velocities, and high thermal conductivities. To achieve excellent performance in these devices, it is necessary to have uniform low resistance ohmic contacts. In this work, we studied the effects of various wet and dry surface pre-treatments on the ohmic contact resistance of alloyed Ti/Al/Ni/Au contacts on AlGaN/GaN devices. Figure 1 shows the contact resistance measured after different pre-treatments. The contact resistance is found to be the lowest for a boron tri-chloride (BCl_3) gas dry plasma treatment, which is applied prior to metal deposition. The inset shows the schematic cross section of the transmission line measurement (TLM) patterns used for contact resistance measurements. These are ohmic contacts with different spacings between them. A plot of the resistance vs. the spacing gives the contact resistance. To obtain low-resistance, uniform ohmic contacts, it is necessary to remove the native oxide on top of semiconductors before metal deposition.

Figure 2 shows the X-ray photoelectron spectroscopy (XPS) data on treated and untreated samples. It was found that low power BCl_3 plasma is effective in removing native oxide from the GaN surface without etching the GaN. In addition, an increase in surface donor density was found due to the BCl_3 treatment, resulting in increased electron density at the surface and reduced contact resistance. Other treatments investigated were $SiCl_4$ plasma and wet HCl. The $SiCl_4$ plasma treatment tends to form a thin SiOx layer on the surface, thus increasing the contact resistance. HCl also removes native oxides but is not effective in creating surface donors, and hence the contact resistance obtained is higher than with BCl_3. Thus BCl_3 treatment demonstrates the potential to achieve low and uniform contact resistance without recessing in AlGaN/GaN devices.



▲ Figure 1: Cross-sectional of TLM structure used to measure contact resistance.



▲ Figure 2: XPS showing decrease in Ga-O due to BCl_3 treatment.

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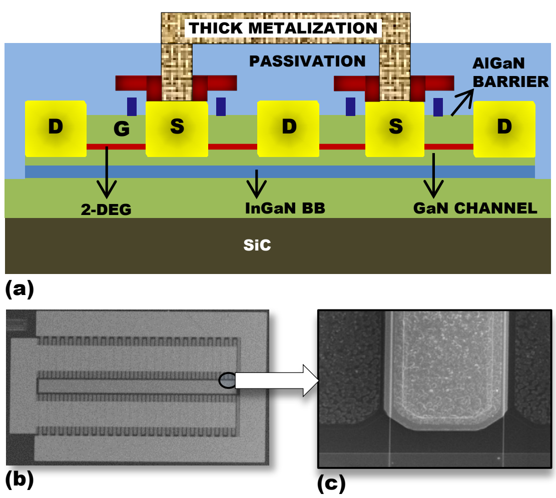
Performance Limits of Large-periphery GaN Power Amplifiers

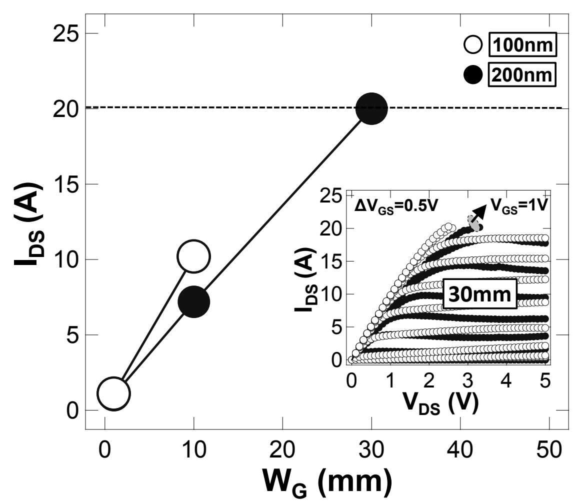
P. Srivastava, D. Piedra, O. Saadat, U. Radhakrisna, J. Scholvin, J. Fiorenza (Analog Devices), T. Palacios
Sponsorship: Schlumberger

GaN-based high-electron-mobility transistors (HEMTs) have been identified as essential high-frequency devices for various microwave or millimeter-wave applications due to GaN's outstanding material properties such as high electron velocity (~ 2.5 × 10^7 cm/s) and high break-down electric field (~ 3.3 MV/cm). These applications require a combination of excellent radio frequency (RF) characteristics and high-power performance. The enhancement of power characteristics can be achieved by improving the current level or breakdown voltage of the HEMTs; however, very limited work has been done so far in understanding the ultimate limit in the power-handling capability of GaN-based electronics.

Large-periphery AlGaN/GaN-HEMTs with InGaN back-barriers on SiC substrate having deep sub-micron gate lengths (L_G) have been designed and fabricated successfully with a maximum gate periphery W_G = 30mm, as in Figure 1. To extract the highest current density from these devices, aggressive lateral scaling with a thick metal interconnect (aluminum) of ~3 µm is integrated. The fabricated transistors show excellent pinch-off characteristics and current density scaling with W_G, as shown in Figure 2. The transistor with W_G = 30 mm and L_G = 100 nm have demonstrated an on-state current of more than 20 A; to the best of our knowledge, this is the first demonstration of a transistor with W_G = 30 mm having only L_G = 100 nm. In addition to the high current density, these devices also show a high breakdown voltage of over ~70 V by incorporating a source field plate. The high frequency (2 GHz) output power (P_{OUT}) of a device with W_G = 200 µm shows a value of 12.3 W/mm (V_{DS}=50 V) measured under class-AB configuration and is one of the highest ever reported P_{OUT} at V_{DS}=50 V. The associated Gain and PAE are 28 dB and 50%. Future work will focus on realizing power performance at higher frequency based on T-gate configuration.



▲ Figure 1: (a) Cross-sectional view of the fabricated large periphery transistors, (b) fabricated transistor with total gate W_G = 30 mm, and (c) close-up view of the active region with a deep sub-micron gate and source field plate.



▲ Figure 2: Measured drain current (I_{DS}) for a multifinger transistor at V_{GS}=1V and V_{DS}=5V. The inset shows the characteristics curves for large periphery transistor (30 mm) with 100-nm and 200-nm gate lengths.

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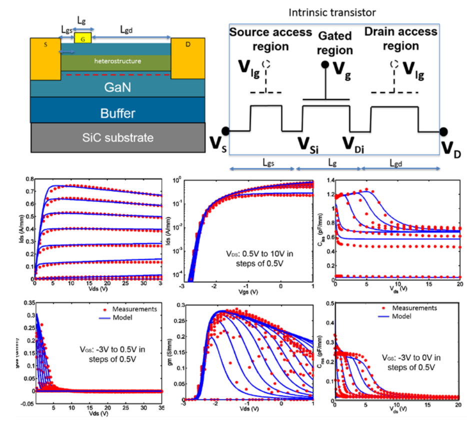
Design of RF GaN HEMT Power Amplifier Using MIT Virtual Source GaNFET-RF Model

U. Radhakrishna, P. Choi, P. Srivastava, D. Piedra, T. Palacios, D. Antoniadis
Sponsorship: SMART-LEES, MIT/MTL GaN Energy Initiative

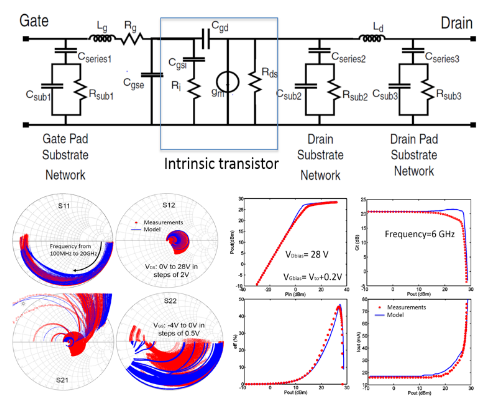
GaN devices outperform CMOS devices for RF power amplifiers (PA) in terms of output power and efficiency, which has resulted in increasing novel circuit applications as the technology matures. The MIT Virtual Source GaNFET–RF (MVSG-RF) compact model captures velocity-saturation/quasi-ballistic carrier transport in highly scaled GaN HEMTs through physics-based analytical expressions. While the model describes the DC and small-signal characteristics, capturing large signal device characteristics is critical for designing non-linear circuits for RF and mm-wave applications. In this work, we extend the MVSG-RF model to predict the large-signal device characteristics that are validated against load-pull measurements of commercial devices.

The intrinsic GaN HEMT region (shown in Figure 1a) is modeled as a sub-circuit of three transistors in series as Figure 1b shows. The gated region is modeled as a virtual source transistor while the non-linear access regions are modeled as implicit-gate transistors. The model is validated against IV measurements of commercial 0.25-mm RF devices as shown in Figure 1c. Bias-dependent input (C_{iss}) and reverse transfer (C_{rss}) capacitances are shown in Figure 1d as a function of drain bias from off-to-on states and match well with measurements. The next step towards large-signal modeling is to add the effect of a bias-independent passive network around the intrinsic transistor of Figure 1, which includes the parasitics associated with pads, substrate, terminal leads; the small-signal equivalent circuit model used for this purpose is shown in Figure 2a. The parasitic elements in Figure 2a are extracted from S-parameter measurements, and the model is compared against measurements (in Figure 2b) across wide bias and frequency ranges. The model benchmarked against small-signal measurements is then used for modeling large-signal devices behaviors in the PA circuit of a 0.25 mm GaN frontend circuit for vehicle-to-vehicle communication.

The commercial GaN-on-SiC device with a width of 2×180 mm is biased at V_{Dbias}=28 V and V_{Gbias}=V_{to}+0.2 V in a class AB mode. The input and output impedances are tuned (up to 3rd harmonics) to obtain maximum P_{out}, and a power sweep is performed at 6 GHz, using *Maury Microwave* setup. The results are compared against harmonic balance simulations that mimic these large-signal measurements in *ADS* software. The MVSG-RF model predicts power sweep metrics such as P_{out}, power gain (G_t), and power added efficiency (PAE) accurately without requiring additional parameters, as Figure 2d shows. The peak power (28.7 dBm) and peak PAE (47%) match well with measurements. MVSG-RF model is thus very accurate and useful for designing GaN-based RF PAs.



▲ Figure 1: (a) Device cross-section schematic, (b) Equivalent circuit model for intrinsic transistor showing the sub-circuit transistors in series, (c) DC model comparison against output and transfer drain current measurements and its derivatives, (d) Small signal non-linear input and reverse transfer device capacitances validated against measurements.



▲ Figure 2: (a) Equivalent small signal circuit for the MVSG-RF model including pad and substrate parasitics (b) Device S-parameters compared between model and measurements (c) Large signal power sweep validation for class AB operation of the device at 6 GHz. The measured power gain, output power and power added efficiency figures match well with the device model.

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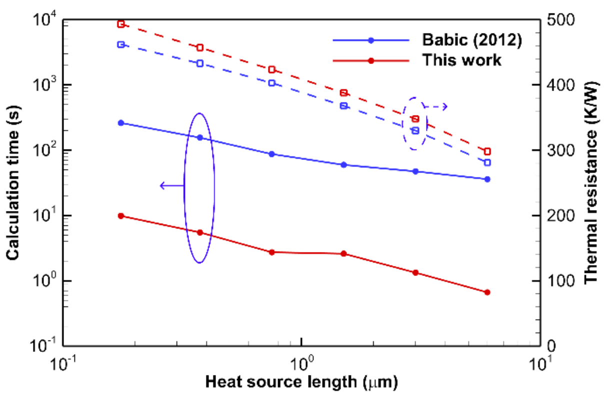
Thermal Characterization of GaN-based Electronics

K.R. Bagnall, B. Barabadi, O.I. Saadat, S.J. Joglekar, T. Palacios, E.N. Wang
Sponsorship: MIT/MTL GaN Energy Initiative, SMART-LEES

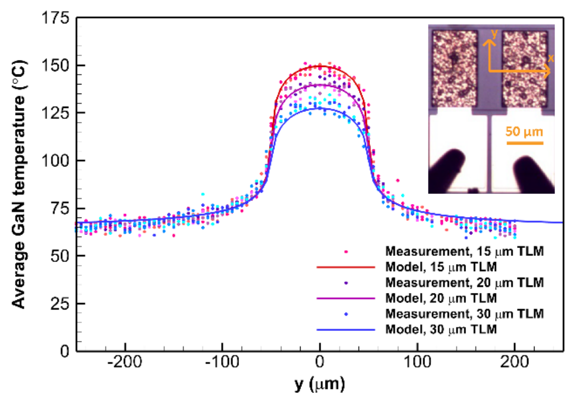
Gallium nitride (GaN)-based electronics are one of the most exciting semiconductor technologies for high-power, high- frequency electronics due to GaN's unique combination of a high critical electric field, carrier concentration, and electron mobility. Although radio-frequency (RF) power densities greater than 40 W/mm have been demonstrated, typical devices are practically limited to one-tenth of this value due to the associated high junction temperatures and degraded performance and reliability. In this work, we have developed analytical thermal models to understand the key dependencies of channel temperature rise and have validated these models with micro-Raman thermography.

Although numerical techniques such as the finite element method are commonly used in thermal modeling of GaN high electron mobility transistors (HEMTs), the large difference in length scales between the region of power dissipation (~1 μm) and chip size (~1000 μm) makes these methods computationally inefficient. In contrast, we have analytically solved the steady-state heat equation for a multi-layer structure with interfacial resistances, temperature-dependent thermal conductivity, and flexible boundary conditions. As shown in Figure 1, we have demonstrated that this solution requires two orders of magnitude less computation time than semi-analytical and numerical methods and provides useful insight on the performance of GaN-on-Si and GaN-on-diamond HEMTs.

In addition, we have utilized micro-Raman spectroscopy to measure the temperature of GaN devices under bias with ~1 μm spatial resolution. We find that the temperature profiles on ungated AlGaN/GaN structures on SiC substrates are in good agreement with our model, as Figure 2 shows. This work provides helpful insight into device design and operation by providing accurate prediction of the temperature near the electronic junction.



▲ Figure 1: Calculation time and thermal resistance of a GaN-on-Si HEMT structure for this work and semi-analytical approach of Babic, *J. Heat Transfer*, 2012. Analytical model in this work is approximately two orders of magnitude more efficient.



▲ Figure 2: Average GaN temperature along the width of ungated (transmission line method or TLM) AlGaN/GaN structures on SiC substrates. Good agreement between model and measured temperature profiles is shown for ungated structures of lengths from 15 to 30 μm.

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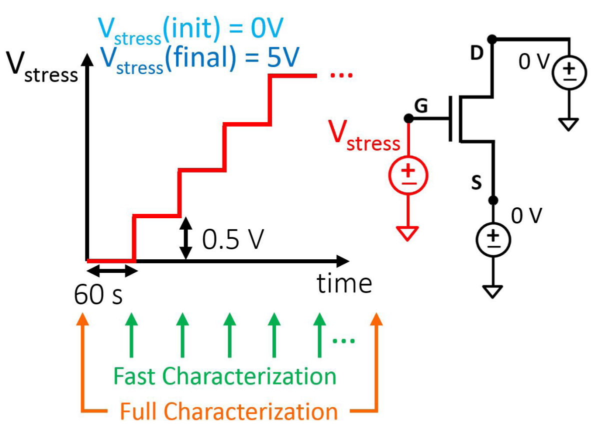
A Stress/Characterization Strategy to Assess the Electrical Reliability of High-voltage GaN Field-effect Transistors

S. Warnock, J.A. del Alamo
Sponsorship: SRC

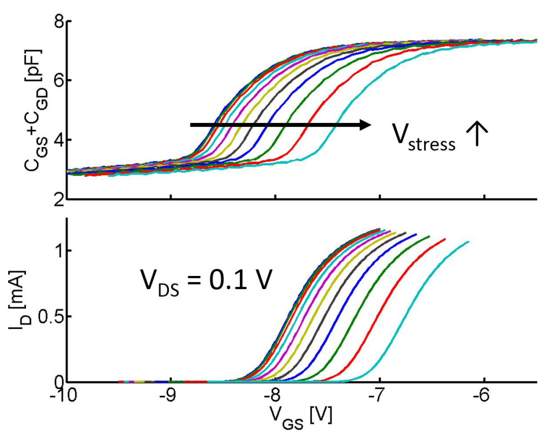
As the demand for more energy efficient electronics increases, GaN field-effect transistors (FETs) have emerged as promising candidates for high-voltage power management applications. Though GaN has excellent material properties, there are still many challenges to overcome before GaN transistors are ready for commercial deployment. One of the concerns, for example, is a phenomenon known as current collapse or dynamic ON resistance, where the ON-resistance of the FET increases dramatically after high-voltage OFF-state biasing, due to excessive trapping. Another problem that interests us is oxide reliability as a result of high voltage stress.

We are interested in contributing fundamental understanding of the physics behind the instability and reliability of high-voltage GaN FETs. Such studies require quick and accurate characterization of transistors during high stress experiments. To meet this goal, we have developed a stress-characterization suite in MATLAB to carry out a variety of stress and recovery tests. Our experimental configuration allows us to isolate DC (for stress and I-V characterization) and AC (for C-V characterization) signals from each other, so we can apply high-voltage stress to a GaN FET, interrupt it, measure the C-V or I-V characteristics (or both) that give a picture of the degradation that may be occurring, and then resume the stress. All of this can be done automatically and without changing the cabling configuration.

Figure 1 shows the details of a typical Step-Stress experiment. We increase the stress voltage applied to the gate of a FET by steps. The drain and source are both grounded. Detailed device characterization is performed at the beginning and end of the experiment, while fast characterization is carried out at the end of each stress step. The circuit diagram shows the FET terminal connections during the stress phase. Figure 2 shows the corresponding C-V and I-V characteristics taken during the experiment. As the experiment progresses, the threshold voltage shifts positive in an increasing manner as the applied stress voltage increases. Preliminary experiments like this one show that our stress-characterization approach will be a powerful tool for exploring reliability and instability issues of high-voltage GaN FETs.



▲ Figure 1: Forward gate voltage step-stress experiment in GaN FET. V_{stress} (V_G) is applied for 60 s and increased from 0 to 5 V in 0.5-V steps. Drain and source terminals are held at 0 V during stress period. I-V and C-V characterization are performed after each stress step.



▲ Figure 2: C-V (top) and I-V (bottom) characteristics of GaN FET during stress experiment of Figure 1. C-V measurements were taken at 500 kHz, and I-V at V_{DS} = 0.1 V.

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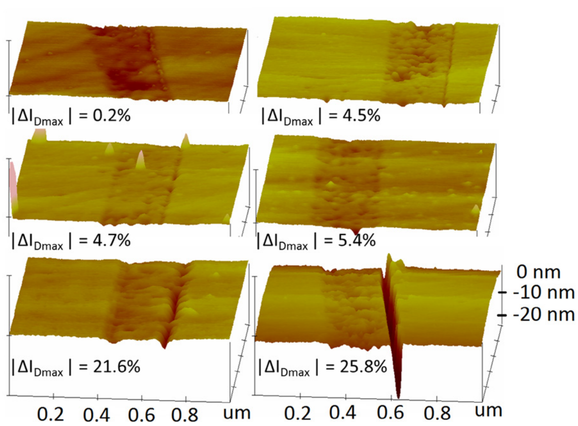
Structural Degradation of GaN HEMTs under High-power and High-temperature Stress

Y. Wu, J.A. del Alamo
Sponsorship: Office of Naval Research DRIFT-MURI

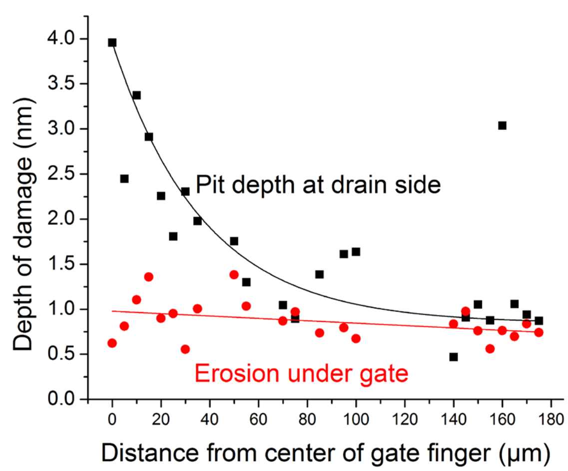
As a result of their wide band gap energy and high breakdown electric field, GaN heterostructure transistors are promising candidates for high-power and high-frequency applications. However, the reliability of GaN high-electron-mobility transistors (HEMTs) is still a major issue that prevents their wide deployment. Several works have shown the appearance of prominent physical damage on the semiconductor surface in the vicinity of the gate after prolonged OFF-state stress. In power amplifier applications, however, the device is typically biased in the ON-state. In spite of its importance, very little research exists on the impact of prolonged high-power stress on the structural degradation of the device. This project investigates the structural degradation of GaN HEMTs biased in the high-power regime.

We stressed GaN transistors at high voltage and current for prolonged periods of time. In all stressed devices, we identified pits and trenches similar to those observed under OFF-state conditions. The degree of physical damage as represented by the width and depth of trenches is found to positively correlate with the overall drain current degradation. Shown in Figure 1 are AFM scans of six different devices with different levels of degradation of the maximum drain current, I_{Dmax} (defined @ V_{DS} = 5 V, V_{GS} = 2 V). The more the I_{Dmax} degrades, the more severe the physical damage at the gate edge. An unexpected finding is visible erosion under the entire gate of the stressed devices, which we have found directly correlates with channel resistance, R_{CH}, degradation.

In agreement with previous studies by our group, we have found that the pit and trench formation at the gate edge is strongly thermally activated. However, the under-gate erosion is only weakly dependent on temperature. Figure 2 shows the average pit depth and under-gate erosion depth as a function of gate finger location starting from the center of the gate. Pit depth is the largest at the center of the gate finger, where the device junction is the hottest, and it decreases away from the center towards the end of the gate finger, where the temperature is lower. In contrast, under-gate erosion is weakly dependent on location. This finding strongly suggests that two different degradation mechanisms are at work.



▲ Figure 1: AFM pictures of the delaminated surface of six devices that have been stressed under V_{DS} = 40 V and I_{DQ} = 100 mA/mm. From top left to bottom right pictures, overall I_{Dmax} degradation increases.



▲ Figure 2: Distribution of pit depth along half of the gate width for the device with an overall I_{Dmax} degradation of 21.6%. Each point in the graph represents an averaged value across a 5-μm scan.

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Threshold Voltage Instability in GaN Power Field-effect Transistors

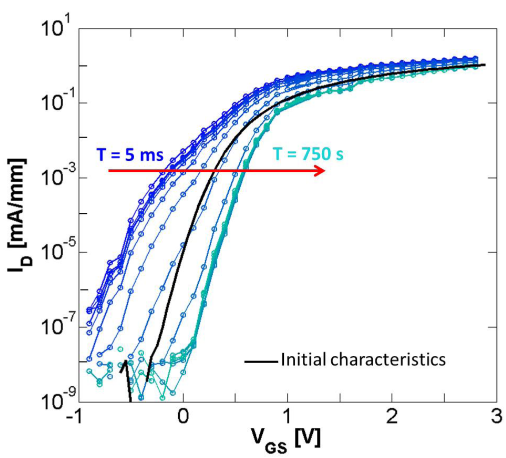
A. Guo, J.A. del Alamo
Sponsorship: NDSEG Research Fellowship

Gallium nitride (GaN) exhibits a higher electron mobility and a higher bandgap than silicon. This combination endows GaN power field-effect transistors (FETs) with a very low ON resistance, fast switching frequency, and an ability to handle large voltages. This makes them a promising alternative to silicon transistors in various high-voltage switching applications including electric vehicles, DC-DC converters, and solar and wind turbine applications. At the same time, GaN power FETs suffer from reliability and stability problems, particularly under high-voltage operation. In this study, we address an important reliability concern, which is the stability of the threshold voltage (V_T) under high-voltage stress.

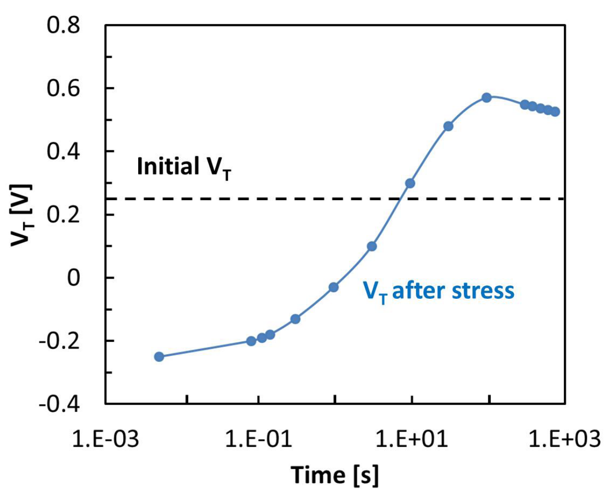
To understand the impact of high voltage stress on the threshold voltage of GaN power FETs, we have developed a benign measurement scheme so that V_T is not affected by the measurement itself. This is especially important for GaN devices because the significant trapping that takes place can "fog" the measurement results. We stress the device at different gate and drain voltages and examine the evolution of V_T during stress. Periodically, we use a thermal step to detrap electrons and return the device to a well-defined state that we use to assess degradation. Preliminary observations show that the magnitude and direction of V_T shift (ΔV_T) are related to both the location (either gate or drain) and magnitude of the stress voltage. In general, $|\Delta V_T|$ increases with the increase of the voltage stress. For reverse gate stress less than 40 V and drain stress less than 90 V, the V_T shift is fully recoverable, suggesting that it is entirely due to trapping.

To understand the cause of this V_T instability, we have developed a technique to map the evolution of the entire transfer characteristics of a transistor after voltage stress in a time scale that starts at 5 ms. This mapping was done by tracing the drain current as a function of time at different gate biases after the stress is removed. Thermal detrapping was used to restore the device to its original state after each trace. Figure 1 shows a typical result after stressing a typical device at V_{GS}=-20 V and V_{DS}=0 V. A prominent negative shift in V_T right occurs as a result of stress that is followed by a positive V_T overshoot. Figure 2 shows this peculiar time evolution of V_T more clearly. The negative V_T shift right after the stress period is restored at around 10 seconds, yet V_T continues to shift positive till about 100 seconds; it slowly starts to recover towards its original value. These observations suggest that the V_T shift under negative gate voltage stress is the result of two competing trapping mechanisms with different impacts on the sign of ΔV_T and different time constants.

Going forward, we will map out the key dependencies of this V_T instability, uncover its physical origin, and provide design recommendations to minimize this problem in GaN power FETs.



▲ Figure 1: Subthreshold characteristics at V_{DS}= 0.1 V of GaN power MOSFET after negative V_{GS} stress (V_{GS}= -20 V, V_{DS}= 0 V) for 30 s. First trace shown is taken 5 ms after stress stops. The last is taken at t= 750 s. Initial characteristics of the virgin device also appear.



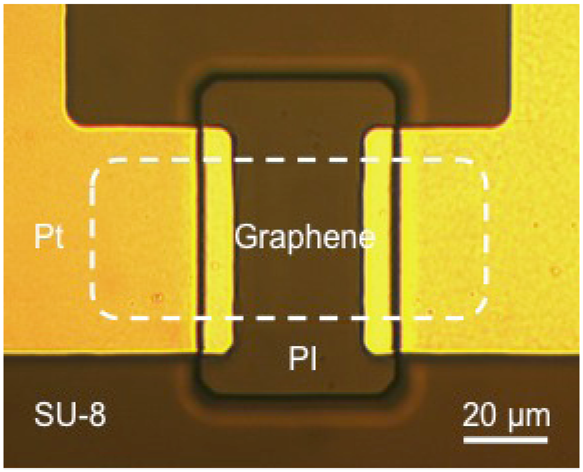
▲ Figure 2: Time evolution of V_T (defined at drain current = 1 µA/mm) for experiment in Figure 1.

Current-voltage Model for Graphene Solution-gated Field-effect Transistors

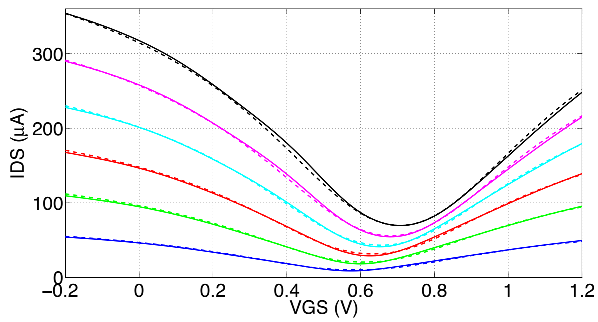
C. Mackin, A. Hsu, L. Hess, Y. Song, J. Kong, J. Garrido, T. Palacios
Sponsorship: Institute for Soldier Nanotechnologies

Graphene's chemical resilience enables a direct interface with many chemical and biological environments. This trait is particularly beneficial for the electrolytic environments present in a variety of biological and chemical sensing applications because graphene can exploit the electrical double layer phenomenon and resulting ultra-high interface capacitance. This large capacitance coupled with graphene's high mobility enables high-transconductance and low-noise field effect transistor (FET) sensors. In addition, the recent development of chemical vapor deposition growth processes enables graphene to span large-areas with continuity and consistent material properties at low cost.

A number of models have been developed to study and predict the behavior of metal-oxide-gated graphene FETs. Little work, however, has been reported for graphene solution-gated FET models. Solution-gated graphene FET models represent an increase in complexity over metal-oxide-gated graphene FETs because the top-gate capacitance cannot be considered constant. The top-gate capacitance of graphene SGFETs, which is comprised of the electrical double layer capacitance and graphene quantum capacitance, varies as a function of ionic species and concentration and also spatially along the graphene channel.



▲Figure 1: MTL fabricated graphene solution-gated field-effect transistor.



▲Figure 2: Experimental (solid) and simulated (dashed) source-drain current versus V_{GS}. V_{DS} varies from 50 mV to 300 mV in increments of 50 mV.

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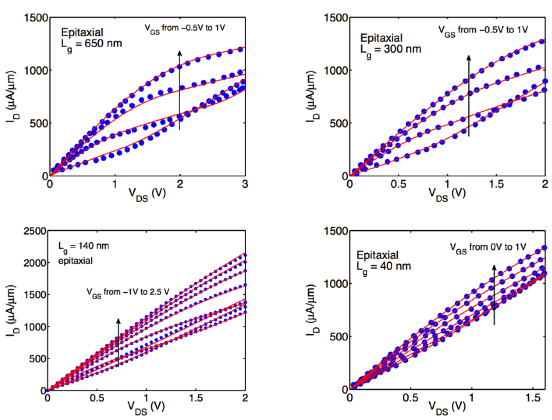
An Ambipolar Virtual-source-based Charge-current Compact Model for Nanoscale Graphene Transistors

S. Rakheja, D.A. Antoniadis
Sponsorship: NSF NCN – NEEDS Node

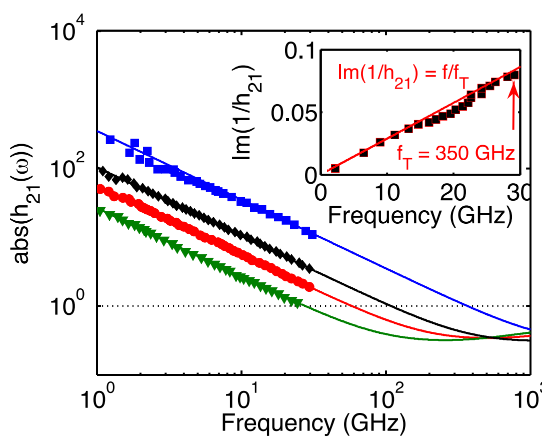
The rich physical properties of graphene make it an excellent candidate for implementing a variety of high-frequency analog electronic devices. To design and simulate electronic circuits built with graphene devices, we need compact device models that include both a description static transport of carriers in the device and dynamic channel-charge distribution.

This work has developed a transport model based on the concept of a virtual source for graphene field-effect transistors (GFETs) in both unipolar and ambipolar regimes of transport. The model describes the quasi-saturation in GFETs that occurs through the shift in the minimum conduction point with drain-source bias in graphene. Further, the model accounts for the asymmetry introduced in the contact resistance for electrons and holes; this asymmetry arises because of the different interfacial potential barrier heights for electrons and holes. The model has a limited number of parameters, most of which have a physical meaning and can easily be obtained from device characterization. To describe the dynamic operation of the transistor, terminal charges are obtained self-consistently with the transport formulation and can be extended to the ballistic regime, where the gradual channel approximation fails. The model has been extensively calibrated with both DC I-V and s-parameter measurement of devices with gate lengths from 650 nm to 40 nm.

Figure 1 shows the output characteristics of devices with various gate lengths. Figure 1 shows that the model (solid lines) provides an excellent match with the experimental data (symbols) of these devices. Figure 2 shows the current gain versus frequency for the GFETs. Experimental data appear in symbols, while model fits appear as solid lines. The quasi-ballistic charge model provides an excellent match to the experimental data. The model developed in the work has continuous currents and charges and can easily be used in the design and simulation of circuits and systems implemented with GFETs.



▲ Figure 1: Output curves of various graphene FETs with gate lengths from 650 nm to 40 nm with Si_3N_4 top-gate dielectric. Symbols represent experimental data; solid lines are obtained from the model.



▲ Figure 2: Current gain versus frequency for GFETs. The inset of the plot shows the cut-off frequency for the 40-nm device obtained using the Gummel method. Symbols represent experimental measurements; solid lines are model fits.

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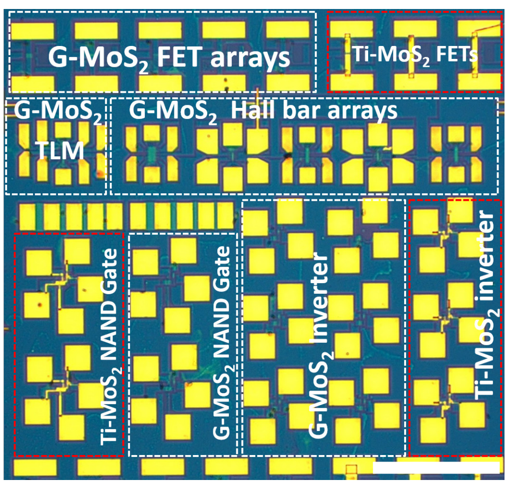
Graphene-MoS_2 Hybrid Technology for Large-scale Two-dimensional Electronics

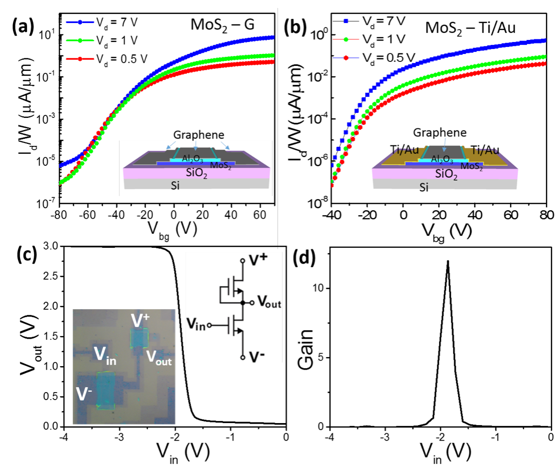
L. Yu, H. Wang, Y. Lee, X. Ling, Y. Shin, J. Kong, T. Palacios
Sponsorship: Office of Naval Research Young Investigator Program, Office of Naval Research GATE-MURI, Army Research Laboratory

Two-dimensional (2D) materials have generated great interest in the last few years as a new set of tools for electronics, for these materials can push electronics beyond its traditional boundaries. This family of materials includes metallic graphene, semiconducting transition metal dichalcogenides (such as MoS_2) and insulating boron nitride. These materials and their heterostructures offer excellent mechanical flexibility, optical transparency, and favorable transport properties for realizing electronic, sensing, and optical systems on arbitrary surfaces. To harvest the full advantages of 2D electronics in bendable electronics, constructing systems solely based on 2D materials and their heterostructures is highly desirable.

We use a novel technology to construct large-scale electronic systems based on graphene/molybdenum disulfide (MoS_2) heterostructures grown by chemical vapor growth. The atomically thin heterostructure is realized by using ALD Al_2O_3 as an etch-stop layer. This Al_2O_3 layer also acts as the top gate dielectric for the devices. High-performance devices and circuits based on this heterostructure with MoS_2 as transistor channel, graphene as contact electrodes and circuit interconnects have been fabricated, as shown in Figure 1. The systematic comparison between graphene/MoS_2 and Ti/MoS_2 devices shows that the use of graphene as contacts for MoS_2 FETs, as discussed above, provides 10 times lower contact resistance, 10 times higher on-current and field effect mobility than conventional MoS_2-metal contacts (Figure 2a,b). The Schottky barrier height of graphene/MoS_2 and Ti/MoS_2 device are extracted through low temperature measurement. The work function of graphene is strongly tuned by the back gate voltage and this unique property significantly improves ohmic contact to MoS_2. Top gated devices are also fabricated and measured. Based on this technology, basic logic integrated circuits are also demonstrated (Figure 2c,d). This technology represents the first scalable platform for constructing large scale electronics on Van der Waals' heterostructures based on 2D material monolayers.



▲Figure 1: (a) Optical micrograph of large-scale chip of MoS_2 devices and circuits using CVD graphene as electrodes and interconnects (white dashed box) and controlled devices and circuits using Ti/Au electrodes in adjacent (red dashed box). Metal pads (gold color) are fabricated on the sample for convenient measurement. (scale bar: 200μm).



▲Figure 2: (a) MoS_2-graphene (MoS_2-G) and (b) MoS_2-Ti FETs back-gate transfer performance at room temperature. Current density in left axis and transconductance in right axis. (c),(d) Demonstration of an integrated logic inverter on MoS_2-G heterostructure. (c) Output curve for MoS_2-G logic inverter. Optical image (inset, left down) and schematic of electronic circuit (inset, right up) for inverter. (d) Gain of inverter is >12.

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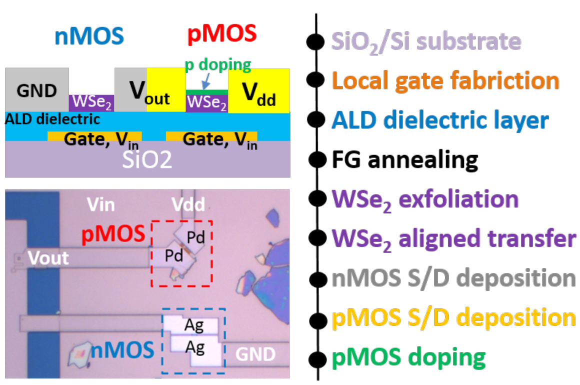
High-performance WSe_2 CMOS Devices and Integrated Circuits

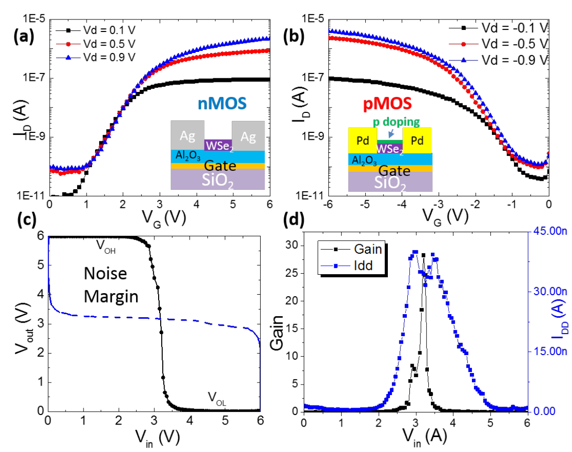
L. Yu, A. Zubair, T. Palacios
Sponsorship: NSF CIQM, Army Research Laboratory, Office of Naval Research

Two-dimensional (2D) crystals have outstanding properties for developing the next generation of electronic devices because of the excellent electrostatic control of the channel associated with their atomically thin structure. For many of these applications, the realization of complementary metal-oxide-semiconductor (CMOS) logic is crucial to get high performance integrated circuits. CMOS logic has high noise immunity, low static power consumption, and high density of integration. So far, complementary logic circuits have been demonstrated only on heterostructures of different layered materials with gain less than 2 and zero noise margins. In this work, we demonstrate both pMOS and nMOS technologies on exfoliated WSe_2, and we use them to fabricate monolithic CMOS integrated logic inverters with rail-to-rail logic operation, small power dissipation, large noise margin, and voltage gain.

Figure 1 (right) shows the fabrication process for our WSe_2 CMOS technology. The gate metal and dielectric stack were deposited before the WSe_2 layer and annealed to remove the negative charge inside the dielectric layer. Then exfoliated WSe_2 flakes were transferred on top of the gate region. A low work function metal (i.e., silver) and a high work function metal (i.e., Pd) were used to contact nMOS and pMOS FET, respectively. After source-drain contact, the nMOS FET shows strong n-type and good ohmic performance, while the pMOS FET shows weak n-type and barely p-type performance and a large Schottky barrier at the contact region. After locally doping the p-type channel, we achieved strong p-type performance and good ohmic contacts. Figures 2 a and b show the transfer characteristics of WSe_2 nMOS and pMOS FETs, respectively. They both show current on/off ratio larger than 10^5 and pinch-off current saturation. The field effect mobility for electron and hole are 5 and 13 $cm^2/V.s.$ respectively. The figures show very symmetric threshold voltage and balanced on-current, which is crucial to get a large noise margin and gain in CMOS inverters. The optical image and output performance of an integrated CMOS inverter are shown in Figure 1 and Figures 2 c and d, respectively. With a V_{dd} of 6V, the threshold for inverting behavior happens at V_{in}=3V with rail-to-rail logic performance (V_{high}=V_{dd} and V_{low} =0V), providing an excellent noise margin, as shown in Figure 1c. The inverter gain is larger than 30 (see Figure 1d), and the switching power is 120nW per cycle. This high performance logic inverter demonstrates the large promise of WSe_2 for the next generation of CMOS technology.



▲Figure 1: Schematic (left, top), optical image (left, bottom) and fabrication process (right) for WSe_2 CMOS FET technology.



▲Figure 2: Transfer characteristics of nMOS (a) and pMOS (b) WSe_2 FETs. (c) Output characteristics of CMOS logic inverter. (d) Inverter Gain and current during operation.

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- H. Wang, L. Yu, Y.-H. Lee, Y. Shi, A. Hsu, M. L. Chin, L.-J. Li, M. Dubey, J. Kong, and T. Palacios, "Integrated Circuits Based on Bilayer MoS2 Transistors," *Nano Lett.*, vol. 12, no. 9, pp. 4674–4680, Sep. 2012.

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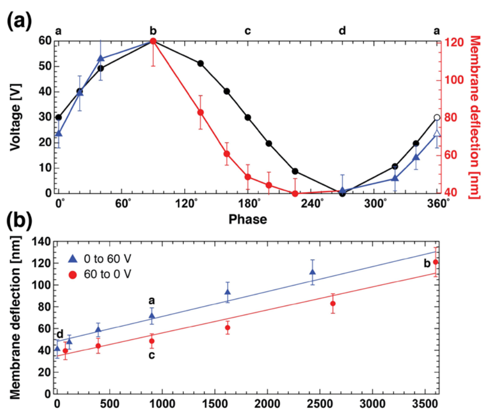
Printed MEMS Membrane Electrostatic Microspeakers

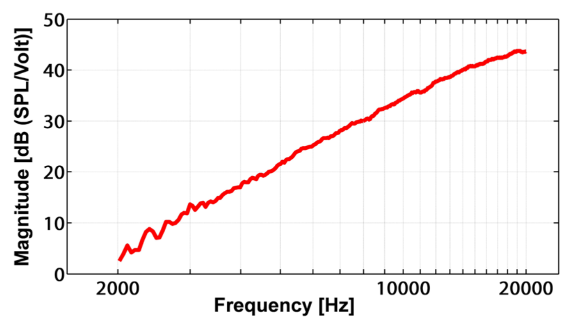
A. Murarka, J. Jean, A. Wang, J. Lang, V. Bulović
Sponsorship: NSF Center for Energy Efficient Electronics Science

This work reports the fabrication and operation of electrostatic microspeakers formed by contact-transfer of 125-nm-thick gold membranes over cavities patterned in a micron-thick silicon dioxide (SiO_2) layer on a conducting substrate. Upon electrostatic actuation, the membranes deflect and produce sound. Additionally, membrane deflection upon pneumatic actuation can be used to monitor pressure. The microspeaker fabrication process reported enables fabrication of MEMS diaphragms without wet or deep reactive-ion etching, thus obviating the need for etch-stops and wafer-bonding. This process enables monolithic fabrication of multiple completely-enclosed drum-like structures with non-perforated membranes to displace air efficiently, in both individual-transducer and phased-array geometries.

We characterized the mechanical deflection of the gold membranes using optical interferometry. The membranes show a repeatable peak center deflection of 121±13 nm across gaps of ~25 microns at 1 kHz sinusoidal actuation with 60 V peak-to-peak amplitude and a 30 V DC bias (Figure 1). The acoustic performance of the microspeakers is characterized in the free field. Microspeaker sound pressure level increases with frequency at 40 dB/decade (Figure 2), indicating that its sound pressure output is proportional to the acceleration of its diaphragm, as expected in the spring-controlled regime for free field radiation. The microspeaker consumes 262 µW of real electric power under broadband actuation in the free field, and outputs 34 dB(SPL/Volt) of acoustic pressure at 10 kHz drive. The silicon wafer substrate (~500 µm thick) dominates the total thickness of the microspeakers; the active device thickness is less than 2 µm. These thin microspeakers have potential applications in hearing aids, headphones, and large-area phased arrays for directional sound sources.



▲ Figure 1: Deflection profiles of gold membrane suspended over cavities, obtained via optical interferometry during 1 kHz AC actuation. Center deflections of this membrane over 83 cavities as functions of time were extracted from the profiles and averaged to yield a single deflection time function. That time function and corresponding applied voltage are plotted. (a) Applied voltage (black) and averaged peak membrane deflection (red and blue) are shown as functions of time. (b) Membrane deflections are plotted against square of applied voltage with time as a parameter. Points labeled a-b-c-d-a in (b) indicate position of corresponding points on the periodic deflection and voltage waveforms in (a).



▲ Figure 2: Acoustic frequency response, from 2 kHz to 20 kHz, of a gold membrane microspeaker, 12.5 mm^2 in area. Magnitude of transfer function, $|T_{pv}|$, from driving voltage amplitude to sound output measured by the microphone is converted to decibels using 20 µPa as reference pressure, i.e., magnitude plotted is $20\log_{10}(|T_{pv}|/20\mu Pa)$.

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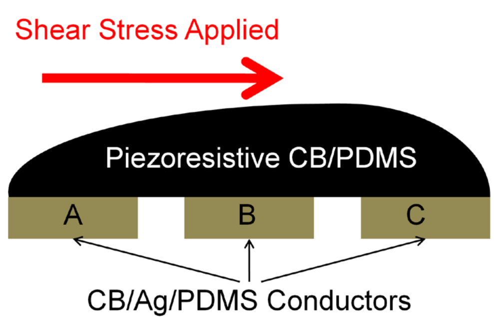
Stretchable Pressure and Shear Sensitive Skin

M. D'Asaro, V. Bulović, J.H. Lang
Sponsorship: NSF CSNE

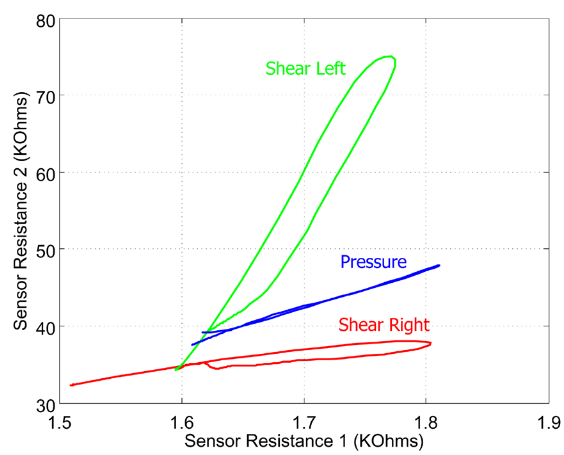
In the fields of robotics and prosthesis design, there is need for inexpensive, wide-area pressure- and shear-sensing arrays that can be integrated into a flexible and stretchable skin analog. This project seeks to meet this need by building combined pressure and shear sensors based on the well-documented piezoresistive (strain dependent resistance) property of composites made from polydimethylsiloxane (PDMS) and carbon black (CB).

The sensor skins are fabricated of three materials which are all PDMS-based: A CB/PDMS mixture is used as the active sensing material, a CB/PDMS and ~1 μm silver particle mixture is used to form strain-insensitive conductors into the skin, and pure PDMS is used to form the base of the skin. These materials are mixed, vacuum degassed, and then molded in custom-machined acytal and aluminum molds to fabricate the sensor arrays. Each sensor consists of a roughly hemispherical piece of CB/PDMS molded on top of a line of three conductors, thus allowing the resistance of each half of the CB/PDMS sensor to be measured independently. A schematic representation of a single sensor is shown in Figure 1.

Our own characterization experiments performed on bulk (1 cm^3) CB/PDMS samples have shown that the resistance of CB/PDMS increases under tensile, compressive, and shear strain but is much more sensitive to tensile strain then compressive strain. This symmetry allows the device to sense both pressure and shear. Under pressure, each half of the sensor has roughly equal compressive strain, and thus the resistance of each half of the device increases roughly equally. However, under shear, one half of the device is under tensile strain while the other half is under compressive strain. Due to the asymmetric response of the CB/PDMS, the resistance of the half of the sensor under tension increases much more than the half under compression, allowing a differentiation between pressure and shear; see Figure 2.



▲ Figure 1: Cut-away side-view of sensor under shear. Pure PDMS skin into which this sensor is embedded is not shown. The CB/PDMS between contacts A and B is under tension, causing large increase in resistance between them while CB/PDMS between contacts B and C is under compression, resulting in relatively little resistance chance between them.



▲ Figure 2: Plot of the resistance of one half of sensor vs. resistance of other half with time as a parametric variable. Note that when sheared, resistance in one half changes much more than the other but when put under pressure, both resistances change.

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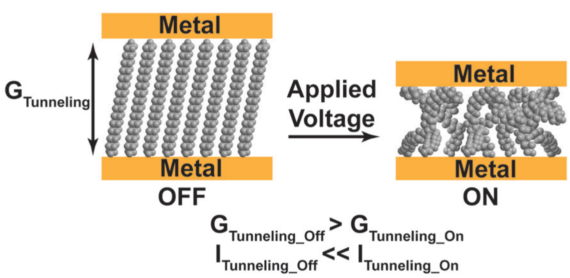
Tunneling Nanoelectromechanical Switches Based on Molecular Layers

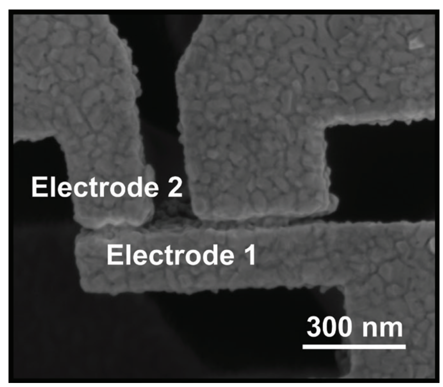
F. Niroui, E.M. Sletten, P.B. Deotare, A.I. Wang, T.M. Swager, J.H. Lang, V. Bulović
Sponsorship: NSF Center for Energy Efficient Electronics Science

Nanoelectromechanical (NEM) switches have emerged as a promising competing technology to the conventional complementary metal-oxide semiconductor (CMOS) transistors. NEM switches can exhibit abrupt switching behavior with large on-off current ratios and near-zero off-state leakage currents. However, they typically require large operating voltages exceeding 1 V and suffer from failure due to stiction. To address these challenges, this work presents NEM switches utilizing metal-molecule-metal switching gaps. These switches operate by electromechanical modulation of the tunneling current through electrostatically-induced compression of the molecular film (Figure 1). The molecular layer helps define few-nanometer-thick switching gaps to achieve low-voltage operation. In addition, the compressed molecules prevent direct contact between the electrodes while providing a restoring force to turn off the device once the applied voltage is removed, thereby preventing permanent adhesion between the electrodes and eliminating stiction.

A prototype two-terminal tunneling NEM switch is fabricated as a laterally actuated cantilever using electron beam-lithography (Figure 2). A fluorinated decanethiol layer is deposited over the device area and into the gap between Electrodes 1 and 2 using self-assembly through thiol-chemistry. During the assembly process, Electrode 1 collapses onto the opposing electrode to form a metal-molecule-metal junction with a nanometer thickness. Experimental results based on a device with a self-assembled fluorinated decanethiol layer demonstrate repeatable switching, indicating the importance of the molecular film in alleviating stiction. Comparison of these results to the theoretically expected device behavior suggests the compression of the molecular layer during the switching process, confirming the electromechanical modulation of tunneling current as the switching mechanism. Our current research focuses on engineering the molecular layer and the device design to optimize the NEM switch performance to achieve stiction-free sub-1-V actuation with more than 6 orders of magnitude on-off current ratio.



▲ Figure 1: Schematic representation of a tunneling NEM switch using a molecular thin-film. An applied voltage compresses the nanometer-thick organic layer to modulate the tunneling current by altering the tunneling gap between the metal contacts



▲ Figure 2: Scanning electron micrograph of a tunneling NEM switch fabricated using electron-beam lithography. A fluorinated decanethiol layer is self-assembled onto the Au electrodes including the gap between Electrodes 1 and 2, forming a nanoscale molecular switching gap.

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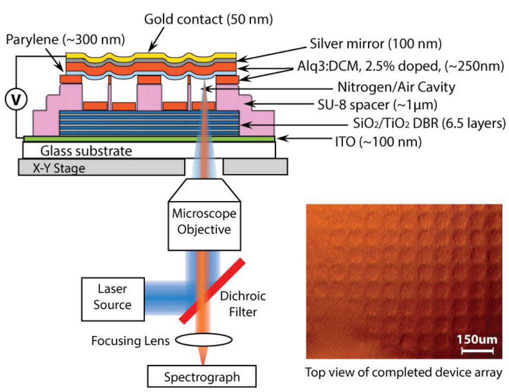
Electrically-Tunable Organic Microcavities

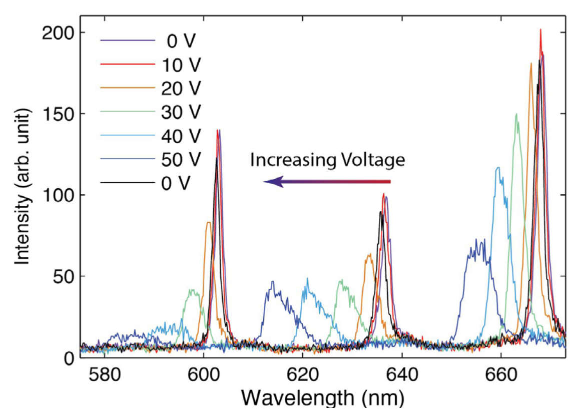
W. Chang, A. Wang, A. Murarka, J.H. Lang, V. Bulović
Sponsorship: NSF Center for Energy Efficient Electronics Science

The availability of a compact, single-system tunable visible light source would benefit a wide range of fields such as remote sensing, spectroscopy, and optical switches. Organic-based materials are attractive for visible light emission over a broad tunable spectrum. However, previously demonstrated frequency-tunable lasing devices required either complex fabrication techniques, external micro-actuated mirror stages, or manual switching between gain media. Tunable air-gap MEMS microcavity structures offer a scalable, integrated solution but their typical fabrication processes are incompatible with solvent- and temperature-sensitive organic gain materials.

We have demonstrated a method for fabricating integrated organic optical microcavities that can be mechanically or electrostatically actuated to dynamically tune their output emission spectra. Fabrication of the micro-opto-electro-mechanical system (MOEMS) structures (as in Figure 1) is enabled by a solvent-free additive transfer-printing method for composite membranes that we have developed. The suspended membrane incorporates an organic laser gain medium, Alq_3:DCM, into the microcavity, and the completed capacitive structure can be electrostatically actuated for dynamic tuning of the optical spectra (see Figure 2). Electrical actuation and optical characterization of a completed cavity structure show reversible resonance tuning greater than 20 nm for net membrane deflections of over 200 nm at 50 V. The device structure and transfer technique are easily scalable for large area fabrication with applications in tunable lasers as well as remote all-optical pressure sensing and low-power optical switches.



▲ Figure 1: Cross-sectional view of a MEMS tunable cavity device structure with a diagram of the optical testing setup. A microscope objective focuses laser excitation and captures cavity emission. Subsequent filter and lens focus emission into spectrograph. Inset: Fabricated device array from top view.



▲ Figure 2: Longitudinal mode emission spectra for a range of applied voltage. The 637-nm center mode shifts to 614 nm under 50 V actuation, indicating a deflection of the composite membrane of over 200 nm. The measurements were taken in order of increasing voltage. The final measurement at 0 V (indicated by black 0 V spectrum) shows that tuning is reversible.

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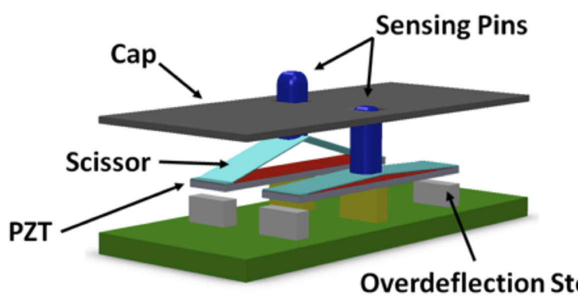
MEMS Tactile Displays

C. Livermore (NEU), S. Teller, L.F. Velásquez-García, X. Xie (NEU), Y. Zaitsev (NEU)
Sponsorship: Andrea Bocelli Foundation

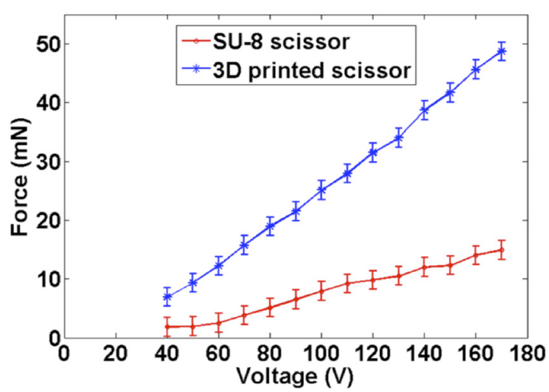
Providing information to people who are blind or have low vision is critical for enhancing their mobility and situational awareness. Although refreshable 2D graphical interfaces are preferred, it is challenging to create actuators that are compact enough to be arrayed into an unlimited number of rows and columns while still being robust, easy to sense, and rapidly switchable. Electroactive polymer actuators are small enough to be arrayed with a few- millimeter pitch and to provide quasistatic millimeter-scale actuations, but they typically have actuation times on the order of seconds. An alternative integrates piezoelectric bending beam actuators perpendicular to the tactile sensing plane, enabling large bending beam actuators to be tightly packed for fully 2D displays.

Ideally, the display's resolution should be about one tactel (i.e., tactile element) per mm^2, which is the density of mechanoreceptors in human finger pads. It should be refreshable in real time (hundreds of Hz, i.e., the frequency response of human touch), allowing the contents of the display to keep up with rapidly changing inputs. Since humans are much more sensitive to motions and changing stimuli than to static patterns, the display should code information not only as static patterns, but also as simulated motion against the user's finger pads. Finally, the power consumption of the display should be compatible with portable use. Although existing displays meet various subsets of these requirements, no existing display can meet all requirements simultaneously.

We are developing tactile displays based on a new type of MEMS tactile actuator created to target these requirements. This new actuator concept uses an extensional piezoelectric actuator that operates a scissor amplifier that transforms the in-plane movement of the piezo into amplified out-of-plane movement (see Figure 1). We have shown these tactile elements to be effective at the milliscale. Their measured performance agrees with the models, with maximum deflections of greater than 10 µm and maximum forces above 45 mN (as in Figure 2) that place the devices well above the sensing threshold. Our analytical model based on ideal pinned hinges is shown to be useful for predicting the behavior of tactels with flexural hinges, especially when coupled with FEA to predict hinge failure. The analytical model validation provides support for further downscaling of the tactile elements to achieve 100 tactels/cm^2. The measured performance confirms sensing thresholds of less than 4 µm and 2 mN for the most effective tactile devices.



▲ Figure 1: Schematic diagram of piezoelectric extension actuators (red) topped by scissor amplifiers (light blue) and cap plate.



▲ Figure 2: Measured tactel force vs. peak amplitude of the applied voltage. Markers represent data; lines guide the eye.

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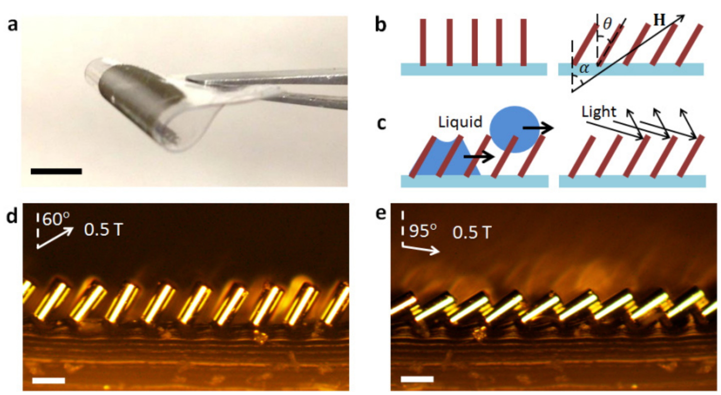
Real-time Manipulation with Magnetically Tunable Structures

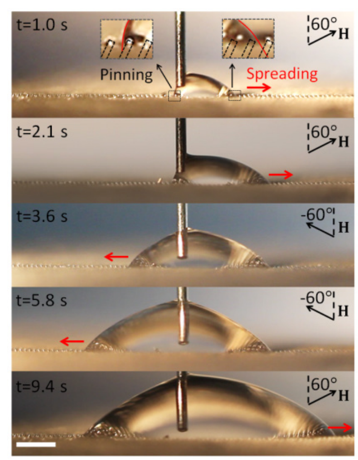
Y. Zhu, D.S. Antao, R. Xiao, E.N. Wang
Sponsorship: Air Force Office of Scientific Research

Responsive actuating surfaces have attracted significant attention as promising materials for liquid transport in microfluidics, cell manipulation in biological systems, and light tuning in optical applications via their dynamic regulation capability. Significant efforts have focused on fabricating static micro and nanostructured surfaces, even with asymmetric features to realize passive functionalities such as directional wettability and adhesion. Recent advances in utilizing materials that mechanically respond to thermal, chemical or magnetic stimuli have enabled dynamic regulation. However, the challenges with these surface designs are associated with the tuning range, accuracy, response time, and multi-functionality for advanced systems.

Here we report dynamically tunable micropillar arrays with uniform, reversible, continuous, and extreme tilt angles with precise control for real-time fluid and optical manipulation. Inspired by hair and motile cilia on animal skin and plant leaves for locomotion, liquid transportation, and thermal-optical regulation, our flexible uniform responsive microstructures (μFUR) consist of a passive thin elastic skin and active ferromagnetic microhair whose orientation is controlled by a magnetic field. We experimentally show uniform tilt angles ranging from 0° to 57° and developed a model to accurately capture the tilting behavior. Furthermore, we demonstrate that the μFUR can control and change liquid spreading direction on demand, manipulate fluid drag, and tune optical transmittance over a large range. The versatile surface developed in this work enables new opportunities for real-time fluid control, cell manipulation, drag reduction, and optical tuning in a variety of important engineering systems, including applications that require manipulation of both fluid and optical functions.



▲ Figure 1: a) Fabricated μFUR. Dark region is micropillar array; transparent substrate is PDMS skin. Scale bar is 5 mm. b) Schematic showing concept of μFUR; tilt angle can be controlled via external magnetic field. θ is micropillar tilt angle; α is magnetic field angle. c) Schematic of potential applications including microfluidic and optical manipulation. Side view of fabricated μFUR with applied magnetic field strength of 0.5 T and field angles of d) α=60° and e, α = 95° respectively. Scale bars are 50 μm.



▲ Figure 2: Time-lapse images of dynamic fluid spreading. Fluid (30% IPA and 70% water) spreading direction is dynamically controlled while the fluid propagates only in the pillar tilt direction (red arrow) and is pinned in all other directions. External magnetic field direction controls pillar tilt direction. Scale bar is 0.5 mm.

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GaN MEMS Resonator Using a Folded Phononic Crystal Structure

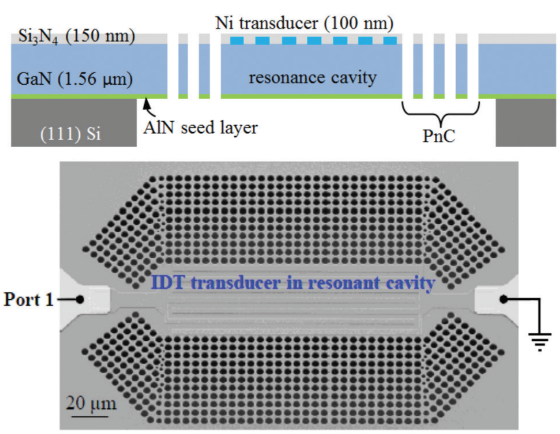
S. Wang, L.C. Popa, D. Weinstein
Sponsorship: DARPA DAHI Foundry, National Science Foundation CAREER Award, EECS

We present a gallium nitride (GaN) Lamb-wave resonator using a phononic crystal (PnC) to selectively confine elastic vibrations with wide-band spurious mode suppression. A unique feature of the design demonstrated here is a folded PnC structure to relax energy confinement in the non-resonant dimension and to enable routing access of piezoelectric transducers inside the resonant cavity. This feature provides a clean spectrum over a wide frequency range and improves series resistance relative to transmission line or tethered resonators by allowing a low-impedance path for drive and sense electrodes. We demonstrate GaN resonators with wide-band suppression of spurious modes, *f.Q* product up to 3.06×10^{12}, and resonator coupling coefficient k_{eff}^2 up to 0.23% (filter BW up to 0.46%). Furthermore, these PnC GaN resonators exhibit record-breaking power handling, with IIP3 of +27.2dBm demonstrated at 993MHz.

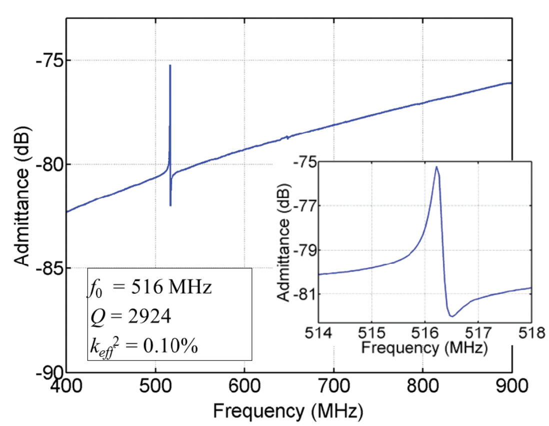
This work focuses on developing MEMS resonators for channel-select filtering in RF receiver front ends. For a MEMS band pass filter, the presence of spurious modes in the constituent resonators strongly impacts filter performance. Resonators with a clean frequency spectrum help reduce ripples in the pass-band and prevent interference from unwanted signals outside the pass-band. Conventional MEMS resonator designs with free mechanical boundaries are inherently prone to spurious modes, since free boundaries act as acoustic reflectors over all frequencies. To resolve this issue, the resonator boundary needs to be frequency selective. One way is by using PnCs, which involve periodic scatters to achieve highly reflective boundary conditions only for frequencies in a specific range. This acoustic band gap can be engineered based on the unit cell size and material configuration. While the acoustic band gap of these PnCs helps reduce resonance outside the band gap, these structures provide no spurious mode suppression inside the band gap. Further, transducers must be routed through the PnC in these configurations, leading to resistive loading of *Q*. In this work, we demonstrate a new resonant structure leveraging both PnC acoustic confinement and the electromechanical benefits of GaN. The proposed GaN folded PnC structure provides several important benefits:

- wide-band spurious mode suppression, both outside and inside the PnC band gap, through relaxed confinement in the non-resonant dimension,
- low-loss electrical routing to the resonant cavity,
- improved heat dissipation relative to other PnC or tethered resonators, and
- robust design that is immune to residual stress and handling.

The folded PnC design achieves these improvements while maintaining quality factor and transducer coupling comparable to traditional tethered resonators.



▲Figure 1: Material stack and SEM of the fabricated resonator. IDT transducers (Ni) are routed into the resonant cavity through openings. The resonator is connected through vias to probe pads, which are made of Au/Ti.



▲Figure 2: Measured frequency response of the resonator shown on the left with wide and narrow sweeps showing spurious-free spectrum.

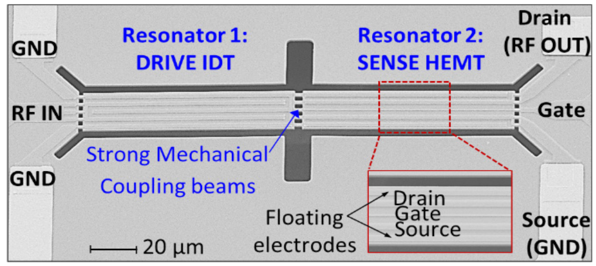
GaN RF MEMS Resonators in MMIC Technology

L.C. Popa, D. Weinstein
Sponsorship: Raytheon, DARPA DAHI, MIT/MTL GaN Energy Initiative

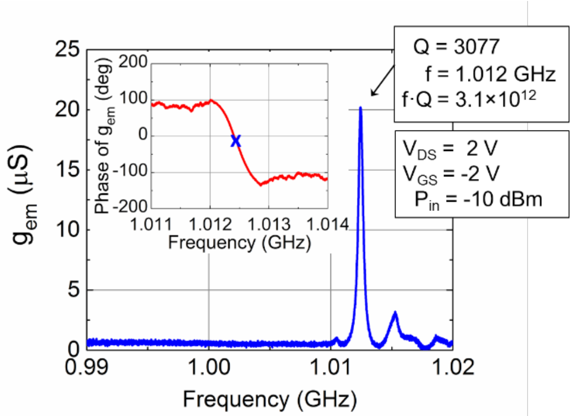
As a wide bandgap semiconductor with large breakdown fields and saturation velocities, gallium nitride (GaN) has been increasingly used in high-power, high-frequency electronics and monolithic microwave integrated circuits (MMICs). At the same time, GaN also has excellent electromechanical properties, such as high acoustic velocities and low acoustic losses. Together with a strong piezoelectric effect, these make GaN an ideal material for RF MEMS resonators. This work focuses on the optimization of L-band (1-2 GHz) GaN resonators in *standard* MMIC technology.

For monolithically integrated resonators, various constraints of the technology must be considered, such as the thickness of the GaN MMIC heterostructure, residual stresses in the GaN film, and the lack of bottom electrodes. Residual stress due to high temperature growth can affect the mechanical properties of the resonators and even lead to cracking and breaking. To achieve high performance resonators with multiple frequencies on the same chip within this technology, we designed 5th-order extensional resonators driven piezoelectrically with a top metal interdigitated transducer (IDT) as shown in Figure 1. These resonators have achieved mechanical quality factors >5500 at 1GHz, with f·Q products $>5.5\times10^{12}$, the highest demonstrated in GaN to date.

Enhanced signal-to-noise ratios (SNR)at high frequencies can be obtained by using active transistor sensing. We demonstrate the first mechanically-coupled Resonant Body Transistor, in which the drive transducer and sensing high electron mobility transistor (HEMT) are embedded in two separate cavities, as shown in Figure 1. This additional electrical isolation between drive and sense allows for an improvement in the SNR of >50× compared to previous designs. The large SNR, together with high Q (Figure 2), makes these resonators ideal for monolithically integrated low-phase noise oscillators, with applications in clocking and wireless communications.



▲ Figure 1: SEM of Mechanically Coupled Resonant Body Transistor. A top metal interdigitated transducer is used to launch acoustic waves. At resonance, strain fields modulate the HEMT's channel charge density, resulting in AC drain current.



▲ Figure 2: Experimental measurement of electromechanical transconductance, Y_{21}-Y_{12}. Inset shows clear phase transition at the resonant frequency.

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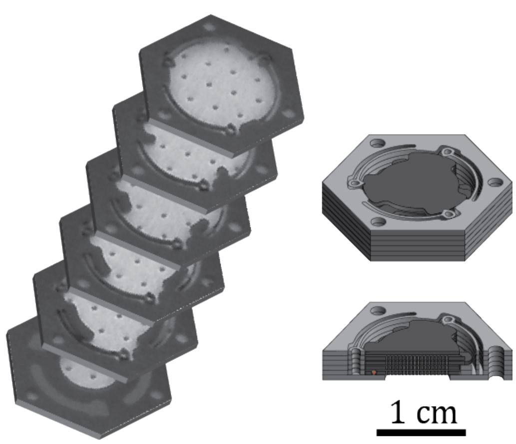
Ion Energy Measurements of Dense Plasmas with a Microfabricated RPA

E.V. Heubel, L.F. Velásquez-García
Sponsorship: NASA

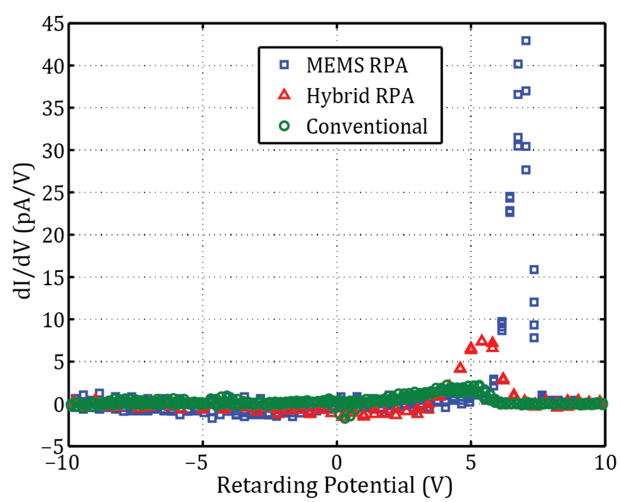
The energy of ions determines the efficiency of plasma propulsion systems and governs surface chemical reactions in plasma etching chambers. In plasma diagnostics, the instrument used to measure the ion energy distribution is the Retarding Potential Analyzer (RPA). However, high-density plasmas of interest require tens- to hundreds-of-microns scale dimensions. Through MEMS processing techniques, our RPA achieves the small aperture sizes necessary to measure dense plasmas. Precise alignment between successive microfabricated grids is achieved through compliant support structures in the housing (as Figure 1 shows). The silicon spring tips mate with corresponding notches in the electrodes to provide robust alignment on the order of 1 µm and to increase the overall sensor's ion transmission.

Our previously reported RPA, deemed "hybrid" on account of incorporating microfabricated electrodes in a conventionally machined sensor, demonstrated improved performance over conventional RPAs. By reducing the aperture size while enforcing some degree of aperture alignment, we achieved a better resolution with no loss in signal strength compared to conventional mesh RPAs. Measurements of the ion energy distribution in a helicon plasma were obtained at MIT's Plasma Science and Fusion Center using our sensors with microfabricated electrodes having 100 µm apertures. However, as a consequence of its larger apertures, the conventional RPA design was unable to effectively trap the plasma, and therefore no ion distribution could be extracted with this traditional device.

Figure 2 shows ion energy distributions obtained with an ion source comparing the performance of a conventional RPA (with 152 µm apertures), the hybrid RPA (with 100 µm apertures), and MEMS RPA (with 150 µm apertures). The MEMS RPA design utilizes a fully microfabricated housing to improve upon the inter-grid aperture alignment over the hybrid sensor. Additionally, various aperture diameters are utilized in the electrode stack to mitigate current interception within the sensor. These RPA improvements result in an order of magnitude increase in signal strength over the conventional device and a threefold increase in energy distribution resolution.



▲ Figure 1: MEMS RPA housing exploded view (left) of actual wafer layers. Concept and cross-section view of sensor with assembled electrodes (right).



▲ Figure 2: Ion energy distribution measurements of a mass spectrometry ion source. The MEMS RPA shows an order-of-magnitude increase in signal strength compared to a conventional RPA with similar aperture sizes, accompanied with a threefold reduction in peak width associated with increased sensor resolution.

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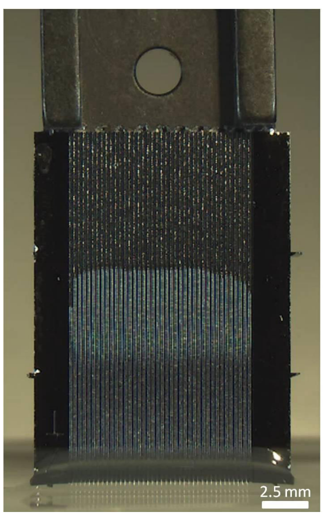
High Throughput Electrospinning of Nanofibers from Batch-microfabricated, Externally-fed Emitter Arrays

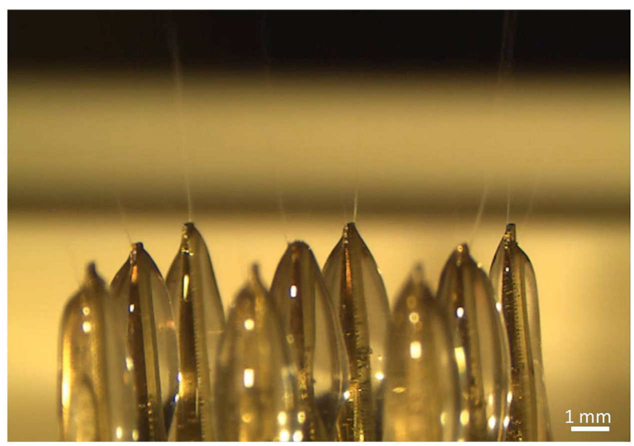
P.J. Ponce de Leon, F.A. Hill, L.F. Velásquez-García

Nanofibers promise to be a key engineering material in the near future due to their unique, nanoscale morphological properties. In particular, the large specific surface area of the porous webs they form make them highly desirable as scaffolds for tissue engineering; layers in multifunctional filters/membranes; and components in devices such as fuel cells, solar cells, and ultra-capacitors. However, their integration into almost all of these technologies is unfeasible as a result of the low throughput, high cost, and poor control of current production methods. The most common process for producing nanofibers involves applying strong electric fields to polar, high-molecular-weight polymeric liquids pumped through a syringe in what is known as electrospinning. Electrospinning is the only known technique that can generate nanofibers of arbitrary length; it has tremendous versatility as it can create non-woven or aligned mats of polymer, ceramic, semiconducting, and/or metallic fibers.

We implement high throughput arrays of externally-fed, batch-microfabricated electrospinning emitters that are precise, simple, and scalable. We fabricate monolithic, linear emitter arrays that consist of pointed structures etched out of silicon using DRIE and assemble these into a slotted base to form a two-dimensional array. By altering the surface chemistry and roughness of the emitters, we can modify their wetting properties to enable wicking of fluid through the micro-texture (as in Figure 1). The interplay between electric, viscoelastic, and surface tension forces governs the fluid transport and fiber formation. We achieve over 30 seconds of stable electrospinning of polyethylene oxide (2-4% w/v in 60/40 water/ethanol solution) from 9 emitters in a two-dimensional array with a density of 11 emitters/cm^2 using bias voltages around 10kV (see Figure 2). This density is 7 times greater than the emitter density achieved in similar array-based approaches. Current work focuses on characterization of larger, denser arrays to demonstrate uniform emission.



▲ Figure 1: Capillary rise against gravity of a 2% w/v polyethylene oxide (PEO) solution through microtrenches. Sufficient liquid supply is necessary for continuous electrospinning.



▲ Figure 2: Stable production of PEO nanofibers from a 3×3 array of 6-mm tall micropillar-patterned emitters.

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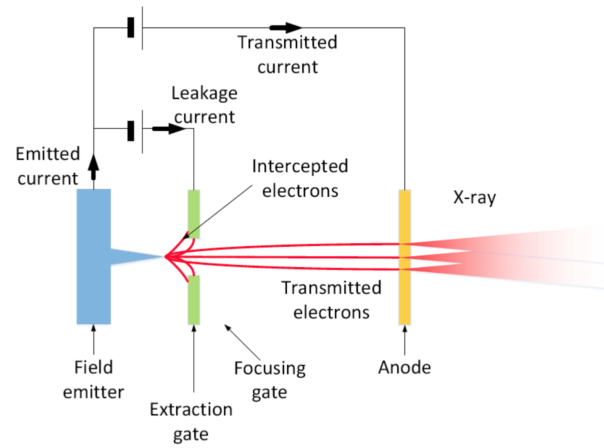
Near-Monochromatic X-ray Sources Using a Nanostructured Field Emission Cathode and a Transmission Anode for Markerless Soft Tissue Imaging

S. Cheng, F.A. Hill, E.V. Heubel, R. Gupta (MGH), L.F. Velásquez-García
Sponsorship: DARPA

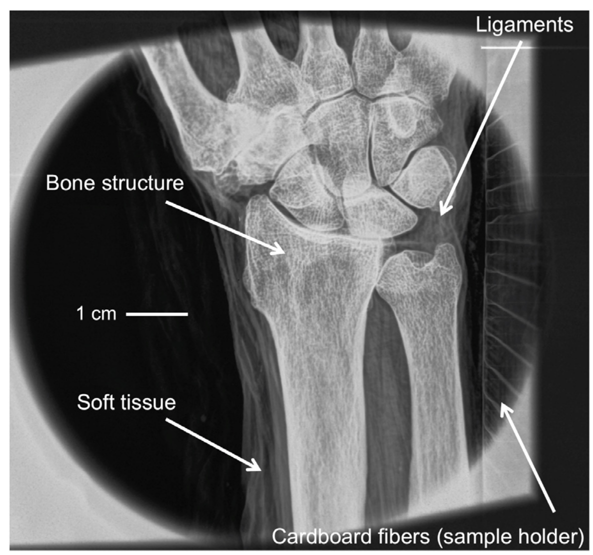
A conventional X-ray generator consists of a thermionic cathode and a reflection anode inside of a vacuum chamber that has an X-ray transmission window. The cathode generates a beam of electrons that is accelerated towards the anode, which is biased at tens of kilovolts above the cathode voltage. Some of the electrons collide with the anode and convert their kinetic energy into radiation, a fraction of which escapes the vacuum chamber through a transmission window made of a suitable material, such as beryllium. The X-ray emission is a mix of bremsstrahlung radiation (broad, continuous spectrum) and fluorescence (emission at specific peaks corresponding to atomic shell transitions). Conventional X-ray technology requires high vacuum to operate, does not efficiently produce X-rays, and has overall low power efficiency. Conventional X-ray generators cannot image well soft tissue unless contrast media, i.e., markers, are employed.

We are developing efficient X-ray generators capable of soft tissue imaging using batch-microfabricated field emission cathodes composed of arrays of self-aligned, gated, and nanometer-sharp n-silicon tips, and a microstructured transmission anode (Figure 1). The nanostructured silicon cathode operates at low voltage and reliably achieves high-current emission with high transmission. The transmission anode efficiently generates X-rays while reducing the background radiation, resulting in emission of X-rays with narrow spectral linewidth for sharp imaging of biological tissue.

Using our first-generation X-ray source (a tabletop apparatus), we have obtained absorption images of ex-vivo samples that clearly show soft tissue and fine bone structures (Figure 2). Current work focuses in miniaturizing the X-ray source into a portable system, and in improving the cathode and anode components to achieve generation of coherent X-rays to make possible phase contrast imaging at a low cost.



▲ Figure 1: Schematic of an X-ray generator with a field emission cathode and a transmission anode.



▲ Figure 2: Absorption X-ray image of an ex-vivo human wrist showing soft tissue structures and fine details of the bone structure.

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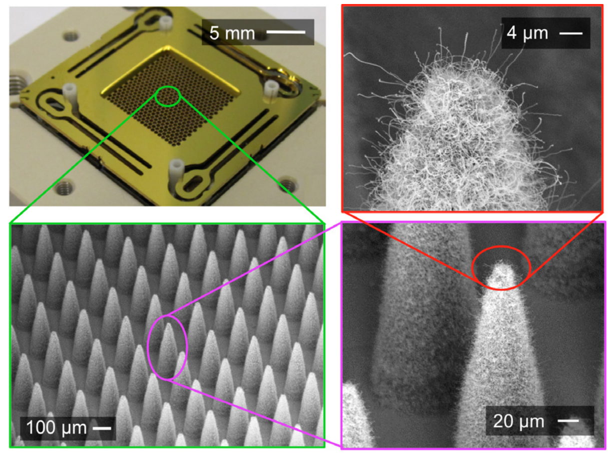
Multiplexed MEMS Electrospray Emitter Arrays with Integrated Extractor Grid and CNT Flow Control Structures for High-Throughput Generation of Ions

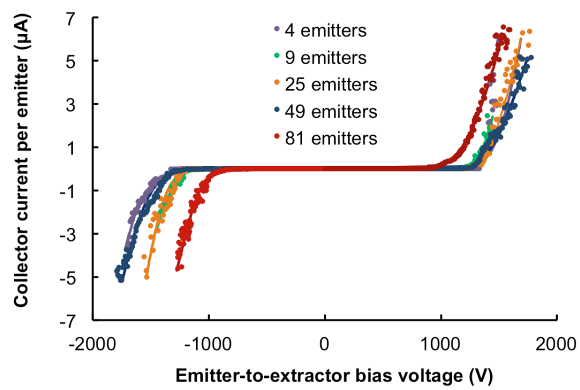
F.A. Hill, E.V. Heubel, P. Ponce de Leon, L.F. Velásquez-García
Sponsorship: DARPA

Electrospray is a process to ionize electrically conductive liquids that relies on strong electric fields. Charged particles are emitted from sharp tips that serve as field enhancers to increase the electrostatic pressure on the surface of the liquid, overcome the effects of surface tension, and facilitate the localization of emission sites. Ions can be emitted from the liquid surface if the liquid is highly conductive and the emitter flowrate is low. Previous research has demonstrated successful operation of massive arrays of monolithic batch-microfabricated planar electrospray arrays with an integrated extractor electrode using ionic liquids EMI-BF_4 and EMI-Im—liquids of great importance for efficient nanosatellite propulsion and nanomanufacturing. The current design builds upon a previous electrospray array designs from our group by increasing the area density of the emitter tips and increasing the output current by custom-engineering nanofluidic structures for flow control.

Our MEMS multiplexed electrospray source consists of an emitter die and an extractor grid die (Figure 1), both made of silicon and fabricated using deep reactive ion etching. The two dies are held together using a MEMS high-voltage packaging technology based on microfabricated springs that allows precision packaging of the two components with low beam interception. The emitter die contains dense arrays of sharp emitter tips with over 1,900 emitters in 1 cm². A voltage applied between the emitter die and the extractor grid die creates the electric field necessary to ionize the ionic liquid. A carbon nanotube forest grown on the surface of the emitters transports the liquid from the base of the emitters to the emitter tips. Our electrospray arrays operate uniformly (Figure 2), and mass spectrometry of the emission demonstrates that our devices only produce ions.



▲ Figure 1: (in counter-clockwise starting on the upper left corner) array of 2,000 electrospray emitters in 1 cm² with integrated extractor grid; close-up of electrospray emitter forest; close-up of a single electrospray emitter covered by a layer of CNTs; detail of an emitter tip.



▲ Figure 2: Collector current per emitter as a function of emitter-to-extractor bias voltage for (A) the electrospray sources with 4, 9, 25, 49 and 81 emitters in 1 cm² evidencing great array uniformity.

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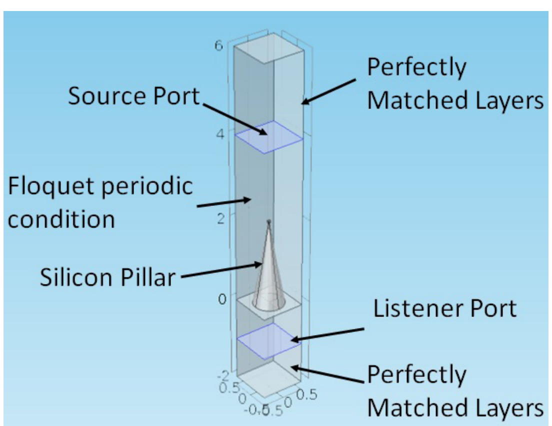
Exploration of the Packing Limits of Ultrafast, Optically-triggered Silicon Field-emitter Arrays Using the Finite Element Method

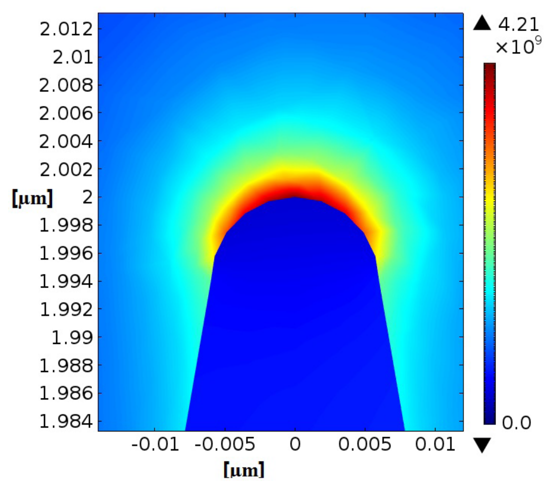
C. Dong, M.E. Swanwick, P.D. Keathley, F.X. Kärtner, L.F. Velásquez-García
Sponsorship: DARPA

Ultrafast optically-triggered field emission cathodes bypass several disadvantages demonstrated by current state-of-the-art ultrafast cathodes, such as requiring ultra-high vacuum to operate and short lifetime, and are a promising technology for implementing spatially-structured electron sources for applications such as free-electron lasers, compact coherent X-ray sources, and attosecond imaging. Ultrafast optically-triggered cathodes composed of massive arrays of high aspect-ratio silicon pillars capped by nano sharp tips and 5 µm pitch were fabricated at MIT MTL. The effect of the geometry and the morphology of the Si pillar arrays on the ultra-fast emission characteristics of such cathodes is now explored using the finite element modeling in 2D and 3D.

Since the field-emitted current depends exponentially on the surface electric field, we are interested in studying how the electric field is enhanced by the geometry and the morphology of the Si pillar arrays. We selected COMSOL Multiphysics to simulate the electric field of the devices. The 3D model (see Figure 1) consists of a single tapered pillar 2.0 µm tall and 0.7 µm wide at the base with a 6-nm radius hemispherical cap. Perfectly matched layers (PMLs) are added on the top and bottom to absorb the excited and higher order modes. Floquet periodicity is applied on the four sides of the unit cell to simulate the infinite 2D array. The port boundary condition is applied on the interior boundary of the PML as the excitation port to simulate the 800-nm incident wave at a glancing angle of 84° from normal (the same experimental setup described in the third reading below). This model is validated by verifying the Fresnel equations between Si and vacuum before inserting the Si pillar. The 2D slice contour plot (see Figure 2) shows the simulated electric field from a 1 GV/m incident field on an emitter with 1-µm pitch using frequency domain analysis. The maximum electric field at the tip is about 4.2 GV/m, i.e., the emitter tip has an field enhancement factor of ~4.2. Both 2D and 3D models are utilized to explore the effect of the geometry and the morphology of the Si pillar arrays on the field enhancement.



▲ Figure 1: The 3D COMSOL model consists of a single pillar, PMLs on the top and bottom, Floquet periodicity on four sides, and a source port with an incident 800-nm wave at a glancing angle of 84°.



▲ Figure 2: 2D slice contour plot from the 3D model with 1-µm pitch shows the maximum electric field at the tip, with a field enhancement factor of ~4.2.

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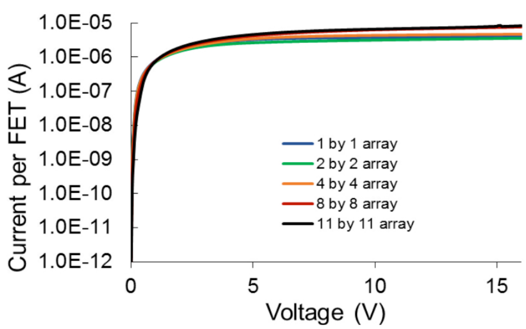
High-Current Field Emission Cold Cathodes with Temporal and Spatial Emission Uniformity

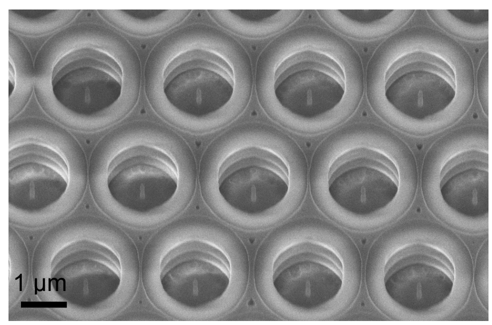
M.E. Swanwick, F.A. Hill, L.F. Velásquez-García
Sponsorship: DARPA

Field emission arrays (FEAs) are an attractive alternative to mainstream thermionic cathodes, which require high vacuum and high temperature to operate. Field emission of electrons consists of the following two processes: first, the transmission of electrons (tunneling) through the potential barrier that holds electrons within the material (workfunction ϕ) when the barrier is deformed by a high electrostatic field and second, the supply of electrons from the bulk of the material to the emitting surface. Either the transmission process or the supply process could be the limiting step that determines the emission current of the field emitter. Due to the exponential dependence on the field factor, the emission current from the tips is extremely sensitive to tip radii variation. We have a process to achieve uniform emission from nanosharp FEAs by both fabricating highly uniform tip arrays and controlling the supply of electrons to the emitting surface (see Figure 1).

We have designed and fabricated FEAs in which each field emitter is individually ballasted using a vertical ungated field effect transistor (FET) made from a high aspect ratio (40:1) n-type silicon pillar. Each emitter has a proximal extractor gate that is self-aligned for maximum electron transmission to the anode (collector). Our modeling suggests that these cathodes can emit as much as 30 $A.cm^{-2}$ uniformly with no degradation of the emitters due to Joule heating; also, these cathodes can be switched at microsecond-level speeds. The design process flow, mask set, and pillar arrays have been completed (as Figure 2 shows) with the self-aligned extractor gate. An ultra-high vacuum chamber has been built to test the devices. The chamber can test full 150mm wafers with six high voltage feed through and a step-down anode at 2×10^{-10} torr pressure while also imaging the electron emission on a phosphorus screen.



▲ Figure 1: IV curves for high aspect ratio Si (1-2 Ω.cm) pillars showing current saturation for 1, 4, 16, 64, and 121 pillars. Each pillar is 25 µm tall, 500 nm in diameter, and capped with Al for ohmic contact.



▲ Figure 2: SEM image of a large array of high aspect ratio pillars with 10-nm radius tips with 5-µm hexagonal packing for individually ballasted field emission with self-aligned gates.

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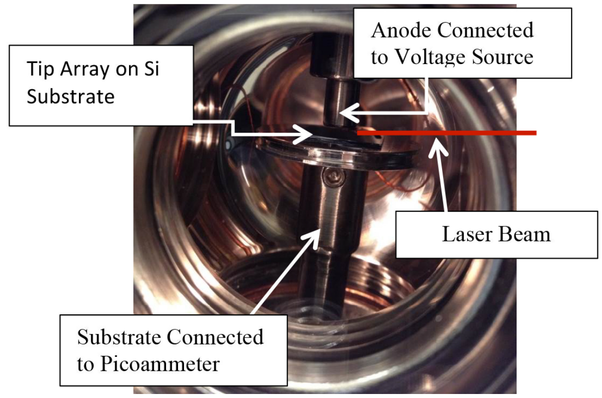
Photoactuated Ultrafast Silicon Nanostructured Electron Sources for Coherent X-ray Generation

M.E. Swanwick, P.D. Keathley, C.D. Dong, F.X. Kärtner, L.F. Velásquez-García
Sponsorship: DARPA

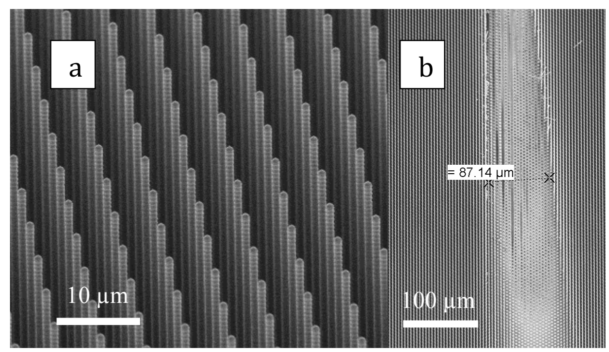
Nanostructured cathodes that can be switched at an ultrafast time scale (<50 ps) have applications in free-electron lasers and coherent X-ray sources. This project is creating the theory, modeling, and experimental results for a compact coherent xray source for phase contrast medical imaging based on inverse Compton scattering of relativistic electron bunches. The X-ray system requires a low-emittance electron source that can be switched at timescales in the low femtosecond range.

The focus of our work has been the design, fabrication, and characterization of massive arrays of a nanostructured high aspect-ratio silicon structures to implement low-emittance and high-brightness cathodes that are triggered using ultrafast laser pulses to produce spatially uniform electron bunches. Laser pulses at 35 fs, 800 nm and a 3 kHz repetition rate from a titanium sapphire laser at an 84° glancing angle, inside a vacuum chamber at ~10^{-8} torr bathe a highly uniform array of ~2200 silicon pillars with a 5-µm pitch. The cathode chip is connected to ground through a picoammeter while the anode, a 0.25-inch plate 3mm above the cathode, connects to a voltage supply (see Figure 1). The cathodes show stable emission and emit over 1.2 pC average charge for over 8-million pulses when excited with 9.5-µJ laser energy with no degradation of the emission characteristic of the cathode. This result shows that silicon-based photon-triggered cathodes processed with standard CMOS processes and operated at high vacuum can function for extended periods without performance degradation.

The cathodes are fabricated from single-crystal <100> n-Si 1-10 Ω-cm wafers. The result is massive arrays of pillars (over half a million elements with 5-µm hexagonal packing) capped by tips with under-5-nm average tip radius and less than 1-nm standard deviation (see Figure 2). Through simulation and experiment we have demonstrated that the emitters operate in two distinctive regimens, i.e., the low-electric field multi-photon regime (similar to a typical photocathode), and the high-field quantum tunneling regime (similar to a field emission cathode). Actuation of the devices with laser pulses of 10 µJ or lower results in electron emission with no device degradation.



▲Figure 1: Experimental set-up with an 800-nm 35-fs laser beam with 80-µm spot size hitting the cathode at 84°.



▲Figure 2: (a) SEM of high aspect-ratio single-crystal Si pillars with uniform nanosharp tips. (b) Damage to Si tips after exposed to 20.5-µJ laser pulses.

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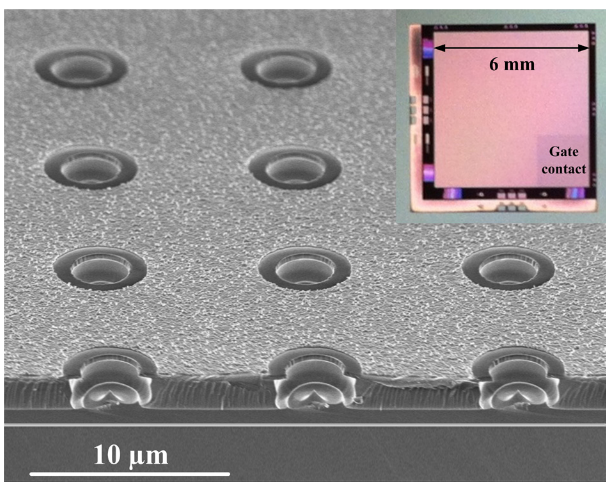
Field Emission Neutralizers for Electric Propulsion of Small Spacecraft in Low Earth Orbit

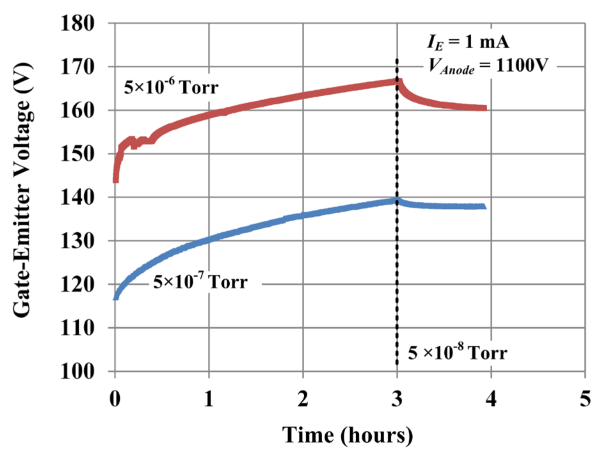
A.A. Fomani, A.I. Akinwande, L.F. Velásquez-García
Sponsorship: DARPA

Electric propulsion (EP) systems are excellent candidates for small spacecraft since EP systems consume less propellant than chemical rockets. In EP systems such as field emission electric propulsion thrusters (FEEPs), ion engines, and hall thrusters, a beam of positive ions is ejected at high speed to produce thrust. If the ejecting charge is not compensated, the operation of the EP system will negatively charge the spacecraft, reducing the propulsion efficiency and eventually stopping the thruster. Hence, development of robust, low-power, and high-current neutralizers that do not consume propellant is necessary to advance the state of the art of EP systems for small spacecraft. Field emission neutralizers (FENs) are promising candidates because of their low power consumption, high specific current, small size, and lack of propellant consumption. For operation in LEO, neutralizers must withstand long-term operation in environments with oxygen partial pressures of ~5×10^{-7} Torr. Carbon nanotube-based FENs could satisfy these requirements; however, they require biases higher than 600 V for 1 mA emission current.

This work develops arrays of Pt-coated, self-aligned, gated tips as low-voltage FENs for electric propulsion of small spacecraft in low Earth orbit. The neutralizers consist of 320,000 tips with 10 µm pitch and 5-10 nm tip radii; they have an integrated self-aligned gate electrode with 3 µm apertures. The devices emit currents higher than 1 mA at bias voltages as low as 120 V, i.e., similar currents at five-fold less bias voltage and emission area than state-of-the-art CNT neutralizers. The devices have a 2.5-µm-thick gate dielectric to prevent device failure due to dielectric breakdown; the tips are coated with a 10-nm-thick Pt film to improve the tip resistance against ion bombardment and reactive gasses. Continuous emission for 3 hours at pressures of 5×10^{-6} Torr in air was demonstrated. Less than 60 V increase in the gate-emitter voltage was sufficient to maintain the emission current at 1 mA.



▲ Figure 1: SEM image of Pt-coated self-aligned gated Si tips. The inset shows optical image of a field emitter neutralizer with 0.32 cm^2 active area consisting of 320,000 gated nanometer-scale tips.



▲ Figure 2: . Continuous field emission at 5×10^{-6} and 5×10^{-7} Torr in air. Less than 60 V increase in the gate-emitter voltage was sufficient to maintain the current at 1 mA.

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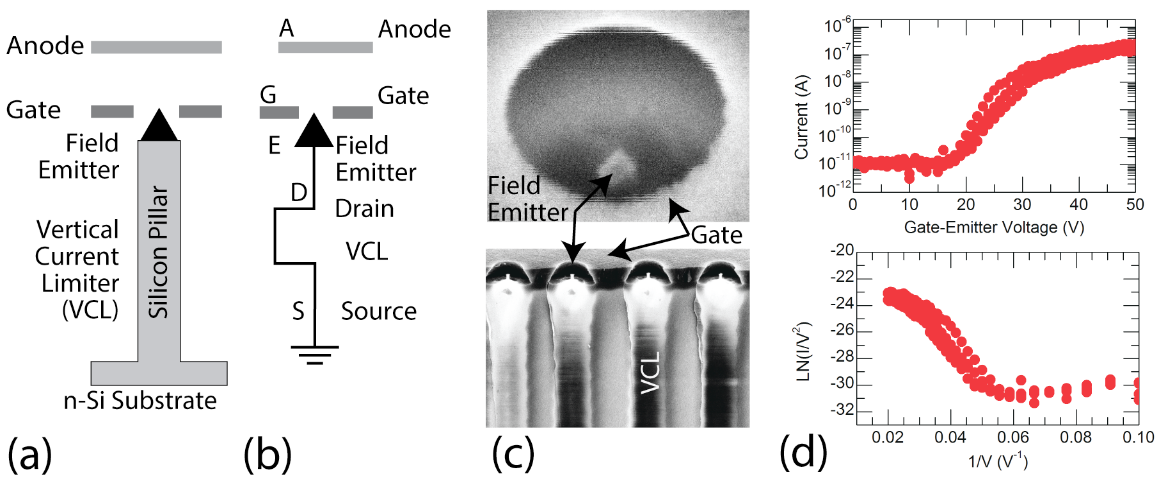
Field Emission Arrays with Integrated Vertical Current Limiters and Self-aligned Gate Apertures

S.A. Guerrera, A.I. Akinwande
Sponsorship: DARPA

Field emission cold cathodes are some of the brightest electron sources ever reported, making them an ideal source in a variety of applications, including microscopy, lithography, imaging, and the generation of terahertz and X-ray radiation. Field emission arrays (FEAs) suffer from emitter tip radius variation across the array and sensitivity to the state of the emitting surface, resulting in spatial and temporal variations of emission current. To address these issues, we previously demonstrated that a high-aspect-ratio silicon vertical current limiter (VCL) that is connected in series with each field emitter in a field emission array could regulate the supply of electrons to each emitter and result in uniform emission; however, due to the lack of an integrated extractor gate, these devices operate at high extraction voltages and 99% of the total emitted current is intercepted by the extraction gate. Large extraction gate voltages are required due to the low field factor, β (cm^{-1}), and result in a high Fowler-Nordheim (FN) slope b_{FN} (V), arising from the large extractor gate–tip distance.

To reduce the extractor voltage and enable low-voltage operation, we report Si FEAs with 1 million individual field emitters that have a 1-micron pitch with integrated VCLs poly-silicon extractor gates. These VCLs are Si pillars that have diameter less than 100 nm and are 10 microns tall, with tip radius under 20 nm. A schematic diagram and circuit diagram are shown in Figure 1 (a),(b). To fill in the gaps between the pillars and to support the self-aligned gate, a novel gap-filling process consisting of silicon dioxide and silicon-rich nitride deposition and chemical-mechanical planarization was employed, resulting in the structure shown in Figure 1 (c). The diameter of the extractor gate aperture is under 200 nm. As shown in Figure 1(d), these devices exhibit turn-on voltages less than 20 V and saturation currents of approximately 1 pA / emitter.



▲ Figure 1: (a) Schematic diagram of a Si field emitter with Si VCL. (b) Circuit diagram of the structure. The VCL behaves as an ungated FET. (c) SEM image of a tilted (top) and cross-section view of the completed structure. (d) I-V characteristics (top) and Fowler-Nordheim characteristics of the completed device. The FEA turns on at <20 V and demonstrates current saturation at <30 V.

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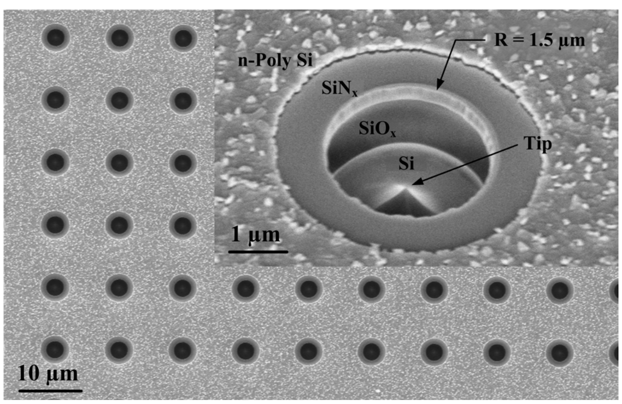
Low-Voltage High-Pressure Gas Field Ionizers

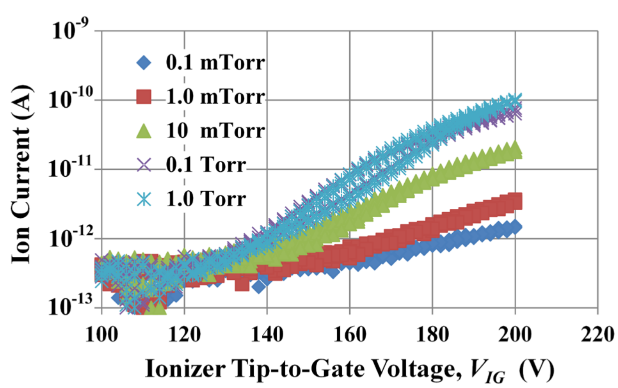
A.A. Fomani, L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

Low power consumption, soft-ionization capability, and the potential for operation at high pressures are characteristics desired in gas ionizers for application to portable analytical instruments. Unlike impact ionization techniques, field ionization provides an efficient method for producing stable molecular ions—even from complex organic compounds. Consequently, field ion sources can generate nonfragmented ions for exact measurement of the mass-to-charge ratio of an analyte. These devices are used in various analytical instruments such as field ion mass spectrometers (FIMS) and atom beam microscopes. Other applications include gas chromatography FIMS for analysis of petroleum products and neutron generators for detection of shielded nuclear material and oil-well logging. Despite the attractive features offered by field ion sources, long-term, reliable, and high pressure operation has not been reported due to high voltages (> 500 V) needed for field ionization using the current state-of-the-art devices.

We have developed low-voltage Torr-level gas field ionizers with operating voltages as low as 150 V even for He, which has the highest ionization potential among molecules. The ionizer consists of a large array of Pt-coated self-aligned gated Si tips with radii <10 nm and gate apertures of 3 µm. The tips were designed to generate fields above 20 V/nm at gate-to-tip voltages lower than 200 V while the field at the edge of the gate remains below 0.2 V/nm. A 2.5-µm-thick stack of silicon oxide/silicon nitride was employed as the gate dielectric to limit the field intensity inside the gate dielectric to less than 100 V/µm, allowing prolonged operation of the device. Continuous field ionization of He and N_2 for 10^4 s was achieved at pressures as high as 10 Torr. A slow decay in ion current was observed over time, which can be explained by adsorption of particles at the tip surface. Nevertheless, the original device characteristics can be recovered by operating the device as field emitter in a high vacuum (<10^{-7} Torr).



▲ Figure 1: SEM images of the fabricated gated tip arrays employed as gas field ionizers.



▲ Figure 2: Field ionization of helium—ion current vs. tip-to-gate voltage at different pressures.

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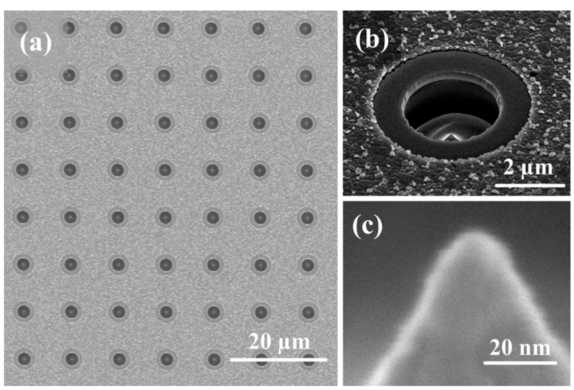
Large-Area Field Emission Arrays for High-Current Applications

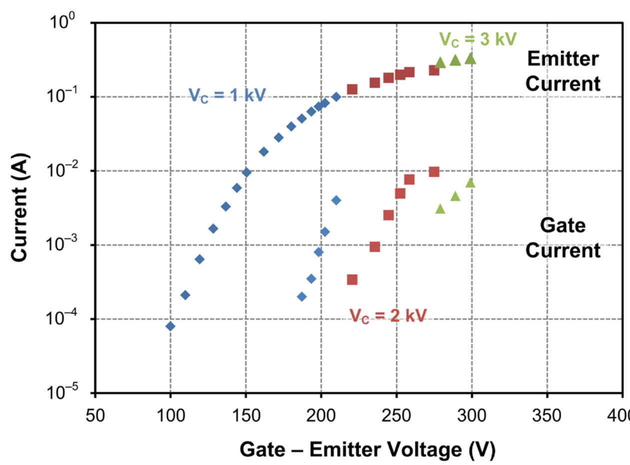
A.A. Fomani, L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

Gyrotrons, free electron lasers (FELs), and THz vacuum electronic devices require intense high-current electron beams. High-current, high-current-density electron beams are also needed for X-ray generation, pumping of gaseous lasers, and surface treatment of materials. Field emission sources show great promise for these applications as they can produce current densities higher than 10 A/cm² at voltages below 100 V. Despite these promising attributes, the state-of-the art devices have produced currents less than 300 mA due to limitated array size (1–10 mm²) because of fabrication issues that result in failure or severe sub-utilization of the array. The major challenges include low yield of fabrication, large variation in gate and tip dimensions across the array, and point defects in the gate dielectric.

We have developed a high-yield process for fabrication of large-area, self-aligned, gated tip arrays with low sensitivity to processing conditions. The fabricated field emission arrays (FEAs) demonstrate average field factor >10⁶ cm⁻¹ using nanometer-scale tips (radii < 10 nm) surrounded by individual gates with 1.5 μm radius of aperture. This ensures low-voltage operation of the device and a turn-on voltage below 50 V. For reliability a thin Pt layer was deposited over the FEA and a SiO_x/SiN_x dielectric stack thicker than 2.5 μm was used as the gate insulator. The Pt coating ensures chemical resistivity of the tips against corrosive gasses/ions, and the thick insulator stack limits the field inside the gate dielectric to < 150 V/μm at Gate-Emitter voltages of < 300 V. Our FEAs consisting of 320,000 tips in 0.32 cm² are capable of emitting currents as high as 350 mA at densities of ~1.1 A/cm². The device operation at higher emission currents was prevented due to plasma ignition because of the excessive outgassing of the anode. At low pressures, long-term (~3 hrs) operation not only was possible but also lowered emission voltage and gate current.



▲ Figure 1: SEM images of a fabricated array showing angle-view, cross-section and close-up images of a gated tip, confirming the self-aligned structure of the device and tip radius of less than 10 nm.



▲ Figure 2: Field emission characteristics of an FEA consists of 320,000 Pt-coated and gated tips with radii below 10 nm. Currents as high as 350 mA were emitted at gate-emitter voltage of 300 V.

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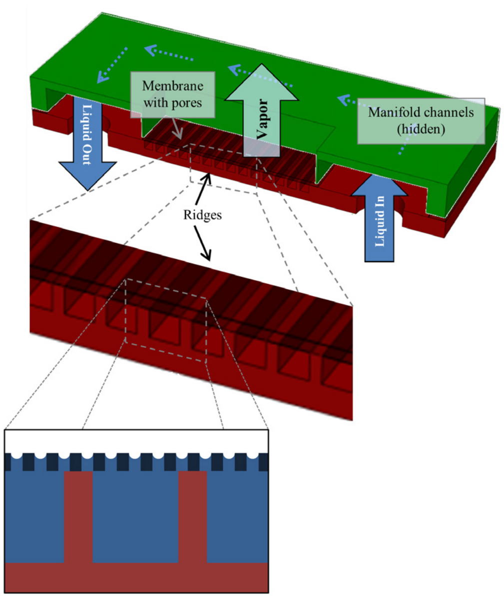
Evaporation through Nanoporous Membranes for High Heat Flux

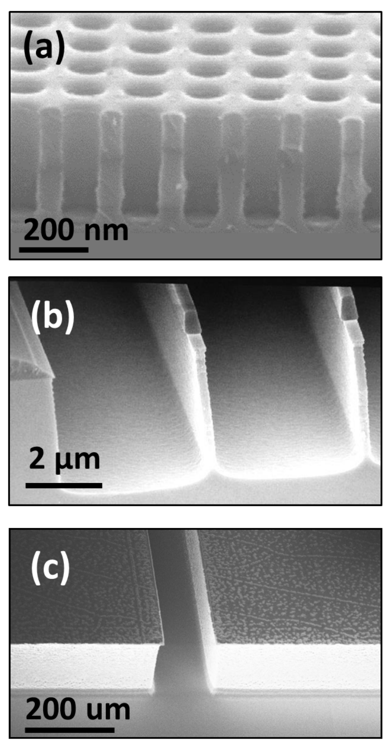
D. Hanks, J. Sircar, Z. Lu, S. Narayanan, D. Antao, B. Barabadi, R. Xiao, R. Raj, R. Enright, E.N. Wang
Sponsorship: Avram Bar-Cohen, DARPA MTO

The development of ever more compact electronic circuits has brought the demands for thermal management to unprecedented levels. Although there has been extensive research on single phase and multi-phase cooling in microchannels, evaporative cooling in the thin film regime has the potential to reach an even higher heat flux. We report the design and fabrication of a novel silicon-based evaporation device for direct integration into high power density electronics.

We designed a micro-scale device, relying on the evaporation of a very thin liquid film to dissipate over 1000 W/cm^2 with an overall temperature difference of less than 30 K. Evaporation occurs in a 200 nm thick silicon membrane patterned with 100 nm pores using interference lithography. The nanopores create a large thin-film evaporation area and generate a large capillary pumping pressure to supply fluid to the membrane. The membrane is thermally bonded to an arrayed supply network of 4 µm x 4 µm microchannels whose walls provide mechanical support and a thermal conduction pathway from the substrate. The substrate is resistively heated, and the temperature is measured with RTDs fabricated with a lift-off pattern. A finite element model is developed to optimize the microchannel and membrane geometry. The convective heat transfer coefficient is modeled by numerically solving governing equations of heat, mass, and momentum conservation at the pore level. Evaporation through nanoporous membranes has the potential for achieving ultra-high heat flux dissipation (5 kW/cm^2) for high-performance electronic devices.



▲ Figure 1: Schematic of supported membrane evaporation device. Liquid from manifold is drawn through ridge channels to surface of membrane pores, where evaporation occurs (not to scale). Membrane and manifold are fabricated using SOI wafer, which is then bonded to a wafer with etched ridge structures.



◀ Figure 2: (a) SEM image of pores etched with interference lithography pattern into silicon. (b) SEM image of etched ridge structures. Dark material on top is photoresist used to define etch. (c) SEM image of liquid manifold channels etched through membrane and BOX into handle.

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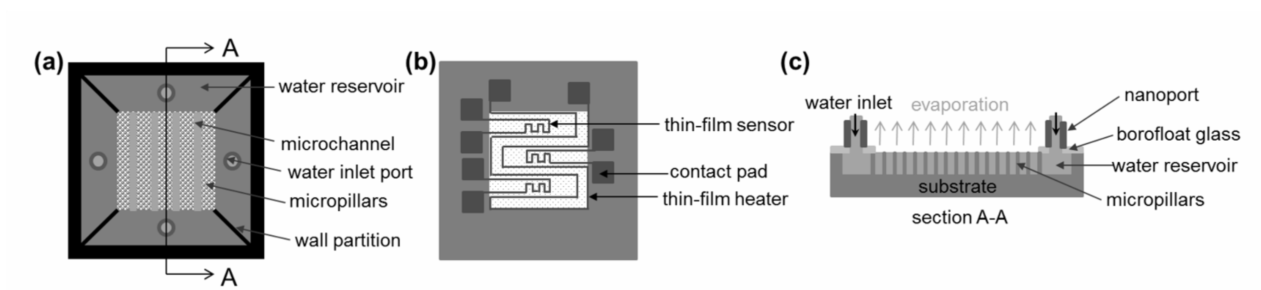
Experimental Investigation of Thin-film Evaporation from Microstructured Surfaces for Thermal Management

S. Adera, D.S. Antao, R. Raj, E.N. Wang
Sponsorship: Office of Naval Research with Mark Spector as program manager, National Science Foundation GRFP

Thermal management is a primary design concern for numerous high power density devices such as integrated circuits, electric vehicles, military avionics, photonic devices, and solar energy convertors. This is especially true in the microelectronics industry where the increase in the number of integrated circuits and operating speed has increased the waste heat that is generated at the device footprint from 30 W/cm2 in the 1970's to 100 W/cm2. Moreover, this heat flux is projected to reach 300 W/cm2 in the next few years introducing new challenges in thermal management that has forced the industry to seek advanced cooling solutions. Unfortunately, the widely used conventional single-phase cooling systems are inferior in performance and cannot be used for applications that require removal of high heat fluxes in excess of 100 W/cm2. As a result, state-of-the-art single-phase cooling systems are limited to low heat flux devices and the proposed solution is to use liquid-vapor phase change systems such as thin-film evaporation [1, 2] to make use of the high latent heat of vaporization that can be harnessed during the phase change process.

In this experimental study, we investigated the complex fluidic and thermal transport processes when a thin-liquid film is evaporating from a microstructured surface. We fabricated well-defined microstructured surfaces using contact photolithography and deep reactive ion etching. In addition to offering rich opportunities to manipulate the fluid dynamics, microstructured surfaces in combination with chemical functionalization have long been recognized for enhancing thermal performance in phase-change process. The induced roughness generates capillary pressure for passive liquid transport [3]. The liquid transport was further assisted by incorporating microchannels which reduce the overall flow resistance of the porous media. For integrated heating and temperature measurement, we used electron-beam evaporation and acetone lift-off to create a thin-film heater and sensors. This work elucidates new and innovative techniques to utilize microstructured surfaces for thermal management.



▲ Figure 1: Test sample. (a) Front, (b) back, and (c) cross sectional view of the schematic of a typical test sample. The overall dimension of the test sample was 3x3 cm2 while the microstructured area was only 1x1 cm2. The diameter, height, and spacing of the micropillars were 4-12, 10-100, and 10-20 μm, respectively. Liquid was supplied to the microstructured area from the surrounding water reservoir via capillary-wicking. Microchannels were also used to assist the liquid transport by reducing the overall flow resistance of the porous media. The microstructured area was heated using a thin-film heater and the backside temperature was measured using sensors.

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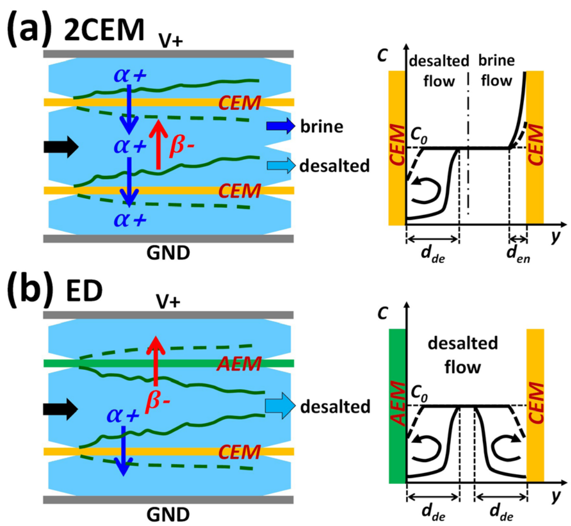
Scalable and Direct Water Purification Technology by Ion Concentration Polarization

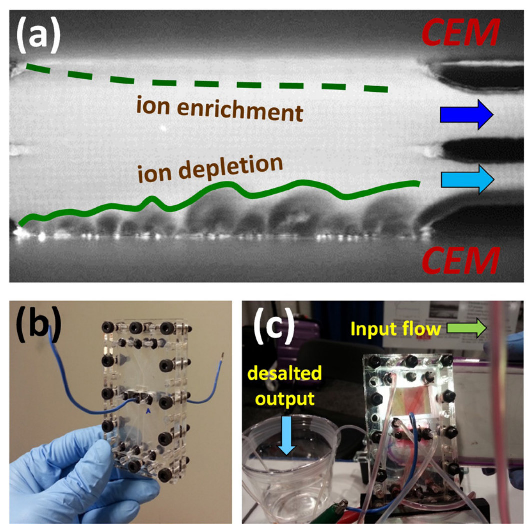
B. Kim, H.J. Kwon, V.S. Pham, J. Han
Sponsorship: ARPA-E

We demonstrate a scalable and direct water purification technology using ion concentration polarization (ICP). Although nonlinear ICP was shown to generate a strong depletion zone near the ion exchange membrane (IEM), several challenges (power consumption, expandability, etc.) must be overcome for ICP to be a competitive technology in desalination. To resolve and improve them, we propose a modified ICP platform for water desalination by involving two identical cation exchange membranes (CEMs); it demonstrates better salt removal and energy efficiency than conventional electrodialysis (ED), as Figure 1 shows. Between two parallel CEMs, ion depletion/enrichment zones are generated near the CEMs under an electric field. As cations selectively transfer through the CEMs, anions relocate to achieve electro-neutrality, resulting in a decreased/increased concentration in the ion depletion/enrichment zone. Given that the desalted and brine flow streams form on the cathodic and anodic CEM in the main channel, respectively, we can separate and collect each desalted and brine flow by bifurcating the channel at the end. Our technique offers a significant advantage for reducing the number of water purification stages over other conventional technologies since we can obtain desalted flow delivering any charged particles (contaminants) to the brine channel simultaneously.

To visualize the electrokinetic phenomena between the membranes, we fabricated a PDMS-based microfluidic chip with thin channel depth (~0.2mm) and injected a sodium chloride solution mixed with fluorescent dye, as in Figure 2(a). Additionally, to increase system throughput, we built a plastic-based desalination prototype (~1ml/min) by expanding the channel depth and successfully operated it over ten hours, as shown in Figures 2(b) and 2(c). Therefore, we expect our ICP desalination to be a practical technology for water purification, providing both lower energy cost and high throughput.



▲Figure 1: Desalination/purification strategy. (a) 2CEM and (b) ED. Blue and red arrows indicate movement of cations α+ and anions β-. Ion depletion zone d_{de} with low ion concentration occurs at anodic side of CEMs (green lines). Ion enrichment zone d_{en} with high ion concentration occur at other side of CEMs (green dotted lines).



▲Figure 2: (a) Fluorescent image of typical desalination process between two cation exchange membranes (~1.2mm). Photograph of (b) high-throughput desalination prototype (~1ml/min) and (c) its long-time operation.

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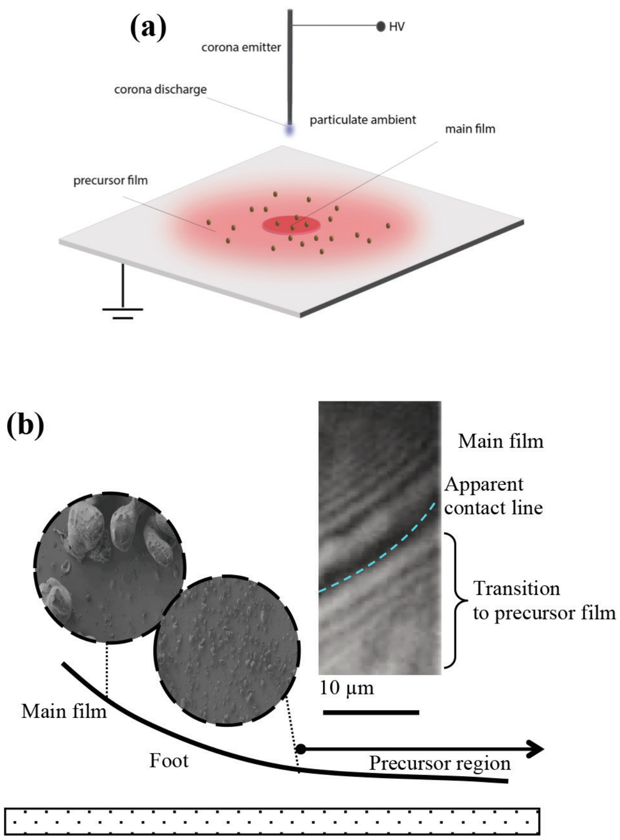
Electrostatic Precursor Films

S.R. Mahmoudi, K. Adamiak (University of Western Ontario), G.S.P. Castle (University of Western Ontario), K.K. Varanasi

When a liquid spontaneously spreads over a solid surface, a progressive microscopic structure—conventionally known as van der Waals driven precursor film—develops ahead of the moving contact line. Here, we report a new class of electrostatically assisted precursors containing microscopic charged particles. This precursor manifests itself as the late stage of forced-spreading of a macroscopic dielectric film subjected to a unipolar ionic discharge in a gas containing particulates. We put a model forward to predict dynamic behavior of this electrostatic precursor dynamics. The spreading of the precursor film is predicted to be proportional to the square root of exposure time, which is consistent with the ellipsometric measurements.



◀ Figure 1: (a) Figurative description of corona discharge assisted spreading of dielectric films. Thin film interferometry of oil/air interface around apparent contact line of oil film exposed to 2400 s corona discharge exposure (b) in the presence of dust particle (Arizona Road Dust®) with a mean size of 5μm. Silicone oil viscosity, surface tension and electrical conductivity were measured to be 50 cst, 21 mN/m, 920 pS/m, respectively at 25°C±2°C.

Continuous-flow Microcalorimetry Using Silicon Microreactors and Off-the-shelf Components

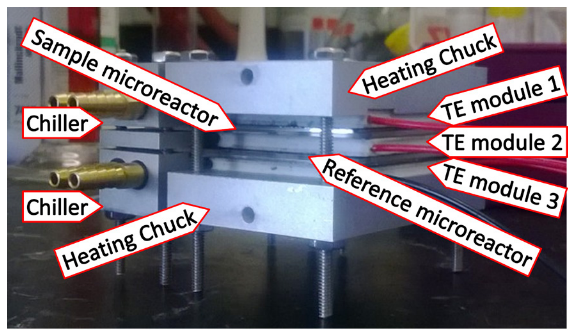
E.W. Lam, M.A. Schmidt
Sponsorship: MTL

Calorimetry is an important method for studying the kinetics and energy requirements of chemical and/or biological reactions. In particular, calorimetry can characterize the heats of reaction (ΔH) to determine the necessary heat transfer requirements when scaling up production, for example whether the system has the appropriate amount of heating/cooling elements to sustain its optimal reaction conditions. There are many products and devices capable of characterizing ΔH, such as differential scanning calorimeters, thermal activity monitors, and isothermal nanocalorimeters; however, these systems utilize fixed volumes of reactants and are inherently incapable of being run in-line with continuous flow without complex modifications.

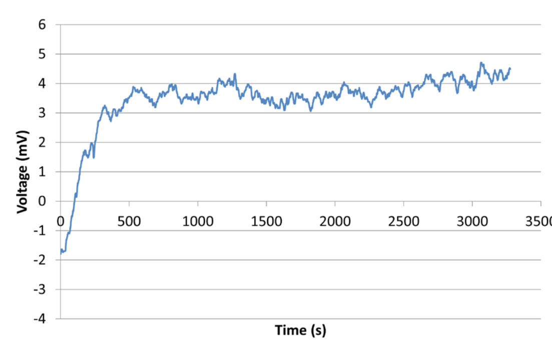
Unlike traditional calorimeters, this microcalorimeter is designed for continuous flow and to run in-line with an automated microfluidic reaction optimization system with little-to-no modifications. Previously, a similar microcalorimeter was proposed; however, the design had a high heat flux threshold (>50mW), limiting its usefulness to high-energy and/or high-concentration reactions (>1M for reactions where ΔH ≥ 50kJ/mol). This previous design had several other drawbacks including long thermal time constants due to its large thermal mass and requiring a control (baseline) reaction to be run sequentially with the sample reaction. Our design utilizes a parallel-reactor setup, enabling the baseline and sample reactions to run concurrently and allows for direct measurement between the parallel reactors. This parallel setup reduces the thermal mass and experimental time and results in a predicted 5x increase in thermal sensitivity. As such, the microcalorimeter is capable of characterizing ΔH's faster than the previously mentioned design while at lower (<1M) concentrations.

Currently, the continuous-flow microcalorimeter consists of two parallel silicon microreactors, one running the chemical reactions and the other running a baseline reaction. The microreactors are sandwiched in between a series of thermoelectric modules and a machined aluminum jig, and the ΔH is measured by heat flux between the microreactors. The microcalorimeter was used to characterize a Paal-Knorr reaction, resulting in the thermoelectric modules measuring a voltage of 3.70±0.27mV, corresponding to a heat flux of 170.7±12.5mW. When running the baseline reaction in both reactors, the system had a noise floor of 0.19mV. Extrapolating the signal to the noise floor, we predict that the microcalorimeter will be capable of measuring heat fluxes as low as 8.6mW.

Our next step for the microcalorimeter is to continue refining the thermal control mechanisms to further improve the heat flux sensitivity. Additionally, we will designed and fabricate a specialized silicon microreactor for the ΔH characterization of solar thermal fuels, molecules designed by our collaborators that are capable of storing solar energy and subsequently releasing the solar energy as heat at a later date. Finally, the system will be inserted into an automated cycling setup to monitor to analyze the stability and cycling longevity of the solar thermal fuels.



▲Figure 1: Photograph of assembled microcalorimeter. The chiller is powered by pumping 0°C water through the aluminum block. Cartridge heaters connected to a PID controller are used to heat the reactors. Sample and reference inlet/outlet ports attach to top and bottom of the chiller blocks, respectively.



▲Figure 2: Voltage of TE module 2 as a function of time when running sample and baseline reactions concurrently. As can be seen, the system takes 5 minutes to reach steady-state and results in average response of 3.70mV, which corresponds to an average heat flux of 170.7mW.

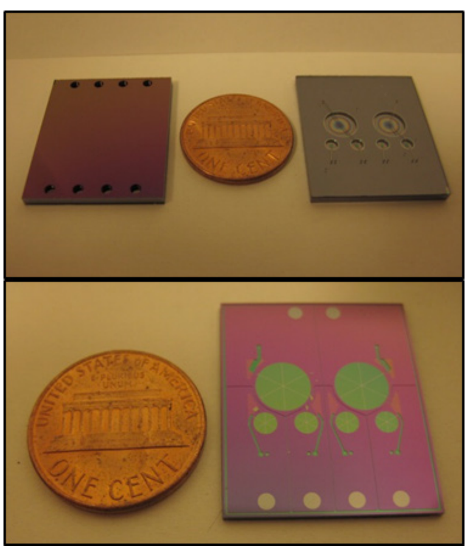
MEMS Two-stage Diaphragm Vacuum Pump

E. Newton, H. Li, M. Schmidt
Sponsorship: DARPA

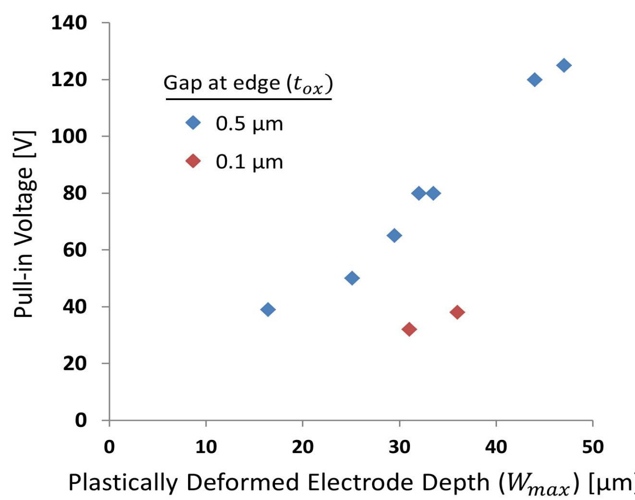
Portable sensing devices such as microscale mass spectrometers need vacuum pumping to lower samples at atmospheric pressure to the desired measurement pressure range. Further improvements for MEMS accelerometers, gyros, and other resonant sensors require internal pressures as low as a few microtorr, which is possible only with active vacuum pumping. While these pressures are easily achieved using macroscale vacuum pumps, the larger pumps are not portable, negating the benefits gained from making small, low-power sensors in the first place. To realize the full potential of portable sensors, a chip-scale vacuum pump needs to be developed.

We have developed what is to our knowledge the first two-stage MEMS displacement pump with integrated electrostatic actuation. Two pump stages, along with an efficient layout that minimizes dead volume and a new actuation scheme should enable it to reach pressures below 30 Torr. Actuation is achieved by electrostatically zipping a thin flexible membrane down onto a stiff curved electrode. This actuator topology allows for large displacements and large forces at relatively low voltages (< 100 V). An image of a fabricated two stage micropump is shown in Figure 1 below.

We have developed two methods for producing curved electrodes in MEMS devices: 1) hot air trapped during wafer bonding expands with enough pressure to plastically deform thin silicon membrane and 2) strain induced when epoxy cures can pull a membrane into a curved shape. Using the plastically deformed electrodes, we have demonstrated that we can reliably and repeatably zip a thin membrane at low voltages and we have mapped out how the critical voltage depends on the deformation magnitude and the oxide thickness. This is shown in Figure 2 below. These accomplishments have helped us understand the fabrication process and physics of device operation. We plan in the next year to further examine the reliability of plastic deformation in our process, testing the actuators at low pressures, and we hope to fabricate a working micropump that is capable of achieving pressures as low as 30 Torr.



▲ Figure 1: Microfabricated two-stage vacuum pump. Top and bottom views of the pumps are shown (top) as are internal fluidic connections (bottom).



▲ Figure 2: Pull-in voltages for 6 mm diameter curved electrodes with a 25 µm thick zipping membrane.

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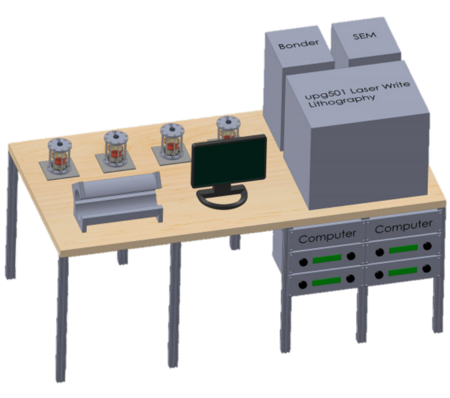
A Tabletop Fabrication System for MEMS Development and Production

P.A. Gould, M.D. Hsing, K.K. Gleason, M.A. Schmidt
Sponsorship: MTL

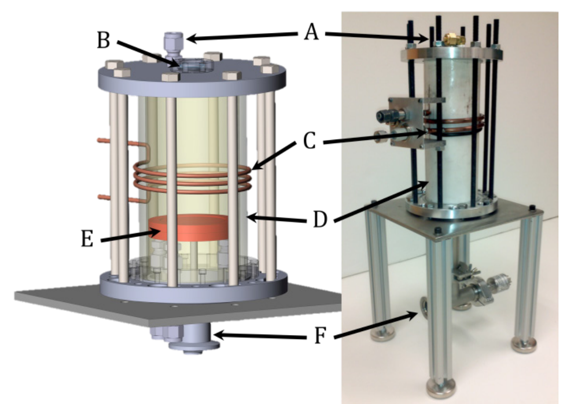
A general rule of thumb for new semiconductor fabrication facilities (fabs) is that revenues from the first year of production must match the capital cost of building the fab itself. With modern fabs routinely exceeding $1 billion to build, this rule serves as a significant barrier to entry for small entities seeking to develop or commercialize new semiconductor devices. The barrier is especially formidable for those groups whose devices target smaller market segments or those which require exotic materials or nontraditional process sequences. The foundry fab model has arisen partially to overcome this inefficiency, but to remain profitable, these foundries typically offer only a few standardized processes that limit customer customization. The limited diversity afforded by these foundries can make some devices with smaller market sizes economically viable, but many devices (particularly in the MEMS sector) require process customization beyond the level currently offered by commercial foundries.

To address these problems, we are working to create a suite of tools that processes 1-2" substrates. This suite of tools (known colloquially as the 1" Fab) takes advantage of modern processing techniques, but at a fraction of the normal cost. We anticipate a full set of tools for product development and small-scale production to cost ~$1 million and require <50 ft^2 of space (roughly a large conference table, see Figure 1 for a rendering), compared to >$1 billion and >50,000 ft^2 for a typical 8" fab. In addition to the reductions in equipment cost and required space, a 1" Fab also uses significantly less total materials and reagents, requires far less energy to operate, and lessens the environmental impact of fabrication. The total throughput possible in a 1" Fab certainly cannot match a typical 8" fab, but the vast majority of devices that are unsuitable for traditional foundries simply do not require this advantage in production rate. For these devices, the cost savings of the 1" Fab platform and its ability to quickly prototype designs far outweigh any expansion in production schedules.

We are currently developing a deep reactive ion etcher (DRIE) tool for the 1" Fab. DRIE tools are used to create highly anisotropic, high aspect-ratio trenches in silicon—a crucial element in many MEMS processes. The modularized design of our DRIE system can be easily adapted to produce other plasma-based etching and deposition tools (like PECVD and RIE). Our DRIE, shown in Figure 2, is the about the size of a large microwave oven and costs just a small fraction of a commercial system. We have demonstrated etch rates of >6 microns per minute and anticipate achieving etch rates of 10μm/min with further process tuning. In the coming year we will continue to optimize our DRIE design and begin developing PECVD and high-temperature process (e.g. oxidation and LPCVD) tools for the 1" fab.



▲ Figure 1: Computer rendering of envisioned 1" Fab toolset. A complete set of tools as shown would allow for standard silicon processing: maskless lithography system, wafer bonder, tabletop SEM, LPCVD / oxidation / annealing furnace, DRIE, PECVD, and a sputtering / evaporation tool.



▲ Figure 2: 1" Fab Tabletop DRIE. The associated labeled parts are as follows: A) process gas inlet, B) viewport, C) RF coil, D) alumina chamber, E) liquid cooled and RF powered wafer chuck, F) vacuum pump inlet.

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Energy: Photovoltaics, Energy Harvesting, Batteries, Fuel Cells

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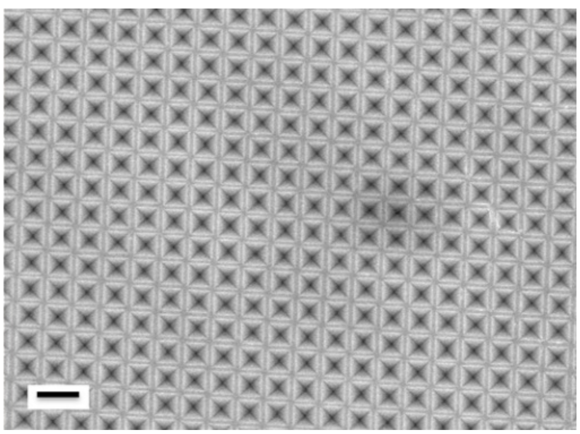
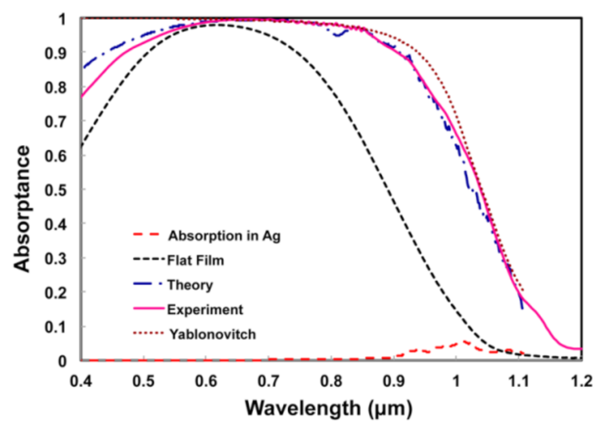
High-efficiency 10-µm-thick Thin Film c-Si Solar Cells Enabled by Inverted Nano-pyramid Light-trapping Structures

M.S. Branham, W. -C. Hsu, S. Yerci, G. Chen
Sponsorship: SunShot Initiative, Department of Energy, USA

Crystalline silicon (c-Si) is the dominant material in the photovoltaic industry, yet silicon is expensive and contributes ~40% to the total module cost of c-Si solar cells. Reducing the material intensity by creating thin-film devices is one strategy to reduce the overall cost of silicon PV. Here, we demonstrate experimentally that an inverted nanopyramid light-trapping scheme for a 10-µm-thick c-Si thin-film can achieve an absorptance value comparable to that of a 300-µm-thick planar device. Figure 1(a) shows a scanning electron microscope image of a 700-nm-pitch inverted nano-pyramids (INPs) light-trapping structure. In Figure 1(b), simulation shows the comparable ultimate efficiency with a 300-µm-thick planar device using a 10-µm-thick c-Si thin-film with INPs structure, and its corresponding reflection data are also measured in Figure 1(c). We are applying these light-trapping structure to thin silicon-on-insulator wafers to produce photovoltaic devices with current energy conversion efficiencies exceeding 13%. To reach the high efficiencies necessary for a commercial product, we also constructed a multi-physics optimization tool incorporating both optical absorption and an electronic carrier collection to understand in detail the loss mechanisms of the devices, including incomplete photonic absorption, contact recombination, surface recombination, and Schottky-Read-Hall and Auger recombination. Our model predicts that a 10-µm-thick thin-film c-Si solar cell with an inter-digitated back contact scheme can have an efficiency higher than 20%.



▲Figure 1: Scanning electron microscope image of inverted nano-pyramids (INPs) with a pitch of 700 nm. The scale bar is 1µm.



▲Figure 2: Comparison of theoretical and experimental absorptance spectra. Dimensions of the flat film structure are 70 nm SiNx, 10 µm Si, 250 nm SiO_2, and 200 nm Ag in thickness. The inverted pyramid structure consists of 90 nm SiNx, 10 µm Si, 0.5 µm SiO_2, and 200 nm Ag. Note that, except for Ag absorption curves, other absorptance spectra account for absorption in all layers.

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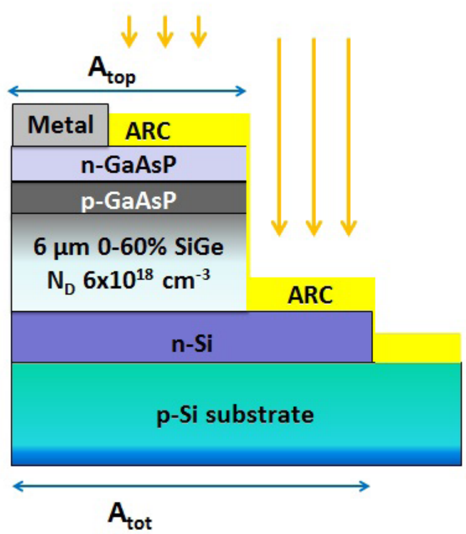
Step-cell Design for Tandem GaAsP/Si Solar Cells

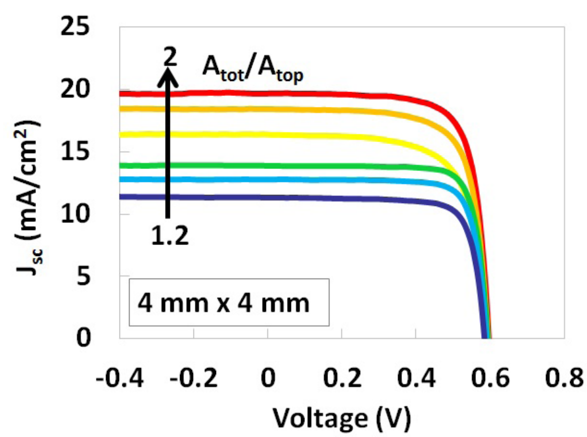
E. Polyzoeva, S. Hadi, E.A. Fitzgerald, A. Nayfeh, J.L. Hoyt
Sponsorship: Masdar Institute of Science and Technology

This work is part of a collaborative project aimed at ultimately achieving photovoltaic conversion with more than 40% efficiency at a lower cost by combining low-cost manufacturing on Si wafers with high-efficiency III-V materials in one tandem cell. In order to grow high quality GaAsP layers on the Si cell, a graded SiGe buffer is used to provide a transition from the lattice constant of the Si to that of the GaAsP, as in Figure 1. However, due to its smaller bandgap than Si, the SiGe buffer absorbs a portion of the light intended for the Si sub-cell and reduces the overall cell efficiency. In this work, we explore a step-cell design aimed at increasing the amount of light reaching the Si sub-cell.

Figure 1 shows the step-cell design for the tandem GaAsP/Si structure. Part of the GaAsP top cell and the SiGe graded buffer is etched away to expose the Si sub-cell. In the initial experiments, the step-cell design was implemented on a Si cell with SiGe layer grown on top to assess the effect of varying the area of exposed Si on the short circuit current of the solar cell. The current-voltage characteristics of the SiGe/Si cells as a function of the A_{tot}/A_{top} ratio are shown in Figure 2. The short circuit current increased from 11 to 20 mA/cm² when the ratio increased from 1.2 to 2. These results demonstrate that the step-cell design is effective in increasing the current of the Si sub-cell and therefore improving the overall efficiency. Going forward, the step-cell design will be implemented into the complete tandem structure, including the GaAsP sub-cell.



▲Figure 1: Step-cell design of GaAsP/Si tandem solar cell with SiGe graded buffer. Part of the GaAsP and SiGe layers is etched away to allow more light to reach the Si sub-cell and to provide higher overall efficiency.



▲Figure 2: J-V characteristics of a SiGe/Si step cell as a function of A_{tot}/A_{top} ratio. The structure is the same as in Figure 1 without the GaAsP layers. The short-circuit current increases from 11 to 20 mA/cm^2 when the ratio increases from 1.2 to 2.

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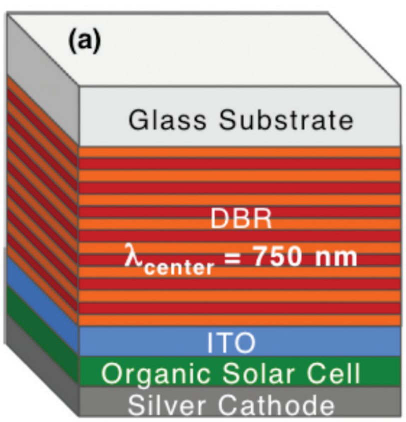
Slow Light-Enhanced Singlet Exciton Fission Solar Cells with 126% External Quantum Efficiency

D.N. Congreve, N.J. Thompson, D. Goldberg (CUNY), V.M. Menon (CUNY), M.A. Baldo
Sponsorship: Department of Energy, Basic Energy Sciences, DE-SC0001088

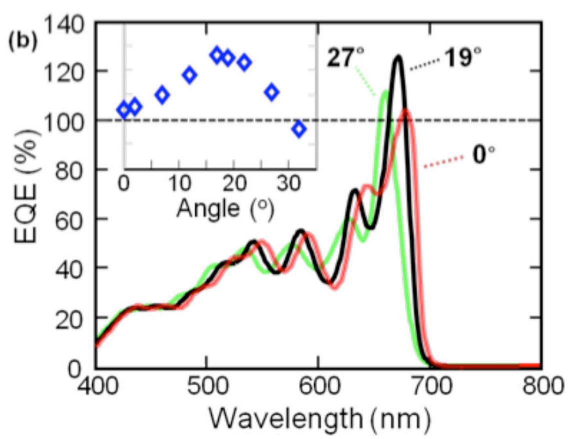
Singlet exciton fission can improve the electrical yield of solar cells without increasing the number of photovoltaic junctions by generating up to two electrons for every incident photon. A key measure of the efficiency of fission is the external quantum efficiency (EQE), the fraction of incident photons that are converted into electrons and delivered to the load. Recent demonstrations using pentacene have proven that singlet exciton fission in organic solar cells can deliver EQEs exceeding the benchmark 100%. The limiting factor in these devices is light absorption. Unfortunately, it is not possible to simply use a thicker layer of pentacene because its excitons decay before dissociating into charge.

Light management, however, is a feasible method to improve absorption within thin pentacene layers. We demonstrate a simple approach for enhancing absorption in thin film organic solar cells by exploiting the slow light modes that appear at the band edge of a distributed Bragg reflector (DBR). Using this approach we show over a 50% enhancement in absorption and EQE of singlet-exciton-fission-based solar cells.

When the DBR band-edge mode is tuned to the peak wavelength of pentacene's extinction coefficient, we observe an EQE peak of 126±1%, as in Figure 2. A control solar cell fabricated identically but without the DBR achieved a peak EQE of only 83% and exhibited nearly zero change in EQE with varying incident angle. The DBR-enhanced device demonstrated EQE greater than 100% for incident angles over the range +/-27°, with a relatively flat response; see inset of Figure 2. This technology can greatly improve absorption without adding significant device complexity.



▲Figure 1: Device structure of the organic photovoltaic. A microcavity is created with the DBR and the silver cathode, boosting absorption in the organic layers.



▲Figure 2: External quantum efficiency as a function of incident light angle. The device shows a photocurrent enhancement for a wide angle range.

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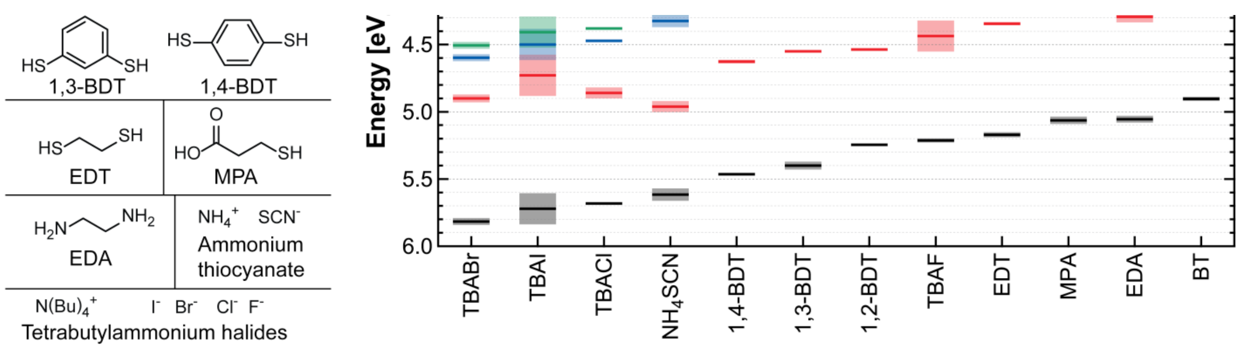
Energy Level Modification in Lead Sulfide Quantum Dot Photovoltaics Through Ligand Exchange

P.R. Brown, D. Kim, N. Zhao, R.R. Lunt, M.G. Bawendi, J.C. Grossman, V. Bulović
Sponsorship: Hertz Foundation, National Science Foundation, Samsung

The electronic properties of lead sulfide (PbS) colloidal quantum dots (QDs) are highly dependent on QD size and surface chemistry. Novel surface passivation techniques involving organic or inorganic ligands have contributed to a rapid rise in the efficiency of QD photovoltaics, yet the influence of ligand-induced surface dipoles on PbS QD energy levels and photovoltaic device operation is not yet fully understood. Ligand exchange treatment is known to shift the valence and conduction band energies of CdSe and InAs QDs, but the incidence of similar shifts in PbS QDs and their relevance to the operation of PbS QD photovoltaics have yet to be explored. Here, the valence band energies of PbS QDs treated with twelve different ligands are measured using ultraviolet photoelectron spectroscopy (UPS) and correlated with the results of atomistic simulations and photovoltaic device characterization. As shown in Figure 1, a valence band shift of up to 0.9 eV is observed between different ligand treatments. Treatments with 1,2-benzenedithiol and 1,3-benzendithiol, which result in valence band energies differing by ~0.2 eV, are employed for PbS QDs in three different solar cell architectures, and changes in device performance are correlated with the measured energy level shift. Atomistic simulations of ligand binding to pristine PbS(100) and PbS(111) slabs qualitatively reproduce the measured energy level shifts. These findings complement the known bandgap-tunability of colloidal QDs and demonstrate an additional level of control over the electronic properties of PbS QDs.



▲ Figure 1: Ligand-induced band energy shifts in PbS QDs. (a) Chemical structure of ligands studied here, including thiols (1,4-benzenedithiol (1,4-BDT), 1,3-benzenedithiol (1,3-BDT), 1,2-benzenedithiol (1,2-BDT), benzenethiol (BT), 1,2-ethanedithiol (EDT), and 3-mercaptopropionic acid (MPA)), primary amines (1,2-ethanediamine (EDA)), ammonium thiocyanate (NH4SCN), and tetrabutylammonium halides (iodide (TBAI), bromide (TBAB), chloride (TBAC), and fluoride (TBAF)). (b) Energy levels of ligand-exchanged 3.3-nm diameter PbS QDs measured by UPS (valence band and Fermi level) and absorption spectrophotometry (conduction band). The measured direction of the shifts correlates with computational simulations of ligands binding to PbS(100) and PbS(111) surfaces and with the performance of PbS QD photovoltaic devices.

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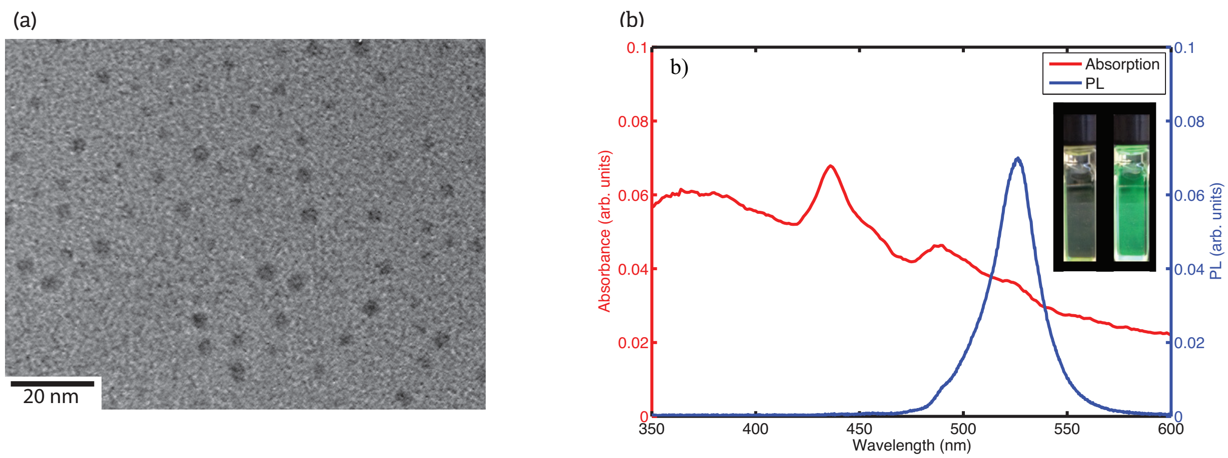
Optical and Structural Properties of Organohalide Perovskite Nanocrystals

P. Tyagi, W.A. Tisdale
Sponsor: U.S. Department of Energy

Over the last few years, organohalide perovskites have emerged as the most promising contenders in the field of photovoltaics. These materials are cost-effective, exhibit large carrier diffusion lengths (~1 micron), and have high power conversion efficiencies (> 14%). Although the general perovskite structure has been known for more than six decades, the unique composition of organohalide perovskites has shown favorable properties for photovoltaic applications. Most research on organohalides has focused on studying charge transport processes in thin films for device fabrication purposes. However, the properties of organohalides in the nanoscale length regime are mostly unexplored. We are currently investigating the correlation between structural and transport properties of perovskite nanocrystals. In particular, we have synthesized nanocrystals (NCs) of methylammonium lead bromide perovskites following the procedure of Schmidt et al. below. The NCs are nearly 4 nm in diameter (see Figure 1a) and exhibit bright emission in the visible (see Figure 1b). Experiments are underway in our lab to study transport properties of these materials using spatially and temporally resolved photoluminescence spectroscopy.



▲ Figure 1: (a) TEM, (b) absorbance (red), and photoluminescence (blue) of methylammonium lead bromide NCs. The inset of (b) shows a cuvette of NCs in the absence (left) and presence (right) of UV excitation.

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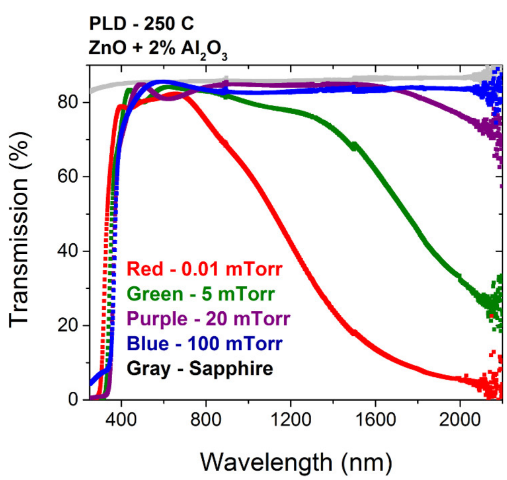
Utilization of Doped-ZnO and Related Materials Systems for Transparent Conducting Electrodes

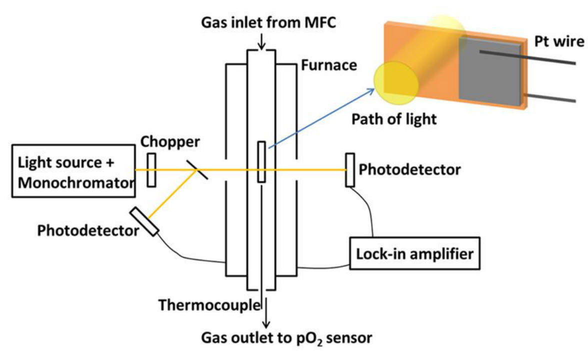
M. Campion, H.L. Tuller in collaboration with A. Gougam, T. Buonassisi
Sponsorship: Masdar Institute of Science and Technology

Efficient transparent electrode materials are vital for applications in smart window, LED display, and solar cell technologies. These materials must possess a wide band gap for minimal optical absorption in the visible spectrum while maintaining a high electrical conductivity. Tin-doped indium oxide (ITO) has been the industry standard for transparent electrodes, but limitations in both deposition temperature and use of the rare element indium has led to a search for better material alternatives. Doped ZnO represents one of the most promising alternatives, but the mechanisms by which processing conditions and defect chemistry affect the final material properties are not well understood. Reported values of the electrical and optical properties for doped ZnO can vary widely for seemingly similar processing conditions performed by different experimental groups. This could be due to the strong dependence on oxygen partial pressure, as demonstrated in Figure 1.

This work seeks to better understand the relationships between processing, defect chemistry, and material properties of ZnO. To accomplish these goals, methods such as *in situ* resistance and impedance monitoring during annealing and atom probe tomography will be applied. In addition, a variety of novel methods such as the *in situ* monitoring of optical transmission (shown in Figure 2) during annealing and the *in situ* monitoring of resistance during physical vapor deposition will be utilized to investigate ZnO. Direct measurements of the key constants for the thermodynamics and kinetics of oxidation in donor-doped ZnO will be experimentally determined for the first time. This increase in understanding will provide a predictive model for determining optical properties, carrier concentrations, and electron mobilities in ZnO, which is becoming an increasingly important material for transparent electrodes, nanostructures, and oxide transistors.



▲Figure 1: Change in optical transmission characteristics of Al-doped ZnO due to changing oxygen partial pressure during deposition. This is brought about through the creation and annihilation of compensating ionic defects, which can heavily alter the carrier concentration.



▲Figure 2: Schematic of experimental setup to be used for simultaneous *in situ* measurement of the optical transmission and electrical conductivity of thin film ZnO samples during annealing under controlled atmosphere and temperature.

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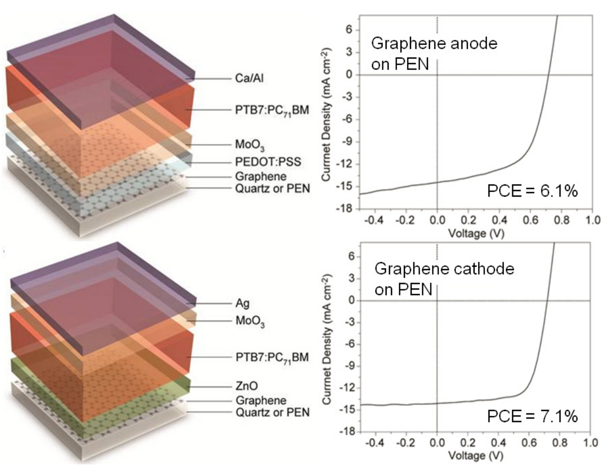
High-efficiency Graphene-based Flexible Organic Solar Cells

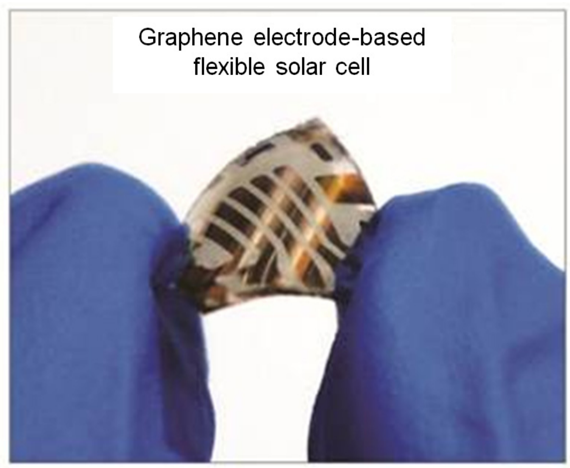
S. Chang, H. Park, X. Zhou, J. Kong, T. Palacios, S. Gradečak
Sponsorship: Eni S.p.A.

Flexible solar cells belong to the promising next generation of optoelectronic devices. Electrode materials with good conductivity, transparency, and flexibility must be developed for these solar cells. Graphene has been considered a promising flexible transparent electrode due to its good electrical conductivity and optical transparency along with mechanical and chemical robustness and potentially low-cost processing. We have successfully demonstrated both graphene anode- and cathode-based flexible polymer solar cells (PSCs) with thieno[3,4-b]thiophene/benzodithiophene (PTB7) and [6,6]-phenyl C71-butyric acid methyl ester ($PC_{71}BM$) by resolving the issues occurring at the interface between graphene and charge transporting semiconducting materials such as molybdenum trioxide (MoO_3) or ZnO. We demonstrate high-efficiency graphene electrode-based flexible PSCs with power conversion efficiencies of 6.1% (anode) and 7.1% (cathode). These efficiencies were achieved by thermal treatment of MoO_3 electron blocking layer and direct deposition of ZnO electron transporting layer on the graphene surface.

We expect our work to pave the way to realizing fully graphene electrode-based flexible solar cells by a simple and reproducible method. The advances accomplished in our work demonstrate graphene's promise as an alternative transparent electrode system in a variety of optoelectronic devices.



▲Figure 1: Schematic of a graphene anode- and cathode-based PSCs and corresponding AM1.5G *J–V* characteristics of graphene-based flexible PSCs.



▲Figure 2: A digital photograph of a flexible graphene PSC.

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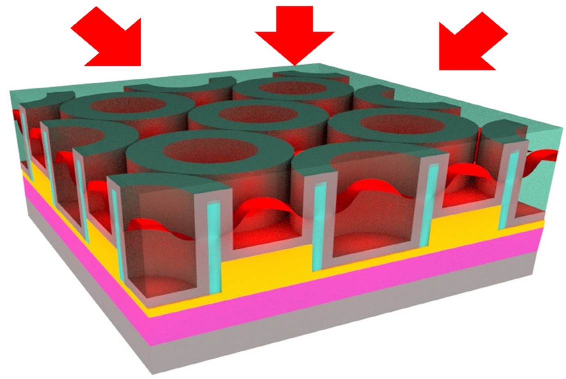
Enabling Ideal Solar-thermal Energy Conversion with Metallic Dielectric Photonic Crystals

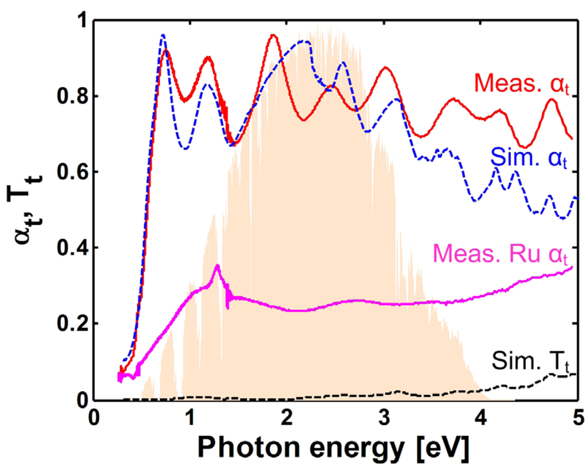
J.B. Chou, S.-G. Kim
Sponsorship: S3TEC

The selective absorption of sunlight plays a critical role in solar-thermophotovoltaic (STPV) energy conversion by tailoring both the absorption and emission spectra for efficient solar-thermal-electrical energy conversion. By selectively absorbing solar energy while suppressing long wavelength emission, optimal solar-thermal energy conversion can be achieved. In practical STPV systems, selective absorbers must simultaneously contain optical, manufacturing, and reliability properties. Here we present our solution, which contains all of the ideal properties of a selective absorber for large-scale and efficient solar energy conversion.

Metal absorption of sunlight plays a critical role in STPV energy conversion, selective solar absorption, selective thermal emission, and hot-electron generation. However, a broadband, high-temperature-stable, omnidirectional, wafer-scale, selective solar absorber from the visible to the near-IR has yet to be demonstrated experimentally. We present a silicon wafer-scale fabricated metallic dielectric photonic crystal (MDPhC) with an average absolute absorption of 85% for photon energies 5 eV>$\hbar\omega$>0.7 eV and an absorption below 10% for $\hbar\omega$<0.4 eV. Angled measurements show the existence of the cavity modes for angles up to 70° from normal. Furnace tests at 1000°C for 24 hours show no degradation in optical performance. Simulations indicate that the broadband absorption is due to a high density of the hybrid cavity and surface plasmon modes overlapped with an anti-reflection coating. The MDPhC was fabricated using traditional MEMS/CMOS-compatible fabrication techniques on a 6" wafer by utilizing the sidewall lithography technique. The optical properties of the MDPhC allow for broadband solar energy conversion and can lead to new applications for metal optics.



▲Figure 1: Schematic of the MDPhC device where incident light is coupled into cavity modes.



▲Figure 2: Measured absorption spectrum of MDPhC (red), simulated spectrum (blue), flat Ru (pink), and transmission through MDPhC (black). The solar spectrum is shown for reference.

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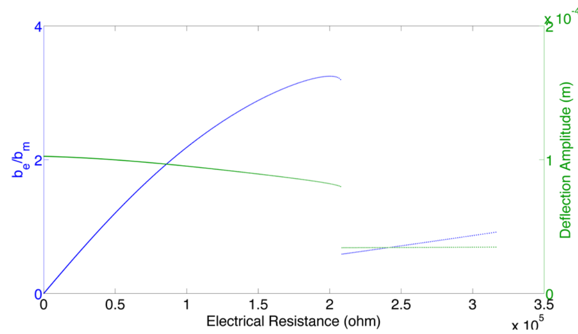
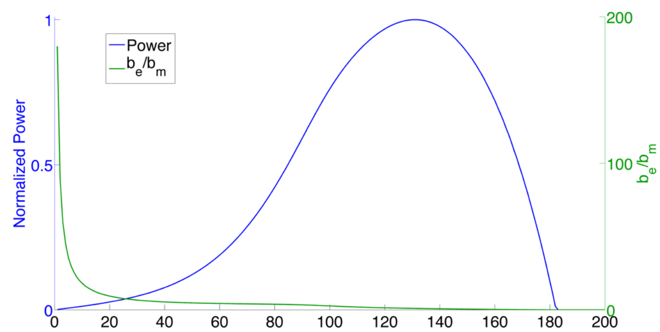
Nonlinear Resonance-based Piezoelectric Vibration Energy Harvesting

R. Xu, G. Gafforelli, Y. Yoon, A. Corigliano, S.-G. Kim

Linear resonance-based energy harvesters have been popular for vibration energy harvesting, due to their simplicity of micro-fabrication and high power efficiency at resonance. Nevertheless, the narrow frequency bandwidths that linear energy harvesters suffer prevent the technology from applying in the real frequency-changing ambient environment. As a promising potential solution, nonlinear resonance widens the power bandwidth by one order of magnitude, which shows the great potential of nonlinear designs. We built an electromechanically coupled, lumped model to provide a comprehensive analysis of nonlinear resonance-based energy harvesting. The model was based on the configuration of a doubly clamped beam with a thin film piezoelectric element working in d_{33} mode. The static indeterminate structure problem was solved with the Euler-Bernoulli beam theory and energy method. By considering the simple case of inputting a sinusoidal force and connecting the harvester to a resistor, we employed Kirchhoff's laws and the Harmonic Balance Method (HBM) to build and solve the nonlinear differential equations. Closed form expressions of the system's parameters were obtained from the analysis. The coupled, lumped model has verified varying electrical loads at each frequency to generate maximum power at that frequency by showing a power spectrum with a much wider bandwidth. Furthermore, the optimal electrical damping at each frequency was obtained; it shows that the electrical damping should be much higher than the mechanical damping to increase the power at low frequencies, and the maximum power is obtained when the electrical damping matches the mechanical damping.



▲Figure 1: The normalized electrical damping and deflection amplitude vs. electrical resistance. The insensitivity of the deflection to the change of damping explains the wide power bandwidth.



▲Figure 2: The maximum power envelope and the normalized optimal electrical damping at each frequency. The optimal electrical damping condition at each frequency could be useful to further widen the power bandwidth.

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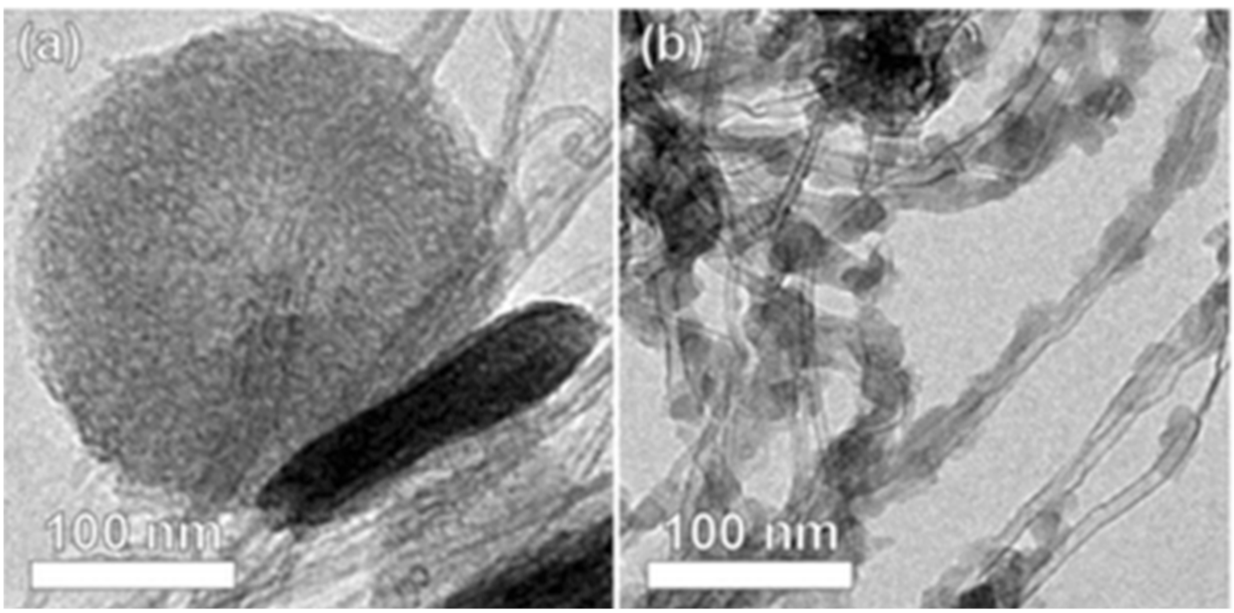
Materials and Structures for Lithium-Air Batteries

T. Batcho, R.R. Mitchell, B. Gallant, D. Li, Y. Shao-Horn, C.V. Thompson
Sponsorship: Bosch, National Science Foundation, MRSEC

Lithium-air batteries hold promise for the next generation of electric vehicles and other applications. By reacting oxygen directly with lithium ions to form Li_2O_2 on discharge, these batteries can achieve energy densities 3-5 times higher than current lithium-ion batteries. However, a number of challenges exist for implementing lithium-air batteries, including poor rate capability, poor cyclability, high overpotentials upon charging, and electrode and electrolyte instability. We seek to address these issues by developing new electrode materials and architectures and performing studies of Li_2O_2 formation in different electrolyte solvents.

Aligned arrays of carbon nanotubes (CNTs) provide ideal conductive scaffolding materials for Li_2O_2, while occupying a small volume fraction and having low mass. CNTs of 5-10 nm in diameter are grown in aligned forests on catalyst deposited silicon wafer and delaminated. These free-standing carpets can be placed directly into our cell. We observed near-ideal gravimetric capacities and high volumetric capacities. We have observed two distinct types of morphologies upon discharge, depending on the rate and depth of discharge. At high rates of discharge, we observe the formation of copious small particles. At low rates and high depths of discharge, we observe the formation of large toroid particles (see Figure 1). From X-ray diffraction and selected area electron diffraction, we determined that these are Li_2O_2 particles with predominantly (0001) surfaces.

Additionally, we have studied the stability of these carbon nanotube electrodes in a lithium-air cell. We observed higher charging overpotentials as the cycle number increased. Using X-ray absorption near edge spectroscopy, we determined that Li_2CO_3 formed in increasing amounts upon cycling at the interface between lithium peroxide and the carbon nanotube. We attribute poor cycling performance and higher charge overpotentials to this Li_2CO_3 formation. We also observe the formation of LiOH in dimethyl sulfoxide solvent. We are currently working on comparative studies of different electrolyte and electrode materials to resolve these issues.



▲ Figure 1: TEM micrographs of Li2O2 formation at a) low rates and b) high rates.

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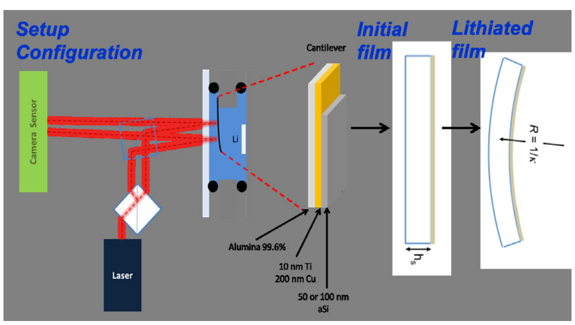
In situ Stress Measurements of Silicon Anodes in Lithium-ion Batteries

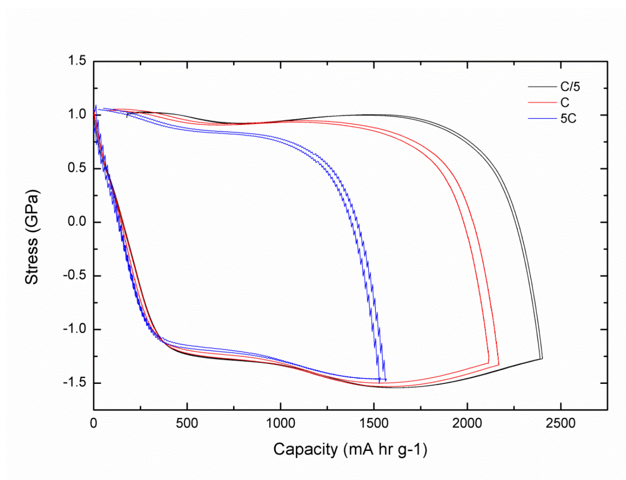
A. Al-Obeidi, S.T. Boles, R. Moenig, C.V. Thompson
Sponsorship: SMART

There is increasing interest in developing autonomous microsystems, which integrate energy harvesting, energy storage, and power management in one package. Ideally suited for these applications are lithium-ion batteries with their relatively high energy-storage capacities. For the anode, we have investigated silicon, which offers among the highest known lithium capacity. However, accessing these large capacities results in large volume changes, rendering fully dense films or substrates unusable. To better understand the forces involved during cycling, *In situ* measurements of stress in silicon thin films (50 nm) were conducted using a home-built system.

During cycling, the silicon film expands during lithiation and contracts during delithiation. Using a cantilever setup, volume change in silicon results in cantilever bending, which can be quantified by laser deflection off the back of the cantilever (see Figure 1). *In situ* stress measurements reveal that during lithiation, there is a linear increase in stress (elastic regime) to ~ 1.2 GPa compressive. The stress then remains at about 1.2 GPa (plastic regime) to the end of lithiation. Upon delithiation, there is elastic unloading to 1 GPa tensile, and remains at that stress until the completion of delithiation. By monitoring the stress evolution of silicon electrodes during cycling allows one to probe the relationship between electrochemistry and mechanical behavior. This information provides new insight into designing nanostructured silicon films that minimize the stress during cycling.



▲Figure 1: *In situ* stress measurement setup to monitor the stress evolution of a 50-nm Si film during cycling.



▲Figure 2: Evolution of stress as a function of anode capacity at different cycling rates.

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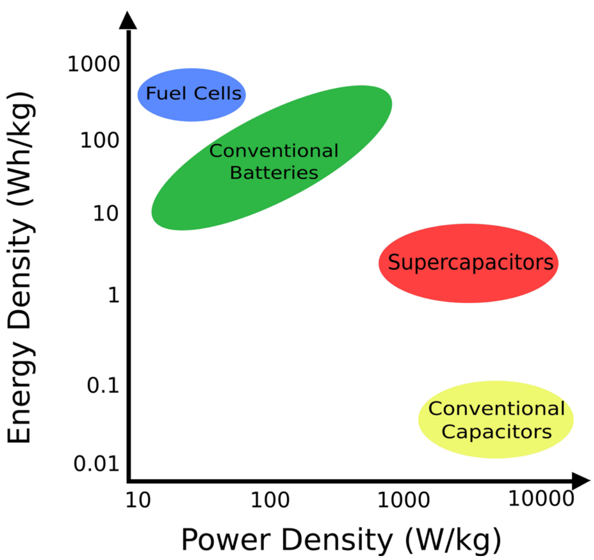
Graphene-based Supercapacitors for High-performance Energy Storage

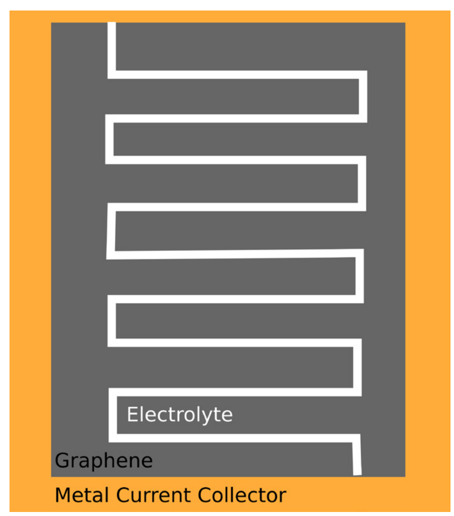
M. Aby, T. Palacios
Sponsorship: MIT-MTL Center for Graphene Devices and 2D Systems

As micro- and nanoscale devices get increasingly smaller and more advanced, supplying sufficient energy to them when needed is becoming more important than ever. Technology for energy storage has lagged behind other nanotechnologies, resulting in devices limited by the size and capabilities of their attached batteries. Electrochemical double-layer capacitors (EDLCs/supercapacitors) and relatively new carbon-based materials such as graphene offer the potential for large capacitances per unit volume, high specific power, high cycle life, rapid charge/discharge times, high efficiency, good performance in extreme conditions, and higher energy densities than conventional capacitors (see Figure 1). The supercapacitor structure allows for two layers of charge separation, one at each electrode, and its performance depends heavily on the choice of materials and on the amount of electrode surface area in contact with the electrolyte. Carbon-based materials, and graphene in particular, are especially promising for use as capacitor electrodes because of their high surface-area-to-volume and -weight ratios. Some work has already been done demonstrating the great promise of these graphene-based supercapacitors, but challenges still exist to scaling up their capacity and their production.

Our work aims to demonstrate supercapacitors based on graphene that are scaleable to energy-relevant dimensions for use in other devices and that can be produced relatively simply and inexpensively. We are currently exploring different ways of producing graphene-based supercapacitors by varying the type of graphene (chemical vapor deposition, reduced graphene-oxide, flakes, aerogels), the electrolyte material, the production method and the capacitor shape. Figure 2 shows an example of a typical supercapacitor structure, where the interlocked "fingers" of graphene electrodes are used to increase the surface area of graphene in contact with the electrolyte. This exploratory work will hopefully serve as a basis for future work in fabricating and scaling such devices and in integrating them with other technologies.



▲Figure 1: Energy density vs. power density comparison for energy storage devices. It is hoped that supercapacitors can eventually outperform current devices in both energy and power density.



▲Figure 2: Structure of an in-plane, graphene-based supercapacitor with solid-state gel-electrolyte. The electrolyte used is (PVA)-H_3PO_4.

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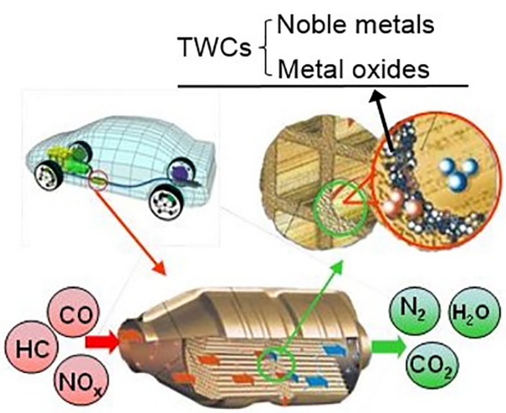
Catalytic Oxygen Storage Materials

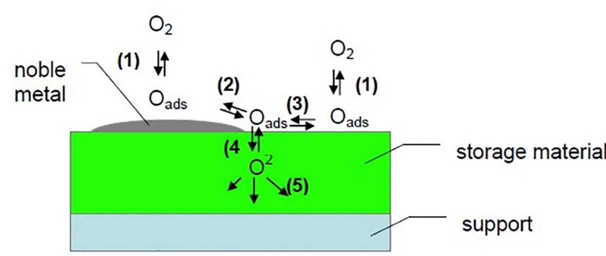
Y. Cao, D. Chen, H. Saltzburg, S.R. Bishop, H.L. Tuller
Sponsorship: Department of Energy, Basic Energy Science

The combustion of fossil fuels, essential for electricity generation and vehicular propulsion, is generally incomplete, leading to harmful NO_x, CO, and unburned hydrocarbon emissions. Progress in minimizing such emissions has relied on the operation of "three way catalysts" (TWCs, see Figure 1) which utilize a combination of noble metals and metal oxides with the ability to take up or release oxygen for reduction/oxidation of pollutants (NO_x to N_2 and CO & HC to CO_2 and H_2O, respectively). In this project, we investigate the rate at which oxygen storage materials (OSM, typically $Ce_xZr_{1-x}O_{2-\delta}$ and $Pr_xCe_{1-x}O_{2-\delta}$) exchange oxygen with the atmosphere and the magnitude of oxygen that they store with the aid of geometrically well-defined thin film and bulk structures (see Figure 2). We use impedance spectroscopy, Kelvin probe, thermogravimetry, Raman scattering, and electrical conductivity measurement methods to determine electrochemical performance and oxygen storage capabilities. Based on the measurements of oxygen non-stoichiometry and electrical conductivity, we have developed defect equilibrium models.

Possible interactions between the noble metals and the metal oxide components in TWCs influence the catalytic activity. The role of the state of OSM and its interactions with catalytic metals will be studied by analyzing *in situ* electrical conductivity simultaneously with catalytic reactions. The electrical properties, when correlated to actual TWC performance, using a differential flow reactor, will allow for a more detailed understanding of performance criteria.



▲ Figure 1: Application of TWCs in the automobile.



▲ Figure 2: Microscopic processes involved in oxygen storage: oxygen ad- and desorption (1), spillover and backspillover (2), surface diffusion between surface exchange and adsorption sites (3), oxygen incorporation and release (4), and bulk diffusion (5).

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Influence of Strain on Ionic Conduction

S.N. Cook, H.L. Tuller
Sponsors: Department of Energy, Basic Energy Science

Ionic conduction in ceramic materials plays a vital role in a wide range of devices in fields as diverse as clean energy generation and healthcare. Device implementation is often hindered by the low inherent conduction levels present at low temperatures, even in highly chemically optimized materials, a side effect of having to move large ions through a relatively static solid state material. Recent reports suggest that ionic conduction properties can be significantly enhanced through the fabrication of nanostructures. The interpretation of these results remains controversial, but it has been suggested that strain due to lattice mismatch at heterointerfaces has the greatest effect. This phenomenon has never been directly measured due to the great deal of complexity inherent in thin film nanostructures.

In this project we take an alternative approach to the isolation of this effect through the direct mechanical manipulation of the strain state of fast ion conducting ceramics using a novel experimental setup. Developing a full understanding of the relationship between strain and ionic conduction will not only allow for devices that take advantage of this relationship, one potential application being high temperature strain gauges, but also allow developments in current device technology where material optimization takes into account chemistry and microstructure, as well as the strain state, facilitating superior device performance and increasing operating condition range.

Development of Reversible Solid Oxide Cells: A Search for New Electrode Materials

C.S. Kim, H.L. Tuller
Sponsorship: Skolkovo Foundation

Recent technological advances in photovoltaic cells have enabled efficient conversion of solar energy to electricity at low cost. However, solar radiation varies throughout the day, and excess electricity generated during the daytime is lost if not used. Electrolysis cells can convert the excess electrical energy into chemical fuels via electrolyzing water (H_2O) or carbon dioxide (CO_2) to hydrogen (H_2) or carbon monoxide (CO), respectively. The excess energy stored in chemical form can be converted back to electricity by operating solid oxide fuel cells (SOFCs). Conversion of energy into chemical fuels via electrolysis is advantageous over storage in batteries given potentially reduced costs and the high energy density of chemical fuels. A reversible SOFC can operate as an electrolysis cell during the day, and as a fuel cell at night. It has been shown that typical SOFCs can be efficiently operated as both fuel cells and electrolysis cells, but with significant degradation. This degradation is mainly due to the redox instability of the electrodes in reverse operating mode. While symmetric solid oxide cells with redox stable electrodes have been investigated, their performance was substantially lower than the state-of-the-art SOFCs. In this project, we are investigating new redox stable electrode materials with high mixed (electrical and ionic) conductivity in both highly oxidizing and reducing conditions. Half-cells and symmetric cells are fabricated by depositing the new electrode material onto an electrolyte by pulsed laser deposition. Structural analysis of the new material is conducted by high-resolution X-ray diffraction and electro-chemical properties are measured by means of impedance spectroscopy in differing temperatures and atmospheres (pO_2 and pH_2).

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Investigation of Fuel Cell Cathode Performance in Solid Oxide Fuel Cells: Application of Model Thin Film Structures

J.J. Kim, D. Chen, N. Perry, N. Thompson, S.R. Bishop, H.L. Tuller
Sponsorship: Department of Energy

Understanding the reaction kinetics controlling the oxygen reduction reaction (ORR) between the gas phase and the oxide lattice in solid oxide fuel cell (SOFC) cathodes is considered to be critical for achieving improved device performance, especially at reduced operating temperatures. Although numerous research activities have been focused on elucidating the electrode reaction mechanisms, their conclusions remain unsatisfactory and controversial. The ORR at mixed conducting oxide thin film cathodes consists of oxygen adsorption, dissociation, charge-transfer, and incorporation steps. The kinetic parameters associated with the overall ORR, such as the diffusion coefficient (D) and surface exchange coefficient (k), are strongly influenced by the oxygen nonstoichiometry, δ, of the oxide. Because many advanced oxide materials used in SOFC experience significant changes in δ during operation at elevated temperatures and under reducing/oxidizing conditions, the ability to diagnose a material's behavior in operando is therefore important.

Our group recently demonstrated that δ in $Pr_{0.1}Ce_{0.9}O_{2-\delta}$ (10 PCO) thin films could be reliably derived by utilizing chemical capacitance extracted from electrochemical impedance spectroscopy (EIS) measurements. Furthermore, we introduced a non-contact optical means for *in situ* recording of transient redox kinetics, as well as the equilibrium Pr oxidation state and, in turn, δ in 10 PCO thin films, by monitoring the change in absorption spectra upon change in pO_2 or temperature. In this study, we are investigating cathode kinetics and nonstoichiometry of two model oxide thin films; $Ba_xSr_{1-x}Ti_{1-y}Fe_yO_{3-y/2+\delta}$ (BSTF) and $Pr_xCe_{1-x}O_{2-\delta}$ (PCO) by simultaneously utilizing *in situ* optical absorption spectroscopy and EIS as a function of temperature, pO_2 and electrical potential. We are also investigating changes in surface chemistry and their impact on electrode impedance by atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), and low-energy ion scattering spectroscopy (LEIS).

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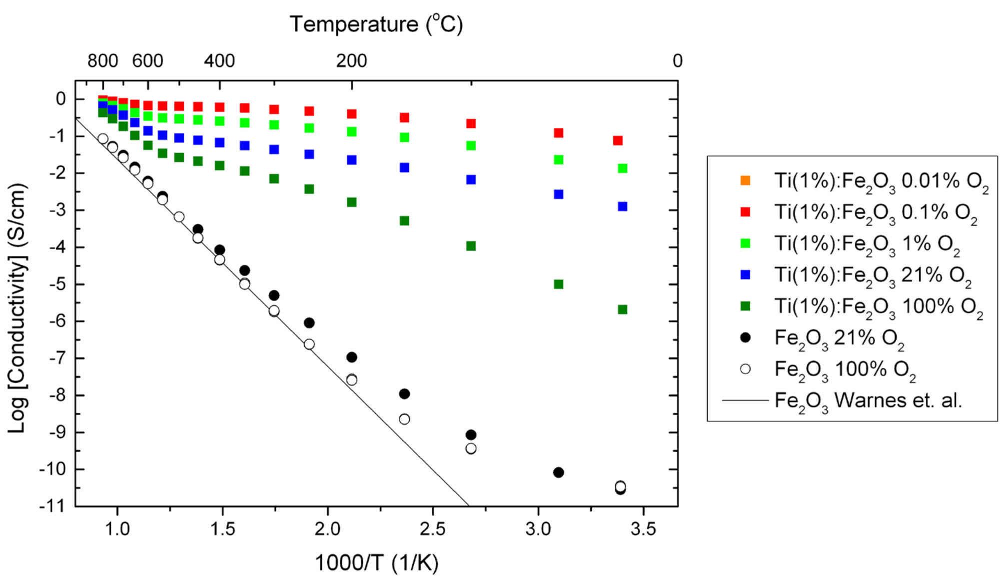
Direct Solar-to-hydrogen Conversion: Low-cost Photoelectrodes

J. Engel, H.L. Tuller, in collaboration with R. van de Krol
Sponsorship: MIT Energy Initiative

With continuously growing energy demands, alternative emission-free solar energy solutions become ever more attractive. However, to achieve sustainability, efficient conversion and storage of solar energy is imperative. Photoelectrolysis harnesses solar energy to evolve hydrogen and oxygen from water, thereby enabling energy storage via chemical means. In this work, we investigate photoelectrodes that offer high conversion efficiency, long-term stability, and low cost,. The focus is on semiconducting metal oxides, in which the energy bands, the defect, and microstructures are tuned to optimize optical absorption, charge transport, and reduce overpotentials. For high efficiency, transition metal-based oxidation catalysts are implemented at the photoelectrode.

Hematite, or α-Fe_2O_3, has emerged as a highly promising photoanode candidate for photoelectrochemical cells. While significant improvements in its performance have recently been achieved, the reason that the maximum photocurrents remain well below their theoretical predictions remains unclear. We report a detailed correlation between the electrical conductivity of undoped and 1 atom% Ti doped hematite and their annealing conditions (varying temperature and partial pressure of oxygen). Hematite thin films grown by pulsed laser deposition onto sapphire single crystals are evaluated by impedance spectroscopy. Hematite's room temperature conductivity can be increased from ~10^{-11} S/cm for undoped films by as much as nine orders of magnitude by doping with the Ti donor. Furthermore, by controlling the non-stoichiometry of Ti-doped hematite, one can tune its conductivity by up to five orders of magnitude. Depending on processing conditions, donor dopants in hematite may be compensated for largely by electrons or by ionic defects (Fe vacancies). We derive a defect model to explain this phenomenon. These results highlight the importance of carefully controlling photoanode processing conditions, even when operating within the material's extrinsic dopant regime, and more generally, provide a model for the electronic properties of semiconducting metal oxide photoanodes.



▲ Figure 1: Conductivity of Ti doped and undoped α-Fe_2O_3 as a function of temperature at different pO_2s.

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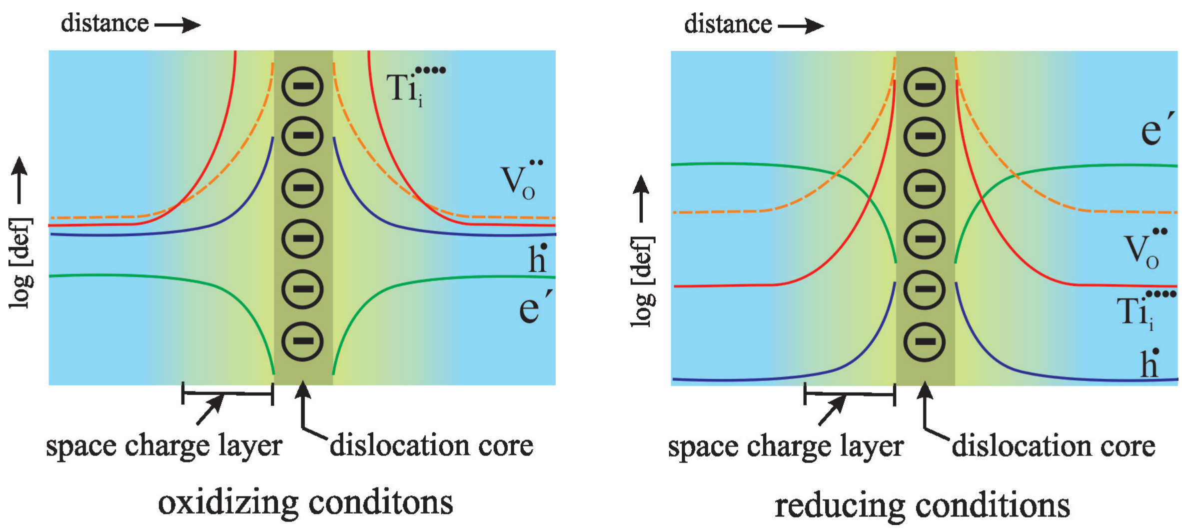
Influence of Mechanical and Electrical Effects on Ionic and Electronic Defect Transport

K.K. Adepalli, B. Yildiz, H.L. Tuller
Sponsorship: Basic Energy Sciences, Department of Energy; MIT Center for Materials Science and Engineering, National Science Foundation

Defects are essential for charge and mass transport in ionic solids. Altering the defect concentration and/or the charge states therefore leads to modification of the transport properties in ionic solids. Hence, aliovalent doping and morphology (grain boundary and/or nano-size effects) engineering have been the topic of interest for several decades. In addition to these zero-dimensional point defects (dopants) and two-dimensional morphological defects (grain boundaries), one-dimensional line defects (or dislocations) can also potentially influence transport properties. Interestingly, a fundamental understanding of the effect of these defects on charge transport is still lacking in ionic solids. A key feature of dislocations in ionic solids is that they are often charged due to a lower defect formation energy and a higher defect segregation driving force in comparison to the bulk. Dislocations also result in a variation in local strain state (compressive or tensile) that can influence defect mobility. Due to excess charge on the dislocation core and the adjacent defect redistribution (space charge zones, see Figure 1) and the locally strained lattice, these defect sites are believed to be electrochemically active centers for catalysis and resistive switching memory behavior through the preferential formation of highly conductive filaments along dislocations. With the understanding of point defect transport as the common thread, this project focuses on these two emerging fields. The project incorporates the investigation of dislocation effects (by mechanical means) on catalytic properties of solid oxide fuel cell cathode materials. In addition, electric field effects on point defect transport will be investigated, not only to find new memristor devices based on electrochemical switching, but also to investigate the underlying mechanism of charge transfer under an applied electric field.



▲ Figure 1: Schematic representation of dislocation core charge and adjacent defect redistribution in space charge regions in TiO_2 under oxidizing and reducing conditions.

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Ionic Conduction Studies in TlBr Radiation Detector Materials

S.N. Cook, S.R. Bishop, H.L. Tuller in collaboration with S. Payne, A. Conway, K. Shah
Sponsors: Domestic Nuclear Detection Office, Lawrence Livermore National Laboratory, Radiation Monitoring Devices, Inc.

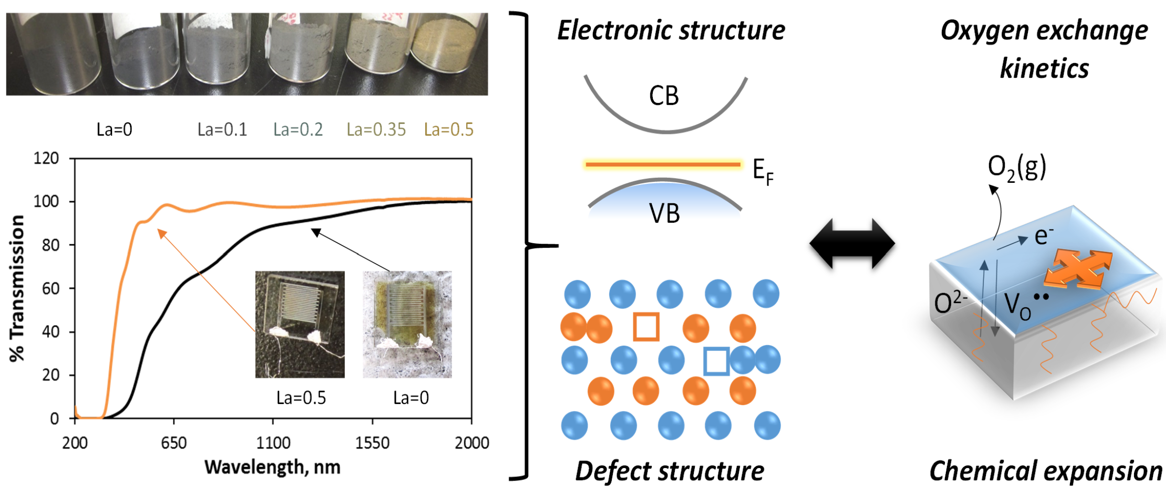
Detection of high-energy radiation (e.g., γ-rays) is key in nuclear non-proliferation strategies. When a wide-band gap semiconductor detector intercepts a γ-ray, electron-hole pairs are formed, resulting in an increase in electrical conductivity, facilitating their detection. As in any photodetecting device, sensitivity is maximized if the conductivity in the non-illuminated (dark) state is very low. While current semiconductor-based technologies require cooling to very low temperatures, adding to cost and reducing portability, TlBr is an attractive detector material given its low room temperature dark conductivity, as well as its high mass density, leading to high radiation absorption. In TlBr the dominant conduction mechanisms, when non-illuminated, are ionic in nature. Their minimization is therefore valuable to produce higher performance detectors. In this project, we characterize the ionic conduction properties of TlBr, dopant association and exsolution using impedance spectroscopy. Through doping techniques, we have determined that TlBr is primarily a Schottky type ionic conductor, meaning that Tl and Br move through the material by vacancy motion. These measurements have led us to predict a doping strategy to minimize dark conductivity. Further limiting device adoption are short operating times of less than 100 days. We are currently implementing the detailed defect model that we have established by investigating the origin of this long-term performance degradation and its relation to electrode chemistry.

Fundamental Studies of Oxygen Exchange and Associated Expansion in Solid Oxide Fuel Cell Cathodes

N.H. Perry, J.J. Kim, D. Marrocchelli, J.E. Thomas, S.R. Bishop, H.L. Tuller in collaboration with B. Yildiz, D. Pergolesi
Sponsorship: Department of Energy

To lower the cost of solid oxide fuel cells (SOFCs), both the low-temperature efficiency and long-term durability need to be improved. Fundamental studies of how fuel cell materials "breathe" oxygen under operating conditions can address these dual needs, since: 1) sluggish oxygen incorporation at the cathode dominates SOFC efficiency losses at low temperatures and 2) chemical expansion during oxygen loss from the oxide can result in catastrophic mechanical failure of the cell. Our recent review article highlights the widespread presence of chemical expansion and its consequences across a number of energy conversion and storage devices.

In this work we experimentally and theoretically investigate cathode systems with model geometries (controlled active surface area and diffusion lengths of thin films) and model chemistries (tailored electronic structure, crystal structure, and defect chemistry) to isolate underlying factors controlling the oxygen exchange and expansion behavior. Previous work on fluorite-structured electrodes is being extended to the perovskite families (Sr,Ba,Ca,La)(Ti,Fe,Co)$O_{3-\delta}$, and (La,Sr)(Ga,Ni)$O_{3-\delta}$, using advanced *in situ* X-ray diffraction, optical absorption, thermogravimetric analysis, dilatometry, electrochemical impedance spectroscopy techniques, defect thermodynamic modeling, and density functional theory calculations. Using this approach we have experimentally confirmed our previous theoretical calculations demonstrating the important role of charge localization in controlling chemical expansion behavior. We have also identified how chemical substitution affects defect chemistry, electronic structure, and corresponding oxygen exchange rate at the cathode surface. This performance over time is being correlated to changes in surface chemistry, studied by high-resolution energy dispersive spectroscopy of thin film cathodes and low-energy ion scattering. Such information is key to the design of both efficient and durable fuel cell electrodes.



▲ Figure 1: Optical properties (left) serve as markers for electronic and defect structures, to determine their relationship to the oxygen exchange kinetics and corresponding expansion of solid oxide fuel cell cathodes.

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A Universal Village: Our Desired Living Conditions

Y. Fang, B.K.P. Horn, I. Masaki
Sponsorship: Intelligent Transportation Research Center, MTL

The worldwide trend of urbanization makes more people live a "modern lifestyle" that revolves around vehicles and consumption of natural resources faster than the rest of the world, which intensifies the environmental and sustainability crisis. The current society is facing serious challenges due to fast urbanization, limited resources, and the increasing population of senior citizens. While there have been efforts to address challenges to humanity up now, many current designs are availability-based, technique-oriented, and bottom-up schemes that focus on individual elements. The whole living environment lacks a coordinated and systematic design and runs into new challenges including new security, safety, and privacy concerns plus environmental and sustainability problems. Right now, transportation is the second cause, after electricity generation, of the CO_2 problem. Instead of passively responding to different emerging problems with temporary solutions, people in different fields should work together to find systematic long-term solutions for the future.

The Universal Village (UV) is a new concept proposed by MIT Universal Village Program, an expanded and advanced version of Smart Cities that pursues human-nature harmony through the wise use of technologies. The concept is named for two considerations. First, "smart" is not the final objective. Instead, the desired future society should follow laws of the universe and protect the environment and ecosystem. Otherwise, Mother Nature suffers and we humans suffer eventually. Second, cities might not be the only living environment in our future. Universal Villages are multi-functional, multi-format, and sustainable communities that incorporate the ideal mixture of cities and suburban areas.

The development of the UV follows a need-based, human-nature-oriented, and systematic top-down design approach. The UV calls for a collective effort from multidisciplinary fields and new innovative technologies that would change our future lives and improve human-nature harmony in the long run. The UV is expected to provide sustainable happiness to residents, so we must understand humans' need in depth before developing intelligent technologies to improve comfort, convenience, and efficiency for human beings. We expect to develop both sensing technologies to understand humans' behavior and cities' activities and integrated system solutions to provide intelligent reactions at various levels in cities. A better understanding of family routines and human activities in buildings will benefit the development of intelligent safety monitoring and intelligent energy saving. Real-time detection of traffic situations will allow control centers to respond to accidents faster than before. Intelligent health monitoring systems, distributed medical treatment, and tele-healthcare can provide early warnings before people physically feel sick and diseases spread widely. We aim to propose new lifestyles that are in harmony with nature and need collective efforts from multi-disciplinary research. The major themes include the following:

- Innovative technologies that support new lifestyles for future transportation, city management, healthcare, etc.
- Integrated solutions to urgent and long-term challenges of safety, security, privacy, climate changes, etc.
- Environmentally friendly energy sources such as solar power, bio-energy, supergrids, wireless charging, etc., and
- Environmentally friendly new materials, e.g., pesticides/fertilizers/etc. without chemical contamination, and decomposable utensils, tools, etc. without extra burdens for garbage disposal.

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Photonics, Optoelectronics

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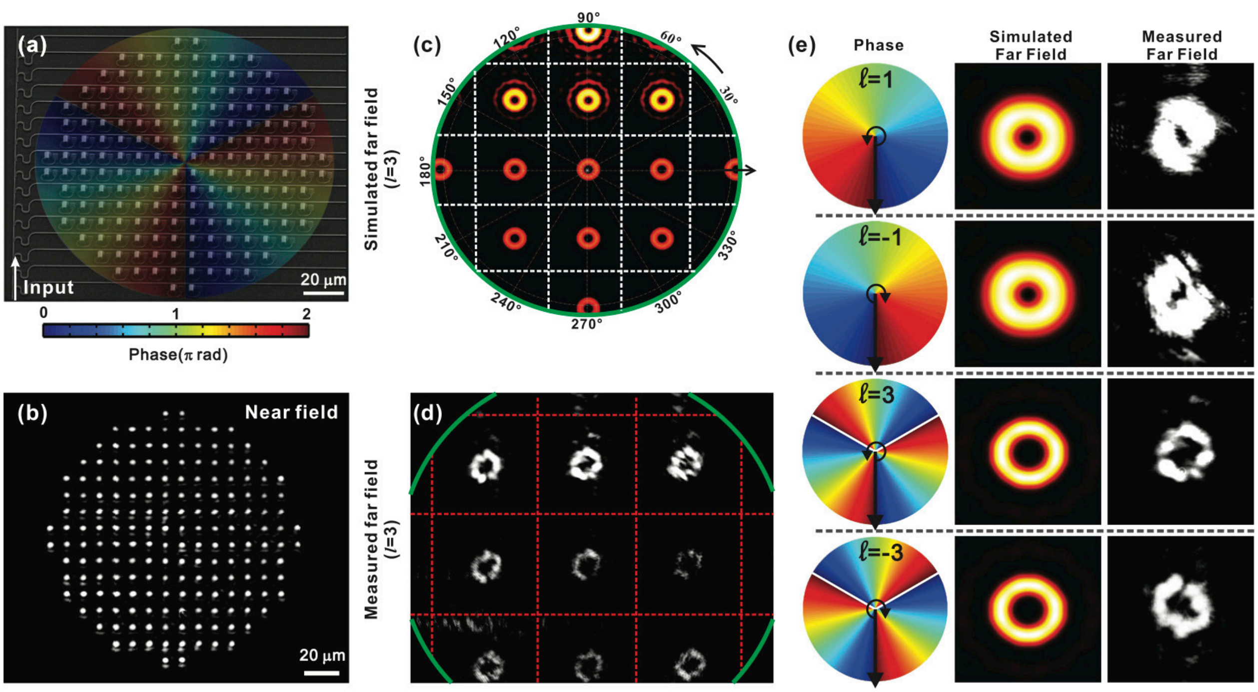
Generating Optical Orbital Angular Momentum with Silicon Photonic Circuits

J. Sun, M. Moresco, M.R. Watts
Sponsorship: DARPA under E-PHI projects, Grant HR0011-12-2-0007

Optical vortices, whose phase profile has an angular dependence $\exp(j \cdot l \cdot \theta)$, carry an orbital angular momentum (OAM) $l\hbar$ per photon where θ is the azimuthal angle with respect to the beam axis and the integer l represents different OAM states. Besides its application in quantum information for high-dimensional entanglement, OAM has recently drawn significant attention for a wide range of classical applications such as high-capacity optical communications and optical micromanipulations. While free-space optical components such as spiral phase plates and spatial light modulators are generally used to generate OAM beams, the alternative integrated solutions are of great interest for device miniaturization, enhanced stability, and the possibility of being integrated with other on-chip photonic components and functionalities. Here we present a silicon photonic integrated circuit to create optical beams with different OAM states.

Figure 1(a) shows a scanning-electron micrograph (SEM) of the fabricated silicon PIC, which is essentially an optical phased array in which the emitting phase of each optical antenna depends on its azimuthal angle θ, as shown in Figure 1(a) where a phase profile $\exp(j \cdot l \cdot \theta)$ is coded to generate an OAM with l=3. Unlike conventional phased arrays where a rectangular layout is used, the 180 optical antennas here are placed within a circle to reflect the circular symmetry of the OAM beam. Figure 1(b) shows the measured near field where uniform emission across all of the 180 optical emitters was observed. The measured far field is shown in Figure 1(d), agreeing well with the simulation in Figure 1(c). Multiple interference orders are seen in the far field since the antenna spacing (9µm) is a multiple of the optical wavelength (1.55µm). The multiple OAM beams can be used, for example, to optically trap and rotate multiple particles simultaneously. By coding the array with different phase profiles, optical beams with different OAM states (l=±1 and ±3) were also generated (Figure 3(e)). All of the generated far-field beams have zero intensity in the center, representing a phase singularity, which is the signature of optical vortices.



▲ Figure 1: (a) An SEM of the fabricated integrated photonic circuit coded with angular phase profile to generate OAM with l=3. (b) Measured near-field emission. (c) Simulated and (d) measured far-field pattern with l=3. (e) OAMs with l=±1 and ±3 are generated (only one interference order is shown in the far field).

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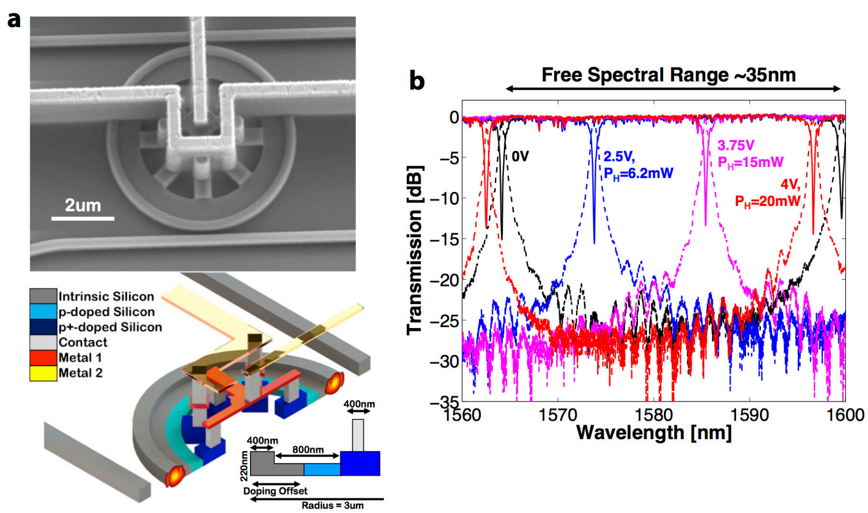
A High-Q Tunable Interior-Ridge Microring Filter

E. Timurdogan, Z. Su, J. Sun, M. Moresco, G. Leake D.D. Coolbaugh, M.R. Watts
Sponsorship: DARPA MTO

Silicon photonics enables wavelength division multiplexed (WDM) networks to be efficiently and cost-effectively implemented on chips with potential for multi-terabit/s communication links. The multiplexing and demultiplexing operations are performed by microring-based filters, which require tight alignment between the laser comb and filter resonances. However, the alignment will be distorted due to wafer-scale dimensional errors and the temperature fluctuations, necessitating high-speed active thermo-optic control of microring filters. The challenge is to implement such control efficiently and rapidly to enable reconfigurable networks as well as track the dynamic processor activity. For this purpose, metal and silicon heaters have been implemented. The metal heaters, buried in or placed over the SiO_2 cladding, achieve the highest temperature change within the metal and not inside the silicon core. This indirect heating method limits the thermal tuning efficiency and speed while increasing thermal crosstalk. On the contrary, the silicon heaters, formed using ion implantation and directly integrated within the silicon microring, enable direct, efficient, and high-speed tuning due to the combination of lower heat capacity and reduced thermal conductance. However, past silicon heater based tunable rings have suffered from increased optical losses due to the coupling geometry.

In this work, we demonstrate an interior-ridge microring resonator with a novel optical and electrical design that eliminates the aforementioned drawbacks of tunable filters with directly integrated silicon heaters (Figure 1-a). The 3-µm radius interior ridge microring resonator demonstrates a quality factor of 1.5×10^5, limited mainly by the line edge roughness, while achieving a low-resistance (1kΩ) integrated silicon heater with a thermal tuning efficiency of 5.5µW/GHz (Figure 1-b). The resonator is used to operate as a 75GHz 3dB bandwidth filter. The filter demonstrates a record low insertion loss <0.05dB, owing to its high internal quality factor, over an uncorrupted 35-nm (4THz) free-spectral range.



▲Figure 1: a- Designed (3D-sketch) and fabricated (scanning-electron-microscopy image) optical tunable silicon modulators are shown to illustrate lossless (no optical overlap to doped regions) single mode operation. Heater is formed within filter using ion implantation (p and p+ doped silicon). b- Integrated optical filter is tuned over entire L-band (1565 nm-1600 nm) with as little as a ~4V drive voltage (20mW heater power).

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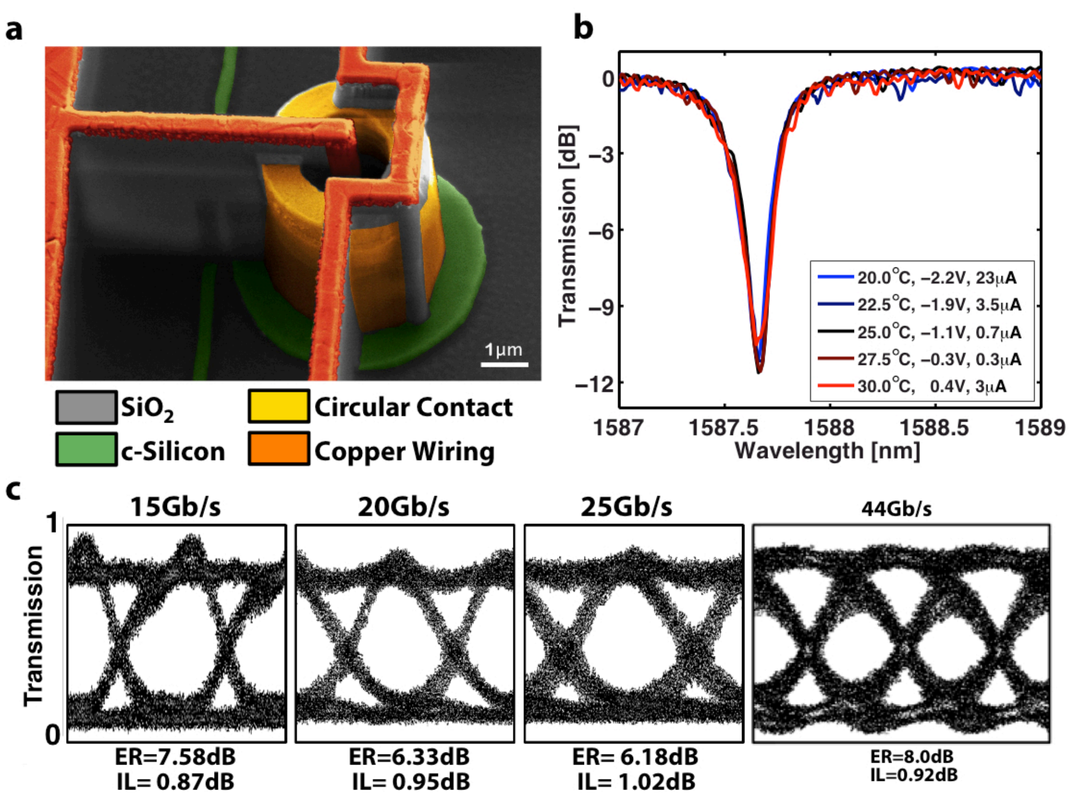
An Ultralow Power Athermal Silicon Modulator

E. Timurdogan, C. Sorace-Agaskar, J. Sun, E. Hosseini, A. Biberman, M.R. Watts
Sponsorship: DARPA MTO

On- and off-chip interconnects, traditionally executed using parallel electrical links, are struggling to satisfy the current bandwidth, density, power consumption and cost requirements of the computing and communication industries. These limitations are becoming apparent in rapidly scaling massively parallel computing systems such as data centers for cloud computing and high-performance "supercomputers" used for large-scale scientific computation. Silicon photonics has emerged as the leading candidate for implementing ultralow power communication networks in high-performance computers, yet current components (lasers, modulators, filters, and detectors) consume too much power for the high-speed femtojoule-class links that ultimately will be required. In this work, we demonstrate and characterize the first modulator to achieve simultaneous high-speed (25 Gb/s), low-voltage (0.5 V_{PP}) and efficient 0.9 fJ per bit error-free operation. This low-energy high-speed operation is enabled by a record electro-optic response, obtained in a vertical p–n junction device that at 250 pm/V (30 GHz/V) is up to 10 times larger than prior demonstrations. In addition, this record electro-optic response is used to compensate for thermal drift over a 7.5° C temperature range with little additional energy consumption (0.24 fJ per bit for a total energy consumption below 1.03 J per bit). The combined results (see Figure 1) of highly efficient modulation and electro-optic thermal compensation represent a new paradigm in modulator development and a major step towards single-digit femtojoule-class communications.



▲ Figure 1: a- Scanning-electron-microscopy image of optical microdisk modulator illustrates circular contacts and short interconnects. b- Athermal operation over 10°C temperature range is realized by changing only modulator DC bias (consuming <1fJ/bit tuning energy). c- The 15- 20- and 25Gb/s transmissions from the optical modulator are taken from a digital communication analyzer, consuming only <1fJ/bit modulation energy. The 44-Gb/s transmission of same optical modulator was possible at higher modulation energy.

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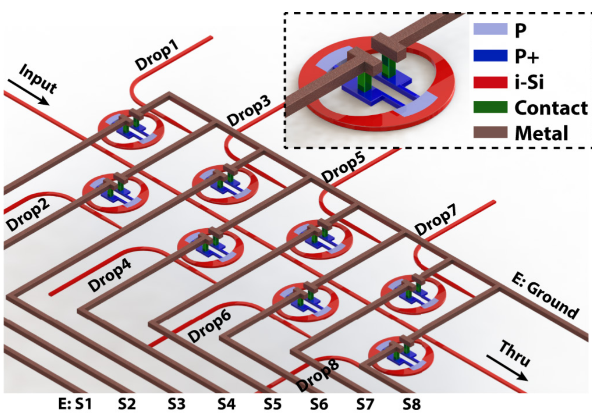
On-chip Wavelength Selective Power Splitter

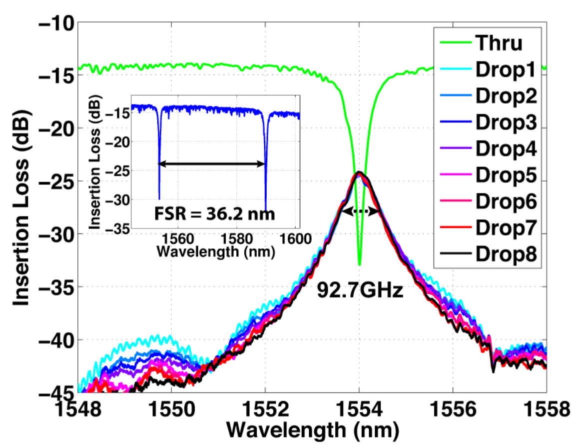
Z. Su, M. Cherchi, E. Timurdogan, J. Sun, M. Moresco, G. Leake, D. Coolbaugh, M.R. Watts
Sponsorship: DARPA MTO

With the scaling of chip multicore microprocessor systems, communications between the cores on-chip and to memory-systems off-chip have become the limiting factor in system performance. Integrated photonics provide an alternative solution to both on- and off-chip communications. Among all of the on-chip optical network topologies, the bus-based broadcasting topology, the most widely used network topology in electronics, has advantages in simplicity, flexibility, and scalability. With integrated photonic devices, bus topologies can be implemented by cascaded power splitters connected to multiprocessors. However, to make full use of wavelength division multiplexing (WDM), wavelength selectivity needs to be incorporated into optical broadcasting system. Previously, single large radius rings with multiple drop ports have been utilized to act as a power divider. However, the limited free spectral range (FSR) and resulting bandwidth of this approach make it incompatible with data- and telecom communications. To overcome this limitation, we propose a new optical broadcasting system based on small radius ring resonators to enable large FSRs and resulting optical bandwidth in the on-chip network.

Here, we introduce a new wavelength-selective on-chip optical broadcasting system based on integrated small-radius tunable resonant filters that offer high tuning efficiency and a large FSR to support additional wavelength channels. The demonstrated 1-by-8 broadcasting system shows an average 3-dB bandwidth of 92.7GHz with a standard deviation of only 3.7GHz, capable of handling high-speed data for communication purpose. The aggregate excess loss of the parallel drop is only 1.1dB with an optical power variation of only 0.11dB between drops. This wavelength-selective parallel drop enables immediate applications such as on-chip optical broadcasting and high-sensitivity transmitters and receivers in on-chip WDM communication networks.



▲Figure 1: Schematic of wavelength selective power splitter. All the rings are designed to be identical to each other with different coupling to bus and drop waveguide. Inset: schematic of the tunable adiabatic microring filter.



▲Figure 2: Transmission spectra of the wavelength selective power splitter after thermal tuning. Inset: spectral response of the device, showing an uncorrupted 36.2-nm FSR.

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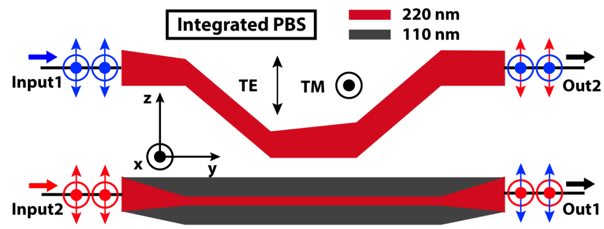
Mode-evolution-based Four-port Polarizing Beam Splitter

Z. Su, E. Timurdogan, E. Hosseini, J. Sun, G. Leake, D. Coolbaugh, M.R. Watts
Sponsorship: DARPA MTO

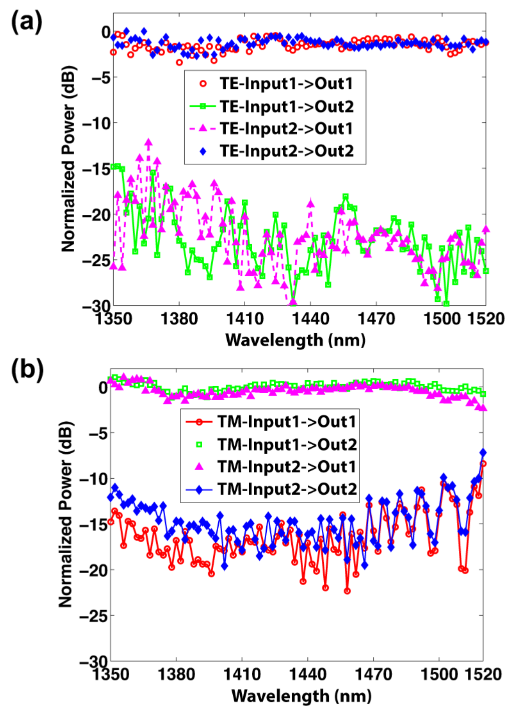
Integrated silicon photonics, which offers single-mode operation, unprecedented bandwidth density, and compactness, is growing rapidly with the exponentially increasing demand for bandwidth with the Internet and within the data centers. While communications are the main driving force for silicon photonics, the resulting silicon photonics platforms can be applied to numerous problems, ranging from sensing to microwave photonics and quantum optics, offering degrees of performance unachievable with their free-space counterparts. The general applicability of the platform is determined by how extensive the component libraries are and how easily free-space optical systems can be implemented. However, among the components demonstrated previously, an exact correspondence to a free-space polarizing beam splitter (PBS), which has four ports (2-input 2-output), is still missing.

On account of the polarization dependence caused by the use of high-index contrast materials such as silicon and silicon-nitride (Si_3N_4) within silicon photonics, polarization components were developed and realized early on to enable polarization independent operations. Yet, while components such as polarization splitters, polarization rotators and integrated polarization splitter-rotators have been demonstrated on silicon platforms, an on-chip equivalent of a free-space polarizing beam splitter (PBS) has not previously been demonstrated. All "so-called" polarizing beam splitters demonstrated so far are in themselves polarization splitters, with only one input and two outputs and not true four-port polarizing beam splitters.

We earlier designed and demonstrated a broadband mode-evolution based polarizing beam splitter implemented on a silicon photonics platform and fabricated on a 300-mm silicon-on-insulator (SOI) wafer with 220-nm device layer, using 193-nm optical immersion lithography. The silicon polarizing beam splitter, the first reported fully-functional integrated PBS (2-input and 2-output ports), operates over a 150-nm bandwidth with less than -10-dB crosstalk. Importantly, this device provides a substantial addition to the component library with immediate application to compact on-chip interferometers and quantum information processing.



▲Figure 1: Proposed integrated four-port polarizing beam splitter.



▲Figure 2: (a) Transmission spectra of the fabricated device for TE-input polarization. (b) Transmission spectra of the fabricated device for TM-input polarization.

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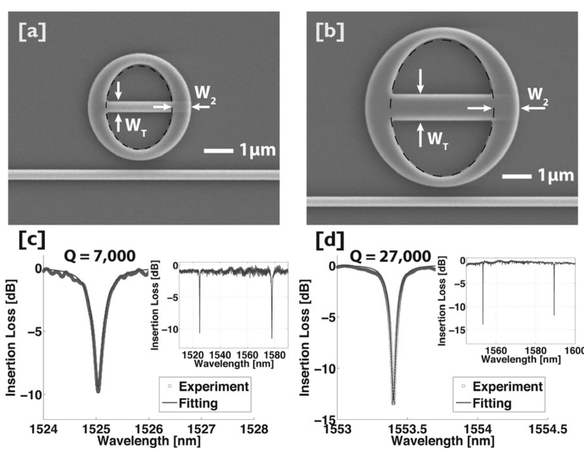
Wafer-Scale Resonance Variation Reduction with Adiabatic Microring Resonators

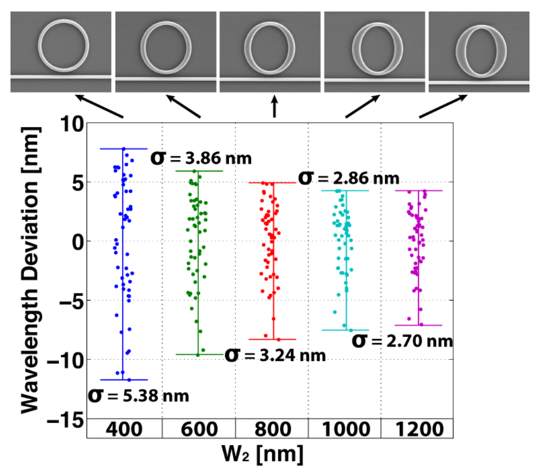
Z. Su, E. Hosseini, E. Timurdogan, J. Sun, G. Leake, D. Coolbaugh, M.R. Watts
Sponsorship: DARPA MTO

Microdisk resonators have been preferred over microrings for applications requiring electrical or mechanical contact to the cavity since the center of the microdisk allows access to the resonator without disrupting the fundamental optical mode. However, microrings are generally preferred for denser wavelength multiplexing (WDM) applications or high order filters due to their large, uncorrupted free spectral ranges (FSRs) that can accommodate more frequency channels on an optical communication line. In general, resonant structures show high sensitivity to wafer-scale variations, which indicates the necessity for active tuning. Therefore, electrically or mechanically contacting these resonators without compromising their quality factors are essential for a number of applications such as electro-optic modulators, tunable filters, and optical sensors, which is, however, nontrivial considering the strong sensitivity of the mode to the shape of the high index resonator. To address those challenges, Watts proposed a new class of microring resonator, the adiabatic microring resonators, to provide low-loss electrical or mechanical contacts to the microring through an adiabatic structure, which has already been applied to modulators, tunable filters, and switches.

Here, we optimize the geometry of adiabatic microring resonators using rigorous 3D finite-difference time-domain (FDTD) simulations, and experimentally demonstrated high-Q (7,000 for a 2-µm-radius and 27,000 for 3-µm-radius) adiabatic microring resonators in the presence of an electrical contact. The experimental results agree well with numerical simulations. Moreover, wafer-scale measurements were performed to analyze the resonant wavelength variations of the adiabatic microring resonators across 54 dies in a 300mm wafer fabricated with advanced CMOS processing techniques. The statistical results show that the wavelength uniformity of the optimized adiabatic microring resonator is twice as good as that of conventional microring resonators.



▲Figure 1: Scanning-electron-microscope (SEM) images of adiabatic microring resonator of (a) 2-µm and (b) 3-µm radius. Transmission spectrum of device of (c) 2-µm radius and (d) 3-µm radius. Insets are the spectra across one whole free spectral range.



▲Figure 2: Top: SEM images of 3-µm radius adiabatic microring resonators with different W2 sizes. From left to right are 400, 600, 800, 1000, 1200 nm. Bottom: Resonant wavelength variations across the wafer for various wider width of the adiabatic microring resonator.

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Integrated $Al_2O_3:Er^{3+}$ Laser in Silicon Nitride Photonics Platform

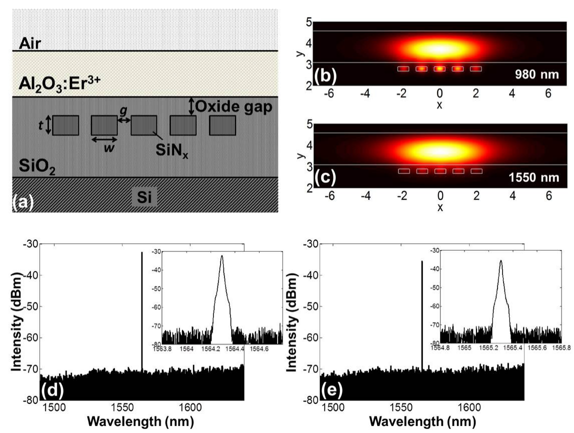
P. Purnawirman, A. Baldycheva, E.S. Hosseini, J.D.B. Bradley, M. Moresco, Z. Su, T. Adam, G. Leake, D. Coolbaugh, M.R. Watts
Sponsorship: DARPA E-Phi program (grant no. HR0011-12-2-0007),Samsung GRO program

Development of lasers on a silicon-compatible platform remains one of the most important pieces in silicon photonics technology. Two most promising candidates for wafer-scale on-chip lasers are III-V hybrid lasers and erbium-doped aluminum oxide ($Al_2O_3:Er_3+$) lasers. $Al_2O_3:Er_3+$ lasers have the advantages of monolithic integration, ultranarrow linewidth, high power, and CMOS compatible. Previously we demonstrated a wafer-scale laser design. In this work, we integrated Al2O3:Er3+ to other photonics devices in a multi-layer photonics platform and demonstrated a temperature-reliable operation.

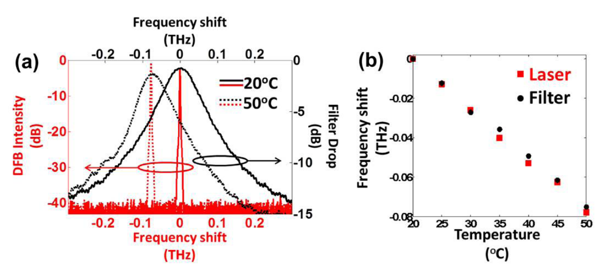
In the previous design, the relatively high index contrast of these materials (nSiN= 1.99 and nAl2O3= 1.65) requires the silicon nitride (Si_3N_4) layer to be very thin, so that the mode overlaps strongly with the gain medium. However, a thin Si_3N_4 layer prevents the layer from being effectively reused to form other important integrated devices such as microring-resonators. We propose a solution by implementing a novel multi-segmented waveguide design in a thick Si_3N_4 to preserve the strong overlap with the gain medium. Additionally, the resulting design facilitates broadband, high confinement, and overlap factors across the entire near-infrared wavelengths (0.9 µm – 2.0 µm), offering potential for amplifier and laser operation across an extremely broad bandwidth, a result that will become of increasing importance as the S, C, and L bands become saturated. Figure 1 illustrates the multi-segmented waveguide design. We obtained $Al_2O_3:Er_3+$ lasers in distributed Bragg reflector (DBR) cavities with maximum output powers of -3.6 dBm and distributed feedback (DFB) cavities with maximum output powers of -7.3 dBm at a wavelength of λ~1565nm.

Further, we propose a temperature-control free optical transceiver operation by using a $Al_2O_3:Er_3+$ laser and Si_3N_4 ring filter. Owing to the small and almost equal thermo-optic coefficient of both the laser and filter, we obtain performance in temperature drift as small as 0.1 GHz/oC. Figure 2 shows the measurement of the laser and filter peak at 20oC and 50oC.

In summary, the progress in $Al_2O_3:Er_3+$ shows the potential of achieving reliable, high-quality laser in silicon photonics. The next step will be to show further integration with electronics component.



▲Figure 1: (a-c) Multi-segmented waveguide design and mode in 980-nm pump and 1550-nm signal. (d-e) DBR and DFB laser measurement in optical spectrum analyzer.



▲Figure 2: Frequency shift measurement of laser and filter at (a) 20°C and 50°C and (b) various temperatures.

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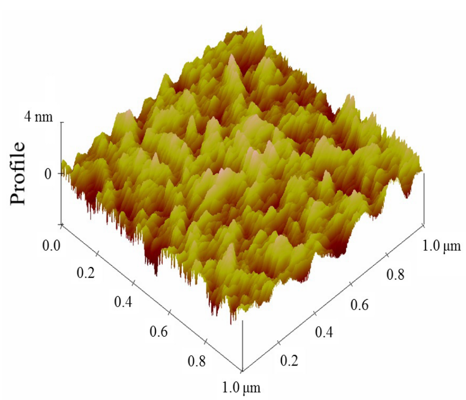
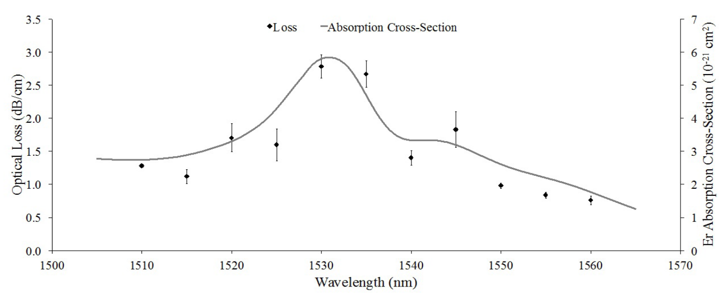
Rare-earth Doped Amorphous Glass Waveguides for Use in Silicon Photonics

E.S. Magden, Purnawirman, C.M. Sorace-Agaskar, E.S. Hosseini, G. Petrich, M. Watts, L. Kolodziejski
Sponsorship: DARPA

Realizing an efficient on-chip optical communications platform requires implementation of photonic devices such as waveguides, couplers, splitters, resonators/filters, switches, amplifiers, and lasers. As a result of the indirect bandgap of silicon, a monolithically integrated light source on silicon remains as one of the big challenges for on-chip photonics today. Due to its compatibility with existing CMOS technologies, the reliability of its reactive sputtering, and the stability of the deposited material, erbium- doped aluminum oxide presents itself as an excellent candidate for gain media in silicon photonics. Here, we demonstrate the deposition of low-loss (0.1 dB/cm) alumina waveguides on silicon at 250 °C using reactive magnetron sputtering. Deposited with a 90 W substrate bias, we obtained a surface roughness of 0.3 nm, as shown in Figure 1, and a refractive index of 1.59 at the communication wavelength of 1535 nm. Using the same sputter technology, we fabricated erbium-doped waveguides whose dopant concentrations are experimentally determined by the ratio of the optical loss to the absorption cross section, as indicated in Figure 2. A concentration of $(1.7 \pm 0.2)\times10^{20}$ cm^{-3} dopant ions has been obtained, after which fluorescent intensity has been shown to quench. At this concentration, we achieved an optical loss of 3 dB/cm at 1535 nm. The flexibility of reactively sputtered aluminum oxide also allows for codopants such as ytterbium, which is used in suppressing laser self-pulsing.



▲Figure 1: Root-mean-square surface roughness of sputtered aluminum oxide is 0.3 nm in a 1-µm^2 area, as measured by atomic force microscopy.



▲Figure 2: Root-mean-square surface roughness of sputtered aluminum oxide is 0.3 nm in a 1 µm^2 area, as measured by atomic force microscopy.

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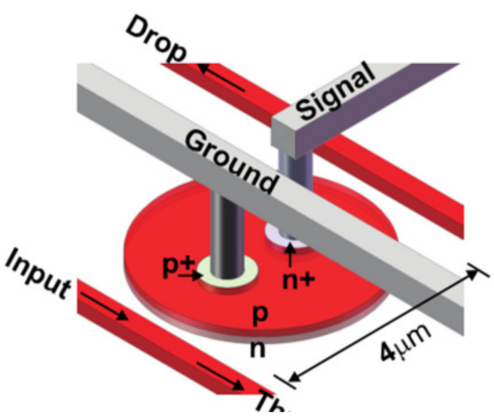
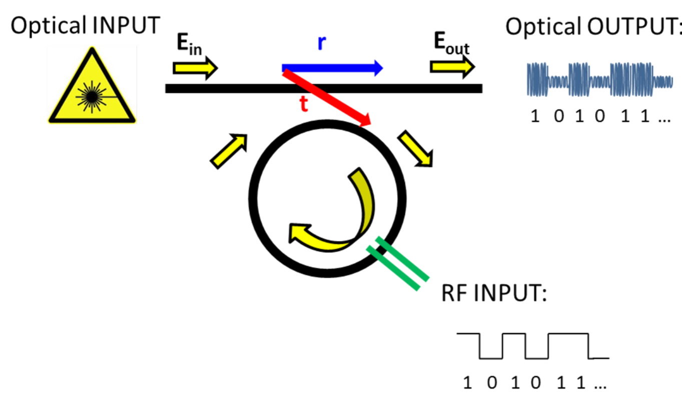
A ModSpec Compact Model of Silicon Optical Modulators

T.-W. Weng, C. Sorace-Agaskar, M. Watts, L. Daniel
Sponsorship: National Science Foundation

Due to the need for high-speed data transmission in data centers and in supercomputers and due to the speed limitations of current electronic devices, silicon photonics has become one of the most promising candidate technologies for the transmission of high volumes of data at low cost. To realize such a goal, we consider silicon optical modulators the key components. They are crucial to introduce wavelength division multiplexing (WDM) techniques, which can successfully expand the capacity of a communication network and therefore increase the aggregate data rate substantially beyond what can be achieved with electrical communications alone. The Photonic Microsystems Group at MIT, led by Professor Michael Watts, has developed a high-speed, very compact and ultralow-power silicon modulator using vertical p-n junction microdisks. Applying a reverse bias across the vertical p-n junction shifts the frequency resonances, and therefore the input 0-1 electrical data can be modulated to 0-1 optical data. The most challenging issue of this device modeling is the multi-physic nature of the electro-to-optical modulation. The scale of the input data is at several GHz, whereas the optical scale is around 193 THz if the 1.55-micrometer carrier wavelength is used. In other words, the output and input make a difference of approximately five orders of magnitude, which may cause simulations to become lengthy and unrealistic. The Computational Prototyping Group at MIT, led by Professor Daniel, has been working tightly with Professors Watts at MIT and Roychowdhury at UC Berkeley on this topic. We are developing a simulation-ready compact model for silicon optical modulators using a model description language called ModSpec Model Specification Language, which support description of compact models from any physical domain and therefore shows promise in solving multiphysics simulation issues.



▲Figure 1: The silicon optical modulator is operated by a compact microdisk resonator.



▲Figure 2: The mechanism of an silicon optical modulator and the multi-physics nature of this device.

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Scalable Integration of Single-photon Detectors on a Photonic Chip

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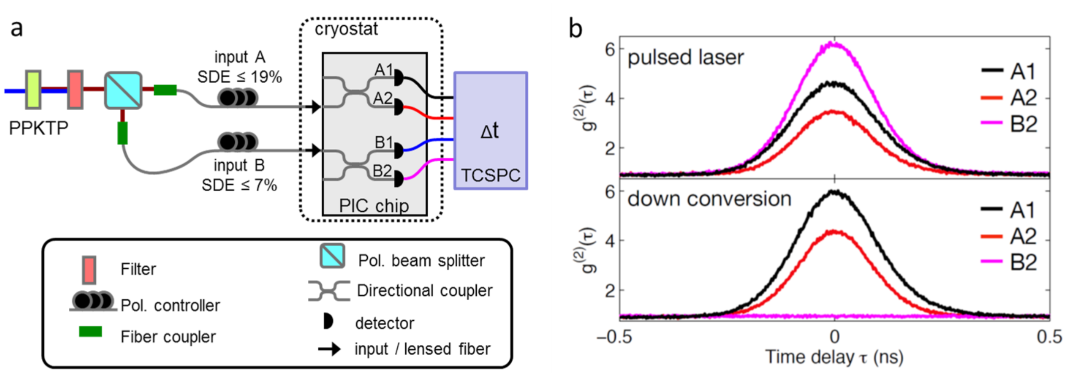
Sponsorship: DARPA, National Science Foundation

Photonic integrated circuits (PICs) enable compact and scalable manipulation of light at the wavelength scale. For quantum-level experiments and optical quantum processors, the integration of single-photon detectors onto photonic chips helps reduce coupling losses. Superconducting nanowire single photon detectors (SNSPDs) are viable candidates, combining near-unity detection efficiency and sub-50-ps timing jitter in the near-infrared. However, to date the integration of more than one SNSPD within the same PIC has yielded sub-0.2% system detection efficiency due to the low nano-fabrication yield of these detectors. We developed a micron-scale flip-chip integration process that allowed us to overcome the yield problem.

We followed a pick-and-place method to overcome the limited detector yield: (1) we fabricated a primary chip with hundreds of SNSPDs on top of micron-scale chiplets, (2) we characterized all detectors to find suitable candidates for integration with PICs, and (3) we removed individual chiplets with detectors on top from the primary chip and transferred them onto the secondary (PIC) chip. We fabricated the SNSPDs, comprising 80-nm-wide ~4-nm-thick niobium nitride nanowires, on top of a sub-300-nm-thick-SiN_x-on-Si substrate and performed a selective silicon etch that resulted in free-standing SiN_x membranes that carried SNSPDs. We used tungsten probes coated with adhesive to transfer the chiplets from the primary chip to the PIC chip. Using this method we assembled a PIC chip, illustrated in Figure 1(a), with four detectors integrated with two on-chip directional couplers.

The high efficiency of our integrated detector system (up to 19% system detection efficiency, including all losses) enabled the on-chip single-photon detection of a non-classical source with multiple detectors within the same photonic circuit. The experimental apparatus is shown in Figure 1(a). Using spontaneous parametric down-conversion (SPDC), we generated time-energy entangled photon pairs with center wavelength at 1560 nm that were highly correlated in time and highly anticorrelated in frequency. We used a polarizing beam splitter to separate signal (sent to PIC input B) and idler photons (sent to PIC input A). With this system we measured the second-order correlation function $g^{(2)}(\tau)$ shown in Figure 1(b). When we measured the time delay τ between a count from B1 and a count from one of the other three detectors, the entangled-photon-pair source resulted, as expected, in coincidence peaks for A1 and A2 but not for B2. As a comparison, a mode-locked pulsed laser yielded coincidence peaks for all detector pairs.



▲Figure 1. (a) Experimental setup for on-chip g(2)(τ) measurement of an entangled-photon source coupled into the photonic circuit via two inputs. The photonic chip was cooled to 3 Kelvin in a closed-cycle cryostat; the lensed fibers were aligned to the polymer couplers *in situ*. (b) Coincidence counts vs. time delay between A1 and B1, B2 and A2 for a pulsed laser and the source shown in (a). The system detection efficiency SDE was 19±2% for input A and 7±1% for input B.

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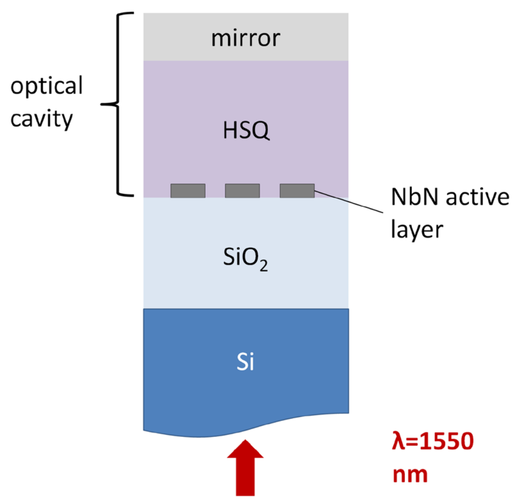
Large area, High-detection Efficiency Superconducting Nanowire Single-photon Detectors

K. Sunter, A. Dane, F. Najafi, K.K. Berggren
Sponsorship: Intelligence Advanced Research Projects Activity (IARPA)/AFRL

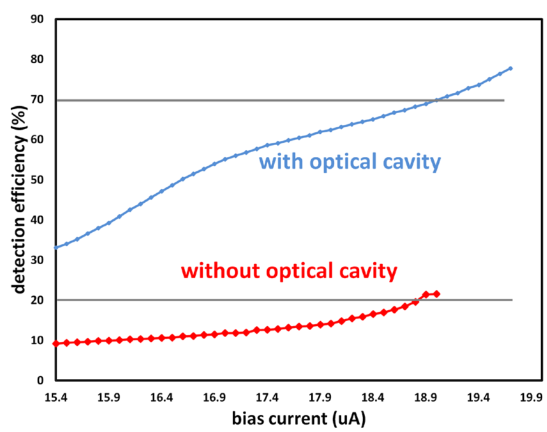
Single-photon detectors that are sensitive to mid-infrared light are necessary for applications that require the measurement of very low levels of light, such as circuit analysis based on imaging the infrared photons produced when the transistors in an integrated circuit switch. We design and fabricate superconducting nanowire single photon detectors based on superconducting niobium nitride nanowires (NWs), which results in fast devices (~5-ns reset time) with low timing jitter (<30 ps) and high detection efficiency.

Figure 1 shows a schematic of the cross section of a typical device. The optimal thickness of each layer is determined with an optical model based on analytical equations. The optical model is adjusted to maximize the absorptance of light in the NbN active layer, which determines the upper bound of the detection efficiency of the device. However, the detection efficiency also depends on other factors--for example, the geometric cross section of the NWs, where a smaller cross section leads to higher sensitivity to low energy photons--which introduce tradeoffs that must be considered when designing high-efficiency devices for infrared applications.

Figure 2 shows the device detection efficiency (DDE) results for a device before and after the optical cavity was fabricated. Before cavity integration, the DDE reached only 20%, but, after cavity integration, the DDE increased by over a factor of 3 to greater than 70%. Current research efforts aim to replicate this result and to understand some of the limits of our device designs. For example, the results in Figure 2 indicate that the device was not saturated, i.e., the DDE did not reach a plateau at high bias current. We are investigating several factors, such as vortex tunneling and fabrication defects, that might contribute to the unsaturated behavior of our detectors.



▲ Figure 1: Cross-sectional view of a device on a silicon substrate. The devices are back-illuminated through the substrate, and the integrated optical cavity dimensions are optimized to increase the absorptance of light in the NbN NWs.



▲ Figure 2: DDE of a superconducting NW avalanche photodiode based on three NWs in parallel (3SNAP) without optical cavity (red) and with optical cavity (blue). The device does not appear to be saturated, but efficiency reaches over 70% with optical cavity.

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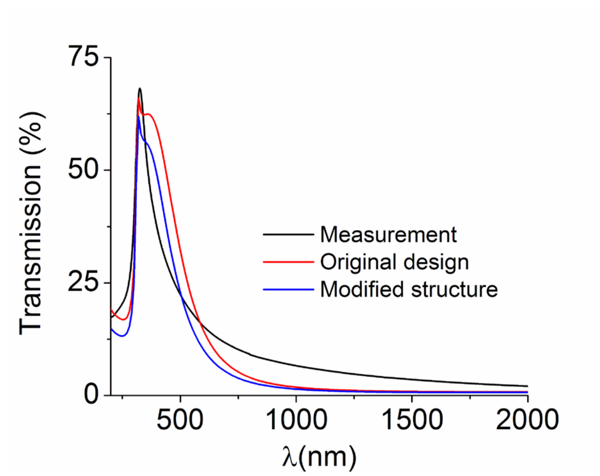
A High-transmissivity Metal-dielectric UV Band-pass Filter

J. Mu, P.T. Lin, L. Zhang, J. Michel, L.C. Kimerling, F. Jaworski, A. Agarwal
Sponsorship: Institute for Soldier Nanotechnologies

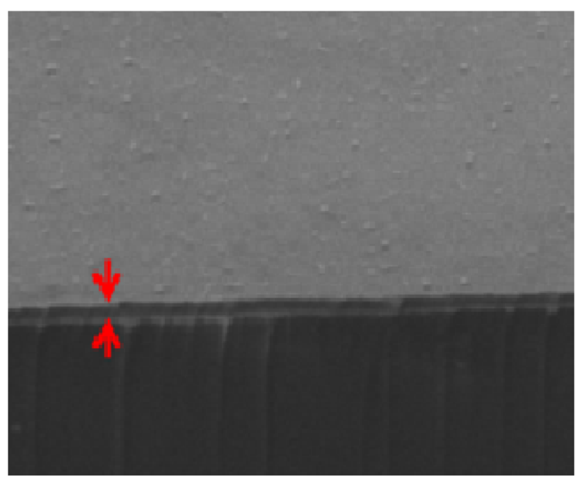
Ultraviolet (UV) technologies have found increasing importance in various applications including pollution monitoring, flame detection, UV astronomy, and space-to-space communications. Due to the strong absorption of sub-200-nm light by ozone and molecular oxygen in the terrestrial atmosphere, most practical technology development occurs in the mid-UV (200-300 nm) and near-UV (300-400 nm) ranges. To allow us to focus only on mid- and near-UV light, it is critical to obtain a solar-blind UV filter that blocks the visible and infrared portions of the solar spectrum.

For UV light detection, wide bandgap materials such as III-nitride based solar-blind UV photo detectors have been proposed and studied. Not all approaches are compatible with standard complementary metal oxide semiconductor (CMOS) fabrication processes; hence integration with silicon-based devices is challenging. Considering currently available mature and cheap silicon processing technologies, the integration of a solar-blind UV band-pass filter with a silicon-based UV photo detector is a solution for obtaining a low-cost and effective UV detector.

Here, we present a simple and general yet efficient approach for designing a UV band pass filter based on metal/dielectric stacks. Experimental transmission measurements and the SEM picture are shown in Figure 1. The measurement results agree well with the simulation data. The measurement of the sample with three-pair Ag/SiO_2 layers shows that the fabricated device has very high transmission efficiency (67%) with a bandwidth around 100 nm. The discrepancy between the measurement and simulation can be attributed to several factors. One possible factor could be the thickness difference between the deposited layer and the simulation value used. To evaluate the impact of layer thickness variation, we simulated a structure in which the second SiO_2 thickness is changed by 4 nm to 29 nm, and the second silver layer thickness is changed by 5 nm to 15 nm. Compared to the original design, as shown in Figure 1(a), the simulation of the thickness-modified structure is closer to the experimental measurement. Another possible factor is that the optical properties of thin silver films deposited by RF sputtering are sensitive to sputtering power, argon pressure, and RF bias voltage.



(a)



(b)

▲ Figure 1: Experimental results from front illumination.(a) The SEM image of the deposited multilayer thin film indicated by the arrows; (b) The three-pair Ag/SiO_2multilayer shows high transmission efficiency (67%) with a bandwidth of about 100 nm.

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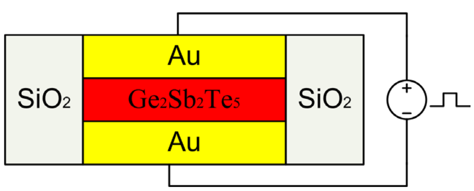
A Nano Optical Latch

J. Mu, Z. Han, S Grillanda, A. Melloni, J. Michel, L.C. Kimerling, A. Agarwal

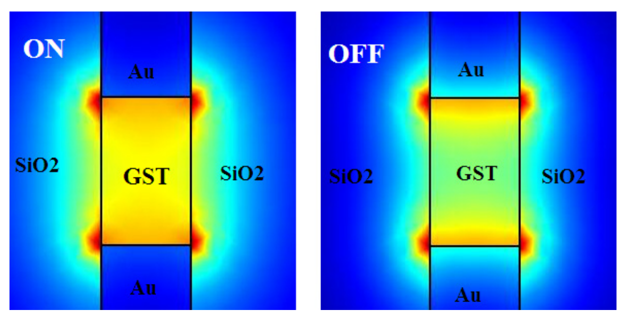
We propose an ultra-subwavelength ON/OFF optical switch based on the variation of the attenuation. The switch consists of a metal-dielectric-metal waveguide structure integrated with $Ge_2Sb_2Te_5$ chalcogenide glasses. The GST is sandwiched between two gold thin films. As Figure 1 shows, gold (i) enables the formation of an optical waveguide by the plasmon polaritonic resonance effect and (ii) serves as an electrical contact.

In the switching-off process, i.e., the transition of the GST material from the amorphous to crystalline state, the process is essentially a re-crystallization under high temperature, yet below the melting point of the material. The resistivity of amorphous GST is so high (typically about 10 Ωm) that there is almost no measurable current below the threshold voltage. However, amorphous GST has a threshold voltage that occurs at a certain current density, above which it becomes conductive without any phase change; the GST consequently generates Joule heating that induces the phase change. The typical switching-off time (or "Set" process in PCM) of 100 ns is used. This is much longer than the typical switching-on time (or "Reset" process), around 1 ns, which indicates that the energy consumption of the switching-off process is dominant, therefore requiring only an optimization of the energy cost for the switching-off process.

For the switching-on process, the crystalline GST melts into liquid and then is rapidly quenched, typically within a few nanoseconds, which results in an amorphization of the structure. Assuming that the conductivity of the crystalline GST does not change before melting and applying a voltage of 3.5 V, we calculate a current density of 1.94×104 kA/cm2. After 57 ps, the maximum temperature reaches the melting temperature (883K). With further heating, GST will melt, and the latent heat (1.37×105 J/kg) will consume most of the input power, pinning the temperature to the melting point. If we assume that the conductivity of GST is constant and that all the heating energy goes into latent heat after 57 ps, then the total phase transition time is only 0.12 ns, which is a little shorter than from other reports. The energy consumption required for the phase transition is 0.4 pJ, which is much smaller than that of the switching-off process. Therefore, the energy consumption per cycle (including both the switching-on and switching-off processes) is 30.4 pJ.



▲Figure 1: Cross section of an electrically driven GST optical latch: GST material is sandwiched between two gold thin films and laterally surrounded by SiO2 for isolation. Gold (i) enables formation of an optical waveguide by the plasmon-polariton resonance effect and (ii) serves as an electrical contact.



▲Figure 2: Simulated electric field (normal to the surface) of the optical mode of the GST-assisted plasmonic latch when the GST is in the ON state (amorphous) and OFF state (crystalline).

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Low-threshold Organic Nanolasers

T. Mahoney, V. Bulović

Since the first demonstration of lasing in organic gain media, there has been great interest in developing an electrically pumped organic laser. Organic lasers have been demonstrated using different device structures such as VCSELS, distributed feedback lasers, and photonic crystal cavity lasers. However, none of these have achieved electrical pumping. Singlet triplet annihilation in the organics leads to unfeasibly large threshold current densities. To lower the threshold for organic lasers, we have designed a cavity with a high quality factor/mode volume (Q/V) ratio and a high spontaneous emission factor (b).

Our design uses a suspended nanobeam photonic crystal cavity (PCNC). The devices are fabricated by e-beam lithography using XR-1451 e-beam resist on a silicon substrate, followed by an XeF_2 sacrificial etch. The suspended patterned membrane is used as a mask to evaporate a 150-nm layer of tris(8-hydroxyquinolinato) aluminum (Alq_3) doped with 4-(dicyanomethylene)-2-methyl-6-(p-dimethylaminostyryl)-4H-pyran (DCM) to form the cavity. Figure 1 shows an SEM image of an example structure before evaporation. We pump the device at 1 kHz with 400-nm light and observe lasing through the fundamental mode of the cavity at 618 nm. We observe evidence of lasing in the form of a threshold energy density and spectral narrowing, limited by the slit width of our spectrometer (see Figure 2). We measured the Q of the cavities to be around 3500; the low value is attributed to surface roughness of the evaporated film. We have demonstrated successful lasing at threshold energy densities of 4.2 uJ/cm².

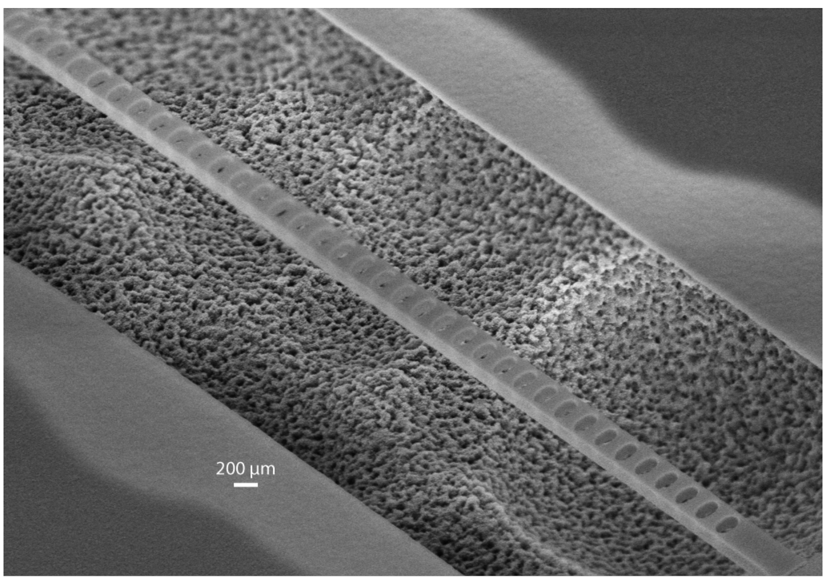

Figure 1: SEM of a photonic crystal nanobeam cavity after XeF_2 etch but before evaporation of organic materials.

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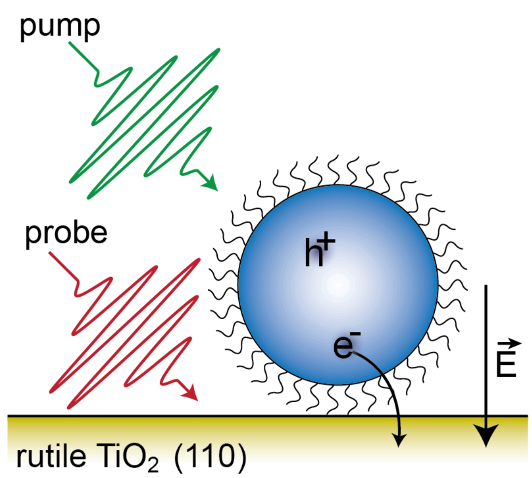
Second Harmonic Generation as a Probe of Interfacial Electron Transfer

R.S. Hoffman, W.A. Tisdale
Sponsorship: National Science Foundation, Department of Energy

Colloidal quantum dots are a promising material for cost-effective, solution-processable optoelectronic devices such as solar cells and light-emitting diodes. Efficient charge extraction from quantum dots is crucial for reaching the potential of quantum dot optoelectronic devices, but these charge transfer processes are not well understood. Transient absorption has been used to study charge transfer from dyes to semiconductors, but this technique does not work well for studying charge transfer from quantum dots to semiconductors. Other techniques are needed. Tisdale *et al.* showed that time-resolved second harmonic generation (TR-SHG) can be used to observe hot electron transfer from PbSe quantum dots to the electron acceptor TiO_2 with femtosecond time resolution. Kaake *et al*. showed that TR-SHG is also a useful probe of charge separation at organic interfaces. We are using TR-SHG to probe interfacial electric fields resulting from charge transfer over a broad experimental space. These experiments will enable us to answer key questions about charge transfer mechanisms at quantum dot-semiconductor interfaces that will aid in the design of more efficient optoelectronic devices.



▲Figure 1: Schematic of time-resolved second harmonic generation as a probe of interfacial electron transfer. A pump pulse creates an electron-hole pair in quantum dot. The electron is transferred to TiO_2, creating an interfacial electric field. At a controlled, variable time after pump pulse, a probe pulse detects interfacial electric field using second harmonic generation.

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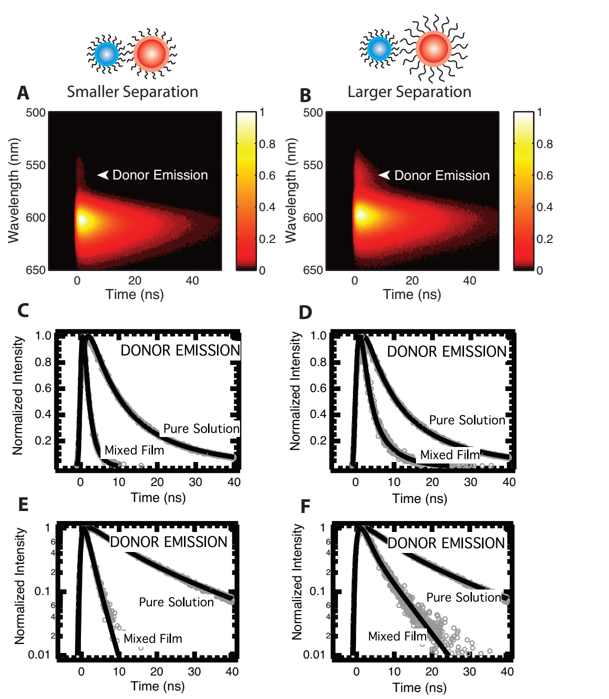
Energy Transfer in Quantum Dot Thin Films

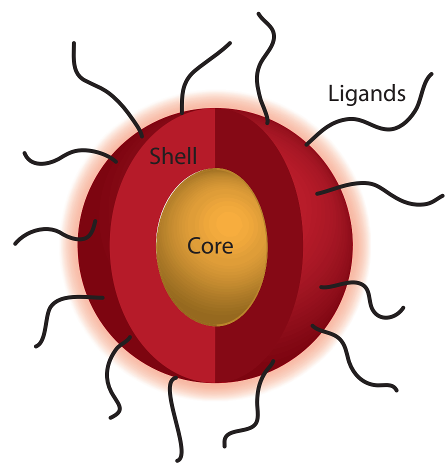
A.J. Mork, N.S. Dahod, M.C. Weidman, W.A. Tisdale
Sponsorship: National Science Foundation GRFP, Department of Energy, Energy Frontier Research Center for Excitonics

Excitonic energy transfer among colloidal nanocrystal quantum dots (QDs) in QD optoelectronic devices affects the design and successful operation of these devices. While Förster's resonant energy transfer theory has successfully accounted for the distance scaling of energy transfer in many QD systems, the overall magnitude of the Förster radius in close-packed QD solids remains an open question. We used spectrally-resolved transient photoluminescence quenching to measure the magnitude of the Förster radius in blended donor-acceptor QD assemblies (as in Figure 1). For blends of CdSe/CdZnS core/shell QDs consisting of green-emitting donors and red-emitting acceptors, we measured energy transfer rates per donor-acceptor pair that are 10-100 times faster than those predicted by standard resonant energy transfer theory. Several factors, such as the absorption cross section, dielectric constant, and shape of the nanocrystals in thin films may contribute to this significant discrepancy.

To understand which factors affect the energy transfer rate between QDs in solid films, we are synthesizing donor and acceptor QDs with a series of different surface ligands, and a series of shell thicknesses to modulate the center-to-center distance between QDs (Figure 2). The center-to-center distance is the most important parameter determining the energy transfer rate, assuming that the QDs behave as point dipoles. Altering the QD ligand or the shell thickness, however, will also result in different dielectric constants for solid films of these materials. We can thus separately probe the roles of inter-particle separation and the dielectric constant of the medium.



▲Figure 1: (A, B) Spectrally-resolved photo-luminescence lifetime measurements of donor-acceptor blends, showing longer donor lifetimes for QD materials with a larger donor-acceptor inter-particle distance. (C, D) Integrated donor emission of mixed film compared to a pure film of donors on linear scale. (E, F) Integrated donor lifetimes on semi-log scale with biexponential fits.



▲Figure 2: Anatomy of a QD, indicating CdSe core, shell, and ligands. Shell thickness and composition, as well as ligand length and structure, may be altered to understand the mechanism for energy transfer in QD materials.

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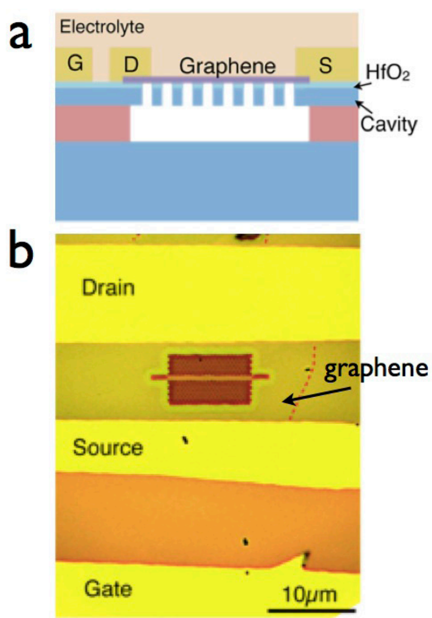
On-chip Graphene Electro-optic Modulators and Photodetectors

R.-J. Shiue, X. Gan, D. Englund
Sponsorship: Energy Frontier Research Center for Excitonics

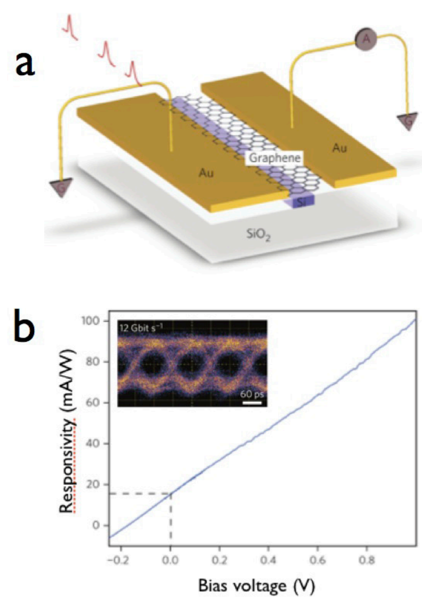
Graphene has shown great potential for compact optoelectronics with low power consumption. To increase the optical absorption in graphene, we have integrated the material with silicon photonic waveguides and photonic crystal (PhC) cavities. In these structures, graphene stongly couples to the evanescent field of the waveguides and cavities, resulting in near-unity absorption. Based on these devices, we have demonstrated an efficient electro-optic modulator and a graphene-based photodetector with high responsivity.

Figure 1(a) shows the scheme of an graphene electro-optic modulator integrated with a PhC cavity. The cavity is made on a silicon-on-insulator (SOI) wafer with a series of electron-beam lithography and dry and wet etching processes. A linear three-hole (L3) defect is introduced to confine cavity modes. Graphene is transferred on top of the cavity, and the electrical contacts are deposited with e-beam lithography, metal deposition, and lift-off. An optical imagine of the finished device is shown in Figure 1(b). We achieved a modulation depth in excess of 10 dB with a switching energy of 300 fJ per bit. We demonstrated the modulation of such graphene-based electro-optic modulators to ~1 GHz with a modulation depth of 3dB. If the device capacitance is controlled, such modulators should reach tens of GHz.

We have implemented a graphene photodetector on a silicon buried waveguide, as in Figure 2(a). When graphene is coupled to the waveguide mode evanescently, over 60% input light is absorbed with a 53-um-long bi-layer graphene channel. As Figure 2(b) shows, the maximum responsivity of the graphene photodetector is 0.108 A/W. It exhibits a response time over 20 GHz and a broadband response in the wavelength range 1450 -1590 nm[3]. We tested the detector in a optical network with a data transmission rate of 12 Gbps and obtained a clear eye-opening diagram (inset of Figure 2b).



▲Figure 1: (a) The scheme of a graphene electro-optic modulator integrated with a PhC cavity. (b) An optical image of the finished device.



▲Figure 2: (a) Scheme of a graphene photodetector integrated with a silicon waveguide. (b) The response of the graphene detector achieves a maximum of 0.108 A/W. Inset: A clear eye-opening diagram at 12 Gbps is tested with the graphene photodetector.

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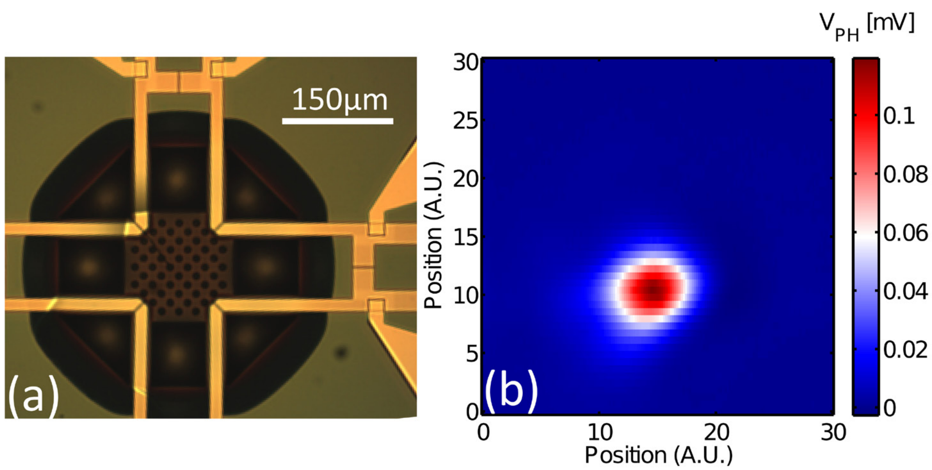
Graphene Mid-IR Photodetectors

P.K. Herring, A.L. Hsu, N.M. Gabor, Y.C. Shin, J. Kong, T. Palacios, P. Jarillo-Herrero
Sponsorship: Air Force Office of Scientific Research

One of our primary projects has been investigating the Mid-IR response of graphene for applications in imaging devices and detectors for this wavelength regime. Our initial devices found that substrate effects dominated the response of the device. After fabricating suspended devices, we have found that there is a significantly improved response (on the order of 100 times larger) for these suspended devices as compared to the on-substrate devices. Additionally, creating thermopile geometry substantially improves the magnitude of the sensitivity, at the cost of increasing the thermal response time, a trade-off that might be exploited to create effective imaging arrays for thermal viewing applications.



▲ Figure 1: (a) Optical image of suspended thermopile device showing optical absorption pad in middle and 4 junctions arranged one at each corner (b) Spatial map of photovoltage measuring one junction showing strong response in vicinity of that junction.

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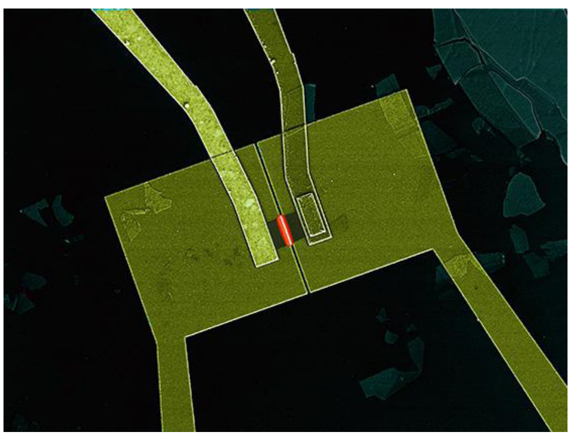
Optoelectronics Based on Monolayer WSe_2 p-n Diodes

B. Baugher, H. Churchill, Y. Yang, P. Jarillo-Herrero
Sponsorship: Office of Naval Research

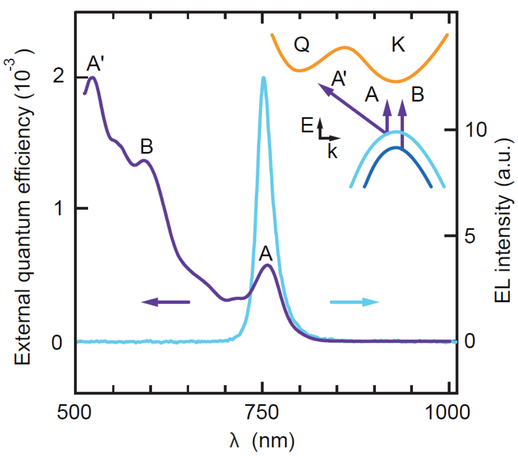
The p–n junction is the functional element of many electronic and optoelectronic devices, including diodes, bipolar transistors, photodetectors, light-emitting diodes, and solar cells. In conventional p–n junctions, the adjacent p- and n-type regions of a semiconductor are formed by chemical doping. Ambipolar semiconductors, such as carbon nanotubes, nano-wires, and organic molecules, allow p–n junctions to be configured and modified by electrostatic gating. This electrical control enables a single device to have multiple functionalities.

Through this initiative, we have pioneered a new class of electrostatically controlled ambipolar p-n junctions, utilizing monolayer WSe_2. With these electrically tunable p–n junctions, we have demonstrated both p–n and n–p diodes with ideality factors better than 2. Under optical excitation, the diodes demonstrate a photodetection responsivity of 210 mAW^{-1} and photovoltaic power generation with a peak external quantum efficiency of 0.2%, promising values for a nearly transparent monolayer material in a lateral device geometry. Finally, we have demonstrated a light-emitting diode based on monolayer WSe_2.

These p–n diodes demonstrate the potential of monolayer WSe_2, in addition to other direct-gap semiconducting dichalcogenides, for novel electronic and optoelectronic applications. Such devices may provide the building blocks for ultrathin, flexible, and nearly transparent optoelectronic and electronic devices. As quality improves, they also lay the foundation for more fundamental quantum transport experiments.



▲Figure 1: Color enhanced scanning electron micrograph of a device, showing monolayer WSe_2 device glowing in center. The device is contacted by two metal leads and lies on top of a split gate, enabling electrostatic control of the p-n junction.



▲Figure 2: External quantum efficiency and electroluminescence intensity spectra. External quantum efficiency spectrum is shown in purple. Peaks correspond to lowest energy band transitions as depicted in inset diagram. Electroluminescence output spectrum shows a strong peak at lowest energy, direct-gap transition.

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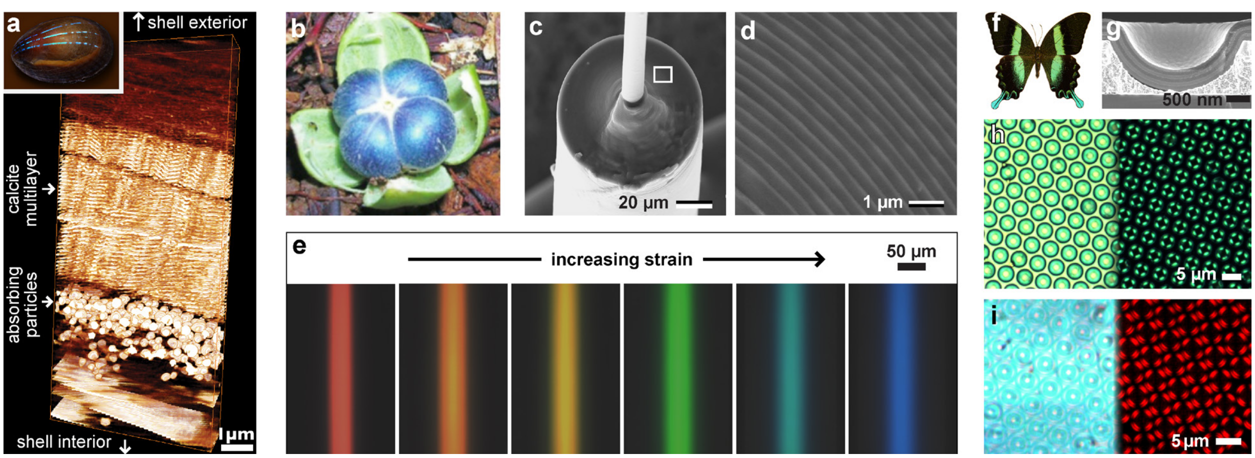
Bio-inspired and Bio-manufactured Photonic Materials

M. Kolle
Sponsorship: Alexander von Humboldt Foundation, Air Force Office of Scientific Research

The research in the Laboratory for Bio-inspired Photonic Engineering focuses on the fundamental and applied aspects of conceiving and developing multifunctional, hierarchically structured, bio-inspired material systems, with particular emphasis on stimuli-responsive and dynamically tunable optical performance. In this regard, we can benefit in several ways from studying sophisticated material solutions that have evolved in various organisms (see Figures 1a, b). We explore design concepts found in biological photonic architectures, seek to understand the mechanisms underlying morphogenesis of bio-optical systems, aim to devise viable manufacturing strategies that can benefit from insight into biological formation processes and the use of established synthetic routines, and ultimately strive to realize new photonic materials with tailor-made optical properties. Recently, we invented color-tunable elastic photonic fibers, a fully synthetic analogue of the photonic structures found in a tropical fruit (see Figures 1b-e). We aim to establish these fibers as a material platform for applications in visual stress and strain sensing, for the optical assessment of mechanical properties of living tissue, and for dynamic textiles and flexible photonic circuitry.

Beyond employing numerous state-of-the-art synthetic components and nanofabrication technologies, we aspire to exploit existing biological machinery for *ex vivo* fabrication of photonic elements on a larger scale. In this respect, we aim to understand and harness the structure-forming capabilities of living cells that lie at the origin of many species' ability to grow photonic materials. Understanding and potentially modifying the underlying mechanisms, with the ambition to exert control over the formation processes, could help to produce photonic elements with desired specifications in industrial quantities. Overall, we benefit from the fact that the optimized combinations of optical, mechanical, and chemical attributes required in biological systems are equally desirable in man-made materials with great potential to advance current technology.

Nature's solutions are a starting point from which our research (see Figures 1f-i) can provide versatile material solutions for many applications in biomedical sensing, imaging, laser surgery, optical lithography, additive manufacturing, light emitting diodes, solar energy harvesting, flexible displays, photonic circuitry, and consumer product design.



▲Figure 1: Biological and bio-inspired photonic architectures. a) Composite photonic structure found in mineralized shell of *Patella pellucida*. b) Blue fruit of Margaritaria nobilis. c) Cross-section of photonic fiber inspired by fruit's photonic arrangement. d) High-resolution image o f fibers' layered periodic morphology. e) Reversible tuning of fiber color by strain. f) Butterfly *Papilio blumei*. g) Electron micrograph of synthetic mimic of butterfly's photonic structure. h) Optical micrograph of mimic taken in non-polarized (left) and polarized light (right). i) Natural design modified for more pronounced optical effects.

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Biological, Medical Devices and Systems

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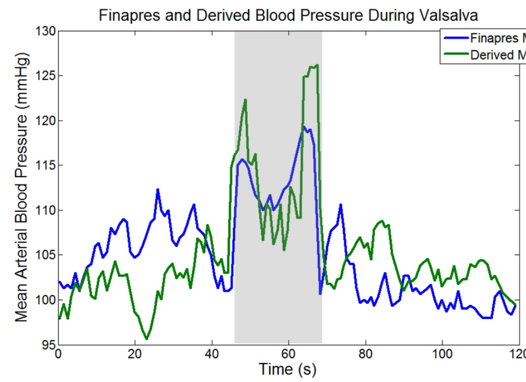
A Wearable Vital-signs Monitor at the Ear

E. Winokur, D. He, C.G. Sodini
Sponsorship: Medical Electronic Device Realization Center, NSERC Fellowship

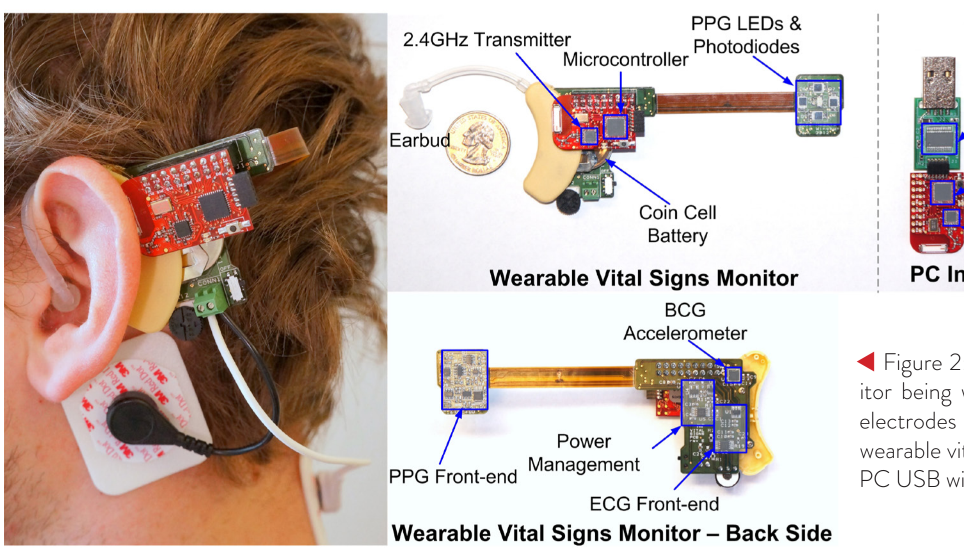
Vital signs such as heart rate, blood pressure, blood oxygenation, cardiac output, and respiratory rate are necessary in determining the overall health of a patient. Continuous monitoring of these vital signs can help healthcare workers assess the wearer's overall state of health and identify risks for cardiovascular diseases.

We propose a site behind the ear as a location for an integrated wearable vital signs monitor. This location offers physiological signals such as the electrocardiogram (ECG), the photoplethysmogram (PPG), and the ballistocardiogram (BCG). The ECG measures the electrical activity from the heart and offers heart rate information. The PPG measures the blood volume and color under the skin using optical illumination. The PPG offers information such as continuous heart rate and blood oxygenation. The BCG measures the body's mechanical reaction to the blood expelled by the heart and also provides the heart rate.

Using the peak timing data from BCG and PPG, the device can measure mean arterial blood pressure. Figure 1 compares the continuous mean arterial blood pressure measured from a Portapres finger-cuff with the continuous blood pressure measurement from the vital signs monitor while a test subject performed a Valsalva maneuver. The device is designed to use the ear as a discreet and a natural anchor that reduces device visibility and the need for skin adhesives. A photo of our prototype device is shown in Figure 2. We have designed custom integrated circuits to reduce the form factor and lower the power consumption while still maintaining signal integrity in variable environments.



▲ Figure 1: A comparison of mean arterial blood pressure measured by a Portapres finger-cuff (blue) and mean arterial blood pressure derived from peak timing information of the vital signs monitor (green) during a Valsalva maneuver.



◀ Figure 2: Left - The vital signs monitor being worn at the ear with ECG electrodes attached. Center - The wearable vital signs monitor. Right - A PC USB wireless receiver.

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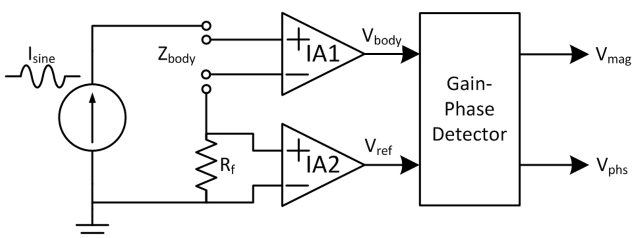
A Portable Bioimpedance Spectroscopy Measurement System for Managing Congestive Heart Failure

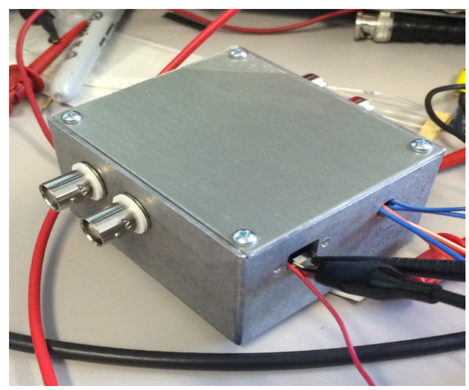
M. Delano, C.G. Sodini
Sponsorship: Medical Electronic Device Realization Center, Analog Devices

An estimated five million people are currently diagnosed with congestive heart failure (CHF) in the United States, with over 400,000 new diagnoses annually. CHF is frequently associated with significant fluid retention in the lungs and legs. Almost one in two patients will be readmitted to the hospital within four to six months of discharge. Readmissions can occur when the patient becomes fluid overloaded due to poor medication and/or diet compliance, among other reasons. Up to 50% of these early re-admissions may be prevented if symptoms are recognized early enough and medication/diet compliance improves.

Bioimpedance techniques can be used to estimate the fluid levels in a patient non-invasively. These measurements have been shown to be predictive of heart failure decompensation up to 14 days before an event occurs. We have developed a portable bioimpedance system that can measure body impedance from 1 kHz to 1 MHz. The system uses the Magnitude-Ratio and Phase Difference Detection method to calculate the magnitude and phase of the measured impedance (see Figure 1). The system is enclosed in aluminum box (see Figure 2) and can be used with four co-axial cables. Each co-axial cable is actively driven by a screen driver circuit that reduces stray capacitance from the cables. Data from the device can be sent directly to a computer or transmitted over Bluetooth (with lid off). The device has been characterized with RC networks and will be validated in healthy volunteers.



▲ Figure 1: A schematic overview of the Magnitude-Ratio and Phase Difference Detection method. A fixed sinusoidal current is driven through the body and a sense resistance. The voltage is amplified and measured by a Gain-Phase Detector chip (AD8302).



▲ Figure 2: The portable bioimpedance spectroscopy measurement system inside the enclosure.

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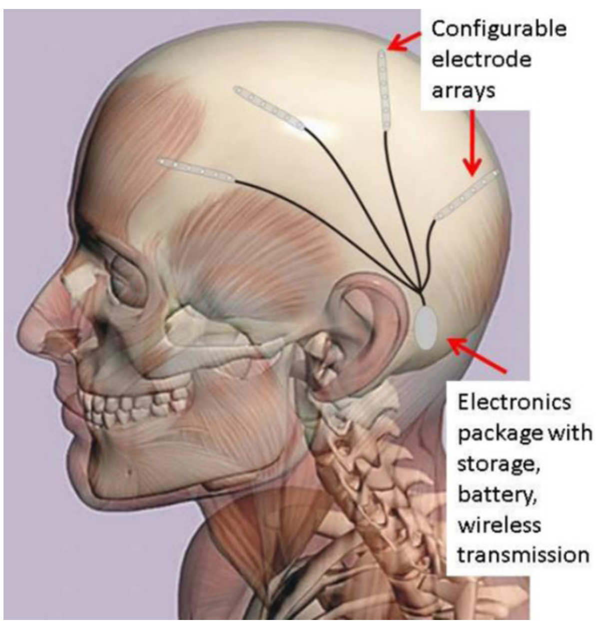
A Subdermal EEG Monitor for Seizure Detection

B. Do Valle, C.G. Sodini
Sponsorship: Center for Integrated Circuits and Systems

Epilepsy is a common chronic neurological disorder that affects about 1% of the world population. It is characterized by repeated seizures, which are caused by an abnormal neuronal firing in the affected brain area. Although EEG has been the chief modality in the diagnosis and treatment of epileptic disorders for more than half a century, long-term recordings (days to weeks) can be obtained only in the hospital setting. Many patients, however, have intermittent seizures occurring far less often. Patients cannot come into the hospital for weeks on end for an event to be captured on EEG – a necessary prerequisite for making a definitive diagnosis, tailoring therapy, moving toward certain kinds of solutions such as surgery, or even establishing the true rate of events. This work aims to address this need by proposing a subdermal implantable 8-channel EEG monitor and seizure detector. The system will be implanted behind the patient's ear, as shown in Figure 1, to guarantee continuous monitoring of the brain's activity. The first step towards creating the implantable EEG monitor was to understand the challenges in recording EEG. To do that, we designed a behind-the-ear-wearable device using off-the-shelf components that is currently being tested at MGH.

The wearable prototype consists of 1 EEG channel sampled at 256 Hz with a 12-bit resolution. The system is housed in a package, shown in Figure 2, created by a 3D printer. One electrode is placed near the temporal lobe (close to T3 or T4), and the other one is placed on the mastoid. The data is transmitted through Bluetooth Low Energy to an iPod Touch, which uploads the data to a secure server via WiFi.



▲ Figure 1: Implanted EEG system showing the location of the electronic package and electrodes.

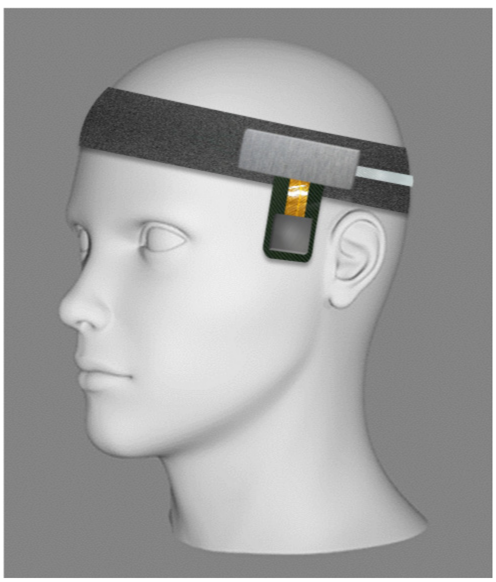
▲ Figure 2: Behind-the-ear wearable prototype currently being tested at MGH.

An Electronically Steered, Wearable Transcranial Doppler Ultrasound System

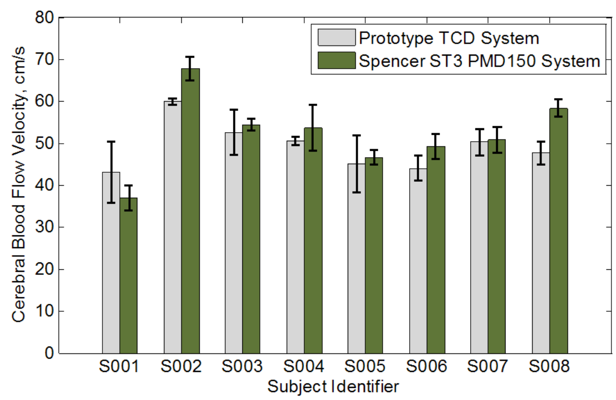
S. Pietrangelo, C.G. Sodini, H.-S. Lee
Sponsorship: Medical Electronic Device Realization Center

The central objective of critical care for patients affected by neurotrauma, cerebrovascular accident (i.e., stroke), and other neurovascular pathologies is to monitor the patient's state and provide suitable medical intervention to mitigate secondary injury and aid in recovery. While several non-invasive cerebrovascular diagnostic modalities exist, the use of transcranial Doppler (TCD) sonography is highly compelling for certain diagnostic needs due to its safety in prolonged studies, high temporal resolution, and relative portability. Despite a growing list of potential diagnostic applications, several constraints – notably operator-dependent measurement results and the need for manual vessel location – have generally confined the use of TCD ultrasound to highly specific clinical environments (e.g., neurocritical care units and vascular laboratories).

Figure 1 illustrates a conceptual TCD system for wearable, autonomous monitoring of cerebrovascular state. Figure 2 compares clinically measured cerebral blood flow velocity data from a first-generation TCD prototype system to a commercially available TCD system. Comparable velocimetry data was obtained using both systems across several different human test subjects.



▲Figure 1: Concept of a wearable TCD monitoring system with integrated ultrasound electronics.



▲Figure 2: Comparison of average cerebral blood flow velocity across subject trials.

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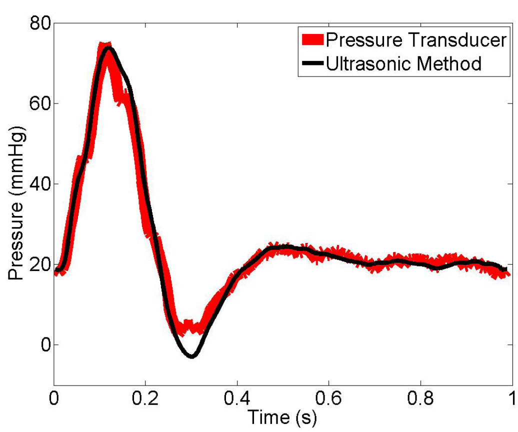
Continuous and Non-invasive Blood Pressure Monitoring using Ultrasonic Methods

J. Seo, H.-S. Lee, C.G. Sodini
Sponsorship: Samsung Fellowship, Center for Integrated Circuits and Systems

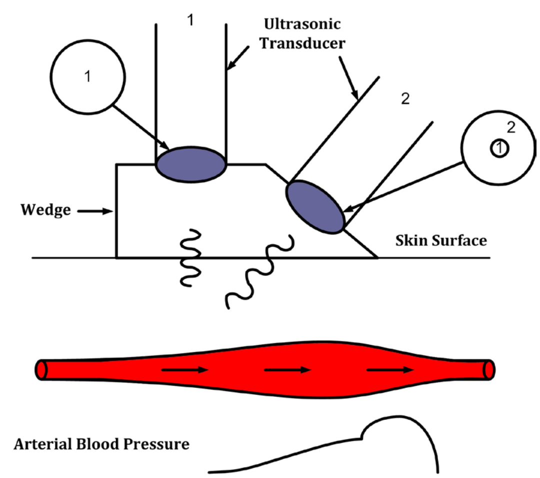
An arterial blood pressure (ABP) waveform provides valuable information in treating cardiovascular diseases. The ABP waveform is usually obtained through a pressure transducer connected to an arterial catheter. Although considered as the gold standard, the disadvantage of this method is its invasive nature. The invasive nature not only increases various patients' risks but makes the usage of the ABP waveform for cardiovascular studies expensive. Therefore, reliable non-invasive ABP waveform estimation has been desired for a long time by medical communities. In that sense, medical ultrasound is an attractive imaging modality because it is inexpensive, free of radiation, cuff-less and suitable for portable system implementation.

The proposed ultrasonic ABP monitoring is achieved by observing the pulsatile change of the cross-sectional area and identifying the elastic property of an arterial vessel, represented by the pulse wave velocity (PWV; the propagation speed of a pressure wave along an arterial tree) with a diastolic blood pressure measurement as a baseline. The PWV can be estimated by obtaining a flow-area plot and then measuring the slope of a linear part in the flow-area plot during a reflection-free period (e.g., the early systolic stage).

An experimental setup was established to validate this pressure estimation technique. The cross-sectional area is estimated from the ultrasonically obtained diameter waveform assuming axisymmetric geometry of a tube. The volumetric flow rate is calculated from the spatial mean velocity of scatterers inside the tube using Doppler ultrasound. Figure 1 compares the resulting pressure waveform from ultrasonic methods to the waveform from a pressure transducer, which shows an excellent agreement. Figure 2 shows a prospective schematic of ultrasonic transducers for a clinical test.



▲Figure 1: Comparison of two pressure waveforms. Assuming the mean pressure of two waveforms are same, a pressure waveform obtained from ultrasonic methods well agrees with a direct pressure waveform measurement from a pressure transducer.



▲Figure 2: Prospective schematic of ultrasonic transducers for a clinical test. Channel 1 measures a vessel diameter while channel 2 measures a blood flow velocity simultaneously to estimate a local PWV and an ABP waveform.

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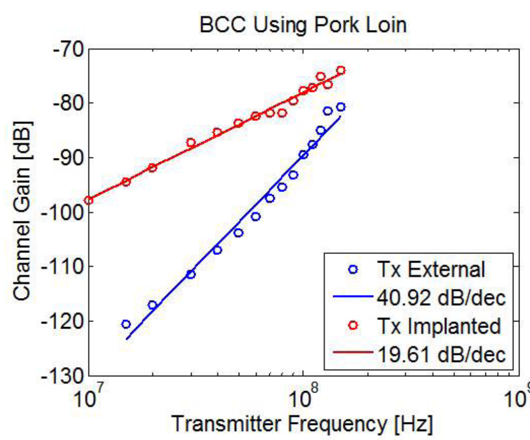
Body-coupled Communication and Implants

G.S. Anderson, C.G. Sodini
Sponsorship: Center for Integrated Circuits and Systems

Body-coupled communication (BCC) is achieved by creating a potential difference in one area of the body and sensing the resulting attenuated potential difference in another area of the body. To do this, the transmitter and receiver each have two electrodes that electrically connect to the body's conductive tissues beneath the epidermis. These connections can be formed either capacitively or galvanically. A capacitive link consists of the electrode forming one plate of a parallel plate capacitor while the conductive tissues form the other plate. A galvanic link is formed by directly putting the electrode/wire in the conductive tissue.

For an implant to communicate to a device outside the body using BCC, the channel utilizes both galvanic and capacitive links (capacitive for the device outside the body and galvanic for the implant). To test if this is possible a pork loin was used to simulate the conductive tissue of the body (see Figure 1). First, both the transmitter's and receiver's electrodes were connected to the pork loin using cardboard spacers between the pork loin and the electrodes, ensuring that both the transmitter and receiver would be capacitively coupled to the conductive tissue in the pork loin. Next the transmitter's output was connected to two alligator clips that were inserted into the pork-loin while the receiver was connected capacitively as before. This configuration simulates an implanted transmitter that is galvanically coupled to the conductive tissue, communicating with a receiver that is capacitively coupled. The results, shown in Figure 2, validate the predictions of the body model detailed in the further reading below

▲ Figure 1: A setup to test implants talking to devices outside the body using BCC.



▲ Figure 2: BCC channel measurements.

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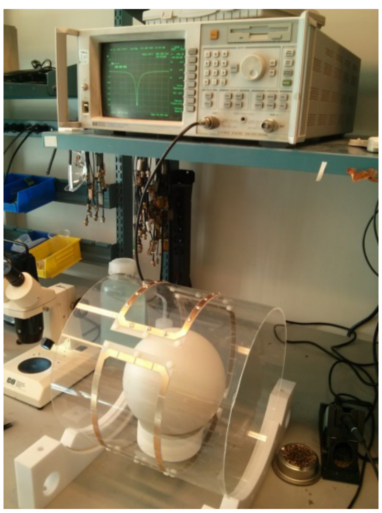
Automated Design of a Robust Decoupling Matrix for Multi-channel Parallel Transmit Coil Arrays in Magnetic Resonance Imaging

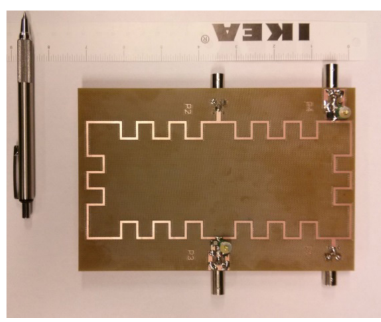
Z. Mahmood, B. Guérin, B. Keil, E. Adalsteinsson, L.L. Wald, L. Daniel
Sponsorship: NIH, NSF NCN – NEEDS Node, SRC

In a coupled parallel transmit array, the power delivered to a channel is partially distributed to other channels because of coupling. This power is dissipated in the circulators, resulting in a significant reduction in the power efficiency of the overall system. Most existing decoupling methods focus on nearest-neighboring channels. Capacitive ladder networks, which aim at decoupling also distant neighbors, are highly sensitive to specific operating conditions; they are rarely used because of this lack of robustness. In this work, we propose an automated approach to design a robust decoupling matrix interfaced between the RF amplifiers and the coils. Similar to a Butler matrix, our decoupling matrix mixes the input signals but is also optimized to ensure that all forward power is delivered to the load. In addition to mixing the input signals to provide uncoupled field patterns, the decoupling matrix also minimizes the power lost in the circulators.

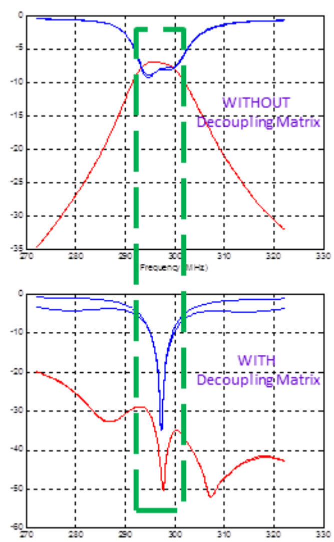
The decoupling condition is that the impedance matrix seen by the power amplifiers is a diagonal matrix with 50 ohms at the diagonal. Intuitively, a dense full rank matrix can be converted to a diagonal matrix by eigen-decomposition. In this work, we diagonalize the impedance matrix of the coupled coils (or antennas) by a multiplication with its eigen-vectors. We accomplish this multiplication via Givens rotations implemented using only passive RF components such as hybrid couplers and lumped reactive elements, as shown in Figure 2. We explore several design aspects of the decoupling matrix, including the network topology, robustness and sensitivity to component values by designing a decoupling matrix for a 2-channel coupled array for magnetic resonance imaging. The results, shown in Figure 3, show that our decoupling matrix achieves near-ideal decoupling. The 2-channel instantiation works for demonstration and evaluation purposes to illustrate the principles of robustness and topology exploration. The methods presented in this abstract scale to any arbitrary number of channels and can be readily applied to other coupled systems such as antenna arrays.



▲ Figure 1: Picture of a coupled 7-Tesla parallel transmit head array to be decoupled.



▲ Figure 2: Layout of a decoupling matrix designed to decouple 2-channels.



▲ Figure 3: Measured S-parameters of a 2-channel array without (top) and with (bottom) a decoupling matrix.

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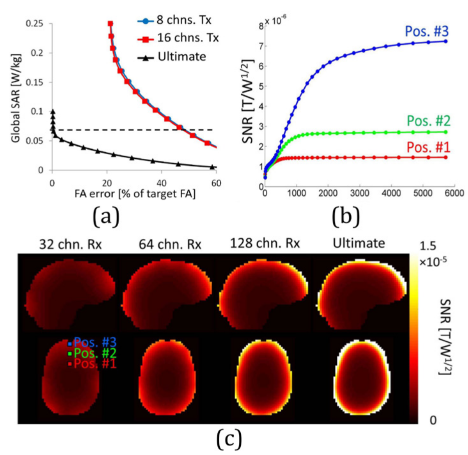
Ultimate Performance Metrics for Magnetic Resonance Imaging RF Coil Designs

J. Fernández Villena, A.G. Polimeridis, B. Guerin, L.L. Wald, E. Adalsteinsson, J.K. White, L. Daniel.
Sponsorship: NIH, MIT Skoltech Initiative

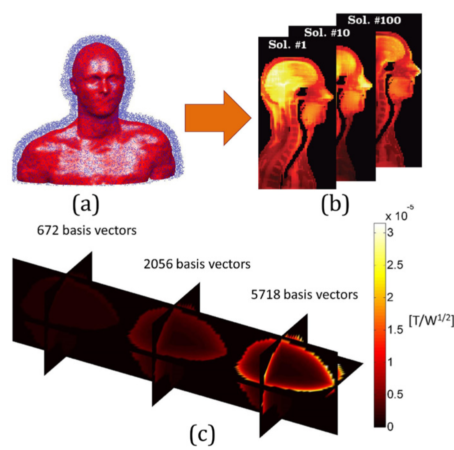
High and ultra-high field (3T, 7T, and beyond) MRI scanners allow improving the signal-to-noise ratio (SNR) and thus image quality. Increasing the frequency (and reducing the wavelength) leads to undesired effects, such as non-uniformity of the magnetic field components within the body, which is ultimately translated into loss of image contrast. Parallel MRI and parallel transmission techniques, using multiple receiving (Rx) and transmitting (Tx) channels, have been introduced to address some of these issues. However, in addition to the higher energy deposition in the body due to the increased field, the use of multiple excitation channels can lead to undesired effects that may increase the local power deposition in certain body areas. To comply with safety limits, the specific absorption rate (SAR), i.e., the rate at which energy is absorbed by the body when exposed to an electromagnetic (EM) field, must be locally monitored and limited. Based on constrained optimization and using the EM field distribution generated by each channel of a given coil array, the RF excitation pulses can be controlled to maximize SNR while minimizing the SAR.

The ultimate SNR and SAR are the best values that such optimization could achieve for any possible coil design. Their computation requires a complete basis for the EM fields in the sample under study, i.e., the body. Existing methods are based on analytical solutions, which only allow the computation of the ultimate SNR and SAR for simple homogeneous spheres and cylinders. Despite the insight gained from these metrics, MRI RF coils are intended for realistic body models. Therefore, results for highly complex inhomogeneous realistic body models can give extremely useful information, insight and intuition to coil designers, and define ultimate figures of merit against which to benchmark new prototype designs (Figure 1).

In collaboration with the RLE MRI group and the HST/MGH A. A. Martinos Center for Biomedical Imaging, we have developed a methodology for generating the basis for the EM fields that any coil design can induce in realistic human body models. The generation of this basis (illustrated in Figure 2) involves the combination of the integral equation formulation of the Maxwell equations, the concepts of the Huygens equivalence surface principle, the application of randomized singular value decomposition (SVD) approaches for the generation of a basis of extremely large operators, and the development of very fast volume integral equation solvers. This basis can be used to generate the ultimate SNR and SAR in realistic body models.



▲ Figure 1: (a) SAR versus flip angle curves, for 8 and 16 channels Tx arrays, and the ultimate solution. (b) Convergence of the SNR to the ultimate value with increasing number of vectors for 3 different brain positions. (c) SNR maps for 32, 64 and 128 channels Rx coil arrays, and ultimate values.



▲ Figure 2: (a) From body model and Huygens surface to (b) EM basis vectors. (c) Evolution of the SNR brain maps with increasing number of vectors.

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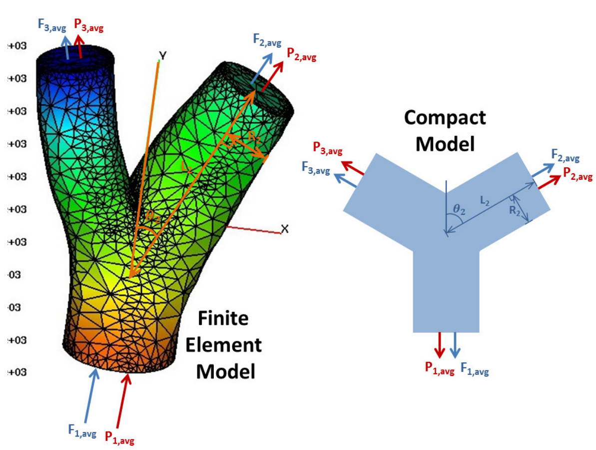
Compact Dynamic Modeling for Large-Scale Cardiovascular System Simulation

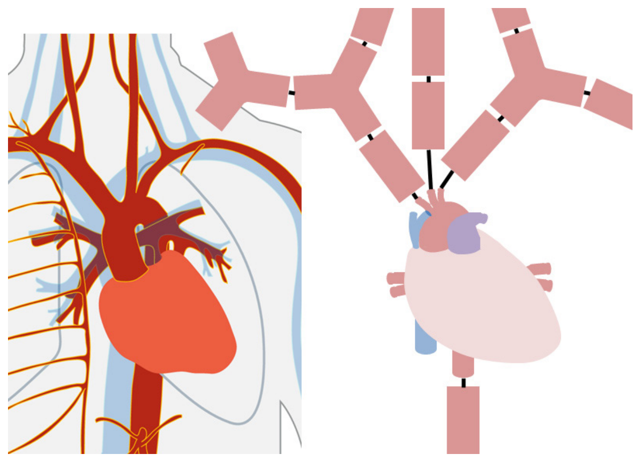
Y.-C. Hsiao, Y. Vassilevski, S. Simakov, L. Daniel
Sponsorship: MIT Skoltech Initiative

Diagnosing medical conditions based on non-invasive (or minimally invasive) measurements requires simultaneous modeling of both (1) local arteries in pathological states, and (2) global large-scale arterial networks from which pressure and flow are directly accessible. For instance, diagnosing atherosclerosis or an aneurysm requires the detailed pressure and flow inside local arterial bifurcation segments as for (1). Such fluid-mechanical interaction problems are solvable by finite-element methods (Figure 1). The simulated pressure and flow are compared against measurements to ensure model quality. However, because of the limited measurability of pressure and flow at pathological sites, it is crucial to develop accurate yet computationally tractable models for global arterial networks to correlate the pathological conditions with the measurements taken from larger vessels in global networks. The final diagnosis can be obtained by solving an inverse problem for the pathological parameters, for instance, aneurysm internal diameter, arterial wall thickness, plague stiffness, etc.

For this strategy to be effective, the model for such a complex large-scale artery network (Figure 2) is required to be compact, computationally tractable, and field-solver-accurate. We proposed an innovative technique to automatically generate nonlinear dynamic models via convex optimization. Our black-box technique trains nonlinear dynamic models using solutions from partial-differential-equation solvers or input-output signal measurements. The generated models are guaranteed to be numerically stable both when (i) simulated alone and (ii) interconnected with each other. This property enables hierarchical modeling: automatically modeling local sub-networks (e.g. a single or a set of artery branches) and then interconnecting local models to form a model of the global network (Figure 2). Through this approach, the physical information, such as artery geometries and full governing PDEs, can be fully exploited in generating training data without compromise due to enormous structure complexity. Our model quality is further enhanced by our automatic mechanism in selecting essential basis functions.



▲Figure 1: Left: Pressure profile of a bifurcation solved by finite element methods. The length of each branch is chosen such that Poiseuille flow is fully developed to satisfy network port assumptions. Right: Compact model generated by our algorithms.



▲Figure 2: Left: Physiological arterial network. Right: Arterial network model that consists of a heart model and local dynamic models of straight and bifurcation arteries.

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Towards Wireless Capsule Endoscopic Ultrasound (WCEU)

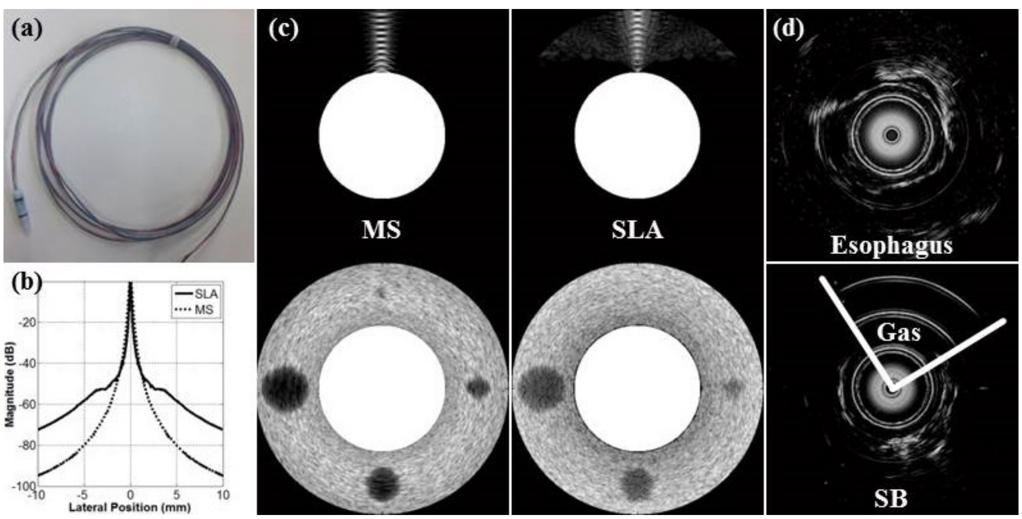
J.H. Lee, C.M. Schoellhammer, G. Traverso, D. Blankschtein, R. Langer, K.E. Thomenius, B. Anthony, D.S. Boning

Imaging of the small bowel (SB) is challenging due to its length and winding path. Wireless Capsule Endoscopy (WCE) provides convenient access to the SB but lacks ultrasound imaging capabilities necessary for accurate diagnosis. Wireless capsule endoscopic ultrasound (WCEU) combines the benefits of WCE and ultrasound imaging. This work evaluates transducer designs appropriate for WCEU in regard to image quality, system complexity, and cost and investigates whether the SB can produce sufficient contact to ensure acoustic coupling necessary for ultrasound imaging.

We evaluated mechanical-scanned (MS) and side-looking array (SLA). MS is implemented with a focused disc transducer and a motor; SLA uses TX and RX focusing with fixed F-numbers. Simulations of point and cyst phantoms were done using Field II. The MS tethered capsule developed for imaging feasibility study shown in Figure 1(a) consists of a 10 MHz transducer and a micro stepper motor with a 4 m long tether. *Ex vivo* pig tissue imaging was done to evaluate image quality. *In vivo* pig esophagus, stomach, and SB imaging were performed using the tethered capsule.

Simulation results are shown in Figures 1(b) and (c). MS performs better for both point and cyst imaging. SLA suffers in the near zone due to the small number of active elements and in the far zone due to large side lobes caused by the curvature of the capsule. Despite the motor, MS has a much simpler system than SLA, which requires a very large number of elements (> 400 for 10 mm φ at $\lambda/2$ spacing), multiplexing, parallel channel front-end and beamforming. MS power can suffer due to the motor, but SLA power suffers from a significantly more complex signal chain. With current transducer technology, the cost for SLA is prohibitively high to be a disposable device.

Figure 1 (d) shows *in vivo* images. Full circumferential coverage was difficult to maintain due to partial contact with the capsule. Peristalsis can potentially produce better coupling, but its effect could not be adequately examined due to reduced activity under anesthesia. With current technology, MS shows better performance overall. *In vivo* imaging shows promising results although the effects of peristalsis and resulting coverage need to be further investigated.



▲Figure 1: (a) Tethered capsule for experiment. (b) Beam profile comparison for SLA and MS. (c) Simulation of point and cyst imaging for MS and SLA. (d) Ultrasound image of esophagus and SB from pig *in vivo* experiment.

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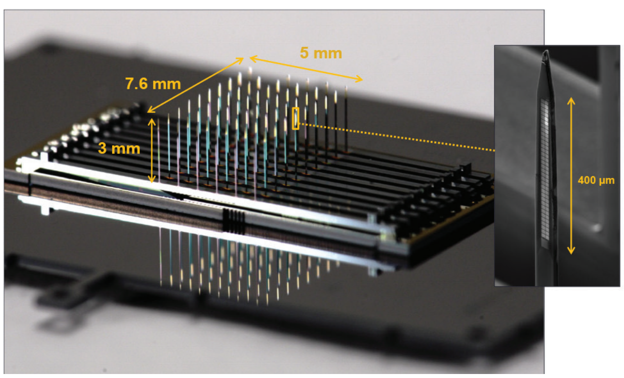
High-Density, Three-Dimensional Microelectrode Arrays for Neural Recording

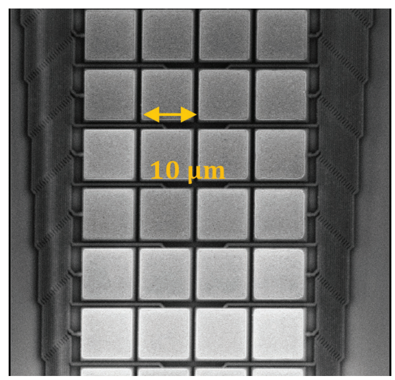
J. Scholvin, A.N. Zorzos, C.G. Fonstad Jr., E.S. Boyden
Sponsorship: Simons Center for the Social Brain, Allen Institute, NIH

Our research focuses on strategies for designing and fabricating three-dimensional microelectrode arrays, to be used for extracellular neural recording. Our designs have customizable electrode locations, targetable to specific neural substrates, and distributed in a volume throughout a neural network in the mammalian brain. We accomplish this by utilizing MEMS microfabrication techniques to create a number of planar structures that are mechanically and electrically assembled into a three-dimensional array (Figure 1). The resulting array consists of a large number of thin needles, and each needle contains many recording sites along its length. To pick up neural activity, exposed metal recording sites are located in along the length of each of the needles (Figure 2). These recording sites are routed along the needle and aggregated at the base of the array, for further routing, amplification and digitization off-chip.

Our approach relies on a number of innovations in different parts of the system design. We developed a simple and customizable toolset to automatically generate the different design components needed, which we then fabricate and assemble into a three-dimensional array. Further, we created mechanical and electrical connections for the arrays as well as packaging solutions aimed at head-fixed recordings in rodents. Finally, we are using electron beam lithography to define sub-micron pitched long metal lines for signal routing, which allows us to create very narrow needles that minimize tissue displacement.



▲ Figure 1: Photograph showing a 4080 channel 3-D probe, consisting of 6x10 needles. Each needle, as show in the insert, contains 68 high-density recording sites on its surface, arranged as two columns of 34 sites each.



▲ Figure 2: Electron micrograph of the high-density recording site configuration, for a four column configuration. Each recording site is approximately 10 µm in size, and densely packed so that the activity of a neuron is picked up by multiple sites simultaneously, enabling automated data analysis.

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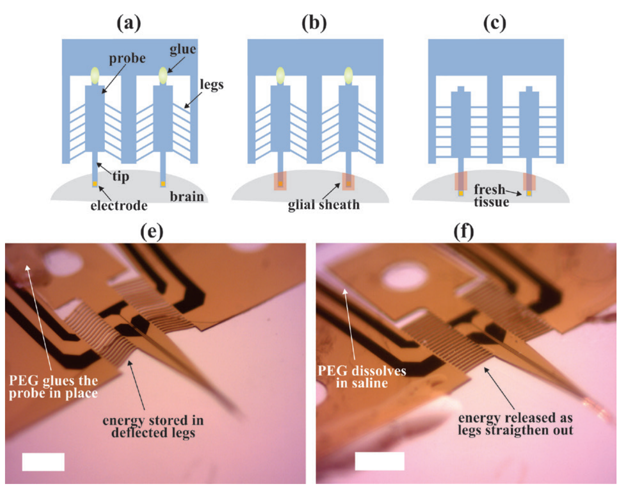
Reconfigurable Neural Probes for Chronic Electrical Recording

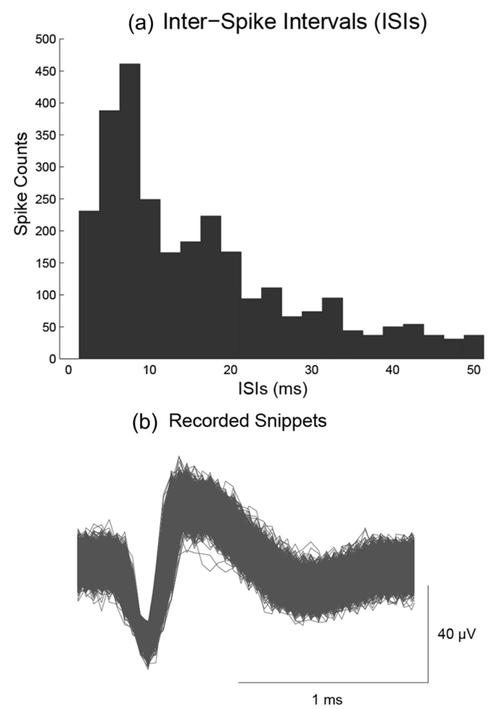
A. Dighe, U. Froriep, M. Sunshine, A. Ievins, P. Anikeeva, C. Moritz, J. Voldman
Sponsorship: National Science Foundation Center for Sensorimotor Neural Engineering (CSNE)

Chronic interfaces with the nervous system are critical for understanding basic neurobiology as well as for enabling new technologies that could be used in neurorehabilitation and in the treatment of various neurological disorders. A major challenge with current brain-computer interfaces is their inability to reliably record single-unit electrical activity over long periods of time (months) due to tissue reaction to foreign objects in the brain. This tissue reaction consists of a sheath of glial cells that encapsulates a neural probe a few weeks after implantation. Here we describe the design of a new neural probe that aims to bypass the body's immune reaction by changing shape once implanted in the brain, thereby providing the ability to chronically monitor neural activity *in vivo*.

Our reconfigurable electrode consists of a thin polymer probe whose body can be deflected and locked prior to insertion via a dissolvable glue such as polyethylene glycol (PEG), storing mechanical energy in the device legs (Figure 1a). After inserting into the brain and waiting for the initial glial sheath to form (Figure 1b), the device can be triggered by dissolving the glue, causing the recording tip of the device to penetrate into fresh tissue (Figure 1c). Designing the tip dimensions to be small (7-20 µm) should prevent the formation of an additional glial sheath post-triggering. We have demonstrated successful triggering and electrical recordings from this device in an acute setting in the rodent brain (Figure 2). This technology holds promise for creating chronic interfaces for recording stable neural activity.



▲ Figure 1: (a) Schematic showing probe deflected and glued prior to insertion into brain. (b) A glial sheath forms over time (~weeks). (c) Dissolving the glue triggers the probe body, pushing it into fresh tissue. (e, f) Photographs of device before and after deployment. Scale bars = 500 µm.



▲ Figure 2: Inter-spike interval (ISI) histogram (top) and time-amplitude sorted waveforms (bottom) recorded intra-operatively immediately following device insertion in a rodent motor cortex.

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Thermal Drawing of Minimally Invasive Neural Probes

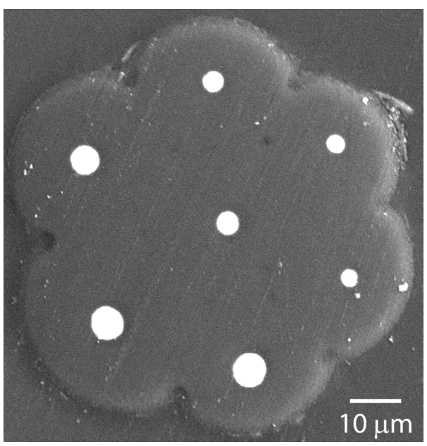
A. Canales, C. Tringides, U.P. Froriep, Y. Fink, P.O. Anikeeva
Sponsorship: National Science Foundation, McGovern Institute for Brain Research, Simons Center for the Social Brain

Understanding the mechanism of debilitating neurological conditions and to enable treatment of these conditions requires reliable recordings of neural activity. Currently available neural probes, however, are limited by deterioration of the electrode-tissue interface supposedly caused by glial scarring and neuronal death around the probe.

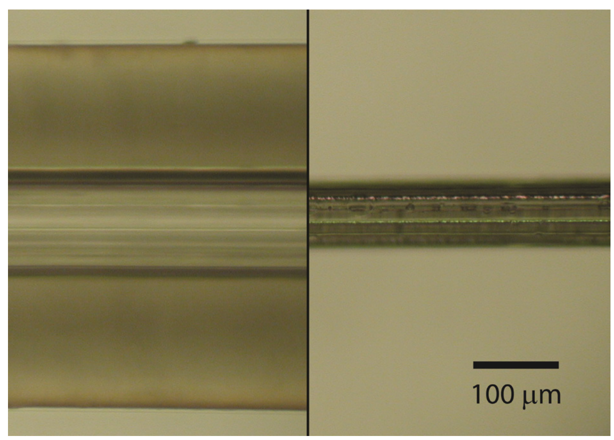
It has been hypothesized that the two main characteristics of neural probes leading to scarring and inflammatory tissue response are the size and the mechanical flexibility of the probe. Thus, flexible, minimally invasive neural probes could be invisible to the neural tissue, and thus could help to decrease tissue response to the device.

To fabricate this kind of probes we apply a thermal drawing process. To this end we start with a template (~2.5-4 cm in diameter), and apply controlled heat and stress to obtain hundreds of meter long fiber with preserved cross-sectional geometry, but reduced in diameter to the micrometer scale. This way, the recording surface of the electrodes can be tuned down to <1 µm, while maintaining controlled pitch.

To achieve a device with low bending stiffness, making it a promising candidate for minimally invasive recordings in neural tissue, we insulated electrodes using two polymer types. In addition, different chemical properties of these two polymers make it possible to employ chemical etching to further modify the geometry of the fiber. The latter allows us to reduce the size of the probe that incorporates 7-10 electrodes to an overall diameter <100µm. Our *in vivo* studies show that the fiber probes record neural activity with a signal-to-noise ratio of up to 20.



▲Figure 1: Cross-section of the neural probe. metal electrodes (white) are cladded by a polymer that provides electrical insulation and mechanical support.



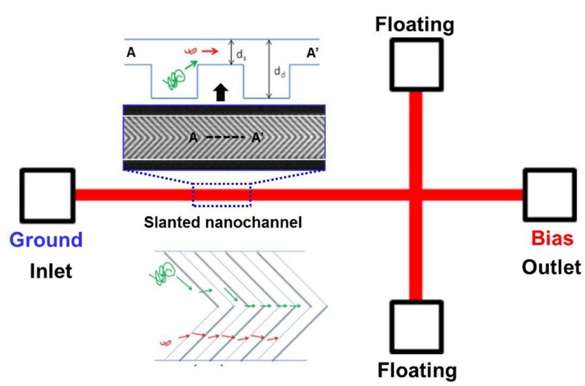
▲Figure 2: Comparison of the fiber before (left) and after (right) etching the polymer cladding. This process increases the mechanical flexibility and decreases the size of the probes.

Size-based Biomolecule Preconcentration using Herringbone Nanofilter Arrays

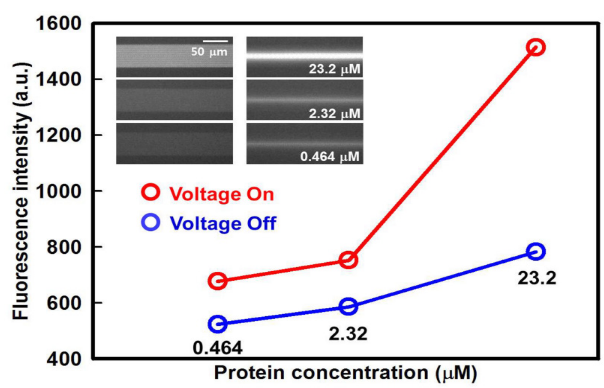
S.H. Ko, J. Han
Sponsorship: DARPA

Micro- and nanofluidic-base sample analysis chips (e.g., labs-on-a-chip) have many advantages over traditional benchtop analyzers, but they suffer from poor detection efficiency because of small sample volume and low optical path length. As a result, many research groups have developed and demonstrated high-performance detection tools (enhancing detection sensitivity) and sample preconcentration methods (directly enhancing signal). Of these, our group has focused on developing mobility-base preconcentrators (charge to size ratio). We recently designed a new size-base biomolecule preconcentrator. This device consists of herringbone nanofilter arrays (HNAs) with periodically patterned deep and shallow nanoslits, as in Figure 1. By the Ogston sieving theory, while small molecules are more likely to flow across in a straight line, large ones are more likely to move toward the center of HNAs, so that relatively large molecules, compared to shallow nanoslit dimensions, can be focused on the center of the device. We demonstrated the preconcentration using trypsin inhibitor (21 kDa), which is denatured by SDS surfactant and heat, and labeled by non-covalent dye, as in Figure 2. In this device, the preconcentration factor and limit of detection (LOD) are about 7 times and 2.32 μm, respectively.

In general, size-based separation methods using nanofilter arrays have diffusion and dispersion issues in the downstream and low optical path length, which lead to a low detection signal. Since the operating mechanism of the HNA is consistent with that of existing nanofilter-base biomolecule separation devices, it is easier to integrate the HNA with the separation device than the mobility-base preconcentrator through standard fabrication. This method enables simultaneous preconcentration and separation of biomolecules in a single chip with operational simplicity, robustness, and minimal sample use. In addition, the HNA makes biomolecules with different sizes have their distinct trajectories and different extents of preconcentration factor, which results in an efficient continuous flow immunoassay.



▲ Figure 1: Schematic of HNAs with periodically patterned deep (120 nm) and shallow (60 nm) nanochannels. Driving force is electrophoresis (inlet-ground, out-positive bias).



▲ Figure 2: Demonstration of denatured trypsin inhibitor preconcentration. Red circles represent preconcentrated proteins, and blue ones are non-preconcentrated proteins. Inset images are fluorescence images before (left) and after (right) preconcentration.

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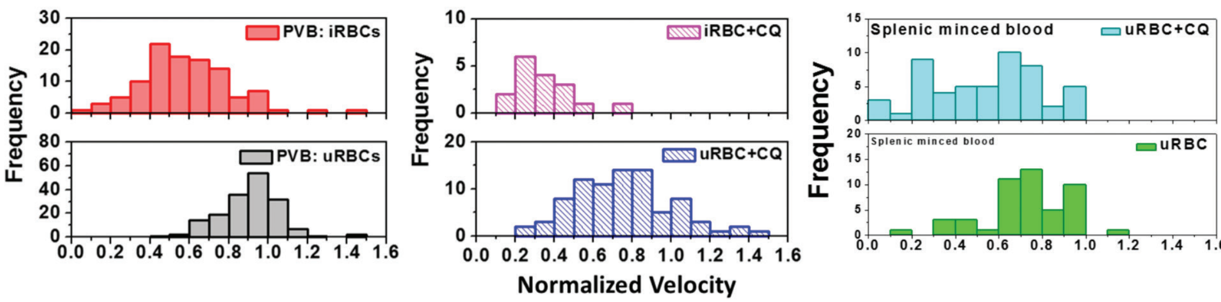
Red Blood Cell Deformability and Splenic Clearance in *Plasmodium yoelii* Infected Mice

S. Huang, A. Amaladoss, M. Liu, H. Chen, R. Zhang, P. Preiser, M. Dao, J. Han
Sponsorship: SMART

During *Plasmodium yoelii* infection, the mechanical filtration of red blood cells in spleen plays an important role in the host's defense against malaria parasites (*1*). Small changes in RBC deformability may significantly impact on the pathophysiological outcome (*2*). In this project, we attempted to gain a better understanding of malaria pathology through the mechanical retention of RBC in spleen. We independently studied the *in vitro* and *in vivo* impacts of malaria infection and/or drug treatment on RBC deformability(*3, 4*). With the microfluidic platform, the dynamic deformability of RBCs were quantitatively measured. Several important aspects pertaining to anemia and splenic retention were explored.



▲Figure 1: uninfected and infected RBC deformability (velocity) from peripheral blood (left). The effect of antimalarial drug chloroquine drug treatment on peripheral blood deformability (middle) as well as on splenic blood deformability (right)

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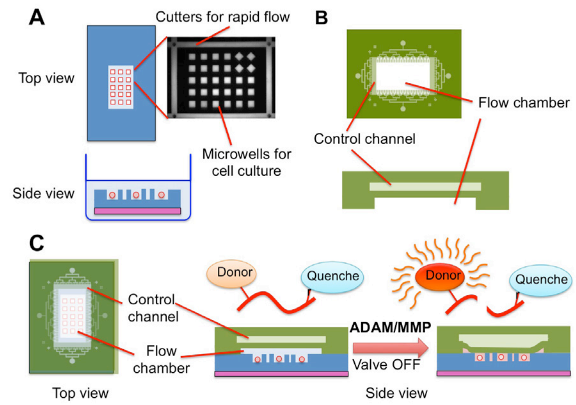
Microwell-based Platform For Single-cell Pericellular Protease Detection

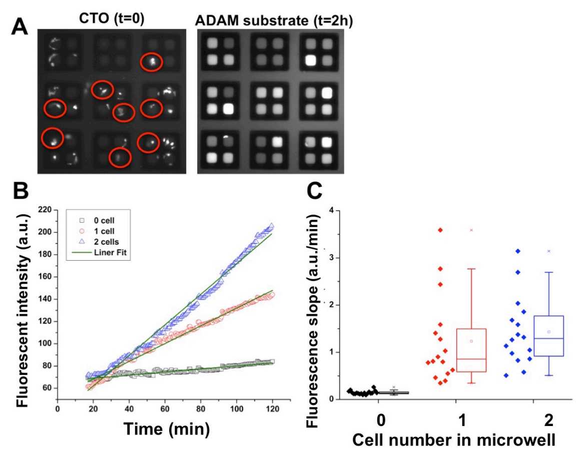
L. Wu, J. Han
Sponsorship: Biosystems & Micromechanics IRG, SMART

Pericellular proteases, including those on cell surfaces and secreted ones, act as a key component of autocrine signaling and impact the microenvironment of individual cells. In particular, A disintegrin and metalloproteinases (ADAMs), which are typical kinds of pericellular protease expressed on cell surfaces, have been linked to various clinical pathological processes, including breast cancer progression. On one hand, previous studies suggest that the heterogenous single-cell protease activity could lead to diverse cellular responses in terms of intracellular kinase activation profiles or cell migration patterns, emphasizing the need for single-cell study of pericellular protease response. On the other hand, no tool is available to measure the catalytical activity of those membrane-bound proteases directly at single cell level. In this work, we present a high-throughput microfluidic platform capable of monitoring single-cell pericellular protease activity.

The designed platform consists of two pieces (Figure 1). The bottom one has a microwell array pattern for cell culture; the top one includes a 2-layer structure for the valving function. Upon assembly of these two pieces by holding them together via mechanical clamping, one can pressurize the control layer of the assembled device to isolate individual microwells rapidly on demand. Thus the cell-surface protease activity measurement can be conducted by confining cells in individual microwells with diffusive FRET-based substrates. We tested the platform with HepG2 cells challenged with 1uM PMA, which is known as a strong stimulator for the shedding of several ADAM17 protease substrates. As shown in Figure 2, microwells of different cell numbers display fluorescent intensity profiles with diverse increasing rates, which are indicators for the protease activity level. These results confirm both the existence of heterogeneity in single-cell ADMA17 protease activity and the feasibility of our platform for studying the pericellular protease behavior of single cells.



▲ Figure 1: Schematic of microfluidic platform for single-cell protease activity measurement. Upon assembly (C) of bottom (A) & top pieces (B), the valve control layer allows pneumatic actuation of flow chamber ceiling to control the closing and opening of microwells.



▲ Figure 2: Heterogeneous protease response of HepG2 cells treated with 1uM PMA. (A) HepG2 cells stained with cell tracker orange (CTO) were confined in closed microwells with FRET-based substrate. Substrate fluorescence after 2h incubation is shown on right. (B) Representative fluorescent profile for microwells of different cell numbers. (C) Box plot of fluorescent slope for each microwell with 0, 1, or 2 cells.

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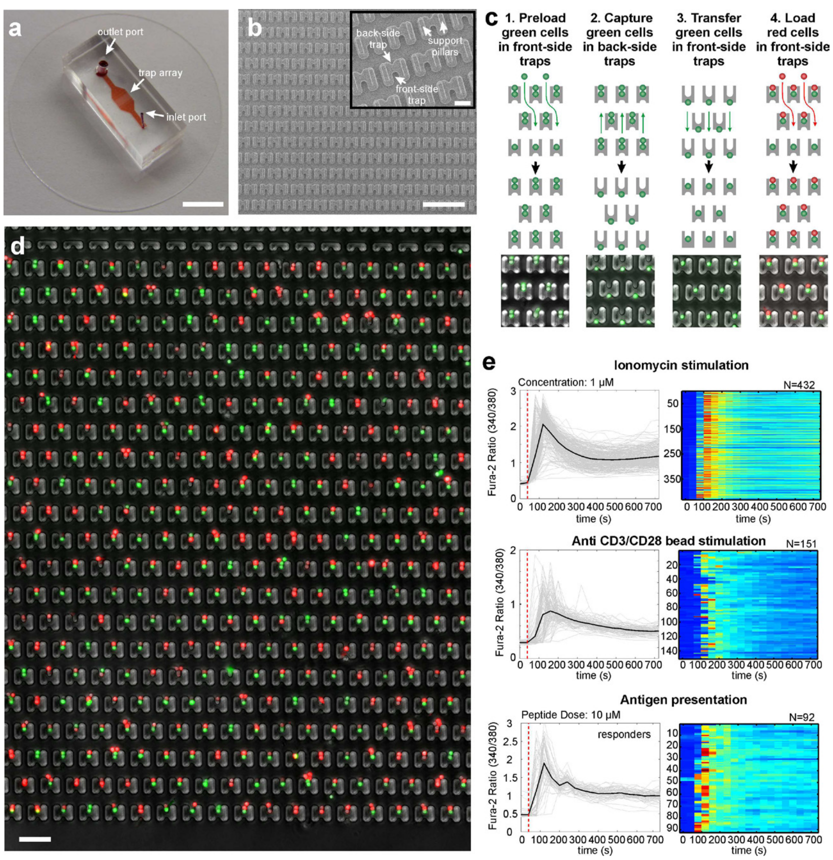
Cell Pairing for Studying Immunity

B. Dura, J. Voldman
Sponsorship: Singapore-MIT Alliance

Many immunological responses are mediated through direct cell-cell interactions. Engagement of immunoreceptors with their corresponding ligands initiates an intracellular signaling cascade that leads to a diverse array of responses including selection, differentiation, proliferation, and cytokine production. Our understanding of how immune responses are shaped by these interactions relies on our ability to examine direct dynamic interactions between immune cells and their partners. Methods to study these immune cell interactions, however, suffer from limited throughput and a lack of control over cell pairing. These limitations prevent statistical inference and complicate experimental analysis, thereby hindering their widespread use.

To address the major shortcomings of current approaches, we developed a microfluidic cell pairing platform for studying immune cell interactions for numbers of cell pairs that afford meaningful statistical analysis (see Figure 1). The platform achieves cell pairing with accurate control in space and time with one-to-one interacting partners, well-defined and synchronous initiation of interaction, and enduring contacts. It enables the use of minimal numbers of primary immune cells (~10^4 cells) and also allows control of the soluble microenvironment by exchange of media without losing cell registration. The pairing technique is compatible with pharmacological, antibody-based, and cellular modes of immune cell stimulation and enables us to examine the early interaction dynamics of immune cells in a highly controlled manner with quantitative analysis of their response profiles.



◀Figure 1: Microfluidic device for immune cell pairing. (a) Image of device. (b) SEM image of cell trap array. (c) Four-step cell loading and pairing protocol. (d) Overlaid phase contrast and fluorescence images showing primary mouse lymphocytes stained with DiI (red) and DiO (green) membrane dyes paired in traps. (e) Ca+ responses of OT-1 CD8 T cells with pharmacological (ionomycin), antibody-bead based (anti-CD3/28) and cell-based (SIINFEKL-loaded antigen presenting cells) stimulations. Scale bars: (a) 5`mm, (b) 100`μm, 20 μm (inset), (d) 50`μm.

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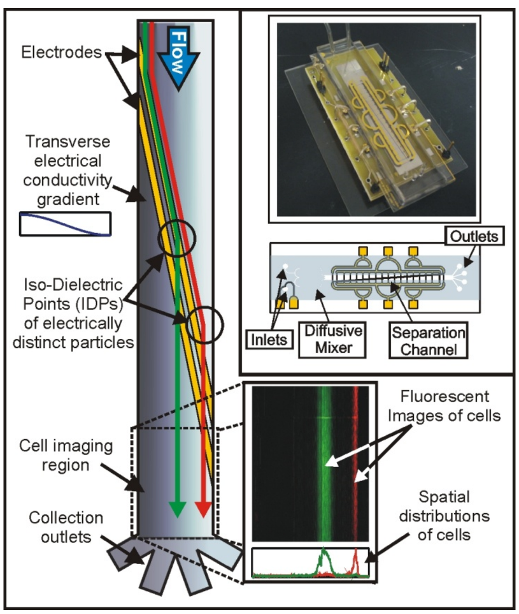
Iso-dielectric Separation of Cells and Particles

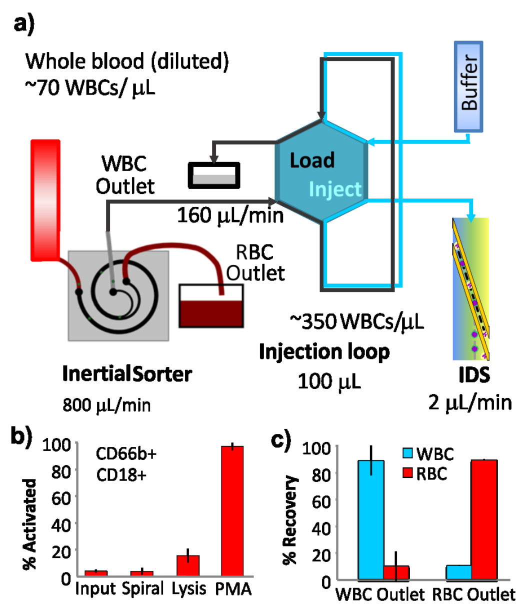
H.W. Su, J. Voldman
Sponsorship: DARPA

The development of new techniques to separate and characterize cells with high throughput has been essential to many of the advances in biology and biotechnology over the past few decades. We are developing a novel method for the simultaneous separation and characterization of cells based upon their electrical properties. This method, iso-dielectric separation (IDS), uses dielectrophoresis (the force on a polarizable object) and a medium with spatially varying conductivity to sort electrically distinct cells while measuring their effective conductivity (as in Figure 1). It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis to concentrate cells and particles to the region in a conductivity gradient where their polarization charge vanishes.

Sepsis is an uncontrolled activation of the immune system that causes an excessive inflammatory response. There is an unmet need to develop tools to monitor sepsis progression, which occurs quickly and provides few clues to indicate if treatment is effective. Previously, we have found that the electrical profile of leukocytes changes with activation state. To rapidly measure the electrical profile of leukocytes from whole blood, we have integrated IDS with the spiral inertial microfluidic sorter for leukocyte isolation using an injection loop (see Figure 2a). The spiral inertial sorter minimizes the effect of activation during leukocyte isolating (Figure 2b) and results in depletion of 90% of erythrocytes and recovery of 90% of leukocytes (Figure 2c). This integrated microfluidic system provides a simple assay to monitor sepsis progression in nearly real time.



▲Figure 1: IDS microfluidic device used to measure electrical properties of the cells. The spatial conductivity gradient makes cells with different electrical properties pass through the electrodes at different positions (Iso-Dielectric Point - IDP).



▲Figure 2: Integrated IDS system with inertial sorter. (a) A spiral inertial microfluidic sorter isolates leukocytes and stores them in injection loop (Load mode). Injection loop then pushes cells into IDS device for enumeration and electrical characterization (Inject mode). (b) Comparison of leukocyte activation level before input, after spiral sorter, after RBC lysis buffer, and after PMA treatment (positive control). Spiral sorter has smaller effect on activation than RBC lysis buffer. (c) Spiral sorter removes 90 % RBCs; it recovers 90% of WBCs.

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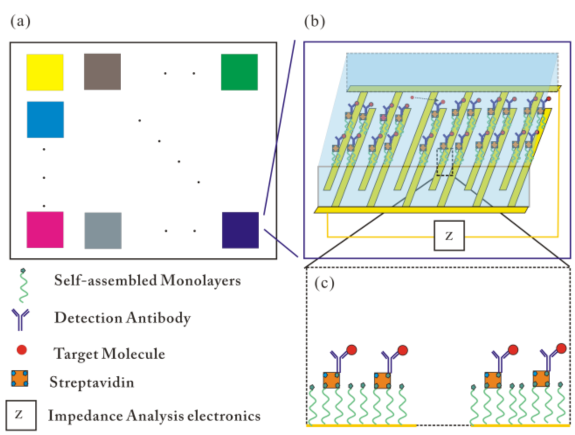
Microfluidic Electronic Detection of Protein Biomarkers

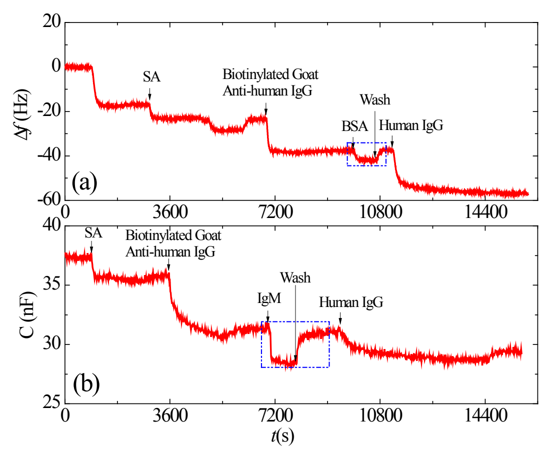
D. Wu, J. Voldman
Sponsorship: Maxim Integrated

Immunoassays use antibodies to detect protein biomarkers, with a substantial market and significant clinical importance. However, traditional immunoassays are performed in centralized laboratories using optical methods, which means results take days and they cannot be highly multiplexed, in turn increasing patient visits, healthcare costs, and decreasing healthcare outcomes. We are developing all-electronic immunoassays with which we can 1) achieve high-throughput, potentially measuring all protein biomarkers in blood samples; 2) reduce cost by taking advantage of the decreasing cost of silicon electronics; and 3) deliver results to patients before they meet with their physicians.

The biosensor is illustrated in Figure 1: samples are loaded into the microfluidic channel, antigens specifically bind to antibodies on intergidital electrodes (IDEs), and finally the presence of antigens is captured by capacitance change due to the binding. To immobilize antibodies onto IDEs, the surface was modified using self-assembled monolayers and specific binding between biotin and streptavidin (SA). The surface modification was first tested on gold crystal and characterized using quartz crystal microbalance monitoring with dissipation (QCM-D). As Figure 2(a) shows, the decrease of frequency after introducing SA, antibody [biotinylated goat anti-human Immunoglobulin G (IgG)] and antigen (human IgG) indicated their bindings. The surface also suppressed nonspecific binding because non-specifically attached bovine serum albumin (BSA) was removed by simple washing (as in the rectangle). The surface modification was then applied on the sensor. The capacitance during surface modification was measured [see Figure 2(b)]. The capacitance decrease caused by nonspecific binding [Immunoglobulin M (IgM)] was recovered by washing (as in the rectangle), which was consistent with the QCM-D result that nonspecifically bound proteins were removed by washing. The specific binding of SA, antibody and antigen was correctly revealed by decrease of capacitance and thus validated the electronic detection of protein biomarkers.



▲ Figure 1: (a) Illustration of multiplexed all-electronic biosensors. (b) Illustration of one pixel of the sensor. (c) Cross-section of one pixel.



▲ Figure 2: (a) QCM-D measurement of protein binding to gold crystals; blocking was applied before and washing was applied after introducing SA, antibody, and antigen; the two are not labeled; (b) Electric measurement of protein binding to gold IDEs; washing was also applied after introducing these proteins but is not labeled.

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Cell-based Sensors for Measuring Impact of Microsystems on Cell Physiology

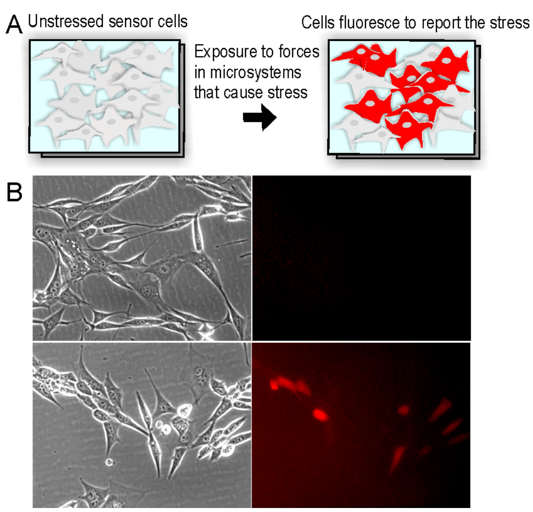
A. Fendyur, S. Varma, J. Voldman
Sponsorship: NIH

The use of microsystems to study and manipulate cells has rapidly advanced in recent years. However, along with the increase in usage comes a growing concern regarding the toxic impact of such microsystems on cell physiology. DNA damage and heat shock are possible adverse outcomes caused by various forces generated in microsystems. In addition, flows within such systems generate fluid shear stress that may adversely affect cell health as well. In this project, we are developing a set of cell-based fluorescent sensors to measure DNA damage, heat shock and shear-induced stress experienced by cells in microsystems. Toxicity assays using cells, engineered to express fluorescent protein driven by an activation of a molecular pathway offer high-throughput, user-friendly and non-destructive alternative to assess gene expression (see Figure 1a).

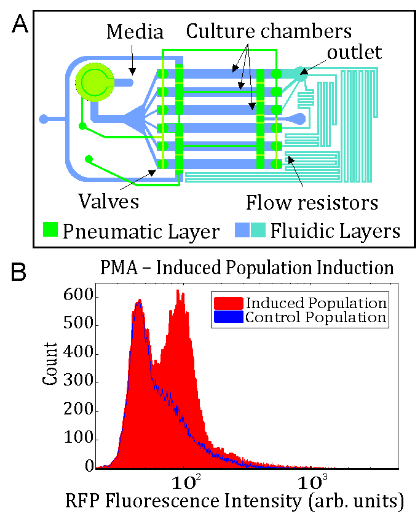
To assay DNA damage, we engineered NIH-3T3 cells to fluoresce upon p53-p21-DNA-damage pathway activation by expressing red fluorescent protein (RFP) (see Figure 1b). Creating the shear-stress sensor was challenging because the relevant molecular pathways have not been entirely elucidated. We characterized the gene expression profile of NIH-3T3 cells using a multi-flow microfluidic device that can simultaneously apply logarithmic (1000×) range of shear stress conditions (as in Figure 2a) and using the qRT-PCR-based approach to identify the shear sensitive genetic node we designed an RFP-reporter plasmid. NIH-3T3 cells were transfected to create shear stress response sensor. We successfully verified our sensor functionality by noting correlating fluorescence response to PMA (chemical inducer of flow shear stress pathway) by flow cytometry (Figure 2b).

For the heat-shock reporting sensor we re-engineered our existing heat shock sensor to express RFP as the activation color, similar to DNA damage and shear stress reporting sensors.

A number of sensors can be combined for multiplexed analysis of multiple stresses at once, as might be experienced in a typical microsystem. Each sensor can be identified by the different constitutive color it expresses.



▲ Figure 1: a) Approach to quantify stress caused by forces generated in microsystems using our sensor. b) DNA damage reporting sensor (upper panel). 24 hrs after DNA damage caused by methyl methanesulfonate - DNA alkylating agent (lower panel), cells fluoresce to report the stress.



▲ Figure 2: a) Perfusion device layout. Cells are seeded in six chambers simultaneously and experience logarithmic shear stress based upon connectivity to fluid flow resistors. b): Histograms of fluorescent intensity of reporter control (blue) and PMA-induced (100 ng/ml) population. The shift towards higher RFP intensity due to PMA proves functionality of designed plasmid and reporters.

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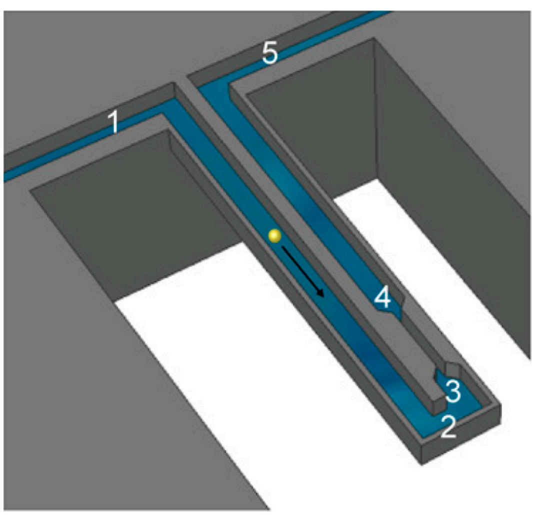
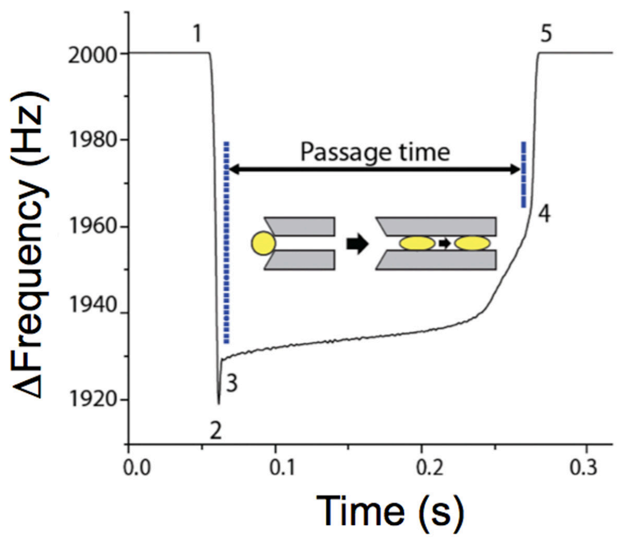
Characterizing Deformability and Surface Friction of Cancer Cells

S. Byun, S. Son, D. Amodei, N. Cermak, J. Shaw, J.H. Kang, V.C. Hecht, M. Winslow, T. Jacks, P. Mallick, S.R. Manalis
Sponsorship: NIH

Metastasis requires the penetration of cancer cells through tight spaces, which is mediated by the physical properties of the cells as well as their interactions with the confined environment. Various microfluidic approaches have been devised to mimic traversal in vitro by measuring the time required for cells to pass through a constriction. Although a cell's passage time is expected to depend on its deformability, measurements from existing approaches are confounded by a cell's size and its frictional properties with the channel wall. We developed a device (Figure 1) that enables the precise measurement of: i) the size of a single cell, given by its buoyant mass, ii) the velocity of the cell entering a constricted microchannel (entry velocity) and iii) the velocity of the cell as it transits through the constriction (transit velocity). Changing the deformability of the cell by perturbing its cytoskeleton primarily alters the entry velocity, whereas changing the surface friction by immobilizing positive charges on the constriction's walls primarily alters the transit velocity, indicating that these parameters can give insight into the factors affecting the passage of each cell. When accounting for cell buoyant mass, we find that cells possessing higher metastatic potential exhibit faster entry velocities than cells with lower metastatic potential. We additionally find that some cell types with higher metastatic potential exhibit greater than expected changes in transit velocities, suggesting that not only the increased deformability but reduced friction may be a factor in enabling invasive cancer cells to efficiently squeeze through tight spaces.



▲Figure 1a: Suspended microchannel resonator (SMR) with a constriction (6 μm wide, 15 μm deep, and 50 μm long) located at the apex. A cell passing through an embedded microfluidic channel is deformed as it flows into the constriction. Numbers 1-5 indicate different positions within the microchannel to demonstrate the trajectory of a cell flowing inside the channel.



▲Figure 1b: The resonant frequency response of the SMR as the cell passes through the microfluidic channel. The numbers 1-5 correspond to the position of the cell in the cantilever, as marked in (A). The height of the peak corresponds to the buoyant mass of the cell (1 → 2). The cell slows down as it deforms to enter the constriction (entry), and then speeds up as it travels through the constriction (transit). The passage time corresponds to the sum of the entry and transit times (3 → 4).

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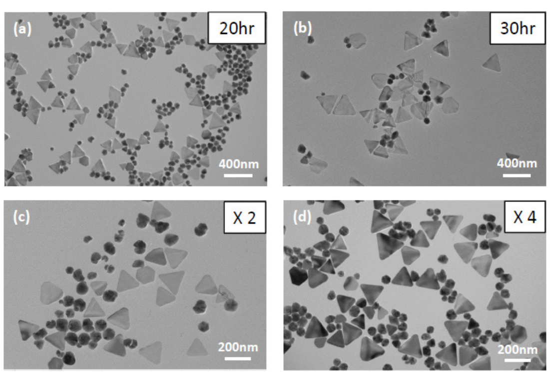
Synthesize Silver Nanoprisms by a Thermal Growth Method

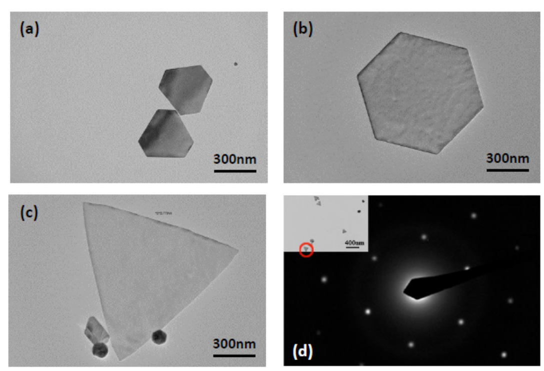
Y. Yang, M. Klug, Q. Hu, D. Jin, N. Fang
Sponsorship: National Science Foundation, Air Force Office of Scientific Research

Silver nanoprisms are plasmonic nanostructures that have attracted much attention because of their strong shape-dependent optical properties and related applications, e.g., surface-enhanced Raman scattering, near-field optical probes, and contrast agents for biomedical imaging. The chemically synthesized silver nanoplates have an extraordinary anisotropy due to the large ratio of lateral dimension to thickness. They support low-loss localized surface plasmon resonance and extremely high electromagnetic-field enhancement. Recently several methods have been developed to synthesize the silver triangular nanoprisms, such as NaBH4 reduction, light-mediated growth, thermal growth.

Here we synthesize silver nanoprisms via a thermal growth method and investigate the dependence of the nanoprisms' size, shape, and concentration on the chemical reaction conditions. We first change the reaction time. As shown in Figure 1(a) and (b), for longer reaction times the size of nanoprisms is larger, but the concentration is smaller. Most nanoprisms are triangles. In Figure 1(c) and (d), the poly (vinyl pyrrolidone) (PVP) solution is condensed by 2 times and 4 times, respectively, compared to the original value mentioned in Washio et al. We find the size and concentration have no obvious changes. It is interesting that when we dilute the PVP solution, shapes other than triangles appear. For example, the triangles with missing corners (Figure 2(a)), the hexagons (Figure 2(b)), and the triangles with huge size (Figure 2(c)). The thermally grown silver nanoprisms have good crystalline structure, which is demonstrated by X-ray diffraction (XRD) measurement (Figure 2(d)). Therefore, we have grasped a definitive procedure for the synthesis of silver nanoprisms based on the thermal growth method. The nucleation and growth of triangular prisms are kinetically controlled by the reduction rate and PVP concentration. These results are valuable for the study of nanoparticle-based photonic and plasmonic devices.



▲Figure 1: TEM images of thermally synthesized silver nanoprisms with different reaction times (a) 20hr and (b) 30hr and condensed PVP solutions whose concentrations are (c) 2- and (d) 4-times more than original solution.



▲Figure 2: (a)-(c)TEM images of thermally synthesized silver nanoprisms with different facial shapes. (d) Detected XRD pattern shows crystalline structure in the silver nano-prisms.

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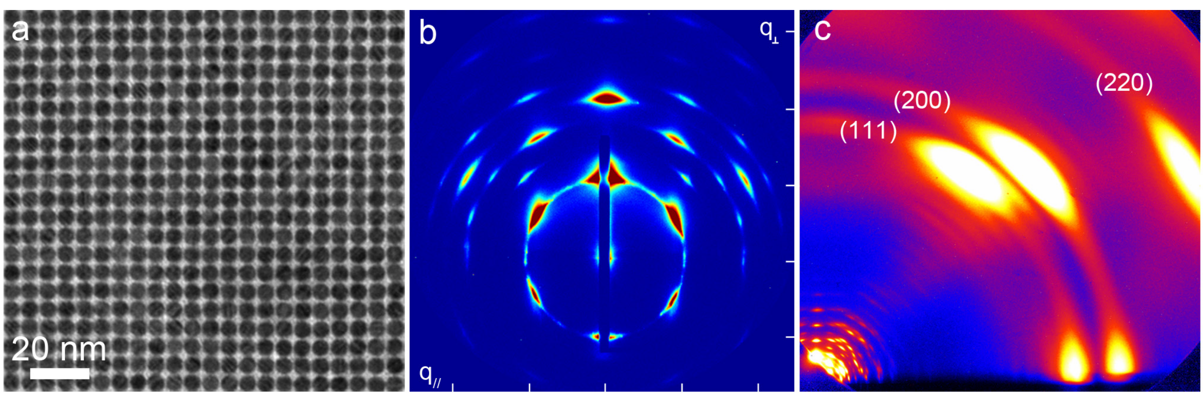
Large-Area Self-Assembly of Lead Sulfide Nanocrystals

M. Weidman, R. Hoffman, W. Tisdale
Sponsorship: Department of Energy, National Science Foundation GRFP

Lead sulfide (PbS) nanocrystals, or quantum dots (QDs), are a useful material because their band gap is dependent on their physical size. By synthesizing the QDs to have diameters in the range of 4-8 nm, we are able to tune their light absorption and emission over a wavelength range of 1000-1800 nm. This tunability makes PbS QDs attractive for applications such as photovoltaics, photodetection, and near-infrared light emission. In most of these applications, the colloidal QDs are deposited as a thin film for their end use. In these thin films, it is desirable to have the QDs assembled in a well-ordered arrangement so as to (1) maximize the amount of QDs in a given volume and (2) maximize the rate at which charge carriers can move throughout the film.

Through synthesis of QD ensembles with low size dispersity (size distribution standard deviation < 3% mean size), we have observed large-area self-assembly of these nanocrystals into highly ordered superlattice structures. These superlattices can be formed through simple laboratory methods such as drop-casting or spin-coating. Figure 1a presents a transmission electron micrograph of a QD superlattice that is approximately 6 layers thick into the plane of the image. We have prepared large-area films by drop-casting concentrated suspensions of the QDs onto silicon wafers, resulting in a 1x1 cm film. The grazing-incidence small-angle X-ray scattering pattern from such a film is shown in Figure 1b. The discrete, high intensity pattern indicates the formation of a single crystal superlattice that indexes to that of a body-centered cubic structure. We present the wide-angle X-ray scattering pattern of the same sample in Figure 1c, which shows that the atomic planes of the individual nanocrystals are aligned in the film as well. This degree of ordering ensures a high packing density for the QDs and could lead to interesting transport properties within the film.



▲ Figure 1: a) Transmission electron micrograph of a QD superlattice. b) Grazing-incidence small-angle X-ray scattering pattern for a large-area (1x1 cm) film of the QDs. The peak locations index to that of a body-centered cubic superlattice. c) Wide-angle X-ray scattering pattern showing that the atomic planes of the QDs are aligned for the same sample used in (b). Atomic planes are labeled in white.

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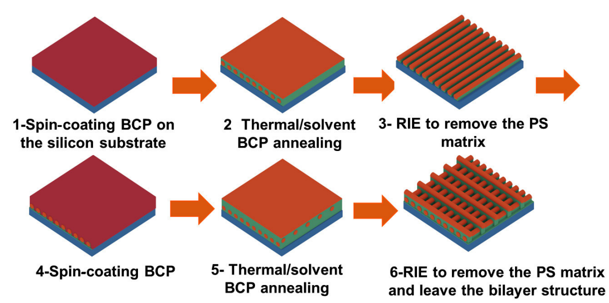
Using Self-Assembled Block Copolymer Patterns to Template Bilayer Mesh Structures

A. Tavakkoli K.G., S.M. Nicaise, W. Bai, C.A. Ross, K.K. Berggren
Sponsorship: SRC, FENA Center, National Science Foundation, TSMC

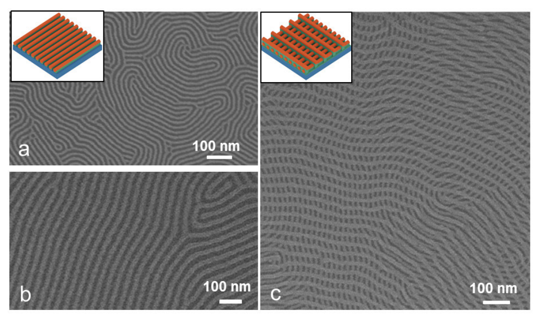
Mesh-shaped patterns are needed for applications such as metamaterials and next-generation integrated circuit architecture in which high throughput of dense features will be required. Our previous studies showed that with arrays of majority-functionalized posts fabricated by electron-beam lithography (EBL), we controlled bilayers of block copolymer (BCP) cylindrical microdomains and fabricated a variety of complicated structures including mesh-shaped patterns. This work required EBL fabrication, difficult in a large-area manufacturing process. In the current study we investigated an EBL-free process for fabricating bilayer mesh structures. We used BCP patterns as templates to self-assemble another BCP layer of the same or different molecular weight, the latter on top of the former.

Figure 1 describes the main steps of the fabrication process. In the first step, poly(styrene-dimethylsiloxane) (PS-PDMS) BCP was spin-coated on the surface of a silicon substrate. Thermal or solvent annealing was used to promote microphase separation and reactive ion etch (RIE) was used to remove the PS matrix and leave the pattern. Next the second layer of PS-PDMS BCP was spin-coated on the patterns and self-assembled with annealing. Finally, RIE removed the PS matrix and left a mesh-shaped bilayer cylinder structure.

Figure 2 (c) shows one of the results of the described process. In this figure, a bilayer rectangular mesh-shaped structure was formed using a 53 kg mol^{-1} PS-PDMS, as in Figure 2(b), on top of a 16 kg mol^{-1} PS-PDMS, as in Figure 2(a). In other systems, BCPs have been shown to orient perpendicular to underlying periodic patterns because the free energy for perpendicular orientation of the second BCP to the bottom pattern is lower than parallel orientation. The layers in Figure 2(c) are not orthogonal all across the substrate because the bottom BCP pattern was poorly oriented. In order for the mesh to be orthogonal, the bottom BCP pattern can be templated.



▲ Figure 1: The major steps of bilayer mesh-shaped structure fabrication.



▲ Figure 2: SEM images of (a) single layer of cylinders from 16 kg mol^{-1} PS-PDMS BCP on silicon substrate, (b) single layer of cylinders from 53 kg mol^{-1} PS-PDMS BCP on silicon substrate, (c) bilayer of 53 kg mol^{-1} PS-PDMS on 16 kg mol^{-1} PS-PDMS cylinders.

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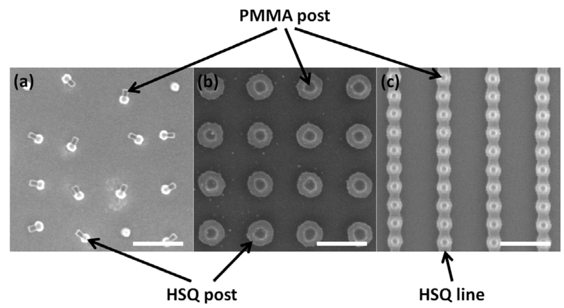
Three-Dimensional Nanofabrication Using HSQ/PMMA Bilayer Resists

H. Do, J. Chang, K.K. Berggren
Sponsorship: Taiwan Semiconductor Manufacturing Company, National Science Foundation

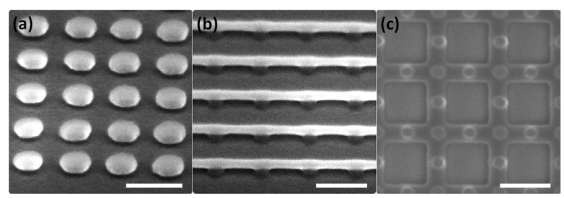
Three-dimensional (3D) devices offer unique advantages over planar devices but are difficult to fabricate. Therefore, a simple and rapid fabrication process for complex 3D nanostructures is necessary. Methods for fabricating such 3D nanostructures using electron-beam lithography (EBL) include consecutive overlay exposures or low and high electron energy exposures. However, these approaches require alignment markers and accurate alignment routines. Here, we describe a self-aligned method of fabricating 3D nanostructures using EBL of hydrogen silsesquioxane (HSQ) and poly(methylmethacrylate) (PMMA).

We used a HSQ/PMMA bilayer resist stack with HSQ as the top layer and PMMA as the negative-tone bottom layer. A dot array was exposed on the bilayer resist stack with the dose necessary to achieve negative-tone PMMA. After exposure, the samples were sequentially developed in salty developer to remove unexposed HSQ, methyl isobutyl ketone (MIBK) and isopropanol (IPA) to remove lightly exposed PMMA, and acetone to remove unexposed PMMA. As shown in Figure 1(a-b), a nanostructure with larger diameter HSQ posts on top of smaller diameter PMMA posts was created due to the sensitivity difference between the two resists. The diameter of both posts was determined by the single dot exposure dose and the posts achieved vertical self-alignment. As shown in Figure 1(c), neighboring HSQ posts merged and formed wavy lines on top of PMMA posts when the dots were positioned sufficiently close to each other.

To better control the size and shape of the nanostructures on each resist layer, we developed a double exposure process in which smaller features on the bottom PMMA layer were defined using high dose exposures. Larger features on the top HSQ layer were defined using low dose exposures. Both layers were exposed in a single writing step without removing the wafer. Nanostructures similar to those shown in Figure 1(a-c) can be created in this method with more control by separately exposing the two resist layers. Figure 2(a-b) shows HSQ posts on top of PMMA posts and HSQ lines on top of PMMA posts, respectively. Because features on each resist layer can be more accurately controlled using this approach, complex 3D nanostructures can be fabricated as shown in Figure 2(c).



▲Figure 1: SEM images of 3D nanostructures fabricated from single dot exposure. All scale bars are 200 nm long. (a) HSQ posts on top of PMMA posts. Collapsed nanostructures clearly show the two resist materials. (b) HSQ posts on PMMA posts. Exposure dose in (b) is 5.65 times the exposure dose in (a). (c) HSQ lines on PMMA posts.



▲Figure 2: SEM images of 3D nanostructures fabricated from double exposure process. SEM images (a) and (b) at 45° tilt angle. Exposure dose of negative-tone PMMA was 7 times exposure dose of HSQ. Scale bars are 100 nm (a-b) and 200 nm (c). (a) HSQ posts on top of 30-nm-diameter PMMA posts. (b) 60-nm-wide free-standing HSQ lines on 30-nm-diameter PMMA posts. (c) 75 nm wide HSQ grid on 50-nm-diameter PMMA posts.

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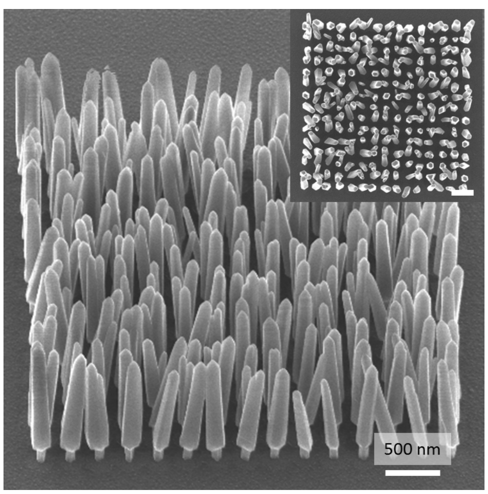
High-Resolution Templated Hydrothermal Growth of ZnO Nanowires

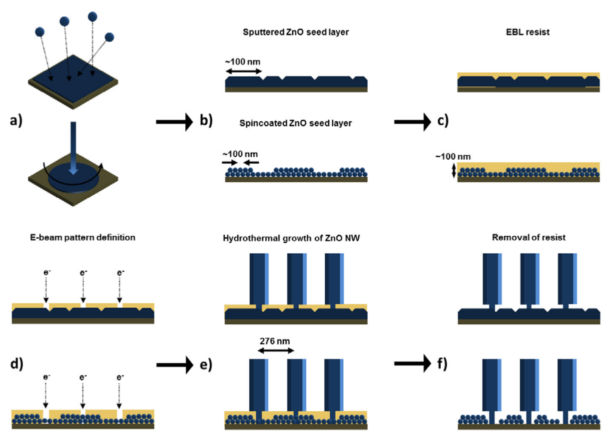
S.M. Nicaise, A. Kiani, J.J. Cheng, S. Gradecak, K.K. Berggren
Sponsorship: MIT Energy Initiative

Zinc oxide nanowires (ZnO NWs) with uniform growth geometries (size, orientation, and pitch) can be grown perpendicular to a ZnO seed-layer thin film via the low-temperature hydrothermal process. In ZnO NW/quantum dot (QD) photovoltaics where NW growth geometry impacts device performance, an ideal NW pitch of 276 nm, similar to the depletion region width, optimizes performance. To control NW pitch as well as analyze other geometric characteristics, we fabricated poly(methyl methacrylate) (PMMA) masks that templated NW growth, Figure 1 shows a key example. While templated ZnO NW growth has been previously reported, this work specifically achieved high-resolution templating on various substrates and analyzed PV-specific geometric characteristics. This work could potentially improve QD infiltration into the NW array and increase exciton extraction efficiency.

Figure 2 shows the major steps of the fabrication process. The ZnO seed layers were spin- and RF-sputtercoated on silicon, indium-tin-oxide-coated glass, and polyethyleneimine substrates. Templating hole arrays were patterned in PMMA via electron-beam lithography. The hole arrays templated the hydrothermal growth of the ZnO NWs so that NWs grew only through the holes. We improved NW alignment and reduced branching by experimentally varying template hole diameter from 30-230 nm. NW alignment (orthogonal to the surface) was measured by the order parameter and found to increase with larger templating hole diameters. In contrast, NWs exhibited less branching for smaller hole diameters. More generally, overall branching was reduced when seed layers were thermally annealed. Atomic force microscopy showed increased grain sizes for annealed seed layers, suggesting an approach to offset branching. This investigation can be applied to improve the photocurrent in ZnO NW/QD PVs, as well as the performances of other ZnO NW-based devices.



▲Figure 1: Scanning helium-ion micrograph (45° and top-down) of templated ZnO NW array. NWs were hydrothermally grown through PMMA hole templates (pitch 276 nm). This example is from unannealed, sputtered ZnO on Si. Branching is negligible; NWs are predominantly perpendicularly aligned.



▲Figure 2: Experimental steps (schematics): a) ZnO seed layer deposited by sputtering (top) or spin-coating (bottom), b) optional annealing at 400°C for 2 hours, c) PMMA resist spin-coated and d) templating holes by EBL, e) NWs hydrothermally grown through template, and f) plasma etching removed PMMA. Grey- substrate, blue -ZnO, green -PMMA.

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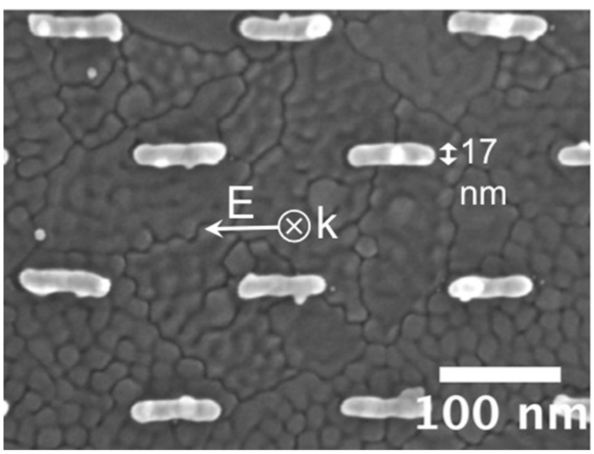
Ultrafast Plasmonic Au Nanorod Array Photocathodes

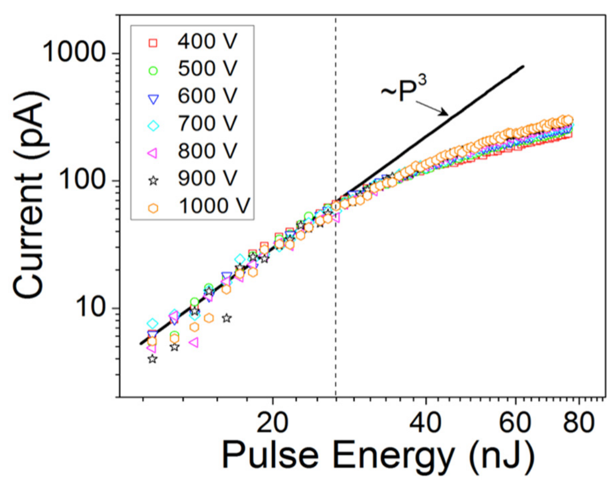
Y. Yang, R. Hobbs, W. Putnam, P. Keathley, E. De Leo, W. Graves, F. Kärtner, K.K. Berggren
Sponsorship: DARPA, Gordon and Betty Moore Foundation

High-density arrays of optically actuated nanoscale electron emitters can facilitate the development of ultrafast and high-brightness photocathodes for the next-generation free-electron lasers (FELs). The emitters can also find applications in time-resolved electron microscopy, crystallography, and spectroscopy Optical near-field enhancement due to localized surface plasmon resonance in metallic nanoparticles generates strong surface fields localized on the nanoscale. These fields are a prerequisite for high-brightness electron sources to minimize the area of electron emission and thus increase the source brightness. Surface-plasmon-enhanced photocathodes with femtosecond pulsed optical switches will enable the development of electron and X-ray analysis of materials with unparalleled spatial and temporal resolution.

In this work, we fabricated arrays of plasmonic Au nanorods with critical dimensions below 20 nm via electron beam lithography and metal lift-off on a sapphire substrate sputter-coated with indium-doped tin oxide (ITO) thin film. We have excited electron emission from Au nanorod arrays using ultrafast pulses of 800-nm light, with pulse durations as short as 7 fs, and repetition rates as high as 84 MHz. We measured the emission current from these photocathodes as a function of incident laser-pulse energy, applied static field, and nanorod array density. Transition from a multiphoton absorption process to strong-field tunneling process in the emission mechanism with increasing laser intensity has been observed, as were space-charge effects with increasing emission current, *e.g.*, linear scaling of emission current with applied static field. The timescale of the emission process was investigated by interferometric autocorrelation, and the emission was shown to be both prompt and on the timescale of the femtosecond optical pulse used to excite emission. Consequently, arrays of optically actuated, surface-plasmon-enhanced Au nanorod electron emitters are promising candidates for applications in high-brightness, ultrafast electron, and X-ray sources.



▲ Figure 1: SEM image of Au nanorod array on 80-nm film of ITO on a sapphire substrate. Orientation of linear polarization (E) of light used to excite electron emission is depicted by arrow, as is direction of light propagation (k) into plane of ITO film.



▲ Figure 2: Emission current vs. pulse energy at various anode bias values for a 1-µm pitch square array of Au nanorods illuminated by a 90-µm (FWHM) beam of 35 fs pulses of 800-nm light (3 kHz rep. rate).

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Determining the Resolution Limits of Electron-Beam Lithography

V.R. Manfrinato, J. Wen, L. Zhang, Y. Yang, R. Hobbs, B. Baker, D. Su, D. Zakharov, N.J. Zaluzec, D.J. Miller, E.A. Stach, K.K. Berggren
Sponsorship: Center for Excitonics (DOE), Brookhaven National Laboratory, Argonne National Laboratory

Electron-beam lithography (EBL) exposure starts with a focused electron beam that deposits energy locally in the resist. This electron beam can also excite secondary electrons (SEs), plasmons, phonons, and photons that may further deposit energy (or break bonds) in the resist. These excited particles deposit energy away from the direct beam and may lead to loss in resolution. Since the invention of EBL 50 years ago, all the mechanisms that lead to the final energy distribution in the resist, that is, the lithographic point-spread function (PSF), are not quantitatively clear. The PSF is the primary metric to understand the resolution limits of the EBL exposure step. The SEs have been considered to be the largest contributors to the lithographic PSF. The role of SEs on EBL has been extensively modeled, but it has not been directly measured to date. Furthermore, the role of plasmons on SE emission has been extensively studied, but the plasmon effect on EBL has not been experimentally investigated. Figure 1a shows the direct-beam PSF (blue), which is the spatial energy density deposited by the direct (or forward-scattered) electron beam in the resist. The direct-beam PSF was measured using chromatic-aberration-corrected energy-filtered transmission electron microscopy. From the direct-beam PSF to the lithographic PSF, we have the total effect of delocalized energy transfer in EBL. Figure 1a shows the measured volume-plasmon (VP) PSF (green), which is the spatial energy density deposition caused by VPs in the resist. We determined the VP PSF by calculating the dielectric constant of the resist at the VP energy (22.5 eV) from electron energy loss spectroscopy. Furthermore, we performed Monte Carlo simulations of the PSF. From Figure 1a we observed that the direct-beam PSF is the largest component for sub-2-nm radius and the VP PSF dominates for radius larger than 2 nm. In Figure 1b we combined the VPs and SEs PSFs by weighting the energy loss of each process. The measured energy loss from VPs was 35% of the total loss. We concluded that VPs were the largest energy loss mechanism in the lithographic PSF, limiting the EBL resolution.

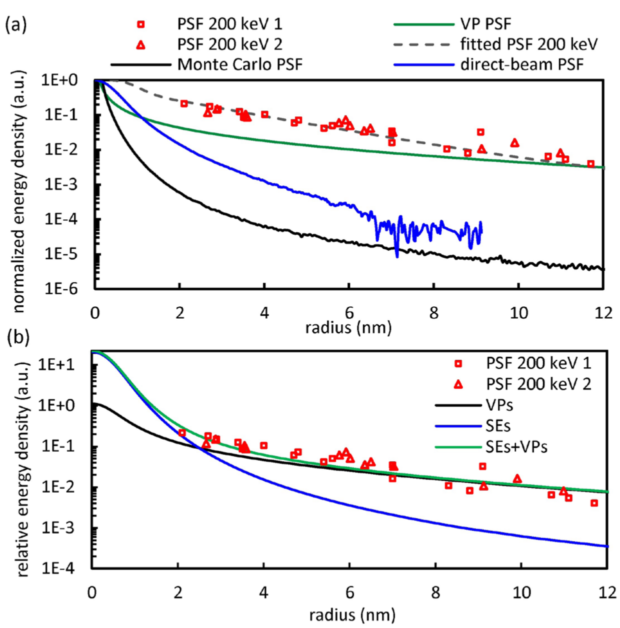

Figure 1: (a) Components of lithographic PSF (maximum value of all PSFs set to unity): (blue) direct-beam PSF, (green) VP PSF, (black) lithographic PSF by Monte-Carlo simulation including SEs, (gray) fitted lithographic PSF, and (red squares - dataset 1 - and red triangles - dataset 2) lithographic PSF from dot-exposure method. (b) (blue) deposited energy density due to SEs, calculated from Monte-Carlo lithographic PSF including SEs and instrument spot size; (black) deposited energy density due to VPs, calculated from VP PSF and direct-beam PSF for energies <50 eV; and (green) total deposited energy density. Lithographic PSF was overlaid with total deposited energy density. The VPs were necessary to match total deposited energy density to lithographic PSF.

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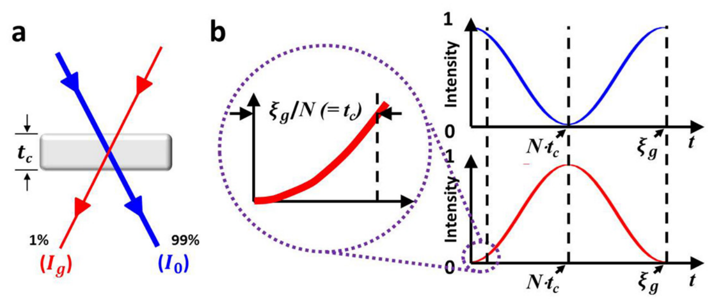
Non-demolition Quantum Electron Microscope in Free-space

C.S. Kim, Y. Yang, V.R. Manfrinato, R.G. Hobbs, K.K. Berggren, P. Kruit
Sponsorship: GBMF

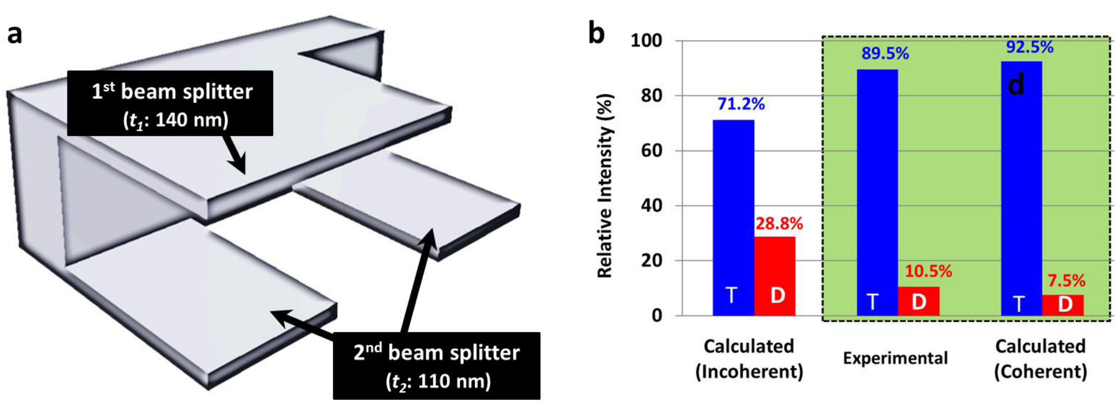
Electron microscopy (EM) has significantly influenced many areas of science and engineering due to its unprecedented atomic resolution. However, the imaging of biological samples has been restricted by sample damage induced by energetic electrons. Despite advances in hydrated environmental chambers, samples still experience physical and chemical damages due to exposure to energetic electrons. In 2009, a quantum electron microscope (QEM) was proposed consisting of two quantum-mechanically coupled electron ring resonators.

We are interested in proof-of-concept of QEM. Thus, we have designed the concept of a free-space QEM based on two electron rings where the electron wavefunction in the two rings is coupled via a diffractive crystal (Figure 1). The diffractive crystal acts to split the incident electron beam into a reference beam and a sample beam, both of which undergo many circulations (100 times) through the coupler to achieve the goal of reduced sample damage as shown in Figure 1.

For diffractive couplers, we used focused Ga and He ion beams to fabricate ~ 10-nm-thick silicon and diamond crystal membranes. We have investigated the impact of the ion beams on the crystal structure of the membranes. Additionally, we have studied decoherence effects induced by the couplers using electron energy loss spectroscopy and simulation. As a first step toward a proof-of-concept non-demolition QEM, we fabricated a linear series of couplers from a single Si crystal and successfully demonstrated (Figure 2) coherent coupling was successfully demonstrated (Figure 2).



◀Figure 1: Non-demolition microscope concept. `(a) Electron rings (red: sample ring, blue: reference ring) overlap in real space and are coupled at a diffractive crystal by Bragg diffraction. (b) Intensity in reference ring ($I_o=cos^2(\pi \times t_c/\xi_g)$) oscillates as a function of crystal thickness; tc is thickness of crystal and xg is extinction distance. Intensity in sample ring decays commensurate with increase in intensity in reference ring ($I_g=sin_2(\pi \times t_c/\xi_g)$). In QEM, each electron undergoes N circulations through coupler as shown.



▲Figure 2: Multiple diffraction-based coupler: (a) Geometry of serial coupler with two thin crystal membranes fabricated from one crystal, thus keeping same crystal orientation in both splitters. Incident electron experiences two successive splitting events by 1st and 2nd beam splitter; (b) Relative intensity in calculation and experiment compared for transmitted vs. diffracted beams.

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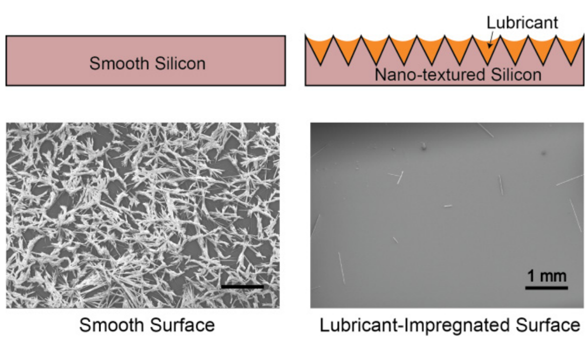
Designing Lubricant-Impregnated Textured Surfaces to Resist Scale Formation

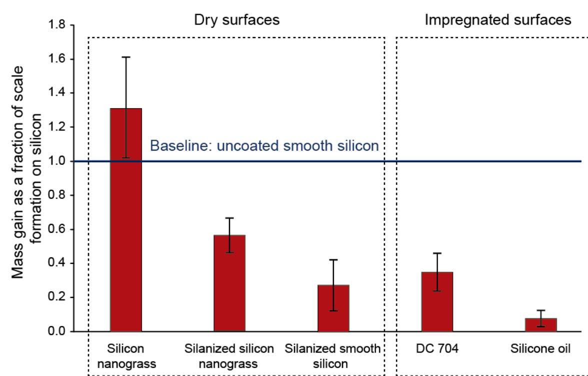
S.B. Subramanyam, G. Azimi, K.K. Varanasi
Sponsorship: MIT Energy Initiative

Scale formation or mineral scale fouling is a widespread problem in industries and households, from the scaling of cooking pots in ancient times to the plugging of pipelines in the modern age. For example, in an oil well in the North Sea, scale formation resulted in a shocking loss of production from 30,000 barrels/day to zero in just 24 hours. It is also estimated that the costs due to fouling of heat exchangers in the United States is about 0.2% - 0.25% of the nation's GNP. Scale deposits reduce process efficiency, increase production costs, lead to under-deposit corrosion, and are centers of radioactivity. The current technologies to address this problem using chemical inhibitors or mechanical/chemical methods of removal are ineffective, energy-intensive, or environmentally unfriendly. Developing surfaces that have a low affinity to scale has been an area of great interest in the last decade.

In this work, we demonstrate the anti-scaling properties of textured surfaces impregnated with a lubricant. The lubricant is stabilized by the capillary forces exerted by the micro/nano features of the solid substrate. From the classical nucleation theory, it is known that reducing the surface energy and the roughness of the substrate reduces the nucleation rate of scale or salt on the surface and hence the overall scale deposition. We optimize the design of the lubricant-impregnated surfaces (LIS) based on the surface tension of the lubricant and its spreading coefficient on the solid. The use of a low-surface-tension spreading liquid as the impregnating lubricant renders the surface extremely smooth and lowers its surface energy. Scale deposition experiments show that the overall scale formation on LIS is reduced owing to their smooth, low-energy surfaces (as in Figure 1). Mass gain measurements indicate that the optimized LIS perform 10 times better than uncoated smooth surfaces (as Figure 2 shows). We extend this idea to an engineering material like stainless steel and show that along with low scale deposition, we also achieve low adhesion of scale to LIS.



▲Figure 1: Comparison of gypsum scale formation on a smooth silicon surface (left) and a lubricant-impregnated surface LIS (right) after ~80 hours of residence time in a saline solution.



▲Figure 2: Mass gain due to calcium sulfate formation after the substrates were immersed in the salt solution for ~80 hours, expressed as a fraction of the mass gain on silicon.

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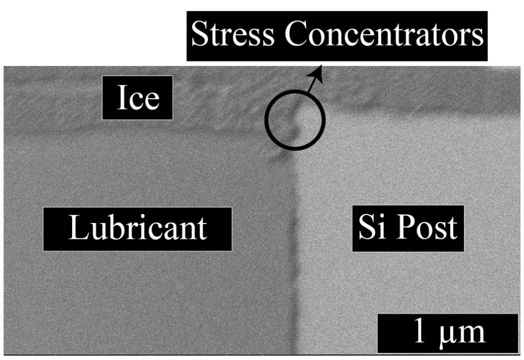
Ice Adhesion on Lubricant-Impregnated Textured Surfaces

S.B. Subramanyam, K. Rykaczewski, K.K. Varanasi
Sponsorship: MIT Energy Initiative, Doherty Chair in Ocean Utilization

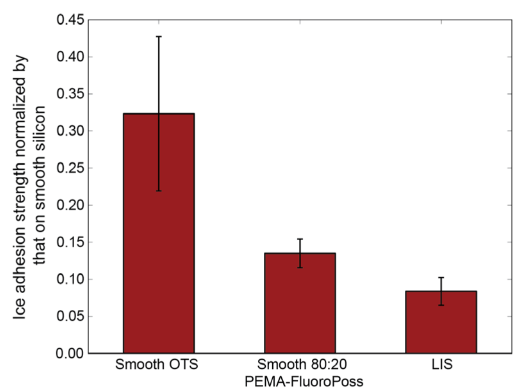
From aircrafts to wind farms, incidents due to excessive ice buildup have threatened human safety and the efficient functioning of energy and transportation systems for many decades. Current efforts of addressing this problem focus on the removal of accumulated ice using a variety of established de-icing methods. However, these approaches are inefficient, expensive and in some cases environmentally unfriendly. Passive approaches such has surfaces that have a strong ice-repellant nature are becoming increasingly important.

One of the ways of quantifying the anti-icing properties of a surface is by measuring the adhesion of ice to the surface. Here, we study the ice-adhesion properties of Lubricant-Impregnated Surfaces (LIS) – micro/nano textured surfaces imbibed with a liquid lubricant. Force measurements show ice adhesion strength on textured surfaces impregnated with thermodynamically stable lubricant films to be higher than that on surfaces with excess lubricant. The excess lubricant, although resulting in a lower ice adhesion, is unstable and can easily be washed away due to external forces like drag, gravity etc. Hence the optimization of LIS is important to attain superior performance compared to the conventional surface treatments.

Systematic ice-adhesion measurements indicate that the ice-adhesion strength is dependent on texture and decreases with increasing texture density. Direct cryogenic SEM imaging of the fractured ice surface and the interface between ice and lubricant-impregnated textured surface (Figure 1) reveal stress concentrators and crack initiation sites that can increase with texture density and result in lowering adhesion strength. Figure 2 shows a comparison of the ice adhesion strength on different surface treatments. The plot compares a smooth silane coating, a fluoroPoss based coating and LIS with the highest texture density. Thus, lubricant-impregnated surfaces have to be optimized to outperform state-of-the-art icephobic treatments.



▲ Figure 1: FIB-cross-section of the interface between ice and LIS under cryogenic conditions. The SEM image indicates the presence of stress concentrator that act as crack nucleation sites.



▲ Figure 2: Comparison of ice adhesion strength on state-of-the-art surfaces – a smooth silane coated surface (OTS), a smooth 80:20 PEMA-FluroPoss coated surface and a Lubricant-Impregnated Surface with the highest texture density.

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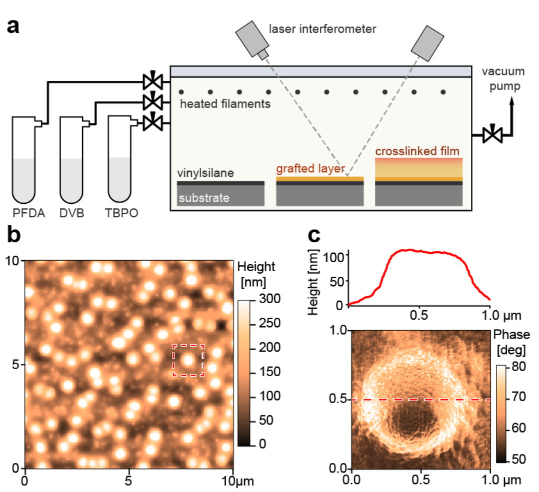
Enhanced Condensation Heat Transfer on Grafted Polymer Films Via iCVD

A.T. Paxson, J.L. Yagüe, K.K. Gleason, K.K. Varanasi
Sponsorship: US Army Research Office, National Science Foundation

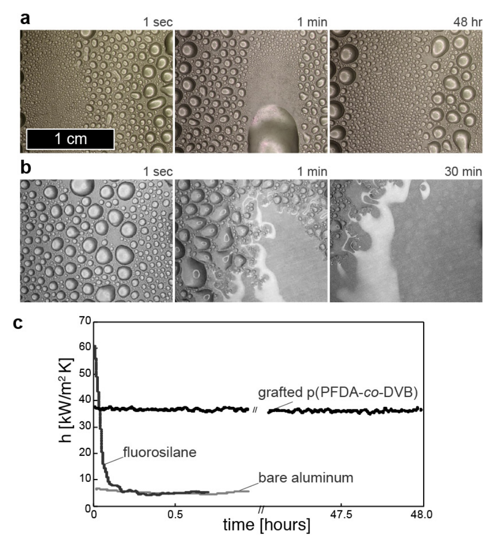
Roughly 85% of the global electricity install base and 50% of desalination plants worldwide rely on steam condensers. Given the massive scale of these processes, any improvements in cycle efficiencies would have a profound effect on global energy consumption. Dropwise condensation has been an active area of research for nearly a century, as the resulting heat transfer coefficients can be an order of magnitude higher than those seen in filmwise condensation. However, the practical implementation of this concept in power generation, desalination, and other applications has been a significant materials challenge, limited by durability of existing hydrophobic functionalization for metal heat transfer surfaces. Metallic heat transfer surfaces must be modified with a hydrophobic coating to obtain dropwise condensation, but because the thermal conductivities of polymeric materials are typically orders of magnitude smaller than that of a metal substrate, it is crucial that a polymer modifier be as thin as possible to minimize thermal resistance. Hence, there is a need for an ultra-thin robust hydrophobic modifier.

We have recently demonstrated the sustained dropwise condensation of steam on a thin film of poly-(1H,1H,2H,2H-perfluorodecyl acrylate)-*co*-divinyl benzene p(PFDA-*co*-DVB) covalently grafted to a metal substrate by initiated chemical vapor deposition (iCVD). The iCVD process is a single-step, solvent-free, low-energy, vapor-phase method used to deposit conformal films with precisely controllable thickness. Briefly, monomer and initiator species (Figure 1a) are flowed into a reactor at controlled rates and encounter heated filaments and a cooled substrate. The locally heated zone around the filaments thermally cleaves the initiator species (tert-butyl peroxide, TBPO). The radical fragments produced initiate vinyl polymerization of the monomers absorbed on the surface to form semicrystalline agglomerations (Figure 1b, c).

Accelerated endurance tests were conducted by condensing steam at 100˚C. Coatings of p(PFDA-*co*-DVB) were compared to fluorosilane coatings, both on aluminum substrates (Figure 2a, b). The grafted polymer coating exhibits dropwise condensation with a departing droplet size of 4.2 ± 0.1 mm and a heat transfer coefficient greater than 35 kW m^{-2} K^{-1}, which is more than 7 times greater than the steady-state filmwise heat transfer coefficient of the degraded silanized surface, with no noticeable degradation after 48 hours of condensation (Figure 2c).



▲Figure 1: iCVD chamber geometry and deposition process (a). AFM images of rough copolymer surface consisting of hemispherical agglomerations (b); detail of semicrystalline agglomeration (c).



▲Figure 2: Sustained dropwise condensation on iCVD copolymer (a) vs. rapid degradation of fluorosilane coating (b). Plot of heat transfer coefficient vs time (c).

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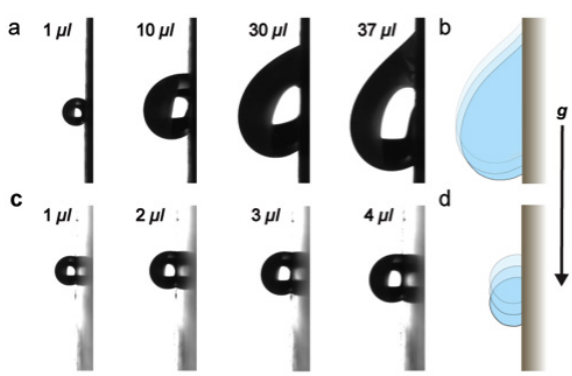
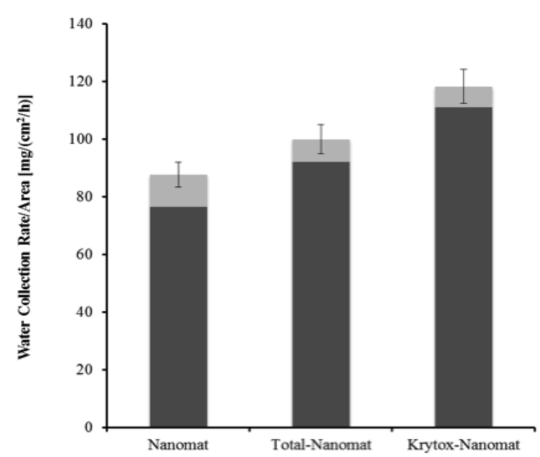
Fog-Harvesting Potential of Lubricant-Impregnated Electrospun Nanomats

B.S. Lalia, S. Anand, R. Hashaikeh, K.K. Varanasi
Sponsorship: MIT, Masdar Institute of Science and Technology

Hydrophobic PVDF-HFP nano-webs were fabricated by a facile electrospinning method and proposed for harvesting fog from the atmosphere. PVDF-HFP polymer was used to prepare electrospun nanomats due to its inherent hydrophobicity. As prepared electrospun nanomats show strong adhesive forces with water. The impregnation of lubricant in nano/micro-pores of nanomats dramatically lowers the retentive force between water droplets and nanomat surface indicated by the low contact angle hysteresis and promotes roll-off of small sized droplets. Impregnation of nanomats with lubricants (Total Quartz Oil and Krytox 1506) decreased the contact angle hysteresis and hence improved roll off of water droplets on the nanomats surface. It was found that water droplets of 5 µl size (dia.=2.1 *mm*) and larger roll down on an oil impregnated surface, held vertically, compared to 38 µl (dia.=4.2 mm) on plain nano-web. Contact angle hysteresis reduced from ~95° to ~23° with the Krytox 1506 impregnation (Figure 1). The prepared nanomats exhibit great potential to prepare stable lubricant impregnated surfaces due to their high porosity by virtue of which they wick large lubricant proportionate to their weight. The fog collection studies show that collection rates on the low hysteresis impregnated sample is higher than the water collection rates on the high hysteresis un-impregnated sample (Figure 2). Further we show that nanomats impregnated with the lubricant show significantly less drainage of oil from the surface along with shedding water.



▲Figure 1: Optical images of different size water drops on the vertical surface of nanomat (a) and nanomat impregnated with Total Quartz Oil (c). Schematic of water drop sliding on the nanomat (b) and on the nanomat impregnated with Total Quartz Oil (d).



▲Figure 2: Fog collection behavior with time for nanomats with and without lubricant impregnation

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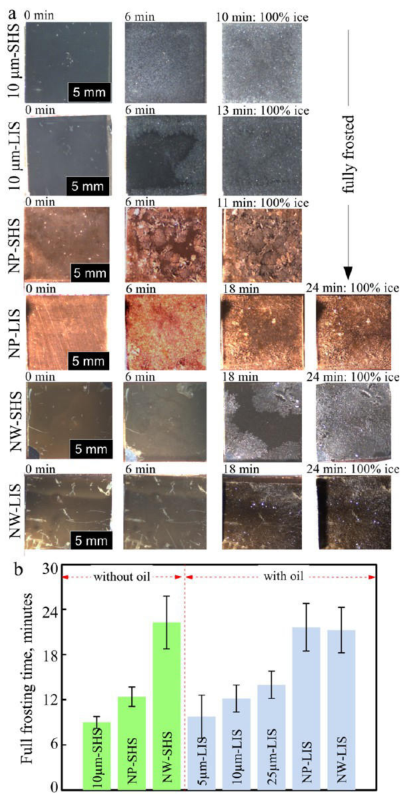
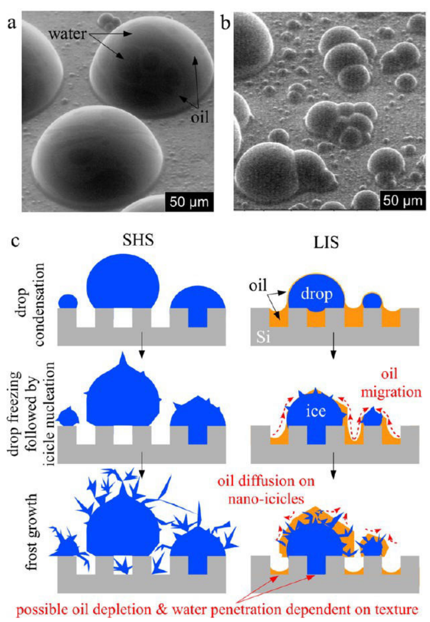
Mechanism of Frost Formation on Lubricant-Impregnated Surfaces

K. Rykaczewski, S. Anand, S.B. Subramanyam, K.K. Varanasi
Sponsorship: National Science Foundation Career Award, MIT Energy Initiative

Frost formation is a major problem affecting a variety of industries including transportation, power generation, construction, and agriculture. Currently used active chemical, thermal, and mechanical techniques of ice removal are time-consuming and costly. The use of nanotextured coatings infused with perfluorinated oil has recently been proposed as a simple passive anti-frosting and anti-icing method. However, we demonstrate that the process of freezing subcooled condensate and frost formation on such lubricant-impregnated surfaces is accompanied by the migration of the lubricant from the wetting ridge and from within the textured substrate to the surface of frozen droplets. For practical applications, this mechanism can comprise the self-healing and frost-repelling characteristics of lubricant impregnated-surfaces, regardless of the underlying substrate' s topography. Thus, further research is necessary to develop liquid-texture pairs that will provide a sustainable frost suppression method.



◀ Figure 1: (a) Example optical images of SHS and LIS samples from the beginning of cooling until full frost coverage. (b) Histogram of average times required for full sample frosting.



▶ Figure 2: ESEM images of (a) oil swirls on top of drops and (b) compound drops condensed on NP-LIS and schematic illustrations contrasting with (c) the mechanism of frost growth via drop condensation and freezing on SHS and LIS. (The extent of illustrated oil depletion and water penetration into the substrate is dependent on the length scale of the underlying texture.)

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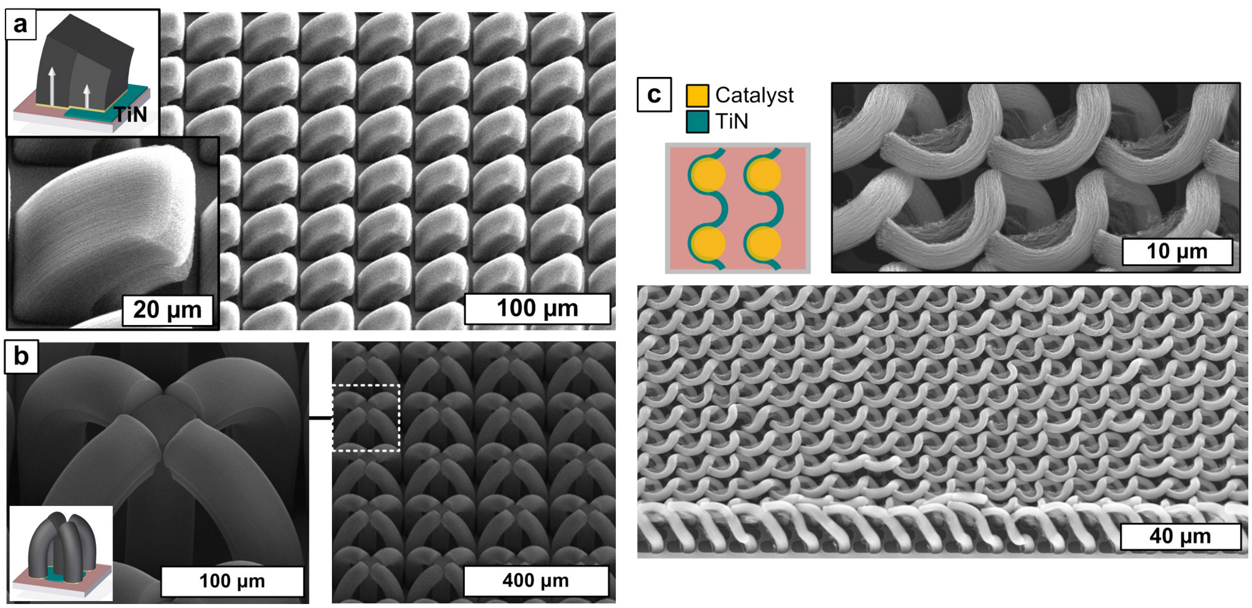
Manufacturing of Freeform Carbon Nanotube Microstructures

M. De Volder, S.J. Park, S. Tawfick, A.J. Hart
Sponsorship: DARPA, Air Force Office of Scientific Research, Office of Naval Research

The skins of many plants and animals have intricate micro-scale surface features that give rise to properties such as directed water repellency and adhesion, resistance to fouling, and camouflage. However, engineered mimicry of these designs has been restrained by the limited capabilities of top-down fabrication processes.

We demonstrate a new technique for scalable manufacturing of freeform microstructures, via strain-engineered growth of aligned carbon nanotubes (CNTs). Offset patterning of the CNT growth catalyst is used to locally modulate the CNT growth rate. This causes the CNTs to collectively bend during growth, with exceptional uniformity over large areas. The final shape of the curved CNT microstructures can be designed via finite element modeling, and compound catalyst shapes produce microstructures with multi-directional curvature and unusual self-organized patterns. Because our process is based on an additive chemical synthesis process instead of a subtractive etching and release technique, it enables the direct synthesis of complex microstructures that are perpendicular rather than parallel to the substrate. This has two major implications: it enables fabrication of closely packed arrays of structures with heterogeneous shapes, and the porosity of the CNT forests enables conformal coating after growth to modify chemical and/or mechanical properties. We demonstrate this latter point by conformal coating of CNT "microtruss" arrays by atomic layer deposition (ALD) and polymer CVD, which increases their mechanical stiffness without changing the geometry. This process establishes versatile principles for design and manufacturing of complex microstructured surfaces that profit from the mechanical, electrical, and thermal properties of CNTs, and can leverage emerging methods for roll-to-roll micro-patterning and chemical vapor deposition.



▲ Figure 1: Strain-engineered growth of 3D CNT microstructures by offset patterning of the growth catalyst on a TiN underlayer: (a) curved micropillars; (b) microtrusses; (c) self-organized woven texture.

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Direct Fabrication of Graphene on Dielectric Substrates

D. McNerny, B, Viswanath, D. Copic, F. Laye, C. Prohoda, A. Brieland-Shoultz, E.S. Polsen, N.T. Dee, V.S. Veerasamy, A.J. Hart
Sponsorship: Guardian Industries, National Science Foundation, Air Force Office of Scientific Research

Recent advances in the growth of graphene by chemical vapor deposition (CVD) have enabled the controlled synthesis of graphene films of uniform thickness and high quality, despite their polycrystalline structure and orientation. To realize many of the potential applications of graphene, there remains a need for scalable methods of transferring graphene from the metal film or foil growth substrate, which is often Cu or Ni, to application-specific substrates. Moreover, graphene transfer methods typically require multiple steps, and can damage the graphene and/or degrade its properties such as electron mobility.

We demonstrate direct production of graphene on SiO_2 by CVD growth of graphene at the interface between a Ni film and the SiO_2 substrate, followed by dry mechanical delamination of the Ni using adhesive tape. This result is enabled by understanding of the competition between stress evolution and microstructure development upon annealing of the Ni prior to the graphene growth step. When the Ni film remains adherent after graphene growth, the balance between residual stress and adhesion governs the ability to mechanically remove the Ni after the CVD process. In this study the graphene on SiO2 comprises micron-scale domains, ranging from monolayer to multilayer. The graphene has >90% coverage across centimeter-scale dimensions, limited by the size of our CVD chamber. Further engineering of the Ni film microstructure and stress state could enable production of highly uniform interfacial graphene followed by clean mechanical delamination. With such understanding, this method could be scaled to manufacturing on wafer-scale and larger dimensions, either using blanket Ni films, or pre-patterned Ni shapes to directly template device geometries. Moreover, our findings suggest that preferential adhesion can enable production of 2-D materials directly on application-relevant substrates.

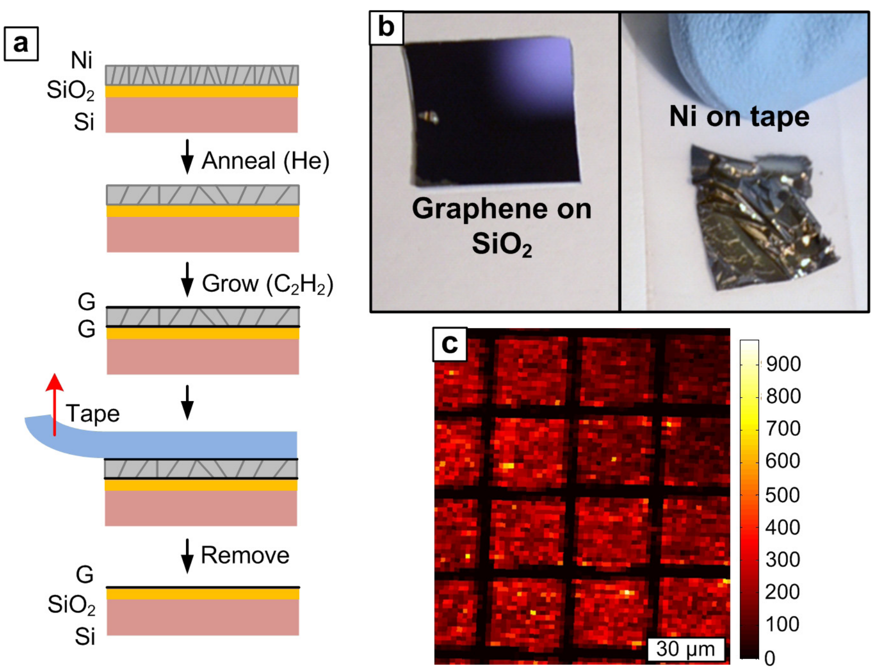

Figure 1: Direct fabrication of graphene on SiO_2 by interfacial growth followed by delamination of the Ni film a) Process schematic, indicating Ni grain growth during annealing in He, followed by graphene growth under CVD conditions, and then removal of Ni using adhesive tape. (b) Photo of substrates (~1×1 cm) and delaminated Ni films in case of ex situ tape delamination after graphene growth. (c) Two-dimensional Raman (G peak) intensity map of substrate with patterned graphene after Ni delamination.

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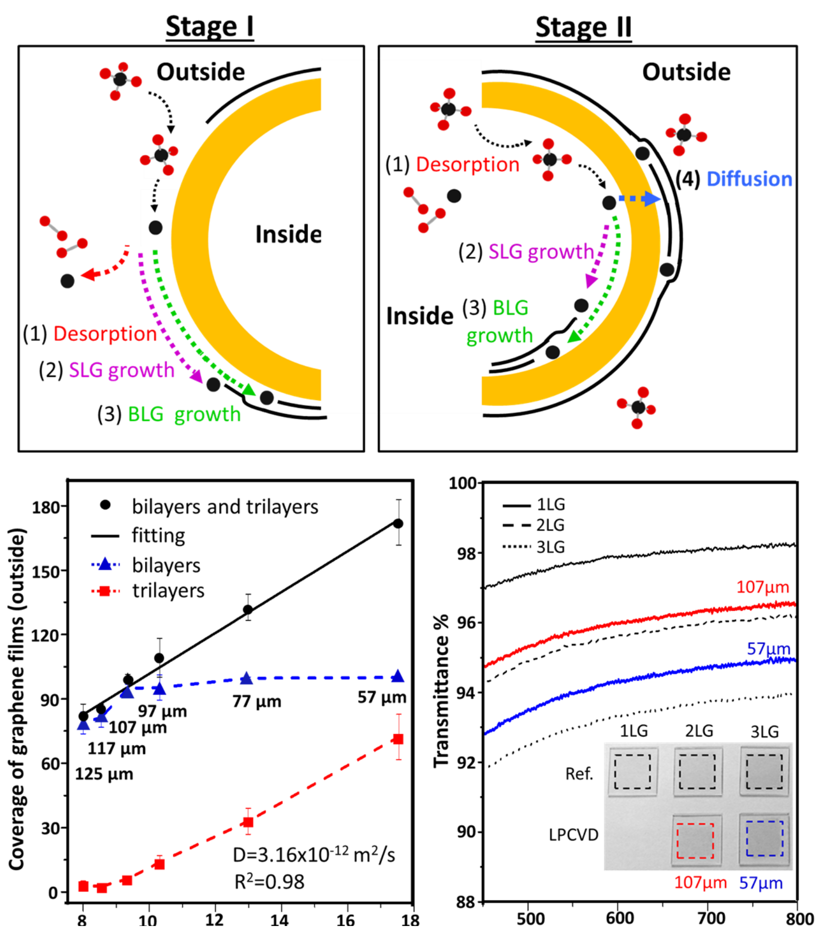
Asymmetric Growth of Bilayer Graphene on Copper Enclosures Using Low-pressure Chemical Vapor Deposition

W. Fang, A.L. Hsu, Y. Song, A.G. Birdwell (US Army Research Laboratory), M. Dubey (US Army Research Laboratory), T. Palacios, M.S. Dresselhaus, J. Kong

In this work, we investigated the growth mechanisms of bilayer graphene on the outside surface of Cu enclosures at low pressures. We observed that the asymmetric growth environment of a Cu enclosure can yield a much higher (up to 100%) bilayer coverage on the outside surface than the bilayer growth on a flat Cu foil, where both sides are exposed to the same growth environment.

By inspecting the evolution of the two surfaces of the Cu enclosure during the low-pressure chemical vapor deposition synthesis, we have gained a better understanding of the bilayer growth mechanism on the outside surface of the enclosure. We conclude that the two surfaces are coupled by carbon diffusion through the Cu foil. By identifying the pathways for methane gases and active carbon, we found that carbon diffusing through the Cu foil allows for a continual growth of bilayers from underneath the outside monolayer graphene. Based on the monolayer graphene growth on the inside surface and the inter-copper carbon diffusion process, we derived a growth model for the bilayer graphene on the outside that agrees well with the experimental findings. Finally, we verified our model by measuring the thickness dependence of the Cu foil on the delivery rate of carbon. Moreover, utilizing inter-catalyst diffusion pathways may serve as a more general method for synthesis of other layer-by-layer hybrid structures, such as graphene on h-BN or isotopic bilayer systems. The improved understanding of the synthesis of bilayer graphene on Cu catalysts will lead to the better control of bilayer graphene growth for future bilayer graphene-based devices and potentially other bilayer nano-materials.



◀ Figure 1: Growth mechanism of bilayer graphene. (a) Growth mechanism for bilayer graphene on outside surface in stage I, when monolayer graphene is incomplete. (b) Growth mechanism for bilayer graphene in stage II, after completion of monolayer graphene at outside surface. (c) Coverage of bilayers (dotted blue), trilayers (dotted red) and summation of both bilayers and trilayers (dotted black) as a function of thickness of Cu foil. Solid black line shows linear fitting of carbon content. (d) Transmittance of layer-by-layer transferred graphene films (black) and directly grown graphene films on Cu enclosures with thickness of 107 µm (red) and 57 µm (blue), respectively. Inset shows photograph of corresponding graphene films on borosilicate. Layer-by-layer transferred graphene was used as reference.

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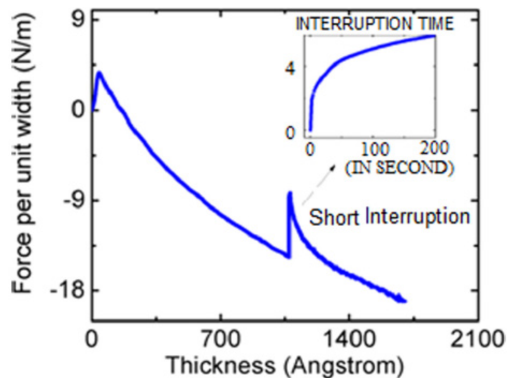
Correlation of Shape Changes of Grain Surfaces and Reversible Compressive Stress Evolution in Polycrystalline Films

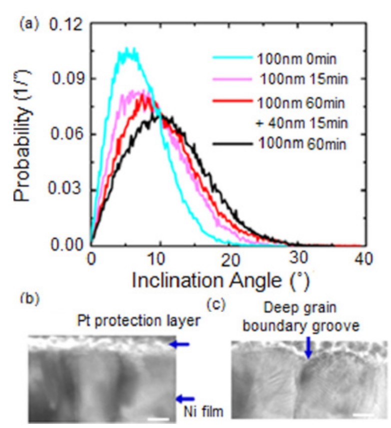
H.Z. Yu, C.V. Thompson
Sponsorship: National Science Foundation

Polycrystalline thin films typically grow by the Volmer-Weber mechanism, in which the atoms condense on the substrate and diffuse to form nuclei, and the nuclei then grow into 3D islands. Further deposition leads to impingement and coalescence of the 3D islands and formation of grain boundaries, resulting in a tensile stress in the film. Under conditions of high atomic mobility, the post-coalescence stress evolves to a compressive state during film thickening, but the stress evolves toward the tensile direction when growth is interrupted. Remarkably, for short interruptions, when growth is resumed, the stress evolves back to the pre-interruption level. One example of such behavior is shown for Ni films deposited at 473K in Figure 1. Understanding the mechanisms for this complex stress evolution has been the focus of much recent research. Most recently, the stress evolution during a growth interruption has been shown to involve multiple kinetic processes, which can be interpreted as a fast reversible process and a slow irreversible process. The slow process was shown to correspond to a process occurring in the bulk of the film and can be attributed mostly to grain growth after deposition. The underlying mechanism for the fast process is still not clear.

Here we report correlated characterization of stress evolution with evolution of the surface structure of polycrystalline nickel films based on atomic force microscopy (AFM) measurements. Figure 2(a) shows the distribution of inclination angles on Ni film surfaces after 0-, 15-, and 60-min growth interruptions. As the interruption time is increased, the distribution curve moves toward the higher inclination angles, i.e., the surface becomes rougher, with regions of higher surface steepness. Also shown in Figure 2(a) is the distribution of inclination angles after a 60-min interruption, followed by a continued growth of 40 nm and a 15-min interruption (in red). Clearly, the subsequent 40-nm deposition and 15-min interruption led to a leftward shift of the curve back to low inclination angles. Overall, the rightward shift of the curve to high inclination angles going from a 15-min to a 60-min interruption and the leftward shift of the curve back to low inclination angles after the subsequent 40-nm deposition and 15-min interruption demonstrate that the change of the surface structure, as characterized using ex situ AFM, is reversible. Representative cross-sectional transmission electron microscopy (TEM) images are shown in Figures 2 (b) and (c) for Ni films after 0-min and 60-min growth interruptions. Deep grooves were observed at the grain boundaries in the latter film but not in the former film, in which the grooves were generally shallow and flat. The AFM and TEM results suggest that the fast reversible stress evolution is associated with reversible changes in the shapes of the surfaces of individual grains (i.e., grooving and flatting) that occur during growth interruptions and upon growth resumption.



▲ Figure 1: Stress evolution during deposition of a polycrystalline Ni film, including a reversible stress change during an interruption of growth.



▲ Figure 2: (a) Inclination angle distribution on the surface of Ni films at different times after growth was interrupted. Cross-sectional TEM images after (b) 0-min and (c) 60-min interruptions.

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Quantitative Analysis and Modeling of Templated Solid-state Dewetting of Thin Single-crystal Ni Films

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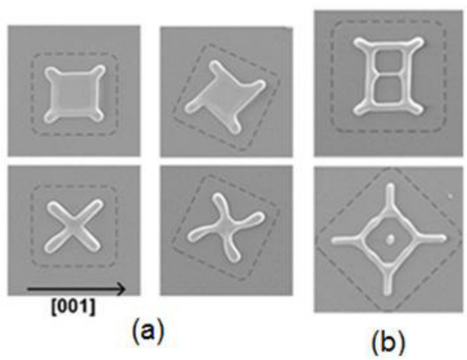
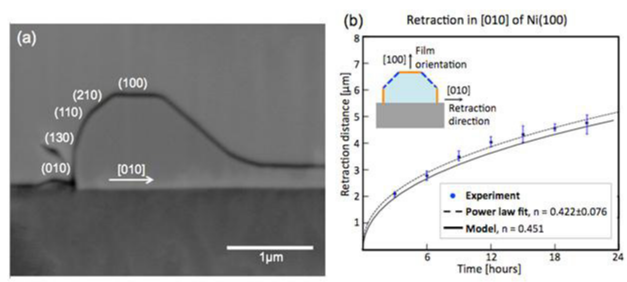
Sponsorship: SMART, National Science Foundation

Thin films are generally metastable in the as-deposited state and will dewet (agglomerate) when heated. Nanometer scale films (<100 nm thick) can dewet at temperatures well below the melting temperature of the film, and dewetting occurs while the film remains solid. This phenomenon can limit the use of very thin films in microsystems, but it can also be used to controllably produce complex structures. Dewetting occurs through retraction of the edges of naturally forming holes or at patterned edges of films. In single-crystal films, anisotropy in surface energy and diffusivity drives the dewetting process to result in regular patterns that relate to the crystal symmetry. We are investigating use of anisotropic dewetting as a self-assembly method to generate complex, small, predetermined patterns. A quantitative understanding of dewetting mechanisms is critical for design of self-assembled structures made through dewetting. We measured the rates of anisotropic edge retraction by solid-state dewetting in kinetically stable edge orientations. These measurements can also be used to estimate the edge retraction rates in a general crystallographic orientation. Additionally, we developed an analytical model for solid-state dewetting via surface diffusion for fully faceted materials to test our understanding of dewetting mechanisms (see Figure 1). This two-dimensional model provides excellent agreement with experimental edge retraction rates for kinetically stable edges. We also developed a three-dimensional phase-field model for dewetting of materials with isotropic surface energies. A three-dimensional model for dewetting of materials with anisotropic surface energies is under development.



▲Figure 1: (a) Partially dewetted patches patterned from a (100) film into squares with different in-plane orientations; top is an earlier time than bottom. (b) Dewetting patterns of larger squares.



▲Figure 2: (a) Cross-sectional SEM image of a [010] edge in a (100) film. (b) Corresponding experimental and theoretical retraction distance vs. time.

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Understanding Electronic, Optical and Thermal Properties of Transition Metal Chalcogenides

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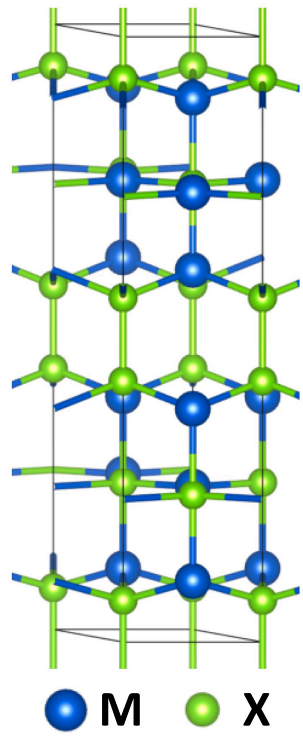
The fundamental properties of a material depend on its atomic structure, nature of bonding, and elemental/chemical composition. Confinement of electrons in 2-dimensional planar structures leads to the realization of several intriguing properties that are not seen in the bulk 3-dimensional counterparts. In this work, we explore the properties of single- and few- layer MX (M: transition metal, X: chalcogen atom) both theoretically and experimentally. Using state-of-the-art density functional theory (DFT), we carried out a stability analysis through phonon, electronic, magnetic, and elastic structure calculations where M=Cu, Ag, and Au and X=S, Se, and Te. The stacking of transition metal chalcogenide (TMC) monolayers is of the type MX-M_2X_2 instead of the usual X-M-X stacking found in TMCs. The differences in geometric structure result in many different stable monolayer forms with different electronic and magnetic properties. Depending on the number of layers, MX structures can be found in 2-, 3-, 4- and 6-MX layer stable configurations. Experiments confirm these dimensionality effects predicted by DFT, such as energy band structures and Raman active modes,. Various different monolayers of MX possess a number of properties that make them highly promising materials for future nanoscale applications.



◄ Figure 1: Bulk geometric structure of MX compounds. M: Transition metal; X: Chalcogen atom.

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

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SELECTED PUBLICATIONS

A. Dighe, U. P. Froriep, M. Sunshine, A. Ievins, P. Anikeeva, C. Moritz, and J. Voldman, "Development and in vivo testing of reconfigurable neural probes for chronic electrical recording," in *Hilton Head Workshop 2014: A Solid-State Sensors, Actuators and Microsystems Workshop*, 2014.

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T. Humplik, R. Raj, S.C. Maroo, T. Laoui, E.N. Wang, "Effect of Hydrophilic Defects on Water Transport in MFI Zeolites," *Langmuir,* 30(22), p. 6446-6453, 2014.

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SELECTED PUBLICATIONS

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Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. 6 faculty members participate in the CICS: Hae-Seung Lee (director), Duane Boning, Anantha Chandrakasan, David Perreault, and Charles Sodini. In September 2013, we welcomed our newest CICS faculty member, Vivienne Sze. Prof. Sze's research focuses on joint design of algorithms, architectures and circuits to build energy efficient and high performance systems. Her work on implementation-friendly video compression algorithms was used in the development of the latest video coding standard HEVC/H.265, enabling it to deliver better compression than previous standards, while still achieving high processing speeds and low hardware cost. She aims to develop energy-aware algorithms and efficient architectures for various energy-constrained applications including portable multimedia, health monitoring and distributed sensing.

CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, biomedical circuits, and power conversion circuits, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. CICS is designed to be the conduit for such synergy. At present, participating companies include Analog Devices, IBM, Linear Technology, Maxim Integrated, Marvell Technology Group, MediaTek, and Texas Instruments.

CICS's research portfolio includes all research projects that the 6 participating faculty members conduct, regardless of source(s) of funding, with a few exceptions. Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication among MIT faculty, students, and industry. We hold two informal technical meetings per year open to CICS faculty, students, and representatives from participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet. The participants then offer valuable technical feedback, as well as suggestions for future research.

More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT or enter into a separate research contract for more focused research for their particular interest. The result is truly synergistic, and it will have a lasting impact on the field of integrated circuits and systems.

Energy Frontier Research Center for Excitonics

Professor Marc A. Baldo, Director

The Energy Frontier Research Center (EFRC) for Excitonics is a collaboration between Massachusetts Institute of Technology, Harvard and Brookhaven National Laboratory. Our objective is to supersede traditional electronics with devices that use excitons to mediate the flow of energy. Excitons are quasiparticle excitations consisting of a bound electron and hole that mediate the absorption and emission of light, especially in disordered and low-dimensional materials.

The motivation for excitonics is that conventional electronic devices can be difficult to manufacture; their constituent materials require very high levels of order, and achieving such low entropy in a semiconductor requires expensive and energy intensive fabrication. For example, the energy payback time for a crystalline silicon solar cell is on the order of 2 years, and at current manufacturing growth rates, it is expected to take at least 20 years to produce enough silicon-based solar cells to make a significant impact on the world energy supply. Similarly, epitaxial growth constraints are likely to limit solid state lighting sources to a small fraction of the overall demand for lighting.

There is an alternate approach that is more suitable for large scale production. In the Center for Excitonics, we address materials with only short-range order. Such nanostructured materials are compositions of nano-engineered elements such as organic molecules, polymers, or quantum dots and wires, in films bound together by weak van der Waals bonds. These materials are characterized by excitons that are localized within the ordered nanostructures. Excitons provide a unique means to transport energy and convert between photons and electrons. Due to localization of excitons, the optical properties of the films are relatively immune to longer-range structural defects and disorder in the bulk. And in contrast with the painstaking growth requirements of conventional semiconductors, weak van der Waals bonds allow excitonic materials to be readily deposited on a variety of materials at room temperature.

We address two grand challenges in excitonics: (1) to understand, control and exploit exciton transport, and (2) to understand and exploit the energy conversion processes between excitons and electrons, and excitons and photons.

(1) Exciton Transport: We are developing new theory to explain and model the movement of excitons in complex nanostructures. We build artificial excitonic antennas that absorb and guide light in nanofabricated circuits of molecular chromophores, J-aggregates, quantum dots and nanowires. We characterize coherence and energy transfer in our antennas using scanning probe microscopy and our recently developed technique of fully phase coherent 2-d Fourier transform spectroscopy. Finally, our excitonic technologies will be applied to low cost solar cells and luminescent solar concentrators, which promise power efficiencies > 30%.

(2) Exciton Dynamics: We are developing new theory for the dynamics of exciton formation and separation. Applications include increasing the efficiency of organic light emitting devices by up to a factor of four and characterizing the fundamental efficiency limits of excitonic solar cells.

We possess two important tools that are unique to the center: Cathodo-luminescence Scanning Transmission Electron Microscopy (CL-STEM), which is used to characterize the structure-function relationships of excitonic nanomaterials, and Superconducting Nanowire Single-Photon Detectors (SNSPDs). SNSPDs can conclusively determine the efficiency of multiple carrier generation, a process with enormous potential for solar cells. Finally, we aim to characterize the link between exciton annihilation and device degradation.

MIT/MTL Center for Graphene Devices and 2D Systems

Professor Tomás Palacios, Director

The MIT/MTL Center for Graphene Devices and 2D Systems (MIT-CG) brings together, MIT researchers and industrial partners to advance the science and engineering of graphene and other two-dimensional materials.

Graphene and other two-dimensional (2D) materials are revolutionizing electronics, mechanical and chemical engineering, physics and many other disciplines. The MIT-MTL Center for Graphene Devices and 2D Systems aims to coordinate most of the work going on at MIT on these new materials, and brings together MIT faculty and students, with leading companies and government agencies interested in taking these materials from a science wonder to an engineering reality.

Specifically, the Center explores advanced technologies and strategies that enable 2D materials, devices and systems to provide discriminating or break-through capabilities for a variety of system applications ranging from energy generation/storage and smart fabrics and materials, to optoelectronics, RF communications and sensing. In all these applications, the MIT-CG supports the development of the science, technology, tools and analysis for the creation of a vision for the future of new systems enabled by 2D materials.

Some of the multiple benefits of the Center's membership include complimentary attendance to meetings, Industry Focus days, and webcasting of seminars related to the main research directions of the Center. The members of the Center also gain access to a resume book that connects students with potential employers, as well as to timely white papers on key issues regarding the challenges and opportunities of these new technologies. There are also numerous opportunities to collaborate with leading researchers on projects that address some of today's challenges for these materials, devices and systems.

MIT/MTL Gallium Nitride (GaN) Energy Initiative

Professor Tomás Palacios, Director

The MIT/MTL Gallium Nitride (GaN) Energy Initiative (MIT-GaN) is an inter-departmental program that brings together 10 MIT faculty and more than 40 other researchers and industrial partners to advance the science and engineering of GaN-based materials and devices for energy applications.

The GaN Energy Initiative provides a holistic approach to GaN research for energy applications and it coordinates work on the growth, technology, novel devices, circuits and systems to take full advantage of the unique properties of GaN. The GaN Energy Initiative is especially interested in developing new beyond-state-of-the-art solutions to system-level applications in RF power amplification, mixed signal electronics, energy processing and power management, as well as advanced optoelectronics. Most of the work is done on GaN materials and devices which are compatible with Si fabrication technologies, in close collaboration with industrial partners to accelerate the insertion of these devices into systems.

The MIT/MTL Gallium Nitride(GaN)Energy Initiative organizes numerous activities to advanced GaN. Some of these activities include webcast of seminars and annual meetings, as well as joint collaborations with industry partners. The Initiative also elaborates a resume book of graduating students and provides timely access to white papers and preprints through its website.

The MIT Medical Electronic Device Realization Center

Professor Charles Sodini, Director

The vision of the MIT Medical Electronic Device Realization Center (MEDRC) is to revolutionize medical diagnostics and treatments by bringing health care directly to the individual and to create enabling technology for the future information-driven healthcare system. This vision will in turn transform the medical electronic device industry. Specific areas that show promise are wearable or minimally invasive monitoring devices, medical imaging, portable laboratory instrumentation, and the data communication from these devices and instruments to healthcare providers and caregivers.

Rapid innovation in miniaturization, mobility, and connectivity will revolutionize medical diagnostics and treatments, bringing health care directly to the individual. Continuous monitoring of physiological markers will place capability for the early detection and prevention of disease in the hands of the consumer, shifting to a paradigm of maintaining wellness rather than treating sickness. Just as the personal computer revolution has brought computation to the individual, this revolution in personal medicine will bring the hospital lab and the physician to the home, to emerging countries, and to emergency situations. From at-home cholesterol monitors that can adjust treatment plans, to cell phone-enabled blood labs, these system solutions containing state-of-the-art sensors, electronics, and computation will radically change our approach to health care. This new generation of medical systems holds the promise of delivering better quality health care while reducing medical costs.

The revolution in personal medicine is rooted in fundamental research in microelectronics from materials to sensors, to circuit and system design. This knowledge has already fueled the semiconductor industry to transform society over the last four decades. It provided the key technologies to continuously increase performance while constantly lowering cost for computation, communication and consumer electronics. The processing power of current smart phones, for example, allows for sophisticated signal processing to extract information from this sensor data. Data analytics can combine this information with other patient data and medical records to produce actionable information customized to the patient's needs. The aging population, soaring healthcare costs, and the need for improved healthcare in developing nations are the driving force for the next semiconductor industry's societal transformation, *Medical Electronic Devices*.

The successful realization of such a vision also demands innovations in the usability and productivity of medical devices, and new technologies and approaches to manufacture devices. Information technology is a critical component of the intelligence that will enhance the usability of devices; real-time image and signal processing combined with intelligent computer systems will enhance the practitioners' diagnostic intuition. Our research is at the intersection of Design, Healthcare, and Information Technology innovation. We perform fundamental and applied research in the design, manufacture, and use of medical electronic devices and create enabling technology for the future information-driven healthcare system.

The MEDRC has established a partnership between microelectronics companies, medical device companies, medical professionals, and MIT to collaboratively achieve needed radical changes in medical device architectures, enabling continuous monitoring of physiological parameters such as cardiac vital signs, intracranial pressure and cerebral blood flow velocity. MEDRC research projects are defined jointly by faculty and researchers, physicians and clinicians, along with our industrial partners. A visiting scientist from a project's sponsoring company is present at MIT. Ultimately this individual is the champion that helps translate the technology back to the company for commercialization and provide the industrial viewpoint in the realization of the technology. MEDRC projects have the advantage of insight from the technology arena, the medical arena, and the business arena, thus significantly increasing the chances that the devices will fulfill a real and broad healthcare need as well as be profitable for companies supplying the solutions. With a new trend toward increased healthcare quality, disease prevention, and cost-effectiveness, such a comprehensive perspective is crucial.

Now a part of MIT's Institute for Medical Engineering and Science, MEDRC is a focal point for engagement with researchers across MIT, the medical device and microelectronics industry, venture-funded startups, and the Boston medical community. The Center fosters the creation of prototype devices and intellectual property and aims to serve as the catalyst for the deployment of medical devices that will reduce the cost of healthcare in both the developed and developing world.

Theses Awarded

S.B.

- **Mariah Hake** (K.K. VARANASI)
Experimental Design to Determine the Effect of Temperature and Mach Number on Entropy Noise
- **Colleen Loynachan** (P.O. ANIKEEVA)
Targeted Magnetic Nanoparticles for Remote Manipulation of Protein Aggregation

M.ENG.

- **Johanna Chong** (R.J. RAM)
Integrated Single and Multiwavelength Fiber Ring Laser with Non-integrated Gain
- **Ragheb El Khaja** (J. HAN)
Electro-chemical Stimulation of Neuromuscular Systems Using Ion-Selective Membranes: Flexible Device Fabrication and Motor Unit Recruitment Order
- **Itaru Hiromi** (C.G. SODINI)
Hybrid Intensity and Time-Off Flight Signal Processing Techniques for Intelligent Distance Sensors
- **Yuxuan Lin** (T. PALACIOS)
Optical properties of 2-dimensional transition metal dichalcogenides
- **Kevin Linke** (C.G. SODINI)
On-Chip Input for a High Voltage SAR ADC
- **Anartya Mandal** (J.A. DEL ALAMO)
Modeling 0.18m BiCMOS (S18) High Sheet Resistance (RPH) Polysilicon Resistor Lifetime Drift
- **Alec Poitsch** (C.G. SODINI)
A High Voltage, High Current, Low Error Operational Amplifier with Novel Features
- **Joohyun Seo** (C.G. SODINI)
Continuous and Non-Invasive Blood Pressure Monitoring Using Ultrasonic Methods
- **Ky-Anh Tran** (C.G. SODINI)
A Spread-Spectrum Clock Generator Using Phase Interpolation for EMI Reduction
- **Theresa Yeh** (T. PALACIOS AND A.P. CHANDRAKASAN)
Efficient Wireless Charging with Gallium Nitride FETs
- **Xianzhen Zhu** (C.G. SODINI)
Build Blocks of a 250MHz bandwidth, 10-bit Continuous-time Delta-Sigma Analog to Digital Converter

S.M.

- **Fahri Erinc Hizir** (N.X. FANG)
Experiments and Simulations on a Metamaterial Based Ultrasonic Scanner
- **Rui Jin** (A.P. CHANDRAKASAN)
Circuits and Systems for Efficient Portable-to-Portable Wireless Charging
- **Karim Khalil** (K.K. VARANASI)
Active Lubricant-Impregnated Surfaces
- **Yoon Kyung Lee** (N.X. FANG)
Light Induced Torque at Multipolar Plasmon Resonance
- **Wenjie Lu** (J.A. DEL ALAMO)
Nano-scale Ohmic Contacts for III-V MOSFETs
- **Ian McKay** (E.N. WANG)
A Thermo-Adsorptive Battery
- **Daniel Preston** (E.N. WANG)
Electrostatic Charging of Jumping Droplets on Superhydrophobic Nanostructured Surfaces: Fundamental Study and Applications
- **Priyanka Raina** (A.P. CHANDRAKASAN)
Architectures for Computational Photography
- **Yufei Wu** (J.A. DEL ALAMO)
Degradation of GaN High Electron Mobility Transistors under High-power and High-Temperature Stress
- **Yang Xi** (H.-S. LEE)
Design of a Continuous-Time Bandpass Delta-Sigma Modulator
- **Yujia Yang** (K.K. BERGGREN)
Development of Optical Field Emitter Arrays
- **Tao Yu** (J.L. HOYT)
InGaAs/GaAsSb Type-II Heterojunction Vertical Tunnel-FETs
- **Dongni Zhang** (A.P. CHANDRAKASAN)
Low-Energy Radix-2 Serial and Parallel FFT Designs

PH.D.

- **Gleb Akselrod** (V. BULOVIĆ)
Exciton Transport and Coherence in Molecular and Nanostructured Materials
- **Mohammad Araghchini** (J.H. LANG)
MEMS Toroidal Magnetics for Integrated Power Electronics
- **Jay-Byum Chang** (K.K. BERGGREN)
Templated Self-Assembly for Complex Pattern Fabrication and Computation

PH.D. (CONTINUED)

- **Albert Chang** (D.S. BONING AND H.-S. LEE)
  Low-Power High-Performance SAR ADC with Redundancy and Digital Background Calibration
- **Kailiang Chen** (C.G. SODINI AND A.P. CHANDRAKASAN)
  A Column-Row-Parallel ASIC Architecture for 3D Wearable / Portable Medical Ultrasonic Imaging
- **Hyungryul Choi** (N.X. FANG AND G. BARBASTATHIS)
  Nanostructured Multifunctional Surfaces
- **Sungwon Chung** (H.-S. LEE)
  Energy-Efficient Wireless Transmitter Architecture for Mobile Multimedia
- **Isaac Ehrenberg** (N.X. FANG AND S. SARMA)
  Fully Conformal Metamaterials via Rapid 3D Prototyping
- **Feng Gao,** (T. PALACIOS)
  Impact of Electrochemical Process on the Degradation Mechanisms of AlGaN/GaN HEMTs
- **Sushmit Goswami** (H.-S. LEE)
  Monolithic RF Frontends for Ubiquitous Wireless Connectivity
- **Stephen A. Guerrera** (A.I. AKINWANDE)
  Individually Controlled Field Emission Arrays
- **Amneet Gulati** (S. MANALIS)
  Mass-based assay for single-cell growth in budding yeast
- **David He,** (C.G. SODINI)
  Dynamic ON-Resistance in High-Voltage GaN Field-Effect-Transistors
- **Eric V. Heubel** (L.F. VELÁSQUEZ-GARCÍA)
  Enhancing RPA Energy Measurements with Micro-Aligned Electrodes
- **Sha Huang** (J. HAN)
  The Relevance of Red Blood Cell Deformability in the Pathophysiology of Blood Disorders
- **Thomas Humplik** (E.N. WANG)
  Investigating Transport Through Sub-Nanometer Zeolites Pores
- **Donghyun Jin** (J.A. DEL ALAMO)
  Dynamic ON-resistance in High-Voltage GaN Field-Effect Transistors
- **Rhokyun Kwak** (J. HAN)
  Nonlinear Ion Concentration Polarization: Fundamentals and Applications
- **Hyuk-Min Kwon** (K.K. VARANASI)
  Tailoring Hydrodynamics of Non-wetting Droplets with Nano-engineered Surfaces
- **Dong Seup Lee** (T. PALACIOS)
  Deeply-Scaled GaN High Electron Mobility Transistors for RF Applications
- **Sunghyuk Lee** (H.-S. LEE)
  Techniques for Low-Power High-Performance ADCs
- **Andrej Lenert** (E.N. WANG)
  Tuning Energy Transport in Solar Thermal Systems using Nanostructured Materials
- **Prayudi Lianto** (C.V. THOMPSON)
  Mechanism of Catalyst Stability of Metal-Assisted Chemical Etching of Silicon
- **Jill Macko** (V. BULOVIĆ)
  Nanostructural Engineering of Vapor-Processed Organic Photovoltaics for Efficient Solar Energy Conversion from Any Surface
- **Mariana Markova,** (H.-S. LEE)
  Precision Hybrid Pipeline ADC
- **Nenad Miljkovic** (E.N. WANG)
  Development and Characterization of Micro/ Nanostructured Surfaces for Enhanced Condensation
- **Robert R. Mitchell III** (C.V. THOMPSON)
  Investigation of Lithium-Air Battery Discharge Product Formed on Carbon Nanotube and Nanofiber Electrodes
- **Adam Paxson** (K.K. VARANASI)
  Advanced Materials for Enhanced Condensation Heat Transfer
- **Rahul Rithe** (A.P. CHANDRAKASAN)
  Energy-Efficient Systems Design for Mobile Processing Platforms
- **Parthiaban Santhanam** (R.J. RAM)
  Thermo-Electrically Pumped Semiconductor Light Emitting Diodes
- **Yasuhiro Shirasaki** (V. BULOVIĆ)
  Efficiency loss mechanisms in colloidal quantum-dot light-emitting diodes
- **Yildiz Sinangil** (A.P. CHANDRAKASAN)
  Energy-Aware System Design Using Circuit Reconfigurability with a Focus on Low-Power SRAMs
- **Han Wang,** (T. PALACIOS)
  Two-Dimensional Materials for Electronic Applications
- **Eric Winokur,** (C.G. SODINI)
  Single-Site, Noninvasive, Blood Pressure Measurements at the Ear Using Ballistocardiogram (BCG) and Photoplethysmogram (PPG)and a Low Power, Reflectance-Mode PPG SoC
- **Liang Jie Wong** (L.F. VELÁSQUEZ-GARCÍA)
  Compact Laser-Driven Electron Acceleration, bunch compression, and Coherent Nonlinear Thompson Scattering (main advisor was F. X. Kärtner)
- **Marcus Yip** (A.P. CHANDRAKASAN),
  Ultra-low-power Circuits and Systems for Wearable and Implantable Medical Devices
- **Hang Yu** (C.V. THOMPSON)
  Mechanisms for Intrinsic Stress Evolution During and after Polycrystalline Film Growth

MTL Seminar Series

MTL hosts a series of talks each semester known as the MTL Seminar Series. Seminar speakers are selected on the basis of their knowledge and competence in the areas of microsystems research, manufacturing, or policy. The seminars are open to the public. A listing of recent seminars is also provided at http://mtlweb.mit.edu. Audio/PPT, MP3 audio, and archived streaming videos of the seminars are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group at MTL and to the MIT community. For more information regarding the MTL Seminar Series, send e-mail to valeried@mit.edu.

FALL 2013

- October 8, 2013
  Yurii Vlasov, IBM
  IBM Silicon Nanophotonics Technology for Datacenters and Computer Systems
- October 22, 2013
  Parijat Deb, Philips Lumileds Lighting Company Solid State
  Lighting: Present Status and Challenges Ahead
- October 29, 2013
  Brent Segal, Lockheed Martin
  Nanotechnology from Laboratory to Space
- November 5, 2013
  John Memishian, Analog Devices
  Fun with Micromachines: Measuring Zeptofarads and Picometers for Under a Buck
- November 12, 2013
  Dennis Buss, Texas Instruments
  Microelectronics: An Industry in Transition
- November 19, 2013
  Naveen Verma, Princeton University
  Systems Based on Large-area Electronics: Bringing Electronics to Life through Extensive Interfacing with the Physical World
- November 26, 2013
  Hidemi Takasu, ROHM Semiconductor
  More Than Moore Opens the New Semiconductor World
- December 3, 2013
  MTL Doctoral Dissertation Seminar: Anthony Zorzos, MIT
  3-D Optical Waveguide Arrays for In-Vivo Optogenetics: Development and Application

SPRING 2014

- February 26, 2014
  Brett Miwa, Maxim Integrated
  Opportunities and Challenges in Mobile Power Management
- March 5, 2014
  Ljubisa Stevanovic, GE Global Research
  Are SiC Power Devices Ready for Prime Time?
- March 12, 2014
  Samuel Schaevitz, Lilliputian Systems, Inc.
  Commercialization of a MEMS Solid Oxide Fuel Cell
- April 2, 2014
  Zachary J. Lemnios, IBM
  IBM: Leading the Next Era of Information Technology
- April 9, 2014
  Marko Loncar, Harvard
  Diamond - Engineer's Best Friend
- Friday, April 25, 2014
  Thomas Stieglitz, University of Freiburg/IMTEK
  Miniaturized Neural Interfaces and Implants in Basic and Translational Research
- April 30, 2014
  Yao-Wen Chang, National Taiwan University
  Design for Manufacturability for Sub-14nm Nanometer Technologies
- May 14, 2014
  MTL Doctoral Dissertation Seminar: Xiang Zhou, MIT
  III-nitride Nanowires & Heterostructures: Growth & Optical Properties on Nanoscale

Glossary

MIT ACRONYMS

BE	Department of Biological Engineering
Biology	Department of Biology
ChemE	Department of Chemical Engineering
CICS	Center for Integrated Circuits and Systems
CMSE	Center for Materials Science and Engineering
DMSE	Department of Materials Science & Engineering
EECS	Department of Electrical Engineering & Computer Science
KI	David H. Koch Institute for Integrative Cancer Research
MAS	Media Arts & Sciences
MechE	Department of Mechanical Engineering
MEDRC	Medical Electronic Device Realization Center
MITEI	MIT Energy Initiative
MIT Skoltech	MIT Skoltech Initiative
MTL	Microsystems Technology Laboratories
NSE	Department of Nuclear Science & Engineering
Physics	Department of Physics
S3TEC	Solid State Thermal Energy Conversion Center
Sloan	Sloan School of Management
SMA	Singapore-MIT Alliance
↳ **SMART**	Singapore-MIT Alliance for Research and Technology (Center)
↳ **SMART-LEES**	SMART Low Energy Electronic Systems
TPP	Technology and Policy Program

OTHER ACRONYMS

AFOSR	Air Force Office of Scientific Research
AFRL	Air Force Research Laboratory
ARL	Army Research Laboratory
ARPA-E	Advanced Research Projects Agency - Energy (DOE)
CIQM	Center for Integrated Quantum Materials - National Science Foundation
CUNY	The City University of New York
DARPA	Defense Advanced Research Projects Agency
↳ **DAHI**	DARPA Diverse Accessible Heterogeneous Integration
↳ **E-PHI**	DARPA Electronic-Photonic Heterogeneous Integration
↳ **MPC**	DARPA Microscale Power Conversion Program
↳ **MTO**	DARPA Microsystems Technology Office

DOE	Department of Energy
↳ **ARPA-E**	Advanced Research Projects Agency – Energy
FENA	Center for Functional Engineered Nano Architectonics
GBMF	Gordon and Betty Moore Foundation
IARPA	Intelligence Advanced Research Projects Activity
IEDM	International Electron Devices Meeting (IEEE)
IEEE	Institute of Electrical and Electronics Engineers
ISSCC	International Solid-State Circuits Conference (IEEE)
MASDAR	Masdar Institute of Science and Technology
MRS	Materials Research Society
NASA	National Aeronautics and Space Administration
NDSEG	National Defense Science and Engineering Graduate Fellowship
NIH	National Institutes of Health
NSRC	Natural Sciences and Engineering Research Council (Canada)
NSF	National Science Foundation
↳ **CIQM**	NSF Center for Integrated Quantum Materials
↳ **CSNE**	NSF Center for Sensorimotor Neural Engineering
↳ **E3S**	NSF Center for Energy Efficient Electronics Science
↳ **GRFP**	NSF Graduate Research Fellowship Program
↳ **MRSEC**	NSF Materials Research Science and Engineering Centers
↳ **NCN-NEEDS**	NSF Network for Computational Nanotechnology - Nano-Engineered Electronic Device Simulation Node
NTU	Nanyang Technological University
NUS	National University of Singapore
ONR	Office of Naval Research
↳ **DRIFT-MURI**	Design-for-Reliability Initiative for Future Technologies - Multidisciplinary University Research Initiative
SRC	Semiconductor Research Corporation
SRC/FCRP	Focus Center Research Program
↳ **C2S2**	SRC/FCRP Center for Circuits & Systems Solutions
↳ **IFC**	SRC/FCRP Interconnect Focus Center
↳ **MSD**	SRC/FCRP Materials Structures and Devices
TSMC	Taiwan Semiconductor Manufacturing Company

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