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GaN-Based DNA Detectors

J. Wu, O. Saadat, T. Palacios

Sponsorship: MIT, MIT-France Program

The ability to detect DNA hybridization is an extremely useful tool that can be used in a variety of biological and medical tests. Currently, the use of microarrays and optical detection is the predominant technology to detect hybridization. However, this technology is slow, requires extensive optical systems and alignment as well as, in many cases, special labeling of at least one of the strands. Although electrical detection of DNA hybridization could overcome many of these problems, no reliable method has yet been developed.

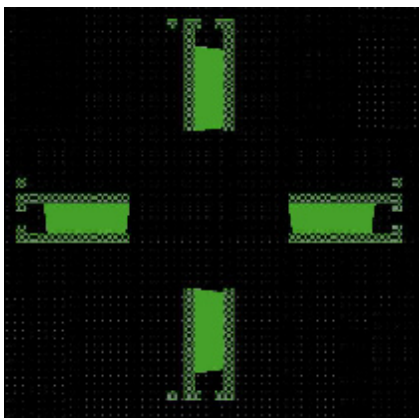
Our group is exploring three new technologies to electrically detect DNA hybridization: surface acoustic wave (SAW) two-dimensional tomography, a quantum-dot conductance sensor and a high electron mobility transistor (HEMT)–based sensor. These technologies primarily rely on the charge and mass changes that occur when single strands hybridize and are based on the excellent properties of nitride semiconductors. These materials are excellent for biological sensors due to their biocompatibility, excellent transport properties and unprecedented chemical stability.

The SAW sensor takes advantage of the piezoelectric properties of GaN to generate acoustic waves which travel along the surface of the semiconductor. These waves are affected by the material through which they travel and the mass of the molecules on top (i.e., DNA). The magnitude of the signal generated by the receiving electrode

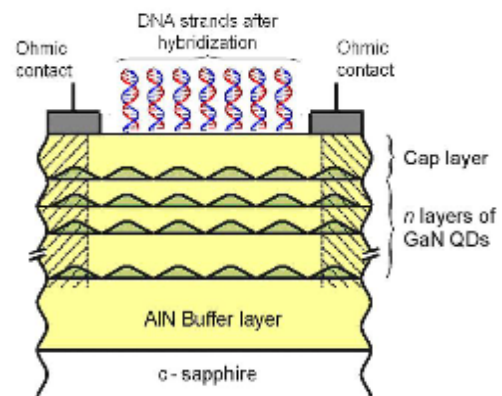
at varying frequencies allows for a measurement of the mass of the molecule on the surface. In the new devices being developed in our group, both the input and output electrodes are tapered in order to achieve spatial selectivity.

In collaboration with CEA-Grenoble (France), we are also developing a new kind of conductance sensor, which measures the effect of charges' electric field on a semiconductor. To increase the sensitivity of the device, an AlN layer containing layers of GaN quantum dots very close to the sensing surface has been fabricated. The exponential dependence in the hopping conduction through the quantum dot layer is expected to allow unprecedented levels of sensitivity in this new device.

The third sensing device being developed is based on GaN HEMTs. Conventional transistor-based sensors operate in a similar way to conductance sensors, and are thus subject to similar problems. Using an entirely different method of measurement may increase the signal to noise ratio. Instead of using the charged DNA to change the gate voltage and resulting current, we are positioning the DNA in the drain access region of the device in order for a change in charge to affect the parasitic capacitance of the transistor and, consequently, the switching frequency. We can then detect whether the single strand of DNA has successfully hybridized by checking if the maximum switching frequency has increased.



▲ Figure 1: Top view of the SAW-based two-dimensional DNA sensor.



▲ Figure 2: Cross-section of the quantum-dot conductivity sensor being developed in our lab.

Transport Properties and Advanced Device Simulation of AlGaIn/GaN Transistors

J.M. Tirado, Z. Xu, B. Lu, T. Palacios
Sponsorship: ONR, DARPA

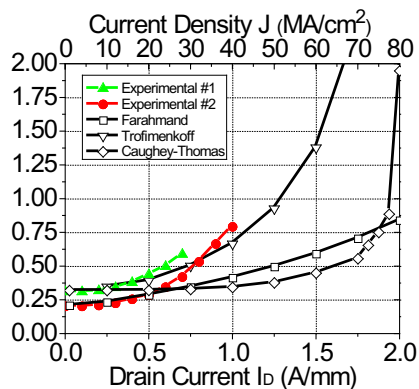
The small signal access resistance (r_s) of AlGaIn/GaN high-electron mobility transistors (HEMTs) plays a critical role in the performance of these transistors. Its importance increases with drain current limits the transconductance, frequency performance, linearity, and efficiency of GaN transistors [1]. This work studies the origin of this increase through a combination of theoretical and experimental approaches. The quasi-saturation of the electron velocity with the electric field due to the emission of optical phonons has been identified as the main reason for the increase.

We have solved the Poisson equation in the channel on an AlGaIn/GaN HEMT to calculate the variation of the longitudinal electric field in the source access region as a function of distance and current density. Three different transport models have been analyzed: (a) Farahmand [2], (b) Trofimenkoff [3], and (c) Caughey-Thomas [4]. The source access resistance in an AlGaIn/GaN HEMT with a source to gate distance of $0.8 \mu\text{m}$ was evaluated as a function of drain current. There is an important nonlinear behavior of the resistivity as the current density is increased. The small signal access resistance of several devices was experimentally measured and compared to theoretical results as it is plotted in Figure 1. Two AlGaIn/GaN HEMT devices grown by MOCVD on SiC substrates and different layer com-

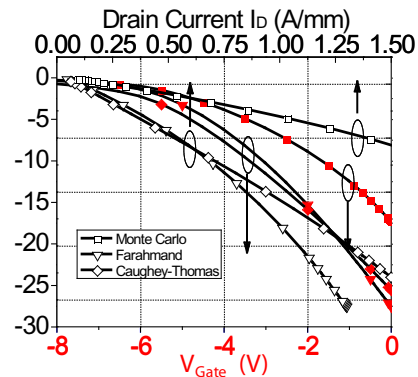
positions were considered. As shown in this figure, excellent agreement between the experimental and the theoretical results has been obtained.

To get more insight into the reasons for the increasing access resistance, a two-dimensional commercial device simulator (Silvaco Atlas) has been used to calculate the electric field in the source access region of a GaN HEMT. The three different transport models were added to the Atlas simulations. Figure 2 shows the results of these simulations. In all the cases, the longitudinal electric field in the source access region is in the 10-30 KV/cm range, a region where the differential mobility is changing very rapidly. From our simulations and modeling, this change in mobility is the dominant cause of the increase of r_s .

In conclusion, our theoretical model, simulations and experimental work indicate that the electron transport in the 30-40 KV/cm range is better described by a Trofimenkoff model than by the different Monte Carlo simulations reported in literature, which indicates that current Monte Carlo techniques are overestimating the mobility at moderate electric fields.



▲ Figure 1: Small signal access resistance, r_s versus drain current I_D (and current density J) calculated for the three transport models considered in this work. The experimental values measured in two different samples are also plotted for comparison.



▲ Figure 2: Electric field versus gate voltage V_G (and drain current I_D) extracted from simulations using Atlas. Each curve belongs to a different transport model: (a) Monte Carlo, (b) Farahmand, and (c) Caughey-Thomas. Values are extracted from the middle point of the distance between S-G contacts.

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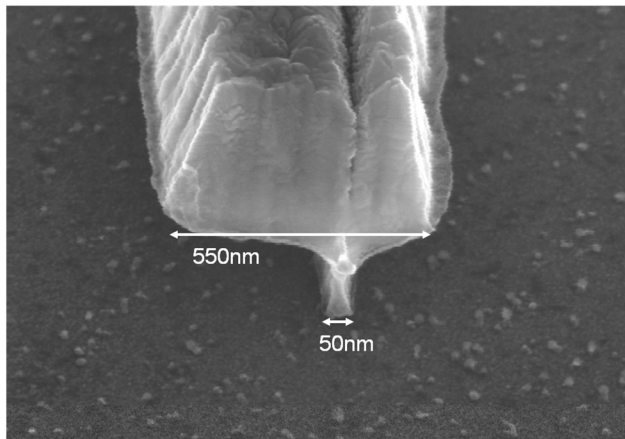
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GaN Transistors for W-band Applications

O. Saadat, J.W. Chung, F. Miéville, T. Palacios
Sponsorship: ONR

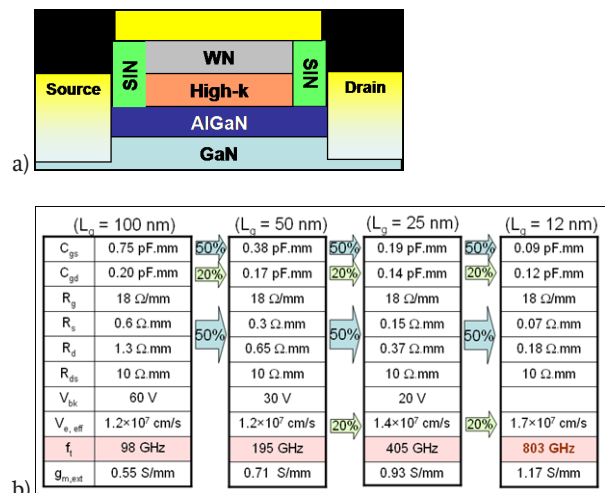
Many applications await the development of compact solid-state amplifiers at frequencies above 30 GHz. Satellite transponders, anti-collision car radars, high-speed point-to-point wireless transmitters, and highly efficient radars for the Navy are only a few of the many civil and military applications that would benefit from these amplifiers in the 30- to 94-GHz range. The basic requirements are common to all these applications: small, reliable, efficient, and low-noise solid-state amplifiers to substitute traveling-wave-tube amplifiers currently used at these frequencies.

GaN-based high electron mobility transistors (HEMTs) are the most promising option for power amplification at frequencies above 30 GHz. However the use of AlGaN/GaN HEMTs at these high frequencies requires the aggressive shrinking of several critical dimensions of transistors. For example, reducing the gate length is crucial for increasing high frequency performance. Therefore, we have fabricated AlGaN/GaN HEMTs with gates with $L_g = 50$ nm. These devices, shown in Figure 1, have gates defined by the Raith 150 e-beam lithography system.



▲ Figure 1: Scanning electron micrograph of an AlGaN/GaN HEMT with a 50-nm gate fabricated at MTL.

In addition to reducing the gate length, we need to reduce the source and drain access resistances by reducing the distances between the source and gate and the drain and gate, respectively [1]. Self-aligned gates will reduce these distances. However, we need a gate stack that can stand the 870°C anneal required to form ohmic contacts. Since the standard Ni/Au/Ni rectifying gate stack does not survive these high temperature anneals, we are developing new gate stacks based on the integration of a high-k dielectric like HfO_2 and a refractory metal like WN. Similar gate stacks for Si devices are able to stand more than 900°C anneals, which makes them promising for self-aligned gates on AlGaN/GaN HEMTs [2]. The dielectric and the gate metal used in this project are deposited in situ by atomic layer deposition, which allows for both atomic layer precision and a clean interface between the high-k dielectric and the gate metal. After the gate is defined, insulating sidewalls are deposited to isolate the gate from the source and drain before depositing the source and drain metal and annealing the metal. A proposed structure for the completed self-aligned gate appears in Figure 2a.



▲ Figure 2: a) Proposed structure for a self-aligned AlGaN/GaN HEMT and b) performance roadmap for sub-mm-wave GaN HEMTs.

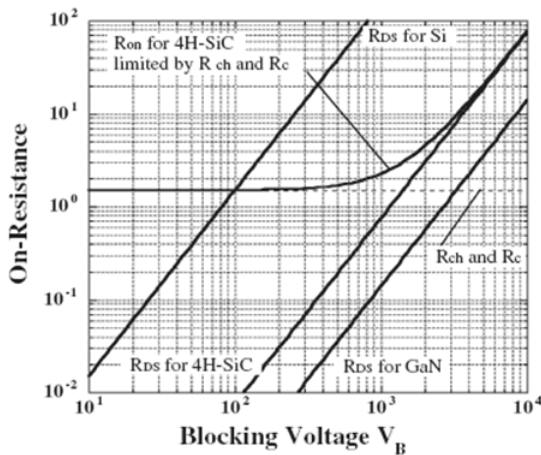
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Nitride-based Power Electronics

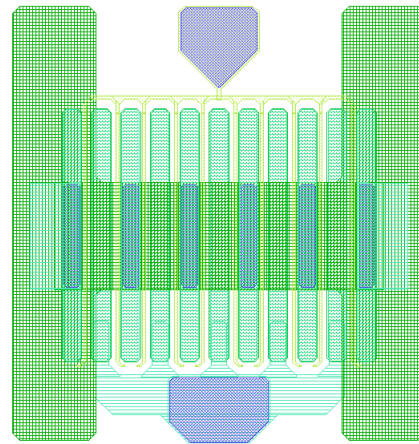
B. Lu, D.J. Perreault, T. Palacios
Sponsorship: MIT, MTL, MITEI

The wide-band-gap III-nitride semiconductors are extremely promising materials for power electronic applications where power switches with high breakdown voltage and ultra-low on-resistance are required. The AlGaN/GaN transistor has unprecedented current-carrying capability due to the extremely high 2-dimensional electron gas density ($>1.3 \times 10^{13} \text{cm}^{-2}$) and mobility ($>2000 \text{cm}^2/\text{V}\cdot\text{s}$) at the heterojunction [1]. The same material system has a very high critical electric field of more than 5 MV/cm. This combination significantly reduces the loss of GaN-based power transistors. Since the total loss (conduction loss and switching loss) of a power switch is reversely proportional to $\mu^{1.5} E_c$ [2], theoretically the total loss of the GaN-based power switches will be about 14 times smaller than Si-based transistors and the switching frequency will be 200 times higher. Figure 1 compares the blocking voltage and on-resistance of GaN with Si and 4H-SiC.



▲ Figure 1: Blocking voltage V_B vs. on-resistance R_{on} for Si, 4H-SiC and GaN [3].

In spite of the great interest of the industry and academia in this material system, its application in power electronics has been hindered until now due to the normally-on character of the state-of-the-art AlGaN/GaN heterojunction field effect transistors. Also, traditionally they are horizontal devices, which are not preferred in power electronics. Our group is working on the design and fabrication of new transistor structures to overcome these two important limitations. Some of the applications of the vertical normally-off GaN-based power devices in our group include the power inverters for hybrid vehicles and power converters for new power delivery systems in microprocessors.



▲ Figure 2: Structure of multi-finger power transistor developed at MIT.

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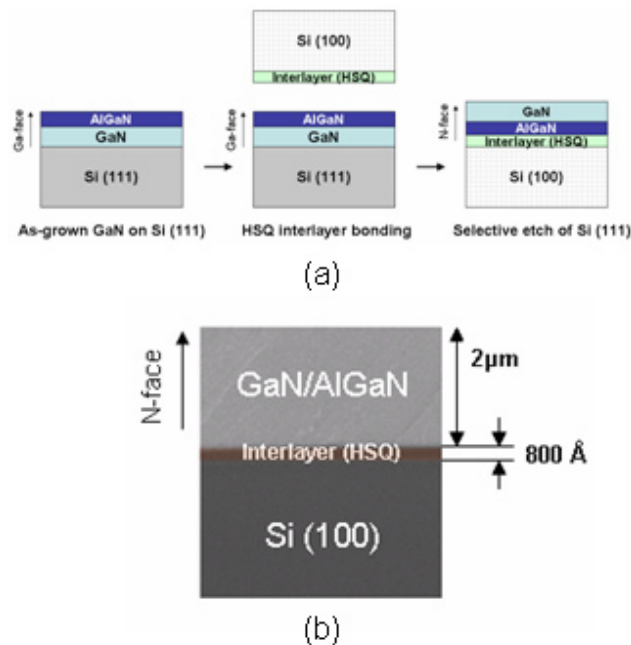
N-face GaN/AlGaN HEMTs on Si (100) Substrate

J.W. Chung, T. Palacios
Sponsorship: DARPA, MIT, MTL

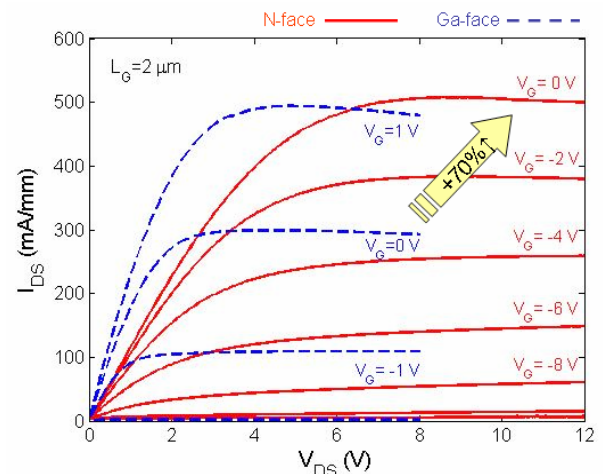
Nitride-based transistors are revolutionizing power electronics and high-frequency amplifiers due to their combination of high current densities and large breakdown voltage. Although most of the reported GaN devices have been fabricated on nitride structures grown along the c-direction (i.e., the Ga-face), N-face GaN/AlGaN transistors have the potential for higher electron confinement and lower contact resistances. However, in spite of this promise, the performance of N-face devices is still much lower than in Ga-face devices due to the inferior material quality. Although N-face devices have been grown by molecular beam epitaxy and, recently, by metal-organic chemical vapor deposition (MOCVD), the growth of N-face nitrides is much more challenging than the growth of the more stable Ga-face structure. In this paper, we present a new method to fabricate N-face GaN/AlGaN HEMTs based on the substrate removal of a Ga-face AlGaN/GaN layer grown on Si.

The Ga-face AlGaN/GaN transistor structures used in this work were grown on Si (111) substrates by MOCVD at Nitronex. To have access to the N-face of these samples, we have developed the substrate transfer technology shown in Figure 1a. First, the Ga-face surface

was bonded to a Si (100) carrier wafer by using a hydrogen silsesquioxane (HSQ) interlayer. After the wafer bonding, the original Si (111) substrate is completely removed by dry etching using an SF_6 -based plasma. Figure 1b shows a scanning electron micrograph of the AlGaN/GaN layer transferred to the Si (100) substrate. After the substrate transfer, the N-face GaN buffer is etched by electron cyclotron resonance-reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture until the desired distance between the N-face GaN surface and the AlGaN/GaN interface is achieved. The N-face GaN/AlGaN structures fabricated through the substrate removal process have been used in the fabrication of N-face high electron mobility transistors (HEMTs). In this sample, the distance between the N-face surface and the 2DEG was reduced to 1000 Å by ECR etch. Figure 2 shows the drain current versus drain voltage characteristic of the N-face device and it is compared to a Ga-face HEMT used as a reference. For a gate voltage of 0 V, the maximum current in the N-face device is almost 70% higher than in the Ga-face device. This difference is mainly due to the higher charge density in the N-face device.



▲ Figure 1: (a) Main processing steps in the fabrication of N-face GaN on Si (100) substrate through substrate removal. (b) Cross-section scanning electron microscope (SEM) picture of the AlGaN/GaN layer transferred to the Si (100) substrate. False color has been added to highlight the HSQ interlayer in the structure.



▲ Figure 2: The DC current-voltage characteristics of N-face (solid line) and Ga-face (dashed line) HEMTs with a gate length (L_G) of 2 μm . Almost 70% higher maximum current at $V_G = 0 V$ is achieved in N-face HEMTs. Higher on-resistance (R_{on}) in N-face HEMTs is due to unoptimized ohmic contacts.

Suitability of GaN Semiconductors for Digital Electronics

F. Miéville, J.W. Chung, T. Palacios
Sponsorship: MIT, MTL

In this work, we study the suitability of nitride-based high electron mobility transistors (HEMTs) for a beyond-Si digital electronic scenario. Table 1 shows some of the formidable challenges that Si devices face in the next few years as well as some of the new solutions offered by GaN-based electronics.

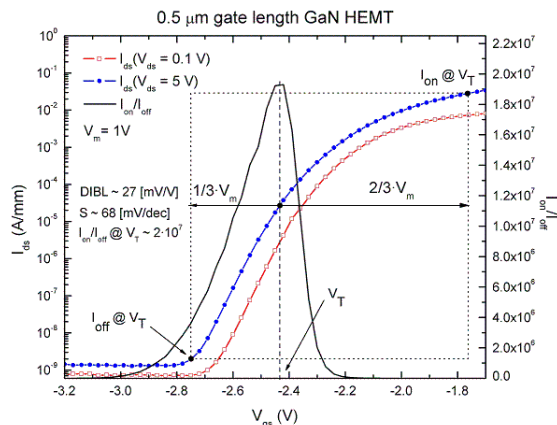
The outstanding properties of nitride semiconductors could be extremely useful in ultra-scale digital electronics. For example, the large bandgap of nitrides allows a significant reduction in the band-to-band tunneling leakage current with respect to Si and other III-V devices. The high dielectric constant of AlN in combination with its very high polarization coefficients allows the fabrication of nitrides devices with an equivalent thickness (EOT) of only 0.6 nm and a charge density in excess of $2 \cdot 10^{13}$ electrons/cm² (without random dopant fluctuations). Moreover, the very high electron velocity, ($> 2.5 \cdot 10^7$ cm/s) coupled with the charge density has already allowed the demonstration of current densities above 3 mA/ μ m in short channel devices.

Our first generation of submicron GaN HEMTs (0.5- μ m gate length) for digital electronics grown on Si substrate has already shown excellent performance through the figures-of-merit for logic [1]. Indeed sub-threshold slope S , ratio I_{on}/I_{off} and drain-induced barrier lowering $DIBL$ extracted in Figure 1 are better than in the actual state-of-the-art 65-nm gate length Si nMOS transistors: $S = 85$ mV/dec, $DIBL = 120$ mV/V and $I_{on}/I_{off} = 3.1 \cdot 10^4$ [2]. Regarding the high-frequency performance, a maximum current gain cut-off frequency (f_T) of 163 GHz and a power gain cut-off frequency (f_{max}) of 230 GHz were already achieved in 90-nm gate length GaN HEMTs on silicon carbide (SiC) substrate [3]. The characterization of below-50-nm devices is part of our ongoing work,

In conclusion, the unique properties of nitrides combined with advanced technologies make nitride materials very attractive options for addressing some of the formidable challenges of digital electronics and for continuing Moore's law beyond the 22-nm node.

	Si Roadmap Challenges	Solutions offered by GaN-based electronics
Low power dissipation	Drain to source and Band to Band tunneling	Large E_g (3.4 eV) reduces tunneling
Excellent channel control	Low gate leakage	Crystalline AlN cap layer, low interface state density, high-k barrier, fluorine treatment
	Enhanced gate control	High effective mass, quantum capacitance
High current	Discrete dopant fluctuations	Polarization doping
	Parasitic resistance	Highly doped InN and polarization grading
	Electron velocity and mobility	$v_e \sim 3 \cdot 10^7$ cm/s For $L_g < 10$ nm $\rightarrow v_{ballistic} \sim 7 \cdot 10^7$ cm/s
	High current density	> 2 A/mm already achieved on large devices 1.3 A/mm in E-mode devices

▲ Table 1: Main challenges for Si technology, according to the International Technology Roadmap for Semiconductor, and some solutions offered by a nitride-based electronics.



▲ Figure 1: Main logic-related figures of merit for a 0.5- μ m gate length GaN HEMT. The definitions used are proposed by Chau *et al.* [1].

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Reliability of GaN HEMTs Grown on Si Substrate

S. Demirtas, J.A. del Alamo
 Sponsorship: ARL

GaN has attracted great attention recently as a new material for high electron mobility transistors (HEMT) due to its wide band gap (3.4 eV) and high breakdown field value ($>3 \times 10^6$ V/cm). These unique properties enable high-voltage, high-power RF operation. The main hindrance to the deployment of GaN HEMTs in such applications is their limited reliability. Recent reliability studies on GaN HEMTs grown on SiC substrates have helped identify the physical mechanisms responsible for degradation [1]. However, silicon, due to its low cost, availability in large diameters and well characterized electrical and thermal characteristics, is a very attractive substrate alternative to SiC. The problem is that with greater lattice and thermal mismatch than in the case of a SiC substrate, GaN layers grown on silicon substrates tend to have many more dislocations. This brings additional concerns to the reliability of GaN HEMTs fabricated on Si substrates.

Our research is focused on the electrical reliability of GaN HEMTs on silicon substrates. We perform our reliability experiments on industrial devices provided by our collaborator, Nitronex Corporation. In these experiments, various stress biases are applied to the devices, which are characterized by a benign characterization suite. Important figures of merit such as the maximum drain current ($I_{D,MAX}$), gate leakage current in the OFF state ($I_{G,OFF}$), drain resistance (R_D) and source resistance (R_S) are monitored before, during and after the stress tests by means of this characterization suite.

Our first observation in GaN HEMTs grown on Si substrate is the relatively high critical voltage for $I_{G,OFF}$ degradation as compared to those built on SiC substrate. $I_{G,OFF}$ is found to degrade permanently

by several orders of magnitude around $V_{DG} = 60$ V when V_{DS} is set to 0 V (Figure 1). No such $I_{G,OFF}$ degradation is observed either in the OFF state, where we stepped V_{DS} up to 60 V while maintaining $I_D = 10$ mA/mm, or under high power stress conditions where we stepped V_{DS} up to 35 V while maintaining $I_D = 400$ mA/mm. These results may be attributed to the reduced elastic energy in the GaN buffer due to relaxation by the greater size and number of dislocations that are present on layers grown on a Si substrate [1]. Initial strain in the GaN buffer layer is a factor in the degradation of GaN HEMTs on SiC substrate through the inverse piezoelectric effect.

As the lattice and thermal mismatches between GaN and Si are larger as compared to GaN and SiC, we have investigated $I_{D,MAX}$ response of a device at rest to a diagnostic pulse before and after electrical degradation. In effect the diagnostic pulse can be considered an injection of carriers to fill the traps associated with dislocations in the fresh device and possibly additional traps created during the electrical stress. As carriers are trapped, we expect $I_{D,MAX}$ to decrease and then increase as these carriers are detrapped over time. Indeed, trapping is observed in both virgin and stressed devices (Figure 2). The amount of current collapse in response to such a carrier injection is proportional to the number of traps. These traps reduce $I_{D,MAX}$ under steady state conditions and even more so after the application of a diagnostic pulse. Clearly, electrical stress has increased the number of traps through the inverse piezoelectric effect.

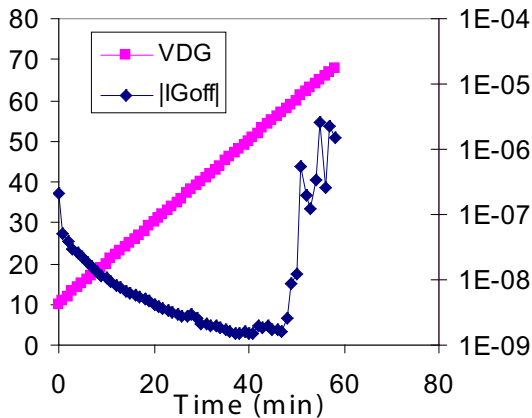


Figure 1: Electrical degradation of gate current in an electrical step-stress with $V_{DS} = 0$ V. Gate voltage is stepped down by 1V starting from -10 V. Gate leakage current degrades by several orders of magnitude starting around $V_{DG} = 60$ V.

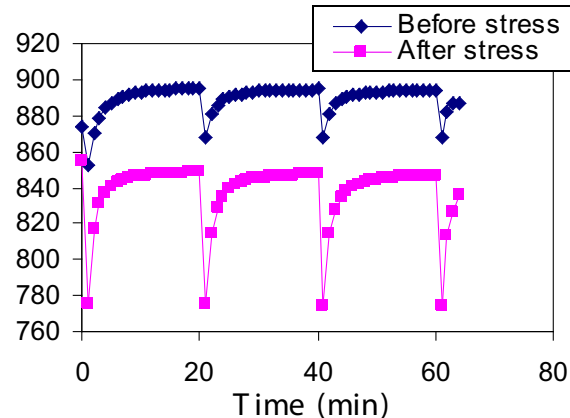


Figure 2: $I_{D,MAX}$ response of a device to a -10 V pulse at its gate before and after a $V_{DS} = 0$ V stress test where gate voltage was stepped down to -80 V. The pulse is applied every 20 minutes when the device is at rest and the current is monitored for more than 60 min. Duration of the pulse is 10 sec.

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Degradation Mechanisms of GaN High-electron-mobility Transistors

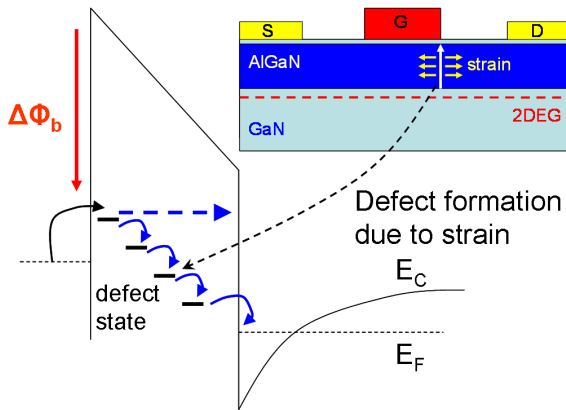
J. Joh, L. Xia, J.A. del Alamo
Sponsorship: ARL

Recently, GaN-based electronic devices have attracted great interest because of their high breakdown electric field ($>3 \times 10^6$ V/cm). Also, due to the strong piezoelectric effect and spontaneous polarization of both GaN and AlN, a high sheet carrier density ($\sim 10^{13}$ cm $^{-2}$) can be easily achieved in the AlGaN/GaN heterostructure without any doping. In addition, high electron mobility (~ 1500 cm 2 /V-s) and high saturation velocity ($\sim 2 \times 10^7$ cm/s) make GaN-based devices, especially GaN high-electron-mobility transistors (HEMT), suitable for high-power and high frequency RF power applications, such as WiMAX or WLAN base stations and radars.

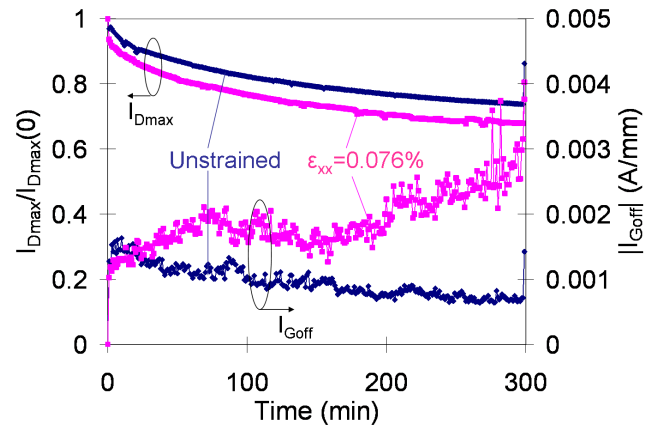
Although promising performance results have been demonstrated, GaN HEMTs still have limited reliability. In RF power applications, GaN HEMTs must operate at high voltage where good reliability is essential. Physical understanding of the fundamental reliability mechanisms of GaN HEMTs is still lacking today. In this research, we perform systematic reliability experiments on GaN HEMTs provided by our industrial collaborators, TriQuint Semiconductor and BAE systems. In our study, GaN HEMTs have been electrically stressed at various bias conditions. During the stress experiments, they were periodically characterized by a benign characterization suite that we have developed.

In previous studies, we have found that one of the main degradation mechanisms in GaN HEMT is crystallographic defect formation in the AlGaN barrier layer due to tensile strain produced by the inverse piezoelectric effect [1]. These introduced defect states decrease the channel carrier density by trapping electrons, which in turn decreases I_D . In our recent research, we have found that a large gate current increase that is widely observed during stress tests is also related to the same mechanism [2]. The defect states in the AlGaN barrier not only trap channel electrons but also provide a path that helps gate current conduction (Figure 1). In order to confirm our hypothesis, we have fabricated a jig through which external mechanical strain can be applied to a chip. In our hypothesis, additional tensile strain should accelerate degradation in I_D and I_G because it adds to the strain produced by the inverse piezoelectric effect. In fact, as Figure 2 shows, degradation in both I_D and I_G is accelerated under external tensile mechanical strain.

Our hypothesis suggests that device design that minimize elastic energy and peak vertical electric field in AlGaN can improve the electrical reliability of GaN HEMTs.



▲ Figure 1: Conceptual I_G degradation mechanism for bias stress. Crystallographic defects produced by the inverse piezoelectric effect provide a leakage path across the AlGaN barrier.



▲ Figure 2: Change in I_{Dmax} and I_{Goff} of OFF-state stress experiments. The devices are stressed at $V_{GS} = -7$ V and $V_{DS} = 35$ V. The device stressed under tensile mechanical strain shows larger degradation in both I_D and I_G .

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RF Power CMOS for Millimeter-wave Applications

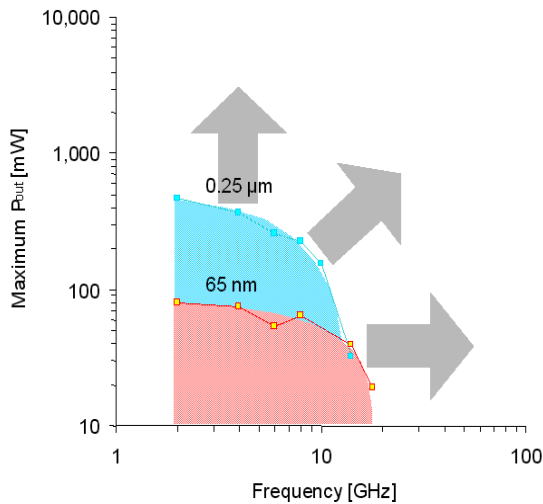
U. Gogineni, J.A. del Alamo, D.R. Greenberg (IBM)
Sponsorship: SRC, IBM

Radio frequency (RF) power amplifiers are core components of almost all wireless systems. Traditionally III-V, SiC, or SiGe devices have been used in power amplifiers because of their ability to deliver high power and operate at high frequencies. Recently there has been an increased interest in using Si CMOS for designing single-chip integrated systems for operation in the millimeter-wave regime. Specific applications in this regime include wireless LAN and collision-avoidance radar. A key concern in using CMOS for these applications is the inability of CMOS to yield high-efficiency power amplifiers with power levels over 10mW in the 60-80 GHz regime.

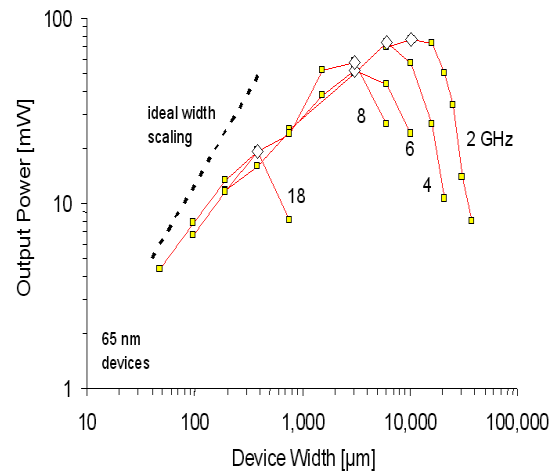
Previous research in our group at MIT into the RF power performance of 65-nm and 90-nm Si CMOS devices [1-2] has shown that it is not possible for currently available Si CMOS to operate significantly beyond 20 GHz (Figure 1). The effective cut-off frequency for power (frequency at which the output power drops below 10 mW) is around 20 GHz for 0.25- μ m, 90-nm, and 65-nm CMOS. This suggests that further scaling is unlikely to improve the situation despite improvements in f_T and f_{max} . The reason for this saturation in the effective power cut-off frequency is that the optimum device width

that delivers the maximum power at any frequency scales down as the frequency goes up (Figure 2). This effect suggests that the bottleneck for power is the device layout, especially the back-end wiring.

In this research, we are investigating options for device optimization with the goal of pushing the power operation of Si CMOS into the millimeter-wave regime. Small-signal equivalent circuits are extracted from S-parameter measurements on devices with different widths to identify the main power gain detractors. A parasitic-aware layout approach is then employed to design new test structures with minimized parasitics, thus resulting in an improvement in the effective power cut-off frequency for a given technology. Some of the design ideas being explored include (a) alternate ways of connecting elemental devices in parallel, (b) use of multiple levels and thicker levels of metal to reduce interconnect resistance and (c) design of on-chip bias and matching circuits. These designs are being implemented on IBM's 65-nm and 45-nm CMOS technologies.



▲ Figure 1: Maximum power (at peak PAE) vs. frequency of operation obtained in nominal 0.25- μ m devices ($V_{dd}=2.5$ V) and 65-nm devices ($V_{dd}=1$ V) fabricated in a 65-nm process [1].



▲ Figure 2: Maximum power (at peak PAE) vs. device width for different frequencies for 65-nm devices ($V_{dd}=1$ V) [1].

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Small-signal Equivalent Circuit Modeling for Si RF Power LDMOSFETs on SOI

Y. Ikura, J.A. del Alamo

Sponsorship: Fuji Electric Device Technology

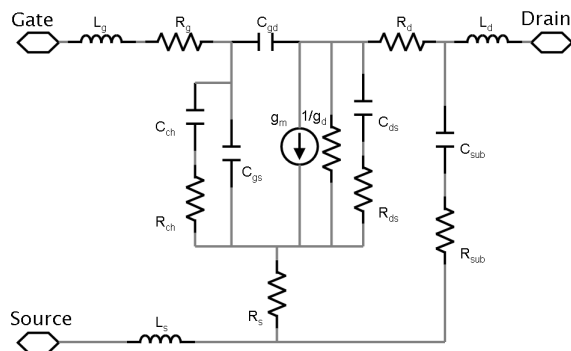
Small-signal equivalent circuits are used to model a transistor's high-frequency performance and to design RF power amplifier circuits. Historically the equivalent circuit of Si LDMOSFETs is borrowed from that of compound semiconductor MESFETs. However, the circuit components are not the same in Si LDMOSFETs, especially in the case of those on SOI. The purpose of our work is to develop an equivalent circuit based on the physical understanding of Si LDMOSFETs on SOI and to identify a suitable small-signal parameter extraction procedure.

In our model, we employ a substrate network and a channel network that is distributed (see Figure 1). The substrate network (C_{sub} , R_{sub}) models the inversion layer that appears at the interface between the Si substrate and the buried oxide and is affected by the gate, drain, and substrate bias, especially in the case of a high resistivity SOI substrate [1]. The channel network (C_{ch} , R_{ch}) models the inversion layer that appears underneath the gate oxide and constitutes a capacitive coupling with the gate.

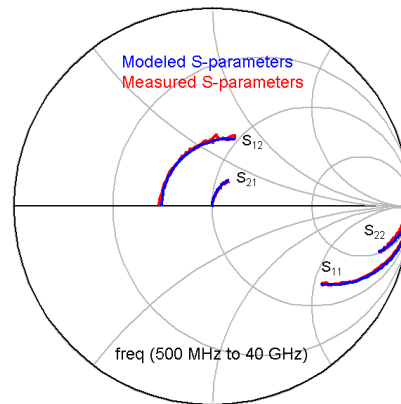
The parameters are extracted using an optimizer that minimizes the least-squares error function between the measured S-parameters and the modeled ones. If there are too many parameters, the extrac-

tion becomes time-consuming and the extracted values are not necessarily consistent with the physical characteristics. We developed a novel parameter extraction procedure that consists of two steps. In each step, there are fewer parameters and they are extracted more accurately than in the case of a single step extraction method. First, the gate-bias independent parameters are extracted from S-parameters measured under zero gate bias ($V_{gs}=0$ V, $V_{ds}=5$ V). In the second step, the remaining parameters are extracted from the S-parameters measured under a gate bias that turns on the transistor and a drain bias that is the same as in the first step ($V_{ds}=5$ V).

Using our model and procedure, we observed excellent fit between the modeled S-parameters and the measured ones from 0.5 to 40 GHz (Figure 2). The cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) are determined as the frequency at which the current-gain $|H_{21}|^2$ and the maximum available gain (MAG) become 0 dB, respectively. We also observed an excellent match between the modeled data ($f_T=16.5$ GHz, $f_{max}=30.5$ GHz) and the measured data ($f_T=16$ GHz, $f_{max}=30.5$ GHz).



▲ Figure 1: Small-signal equivalent circuit of LDMOSFET on SOI. A distributed substrate network and a distributed channel network are employed.



▲ Figure 2: Modeled S-parameters (blue lines) and measured ones (red lines) of LDMOSFET on SOI.

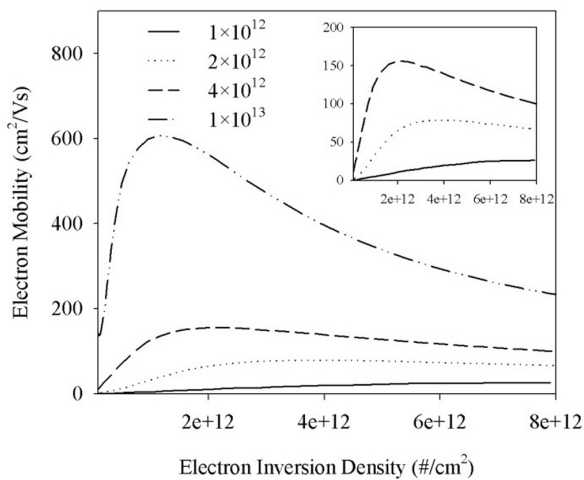
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ALD Gate Dielectrics for High-mobility Materials

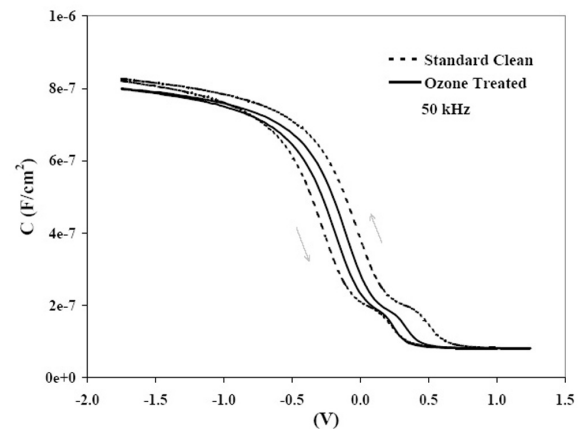
J. Hennessy, A. Ritenour, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

Maintaining historical performance trends for CMOS devices requires semiconductors with high carrier mobility. Germanium offers significant enhancements in bulk electron and hole mobility relative to silicon; however, past work on surface-channel Ge n-MOSFETs has shown poor performance. In this work, high-k gate dielectrics were deposited on germanium using atomic layer deposition (ALD) in order to explore methods for improving the electrical quality of the gate interface. Figure 1 shows the extracted electron mobility of phosphorous-implanted Ge n-FETs fabricated with an $\text{Al}_2\text{O}_3/\text{AlN}$ gate stack [1]. It is seen that n-FETs that received the highest dose implant exhibit buried channel behavior and show a large increase in peak mobility. This demonstrates that the gate/channel



▲ Figure 1: Effective carrier mobility for Ge and n-FETs that received 1×10^{12} , 2×10^{12} , 4×10^{12} , and 1×10^{13} cm^{-2} phosphorous channel implants. Inset shows electron mobilities for the devices that showed no buried-channel operation [1].

interface is the primary contributor to degraded Ge n-FET performance. Figure 2 illustrates an example of the ongoing effort towards improving the electrical characteristics of the Ge/high-k interface. MOS capacitors were fabricated with an $\text{Al}_2\text{O}_3/\text{AlN}$ gate deposited by ALD. Substrates treated only with a wet clean show capacitance-voltage characteristics with minimum mid-gap density of interface states (D_{it}) of $\sim 2 \times 10^{12}$ $\#/\text{cm}^2$. Substrates that received the same wet clean plus in-situ exposure to ozone immediately prior to gate deposition show a substantial reduction in both D_{it} ($\sim 4 \times 10^{11}$ $\#/\text{cm}^2$) and hysteresis.



▲ Figure 2: MOS capacitors on p-Ge with an $\text{Al}_2\text{O}_3/\text{AlN}$ dielectric. Both samples received a wet clean in $\text{HCl} \rightarrow \text{NH}_4\text{OH}/\text{H}_2\text{O}_2 \rightarrow \text{HCl}$ prior to deposition. The ozone treated sample received a 30-min exposure to O_3 (20% wt in O_2) immediately prior to dielectric deposition.

Reference

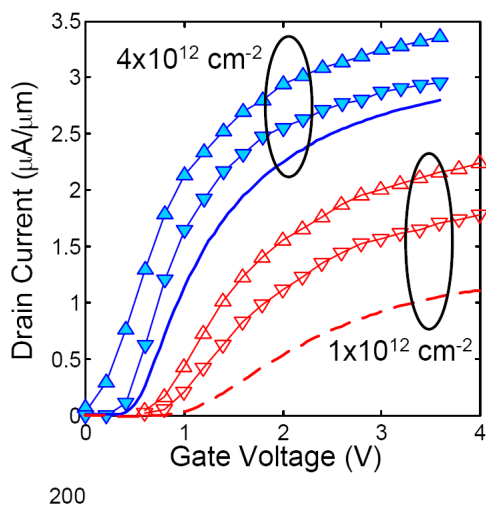
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Pulsed I-V and Q-V Characterization of Germanium MOSFETs

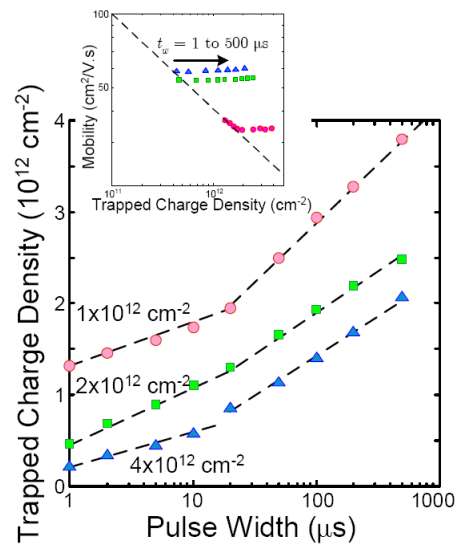
A. Khakifirooz, A. Ritenour, J. Hennessy, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

Despite significantly higher electron and hole mobility in bulk germanium compared to silicon and the early reports of very high carrier mobility in Ge-channel NMOS and PMOS transistors [1], recent efforts to demonstrate high-performance germanium MOSFETs have not been successful. Carrier mobility is generally much lower than what is expected in germanium inversion layers. While hole mobility improvement as high as $2.5\times$ compared to the silicon universal curve has been observed with an epitaxially grown silicon passivation layer [2], reported values of electron mobility are still disappointing. This low mobility is believed to be in part due to the presence of high concentration of interface traps near the conduc-

tion band [3]. In this work, pulsed I-V and Q-V measurements are used to characterize carrier transport and charge trapping in germanium-channel NMOS transistors. Charge trapping is shown to be significant in these transistors and the “intrinsic” electron mobility extracted from pulsed I-V measurements can be much higher than what extracted from DC measurements, as Figure 1 shows. As Figure 2 shows, phosphorus passivation of the germanium-dielectric interface reduces the density of fast traps near the Ge-dielectric interface. Analysis of the relationship between electron mobility and trapped charge density reveals that mobility depends only on the density of fast traps.



▲ Figure 1: Comparison of I_d-V_g characteristics from DC (lines) and pulsed (symbols) measurements for devices that received different doses of phosphorus implantation prior to high-k deposition. Measurements were performed on ring transistors with $W/L = 180/5\mu\text{m}$. Pulsed measurements were done by applying a train of pulses with increasing pulse height, $t_r = t_f = 100$ ns, and $t_w = 100$ μs . The \triangle represents the measurements at the beginning of the pulse, while ∇ indicates the values after t_w .



▲ Figure 2: Pulse-width dependence of the density of trapped charges for Ge NMOSFETs with different doses of phosphorous passivation implant and at a constant inversion charge density of about $1.7 \times 10^{13} \text{cm}^{-2}$ at the beginning of the pulse (corresponding to a pulse amplitude of about 3 V). The inset shows the relation between mobility and density of trapped charges and demonstrates that electron mobility depends only on the density of fast traps.

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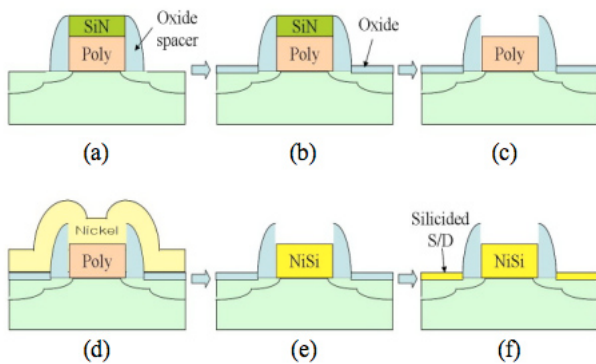
Low-temperature NiSi-gate, -source/drain Si/SiGe Heterostructure MOSFETs

J. Lee, J.L. Hoyt, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

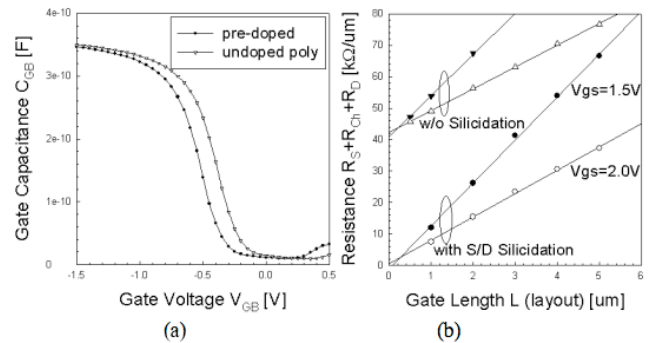
The development of integrated circuits and devices faces many technological challenges, which are related to material and process integration [1]. This work presents a nickel silicidation as a low-temperature process for the fabrication of heterostructure MOSFETs. Low-temperature processing is necessary for heterostructure devices with high germanium contents (>50%) in order to maintain the source/drain and channel structure.

Nickel silicide (NiSi) has been widely studied in recent years for use as a contact material, and now it has been widely used as a gate material. NiSi gates offer higher gate capacitance, lower sheet resistance and superior scalability compared to conventional

polysilicon gates [2,3]. Low source/drain (S/D) series resistance is also important for nano-scale devices due to their higher current densities. The nickel silicidation process can be done with simple heat treatment at temperatures lower than 450°C, which is necessary in order to preserve the shallow junctions and hetero channel structure of high-performance, short-channel devices. This work shows the integration of a nickel fully silicided (FUSI) gate and silicided source/drain regions with a Si/SiGe heterostructure MOSFET device (see Figure 1). Figure 2 shows the modulation of gate work function (a) and the reduction of S/D resistance (b) by the nickel silicidation process.



▲ Figure 1: CMP-free FUSI gate fabrication: (a) gate stack and oxide spacer; (b) reoxidation of S/D; (c) SiN removal; (d) nickel deposition; (e) anneal and Ni removal; (f) S/D silicidation.



▲ Figure 2: (a) Flat-band voltage shift due to modulation of the gate work function, which is done by pre-doping the poly gate. (b) NiSi source/drain silicidation effect on Si/SiGe heterostructure MOSFETs.

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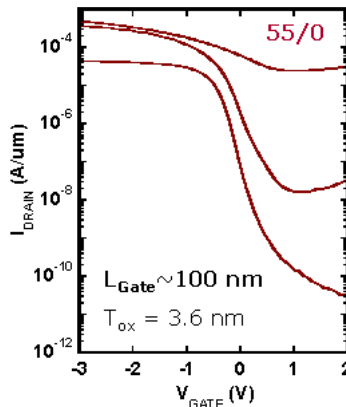
Fabrication of Strained-SiGe and Strained-Ge Short Channel p-MOSFETs on Insulator

L. Gomez, P. Hashemi, J.L. Hoyt

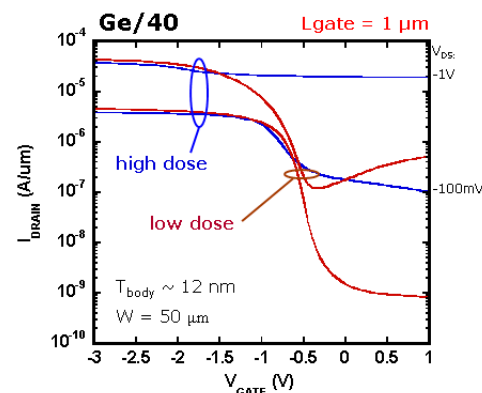
Sponsorship: NSF Graduate Student Research Fellowship, SRC/FCRP MSD

Scaling of device dimensions can no longer provide the necessary current drive enhancements to continue historic performance gains. The use of strain and novel channel materials provides enhanced transport characteristics to increase device performance. Thin-body on-insulator substrate configurations can also be utilized to offer improved electrostatic control in deeply scaled MOSFETs. In this work these two performance enhancers are combined onto a single substrate to realize the performance benefits of strained-Si/strained-Ge heterostructures on insulator (Ge HOI). Hole mobility enhancements as high as 10x have been observed for an 8-nm-thick buried Ge channel strained to $\text{Si}_{0.5}\text{Ge}_{0.5}$ at an inversion charge density of 7×10^{12} [1]. The goal of this work is to determine if significant performance enhancement can be observed at shorter gate lengths. A short-channel process has been developed to characterize the performance of p-MOSFETs fabricated in this material.

Short channel process development was conducted on substrates with strained $\text{Si}_{0.45}\text{Ge}_{0.55}$ channels pseudomorphic to unstrained SOI. Devices were fabricated with gate lengths down to ~ 100 nm. Figure 1 presents the ID-VG characteristics for a 100-nm p-MOSFET with reasonable electrostatic behavior. Further work was conducted to investigate the effect of source/drain doping and damage on off-state leakage in strained-Ge channel devices. Figure 2 presents ID-VG characteristics for 1- μm -long devices fabricated on Ge/40 HOI. The use of a low-mass (Boron) and low-dose implant condition is observed to provide a significant reduction in off-state leakage. Work is in progress to utilize the developed short channel process to fabricate strained-Ge p-MOSFETs that incorporate the modified implant condition to reduce the off-state leakage.



▲ Figure 1: Drain current vs. gate bias for 100-nm 55/0 strained SiGe channel device. The strained-SiGe channel thickness is ~ 7 nm. The V_{DS} was biased at -100mV , -1V , and -2V .



▲ Figure 2: Drain current vs. gate bias for 1- μm -long p-MOSFET fabricated on Ge/40 HOI substrates with two different implant conditions. The high-dose implant conditions are BF_2 , $4 \times 10^{15} \text{cm}^{-2}$, at 17 keV. The low-dose implant conditions are Boron, $2 \times 10^{14} \text{cm}^{-2}$, at 6 keV.

Reference

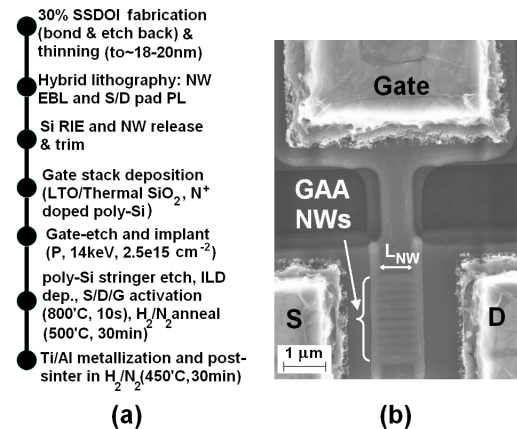
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Fabrication and Characterization of Uniaxially Strained-Si Gate-all-around n-MOSFETs

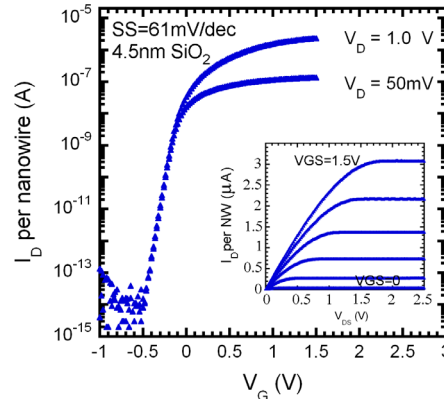
P. Hashemi, L. Gomez, M. Canonico (Freescale Semiconductor), J.L. Hoyt
Sponsorship: SRC/FCRP MSD

Gate-all-around nanowire (NW) MOSFETs are of great interest for future CMOS technology generations due to the enhanced scalability compared to conventional planar MOSFETs [1]. Strain engineering is mandatory to improve the mobility and drive current of these devices. Among possible strain configurations, uniaxial tension in the [110] direction is most favorable to enhance NMOS performance due to reduction of the electron effective mass [2]. In this work, fabrication of uniaxially strained-Si NW n-MOSFETs with a gate-all-around (GAA) architecture is reported. Figure 1(a) shows the MOSFET fabrication process flow. The starting material was 18-20-nm-thick Strained-Silicon-Directly-on-Insulator (SSDOI) substrate (with high biaxial stress level of 2.2GPa), fabricated using a bond and etch-back technique. Unstrained, commercial SOI was also thinned to the same thickness as the SSDOI films, by successive dry oxidation and oxide removal. The device mesa isolation was performed using hybrid lithography, after a photolithography (PL) step to create e-beam alignment marks. For this purpose, a XR-1541™ NW hard mask layer was created using e-beam lithography at a dose of 1.2mC/cm² and energy of 30keV, followed by development in TMAH. The S/D regions were then patterned using photolithography and the Si was etched in an RIE system. The hard-mask removal and nanowire suspension were performed using dilute HF solution. This nano-scale patterning is shown to transform the biaxial stress to uniaxial tension (~2.2GPa), as confirmed by UV-micro Raman

spectroscopy. After RCA cleaning, which further trims the NWs, a poly-Si (~80-nm)/SiO₂ gate stack was formed all around the wires. Two sets of gate oxides were created: 14-nm deposited LTO and 4.5-nm thermally grown oxide. The gate was then patterned using SEM-corrected photolithography with alignment error of less than 50 nm. Next, S/D phosphorous ion implantation was performed at 14 keV with a dose of 2.5e15 cm⁻². The poly-Si stringers on S/D regions were removed by photolithography followed by an RIE step. After interlayer dielectric deposition, the implant was activated at 800 °C for 10sec. A hydrogen anneal at 500 °C significantly improves the subthreshold characteristics. Contact vias were opened, followed by Ti/Al contact metallization, metal patterning, and H₂/N₂ annealing. Figure 1(b) shows a SEM micrograph of 0.8-μm-long GAA strained-Si NW n-MOSFET with 10 parallel NWs (each ~20nm wide). Figure 2 shows the transfer characteristics of a 1-μm-long strained-Si NW n-MOSFET (W_{NW}~15nm and t_{NW}~13nm) with 4.5-nm thermal oxide dielectric. The inset shows the output characteristics of this MOSFET. The device shows excellent long channel characteristics with ideal subthreshold swing of 61mV/dec and high on-to-off ratio of ~10⁸. The drain current is scaled per NW. Further analysis is in progress to study the effect of the uniaxial strain on the performance of GAA NW n-MOSFETs.



▲ Figure 1: (a) Fabrication process and (b) SEM image of GAA NW n-MOSFET (W_{NW}~20nm, L_{NW}=0.8μm).



▲ Figure 2: Transfer and output (inset) characteristics of 1-um-long GAA strained-Si NW n-MOS (W_{NW}~15nm and t_{NW}~13nm) with 4.5-nm thermal oxide dielectric.

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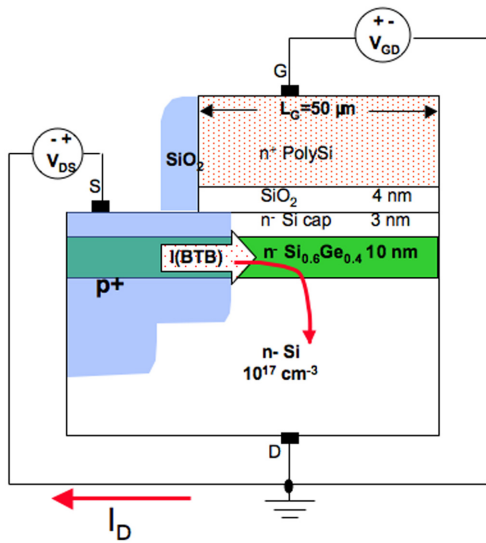
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Measurement and Analysis of Enhanced Gate-controlled Band-to-band Tunneling in Highly Strained Silicon-Germanium Diodes

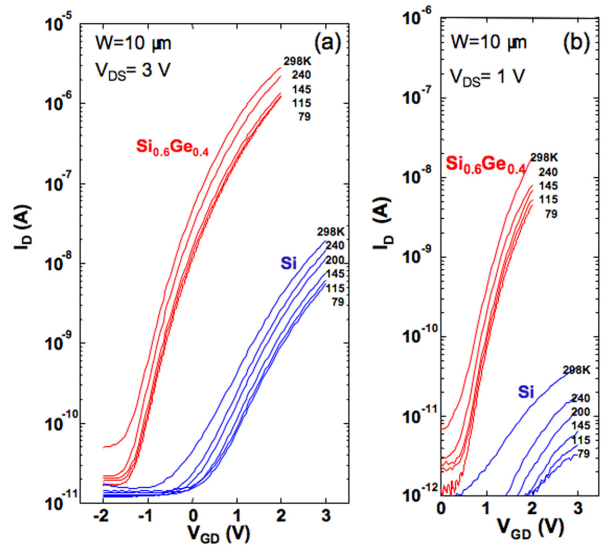
O.M. Nayfeh, C. Ni Cheirigh, J.L. Hoyt, D.A. Antoniadis
 Sponsorship: SRC/FCRP MSD, Singapore-MIT Alliance, Intel Fellowship

Strained silicon-germanium ($\text{Si}_{0.6}\text{Ge}_{0.4}$) gated diodes have been fabricated and analyzed. The devices exhibit significantly enhanced gate-controlled tunneling current over that of co-processed silicon control devices. The current characteristics are insensitive to measurement temperature in the 80- to 300-K range. The independently extracted valence band offset at the strained $\text{Si}_{0.6}\text{Ge}_{0.4}$ /Si interface is 0.4 eV, yielding a $\text{Si}_{0.6}\text{Ge}_{0.4}$ bandgap of 0.7 eV, much reduced

compared to that of Si. The results are consistent with device operation based on quantum mechanical band-to-band tunneling rather than on thermal generation. Moreover, simulation of the strained $\text{Si}_{0.6}\text{Ge}_{0.4}$ device using a quantum mechanical band-to-band tunneling model is in good agreement with the measurements. The results are important for the realization of tunneling field-effect transistors with large current drive and steep sub-threshold swing.



▲ Figure 1: Schematic cross-section of the gated strained $\text{Si}_{0.6}\text{Ge}_{0.4}$ diode and measurement biasing.



▲ Figure 2: Measured characteristics for $\text{p}^+\text{Si}_{0.6}\text{Ge}_{0.4}/\text{n Si}$ and $\text{p}^+\text{Si}/\text{n Si}$ gated-diode structures, for various temperatures from 300 down to 80K, at reverse diode biases of (a) 3V, and (b) 1V. The doping profiles are similar for both the $\text{Si}_{0.6}\text{Ge}_{0.4}$ and Si devices. The significant increase in tunneling rate, due to the smaller bandgap, is evident in the measurements of the $\text{Si}_{0.6}\text{Ge}_{0.4}$ gated diodes.

Reference

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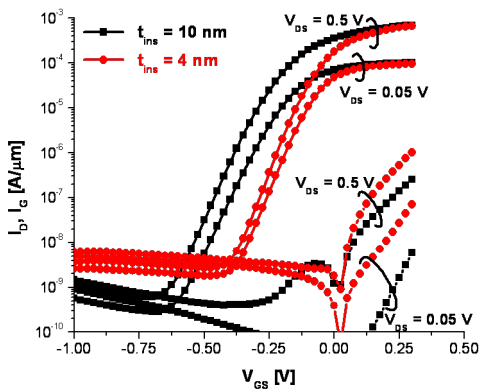
Logic Potential of 40-nm InAs HFETs

D.-H. Kim, J.A. del Alamo

Sponsorship: Intel Corporation, SRC/FCRP MSD

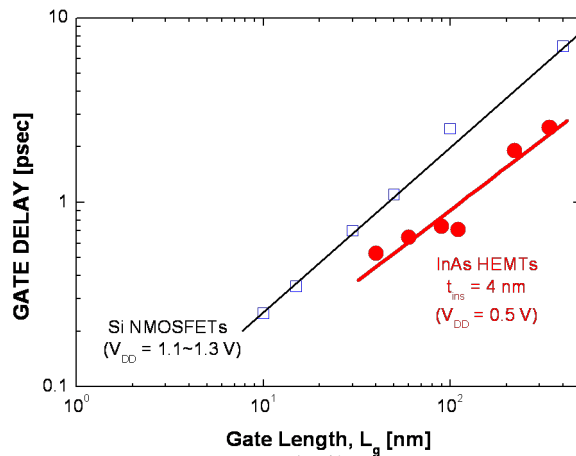
Scaling of Si CMOS has been the cornerstone of the microelectronics revolution during the past 30 years. While a matter of considerable debate, CMOS scaling now seems to be fast approaching the end of the roadmap. It is therefore of great importance to find a new technology that would allow the extension of Moore's law beyond the point where Si can reach. Indium Arsenide (InAs), with a room temperature bulk electron mobility in excess of 20,000 cm²/V-s, is a promising candidate for channel material in a future III-V CMOS technology [1]. In our work, we are investigating the logic potential of InAs heterostructure-FETs (HFETs) as a model device for a future InAs MOSFET with a high-k gate dielectric [2].

We have fabricated pseudomorphic InAs HFETs on InP substrate with two different values of InAlAs insulator thickness ($t_{\text{ins}} = 10$ nm and 4 nm). Our shortest device has a gate length of 40 nm. We have evaluated the logic performance of these devices. Figure 1 shows sub-threshold and gate leakage (I_g) characteristics of representative



▲ Figure 1: Subthreshold and gate leakage characteristics of 40-nm InAs HFETs with two different values of t_{ins} at $V_{\text{DS}} = 0.05$ and 0.5 V. The $t_{\text{ins}} = 4$ nm devices exhibit excellent subthreshold behavior.

40-nm InAs HFETs with two different values of t_{ins} , at V_{DS} of 0.05 and 0.5 V. As t_{ins} decreases, V_{T} shifts positive and sub-threshold slope improves considerably. Excellent $S = 70$ mV/dec and $\text{DIBL} = 80$ mV/V are obtained for the $t_{\text{ins}} = 4$ nm device. This sharp sub-threshold characteristics yield an $I_{\text{ON}}/I_{\text{OFF}}$ ratio in excess of 10^4 at $V_{\text{DD}} = 0.5$ V. Figure 2 shows the logic gate delay (CV/I) as a function of gate length of InAs HFETs with $t_{\text{ins}} = 4$ nm. For comparison, values of state-of-the-art Si CMOS are also shown. Our InAs HFETs exhibit significantly better logic delay than Si-CMOS, in spite of the lower voltage of operation. Also, the logic delay scales gracefully down to a 40-nm gate length regime, suggesting further scaling potential. This outstanding performance of our InAs HFETs stems from the excellent transport properties of the InAs channel. Our research reveals that InAs is a material with great potential for applications beyond Si CMOS logic.



▲ Figure 2: Logic gate delay (CV/I) as a function of gate length for InAs HFETs with $t_{\text{ins}} = 4$ nm, as well as Si CMOS. Our InAs HFETs exhibit much lower values of CV/I than those of Si CMOS even at the lower supply voltage of 0.5 V.

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90 nm Self-aligned InGaAs HEMT for Logic Applications

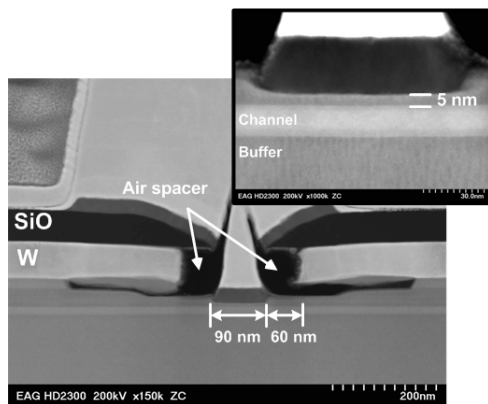
N. Waldron, J.A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel

As conventional CMOS scaling approaches the end of the roadmap, identifying a new logic device technology is becoming a matter of great urgency. With a room temperature electron mobility easily in excess of $10,000 \text{ cm}^2/\text{V}\cdot\text{s}$, InGaAs represents a very attractive proposition as a channel material. Previously it has been shown that InGaAs-based high-electron-mobility transistors (HEMT) show great promise for logic applications [1]. However, the conventional design of HEMTs is not well suited for VLSI applications. The gate is not self-aligned and is typically separated from the source/drain by a distance of around $1 \mu\text{m}$. This results in a large device footprint and associated parasitics. Also the exposed surface area and alloyed contacts represent a reliability concern.

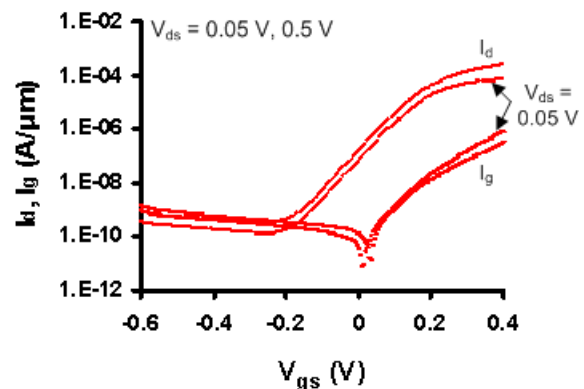
To address these issues we have developed a self-aligned process that reduces the gate to source/drain distance to less than 60 nm [2]. This distance is about a $15\times$ improvement over the conventional design. We start by depositing a layer of W to form the non alloyed source drain regions which is followed by a SiO deposition. The gate

is formed by a two step electron-beam lithographic process. In the first step, the gate foot is defined by etching the SiO and W. At this point the W is co-incident with the edge of the SiO. The W is then pulled back from the edge of the SiO by means of a selective etch thus forming an "air-spacer". The second litho is then aligned back to this etched foot, the recess etch is carried out and gate metal is deposited and lifted off. In this process we achieve device enhancement mode operation by thinning the insulator by means of a dry etch. Figure 1 shows a TEM of a completed device with a gate length of 90 nm . The self-aligned devices exhibit excellent logic figures of merit. The 90 nm devices in which the barrier was thinned to 5 nm have a V_T of 60 mV , maximum transconductance of $1.3 \text{ mS}/\mu\text{m}$, sub-threshold (SS) swing of $70 \text{ mV}/\text{dec}$ and drain-induced barrier lowering (DIBL) of $55 \text{ mV}/\text{V}$ with an $I_{\text{on}}/I_{\text{off}}$ ratio of 1.8×10^3 (Figure 2).

The self-aligned architecture developed in this work should allow us to map out the ultimate logic potential of III-V FETs.



▲ Figure 1: TEM of a completed 90-nm gate length self-aligned device. The gate is separated from the W source/drain ohmics by an "air-spacer" of 60 nm . This is about a $15\times$ improvement over conventional designs. The barrier thickness has been thinned by means of a dry etch to 5 nm (see inset). This vertical scaling results in enhancement mode devices with excellent electrostatic integrity.



▲ Figure 2: Subthreshold characteristics of a 90-nm self-aligned device where the barrier thickness has been scaled to 5 nm . At a V_{ds} of 0.5 V , the device has a threshold voltage of 60 mV , SS of $70 \text{ mV}/\text{V}$, DIBL of $55 \text{ mV}/\text{V}$ and a maximum transconductance of $1.3 \text{ mS}/\mu\text{m}$.

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P-channel InGaAs HEMTs for Beyond-Si Complementary Logic

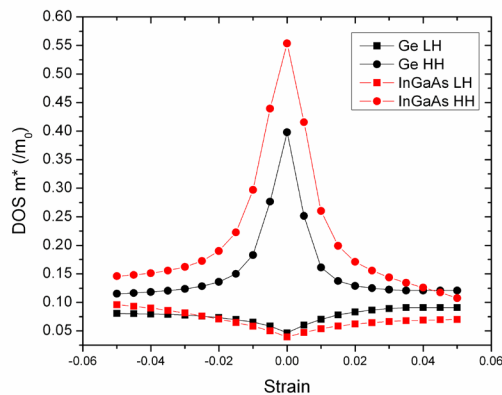
L. Xia, J.A. del Alamo
Sponsorship: SRC/FCRP MSD

As the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches the end of the roadmap, its performance improvement brought by size-scaling will reach a limit. Among beyond-Si logic alternatives, InGaAs shows superior potential for n-channel FET-type devices. [1] However, to match the performance of n-channel InGaAs FETs, great efforts are needed to improve current p-channel InGaAs devices. The goal of our study is to enhance the transport properties in p-channel InGaAs FETs, to ultimately implement complementary logic based on InGaAs as a successor to modern Si technology.

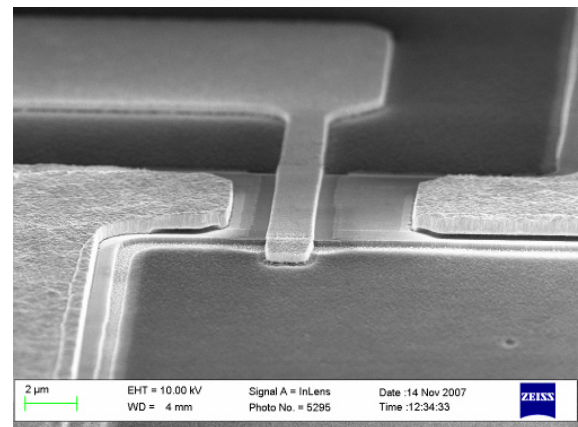
In order to boost the speed of p-channel InGaAs FETs, we are studying the possibility of enhancing the hole mobility through the application of mechanical strain to the channel. Strain-induced enhancements have been used in Si and Ge devices for some time. Compared with their unstrained counterparts, strained Ge and Si showed 6× and 2× higher hole motilities, respectively [2, 3]. Theoretical studies have shown that in Si, Ge and compound semiconductors such as InGaAs, strain can split the heavy-hole and light-hole valence bands, which are degenerate at the Γ -point in the unstrained semiconductor. This can lead to preferential occupation of holes into the lighter band, so that the conductivity effective mass of the holes decreases. What is more, strain can also reduce the density-of-states (DOS) ef-

fective mass of holes. In Figure 1, the change of DOS effective mass due to strain is calculated by the 8x8 k.p method for both Ge and InGaAs. It can be seen that the effect in InGaAs follows a trend similar to that of Ge. It is therefore reasonable to expect a sizable improvement in the hole mobility in InGaAs through the application of mechanical strain.

To experimentally verify the potential enhancement, we are exploring two threads. Along the first thread, a chip-bending apparatus has been fabricated. This apparatus has four ridges whose vertical and horizontal positions are controlled by micrometers. By manipulating the micrometers, we can use the ridges to apply either tensile or compressive uniaxial strain on an InGaAs chip down to the size of 4mm×4mm. At the same time, we can conduct electrical measurements on the strained devices. Our second thread is to fabricate p-channel InGaAs high-electron-mobility transistors. In these devices, spatial separation between dopants and a two-dimensional hole gas results in reduced ionized impurity scattering and high mobility. Figure 2 shows an example of a fabricated device. By combining the two threads, we hope to provide understanding of the speed-enhancing effects of strain in p-channel InGaAs FETs.



▲ Figure 1: The density-of-states effective mass of Ge and InGaAs under different amount of compressive (-) and tensile (+) strain.



▲ Figure 2: An SEM image of a fabricated InGaAs FET.

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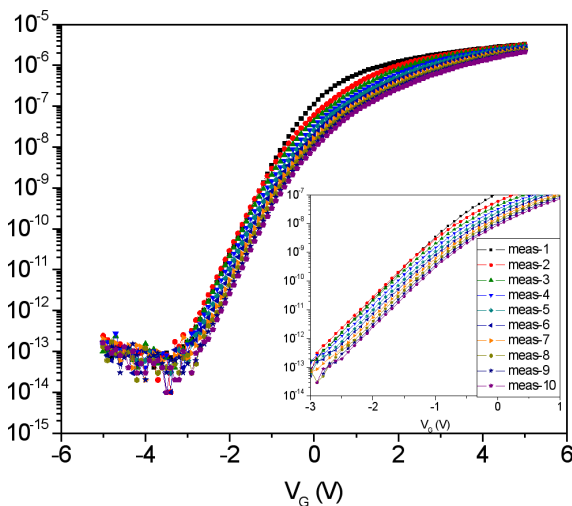
Stability of Metal Oxide-based Field-effect Transistors

B. Yaglioglu, A. Wang, K. Ryu, H. Tang, C.G. Sodini, A.I. Akinwande, V. Bulović
Sponsorship: Hewlett-Packard, DARPA

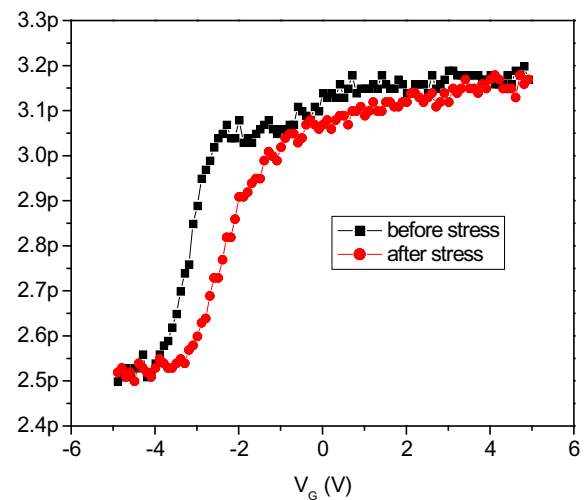
Over the last few years, there has been a considerable effort to understand the behavior of metal-oxide-channel field-effect transistors (FETs) in order to produce devices for low-cost, large-area electronic applications [1-3]. Field-effect mobility, sub-threshold slope, and threshold voltage of FETs are the main parameters that need to be characterized to design circuits made of amorphous oxide semiconductors. Just as important as these characteristics is the endurance of FETs over repeated switching cycles, which determines the reliability of the transistors.

In this study we test the stability of FETs that have a polymer dielectric, parylene, and an oxide semiconductor ($\text{ZnO}:\text{In}_2\text{O}_3$). The devices are processed lithographically at low temperatures ($T \leq 100$ °C). Figure 1 shows transfer characteristics that are obtained

by repetition of current-voltage (I-V) sweeps under a gate bias between measurements. Preliminary results of I-V tests along with capacitance-voltage (C-V) measurements (see Figure 2) show a positive shift in the threshold voltage. Two possible mechanisms that are originally proposed for similar shifts in amorphous Si FET's are metastable state generation in the semiconductor and charge trapping in the dielectric [4]. Operation of stability experiments at different temperatures and bias gate voltages are conducted to elucidate the instability mechanisms in these hybrid (inorganic/organic) devices. The outcome of these experiments will provide a path for increasing the performance and lifetime of transistors based on oxide semiconductors.



▲ Figure 1: Transfer characteristics of a transistor under a bias stress, $V_{GS} = 10\text{V}$ and $V_{DS} = 0\text{V}$, between measurements (stress time = 20s). Data are taken from -5V to 5V with 0.1V steps while $V_{DS} = 1\text{V}$. The sub-threshold regime of curves is enlarged in the inset.



▲ Figure 2: Quasi-static C-V measurements collected from the same device before and after bias stress test.

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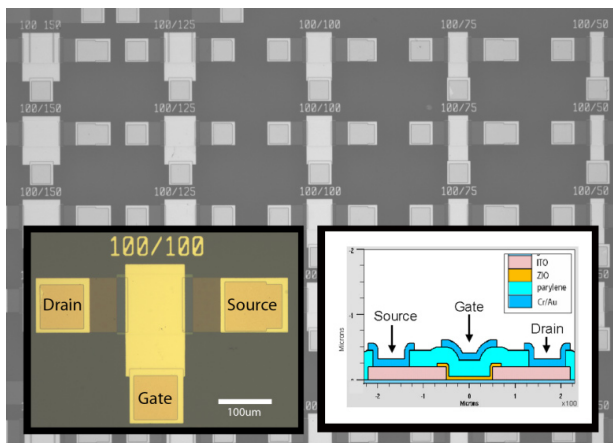
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Lithographically Patterned Metal Oxide Transistors for Large-area Electronics

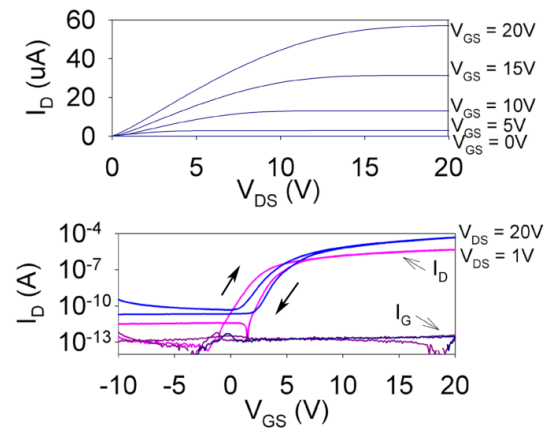
A. Wang, B. Yaglioglu, H. Tang, C.G. Sodini, V. Bulović, A.I. Akinwande
Sponsorship: Hewlett-Packard, DARPA

Recently, sputtered metal-oxide-based field-effect transistors (FETs) have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1-3]. Because the optically transparent semiconducting oxide films can be deposited at near-room temperatures, these materials are compatible with future generations of large-area electronics technologies that require flexible substrates [4]. It is possible to process FETs by shadow-mask patterning, but this method limits the range of feature sizes, accuracy of pattern alignment, and scalability of the process to large substrates. Consequently, our project aims to develop a low-temperature, lithographic process for metal oxide-based FETs that can be integrated into large-area electronic circuits.

We have fabricated top-gate, fully lithographic FETs of varying channel lengths on 100-mm glass wafers with a sputtered ZnO:In₂O₃ channel layer, using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts. All layers were subtractively patterned by a combination of dry- and wet-etch processes. Figure 1 shows a micrograph of several completed FETs. Current-voltage characteristics for a single device (pictured in inset of Figure 1) appear in Figure 2. From the current-voltage and capacitance-voltage curves, device- and circuit parameters such as threshold voltage, subthreshold slope, gate leakage, and channel capacitance can be extracted and also used to monitor the reproducibility of our process. These measurements are used as a guide to determine processing conditions for the fabrication of oxide-based field-effect transistors and circuits.



▲ Figure 1: Micrograph of fabricated array of single devices with varying channel lengths. The left inset gives a larger view of a single field effect transistor ($W/L = 100\mu\text{m} / 100\mu\text{m}$). The right inset shows a schematic cross-section of the device.



▲ Figure 2: Electrical characteristics of lithographically patterned FET ($W/L = 100\mu\text{m} / 100\mu\text{m}$). Output curves are plotted in the top graph; double-swept transfer curves taken in saturation and triode regions are plotted on the bottom. As the bottom graph shows, gate leakage current through the parylene dielectric is low.

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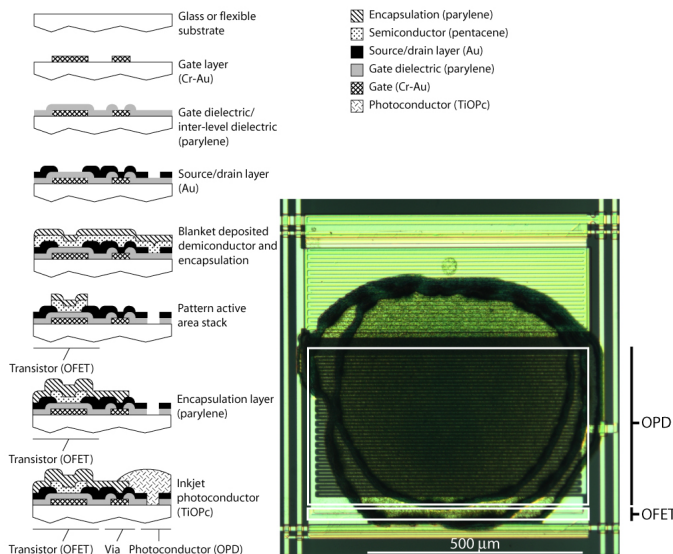
Engineering the Flatband Voltage in Organic Field-effect Transistors for Enhancement-depletion Mode Logic

I. Nausieda, D. He, K. Ryu, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

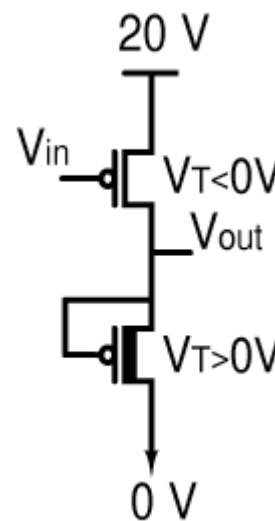
Organic semiconductors could enable large-area, mechanically flexible electronic systems such as e-paper, large-area imagers, and rollable displays due to their low processing temperatures and suitable electronic properties. We have developed a near-room-temperature ($\leq 95^\circ\text{C}$), scalable process to fabricate integrated organic field-effect transistors (OFETs) [1].

The OFET's semiconducting layer is a thin (15-nm) film of pentacene - chosen for its air-stability and high hole mobility ($\approx 1\text{ cm}^2/\text{Vs}$) [2]. Since there exists no air-stable, electron-transporting organic semiconductor with comparable mobility, our process produces p-channel transistors only. The nominal process pictured in Figure 1 yields enhancement-mode OFETs with threshold voltages of -1V .

The goal of this project is to achieve enhancement and depletion mode devices on a single substrate. The OFET flatband voltage, nominally the difference between the gate and semiconductor work functions, may be shifted by changing the gate metal work function. With the use of two gate metals, enhancement and depletion mode devices can be obtained. Such a process would enable the creation of high-noise margin inverters, robust to process variation (see Figure 2). Connecting the gate to the source permits use of the depletion-mode transistors as current sources, making possible a variety of analog circuits such as high-gain amplifiers and comparators.



▲ Figure 1: Integrated process for OFETs and organic photoconductors (OPDs) developed at MIT.



▲ Figure 2: Inverter/common-source amplifier with enhancement-mode driver and depletion-mode load.

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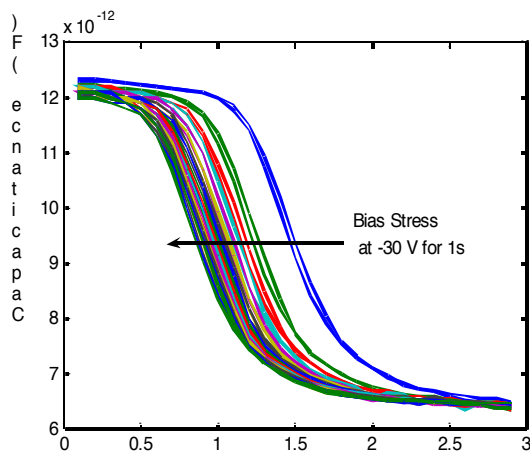
Bias-induced Instability in Pentacene and Zinc Oxide Thin-film Transistors

K. Ryu, D. He, I. Nausieda, A. Wang, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

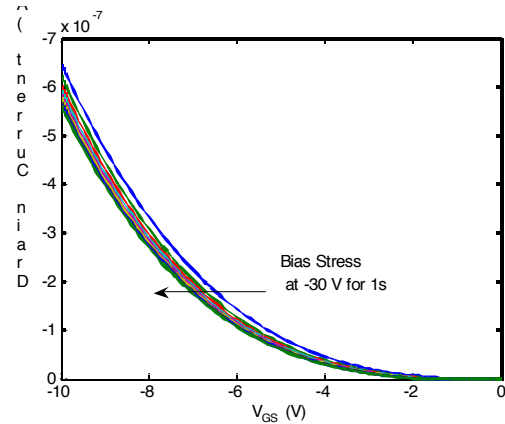
Thin-film transistors (TFTs) are a type of field-effect transistor made by depositing a thin film of semiconductor as the active layer over a substrate that provides mechanical support. This thin semiconductor layer is polycrystalline or amorphous, which results in trap states in the bandgap and therefore exhibits poorer carrier mobility than single crystal films. However, TFTs can enable large-area electronics because they are not limited by the substrate materials. The TFTs based on semiconducting organic small molecules (e.g., pentacene) and metal oxides (e.g., zinc oxide) offer near-room-temperature processing, which makes them compatible with lightweight, flexible plastic substrates. These new devices have been employed to make paper-like flexible displays that are commercially available. Although TFTs' primary function has been limited to the switching elements in displays, there is significant interest in expanding their function to integrate new digital and analog circuit blocks such as display decoders, multiplexers, and OLED drivers. Operational sta-

bility is required for these new applications, but both organic TFTs and metal oxide TFTs have been reported to have bias-stress stability problems. Figures 1 and 2 show that for gate bias stress of -30V for ten seconds, the flatband voltage shifts 0.6 V.

The goal of this work is to investigate the mechanisms that cause bias-induced instability in pentacene and zinc oxide transistors and use the knowledge to develop a method of quenching bias-instability for thin-film transistors at low processing temperatures. The work involves physical modeling of I-V, and C-V characteristics of TFTs to identify the changing physical parameters. Electrical characterization methods such as $1/f$ noise, I-V, and C-V measurements will be employed to determine the mechanisms that cause bias instability.



▲ Figure 1: A C-V graph of a pentacene TFT (1000/25 μm), which shows V_{FB} shift as the bias-stress is applied.



▲ Figure 2: An I-V graph of a pentacene TFT (1000/25 μm), which shows V_{FB} shift as the bias-stress is applied.

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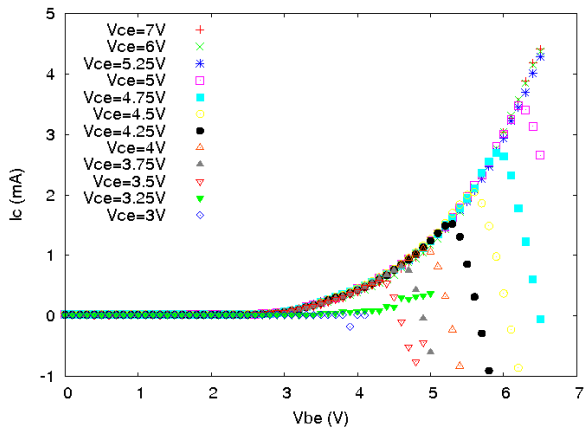
Fabrication of the Ferromagnetic Kisaki Transistor

M. van Veenhuizen, J. Chang, J.S. Moodera
Sponsorship: DARPA, KIST-MIT project

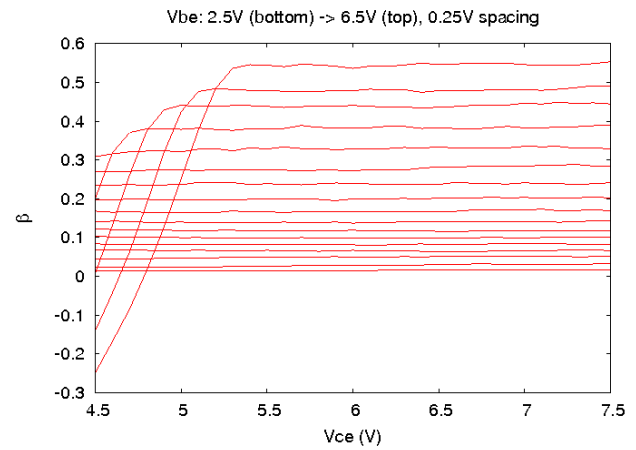
The research field of spintronics, which aims at creating electronic devices based on the spin quantum number of the charge carriers, has seen a major advancement since its invention two decades ago, culminating in this year's Nobel Prize for the GMR spin-valve. The current emphasis is on semiconductor spintronics, which, owing to the long spin-coherence lengths as well as engineering feasibility, is promising for new or better device technology. Conventional sources of spin-polarization are the 3-d ferromagnets whose high Curie temperatures as well as ease of fabrication make them a logical choice as sources of spin-current into semiconductors. However, the incorporation of ferromagnetic metals with semiconductors is hampered by the conductivity mismatch that hinders efficient spin-injection[1], and also by Schottky-barrier formation.

This project aims at realizing efficient spin-injection into silicon. Silicon has a very long spin-coherence length [2] and is therefore especially suitable for spintronics applications. The electrical spin-injection is achieved by means of a ferromagnetic Kisaki transistor [3], a scheme that overcomes both the conductivity mismatch as well as Schottky barrier formation. The Kisaki transistor is a bipolar transistor with the n-type emitter being a metal, separated from the p-type base by a tunnel junction. Figures 1 and 2 demonstrate the transistor action for an early version of the transistor. The current emphasis is on improving the device performance.

We gratefully thank Siltronic for the generous donation of silicon wafers.



▲ Figure 1: Emitter current as a function of base-emitter voltage for different values of collector-emitter voltages.



▲ Figure 2: Current ratio as a function of collector-emitter voltage for different values of base-emitter voltages.

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Spin-dependent Photocurrent Transport in GaAs/MgO/Fe Structure

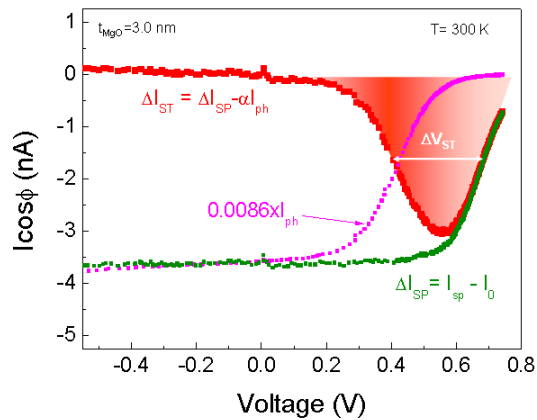
Y.J. Park, M. van Veenhuizen, D. Heiman, C.H. Perry, J.S. Moodera
Sponsorship: KIST-MIT project

Our approach employs MgO/Fe as a spin injector/detector on a GaAs semiconductor. To understand the spin filtering effect of this GaAs/MgO/Fe structure, we used the measurement technique of spin-dependent photo-current (SDPC)[1] to create a spin-imbalance in the GaAs by optical means that is subsequently detected electrically through the MgO/Fe structure. The growth of 2-4 nm MgO/7 nm Fe/4 nm Au layers on n+(001) GaAs substrates was performed in a molecular beam epitaxy (MBE) system with a base pressure $\sim 2 \times 10^{-10}$ torr. The layers were deposited at room temperature with typical deposition rates of 0.01-0.02 nm/s. Post-annealing was conducted in the growth chamber under UHV conditions.

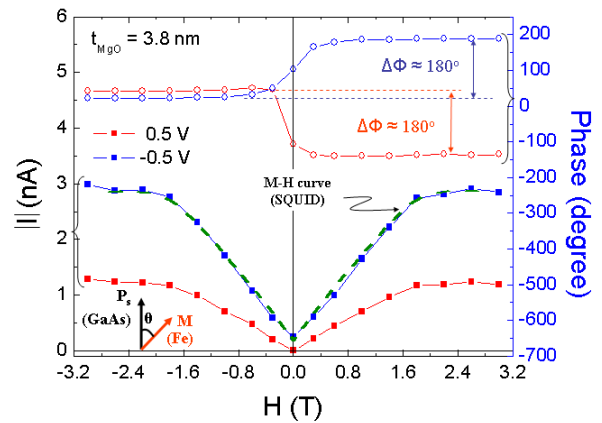
Figure 1 shows one of the results, the bias dependent in-phase component of photocurrent. Here, ΔI_{ST} represents the spin-transferred photocurrent, which is defined by $\Delta I_{ST} = \Delta I_{SP} - \alpha I_{ph}$, where ΔI_{SP} is a net spin-dependent photocurrent and αI_{ph} is a magneto-optical background, such as MCD (magnetic circular dichroism), contribution. The MCD fit parameter, α , is estimated to be 0.0086, as Figure 1 shows. The I_{ph} represents unpolarized light-induced total photocurrent. The net SDPC, ΔI_{SP} , is obtained by subtracting the zero field photocurrent I_0 . A simple manipulation of the measured photocur-

rents leads to a clear spin current transferred region (shaded area in Figure 1) at $0.2V \leq V \leq 0.75V$, which is much broader (i.e., $\Delta V_{ST} \sim 0.3V$, determined by full width at half maximum of bias dependent spin transferred photocurrent) than those of Schottky barrier ($\sim 0.08V$)[2] and AlGaAs barrier cases ($\sim 0.1V$)[3]. This is closely related to the carrier transport processes associated with MgO tunnel barrier.

Figure 2 shows the photocurrent amplitude and phase as a function of applied magnetic field. The M-H curve of the Fe layer is in good agreement with the photocurrent. This finding indicates that the SDPC varies with the P_s (spin polarization of photo-excited carriers in the GaAs) and M (magnetization of Fe layer). Also shown is the phase dependence of the photocurrent: a clear phase shift of approximately 180° depending on the bias can be observed as the magnetic field sweeps from minus to plus. Finally, the GaAs/MgO/Fe structure unambiguously showed a spin-filtering effect, which is useful for the device application.



▲ Figure 1: Spin-dependent photocurrent measured at 300K. The shaded area represents the spin-filtered photocurrent region. The MCD fit parameter α was estimated to be 0.0086.



▲ Figure 2: Magnetic field-dependence of spin-dependent photocurrent (left axis) and phase change (right axis). The dotted line is the M-H curve obtained from SQUID measurement. Bottom left inset shows the definition of angle θ between P_s and M .

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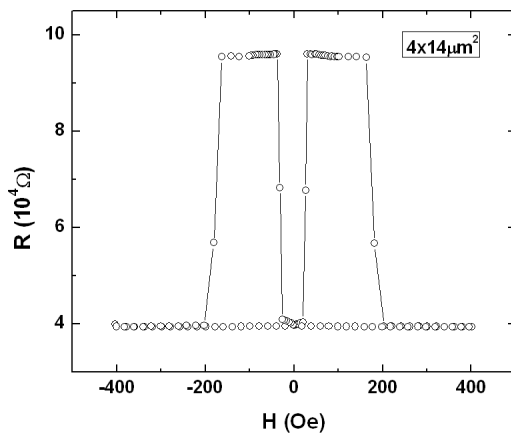
Spin Torque Transfer Study in Fully Epitaxial Fe/MgO/Fe MTJs for MRAM Applications

G.X. Miao, J.S. Moodera

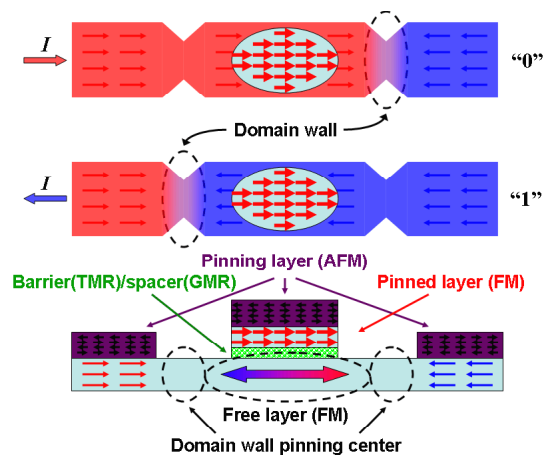
Sponsorship: NSF, ONR, KIST-MIT project

Magnetic Random Access Memory (MRAM) is the new generation of universal memory unit, and it has all the advantages of high density, high speed, non-volatility, and high endurance for harsh environments. The newly discovered memory “writing” mechanism based on spin transfer torque (STT) [1] has shown promise to further increase memory density. In our lab, we use a UHV MBE system to deposit the fully epitaxial Fe/MgO/Fe magnetic tunnel junction (MTJ) stacks on top of etched Si (100), and we use the MTL facilities for the micro-fabrications. Due to the presence of coherent tunneling in such epitaxial systems [2] (i.e., the tunneling electrons conserve both their spins and the angular momentum), a giant TMR of 150% has been achieved at room temperature (see Figure 1).

In order to bypass the large current density required for an STT-based switching mechanism, we fabricate the domain wall storage unit as illustrated in Figure 2. The writing current now flows completely inside the free layer and the spin transfer torque from this current can toggle the domain wall between the “left” and the “right” pinning positions when the current is flowing towards left, or right, respectively, thus enabling the writing of the “0” and “1” memory states. This novel writing technique can dramatically reduce the probability of tunnel barrier breakdown and increase the durability of the device.



▲ Figure 1: An example of Fe/MgO/Fe-based MTJ at RT. The top Fe layer is magnetically hardened with Co in order to achieve the desired magnetic separation.



▲ Figure 2: The domain wall position can be toggled between the pinning centers, by alternating the driving current direction, and the TMR stack on top will read the memory state of the unit. The free layer is one electrode of the MTJ.

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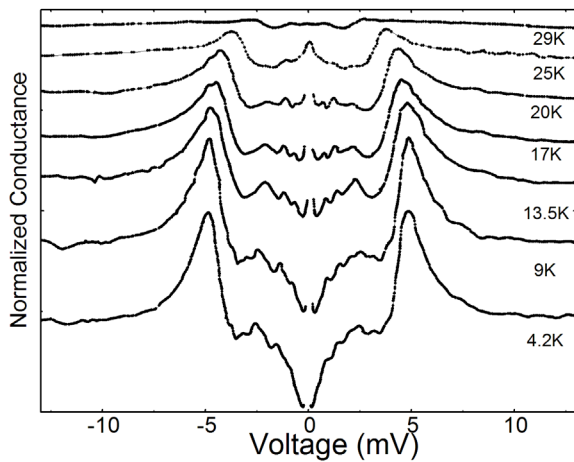
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Development of MgB₂ Superconductor-based Electronics: Basic and Device Studies

M.V. Costache, G. Miao, J.S. Moodera
Sponsorship: ONR

Magnesium diboride (MgB₂), a material known since the 1950s, was recently discovered to be superconductor at a remarkably high critical temperature $T_c = 40$ K for a binary compound, its high T_c , simple crystal structure, large coherence lengths, and high critical current densities and fields indicate that MgB₂ has potential for superconducting devices that operate at 20-30 K, the temperature reached by current commercial cryocoolers. Furthermore, the larger superconducting gap allows for higher operating speeds (up to 3.5 THz) than Nb-based junctions.

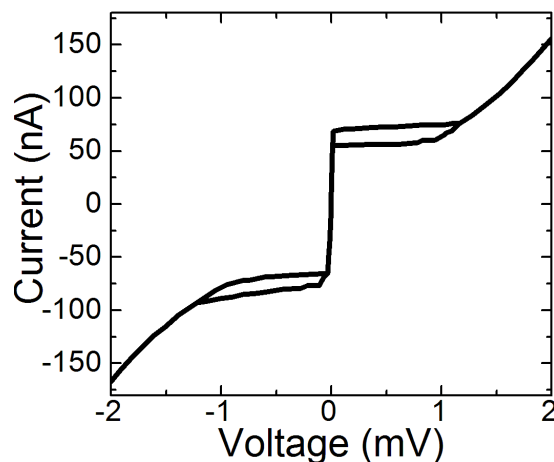
The goal of the project is to growth epitaxial superconducting MgB₂ thin films by molecular beam epitaxy (MBE) suitable for fabrication of all-MgB₂ Josephson junctions. Using MBE technique we have fabricated MgB₂/I/MgB₂ tunnel junctions [1, 2] where the tunnel barrier (I) is natural (by oxidation of base electrode) or artificial (e.g., Al₂O₃, MgO and AlN).



▲ Figure 1: Normalized conductance vs. voltage at selected temperatures for a MgB₂/natural oxide/MgB₂ junction.

Figure 1 shows the conductance vs. voltage at selected temperatures for a MgB₂/native oxide/MgB₂ tunnel junction defined using shadow mask techniques. In spite of the presence of superconducting energy gaps to over 30 K, the junction exhibited sub-gap characteristics and no supercurrent was observed. Furthermore, we have fabricated MgB₂/MgO/MgB₂ tunnel junctions using photolithography and etching techniques. As expected, the dc Josephson effect was observed for this junctions, as Figure 2 shows. For the fabrication of all-MgB₂ Josephson junctions-based devices, our results demonstrate that the junction oxidation process is less reliable in contrast to growing an artificial barrier.

We acknowledge the Office of Naval Research for providing financial support.



▲ Figure 2: The I-V characteristics for a MgB₂/MgO/MgB₂ junction, showing dc Josephson effect.

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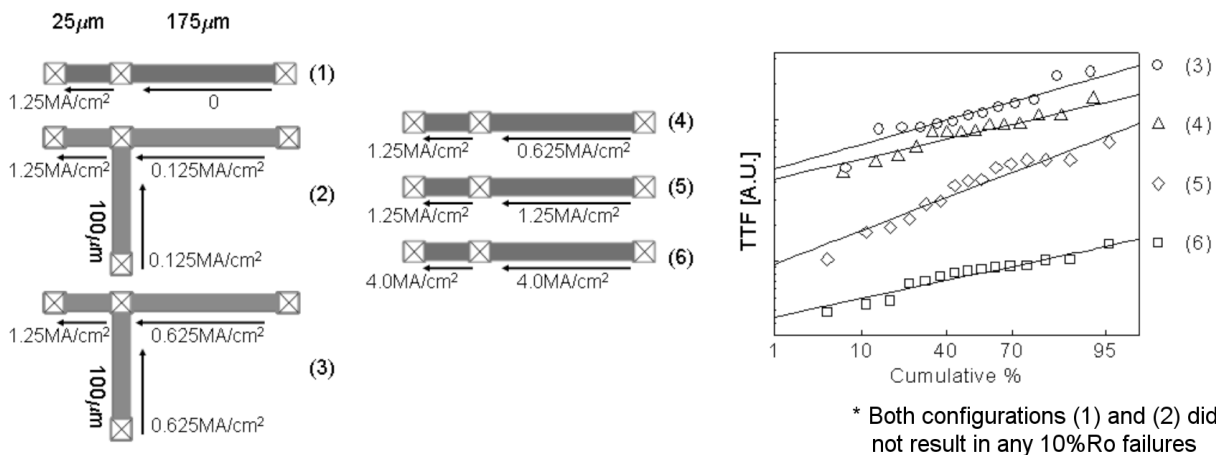
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Effects of Active Atomic Sinks and Reservoirs on the Reliability of Cu/low-*k* Interconnects

F.L. Wei, C.S. Hau-Riege (AMD), A.P. Marathe (AMD), T.J. Park, T. Chookajorn, C.V. Thompson
Sponsorship: Intel, AMD, Texas Instruments, SRC

Electromigration experiments using Cu/low-*k* interconnect tree structures (as in Figure 1) were carried out in order to study the effects of active atomic sinks and reservoirs on interconnect reliability. In all cases, failures occurred after a long period of void growth. Kinetic parameters were extracted from resistance versus time data, giving $(Dz^*)_{o,eff} = 3.9 \times 10^{-10} \text{ m}^2/\text{s}$ and $z^* = 0.40 \pm 0.12$. Using these values, the evolution of stress in each of the interconnect tree segments could be calculated and correlated with the rate of void growth and failure times for all test configurations. It is demonstrated that segments that serve as atomic sinks and reservoirs for the failing segments affect the lifetime by modifying the con-

ditions for stress-induced migration. Reservoirs can lead to increased lifetimes, while sinks can lead to reduced lifetimes. We made quantitative predictions of the times required for failure for Cu/low-*k* interconnect trees as a function of the effective bulk elastic modulus of the interconnect system, *B*. As the Young's modulus of the inter-level dielectric (ILD) films decreases, *B* decreases; further, the positive effects of reservoirs are diminished and the negative effects of sinks are amplified [1].



▲ Figure 1: Simple multi-segment interconnect trees were tested with different currents in each segment. In the case shown above, tests were carried out to determine effects of both active (with current) and inactive (without current) segments serving as atomic reservoirs for the short segment. The arrows indicate the direction of electron transport. Both active and inactive reservoirs lead to improved reliability. Interconnect trees were also tested with long segments serving as atomic sinks for short test segments. These atomic sinks led to a degradation in reliability.

Reference

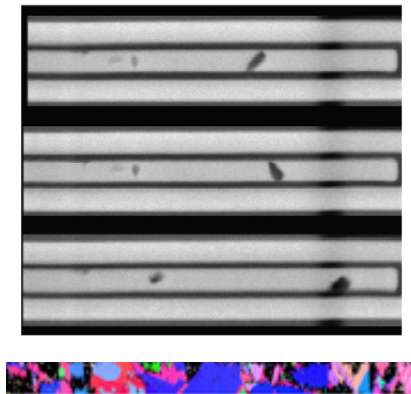
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Surface Electromigration, Void Dynamics, and the Reliability of IC Interconnects

Z.-S. Choi, R. Monig, T. Chookajorn, T.J. Park, C.V. Thompson
Sponsorship: Intel, AMD, SRC

Electromigration is atomic diffusion due to a momentum transfer from conducting electrons. Electromigration of metallic IC interconnects is and will remain a major reliability concern as future technologies demand increasing device and wire densities as well as higher current densities. In Cu-based metallization, electromigration occurs by diffusion of Cu at the interface between polycrystalline Cu and the dielectric overlayer, and it leads to formation of voids that cause an increase in resistance and to failure. The rate of failure is therefore highly dependent on the Cu atomic diffusivity, which is affected by the grain structure of the Cu, as well as the stress conditions.

In situ scanning electron microscope observations have been performed on passivated Cu interconnects of different widths during accelerated electromigration tests. In some cases, voids form and grow at the cathode. However, an alternative failure mode is also observed, during which voids form distant from the cathode and drift toward the cathode, where they eventually lead to failure. The number of observations of this failure mode increased with increasing line width. During void motion, the shape and the velocity of the drifting voids varied significantly. Postmortem electron backscattered diffraction (EBSD) analysis was performed (see Figure 1), and a correlation of EBSD data with the *in situ* observations reveals

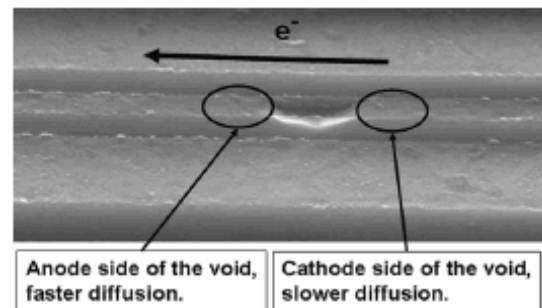


▲ Figure 1: *In situ* SEM images of the cathode of a test structure, showing void drift toward cathode end. The test line is surrounded by a Cu-extrusion monitor. Bottom image is a texture mapping by EBSD obtained after EM test.

that locations of voids, their shape evolution, and their motion all strongly depend on the locations of grain boundaries and the crystallographic orientations of neighboring grains. [1]

A separate experiment determined surface electromigration rates on oxide-free surfaces of unpassivated damascene Cu interconnect segments through electromigration testing under vacuum. Electromigration-induced voids grew at the cathode end of the segments due to a flux divergence at refractory-metal-lined vias to the lead lines below the test segment. Diffusivity on a clean Cu surface was determined by measuring the size of the voids as a function of time and test temperature at a fixed current. An activation energy of 0.45 ± 0.11 eV and a pre-factor of 3.35×10^{-12} m²/s were found for the product of the effective charge z^* and the surface diffusivity D_s [2]. Through correlations of void growth rates with the crystallographic textures of adjacent grains (Figure 2), relative surface diffusivities for grains with different crystallographic orientations have been determined [3].

Data acquired in the experiments described above are being used in simulations of electromigration-induced failure, to develop improved methods for reliability projections based on accelerated electromigration tests.



▲ Figure 2: EBSD has been used to determine the crystallographic orientations of grains adjacent to voids. Correlation with void growth rates allows determination of relative values of the surface diffusivity.

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Grain Structure and Residual Stress in Polycrystalline Metallic Films

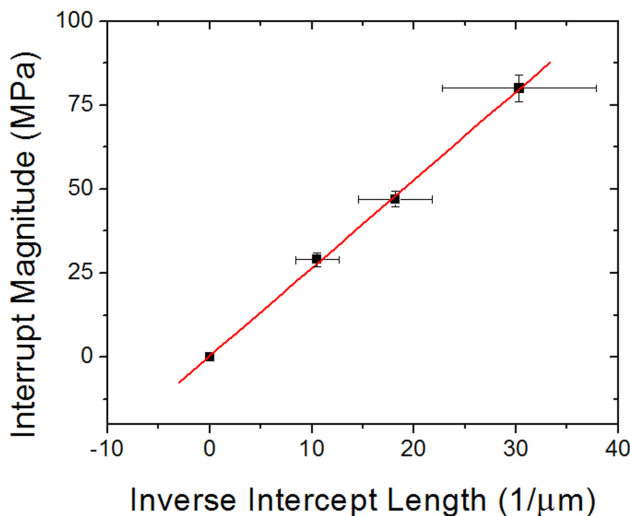
J. Leib, C.V. Thompson
Sponsorship: NSF

In thin metal films deposited for various applications, there are obvious advantages to both understanding and controlling the intrinsic stresses in the films as-deposited. For high-mobility metal films (e.g., Au, Ag, Al, Cu) deposited on amorphous substrates, much of the observed stress can be attributed to the grain structure that evolves as the Volmer-Weber film transitions from individual islands to a continuous film. The stress behavior during this process shifts from tensile (during island coalescence) to compressive (as the film grows past continuity). Initially, the grain size of the continuous film is equal to the island size at coalescence.

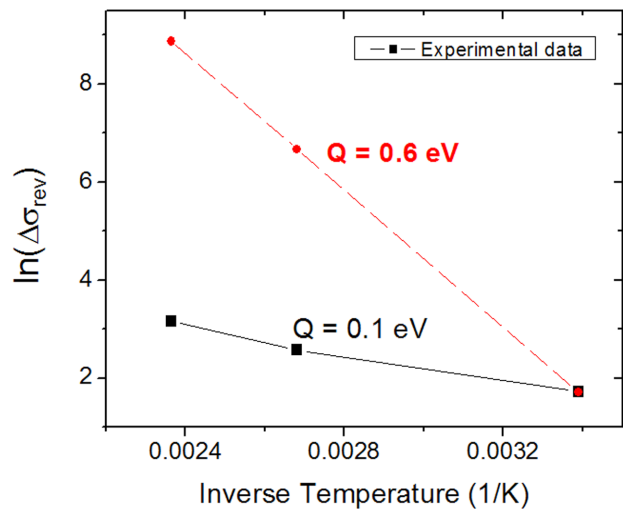
The role of grain boundaries in the post-coalescence compressive stress has been debated extensively in the literature [1-4], but no experimental research has been performed to quantify the relationship between grain size and stress in polycrystalline films. In-situ stress monitoring and transmission electron microscopy (TEM) have been used to investigate stress and grain size in gold films deposited on silicon nitride. When films were treated to different grain

sizes, stress-measured, and then imaged in TEM, the inverse of grain size and corresponding tensile rise was found to be linear, with zero stress at infinite grain size. This relationship indicates that grain boundaries are critical to the formation of compressive stress in these films, with the stress proportional to the grain boundary perimeter line length per area of film (see Figure 1).

While this result supports a model for compressive stress arising from trapping of an excess population of self-interstitials at grain boundaries (as in reference [3]), the expected relaxation of these defects would be their diffusion back to the surface and attachment to surface steps. However, the thermal activation for grain boundary diffusion (~0.6 eV) was not observed in the corresponding stress relaxation (see Figure 2). Current investigations focus on identification of mechanisms consistent with the observed small activation energy (~0.1eV).



▲ Figure 1: Stress as a function of inverse grain size. As the grain size increases, the stress trends towards zero.



▲ Figure 2: Activation plot of log stress as a function of inverse temperature. The black line shows experimental data, while the red line shows the expected trend for self-interstitial grain boundary diffusion in gold. The difference at the highest temperature is more than two orders of magnitude.

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12-Watt Thermoelectric Generator Powered by Combustion

P. Santhanam, R.J. Ram

Sponsorship: ONR Thermo-Electric Conversion MURI Program

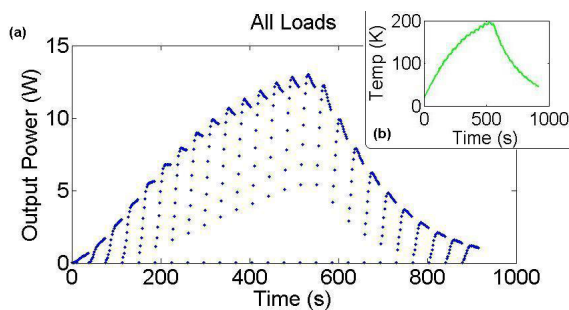
As part of a recent effort to demonstrate the capability of newly-developed thin-film thermoelectric (TE) materials to generate macroscopic quantities of electrical power, we have constructed a 12-watt TE generator.

Both the efficiency of TE generators and the coefficient of performance for TE coolers are closely tied to a quantity Z , which depends on the material's Seebeck coefficient (S), electrical conductivity (σ), and thermal conductivity ($\kappa = \kappa_e + \kappa_{ph} \approx \kappa_{ph}$). For this reason, when evaluating TE materials it is common to define the figure-of-merit ZT , where T is the absolute temperature, as $ZT = (S^2\sigma/\kappa)T$. Despite much initial excitement over the potential for semiconductors in the field during the 1950s, the limited application of thermoelectricity has been due in great part to the decades-long stagnation of the maximum achievable room-temperature ZT (~ 1 for Bi_2Te_3) [1]. Recently, however, new nanostructured materials have shown promise to break this trend [2, 3], and there is strong evidence that the gains thus far are due to a reduction in phonon-dominated thermal conductivity [4].

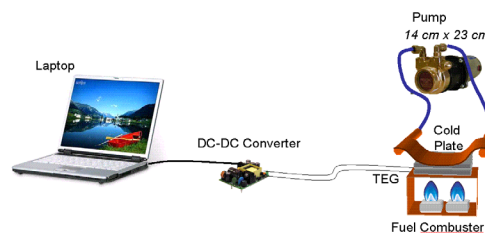
In the past five years, our MURI collaboration has developed a superlattice material formed with layers of InGaAs doped with Er beyond the solubility limit interleaved with undoped InGaAs. The material's doped layers contain amorphous ErAs islands that scatter short-wavelength phonons, while the superlattice structure scatters long-wavelength phonons. Together, these properties impede the phonon thermal transport, substantially decreasing the overall thermal transport and increasing the material's ZT .

While an increased ZT in theory implies electrical power generation efficiency, numerous system-level challenges become more prominent for thin-film materials being used in macroscopic generators. For instance, due to geometry alone, for a given thermal power flux, thin-film materials will see substantially smaller temperature drops from hot-side to cold than will their thicker bulk counterparts. On a system level, it is also possible for interfacial thermal impedances elsewhere in the generator to dominate the TE material in the overall thermal impedance of the generator, causing reduction of the thermal power flow between a given pair of fixed-temperature reservoirs. Together these issues can substantially reduce the temperature drop across the TE module itself and, since the generated electrical power is proportional to the square of the temperature drop, the overall power output as well.

In order to mitigate these concerns, we have chosen to first demonstrate thin-film thermoelectrics within a module that also contains a traditional bulk TE material. Our initial generator designs have implemented a commercial bulk TE module, which we have used to produce upwards of 12 W of DC electrical power (Figure 1a) due to a temperature drop of around 200K (Figure 1b). Our intentions are to replace this commercial bulk module with a segmented thin-film and bulk module, and use the generator to drive a low-power computer (Figure 2).



▲ Figure 1a: Electrical power output as a function of time. The peaks of the oscillations represent the impedance-matching condition for maximum power. The peak observed value is 12.99W. Figure 1b: Temperature difference across the module with time. Electrical power is proportional to the square of this temperature difference.



▲ Figure 2: Schematic for final demonstration system, set to include a module containing both thin-film and bulk TE materials.

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Bonded-wafer Process for Optimized InP Avalanche Photodetectors

H. Li, D. Oakley, J. Donnelly, V. Diadiuk, S. Groves

Fabrication of low-dark-count, low-after-pulsing InP avalanche photodetectors (APD) may require a “n-on-p” epilayer structure, whereas the crystal growth requirements favor a “p-on-n” sequence. The primary limitation in crystal growth is related to diffusion of the p-type dopant (Zn) that is normally used in organometallic vapor phase epitaxy (OMVPE).

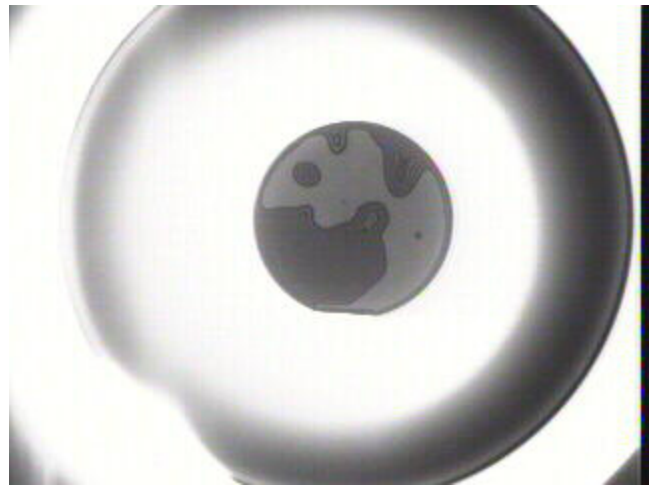
A possible way to overcome these limitations and achieve optimum conditions for both crystal growth and device structure capitalizes on MTL’s extensive wafer bonding experience. The basic concept consists of growing the preferred InP epilayer structure (p-on-n) and then bonding the top layer of that wafer to a virgin InP wafer (the “handle wafer”), which becomes the new device substrate. After bonding, the original InP substrate is ground off by chemo-mechanical polishing (CMP) or wet-etched away and the APDs are fabricated on the composite wafer (which contains the transferred epilayers).

Preliminary experiments yielded bonded-wafer InP APDs that showed dark count rates (DCR) comparable to standard APDs, indicating that the bonding step does not damage the epi-layers or p-n junction; in addition, the bonded-wafer InP APDs, which have minimum Zn diffusion, are likely to exhibit reduced after-pulsing. Recently, epi-wafers that had substantially fewer particles on the surface were successfully bonded to virgin InP wafers without CMP, in spite of a few surface inclusions and non-uniformities. This is an important step forward, since InP is very fragile and easily damaged. Figure 1 shows an infra-red image of the two wafers in contact but not bonded; Figure 2 shows this bonded-pair after annealing at 300 °C for 3 hours; diffraction rings show where the surface is NOT bonded. There are many large well-bonded areas suitable for detector fabrication.

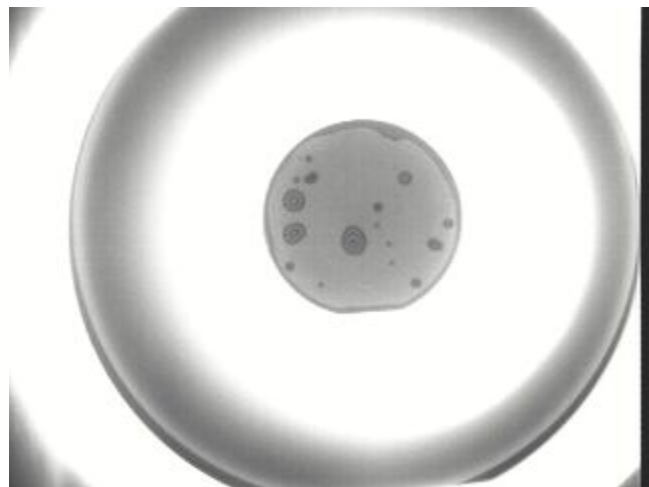
Wet etching in HCl, rather than grinding, was successful for removing the original substrate. Given the presence of the InGaAs layer, which serves as an etch stop, wet etching is very effective and it increases process robustness and reproducibility. APDs have been fabricated and measurement of DCR and after-pulsing show that there is no degradation in the device performance due to either the bonding step or substrate removal. Epi wafers with better surfaces and different epi-layer composition will be grown to optimize detector performance.

Future plans include replacing the InP handle wafer with a GaP wafer in which a lenslet array has been fabricated. This would provide several fabrication and device performance advantages such as elimination of the air gap between the detector and lenslet arrays, wafer-level alignment of detector and lenslet arrays, and increased detection efficiency.

This work is supported by a grant from the Lincoln Laboratory Advanced Concepts Committee.



▲ Figure 1: An infra-red image of InP wafer 377-A, in contact with a new InP substrate; large dark areas indicate gaps between the 2 surfaces.



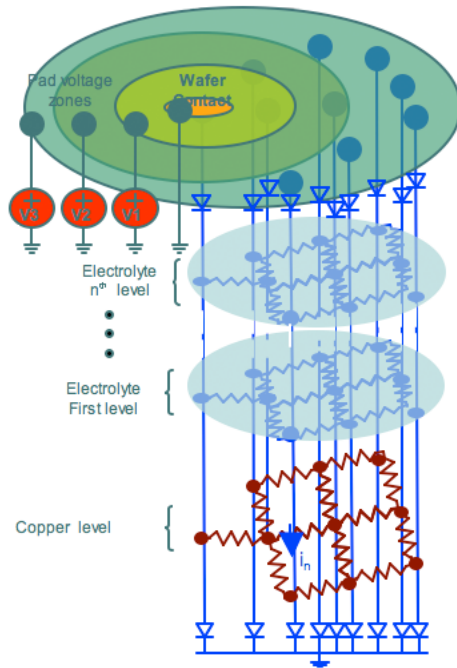
▲ Figure 2: An infra-red image of bonded-pair 377-A, annealed at 300 °C for 3 hrs; diffraction rings show where the surface is NOT bonded.

Modeling of Electrochemical-mechanical Planarization (eCMP)

J. Johnson, W. Fan, Z. Li, D.S. Boning

Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

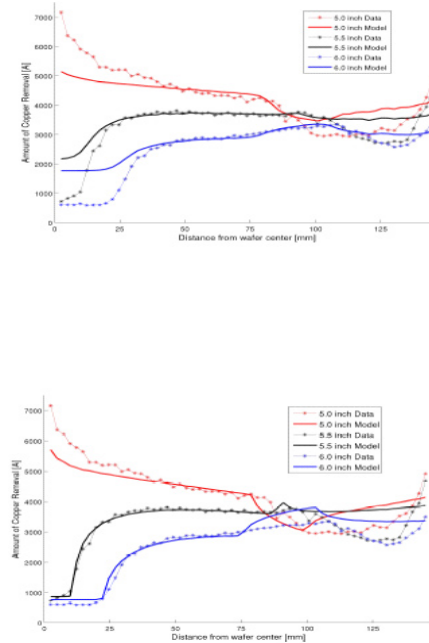
The process of electrochemical-mechanical polishing (eCMP) is well established for the removal of bulk copper. In previous work, a wafer-level physically-based eCMP model accounting for time-averaged current-density distributions across a wafer due to multiple cathodic voltage zones was proposed. An extension of this purely ohmic model to a non-ohmic model accounting for the exponential dependence of current on overpotential at the electrode/electrolyte interface has been developed. As Figure 2 shows, the model captures the nonlinear dependence of removal rate on applied voltage in different voltage zones across the wafer. We are seeking to extend and complete this non-ohmic model to account for the electrochemical reactions occurring at both the anode (wafer) and cathode as well as the lateral coupling/current contributions. Figure 1 shows the new extended model, which accounts for the electrical current



▲ Figure 1: Modified wafer-level modeling approach for eCMP, accounting for the distribution of current at the wafer and platen electrodes and through the electrolyte.

distributions on the wafer surface and in the electrolyte, yielding the copper removal rate at each location on the wafer. We are also examining the effects of passivation layer formation and removal on the time-averaged voltage.

This enhanced eCMP model will attempt to adequately characterize the full removal of copper physically and electrochemically, in hopes of optimizing the process to remove the entire copper layer as well as the barrier metal, reducing the need for traditional CMP. Ultimately we seek to model the eCMP process on the wafer, chip, and feature scale, capturing both layout pattern dependency and tool uniformity effects.



▲ Figure 2: Amount of copper removal for head positions of 5.0, 5.5, and 6.0 inches, and voltage zone settings of V_1, V_2 , and $V_3 = 2, 1$, and $3V$, respectively. (Top) Basic ohmic model versus data. The RMS error of this fit is 531 \AA . (Bottom) Non-ohmic model versus data. The RMS error of this fit is 412 \AA , a 22% improvement.

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