MTL

microsystems technology laboratories

massachusetts institute of technology

Annual Research Report

September 2008

MTL Annual Research Report *September 2008*

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PSB 08-06-0393

Introduction

Anantha P. Chandrakasan
Director, MTL

Welcome to the 2008 Microsystems Technology Laboratories (MTL) Annual Report. This report summarizes the research from 115 faculty and senior research staff associated with the MTL. The report covers diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, and micro-electromechanical systems (MEMS), as well as molecular and nano-technologies. These investigators come from more than 38 different departments, labs, and centers across the Institute.

MTL is an interdepartmental laboratory at MIT with a mission to foster research and education in semiconductor process and device technology, and integrated circuits and systems design. MTL provides micro- and nano-fabrication and computer aided design (CAD) infrastructure to the entire campus. Last year, more than 550 researchers, primarily graduate students, conducted research using the MTL infrastructure.

MTL's fabrication environment includes three clean rooms: the Class 10 Integrated Circuits Laboratory, the Class 100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation (EDA) for device, circuit and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL partners with industry through the Microsystems Industrial Group (MIG), who provide significant support, both financial and technical, in support of MTL's research and research infrastructure. This year, two new members, Taiwan Semiconductor Manufacturing Corp. (TSMC) and STMicroelectronics, have joined the MIG. The members of the Industrial Advisory Board (one member from each of our MIG companies) provide guidance in shaping the vision of MTL. The current IAB can be found at the following website: http://mtlweb.mit.edu/mig/iab.html.

A number of committees set strategies and direction for the lab. The MTL Seminar Series Committee has put together a an excellent seminar series open to the public. MTL's flagship event is the MTL Annual Research Conference (MARC) held annually in Waterville Valley, New Hampshire. The conference is run by MTL graduate students in collaboration with a steering committee chaired by Professor Joel Voldman. The conference has grown substantially over the past few years and is widely attended by industry, faculty, students and staff. MARC 2008 had more than 200 attendees. MTL Days at MIG companies, where MTL graduate students and faculty present leading-edge results to our industry partners, have also been popular.

Research conducted at MTL (as organized in the Annual Report) can be broadly classified into five categories: Circuits & Systems, Electronic Devices & Emerging Technologies, MEMS & BioMEMS, Molecular & Nanotechnology, and Photonics. MTL has four affiliated industrial research centers with more focused interests: the Center for Integrated Circuits and Systems (CICS), the Intelligent Transportation Research Center (ITRC), MEMS@MIT, and the Center for Integrated Photonic Systems (CIPS).

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A.I. Akinwande	Microstructures and nanostructures for sensors and actuators, and vacuum microelectronics. Devices for large area electronics and flat panel displays.	39-553b	617-258-7974	akinwand@mtl.mit.edu
D.A. Antoniadis	Fabrication, measurements and modeling of silicon- and germanium-based devices for high-speed and low-power integrated circuits.	39-427b	617-253-4693	daa@mtl.mit.edu
M.A. Baldo	Molecular electronics, integration of biological materials and conventional electronics, electrical and exciton transport in organic materials, energy transfer, metal-organic contacts, nanomechanical transistors.	13-3053	617-452-5132	baldo@mit.edu
K.K. Berggren	Superconductive nanodevice physics and applications; nanofabrication methods, processes, and tool-development for application to superconductive quantum computing and single-photon detection.	36-219	617-324-0272	berggren@mit.edu
S.N. Bhatia	Micro- and nano-technologies for tissue repair and regeneration. Applications in liver tissue engineering, cell-based BioMEMS, and nanobiotechnology.	E19-502d	617-324-0221	sbhatia@mit.edu
D.S. Boning	Characterization and modeling of variation in semiconductor and MEMS manufacturing with emphasis on chemical mechanical polishing (CMP), electroplating, plasma etch, and advanced interconnect processes. Understanding the impact of process and device variation on circuit performance and design for manufacturability.	38-435	617-253-0931	boning@mtl.mit.edu
V.M. Bove, Jr.	Sensing, display, user interface, and computation for consumer electronics applications, particularly self-organizing ecosystems of devices. Advanced data representations for multimedia.	E15-368B	617-253-0334	vmb@media.mit.edu
V. Bulović	Physical properties of organic and organic/inorganic nanocrystal composite thin films and structures; development of nanostructured electronic and optoelectronic devices.	13-3138	617-253-7012	bulovic@mit.edu
A.P. Chandrakasan	Design of digital integrated circuits and systems. Energy efficient implementation of signal processing and communication systems. Circuit design with emerging technologies.	38-107	617-258-7619	anantha@mtl.mit.edu
L. Daniel	Parameterized model order reduction of linear and nonlinear dynamical systems; mixed-signal, RF and mm-wave circuit design and robust optimization; power electronics, MEMs design and fabrication; parasitic extraction and accelerated integral equation solvers.	36-849	617-253-2631	luca@mit.edu
J.L. Dawson	Analog system theory and its applications. RF transceivers, power amplifier linearization, high-speed data conversion, problems in nonlinear control.	39-527a	617-324-5281	jldawson@mtl.mit.edu
J.A. del Alamo	Microelectronics device technologies for gigahertz and gigabit-per-second communication systems: physics, modeling, technology and design. InGaAs as a post-CMOS semiconductor logic technology. Technology and pedagogy of online laboratories for engineering education.	39-567a	617-253-4764	alamo@mit.edu
C.G. Fonstad, Jr.	Compound semiconductor heterostructure devices and physics. Optoelectronics: laser diodes, photodiodes, quantum effect devices, and OEICs. Monolithic heterogeneous integration. Microscale thermophotovoltaics.	13-3050	617-253-4634	fonstad@mit.edu
S. Gradečak	Nano-electronics and photonics; correlation of structural, optical, electronic, and magnetic properties of semiconducting materials; inorganic nanowires, nanowire heterostructure and devices; III-V semiconductor epitaxial films and low-dimensional systems; development of advanced electron microscopy techniques.	13-5094	617-253-9896	gradecak@mit.edu

NAME	RESEARCH AREAS & SPECIAL INTERESTS	OFFICE	PHONE	E-MAIL
J. Han	Nanofluidic/microfluidic technologies for advanced biomolecule analysis and sample preparation: novel nanofluidic phenomena, nanofluidic biomolecule separation and pre-concentration, molecular transport in nano-confined space.	36-841	617-253-2290	jyhan@mit.edu
J.L. Hoyt	Epitaxial growth, fabrication and device physics of silicon-based heterostructures and nanostructures. High mobility Si and Ge-channel MOSFETs and silicon-germanium photodetectors for electronic/photonic integrated circuits.	39-427A	617-452-2873	jlhoyt@mtl.mit.edu
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R. Karnik	Micro- and nanofluidic systems. Application of transport phenomena in nanofluidics for flow control, separation, sensing. Microfluidic devices for studying chemical kinetics and nanoparticle synthesis.	3-461A	617-324-1155	karnik@mit.edu
A. Khademhosseini	Development of micro- and nanoscale technologies to control cellular behavior. Particular emphasis in developing microscale biomaterials and engineering systems for tissue engineering and drug delivery.	E25-342	617-768-8395	alik@mit.edu
S.-G. Kim	Nanomanufacturing, MEMS assembly en masse, carbon nanotube transplanting assembly. self-cleaning RF MEMS switch, piezoelectric energy harvesting, printable PZT MEMS.	1-310	617-452-2472	sangkim@mit.edu
L.A. Kolodziejski	Research in integrated photonic devices and optoelectronic components. Design and fabrication of photonic crystals and III-V semiconductor devices. Electronic materials growth and characterization.	36-287	617-253-6868	leskolo@mit.edu
J. Kong	Synthesis, characterization and applications of carbon-based nanomaterials (nanotubes and graphene) and inorganic nanowires.	13-3065	617-324-4068	jingkong@mit.edu
J.H. Lang	Analysis, design and control of electromechanical systems with application to traditional electromagnetic actuators, micron-scale actuators and sensors (MEMS), and flexible structures.	10-176	617-253-4687	lang@mit.edu
H.-S. Lee	Analog and mixed-signal integrated circuits with a particular emphasis on data conversion circuits in scaled CMOS.	39-553	617-253-5174	hslee@mtl.mit.edu
C. Livermore	Microelectromechanical systems (MEMS). Design and fabrication of high power microsystems, including electrical generators and MEMS components for lasers. Self-assembly techniques for nano- and micro-scale manufacturing.	3-449C	617-253-6761	livermor@mit.edu
S.R. Manalis	Microdevices for biomolecular and single-cell detection.	E15-422	617-253-5039	scottm@media.mit.edu
I. Masaki	VLSI architecture. Emphasis on interrelationship among applications, systems, algorithms, and chip architectures. Major application fields include intelligent transportation systems, video, and multimedia.	38-107	617-253-8532	imasaki@aol.com
T. Palacios	Design, fabrication, and characterization of novel electronic devices in wide bandgap semiconductors; polarization and bandgap engineering; transistors for sub-mm-wave power and digital applications; new ideas for power conversion and generation; interaction of biological systems with semiconductor materials and devices; nanowires and carbon nanotube –based transistors.	39-567B	617-324-2395	tpalacios@mit.edu
D.J. Perreault	Power electronics and energy conversion, Electronic circuit design and control. Applications to industrial, commercial, scientific, transportation, and biomedical systems.	10-039	617-258-6038	djperrea@mit.edu

NAME	RESEARCH AREAS & SPECIAL INTERESTS	OFFICE	PHONE	E-MAIL
M.H. Perrott	Circuit and architecture design for high speed mixed-signal circuits such as phase-locked loops and A/D converters: circuit topologies, architectural approaches, design methodologies, modeling and simulation techniques. Communication system simulation software and tutorials for engineering education.	38-344b	617-452-2889	perrott@mit.edu
R.J. Ram	Photonic devices for applications in communications, computing, and biological sensing with special emphasis on fiber-to-the-home, InP photonic integration, Silicon photonics and high speed interconnects, microscale bioreactors, and biomanufacturing.	36-491	617-253-4182	rajeev@mit.edu
C.A. Ross	Fabrication, properties and applications of magnetic and magnetooptical films and nanostructures; self assembly, block copolymer lithography.	13-4005	617-258-0223	caross@mit.edu
R. Sarpeshkar	Biomedical systems, circuit modeling of biology, bio-inspired systems.	38-294	617-258-6599	rahuls@mit.edu
M.L. Schattenburg	Advanced lithography, including x-ray, electron-beam, ion-beam, and optical. Nanotechnology and nanofabrication. Precision engineering and nano-accuracy dimensional metrology. Advanced interference lithography technology for high-accuracy patterning of general grating and grid patterns. Micro and nanometer fabrication technology applied to advanced astronomical and laboratory instrumentation. Silicon micromachined structures applied to high-precision optical assembly. X-ray optics and instrumentation.	37-487	617-253-3180	marks@space.mit.edu
M.A. Schmidt	Micromechanical systems (MEMS). Microfabrication technologies for integrated circuits, sensors, and actuators; design of micromechanical sensor and actuator systems; mechanical properties of microelectronic materials with emphasis on silicon wafer bonding technology; integrated microsensors, and microfluidic devices. Novel applications of MEMS and nanotechnologies to a variety of fields, including miniature gas turbines, miniature chemical reactors, miniature gas analyzers, microswitches, biological applications, and sensors monolithically integrated with electronics.	39-521	617-253-7817	schmidt@mtl.mit.edu
A.H. Slocum	Precision machines and mechanisms from macro to nanoscale.	3-445	617-253-0012	slocum@mit.edu
H.I. Smith	Co-director, NanoStructures Lab. Development of nanofabrication tools and techniques aimed at reaching molecular dimensions and sub-1nm positional accuracy; nanophotonics; templated self assembly.	36-225	617-253-6865	hismith@mit.edu
C.G. Sodini	Design of technology-intensive Microsystems, emphasizing integrated circuit design at the device level, including organic integrated circuits, high data rate wireless LANs, and mm-wave imaging systems.	39-527b	617-253-4938	sodini@mit.edu
V. Stojanović	On-chip interconnects and high-speed off-chip interfaces (electrical, photonic). Modeling and analysis of noise and dynamics in circuits and systems. Application of optimization techniques to digital communications, analog and digital circuits. Digital communications and signal-processing architectures, clock generation and distribution, high-speed digital circuit design, VLSI and mixed-signal IC design.	38-260	617-324-4913	vlada@mit.edu
C.V. Thompson	Processing and property optimization for thin films and nanostructures for applications in electronic and electromechanical integrated device systems. Advanced, reliable integrated circuit interconnects.	13-5069	617-253-7652	cthomp@mit.edu
H.L. Tuller	Resonant and chemoresistive sensors, micro-fuel cells, high K dielectrics, electro-optic and piezoelectric thin films, solid state ionics, thin film transistors, MEMS structures and devices.	13-3126	617-253-6890	tuller@mit.edu
J. Voldman	Microtechnology for basic and applied cell biology; Microfluidic perfusion culture, patterning, and manipulation of stem cells. Electrostatics at the microscale, especially dielectrophoresis.	36-824	617-253-2094	voldman@mit.edu

NAME	RESEARCH AREAS & SPECIAL INTERESTS	OFFICE	PHONE	E-MAIL
E. N. Wang	Micro/nanoscale transport micro-/nanoscale transport phenomena, MEMS/NEMS design and sensing, optical diagnostics, numerical modeling, and surface nanoengineering for thermal management, energy conversion, water desalination, and biological systems.	3-461b	617-324-3311	enwang@mit.edu
B.L. Wardle	Nano-engineered composites, MEMS Power devices and energy harvesting, advanced composite materials and systems, structural health monitoring (SHM), fracture, fatigue and damage mechanics, durability modeling/testing, finite-element modeling, structural response and testing, buckling mechanics, project design and management, business strategy and growth, cost modeling.	33-314	617-252-1539	wardle@mit.edu

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Circuits & Systems

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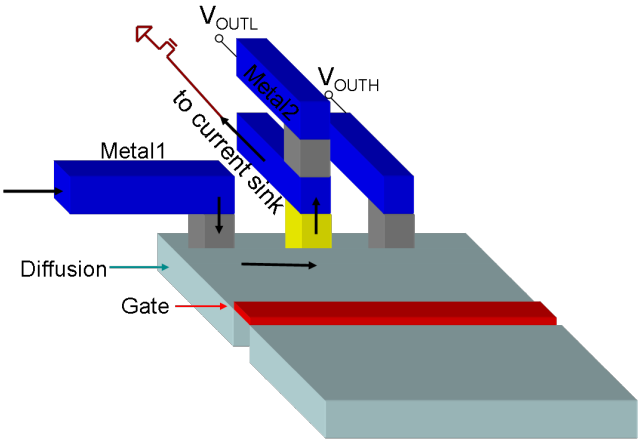
Contact-resistance Variation in Advanced Technologies

K. Balakrishnan, D.S. Boning

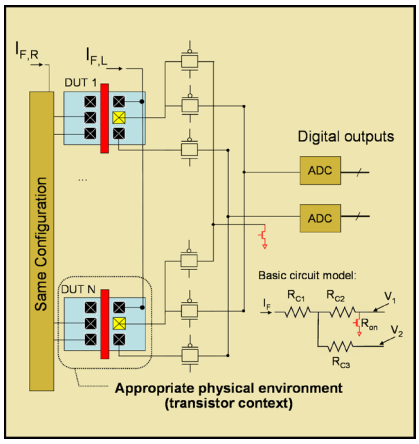
Sponsorship: SRC/FCRP IFC, Samsung

Due to the continuous and aggressive scaling of CMOS technology, the parameters and characteristics that are most critical in determining the quality and robustness of a device are changing. One such trend is the impact of silicide-diffusion contact resistance, which is becoming an increasingly larger component of the total resistance in a MOSFET [1]. Consequently, variability in contact resistance must now be considered in order to accurately capture the robustness of a transistor. The primary goal of this work is to design and fabricate a test chip that will characterize the variability of contact resistances by measuring a large array of devices under test. Completing the characterization of contact resistances will allow for the generation of a compact model that incorporates sensitivities to various parameters into the determination of individual contact resistances. Finally, this methodology can be generalized to investigate contacts in novel technologies, such as carbon nanotube-based contacts.

A test chip has been designed and will be fabricated using an IBM 90-nm process to investigate this variability and gather statistics regarding its characteristics. Figure 1 shows a general setup with which the resistance of a contact can be measured using the equivalent of a four-point probing Kelvin-based structure. This scheme is multiplexed across multiple devices to gather large amounts of data for variability analysis (see Figure 2). In this test chip, the silicide-diffusion contact resistances are measured for a large array of transistors using a multiplexed current-force voltage-sense methodology. The design of experiments includes different combinations of values for parameters such as contact-to-gate distance, contact-to-diffusion edge distance, and the number of contacts on the sources and drains of devices. In addition, the test chip also contains structures that can gather contact resistance information as well as device characteristics to decouple variability information.



▲ Figure 1: Current-force voltage-sense methodology to determine resistance of contact highlighted in yellow. With the transistor turned off, the current forced through metal line will go through the contact, and then the resistance is directly proportional to $V_{OUTH} - V_{OUTL}$.



▲ Figure 2: Multiplexing strategy to characterize a large number of silicide-diffusion contacts. A sink device is used to carry all the input current. With off-chip ADCs, measurement accuracy and test chip area are both maximized, while the losses with respect to increased noise are minimal because of DC measurements.

Reference

[1] S.D. Kim, C.M. Park, and J.C.S. Woo, "Advanced model and analysis of series resistance on CMOS scaling into nanometer regime – Part 2: Quantitative analysis," *IEEE Transactions on Electron Devices*, vol. 49, pp. 467-472, Mar. 2002.

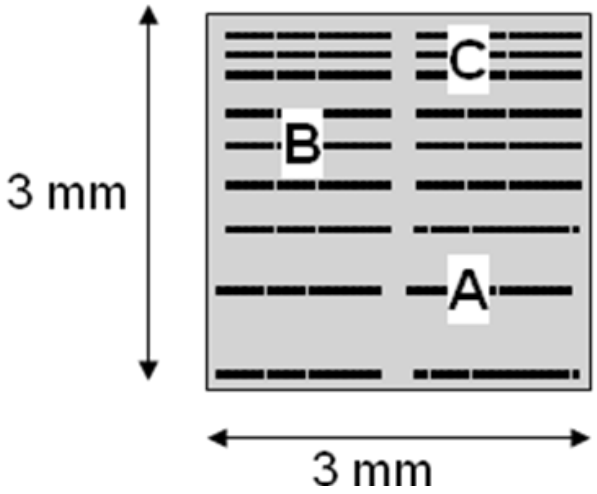
Test Circuits for $I_{D(sat)}$ Variation Characterization

A.H. Chang, D.S. Boning
Sponsorship: TSMC

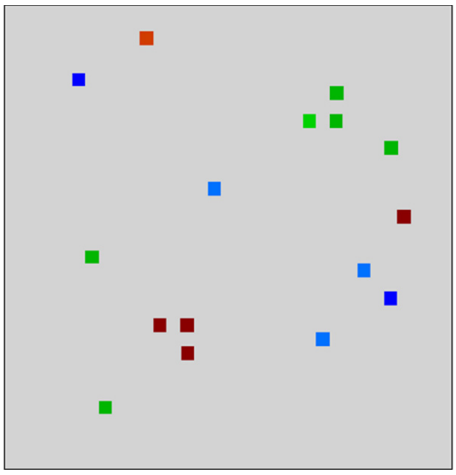
The variation in process, device, and circuit is an increasingly difficult and critical concern for future integrated circuit design. Variation may have systematic components such as spatial, device-size, or pattern-density dependency, or it may have random stochastic components such as random doping fluctuations. Increasing effort is needed in the modeling and characterizing of device variations in order to design circuits robustly.

Figure 1 shows three common types of measuring schemes. Type *A* is the simplest approach, in which direct probing is used for full electrical characterization of a device. The Type A measuring scheme requires dedicated pads for probing; therefore, only a small number of probing terminals is available. The probing may also introduce extra stress on the device, which could change the device characteristic after measurement. Type B uses multiplexed circuitry to extract DC current-voltage (I-V) measurements [1, 3, 4]. This pad-sharing scheme is more efficient, enabling characterization of more devices than in Type A. Type C is a dedicated circuit structure focused on extracting a specific device parameter, such as V_T [2].

Figure 2 illustrates a systematic variation of saturation current across a single chip schematically. Several sources may contribute to observed $I_{D(sat)}$ variation, and each must be considered and understood. In deeply scaled technologies, variation in V_T is believed to be mostly due to random dopant fluctuation [3] and would not explain systematic dependencies or neighborhood pattern dependencies. Different STI pattern densities can be explored to see if the resulting device variations show a clear systematic layout density offset. This component is of particular interest, as it is conjectured that stress or thermal annealing process effects may contribute to $I_{D(sat)}$ variation. While previous research efforts have explored the variation and layout dependency of V_T and channel length individually, few have focused on the effect of stress or annealing related mobility variation [1-5]. In this project, our goal is to design test-circuit approaches to isolate the device variation parameters (V_T, L, and μ) and dependencies for future technologies, focusing especially on $I_{D(sat)}$ variation. A set of design rules and guidelines can then be formulated to minimize these variations.



▲ Figure 1: Three common types of measuring schemes. Type A is direct probing; Type B is multiplexed I-V measurement structure; and Type C is customized circuits for specific parameter extraction.



▲ Figure 2: Hypothesized clustering of saturation current across a die. The effect of local and neighborhood layout practices (transistor feature sizes, STI pattern density, etc.) on systematic deviations in $I_{D(sat)}$, and in variance of saturation current, need to be understood. Test structures and circuits to identify and separate sources of variation are being developed.

References

[1] K.G. Gettings, "Study of CMOS process variation by multiplexing analog characteristics," Ph.D. Thesis, MIT, Cambridge, June 2007.
[2] N. Drego, A. Chandrakasan and D. Boning, "A test-structure to efficiently study threshold-voltage variation in large MOSFET arrays," *IEEE International Symposium on Quality Electronic Design*, Mar. 2007, pp. 281-286.
[3] K. Agarwal, S. Nassif, F. Liu, J. Hayes, and K. Nowka, "Rapid characterization of threshold voltage fluctuation in MOS devices," *International Conference on Microelectronic Test Structures*, pp. 74-77, 2007.
[4] L.T. Pang and B. Nikolic, "Impact of layout on 90nm CMOS process parameter fluctuations," *Symposium on VLSI Circuits, Digest of Technical Papers*, 2006, pp. 69-70.
[5] P. Friedberg, Y. Cao, J. Cain, R. Wang, J. Rabaey, and C. Spanos, "Modeling within-die spatial correlation effects for process-design co-optimization," *Proc. of the Sixth International Symposium on Quality Electronic Design*, Mar. 2005.

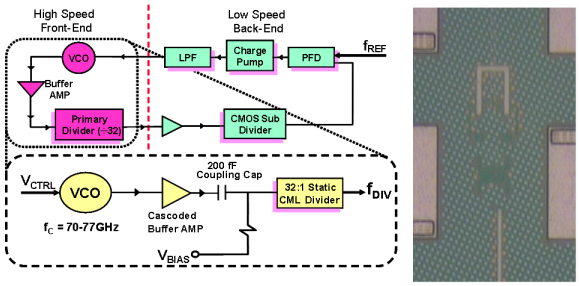
Process Variation in High-speed RF Front-end Circuits

D. Lim, D.S. Boning

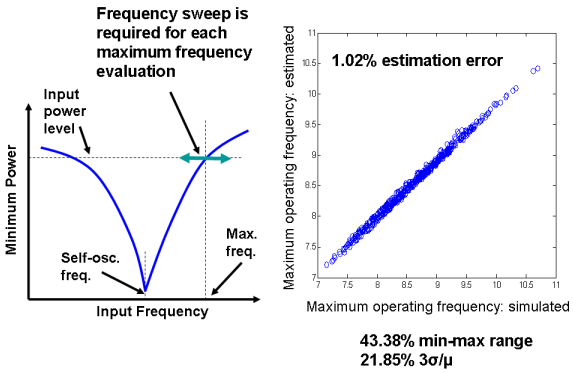
Sponsorship: IBM, SRC/FCRP C2S2

Modern RF circuit designs in deeply scaled CMOS technologies need efficient characterization of process-induced variation in performance variables and robust optimization methods to obtain high-yielding chips. A PLL front-end consists of a VCO and 2:1 frequency divider. Since the PLL front-end operates at the highest frequency in the system, speed, power consumption, and noise characteristics must be considered carefully during design. Furthermore, the tuning range of the VCO is significantly narrowed by the reduced ratio between varactor and parasitic capacitance in scaled devices. The operating range of the frequency divider is also limited since input signal power is reduced due to the loss in interconnects. Recently, 22.8% 3σ/μ variation in the self-oscillation frequency of dividers in 65-nm SOI technology has been reported [1]. The mismatch between the operating ranges of the VCO and the frequency divider due to process variation can cause a serious yield problem.

A 70-GHz mm-wave PLL front-end with an LC-VCO and 2:1 CML frequency divider has been implemented as in Figure 1. The variation in the VCO and divider performance has been measured and their correlation has been estimated. The variation in the frequency divider is critical for the functionality of the PLL front-end circuit, and the bias condition of the divider has been optimized for the highest functional yield while achieving the maximum output signal-to-noise ratio [2]. Additionally, the estimation of the variation in the maximum operating frequency of the divider is extremely time-consuming since input frequency must be swept by a small step for fine resolution in each Monte Carlo simulation run. We suggest a new time delay model for a CML differential buffer that is based on a quadratic function of physical delay components. The suggested model estimates the maximum operating frequency variation with roughly 1% error in 500 Monte Carlo runs, as Figure 2 shows.



▲ Figure 1: A 70-GHz mm-wave PLL diagram and high-speed front-end building blocks, including a VCO and a frequency divider with external bias control. The circuit is fabricated in 65-nm SOI CMOS and the die photo is shown.



▲ Figure 2: An input sensitivity curve of a frequency divider and scattering plot of simulated and estimated maximum operating frequency of the divider. The maximum operating frequency simulation is extremely time-consuming for frequency and power sweeping; the suggested model provides around 1% estimation error.

Reference

[1] D. Lim, J. Kim, J.-O. Plouchart, C. Cho, D. Kim, R. Trzcinski, and D. Boning, "Performance variability of a 90-ghz static CML frequency divider in 65-nm SOI CMOS technology," *IEEE ISSCC Digest of Papers*, Feb. 2007, pp. 542-621.

[2] D. Lim, J. Kim, J.-O. Plouchart, C. Cho, D. Kim, and D. Boning, "Performance and yield optimization of mm-wave PLL front-end in 65-nm SOI CMOS," *IEEE RFIC Symposium Digest of Papers*, June 2007, pp. 525-528.

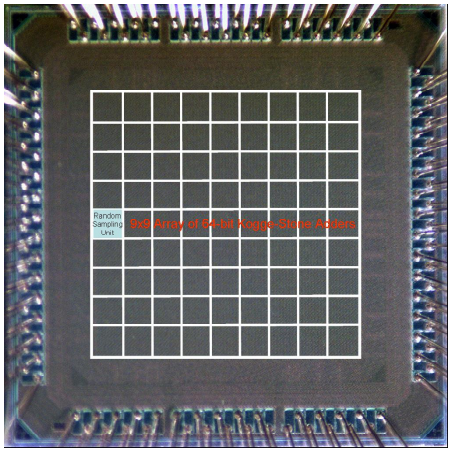
Spatial Variation in Advanced CMOS Devices and Circuits

N. Drego, A.P. Chandrakasan, D.S. Boning
Sponsorship: SRC/FCRP C2S2

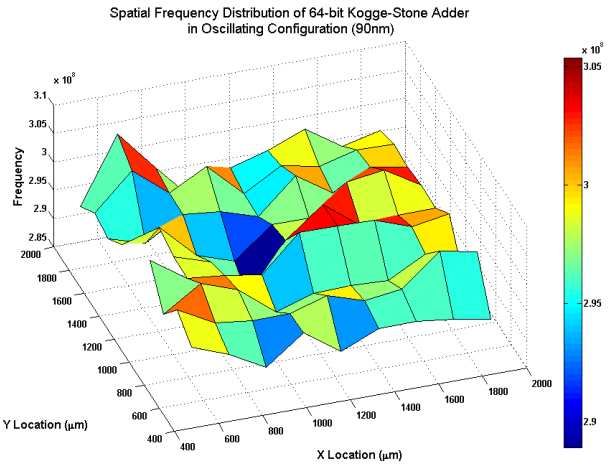
Modern circuit designs in deeply scaled technologies need efficient characterization of process variation in order to obtain high-yielding chips. Circuit designers need accurate guidelines to prevent failures due to layout-induced variations. We address one specific portion of this need by characterizing and quantifying spatial variation trends in both device parameters and circuit performance.

At the device level, we have implemented a test-structure capable of efficiently measuring leakage currents of a large number of devices (~70K NMOS + ~70K PMOS). All devices are minimum length and range in width from minimum width to 3.0μm. By measuring leakage currents, we are able to extract mismatches in threshold voltage between two devices, ΔV_T [1]. Measured leakage currents and extracted ΔV_T from the test chip indicate no within-die spatial correlation and no inter-die correlation in the variation pattern. These results indicate that a truly random process, such as Random Dopant Fluctuation (RDF), is the dominant source of threshold voltage variation. Furthermore, this lack of correlation poses problems in low-power, low-voltage systems where the effect of V_T variation is dominant. In particular, sub-threshold circuits are most susceptible to completely random variation. Simulations show that even with strong correlation in channel length variation, as the operating voltage of a circuit decreases below twice the nominal V_T of the process, correlation in circuit performance decreases quickly.

To quantify this correlation in circuit performance, a test-chip has been implemented (Figure 1) containing adder delay paths in an oscillating configuration with simple asynchronous counters to measure frequency. A Phase-Frequency Detector and random sampling technique to quantify delay variation in individual bits of each adder are also included. Monitor ring-oscillator circuits are also laid out to characterize correlation between monitor circuits and actual critical paths of 64-bit Kogge-Stone adders. Preliminary results indicate only weak within-die spatial correlation between adjacent adders as well as between adders and adjacently placed monitor ring-oscillators. Figure 2 is a plot of the adder frequencies on a single-die showing no spatial trend. However, die-to-die correlation is high (~0.9) but degrades with decreasing V_{DD}, as predicted by the simulations performed previously. On-going data gathering will provide additional statistical confidence in these measurements.



▲ Figure 1: Test-chip containing eighty 64-bit Kogge-Stone adders in an oscillating condition along with monitor ring-oscillators and frequency counters. A random-sampling technique is also implemented to measure delays between individual bits of the adders.



▲ Figure 2: Spatial distribution of 80 Kogge-Stone adders on a single die showing no spatial trends. Further statistical analysis reveals only weak within-die spatial correlation but strong die-to-die correlation, degrading with decreasing operating voltage

Reference

[1] N. Drego, A. Chandrakasan, and D. Boning, "A test structure to efficiently measure V_T-variation in large MOSFET arrays," *International Symposium on Quality Electronic Design*, Mar. 2007.

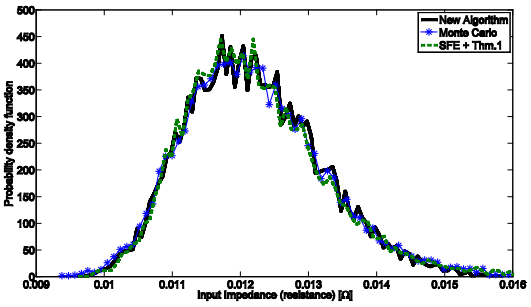
A Stochastic Integral Equation Solver for Efficient Variation-aware Interconnect Extraction

T. Moselhy, L. Daniel

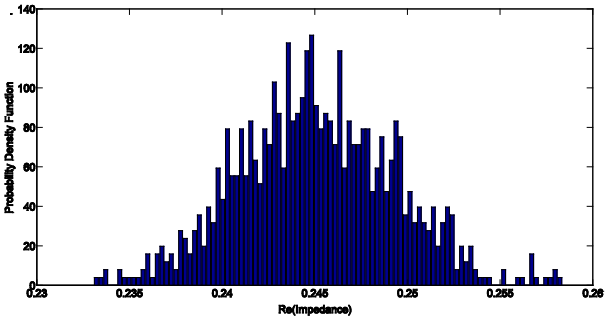
Sponsorship: Cadence Design Systems, SRC/FCRP IFC, SRC

On-chip and off-chip fabrication processes may typically generate interconnect structures of irregular geometries. Such irregularities are not deterministic and are produced by several different manufacturing steps, such as etching, chemical mechanical polishing (CMP), electro-deposition, and photolithography. However, as a result of technological scaling, such manufacturing uncertainties are now beginning to play a major role in determining the electrical characteristics of the interconnect structures. Consequently, variation-aware interconnect extraction is becoming increasingly important.

In this research we have developed a new methodology to solve large stochastic linear systems typically appearing during variation-aware extraction [1]. We have derived a new theorem to compute the coefficients of the multivariate Hermite expansion using only low-dimensional integrals, resulting in a time complexity that is independent of the number of variables and dependent only on the order of the expansion. Practically speaking, for a typical large multivariate expansion, the new theorem provides an improvement in the computation time by 86 orders of magnitude as compared to the standard tensor product rule, or by 10 orders of magnitude as compared to the state of the art (Monte Carlo integration or sparse grid integration [2]). Such a theorem is not only useful for our methodology but also can be applied to any algorithm that relies on expanding a random process, such as the stochastic finite element method (SFE) [3]. We have also provided a new stochastic simulation technique by merging both the Neumann expansion and the polynomial chaos expansion. The main advantages of the resulting technique are the compact size of the system at any time (unlike SFE) and the ease of calculating the statistics of the high-order terms (unlike Neumann expansion [4]). In addition, the new simulation algorithm is parallizable and can therefore take advantage of the state of the art in processor design. We have demonstrated the computational efficiency of the new methodology by solving problems that were completely intractable before. We have demonstrated that our algorithm can be used to compute the complete probability density function of the input impedance of very large problems (up to 400 random variables) in less then 8 hours using Matlab on a standard 4-core machine and using only 121 MB RAM.



▲ Figure 1: Comparison between the probability density function of the microstrip line obtained from our new algorithm and the reference Monte Carlo simulation.



▲ Figure 2: Probability density function of the real part of the input impedance at 1GHz for correlation length Lc = 50μm. The resistance of the non-rough surface is 11.3% smaller than the mean of the obtained distribution.

References

[1] T. Moselhy and L. Daniel, "Stochastic Integral Equation Solver for Variation-Aware Interconnect Extraction," presented at *Design Automation Conference*, June 2008.

[2] D. Xiu and G. Karniadakis, "The Wiener-Askey Polynomial Chaos Expansion for Stochastic Differential Equations," *SIAM Journal of Scientific Computing*, vol. 24, pp. 619-644, Oct. 2002.

[3] R. Ghanem and P. Spanos, *Stochastic Finite Elements: A Spectral Approach*. Springer-Verlag, 1991.

[4] Z. Zhu and J. White, "FastSies: A Fast Stochastic Integral Equation Solver for Modeling the Rough Surface Effect," in *Proc. IEEE/ACM International Conference on Computer Aided Design*, Nov. 2005, pp. 675-682.

A Piecewise-linear Moment-matching Approach to Parameterized Model-order Reduction for Highly Nonlinear Systems

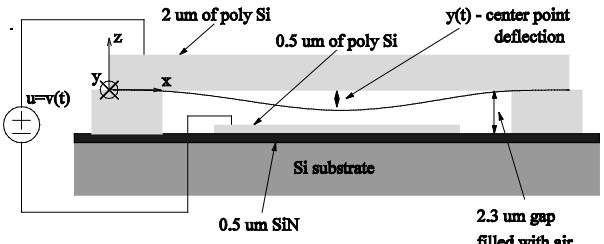
B. Bond, L. Daniel

Sponsorship: SRC/FCRP, NSF, DARPA

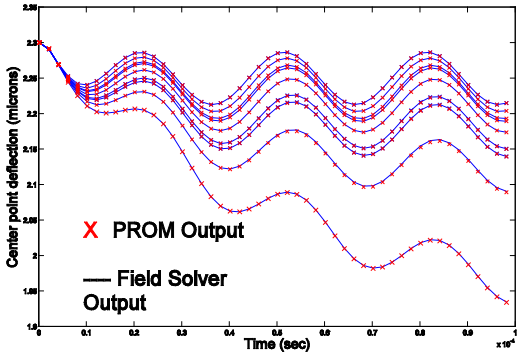
The automatic extraction of parameterized macromodels for modern mixed-signal System-on-Chips is an extremely challenging task due to the presence of several nonlinear analog circuits and Micro-Electro-Mechanical (MEM) components. The ability to generate Parameterized Reduced Order Models (PROMs) of nonlinear dynamical systems could serve as a first step toward the automatic and accurate characterization of geometrically complex components and subcircuits, eventually enabling their synthesis and optimization.

Our approach to this problem combines elements of a non-parameterized trajectory piecewise-linear method [1] for nonlinear systems with a moment-matching parameterized technique [2] for linear systems. By building on these two existing methods, we have created an algorithm for generating PROMs for nonlinear systems. The algorithms were tested on three different systems: a MEM switch, shown in Figure 1, and two nonlinear analog circuits. All of the examples contain distributed strong nonlinearities and possess dependence on several geometric parameters.

In addition, we have proposed a model-construction procedure in which we approximate the system sensitivity to parameters of interest for the purpose of efficiently sampling important regions of the parameter space. Figure 2 shows the output of one PROM created for the example in Figure 1 and compared to the field solver output of the full nonlinear system at several parameter values. Typical PROMs constructed in this manner can be accurately reduced in size by a factor of 10, yielding a speedup of a factor of 10 in general. For further details on parameter-space accuracy and cost of the algorithms, see [3].



▲ Figure 1: Application example: MEM switch realized by a polysilicon beam fixed at both ends and suspended over a semiconducting pad and substrate expansion.



▲ Figure 2: Center point deflection predicted by our parameterized reduced model (crosses) at a series of parameter values, compared to a finite difference detailed simulation (solid lines).

References

[1] M. Rewienski and J.K. White, "A trajectory piecewise-linear approach to model-order reduction and fast simulation of nonlinear circuits and micromachined devices," In *Proc. of IEEE/ACM International Conference on Computer Aided-Design*, San Jose, CA, Nov. 2001, pp. 252-257.

[2] L. Daniel, C.S. Ong, S.C. Low, K.H. Lee, and J.K. White, "A multiparameter moment-matching model reduction approach for generating geometrically parameterized interconnect performance models," *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, vol. 23, no. 5, pp. 678-693, May 2004.

[3] B. Bond and L. Daniel, "A piecewise-linear moment-matching approach to parameterized model-order reduction for highly nonlinear systems," *IEEE Trans. on Computer-Aided Design*, vol. 26, no. 12, pp. 2116-2129, Dec. 2007.

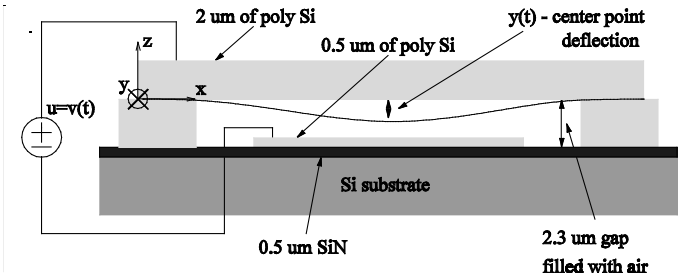
Stable Model-order Reduction for Highly Nonlinear Systems

B. Bond, L. Daniel

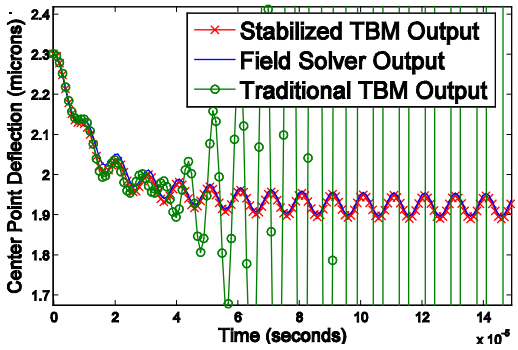
Sponsorship: SRC/FCRP, NSF, DARPA

The ability to generate accurate reduced-order models (ROMs) of nonlinear dynamical systems, such as analog circuits and micro-electromechanical systems (MEMS), is a crucial first step in the automatic design and optimization of such systems. One popular approach to model order reduction (MOR) of highly nonlinear systems employs trajectory-based methods, such as the piecewise-linear (PWL) approach. Despite substantial recent interest in such methods [1, 2], trajectory-based models (TBMs) have failed to gain widespread acceptance due to a lack of theoretical statements concerning the accuracy of the resulting ROMs. In this work we address one such theoretical issue – guaranteed stability. Specifically, we present a scheme for preserving stability in PWL models whose system matrices possess a certain structure. We also propose a projection scheme and set of weighting functions, which together allow us to extend some of these stability results to PWL systems composed of arbitrary unstructured matrices.

The stability of nonlinear systems is determined by the existence of a Lyapunov function. Our stabilizing scheme ensures stability by constructing the projection matrices such that there exists a Lyapunov function for the resulting ROM. In the case where a system's Jacobians all possess a certain structure, examples of which are given in [3], we present a projection routine that guarantees the existence of a quadratic Lyapunov function for both the large PWL model and the ROM. In the case where the system's Jacobians have no structure, and it is not known whether a Lyapunov function exists for the large PWL model, we utilize a new nonlinear projection and new set of interpolation functions to create a collection of stable nonlinear systems. The final ROM will switch between the various stable nonlinear ROMs. One example of a system that produces unstructured Jacobians, and thus potentially unstable TBMs, is a MEMS switch (shown in Figure 1). Figure 2 shows a sample output from the MEMS switch, a stable TBM generated by our approach, and an unstable TBM generated by the traditional approach. For further details on the stabilizing procedure see [3].



▲ Figure 1: Application example: MEM switch realized by a polysilicon beam fixed at both ends and suspended over a semiconducting pad and substrate expansion



▲ Figure 2: Center point deflection predicted by our stabilized reduced model (red crosses), compared to a finite difference detailed simulation (solid blue lines) and the traditional TBM approach (green circles).

References

[1] M. Rewienski and J.K. White, "A trajectory piecewise-linear approach to model-order reduction and fast simulation of nonlinear circuits and micromachined devices," in *Proc. of IEEE/ACM International Conference on Computer Aided-Design*, San Jose, CA, Nov. 2001, pp 252-257.

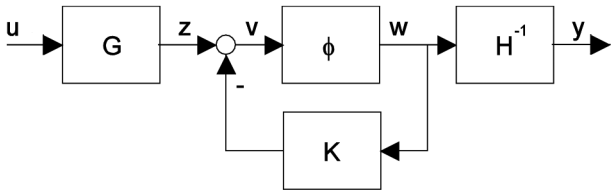
[2] B. Bond and L. Daniel, "A piecewise-linear moment-matching approach to parameterized model-order reduction for highly nonlinear systems," *IEEE Trans. on Computer-Aided Design*, vol. 26, no. 12, pp. 2116-2129, Dec. 2007.

[3] B. Bond and L. Daniel, "Stabilizing schemes for piecewise-linear reduced order models via projection and weighting functions," *Proc. of the IEEE Conference on Computer-Aided Design*, San Jose, CA, Nov. 2007, pp. 860-867.

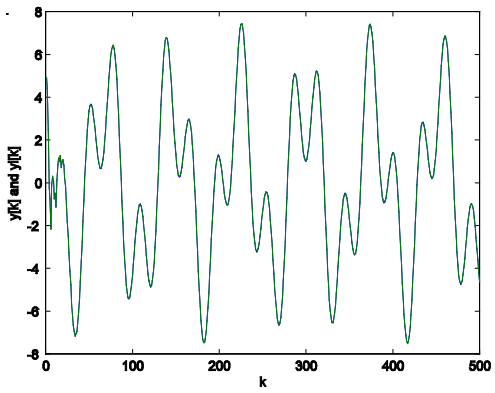
Convex Relaxation Approach to the Identification of the Wiener-Hammerstein Model for Modeling of Non-Linear Analog Circuit Blocks

K.C. Sou, A. Megretski, L. Daniel
Sponsorship: DARPA, SRC/FCRP IFC

Analog and mixed/signal VLSI circuits exhibit an ever-increasing and pressing need for automatic and accurate characterization of their non-linear components and subcircuits, in order to enable synthesis and optimization. While non-linear model order reduction has already been attempted using several types of clever linearizations or parametric approximation, in this project we are instead attempting a completely orthogonal approach. Specifically, this work proposes an input/output system identification technique for the Wiener-Hammerstein model and its feedback extension. In the proposed framework, the identification of the nonlinearity is non-parametric. The identification problem can be formulated as a non-convex quadratic program (QP). A convex semi-definite programming (SDP) relaxation is then formulated and solved to obtain a sub-optimal solution to the original non-convex QP. The convex relaxation turns out to be tight in most cases. When the relaxation idea is combined with the use of local search, high-quality solutions to the Wiener-Hammerstein identification can frequently be found. We identify randomly generated Wiener-Hammerstein models as examples of the application. Furthermore, we are attempting to use our method to identify small analog circuit blocks such as operational amplifiers. This work has been accepted for publication and will be presented at the Conference on Decision and Control inDecember 2008. [1]



▲ Figure 1: Wiener-Hammerstein model to be identified.



▲ Figure 2: Matching of outputs of the original system and the identified system.

Reference

[1] K.C. Sou, A. Megretski, and L. Daniel, "Convex relaxation approach to the identification of the Wiener-Hammerstein Model," to be presented at *IEEE Conference on Decision and Control*, Dec. 2008.

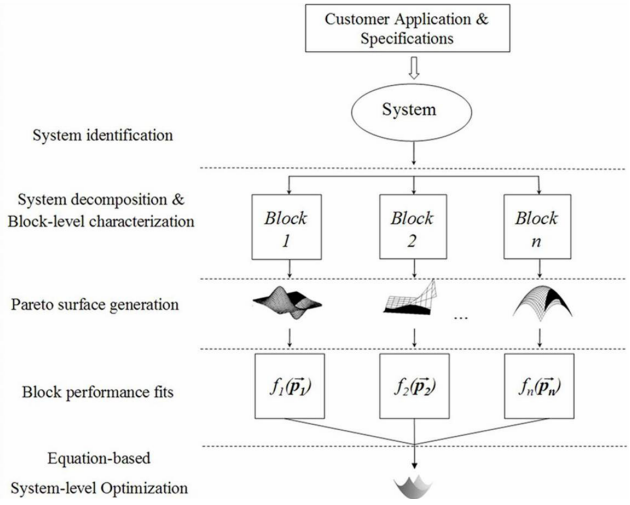
A Hierarchical, Equation-based Design Methodology for Optimizing Mixed-signal Systems

T. Khanna, W. Sanchez, J.L. Dawson

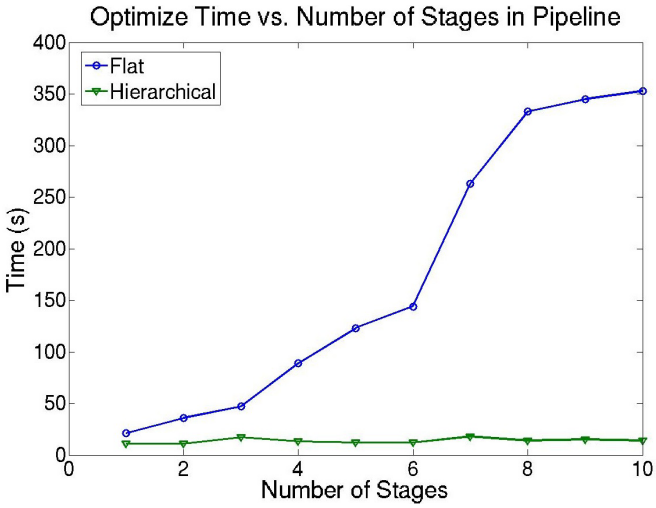
This work shows a hierarchical, equation-based optimization strategy suitable for system design, as Figure 1 shows. Because it is a hierarchical methodology, it scales gracefully to systems that are much larger than can be handled by known optimization methods. The desired system is broken into circuit blocks, whose performance spaces are quantitatively described as Pareto-optimal surfaces between system design variables. Exploiting the surfaces' gentle nature and amenability to low-order equation fits, the trade-off surfaces are abstracted to higher levels as representations of the circuit block. Thus, resources (such as power dissipation, noise budget, gain, etc.) are allocated at the system level very rapidly and very efficiently using familiar equation-based optimization strategies.

We have achieved excellent matching between flat and hierarchical optimizations in the discrete implementation of both a transmitter front-end and a 10-stage pipeline ADC in a 0.18-μm CMOS process. Using equation-based optimization, we have quantitatively described the Pareto surfaces of each pipeline stage and abstracted them to the system level. The surfaces were modeled with monomial fits, which all had less than a 10% relative error. We obtain a 4x and 25x running-time improvement in the receiver and ADC examples, respectively, when using a hierarchical optimization, a clear advantage for larger scale systems. The optimize times appear in Figure 2.

The value of the Pareto surfaces lies in the compact global perspective they provide to system designers. Because the Pareto surfaces are well behaved, we can use low-order functions in the abstraction, resulting in a low-complexity system optimization. The proposed methodology restores the tractability of system-level design problems and is a powerful aid to designers of large, mixed-signal systems.



▲ Figure 1: Hierarchical bottom-up (H-BU) design methodology that shows the steps involved in the complete system design cycle.



▲ Figure 2: Optimize times for the flat and hierarchical optimizations of pipeline ADC for varying number of stages. There is a 25x speed-up when using the hierarchy.

References

[1] M. Hershenson, S. Boyd, and T. Lee, "Efficient description of the design space of analog circuits," in *IEEE/Association for Computing Machinery Design Automation Conference*, June 2003.

[2] T. Eekeleart, T. McConaghy, and G. Gielen, "Efficient multiobjective synthesis of analog circuits using hierarchical Pareto-optimal performance hypersurfaces," *Design Automation and Test in Europe Conference Proc.*, pp. 1070-1075, June 2005.

[3] T. Eekeleart, R. Shoofs, G. Gielen, M. Steyeart, and W. Sansen, "Hierarchical bottom-up analog optimization methodology validated by a delta-sigma A/D converter design for the 802.11a/b/g standard," *IEEE/Association for Computing Machinery Design Automation Conference*, pp. 25-30, July 2006.

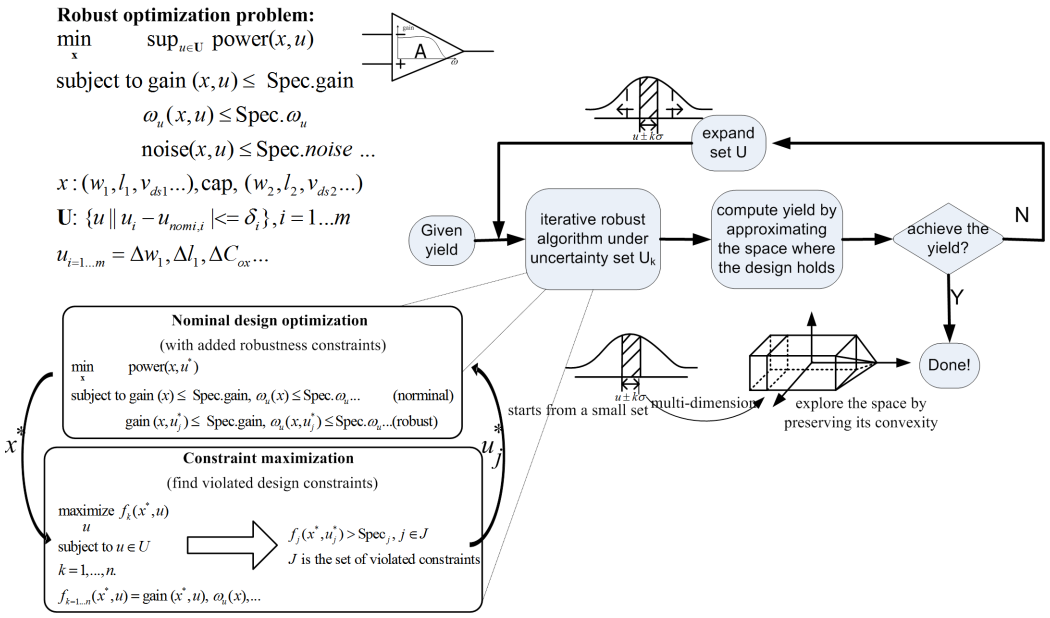
Iterative Robust Optimization of Analog Circuits

Y. Li, V. Stojanović

Sponsorship: SRC, CICS

As IC technologies scale down to the deep submicron region, process variation is becoming an increasingly severe issue for circuit designers. Designs are verified over process corners to improve the robustness of circuits and increase the manufacturing yield. However, corner-based robust design requires long design periods and often leads to overdesign. We are trying to develop new numerical algorithms fitted into an equation-based circuit optimization methodology [1], which incorporates the process variations, as well as provides yield estimation.

Inspired by the algorithm used in a robust taper design [2], we have developed and implemented the iterative robust optimization algorithm as shown in the left blocks in Figure 1. Rather than formulate the problem into a stochastic optimization problem as done in some previous work [3], we propose a more practical way. The optimization problem runs iteratively, with added robust constraints in each iteration. Thus, the optimization problem size grows, resulting in a more and more robust system. Relying on an existing optimization solver, we can solve the growing problem efficiently. As an example, a two-stage op-amp could be designed with robustness within minutes. The left flow in Figure 1 shows an outer loop around the iterative algorithm to generate a yield-aware design. The algorithm starts from a design with small process-variation range and we estimate the yield. The variation ranges keep growing until the yield reaches the desired value. This approach could enable rapid generation of trade-off surfaces for desired circuit blocks, parameterized by yield.



▲ Figure 1: Robust optimization problem formulation and the iterative robust optimization algorithm as shown on the left. Block diagrams on the right show the yield estimation flow.

References

[1] M. Hershenson, S.P. Boyd, and T.H. Lee, "Optimal design of a CMOS op-amp via geometric programming," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and System*, vol. 20, no. 1, pp. 1-21, Jan. 2001.

[2] A. Mutapcic and S. Boyd, "Robust design of slow-light tapers in periodic waveguides," to appear in *Engineering Optimization*, 2008.

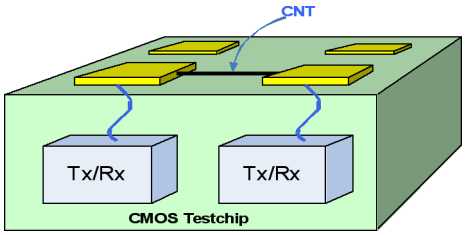
[3] Y. Xu, X. Li, K. Hsiung, S. Boyd, and I. Nausieda, "OPERA: optimization with ellipsoidal uncertainty for robust analog IC design," in *Proc. of the 42nd Design Automation Conference*, pp. 632-637, June 2005.

On-chip, High-frequency Characterization of Carbon Nanotubes

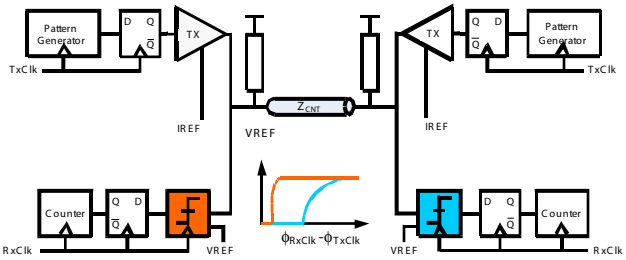
F. Chen, A.P. Chandrakasan, V. Stojanović
Sponsorship: SRC/FCRP IFC

Measuring the high-frequency characteristics of nanoscale devices such as CNTs and nanowires is a critical step in determining their viability for semiconductor applications [1]. Previous efforts to measure high-frequency characteristics of CNTs have been limited by a handful of common problems. First, the traditional approach of using a network analyzer (VNA) to capture the frequency response is limited by the poor power transfer between the high impedance (> 10 kΩ) of the device and the 50 Ω test equipment termination). This impedance mismatch offsets the selective bandwidth of the VNA used to reduce the noise floor, resulting in a large variance of measured data due to signals being at or near the noise floor. Second, measurement parasitics from test probes and pads often dominate the reactance of the CNTs being measured, limiting both the accuracy of the results and the bandwidth of the measurement. Third, given the dimensions of CNTs, test setups are difficult to reproduce, limiting the range of lengths and number of CNTs that can be measured.

To address these issues, we have developed an on-chip test platform consisting of an array of 256 transceivers. Figure 1 shows a conceptual drawing of the CNT to CMOS test chip interface. Under each pad in the array is a transceiver that is independent of all others, allowing for measurement between any two pads in the array. Figure 2 shows the top level block diagram of two transceivers linked by a CNT "channel." Similar to [2] but with mostly on-chip components, the step response of the channel is captured by changing the threshold voltage of the sampler (VREF) and the relative phase of the receiver clock (RxClk) with respect to the transmit clock (TxClk). Each transceiver has an adjustable termination and employs a capacitance compensation technique to allow full-sized bond pads for device characterization at the chip interface while maintaining input drive bandwidths up to 1GHz for a 4 kΩ termination. A 20-bit counter accumulates samples at each point, to average out timing noise due to jitter and any dynamic voltage offsets in the sampler.



▲ Figure 1: Conceptual drawing of the CNT to CMOS test chip interface.



▲ Figure 2: Block diagram of 2 transceivers linked by a CNT and conceptual waveforms captured by shifting VREF and RxClk.

References

[1] P.J. Burke, et al., "Nanotube technology for microwave applications," *Microwave Symposium Digest, 2005 IEEE MTT-S International*, June 2005, pp. 12-17.

[2] K. Soumyanath, et al., "Accurate on-chip interconnect evaluation: a time-domain technique," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 5, pp. 623-631, May 1999.

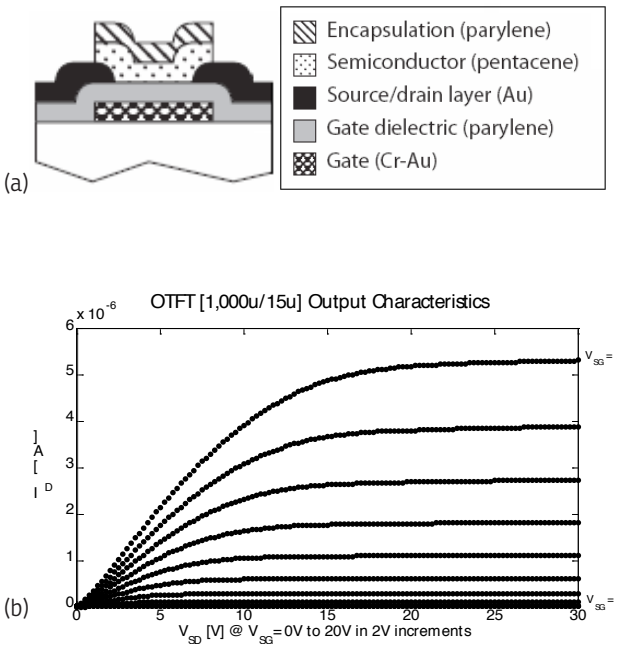
Organic Thin-film Transistor Integrated Circuits

D. He, I. Nausieda, K. Ryu, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2, Hewlett-Packard, NSERC Fellowship

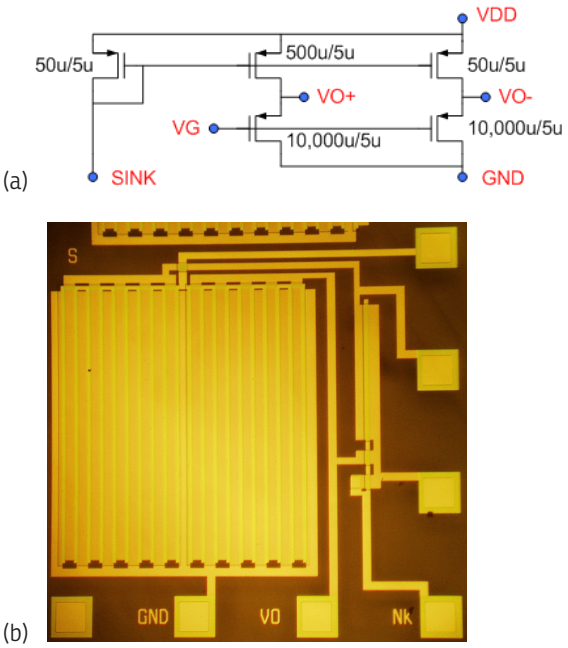
The organic thin-film transistor (OTFT) is a field-effect transistor technology that uses an organic material as the semiconductor. Electronically, OTFTs have field-effect mobilities that are comparable to those of hydrogenated amorphous silicon TFTs [1]. Mechanically, organic materials can be processed at room temperature, thus permitting substrates that are low-cost, large-area, and mechanically flexible [2]. We investigate the OTFT technology through device characterization and circuit design.

The OTFTs used in our work are lithographically processed at temperatures less than 95 ºC to produce integrated circuits compatible with mechanically-flexible substrates [3]. Figure 1a shows the OTFT device cross-section, with typical output characteristics in Figure 1b. **Device parameters such as threshold voltage, charge mobility,** subthreshold slope, and contact resistance are characterized and studied.

We design OTFT circuits to achieve two goals: to aid the understanding of device physics and to evaluate the feasibilities of various OTFT applications. One such circuit is the complementary-to-absolute-temperature (CTAT) circuit shown in Figure 2. The CTAT circuit promotes the study of thermally activated device mechanisms. At the same time, we use the circuit to explore highly-linear and low-power temperature-sensing applications. Another OTFT circuit is the 4×4 active-matrix imager, as described in [4]. Additional OTFT circuits include digital logic gates, ring oscillators, display pixel drivers, comparators, and static random-access memory cells.



▲ Figure 1: (a) OTFT device cross-section and (b) typical OTFT output characteristics.



▲ Figure 2: (a) CTAT circuit schematic and (b) its die micrograph (area of 1mm^2).

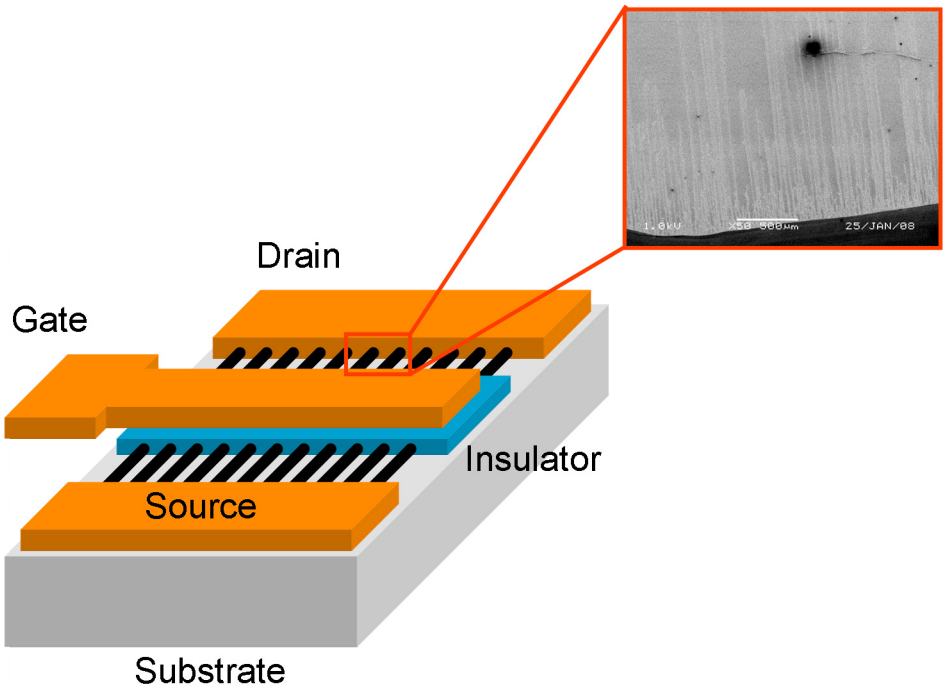
References

[1] Y.Y. Lin, D.J. Gundlach, and T.N. Jackson, "High-mobility pentacene organic thin film transistors," *Device Research Conference Digest*, June 1996, pp. 80–81.
[2] M. Chason, P.W. Brazis, J. Zhang, K. Kalyanasundaram, and D.R. Gamota, "Printed Organic Semiconducting Devices," *Proc. of the IEEE*, July 2005, pp. 1348–1356.
[3] I. Kymissis, C.G. Sodini, A.I. Akinwande, and V. Bulovic, "An organic semiconductor based process for photodetecting applications," *IEEE International Electron Devices Meeting Technical Digest*, Dec. 2004, pp. 377–380.
[4] I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulovic, and C.G. Sodini, "An organic imager for flexible large area electronics," *Digest of IEEE International Solid-State Circuits Conference*, San Francisco, Feb. 2007, pp. 72–73.

Design and Integration of Complementary CNT-FETs

K.-J. Lee, J. Kong, A.P. Chandrakasan
Sponsorship: SRC/FCRP IFC, Intel

The high mobility and nanometer-scale dimensions of carbon nanotubes (CNTs) make them attractive for many electronic applications. Experimental work has shown near-ballistic transport properties of CNT field-effect transistors (FET) [1] and demonstrated rudimentary circuit structures [2, 3]. While these efforts highlight the potential of CNT-FETs, improving device reliability and large-scale integration schemes remains a big challenge. This project investigates the fabrication process of complementary CNT-FETs. Similar to [3, 4], CNT-FETs are fabricated by first growing high-density, aligned CNTs via chemical vapor deposition. As-grown CNTs have a mixture of metallic and semiconducting CNTs, which significantly degrades the on-off current ratio. This mixture can be improved by electrically burning metallic CNTs. Then, device parameters are optimally tuned by high-K gate insulator deposition and metal-gate engineering [2]. This project examines device reliability, design trade-offs, and the integrity of the process flow.



▲ Figure 1: Schematic of a CNT-FET with metal-gate on top of a high-K gate insulator. A single device consists of many CNTs. An SEM micrograph shows high-density, aligned CNTs grown from a thick catalyst region at the bottom of the image.

References

[1] A. Javey, J. Guo, M. Paulsson, Q. Wang, D. Mann, M. Lundstrom, and H. Dai, "High-field quasi-ballistic transport in short carbon nanotubes," *Physics Review Letter*, vol. 92, p. 106804, Mar. 2004.

[2] Z. Chen, J. Appenzeller, Y.-M. Lin, J. Sippel-Oakley, A.G. Rinzler, J. Tang, S.J. Wind, P.M. Solomon, and P. Avouris, "An integrated logic circuit assembled on a single carbon nanotube," *Science*, vol. 311, no. 5768, p. 1735, Mar. 2006.

[3] P.-W. Chiu and C.-H. Chen, "High-performance carbon nanotube network transistors for logic application," *Applied Physics Letters*, vol. 92, p. 063511, Feb. 2008.

[4] S.J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M.A. Alam, S.V. Rotkin, and J.A. Rogers, "High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes," *Nature Nanotechnology*, vol. 2, pp. 230-236, Mar. 2007.

Optimization of Transistors for VHF Resonant Power Converters

A. Sagneri, D.J. Perreault

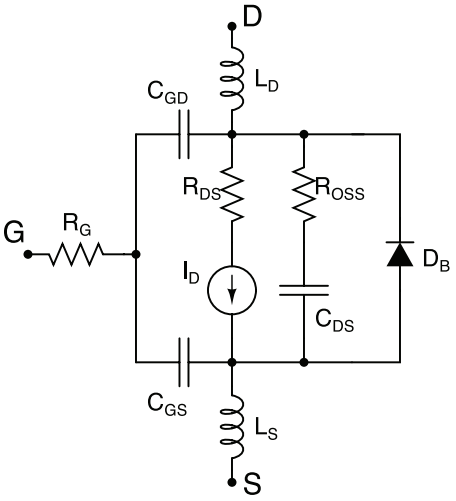
Sponsorship: National Semiconductor Corporation, NSF, CICS

At current switching frequencies (about 1-10 MHz), the required energy storage in a typical dc-dc converter yields passive component dimensions that are large with respect to integrated processes. A continuing effort to switch in the VHF regime (30-300 MHz) has relaxed this restriction, eliminating the need for magnetic materials and reducing component sizes to the point where integration or co-packaging is feasible [1-4]. A prototype boost converter operating at 110 MHz, with an 8-18V input and a 33V, 23W output achieved better than 87% efficiency using an off-the-shelf RF power LDMOSFET [4]. The need for lower cost and integrated switches prompted experiments with LDMOSFETs fabricated using an integrated power process. These prototypes operate at 50 MHz over similar voltage and power ranges, but with roughly 12% lower efficiency [2].

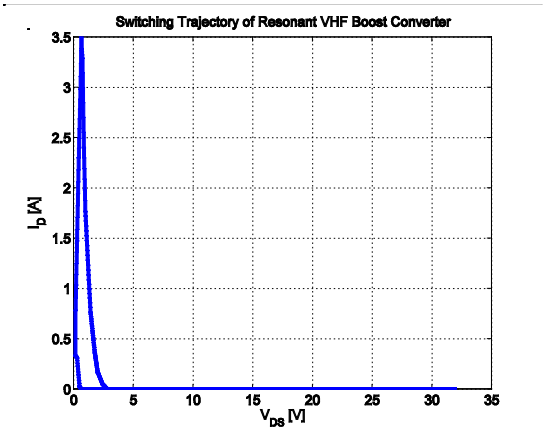
The present work shows that optimization of device layout, without changes to the underlying process or its design rules, leads to significant improvement in integrated LDMOSFET performance. Layout optimization is accomplished by creating a device model in Matlab that relates device parasitic elements and on-state resistance to layout geometry, as in Figure 1. A search of the design space bounded by layout rules yields the best performing device. It was possible, for example, to reduce gate resistance by a factor of three using this technique.

The ability to operate these devices above their typical breakdown voltage limits allows further performance gains. For LDMOSFETs, hot-carrier effects usually set the breakdown voltage [5]. In VHF power converters, soft-switching provides minimal voltage and current overlap, as Figure 2 shows, thereby avoiding the hot-carrier regime. Therefore, operation closer to the avalanche breakdown limit is possible. This allows for a shorter drain extension at a given breakdown voltage, conferring smaller parasitic capacitance and lower specific on resistance. Testing has validated the use of a device usually rated for 20 V at up to 35 V with appropriate topologies.

Prototype converters built using these optimized devices achieve efficiencies on par with those using commercial RF LDMOS devices, or roughly 88% drain efficiency for an overall converter efficiency of 85-86%.



▲ Figure 1: MOSFET model detailing loss mechanisms important at VHF. In particular, losses in R_{OSS} and R_G represent displacement loss and gating loss, both frequency-dependent mechanisms that can be influenced favorably by optimizing the layout geometry.



▲ Figure 2: Switching trajectory of a resonant dc-dc boost converter. Voltage and current are never simultaneously large. This allows hot-carrier effects to be largely neglected when determining maximum allowable switch operating voltage.

References

[1] J.M. Rivas, R.S. Wahby, J.S. Shafran, and D.J. Perreault, "New architectures for radio-frequency dc-dc power conversion," in *Proc. 35th Annual IEEE Power Electronics Specialist Conference*, Aachen, Germany, June 2004, pp. 4074-4084.

[2] A.D. Sagneri, "The design of a VHF dc-dc boost converter," Master's thesis, Massachusetts Institute of Technology, Cambridge, 2007.

[3] J.M. Rivas, "Radio frequency dc-dc power conversion," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2006.

[4] R. Pilawa, A.D. Sagneri, J.M. Rivas, D. Anderson, and D.J. Perreault, "Very high-frequency resonant boost converters," in *Proc. 38th IEEE Power Electronics Specialist Conference*, Orlando, FL, June 2007.

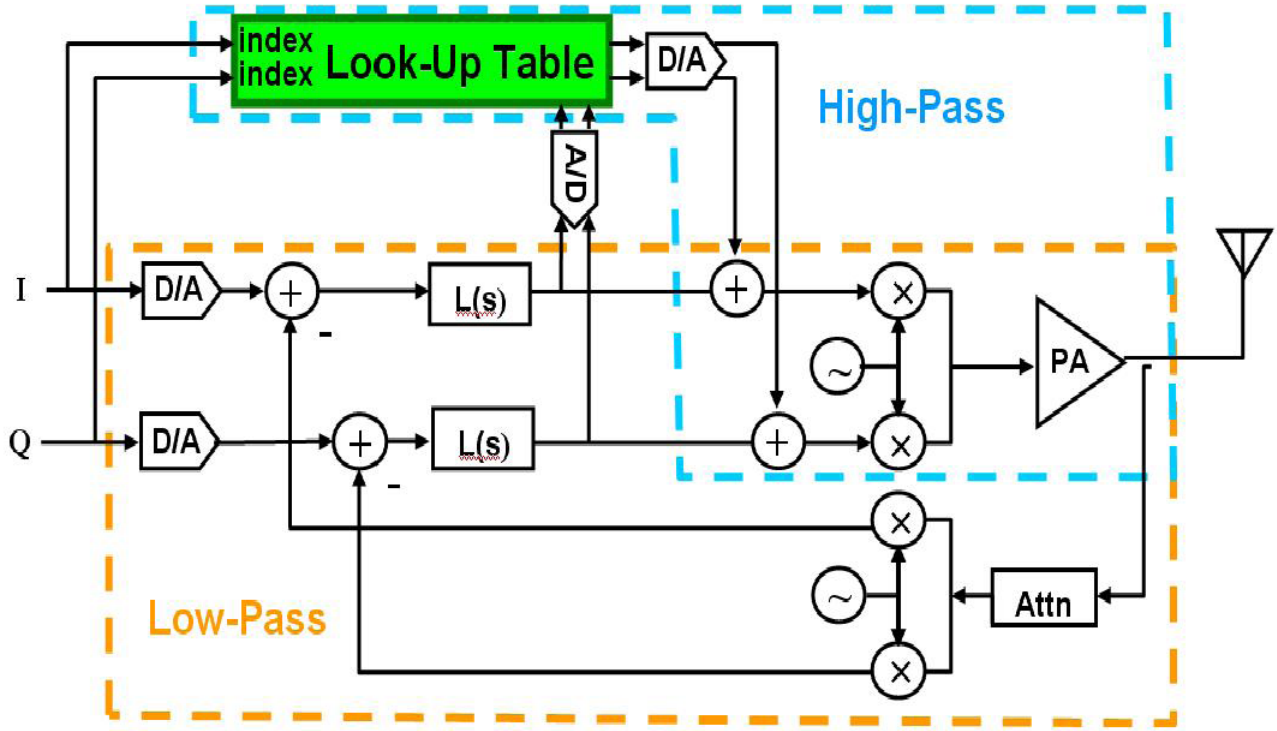
[5] A. Hastings, *The Art of Analog Layout*. New Jersey: Prentice-Hall, Inc., 2001.

Two-point Wideband Linearization of RF Power Amplifiers for Memory Compensation

H. Boo, S. Chung, J.L. Dawson

Linearizing RF power amplifiers (PAs) has become a very challenging issue in RF design. The PAs are known for their nonlinear behavior and distortion emissions. High data rates and envelope variations in communication systems impose severe wideband linearity requirements on the PA. Also, at high power levels, memory effect, frequency-dependent distortion, comes into effect. Previous work on Cartesian Feedback (CFB) offers high linearization while also suppressing memory effect. However, the loop dynamics inherently limit its application to low bandwidth transmission. Digital predistortion (DPD) relies on baseband symbol mapping using a look-up table to predistort symbols; the mapping implements the inverse of the PA nonlinearity. Although the technique allows wide bandwidth transmission, it cannot compensate for memory effect since the look-up table does not model the constantly changing behavior of the PA.

We consider a two-point linearization system in which a CFB and DPD are combined to linearize the PA for high bandwidth transmission with memory-effect compensation. The CFB path takes care of the low bandwidth portion while suppressing the memory effect, and the DPD covers the high frequency range while suppressing the memoryless nonlinearity. The two-point architecture offers linearization without any complex PA modeling or the use of power-hungry DSP.



▲ Figure 1: Two-point architecture that combines CFB and DPD for PA linearization. The architecture enables high bandwidth transmission, in addition to suppressing memory effect.

References

[1] S. Chung, J.W. Holloway, and J.L. Dawson, "Open-loop digital predistortion using Cartesian feedback for adaptive RF power amplifier linearization," *IEEE MTT-S International Microwave Symposium*, Honolulu, HI, June 2007.

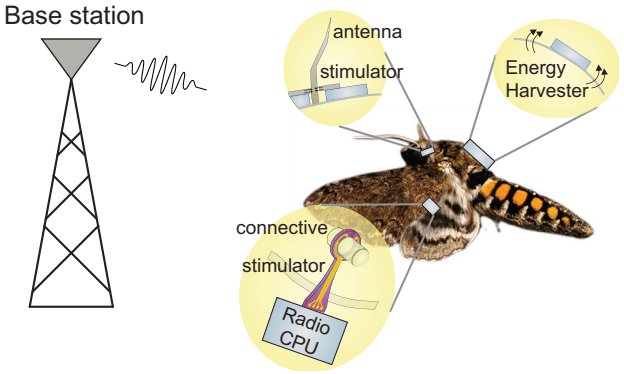
[2] C. Cohen-Tannoudji, J. Dupont-Roc, and G. Grynberg, *Atom-photon Intereactions*. New York: John Wiley & Sons, Inc., 1992.

Energy-efficient Pulsed-UWB Transceiver for Insect Flight Control

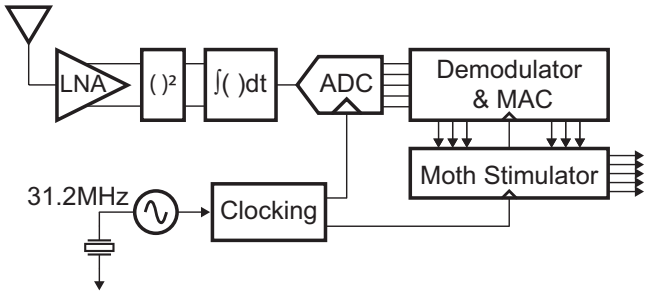
D.C. Daly, P.P. Mercier, M. Bhardwaj, A.P. Chandrakasan
Sponsorship: DARPA, NSERC, STMicroelectronics

Due to continued process improvement and miniaturization of electronics, complex highly integrated systems can now be realized on the micro-scale. Micro-scale electronics and micro-electromechanical systems (MEMS) are particularly relevant for biomedical and biological applications, in which devices are often implanted within or on organisms. An emerging application for micro-scale electronics is hybrid-insect flight control, where MEMS devices are placed on and within insects to alter flight direction. Such a hybrid insect system would take the best qualities of biology — energy storage, efficient flight control, highly adapted sensing — and combine them with the best qualities of MEMS — low weight, small size, deterministic control, and interfacing with computation. Figure 1 presents an overview of the moth flight control system being developed in collaboration with other scientists and researchers at MIT, the University of Washington, and the University of Arizona.

A critical component of the hybrid-insect system is the wireless communication link, which provides flight control commands to the moth. Pulsed ultra-wideband (UWB) wireless signaling is employed as UWB radios can achieve highly integrated, energy-efficient operation in nanometer CMOS processes [1, 2]. Power, weight and volume are all highly constrained, necessitating a highly integrated solution with minimal off-chip components. To reduce power requirements and system complexity, communication is unidirectional from the base station to the moth. Data is transmitted by PPM modulation in one of three 500-MHz channels in the 3-5-GHz band. The highly digital base station transmitter consumes zero static bias current and achieves an energy efficiency of 113-to-19pJ/pulse at data rates from 100kbps-to-15.6Mbps [3]. The moth receiver consists of a packaged chip along with an off-chip crystal resonator to provide a stable clock. Figure 2 presents a block-diagram of the system-on-chip for the hybrid-insect wireless receiver. The non-coherent receiver amplifies, squares, and integrates received pulses to measure the amount of energy received in a given time period. A highly parallelized demodulator detects packets and rapidly synchronizes and receives payload data. The moth stimulator supplies a digital, pulse-width modulated signal to eight channels to control flight direction.



▲ Figure 1: Overview of hybrid-insect flight control system (Moth image courtesy of Armin Hinterworth).



▲ Figure 2: Block diagram of the wireless receiver for the moth.

References

[1] F.S. Lee and A.P. Chandrakasan, "A 2.5nJ/b 0.65V 3-to-5GHz sub-banded UWB receiver in 90nm CMOS," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2007, pp. 116-117.

[2] D.D. Wentzloff and A.P. Chandrakasan, "A 47pJ/pulse 3.1-to-5GHz all-digital UWB transmitter in 90nm CMOS," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2007, pp. 118-119.

[3] P.P. Mercier, D.C. Daly, and A.P. Chandrakasan, "A 19pJ/pulse UWB Transmitter with Dual Capacitively-Coupled Digital Power Amplifiers," presented at the *IEEE Radio Frequency Integrated Circuits Symposium*, June 2008.

Wideband Polar Transmitter for Multi-standard Communications

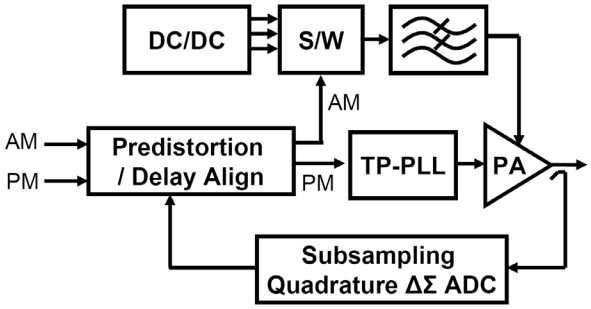
S. Chung, P. Godoy, S. Rayanakorn, D.J. Perreault, J.L. Dawson
Sponsorship: Deshpande Center for Technological Innovation

This work focuses on implementing an RF transmitter that is suitable for multi-standard transmission without the need for an array of bulky, impossible-to-integrate filters. Polar transmitters have long been recognized as having a fundamental advantage in this regard [1]. However, many challenges must be overcome to put polar transmitters into use; these challenges divide into three main parts: (1) a wideband, highly efficient amplitude modulator, (2) a wideband phase modulator, and (3) the predistortion/time alignment circuitry.

To achieve high-efficiency amplitude modulation, a switching-mode DC/DC converter whose switching frequency is several times the signal bandwidth, is typically used. However, the converter efficiency is severely degraded for wideband signals due to increased switching losses [2]. To overcome this difficulty, we use only a few discrete amplitude values in the DC/DC converter. We can do this by leveraging the fact that most modulation schemes are digital and require only discrete signal amplitudes (e.g., for QAM-16, only three amplitude levels are possible.). A low-pass filter shapes the resulting signal spectrum to meet spectral mask requirements.

A two-point modulator performs the wideband phase modulation [3]. It is a phase-locked loop (PLL) with two input paths. The first input path is low-pass-filtered to the output by the closed-loop transfer function of the PLL, whereas the second input path is high-pass-filtered to the output. In theory, the bandwidth of the two-point modulator is unbounded. However, nonlinearity in the voltage-controlled oscillator introduces significant phase errors in the second data path. These phase errors are corrected with an adaptive digital predistortion circuit, similar to that applied to power amplifiers [4].

The wideband predistortion [4] is necessary to linearize a highly power-efficient but nonlinear switching power amplifier. The time-delay alignment compensates for the delay difference between the amplitude path and the phase path.



▲ Figure 1: Polar transmitter architecture.

References

[1] E. McCune, "Advanced architectures for high-efficiency, multi-mode, multi-band terminal power amplifiers," *IEEE Radio and Wireless Conference*, pp. 167-170, Sept. 2004.

[2] F. Wang, D.F. Kimball, D.Y. Lie, P.M. Asbeck, and L.E. Larson, "A monolithic high-efficiency 2.4-GHz 20-dBm SiGe BiCMOS envelope-tracking OFDM power amplifier," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1271-1281, June 2007.

[3] K.C. Peng, C.H. Huang, C.J. Li, and T.S. Horng, "High-performance frequency-hopping transmitters using two-point delta-sigma modulation," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 52, no. 11, pp. 2529-2535, Nov. 2004.

[4] S. Chung, J.W. Holloway, and J.L. Dawson, "Open-loop digital predistortion using Cartesian feedback for adaptive RF power amplifier linearization," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1449-1452, June 2007.

A Low-jitter Programmable Clock Multiplier Based on a Pulse Injection-locked Oscillator

B. Helal, M.H. Perrott

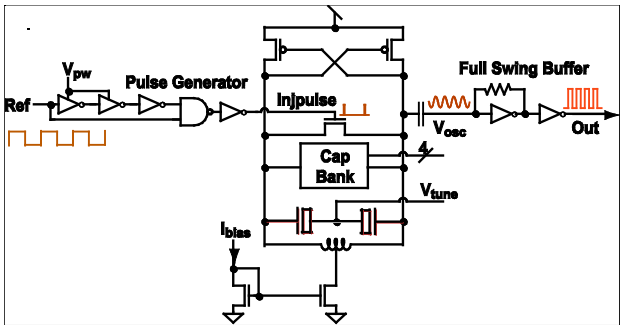
Sponsorship: NSF, CICS

Recently, there has been an increased interest in CMOS circuits that leverage injection-locked oscillators for applications such as frequency division and clock multiplication. Clock multiplication using subharmonic injection-locked oscillators [1] has the potential advantage of suppressing the phase noise of the oscillator at a significantly higher bandwidth than integer-N Phase-Locked Loops (PLLs), which are typically used for clock multiplication. However, the lack of continuous tuning of the injected oscillator necessitates a large injection power to ensure locking over sufficient bandwidth. Even when an Injection-Locked Phase-Locked Loop (ILPLL) provides continuous tuning [2], increased frequency spurs can result due to the mismatch between the injection and the PLL paths and the typical analog nature of the tuning path. A similar issue occurs with realigned PLLs as described in [3].

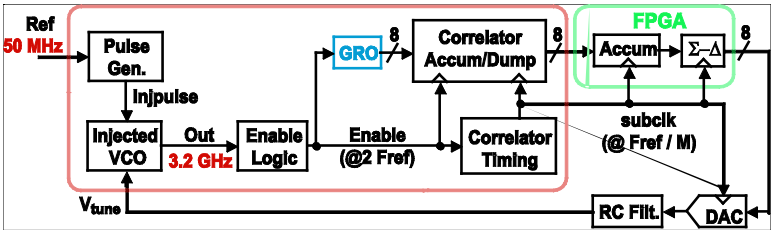
This research aims to develop a subharmonic injection-locked architecture that is continuously tuned with low frequency-spurs and significantly lower output jitter than a typical PLL. We propose a Pulse Injection-Locked Oscillator (PILO)that is suitable for continuous tuning using a highly-digital tuning technique that we recently introduced [4]. In addition, the operation of the PILO can be more intuitively understood than typical injection-locked techniques and a linearized context can be used to model its phase noise using [3].

Figure 1 shows the proposed PILO circuit in which the LC tank of the oscillator is frequency locked by periodically shorting the tank with a switch that is driven by a train of narrow pulses. The pulses are generated from a reference source, whose frequency is at a sub-multiple of the desired output frequency. To achieve low output jitter, the reference source must also have low jitter since its noise will be mostly passed on to the oscillator output [3].

Figure 2 shows the prototype of the proposed highly-digital PILO architecture that offers continuous frequency tuning of the injection-locked oscillator and eliminates sources of analog mismatches in the tuning path. The cornerstones of the tuning technique are a digital correlation technique and a scrambling time-to-digital converter (TDC). The architecture eliminates mismatches and offsets in analog detection and integration blocks by using a single detection path and replacing the charge pump and analog integrator with a digital accumulator [4]. A test chip was fabricated using a CMOS 0.13 µm process, and the prototype used a 50 MHz reference input to generate an output at 3.2 GHz (and up to 4 GHz). For the 3.2 GHz output, measured results demonstrated overall reference spurs of -63.4 dBc and estimated random and deterministic jitter of 134 fs (rms) and 211 fs (peak-to-peak), respectively [5].



▲ Figure 1: Proposed PILO structure.



▲ Figure 2: PILO prototype and its highly-digital tuning circuit.

References

[1] H. Ahmed, C. DeVries, and R. Mason, "A digitally tuned 1.1 GHz subharmonic injection-locked VCO in 0.18 um CMOS," in *Proc. European Solid State Circuits Conference (ESSCIRC)*, Sept. 2003, pp. 81- 84.

[2] S. Kudszus, M. Neumann, T. Berceli, and W. Haydl, "Fully integrated 94-GHz subharmonic injection-locked PLL circuit," *IEEE Microwave Guided Wave Letters*, vol. 10, no. 2, pp. 70-72, Feb. 2000.

[3] S. Ye, L. Jansson, and I. Galton, "A multiple-crystal interface PLL with VCO realignment to reduce phase noise," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1795–1803, Dec. 2002.

[4] B. Helal, M. Straayer, G. Wei, and M. Perrott, "A highly-digital MDLL-based clock multiplier that leverages a self-scrambling time-to-digital converter to achieve sub-picosecond jitter performance," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 855 – 863, Apr. 2008.

[5] B. Helal, C.-M. Hsu, K. Johnson, and M. Perrott, "A Low-noise Programmable Clock Multiplier based on a Pulse Injection-locked Oscillator with a Highly-digital Tuning Loop," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium Digest of Papers*, Jun. 2008, pp. 423-426.

A 3.6-GHz Low-noise, 500-kHz BW Digital-frequency Synthesizer with Digital Noise Cancellation

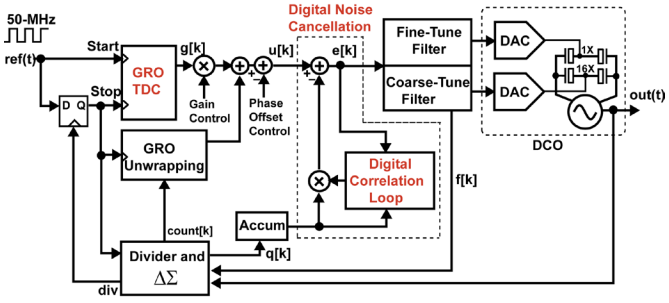
C.-M. Hsu, M.H. Perrott

Sponsorship: SRC/FCRP C2S2

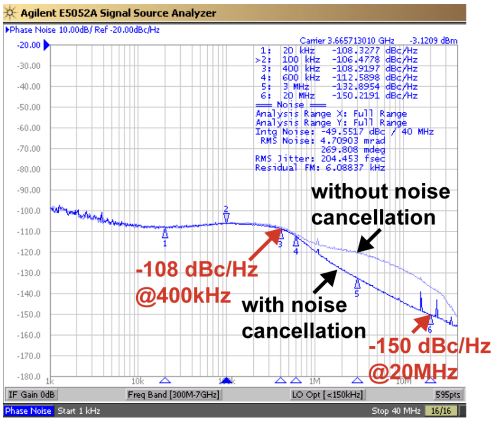
A digital fractional-N frequency synthesizer is presented that leverages a noise-shaping time-to-digital converter (TDC) and a simple quantization noise cancellation technique to achieve low phase noise with a wide PLL bandwidth of 500 kHz. In contrast to previous cancellation techniques, the proposed structure requires no analog components and is straightforward to implement with standard cell digital logic. With the cancellation technique enabled, the synthesizer achieves phase noise of -132 dBc/Hz at 3 MHz offset, and an integrated phase noise from 1 kHz to 40 MHz of 204 fs rms at 3.67 GHz.

Figure 1 shows a block diagram of the proposed synthesizer. High-resolution digital phase detection is performed with an improved version of the gated ring oscillator (GRO) time-to-digital converter presented in [1]. Another interesting component of the architecture is an asynchronous frequency divider that avoids divide-value delay variation at its output. In addition, in contrast to previous digital PLL implementations [2], the digitally-controlled oscillator (DCO) is implemented as a conventional LC voltage-controlled oscillator (VCO) with coarse and fine varactors, which are controlled by two passive 10-bit, 50-MHz digital-to-analog converter (DAC) structures. An additional four-bit MIM capacitor bank is included in the VCO to improve its tuning range. To control both the coarse and fine varactors in the VCO, the loop filter consists of two paths.

The chip is implemented in a 0.13-μm CMOS process and has an active area of 0.95 mm². The prototype consumes 26mA from a 1.5V supply, excluding the VCO output buffer that consumes 7mA from a 1.1V supply. Figure 2 shows the measured phase noise at 3.67GHz from an Agilent Signal Source Analyzer E5052A, and the results are shown with and without cancellation of the quantization noise. As the figure reveals, greater than 15 dB noise cancellation is achieved such that the VCO dominates out-of-band noise. With noise cancellation enabled, the in-band noise is -108dBc/Hz at 400 kHz offset, and out-of-band noise is -132dBc and -150dBc at 3 MHz and 20 MHz offsets, respectively. The reference spur was measured with an Agilent Spectrum Analyzer 8595E to be -65dBc. Fractional spurs were first measured at carrier frequencies spanning from 3.620 GHz to 3.670 GHz in increments of 1MHz. With this setup, worst case spurs were measured to be -53dBc at carrier frequencies of 3.649 and 3.651GHz and -64dBc at carrier frequencies of 3.648 and 3.652GHz;, the spurs were less than -65 dBc at all the other carrier frequencies. When VCO frequency was set closer to 3.65GHz, the worst case spur was observed to be -42dBc when carrier frequency was at 3.6504GHz.



▲ Figure 1: Block diagram of proposed synthesizer.



▲ Figure 2: Measured phase noise performance.

References

[1] B. Helal, M. Straayer, G. Wei, and M. Perrott, "A Low-jitter 1.6-GHz Multiplying DLL Utilizing a Scrambling Time-to-digital Converter and Digital Correlation," *VLSI Symposium Digest of Technical Papers*, pp. 166-167, June 2007.

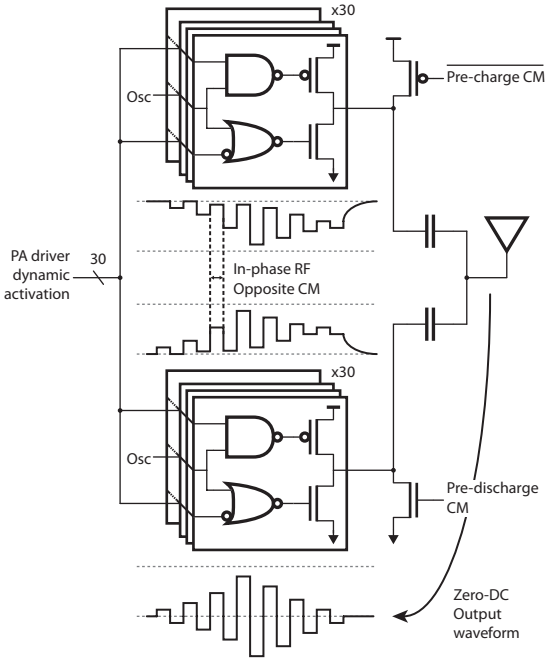
[2] R.B. Staszewski et al., "All-digital PLL and GSM/EDGE Transmitter in 90-nm CMOS," *ISSCC Digest of Technical Papers*, pp. 316-317, Feb. 2005.

An All-digital UWB Transmitter with Dual Capacitively-coupled Power Amplifiers

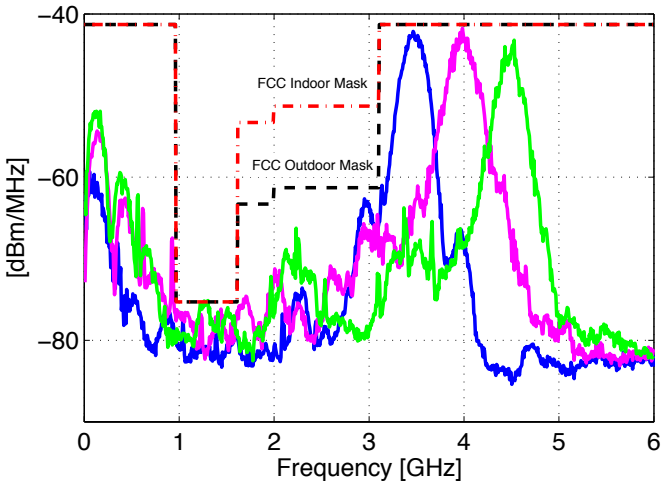
P.P. Mercier, D.C. Daly, A.P. Chandrakasan
Sponsorship: DARPA, NSERC, STMicroelectronics

Applications like sensor networks, medical monitoring, and asset tracking have led to a demand for energy-efficient and low-cost wireless transceivers. These types of applications typically require low effective data rates, thus providing an opportunity to employ simple modulation schemes and aggressive duty-cycling. Due to their inherently duty-cycled nature, pulsed-UWB systems have been shown to be amenable to low-power operation [1, 2]. Furthermore, the use of non-coherent signaling greatly simplifies both transmitter and receiver implementations, offering substantial energy savings [3].

This work presents an all-digital transmitter designed for a non-coherent pulsed-UWB system [4]. By exploiting the fact that center frequency tolerances are relaxed in wideband non-coherent communication, the transmitter can synthesize UWB pulses from an energy-efficient, single-ended digital ring oscillator. To generate phase modulated pulses (which are required for spectral scrambling purposes), the oscillator output is fed to two banks of parallel tri-state inverters, shown in Figure 1. Maintaining opposite common modes at the output of these inverters during idle mode (i.e., when no pulses are being transmitted) eliminates low-frequency turn-on and turn-off transients typically associated with single-ended digital circuits driving single-ended antennas. Thus, no area-expensive balun is required to generate BPSK-modulated pulses. The parallel inverter banks permit digital pulse-shaping, resulting in on-chip FCC-compliant operation, as Figure 2 shows. The transmitter was fabricated in 90-nm CMOS, consumes zero static bias current, and achieves an energy efficiency of 113-to-19pJ/pulse at data rates from 100kbps-to-15.6Mbps.



▲ Figure 1: Dual-digital power amplifiers create a bi-polar (zero-DC) output pulse by combining paths that are in-phase at RF yet have counter-phase common-mode components that are cancelled.



▲ Figure 2: Output spectral densities in three channels, from 3.5-to-4.5 GHz, illustrating on-chip FCC compliance.

References

[1] F.S. Lee and A.P. Chandrakasan, "A 2.5nJ/b 0.65V 3-to-5GHz Sub-banded UWB Receiver in 90-nm CMOS," in *Proc. IEEE International Solid-State Circuits Conference*, Feb. 2007, pp. 116-117.

[2] D.D. Wentzloff and A.P. Chandrakasan, "A 47pJ/pulse 3.1-to-5GHz All-digital UWB Transmitter in 90-nm CMOS," in *Proc. IEEE International Solid-State Circuits Conference*, Feb. 2007, pp. 118-119.

[3] L. Stoica, A. Rabbachin, H. Repo, S. Tiuraniemi, and I. Oppermann, "An ultra-wideband system architecture for tag-based wireless sensor networks," *IEEE Transactions on Vehicular Technology*, vol. 54, pp. 1632-1645, Sept. 2005.

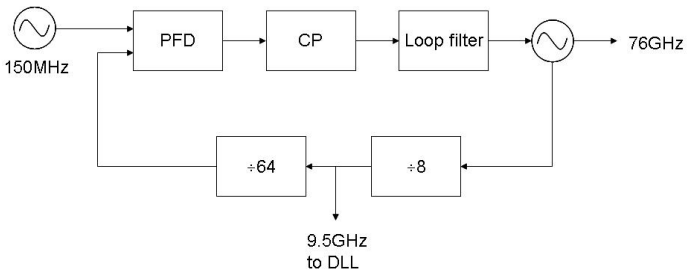
[4] P.P. Mercier, D.C. Daly, and A.P. Chandrakasan, "A 19pJ/pulse UWB Transmitter with Dual Capacitively-coupled Digital Power Amplifiers," in *Proc. IEEE Radio Frequency Integrated Circuits Symposium*, Jun. 2008.

Phase-locked Loop Design for Millimeter-wave Imaging

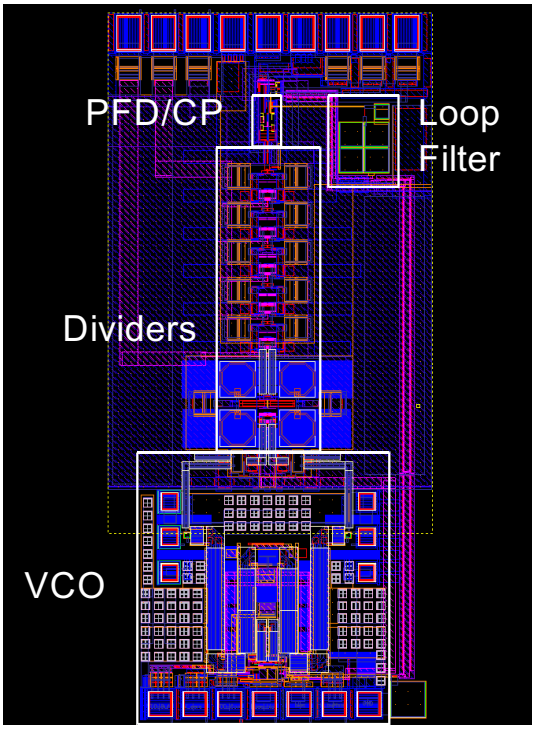
K.M. Nguyen, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

Millimeter-wave imaging has potential applications such as collision-avoidance radar at 77 GHz and concealed weapons detection at 77 GHz, 94 GHz, and higher. This research investigates the challenges of designing a phase-locked loop (PLL) that could be used in a millimeter-wave (MMW) imaging system. We envision an active imaging receiver that will consist of an array of 1000 antenna and per-antenna processor (PAP) units with an operating frequency of 77 GHz [1]. A central processor will perform digital beamforming on the aggregated data from the array to achieve an expected frame rate of 10 fps. The 77-GHz input signal will be downconverted by a mixer with a 76-GHz local oscillator, generated by the PLL, to obtain an intermediate frequency (IF) of 1-GHz. This signal is digitized by an analog-to-digital converter that is operating at 4.75 GHz and is sent to the CPU.

Since accurate beamforming requires tight control of the phase over the array of elements to prevent blurring between pixels, the PLL will be designed for minimal phase noise and power dissipation. The PLL will provide a pure 76-GHz tone for the imaging system. Figure 1 shows a block diagram of the PLL that was designed in 130-nm silicon-germanium (SiGe) BiCMOS process. A low phase noise 150-MHz crystal oscillator will be used as the reference. The PLL bandwidth was chosen to be 5 MHz to balance the phase noise caused by the voltage controlled oscillator (VCO) and the charge pump. The 76-GHz VCO is based on the cross-coupled design used in the passive imager [2]. The divider chain consists of nine divide-by-2 static frequency dividers. The first six are created in emitter coupled logic and the last three are designed in CMOS. The highest frequency divider utilizes inductive peaking for increased operating frequency. In simulation, the core PLL consumes 130mW and the buffers consume 45mW from a 2.5V supply. Figure 2 shows the layout of the test chip containing the full PLL that was submitted for fabrication in December 2007.



▲ Figure 1: Block diagram of the 76-GHz PLL.



▲ Figure 2: Layout of 76-GHz PLL that was submitted in December 2007 in a 130-nm SiGe BiCMOS process. The die dimension is 2mm x 1mm.

References

[1] A. Accardi, "Digital Compensation in Imaging Systems," Dissertation proposal, Massachusetts Institute of Technology, Cambridge, 2007.
[2] J. Powell and C.G. Sodini, "A 77-GHz Receiver Front-end for Passive Imaging," presented at the *Radio Frequency Integrated Circuits Symposium*, June 2007.

Digital Phase Tightening for Improved Spatial Resolution in Mm-wave Imaging Systems

K. Lu, C.G. Sodini

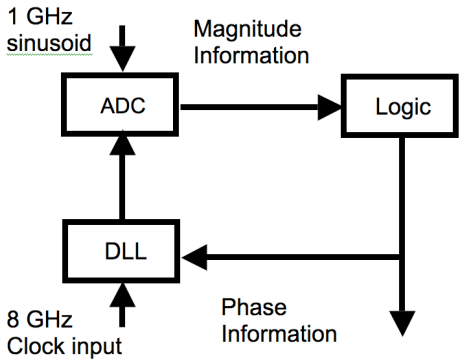
Sponsorship: Lincoln Laboratory

Due to advances in silicon and digital processing technology, millimeter-wave (MMW) imaging solutions with high antenna array density are now viable at a low cost [1]. Millimeter resolution is desirable for many applications, such as automotive collision avoidance and concealed weapons detection.

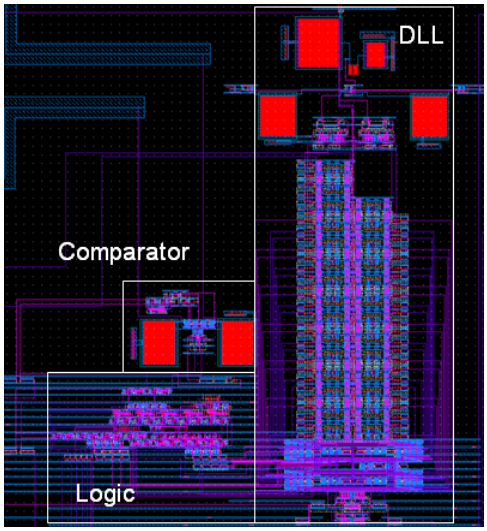
An MMW imaging system utilizes an antenna array to capture the image. Each array node records magnitude and phase information, which then can be combined via a beamforming process to estimate the radiation incident from a particular direction, according to a beam pattern [2]. The beam can be steered electronically to acquire different regions of the target image. Unconstrained by the physics of a lens, digital image formation provides a greater level of computational flexibility. Unfortunately, this places a very stringent specification on the amount of timing jitter in the system. Using digital phase tightening can alleviate this problem.

Figure 1 shows the system used for digital phase tightening of the antenna array. The system extracts the phase and magnitude information from the input signal, which is approximately a 1 GHz sinusoid. After many cycles, this system locks onto the maxima, the minima and the zero crossings of the input. The outputs from the logic carry the phase information, while the outputs from the ADC carry the magnitude information. These outputs, gathered from each antennae array node, are used to calculate the image.

We are designing a system that is easy to manufacture and scale, and for which the control of phase is totally in the digital domain. Figure 2 shows a screenshot of the layout of a prototype system. The design is currently being fabricated in a 90-nm CMOS process.



▲ Figure 1: Block diagram of overall system.



▲ Figure 2: Screenshot of the chip in layout with key blocks highlighted.

References

[1] W. Simburger et al., "Silicon-based RF ICs up to 100 GHz: Research trends and applications," in *Proc. Solid-State and Integrated Circuits Technology*, 2004, pp. 1:12-19.

[2] A. Accardi, "Digital Compensation in Imaging Systems," Ph.D. thesis proposal, Massachusetts Institute of Technology, Cambridge, 2007.

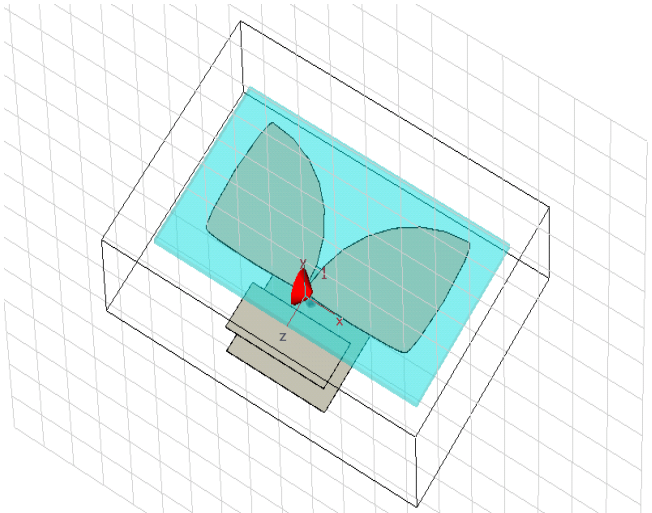
77- and 94-GHz Front-end Receivers with Flip-chip Antenna for MM-wave Imaging

J. Powell, H. Kim, C.G. Sodini
Sponsorship: SRC/FCRP C2S2, Lincoln Laboratory

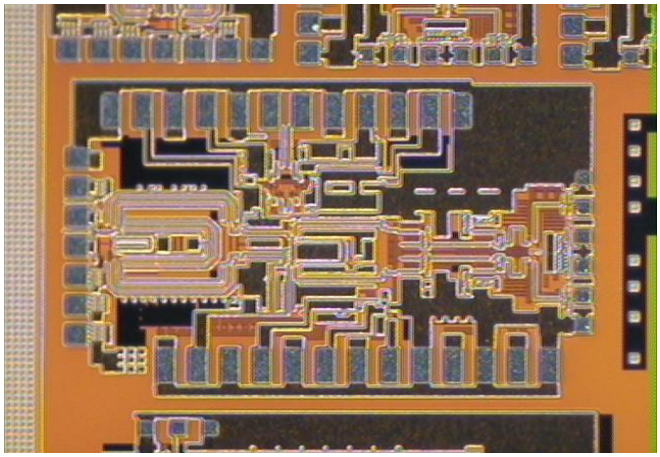
The area of Millimeter-wave (MMW) system research and design has become increasingly popular in recent years, as advanced silicon processes have enabled integrated circuit operation in the MMW regime. Several applications exist for MMW design, including wireless communications at 60-GHz, collision-avoidance radar imaging at 77-GHz, and concealed weapons detection at 77-GHz and higher. Significant advances have been made in these areas using SiGe technology [14]. This research focuses on passive imaging front-end receivers that have been developed and tested for the application of concealed weapons detection.

In this research, 77- and 94-GHz front-end receivers with antennas have been designed. Compared with current MMW research, these systems are wideband receivers that are fully differential. The RF front-ends are composed of low-noise amplifiers (LNA) and double-balanced mixers that downconvert the RF frequency to the intermediate frequency (IF) range of 1-9 GHz. The 77-GHz front-end also incorporates an on-chip cross-coupled voltage controlled oscillator (VCO). The antenna design is a Vivaldi-type antenna, designed for wideband performance. The antenna will be connected to the RF front-end via a flip-chip method. Gold solder bumps will be used to fuse the antenna to the receiver chips. Figure 1 shows a conceptual design of the MMW antenna.

Figure 2 shows the integrated 77-GHz RF front-end receiver implemented in 0.13 um SiGe. It achieves a particularly impressive maximum conversion gain of 46 dB. The full conversion gain ranges from 38-46 dB, and NF ranges from 6.5-10 dB within the IF frequency band of 1-9 GHz. The P1dB is approximately -38 dBm at 76 GHz RF.



▲ Figure 1: Vivaldi-type MMW antenna, designed in CST Microwave Studio.



▲ Figure 2: Photo of 77-GHz Front-end receiver die.

References

[1] J. Powell, H. Kim, and C. Sodini, "A 77-GHz front-end receiver for passive imaging," *Proc. RFIC*, June 2007, Honolulu, HI, pp. 145-148.
[2] B.A. Floyd, S.K. Reynolds, U. Pfeiffer, and T. Beukema, "SiGe bipolar transceiver circuits operating at 60 GHz," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005.
[3] S. Reynolds, et al., "Progress toward a low-cost millimeter-wave silicon radio" (Invited), *Proc. IEEE CICC*, Sept. 2005, pp. 563-570.
[4] A. Natarajan, et al., "A silicon-based 77-GHz transmitter with local LO-path phase shifting," *Proc. ISSCC*, Feb. 2006, pp. 182-183.

Noise-shaping Gated-Ring Oscillator Time-to-digital Conversion

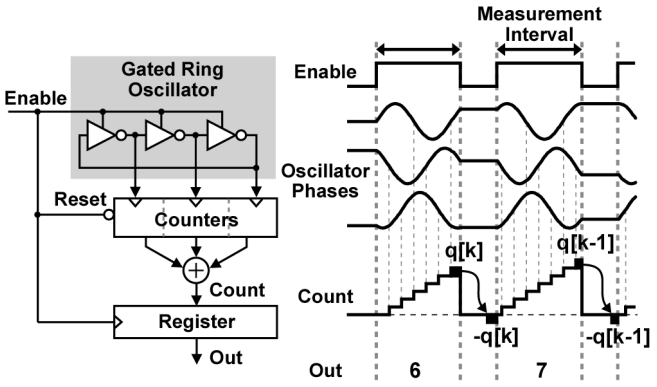
M. Straayer, M.H. Perrott
Sponsorship: Lincoln Laboratory

High-performance oversampling and feedback applications, such as phase-locked loops, delay-locked loops, and clock-and-data recovery loops, utilize time-to-digital converters (TDC) as fundamental building blocks that bridge the gap between analog and digital signal domains. In this work, we fully utilize the inherent low-pass filtering action of these systems by providing first-order noise-shaping within a gated-ring oscillator time-to-digital converter.

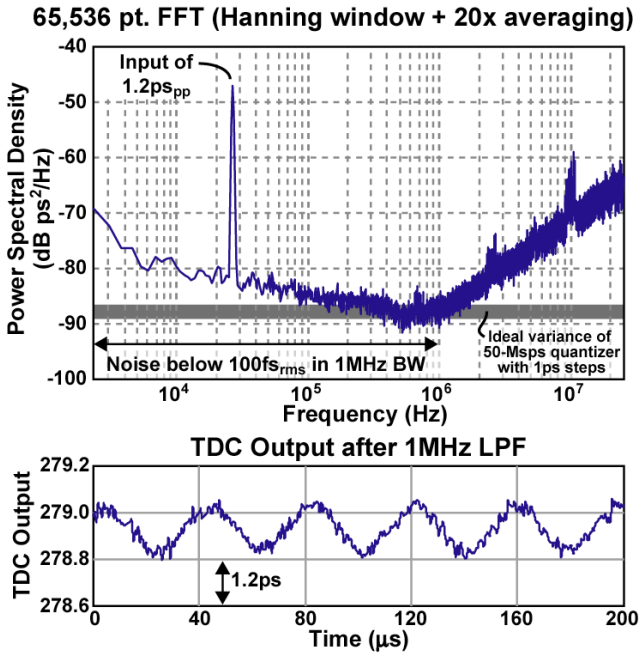
As Figure 1 shows, the gated-ring oscillator TDC is enabled during the measurement interval, and the transitions that occur for that measurement are counted and summed. At the end of each measurement interval, the oscillator is disabled, and the state of the oscillator is held until the next input sample. The preservation of oscillator state transfers the quantization error from one sample to the next, which results in a first-order difference equation on the quantization error, or equivalently first-order noise-shaping in the frequency domain [1].

A prototype 11-bit GRO-TDC was designed and fabricated in 0.13-um CMOS [2]. The 1x1mm chip with 20 pads has an active area of only 157x258um (0.04mm2). A 1.5-V supply used for measurements results in a raw TDC resolution equal to 6ps, and operation was verified from 1.0-1.6V. Likewise, the sample rate is set to 50-Msps and verified over 100-Msps. Current is a linear function of the average measurement time, and it ranges from 1.5-14mA (2.2-21mW). Figure 2 shows a measurement of the TDC output with a 1.2ps(ppk) input signal at 26kHz. The rms timing jitter (measurement error) in a 1MHz bandwidth is below 100fs.

The authors wish to acknowledge MIT Lincoln Laboratory for research support through the Lincoln Scholars Program.



▲ Figure 1: Gated ring oscillator concept.



▲ Figure 2: Measured output for 1.2ps(ppk) 26-kHz input.

References

[1] B. Helal, M. Straayer, and M.H. Perrott, "A Low-jitter 1.6-GHz multiplying DLL utilizing a scrambling time-to-digital converter and digital correlation," *IEEE VLSI Symposium Digest of Technical Papers*, 2007.

[2] C.M. Hsu, M. Straayer, and M.H. Perrott, "A low-noise, wide bandwidth, 3.6-GHz digital SD fractional-N frequency synthesizer with quantization noise cancellation," *IEEE ISSCC Digest of Technical Papers, 2008.*

An Ultra-Low Power CMOS RF Transceiver for Medical Implants

J. Bohorquez, J.L. Dawson, A.P. Chandrakasan
Sponsorship: SRC/FCRP C2S2

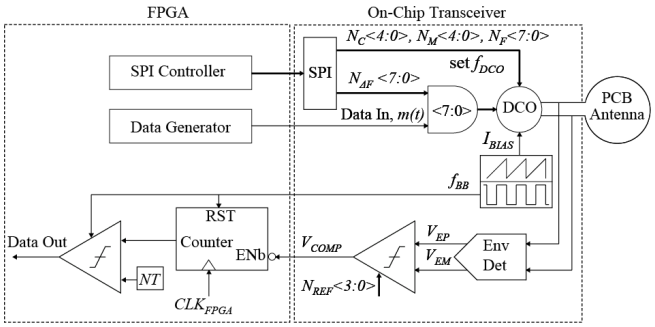
Until recently, few medical implantable devices existed and fewer still provided the capability for wireless transmission of information. Most devices capable of data transmission did so through inductive coupling, which requires physical contact with the base-station and allows for only low data rates. In 1999, the FCC created the Medical Implant Communications Service (MICS) band in the range of 402–405 MHz specifically for medical telemetry [2]. The MICS band plan allows for RF communication between a medical implant and a base-station that is up to two meters away. This research seeks to design a transceiver specifically optimized for low-power, short-distance data transmission in a temperature-regulated environment, i.e., the human body. We do this by pushing as much complexity as possible out of the implant and into the base-station, taking advantage of the attributes of the environment, such as temperature control and slow transients, and incorporating the antenna into the oscillator for reduced power and improved performance. By optimizing the transceiver for reduced volume and power, we hope to extend the battery lifetime and functionality of medical implants for greater comfort and benefits to patients.

We propose a simple, almost all-digital transceiver (Figure 1) comprising a direct modulation frequency-shift keying transmitter and a super-regenerative receiver. The transmitter is composed of a digitally-controlled oscillator (DCO) and simple digital logic; the receiver uses the same DCO, a quench oscillator, an envelope detector, a comparator and simple digital blocks. Data is transmitted by directly modulating the frequency of the DCO through a capacitor bank. The frequency deviation constant is digitally set through a serial-to-parallel interface such that digital data composed of ones and zeros shift the DCO frequency by a desired amount. We linearize the digital-to-frequency relationship of the DCO by pre-distorting the capacitor banks used to tune the frequency and the frequency deviation constant of the transmitter. Instead of driving the antenna with a matched power amplifier, we exploit the low radiation power requirement of MICS to incorporate a loop antenna into the DCO. The inherently high Q of the antenna leads to improved noise performance for a given amount of power.

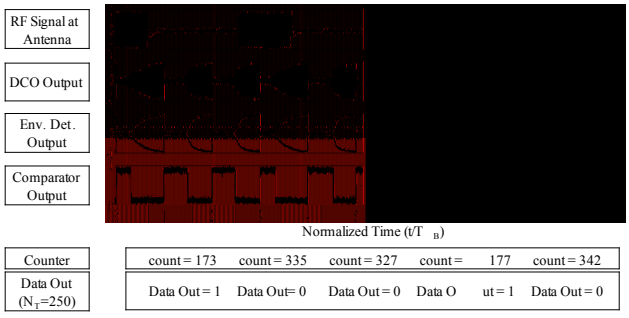
The SRR receives on-off keying (OOK) data and determines whether a one or a zero was sent by measuring the amount of time required for the envelope of the DCO output to reach a threshold. Input signals with large amplitudes and strong frequency content near the DCO's resonant frequency result in faster startup times. A digital counter determines the startup time and compares it to a threshold. Figure 2 shows normalized time domain signals in the receiver chain.

Our design was implemented in IBM 90-nm CMOS. The transmitter consumes under 350μW and meets MICS mask specifications with data rates up to 120kbps. The receiver consumes under 400μW and achieves a sensitivity of -99dBm or better at data rates of 40kbps, or -93dBm at data rates of 120kbps. The DCO tunes 24MHz in frequency steps smaller than 2kHz.

The authors acknowledge the support of the Focus Center for Circuit & System Solutions (C2S2), one of five research centers funded under the Focus Center Research Program, a Semiconductor Research Corporation Program.



▲ Figure 1: Direct FSK transmitter and OOK super-regenerative receiver with on-chip quench oscillator.



▲ Figure 2: Normalized time domain signals in the receiver chain.

Reference

[1] FCC Rules and Regulations, "MICS Band Plan," *Part 95*, Jan. 2003.

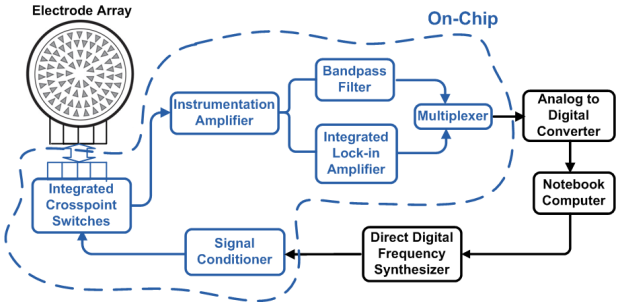
Impedance Measurement Utilizing an Integrated High-frequency Lock-in Amplifier for the Assessment of Neuromuscular Disease

O.T. Ogunnika, R.C. Cooper, J.L. Dawson
Sponsorship: CIMIT

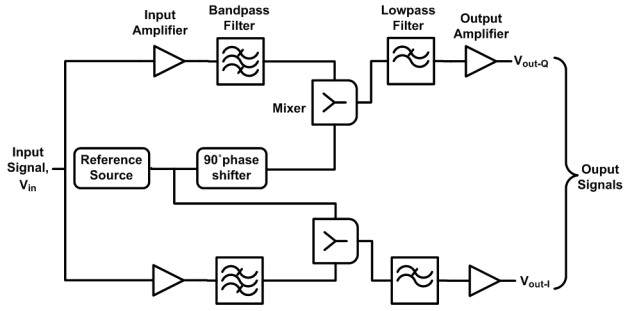
Electrical Impedance Myography (EIM) is a non-invasive, painless clinical technique for the diagnosis and monitoring of a variety of neuromuscular diseases including generalized disorders, such as amyotrophic lateral sclerosis and muscular dystrophies, and localized conditions, such as focal nerve injuries [1]. It involves the application of a low-intensity alternating current to a muscle group and the measurement of the consequent surface voltage patterns [2]. This data is then used to compute the impedance of the muscle group under investigation.

The EIM measurement system (Figure 1) will be designed to take measurements from 10kHz to 10MHz. With the exception of the analog-to-digital converter (ADC) and direct digital frequency synthesizer (DDFS), all circuit blocks will be integrated onto a single IC. The system will operate in two modes selected by the multiplexer: high precision (using lock-in amplifier) and high speed (using bandpass filter). Note that in both modes of operation, this measured signal will be digitized by the ADC for further processing on a portable computer. The signal to be used in the interrogation of the muscle tissue is first created by this portable computer and then downloaded to the DDFS. The signal conditioner converts the signal generated by the DDFS from single-ended to differential and amplifies it to a level suitable for use with the crosspoint switches and reconfigurable electrode array in contact with the patient's skin. An instrumentation amplifier senses and amplifies the voltage that is induced across the muscle. Its output is bandpass-filtered before processing by the lock-in amplifier.

Lock-in amplifiers are capable of extracting a signal from noise in situations where linear filtering is not sufficient [3]. It is essentially a phase-sensitive detector that measures the amplitude and phase of a noisy signal and then reduces the effective noise bandwidth by means of synchronous detection, which requires knowledge of the desired signal's frequency. The architecture to be used in this work is the dual-phase lock-in amplifier shown in Figure 2. The input signal is multiplied by a reference signal at the same frequency, producing an output with a DC component proportional to the product of their amplitudes. The AC components in the output of the lock-in amplifier are filtered out by a lowpass filter. Good noise isolation requires the output lowpass filter to have a very small bandwidth (<1Hz). Typically, the implementation of filters with very small bandwidths require the use of passive components that produce large time constants leading to undesirably long signal settling times. Thus, the design of the output filter requires a tradeoff between measurement time and bandwidth. The division of the total signal amplification between the AC coupled input amplifiers and the DC coupled output amplifiers will be optimized. Too much amplification by the AC amplifiers could saturate the mixer while too much amplification by the DC amplifiers will lead to increased signal drift with time and temperature. Auto-scaling of the input signal drive will also be implemented to ensure that the EIM system can adapt to variations in load impedance without the need for time-consuming calibration.



▲ Figure 1: System diagram of multi-frequency EIM measurement system.



▲ Figure 2: Concept diagram of dual-phase lock-in amplifier.

References

[1] S.B. Rutkove, R. Aaron, and C.A. Shiffman, "Localized bio-impedance analysis in the evaluation of neuromuscular disease," *Muscle & Nerve*, pp. 390-397, Mar. 2002.

[2] G.J. Esper, C.A. Shiffman, R. Aaron, K.S. Lee, and S.B. Rutkove, "Assessing neuromuscular disease with multifrequency electrical impedance myography," *Muscle & Nerve*, vol. 34, pp. 595-602, July 2006.

[3] G. Ferri, P. De Laurentiis, A. D'Amico, and C. Di Natale, "A low-voltage integrated CMOS analog lock-in amplifier prototype for LAPS applications," *Sensors and Actuators*, A 92, pp. 263-272, 2001.

A Low-power, Blocking-capacitor-free, Charge-balanced Electrode-stimulator Chip with Less than 6-nA DC Error for 1-mA Full-scale Stimulation

J. Sit, R. Sarpeshkar

Large DC-blocking-capacitors are a bottleneck in reducing the size and cost of neural implants. We describe an electrode-stimulator chip that removes the need for large DC-blocking capacitors in neural implants by achieving precise charge-balanced stimulation with <6 nA of DC error. For cochlear implant patients, this is well below the industry's safety limit of 25 nA. Charge balance is achieved by dynamic current balancing to reduce the mismatch between the positive and negative phases of current to 0.4%, followed by a shorting phase of at least 1 ms between current pulses to further reduce the charge error. On +6- and -9-V rails in a 0.7–μm AMI high voltage process, the power consumption of a single channel of this chip is 47 μW when biasing power is shared by 16 channels.

An Energy-efficient Micropower Neural Recording Amplifier

W. Wattanapanitch, M. Fee, R. Sarpeshkar

This paper describes an ultra-low-power neural recording amplifier. The amplifier appears to be the lowest power and most energy-efficient neural recording amplifier reported to date. We describe low-noise design techniques that help the neural amplifier achieve input-referred noise that is near the theoretical limit of any amplifier using a differential pair as an input stage. Since neural amplifiers must include differential input pairs in practice to allow robust rejection of common-mode and power supply noise, our design appears to be near the optimum allowed by theory. The bandwidth of the amplifier can be adjusted for recording either neural spikes or local field potentials (LFPs). When configured for recording neural spikes, the amplifier yielded a midband gain of 40.8-dB- and a -3-dB-bandwidth from 45 Hz to 5.32 kHz; the amplifier's input-referred noise was measured to be 3.06 μV_{rms} while consuming 7.56 µW of power from a 2.8-V supply, corresponding to a noise efficiency factor (NEF) of 2.67 with the theoretical limit being 2.02. When configured for recording LFPs, the amplifier achieved a midband gain of 40.9 dB and a -3-dB bandwidth from 392 mHz to 295 Hz; the input-referred noise was 1.66 μV_{rms} while consuming 2.08 µW from a 2.8-V supply corresponding to an NEF of 3.21. The amplifier was fabricated in AMI's 0.5-µm CMOS process and occupies 0.16 mm^2 of chip area. We obtained successful recordings of action potentials from the robust nucleus of the arcopallium (RA) of an anesthesized zebra finch brain with the amplifier. Our experimental measurements of the amplifier's performance including its noise were in good accord with theory and circuit simulations.

A 12-b, 100-MS/s, Fully Differential Zero-crossing-based ADC

L. Brooks, H.-S. Lee

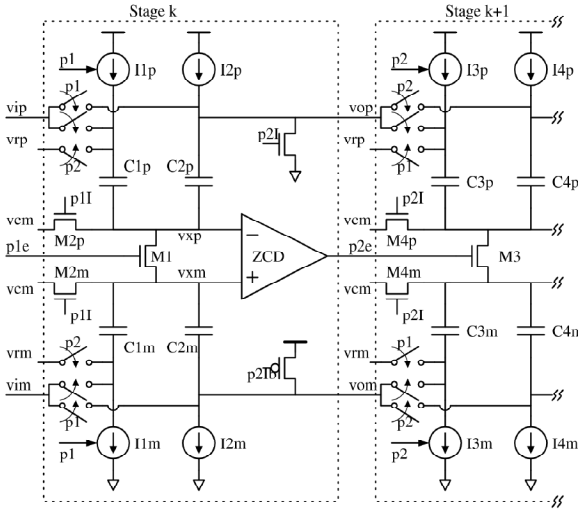
Sponsorship: CICS, NDSEG, DARPA

In an effort to improve on the resolution and production-worthiness of zero-crossing-based circuits (ZCBC) [1], a 12-b, 100-MS/s, fully differential pipelined ADC has been designed with the goals of improved power supply noise rejection, automatic offset compensation, and output signal range enhancement.

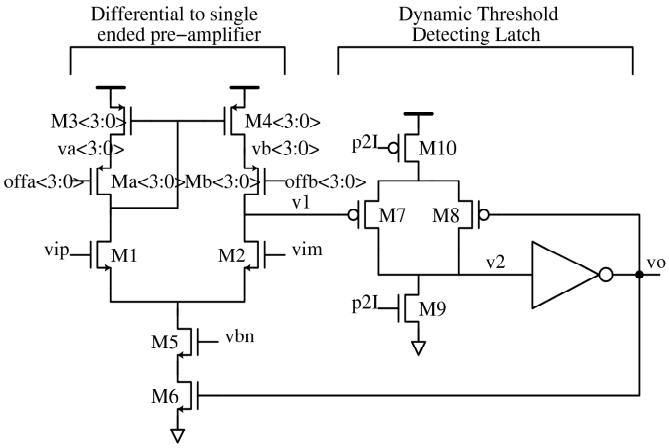
Figure 1 shows the implementation of two adjacent pipeline stages. The differential input (vip,vim) is sampled onto capacitors C1 and C2 during the sampling phase, when p1 is high. Then during the transfer phase, when p2 is high, current sources I2, I3, and I4 turn on to create a differential ramp on the output nodes (vop, vom). When the zero-crossing detector (ZCD) detects that the virtual ground condition has been realized, the sampling switch M3 turns off to lock the desired charge onto capacitors C3 and C4, which are the sampling capacitors of the next stage.

Figure 2 shows the schematic of the ZCD implementation. A pre-amplifier that performs a differential to single-ended conversion precedes a dynamic threshold-detecting latch that is similar to the dynamic zero-crossing detector introduced in [1]. The pre-amplifier consists of a differential pair (M1, M2) , a current bias source (M5), and a current mirror (M3, M4). For increased power savings, device M6 shuts off the bias current after the ZCD switches. Devices Ma and Mb function as enable switches to vary the gain of the current mirror to provide a digital method of adjusting the offset of the ZCD. For automatic offset compensation, a chopping technique similar to [2, 3] has been developed. The offset is estimated from the chopped output signal prior to demodulation. This offset estimate is then fed back and nulled in the ZCD to reduce the flicker noise and improve the signal range.

A fully differential implementation has been used to provide better power supply rejection. Continuous time common mode feedback is not necessary for several reasons. One is that unlike an op-amp based implementation, this implementation has very little common mode gain from the input to the output of each stage. Another is that using switch M3 as configured in Figure 1 as the only sampling switch ensures that despite mismatch between the current sources, the positive and negative sampling capacitors receive the same amount of charge and thus receive a common mode reset.



▲ Figure 1: Schematic of adjacent fully differential zero-crossing-based pipelined stages.



▲ Figure 2: Schematic of zero-crossing detector with digitally programmable offset.

References

[1] L. Brooks and H.-S. Lee, "A zero-crossing based 8b, 200ms/s pipelined ADC," *ISSCC Digest of Technnical Papers*, Feb. 2007, pp. 460–461.

[2] H. van der Ploeg, G. Hoogzaad, H.A. Termeer, M. Vertregt, and R.L. Roovers, "A 2.5-v 12-b 54-msample/s 0.25-µm CMOS ADC in 1-mm2 with mixed-signal chopping and calibration," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 1859–1867, Dec. 2001.

[3] S.M. Jamal, D. Fu, N. Chang, P. Hurst, and S.H. Lewis, "A 10-b 120-msample/s time-interleaved analog-to-digital converter with digital background calibration," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1618–1627, Dec. 2002.

Ultra-high Speed A/D Converters Using ZCBC Topology

A. Chow, H.-S. Lee

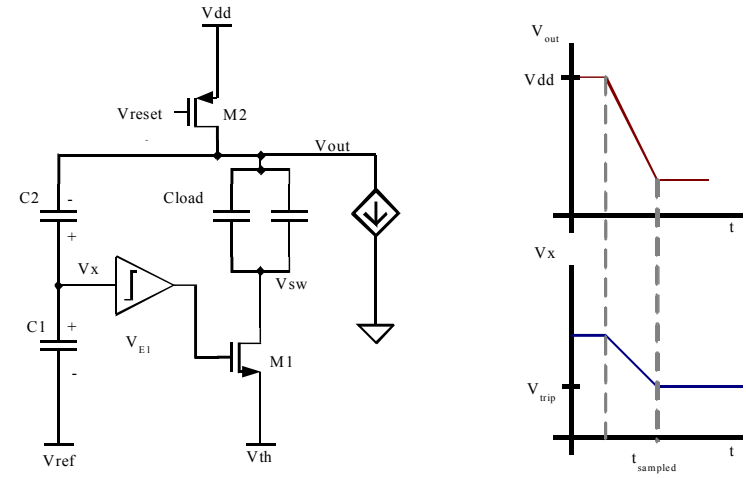
Sponsorship: SRC/FCRP C2S2

With an increasing need for higher data rates, both wireless applications and data links are demanding higher speed analog-to-digital converters (ADC) with medium resolution. In particular, this work will investigate ADC's with sampling rate up to 10 Gs/s with 6-8 bits of resolution.

Time-interleaved converters achieve their high sampling rate by placing several converters in parallel. Each individual converter, or channel, has a delayed sampling clock and operates at a reduced sampling rate. Therefore, each channel is responsible for digitizing a different time slice. This method requires that the individual converters, which make up the parallel combination, be matched. Mismatches and non-idealities, such as gain error, timing error, and voltage offset, degrade the performance. Therefore channel matching is an important design consideration for time-interleaved ADCs.

Although digital calibration can mitigate many of these non-idealities, timing mismatches constitute a non-linear error that is more difficult to remove. At sampling rates up to 10Gs/s, digital calibration would consume a large amount of power. An alternative solution uses a global switch running at the full speed of the converter. Although this technique works reasonably well for medium-high speed ADC's [1, 2], parasitic capacitance limits its effectiveness. We have developed a double-global sampling technique to remove the effect of parasitic capacitance on timing skew. At higher speeds the ability to turn the switch on and off at the full sampling rate becomes a major challenge. The use of scaled CMOS technology and gate bootstrapping still enables multi-GHz input bandwidth.

Power optimization is a major design consideration when implementing a time-interleaved ADC. We will lower total power consumption by exploring innovative technologies for implementing the individual ADCs in the channel, such as the zero-crossing-based circuit (ZCBC) topologies previously presented. In particular, this work is investigating a fast, single-slope architecture (see Figure 1). The primary emphasis is the development of high-speed, highly power-efficient single-slope ZCBC architecture. Since the single-slope architecture is more sensitive to non-idealities such as ramp nonlinearity, we are carefully studying the sources of non-idealities and developing clever techniques to address the accuracy issues.



▲ Figure 1: One stage of a single-slope CBSC-based pipelined ADC.

References

[1] M. Gustavsson, "A global passive sampling technique for high-speed switched-capacitor time-interleaved ADCs," *IEEE Trans. on Circuits and Systems II*, pp. 821-831, 2000.

[2] S. Gupta, et al, "A 1GS/s 11b time-Interleaved ADC in 0.13µm CMOS," *Digest of the International Solid State Circuits Conference*, 2006, pp. 576-5771.

A High-bandwidth Zero-crossing-based Sigma-delta ADC

J. Feng, H.-S. Lee

Sponsorship: BAE Systems, CICS

Recently, comparator-based switched-capacitor (CBSC) circuits and zero-crossing-based circuits (ZCBC) were introduced [1, 2] as a viable alternative to op-amp-based circuits. The use of op-amps in analog signal processing circuits is becoming more difficult due to the decreased intrinsic device gains and reduced signal swings obtained in scaled CMOS technologies. Op-amps rely upon high gain in the negative feedback mode in sampled data systems because the gain determines the accuracy of the output value. CBSC and ZCBC-based circuits replace the op-amp using a comparator and a current source and therefore do not require high gain and stability simultaneously, as in op-amp-based circuits. In this work, we explore the use of zero-crossing-based circuits to replace op-amps in high-bandwidth ,discrete time sigma-delta ADCs.

Sigma-delta ADCs are advantageous for realizing high resolutions with relaxed matching requirements between integrated circuit components. Traditionally, sigma-delta ADCs have been limited to voice band signals because of the inherent oversampling in the architecture. However, because of the demand for higher conversion bandwidths such as in broadband internet, sigma-delta ADCs have made significant progress in improving the effective conversion rate while maintaining high resolutions [3].

This research focuses on the development of innovative circuits and sampling architectures to design a zero-crossing-based sigma-delta ADC with a signal bandwidth of >20 MHz, sampling rate of 500 MHz, and 13 bits of accuracy. An example of a possible application appears in VDSL systems. We are investigating chopper-stabilization techniques to remove errors due to offsets, overshoot, and flicker noise in zero-crossing detectors. The use of zero-crossing circuits will ultimately result in large power savings over op-amp-based sigma-delta ADCs.

References

[1] T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2006, pp. 220-221.

[2] L. Brooks and H.-S. Lee, "A zero-crossing-based, 8b, 200MS/s pipelined ADC," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2007, pp. 15-17.

[3] P. Balmelli and Q. Huang, "A 25-MS/s, 14-b, 200-mW ΣΔ modulator in 0.18-µm CMOS," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2004, pp. 74-75.

A Low-voltage Zero-crossing-based Delta-sigma ADC

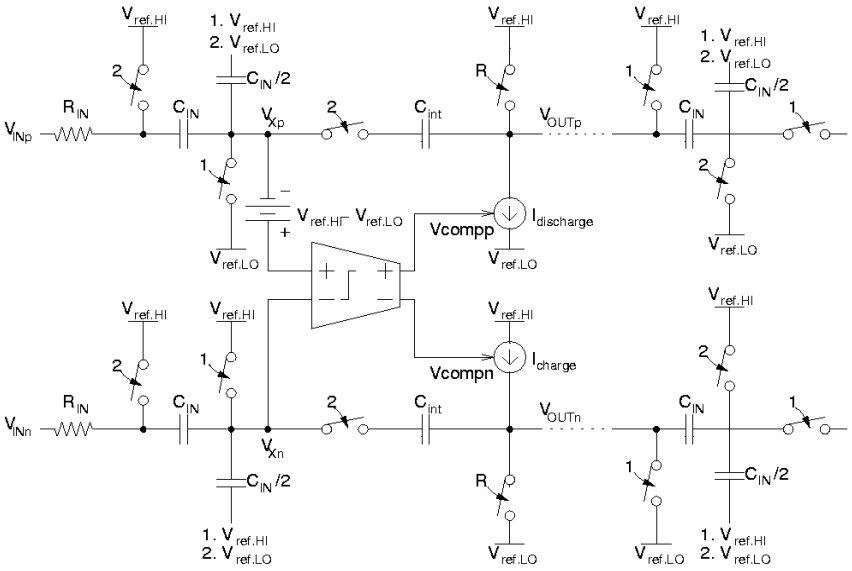
M. Guyton, H.-S. Lee

Sponsorship: CICS, DARPA

Many analog signal processing circuits use operational amplifiers (op-amps) in a negative feedback topology. Error in these feedback systems is inversely proportional to the gain of the op-amp. Because scaled CMOS technologies use shorter channel lengths and require lower power supply voltages, it becomes more difficult to implement high gain op-amps. Recently, a comparator-based switched-capacitor (CBSC) technique was proposed [1] that uses a comparator rather than an op-amp to implement switched-capacitor topologies. This technique was generalized to the use of zero-crossing detectors [2].

In this project, we investigate very-low-voltage delta-sigma converters. One of the biggest challenges of low-voltage circuits is the transmission gates that must pass the signal. If the signal is near the middle of the power supply range, neither the NMOS nor the PMOS transistor has sufficient gate drive to pass the signal properly. The switched-op-amp technique [3] was proposed to mitigate this problem. In this technique, the output of the op-amp is directly connected to the next sampling capacitor without a transmission gate to perform charge transfer. During the charge transfer phase, the op-amp is switched off, and the output is grounded.

Much like the standard switched-capacitor technique, zero-crossing-based (ZCB) circuits use two-phase clocking, having both sampling and charge-transfer clock phases. Unlike in a standard switched-capacitor circuit, in a ZCB circuit all current sources connected to the output node are off at the end of the charge-transfer phase. Therefore, there is no op-amp or current source to turn off to accommodate the charge transfer without a transmission gate. Thus, the ZCB technique is inherently better suited to low-voltage applications than switched-op-amp circuit topologies. Figure 1 shows a fully-differential low-voltage ZCB integrator stage using the combined techniques. We are designing a fourth-order delta-sigma ADC for operation at 1-V power supply using this integrator stage for audio-band applications. A new output pre-sampling technique has been developed to dramatically reduce the linearity requirement of the ramp waveform.



▲ Figure 1: Fully-differential zero-crossing-based switched-capacitor integrator. The input of the next integrator stage is also shown.

References

[1] T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *2006 IEEE ISSCC Digest of Technical Papers*, Feb. 2006, p. 220.

[2] L. Brooks and H.S. Lee, "A zero-crossing-based 8b, 200 MS/s pipelined ADC," *2007 IEEE ISSCC Digest of Technical Papers*, Feb. 2007, pp.460-461.

[3] J. Crols and M. Steyaert, "Switched-op-amp: an approach to realize full CMOS switched-capacitor circuits at very low power supply voltages," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 8, pp. 936-942, Aug. 1994.

A High-performance Zero-crossing-based Pipeline ADC

J. Chu, H.-S. Lee

Sponsorship: SRC/FCRP C2S2

In this work, we are designing a high-performance pipeline ADC using a zero-crossing-based (ZCB) structure [1], which is an extension of the comparator-based switch-capacitor circuit (CBSC) design methodology [2]. The focus of the project is to explore novel circuit structures based on ZCB circuits (ZCBCs) to improve the figure-of-merit (FOM) of ZCBCs. The FOM is generally defined as the power consumption divided by the signal bandwidth and the signal-to-ratio, and it is a measure of the power efficiency of a circuit. The state-of-the-art FOM for a 12-bit ADC with sampling rates of 100MS/s and up is approximately 1pJ/step. In this project, we are investigating pipeline ADCs with 12-bit resolution and 200 Ms/s sampling rate. Our target for the FOM is 10 fJ/step or better, representing 2 orders of magnitude improvement from the state-of-the-art. In particular, we are investigating the use of a differential structure to improve ZCBCs' robustness against common mode noise. An additional benefit of differential design is the increase in the available signal range, which helps to improve SNR. We plan to implement a multi-bit MDAC to improve its power efficiency and to help relax component accuracy requirements. In this design, we plan to use dynamically biased current sources to achieve high linearity at high operating frequencies. Dynamic biasing can be used to compensate for finite output impedance in current sources, which improves the linearity of the system.

Future iterations of this project will use time-interleaving to achieve ultra-high sampling rates (>1GS/s) with very low power. In a time-interleaved structure, matching between the different channels will be very important to maintain the desired performance. Any mismatch in non-idealities such as gain error, offset, or timing errors can greatly degrade the performance. We plan to use a global sampling technique, which mitigates the timing errors [3-4]. Careful design and layout will be needed to reduce the other mismatches.

References

[1] L. Brooks and H.-S. Lee, "A zero-crossing-based 8b 200MS/s pipelined ADC," *IEEE International. Solid-State Circuits Conference Digest of Technical Papers*, 2007, pp. 15-17.

[2] T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE International. Solid-State Circuits Conference Digest of Technical Papers*, 2006, pp. 220-221.

[3] M. Gustavsson, "A global passive sampling technique for high-speed switched-capacitor time-interleaved ADCs," *IEEE Transactions on Circuits and Systems II*, pp. 821-831, 2000.

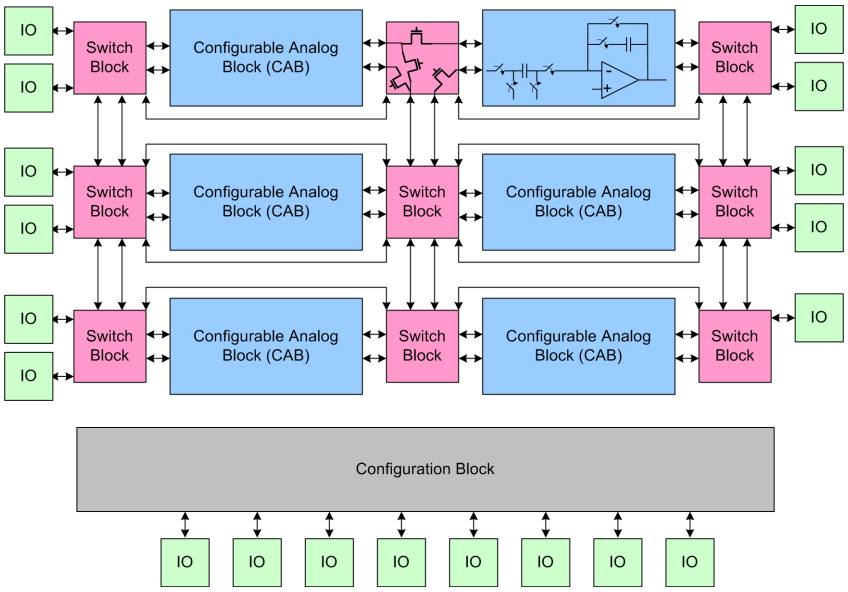
[4] S. Gupta, et al., "A 1Gs/s 11b time-interleaved ADC in 0.13-µm CMOS," *Digest of International Solid-State Circuits Conference*, 2006, pp. 576-577.

Highly Reconfigurable Zero-crossing-based Analog Circuits

P. Lajevardi, A.P. Chandrakasan, H.-S. Lee
Sponsorship: CICS, DARPA

Switched-capacitor circuits can be used to implement many analog systems, such as ADCs, DACs, filters, amplifiers, and integrators. In an earlier phase of this research, we proposed a reconfigurable switched-capacitor system to implement different analog systems. A prototype system is now being fabricated that shows basic reconfigurability to implement a pipe-lined ADC and a switched-capacitor filter. A second prototype system is being designed that utilizes highly reconfigurable blocks. Figure 1 shows the block diagram of the system. The building blocks have the same functionality and can implement an integrator or a multiplier with a reconfigurable coefficient. There is a reconfigurable connection between blocks. Such a system has many applications, such as in software-defined radios and rapid prototyping of analog circuits.

The design of such systems has had limited success since many different op-amp topologies are required to cover a large performance and configuration space. Recently, [1] and [2] proposed zero-crossing circuits to design ADCs. Zero-crossing circuits can replace the op-amp in the traditional switched-capacitor design with a combination of a current source and a zero-crossing detector. The power consumption of zero-crossing-based analog circuits scales according to the operating frequency and required SNR. In addition, while new technology nodes provide transistors with higher f_t, the design of op-amps is becoming more challenging as the supply voltage and intrinsic gain of transistors are decreasing. Zero-crossing circuits can benefit more from technology scaling due to their more digital-circuit-like operation. In addition, due to the lack of high static gain and stability requirements, the topology of zero-crossing detectors is far simpler than that of op-amps. Therefore, a single topology is suitable for a very wide range of performance space. Zero-crossing circuits are used to implement the reconfigurable analog blocks in this research. The system can operate at different speeds and SNR requirements while the power consumption is kept at the optimum level.



▲ Figure 1: Block diagram of reconfigurable zero-crossing-based analog circuits. Each configurable analog block can be programmed to perform an integration or multiplication. The connection of blocks is also programmable.

References

[1] T. Sepke, J. Fiorenza, C.G. Sodini, P. Holloway, and H.-S Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2006, pp. 220-221.

[2] L. Brooks and H.-S. Lee, "A zero-crossing-based 8-b 200MS/S pipeline ADC," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2007, pp. 460-461.

Zero-crossing-based Switched-capacitor Filters

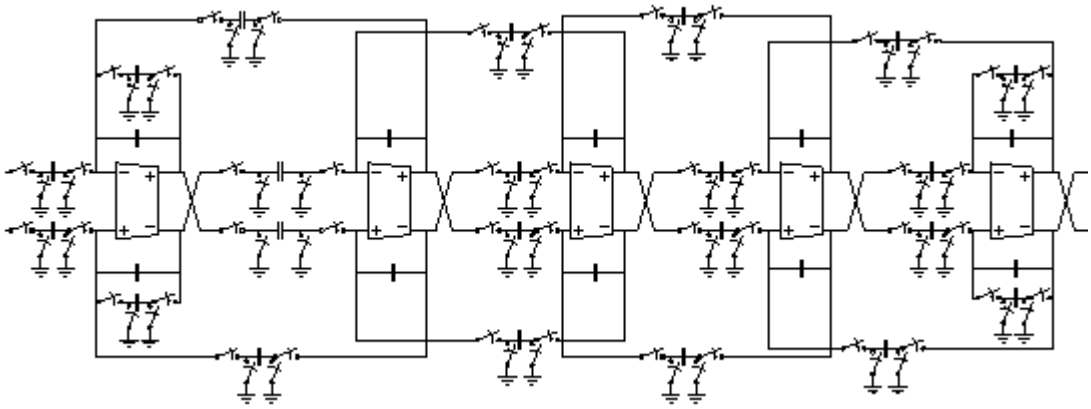
S. Lee, H.-S. Lee

Sponsorship: Korea Foundation for Advanced Studies Scholarship

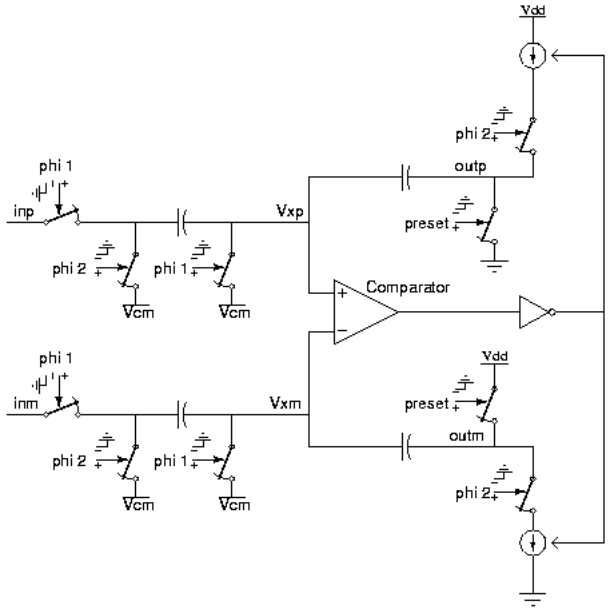
Design of switched-capacitor circuits in scaled CMOS technologies is becoming difficult because of low device intrinsic gain and reduced power supply voltage. To solve these problems, comparator-based switched-capacitor (CBSC) circuits and zero-crossing-based circuits (ZCBC) were suggested as possible solutions to the op-amp based circuits. In this project, we explore zero-crossing-based circuits (ZCBC) in high-order differential switched-capacitor filters to replace area-inefficient op-amps-based continuous-time base-band filters.

If high-order filters are implemented by cascading second-order filters, the frequency response will be very sensitive to component variations. To implement less sensitive high-order filters, this project will use a low-pass ladder filter network as the prototype for the zero-crossing-based high-order switched-capacitor filter. After several transforming steps, this low-pass ladder filter prototype has been transformed into a differential high-order switched-capacitor filter, which is shown in Figure 1. This architecture has been verified by SWITCAP, giving the frequency response with low-pass characteristics.

Differential op-amps in a high-order switched-capacitor filter shown in Figure 1 are replaced by zero-crossing-based circuits (ZCBC). Figure 2 shows a differential zero-crossing-based circuits (ZCBC) integrator, which is the key component in a high-order switched-capacitor filter, which consists of a comparator and current sources.



▲ Figure 1: A 5th-order differential-switched-capacitor ladder filter.



▲ Figure 2: Circuit diagram for a differential ZCBC integrator.

High-accuracy Pipelined A/D Converter Based on Zero-crossing Switched-capacitor Circuits

M. Markova, P. Holloway, H.-S. Lee
Sponsorship: EECS Fellowship, CICS

Technology scaling poses challenges in designing analog circuits because of the decrease in intrinsic gain and reduced swing. An alternative to using high-gain amplifiers in the implementation of switched-capacitor circuits has been proposed [1] that replaces the amplifier with a current source and a comparator. The new comparator-based switch-capacitor (CBSC) technique has been implemented in two pipelined ADC architectures at 10MHz and 200MHz and 10-bit and 8-bit accuracy, respectively [1, 2].

The purpose of this project is to explore the use of the CBSC technique for very high-precision AD converters. The goal of the project is a 100MHz 16-bit pipelined ADC. First, we are investigating multiphase CBSC operation to improve the power-linearity trade off of the A/D conversion [3]. We are also developing linearization techniques for the ramp waveforms. Linear ramp waveforms require fewer phases, thus allowing faster operation. Techniques for improving linearity beyond using a cascoded current source are explored. A linear ramp generator, which decouples the current source from the output ramp through a Miller capacitor, is proposed to improve the linearity of the ramp waveform in all phases. This ramp generator improves the range by improving linearity through compensation of the gate-to-source voltage of the current source without the use of a cascode. In addition it lends itself to a symmetric differential implementation for the final phase to ensure adequate noise rejection. At the target resolution of 16 bits, power supply and substrate noise coupling can limit the performance. We are studying their effects in CBSC circuits. For reduced sensitivity to power supply and substrate noise, we are developing a differential CBSC architecture. Other techniques that we are presently developing include power-efficient offset cancellation in comparators and exploiting *a priori* information from previous stages in the pipeline structure to increase linearity and speed.

References

[1] T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched capacitor circuits for scaled CMOS technologies," *IEEE Journal of Solid State Circuits*, vol. 41, no. 12, pp. 2658-2668, Dec. 2006.

[2] L. Brooks and H.-S. Lee, "A zero-crossing-based 8b 200MS/s pipelined ADC," in *IEEE International Solid State Circuits Conference Digest of Technical Papers*, San Francisco, CA, Feb. 2007, pp. 460-461.

[3] J.K. Fiorenza, "A comparator-based switched-capacitor pipelined analog-to-digital converter," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.

On-chip Voltage-scalable Switched-capacitor DC-DC Converter

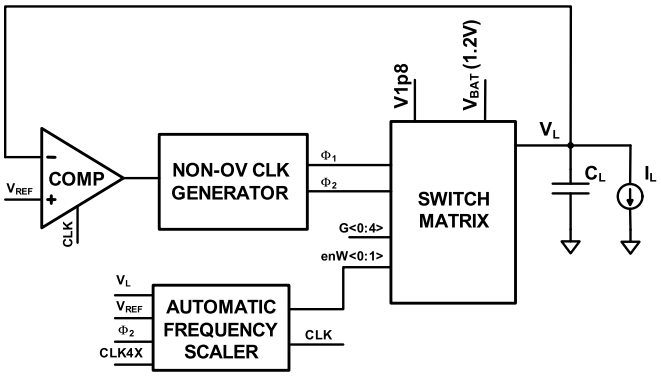
Y.K. Ramadass, A.P. Chandrakasan

Sponsorship: DARPA

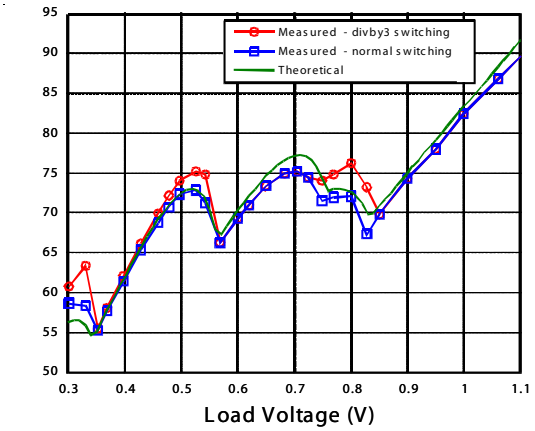
Minimizing the energy consumption of battery-powered systems is a key focus in integrated circuit design. Dynamic voltage scaling (DVS) [1] and sub-threshold operation are popular methods to achieve energy efficiency in systems that have widely variant performance demands. However, to realize the full energy benefits of voltage scaling, an efficient voltage-scalable DC-DC converter is of great importance. DVS systems also often require multiple on-chip voltage domains with each domain having specific power requirements. A switched-capacitor (SC) DC-DC converter is a good choice for such battery operated systems because it can minimize the number of off-chip components and does not require any inductors, thereby reducing the overall DC-DC converter volume and cost.

Figure 1 shows the architecture of a switched-capacitor DC-DC converter [2] implemented in 0.18-µm CMOS. The converter employs Pulse Frequency Modulation (PFM) to achieve voltage regulation. In this mode of control, the converter stays idle till the load voltage (V_L) falls below a user-defined reference voltage (V_{REF}), at which point the comparator enables the switch matrix to transfer one charge packet to the load. The switched capacitor DC-DC converter employs on-chip charge-transfer capacitors and can provide scalable load voltages from 0.3V to 1.1V. In order to maintain efficiency over this voltage range, the converter employs 5 different gain settings (G<0:4>) which help in minimizing conduction loss [2]. The automatic frequency-scaler block helps to adjust the frequency of operation and the size of the switches (enW<0:1>) within the switch matrix, with changes in load power. This helps in scaling the switching losses as the load power varies. A divide-by-3 switching scheme [2] was employed in the converter to reduce the parasitic bottom-plate losses and improve efficiency. Also, the all-digital control circuitry used in the converter consumes no static power. The voltage-scalable SC DC-DC converter with integrated on-chip charge transfer capacitors was implemented in National Semiconductor's 0.18-µm CMOS process and consumed an active area of 0.57 mm². The converter achieved above 70% efficiency over a wide range of load powers from 5µW to 1mW, while delivering load voltages from 300mV to 1.1V. Figure 2 shows the efficiency of the converter with change in load voltage while delivering 100µW to the load.

A modified version of this design was implemented as part of a 65-nm sub-threshold microcontroller system [3]. The DC-DC converter in the microcontroller occupied just 0.12 mm² in area and was able to achieve 75% efficiency at a load voltage of 500mV with the microcontroller as the load.



▲ Figure 1: Architecture of the switched-capacitor DC-DC converter employing the PFM mode of control.



▲ Figure 2: Efficiency plot of the DC-DC converter with change in load voltage.

References

[1] B.H. Calhoun and A.P. Chandrakasan, "Ultra-dynamic voltage scaling using sub-threshold operation and local voltage dithering in 90nm CMOS," *ISSCC Digest of Technical Papers*, pp. 300-301, Feb. 2005.

[2] Y.K. Ramadass and A. Chandrakasan, "Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications," *IEEE Power Electronics Specialists Conference*, pp. 2353-2359, June 2007.

[3] J. Kwong et al., "A 65nm sub-V_t microcontroller with integrated SRAM and switched-capacitor DC-DC converter," *ISSCC Digest of Technical Papers*, pp. 318-319, Feb. 2008.

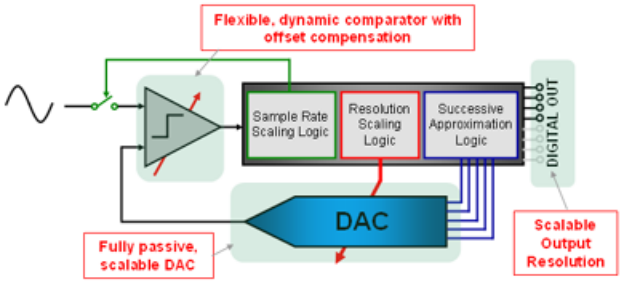
A Highly Digital, Resolution- and Voltage-scalable SAR ADC

M. Yip, A.P. Chandrakasan
Sponsorship: DARPA, NSERC

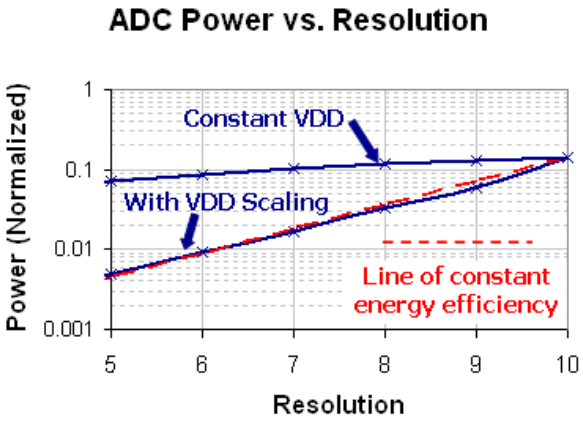
In energy constrained systems such as wireless sensor nodes or mobile electronics, it is desirable to have analog-to-digital converters (ADC) that can operate in the sub-threshold regime to minimize energy during long standby periods but can also dynamically elevate their performance to meet system demands. In this work, a highly digital, energy-efficient successive approximation register (SAR) ADC with scalable resolution from 5 to 10-bits is being designed. Recent SAR ADCs have achieved energy efficiencies on the order of a few fJs per conversion step, but only at a fixed resolution [1]. The main challenge in designing a scalable ADC is maintaining its energy-efficiency across all resolutions.

This SAR ADC consists of a comparator, a digital-to-analog converter (DAC) and digital control logic to implement a binary search algorithm. Figure 1 shows the system level block diagram. Clock gating is used to enable sample rate scaling from 1-MS/s down to 0. Special techniques are used to deactivate extraneous circuitry as resolution is reduced to maintain energy efficiency. Often, this scalability involves using analog switches at critical nodes and must therefore be carefully designed, especially at low supply voltages.

Lastly, voltage scaling is used to maintain a constant energy efficiency as the resolution is reduced. Recently, SAR ADCs operating on a 500-mV supply have been reported [2]. This ADC will be designed to operate at 10-bits at 1-V, down to 5-bits at 400-mV. Figure 2 shows how voltage scaling allows the ADC to maintain constant energy efficiency over all resolutions.



▲ Figure 1: System-level block diagram of scalable ADC. Digital logic is used to control the resolution, the sample rate and the comparator mode of operation.



▲ Figure 2: ADC power vs. resolution. Voltage scaling from 1-V down to 400-mV is used to maintain energy efficiency across all resolutions.

References

[1] M. van Elzakker, E. van Tuijl, P. Geraedts, D. Schinkel, E. Klumperink, and B. Nauta, "A 1.9µW 4.4fJ/conversion-step 10b 1MS/s charge-redistribution ADC," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2008, pp. 244-245.

[2] S. Gambini and J. Rabaey, "Low-power successive approximation converter with 0.5 V supply in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 11, pp. 2348-2356, Nov. 2007.

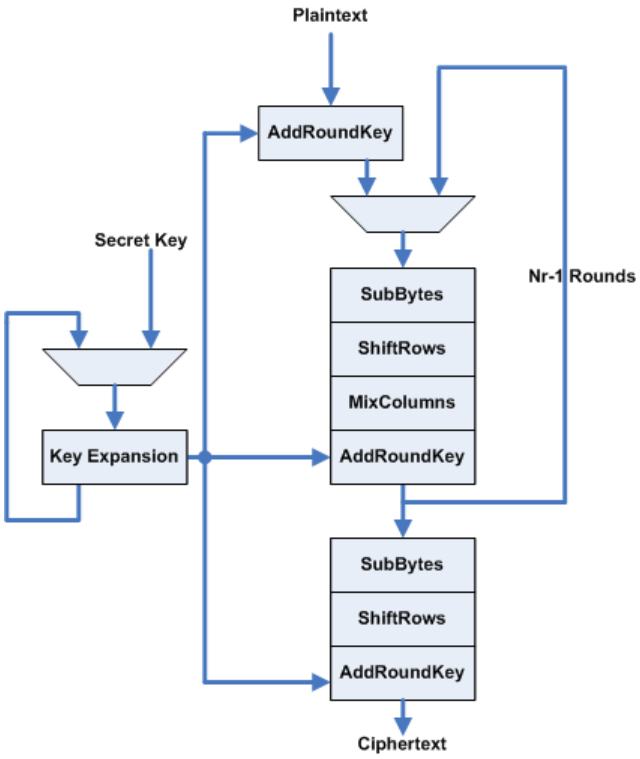
An AES-based Energy-efficient Encryption Processor with Resistance to Differential Power Analysis Attacks

H.W. Chung, A.P. Chandrakasan

Security concerns for transmission or storage of data by battery-operated wireless systems require the development of an energy-efficient encryption processor. However, even with the security ICs, core information can be discovered by attackers since the ICs are vulnerable to side-channel attacks. Among all the side-channel attacks, differential power analysis (DPA) attack is effective in finding a secret key. Measuring the current from power supply and then performing statistical analysis of the measured power traces can lead to discovery of the secret key. Therefore, development of an energy-efficient encryption processor that is immune to differential power analysis attack is required for the secure transmission and storage of the data in battery-operated security ICs.

The Advanced Encryption Standard algorithm [1] is a block cipher that converts 128-bit plaintext to ciphertext with selectable key lengths (128, 192, or 256 bits). The algorithm is organized as a repeated "round transformation" that includes four types of sub-operations, i.e., "SubBytes," "ShiftRows," "MixColumns," and "AddRoundKey"(Figure 1). For the design of an energy-efficient processor with performance requirement, two architectural approaches can be used with voltage scaling. Since a total of 32 bytes is manipulated in one round of transformation, parallel operation of each byte can compensate for the reduced speed that results from the supply voltage scaling. Pipelining also helps maintain the throughput even with the reduced supply voltage.

The DPA attack is based on the asymmetry in power dissipation, depending on the input data. Dynamic differential logic consumes the same dynamic power regardless of any input data [2], since during the precharge phase, one node is always precharged to VDD, and during the evaluation phase, one node is always discharged to ground. Resistance to DPA attack with dynamic differential logic, however, comes at the expense of increased power dissipation. Therefore, the trade-off between security and power dissipation should be examined carefully and optimized for the specified design purposes.



▲ Figure 1: AES algorithm with a repeated round transformation

References

[1] NIST, "Federal information processing standards PUB 197 advanced encryption standard" (Nov. 2001). [Online]. Available: http://www.nist.go/aes/

[2] I. Verbauwhede, P. Schaumont, and H. Kuo, "Design and performance testing of a 2.29-GB/s Rijndael processor," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 569-572, Mar. 2003.

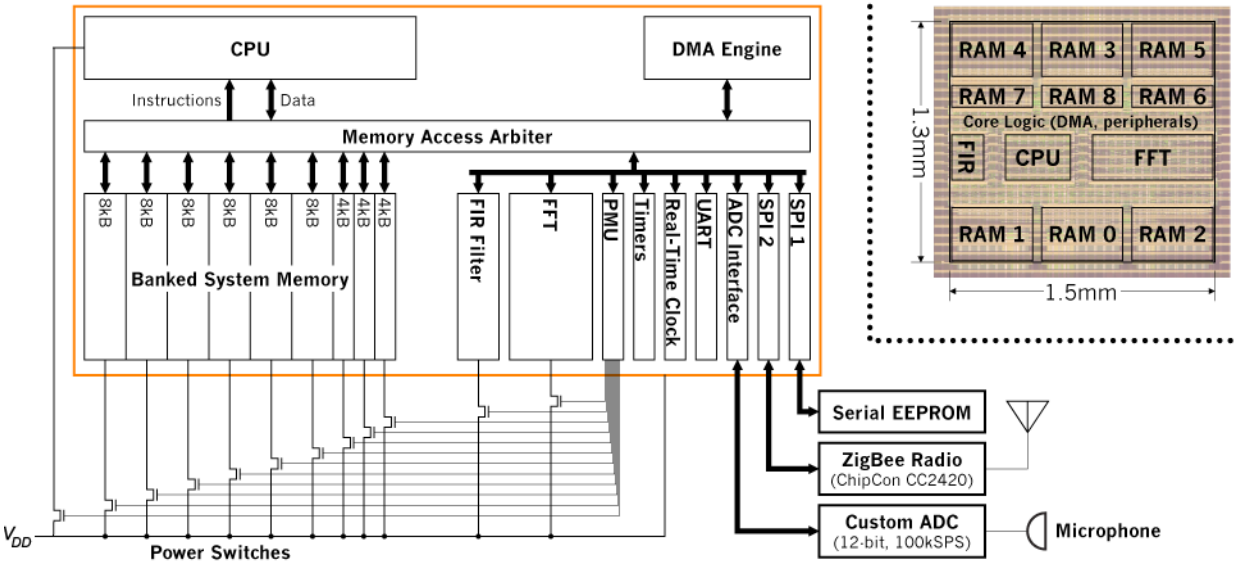
A Micropower DSP for Sensor Applications

N. Ickes, A.P. Chandrakasan

Sponsorship: DARPA, Texas Instruments

Distributed microsensor networks consist of hundreds or thousands of miniature sensor nodes. Each node individually monitors the environment and collects data as directed by the user, and the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. However, the small size and highly distributed arrangement of the individual sensor nodes make aggressive power management a necessity.

The aim of our project is to develop a micropower DSP platform optimized for medium-bandwidth (up to 100 kHz) microsensor applications, such as acoustic sensing and tracking. These applications require significant signal processing capability at each node within a sensor network, while maintaining a roughly 100 µW average power consumption to enable self-powered (energy scavenging) operation. As illustrated in Figure 1, our DSP includes a general-purpose processor core with an energy efficient instruction set, as well as coprocessors for accelerating Fourier transforms and FIR filtering. Power consumption in the large (60 kB) on-chip memory is reduced by dividing the memory into banks (to reduce access energy) and by power-gating inactive banks (to reduce leakage energy). The CPU, FIR, and FFT cores are also power-gated. The DSP was fabricated in 90-nm CMOS by ST Microelectronics.



▲ Figure 1: DSP architecture, illustrating the twelve independent power domains, controlled by off-chip power switches. When combined with an external nonvolatile memory (for program storage), radio, and ADC, the DSP becomes a complete microsensor node. Inset: Die photo of the DSP, implemented in 90-nm CMOS.

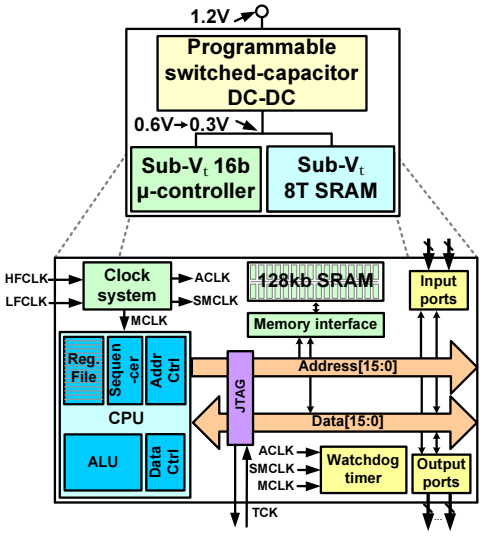
A 65-nm Sub-V_t Microcontroller with Integrated SRAM and DC-DC Converter

J. Kwong, Y. Ramadass, N. Verma, A.P. Chandrakasan

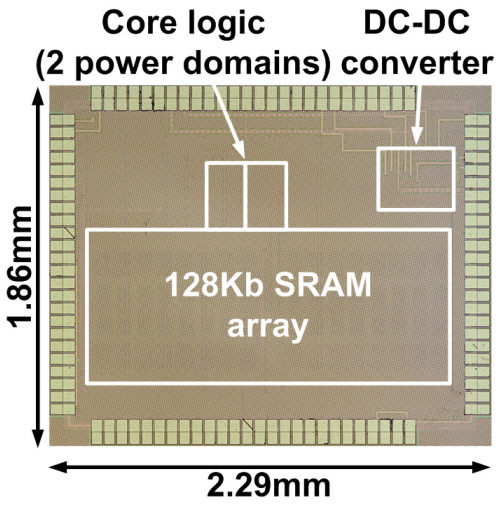
Sponsorship: DARPA, Texas Instruments Graduate Woman's Fellowship (J. Kwong), Intel Foundation Ph.D. Fellowship (N. Verma)

Aggressive scaling of the power supply to below the device threshold voltage (V_t) is a compelling approach for energy minimization in digital circuits [1]. Although circuits exhibit slower speeds at low supply voltages, the trade-off remains attractive for energy-constrained systems with relaxed throughput constraints. However, effects of process variation become more prominent at low supply voltages, impacting functionality. A 65-nm sub-V_t microcontroller (see Figure 1) demonstrates several approaches to enable operation down to 300mV [3]. In sub-V_t, logic gates no longer exhibit rail-to-rail voltage swings due to variation and reduced ratio of on-to-off currents. A standard cell library design methodology increases device sizes appropriately to mitigate these effects [4]. Moreover, circuit delays exhibit order-of-magnitude higher variability at low voltages. Conventional timing analysis approaches that treat delays as deterministic are insufficient. Instead, a variation-aware methodology combining simulation and analysis was developed to verify hold-time constraints.

The SRAM represents a dominant portion of power and area in this system. Therefore, energy and leakage reduction through voltage scaling is highly desirable. In conventional 6-T SRAMs, V_t variation causes severely degraded read-current and increased cell instability, limiting the minimum functional voltage. The SRAM in this chip employs an 8-T bit-cell to address these limitations [5]. Further, peripheral circuit assists enforce the relative device strengths needed for read and write functionality, even in the presence of significant variation. A fully integrated, switched-capacitor DC-DC converter provides highly efficient power delivery at the low voltage and power levels required by energy-constrained systems [6]. Featuring multiple gain settings and efficient control circuitry, the DC-DC converter can deliver variable load voltages and achieves above 75% efficiency while supplying 500mV in the range of 10µW to 250µW. The microcontroller chip (see Figure 2) was fabricated by Texas Instruments.



▲ Figure 1: Block diagram of 65-nm sub-V_t system-on-a-chip and detailed diagram of microcontroller core.



▲ Figure 2: Die micrograph of prototype test-chip.

References

[1] A. Wang, A. Chandrakasan, and S. Kosonocky, "Optimal supply and threshold scaling for sub-threshold CMOS circuits," *Proc. IEEE Computer Society Annual Symposium on VLSI*, Apr. 2002, pp. 7-11.

[2] B. Zhai, L. Nazhandali, J. Olson, et al., "A 2.60pJ/Inst sub-threshold sensor processor for optimal energy efficiency," *IEEE Symposium on VLSI Circuits Dig. Tech. Papers*, June 2006, pp. 154-155.

[3] J. Kwong, Y. Ramadass, N. Verma, et al., "A 65nm sub-V_t microcontroller with integrated SRAM and switched-capacitor DC-DC converter," *IEEE International Solid-State Circuits Conference Dig. Tech. Papers*, Feb. 2008, pp. 318-319.

[4] J. Kwong and A.P. Chandrakasan, "Variation-driven device sizing for minimum energy sub-threshold circuits," *Proc. IEEE International Symposium on Low Power Electronics and Design*, Oct. 2006, pp. 8-13.

[5] N. Verma and A.P. Chandrakasan, "A 65nm 8T sub-V_t SRAM employing sense-amplifier redundancy," *IEEE International Solid-State Circuits Conference Dig. Tech. Papers*, Feb. 2007, pp. 328-329.

[6] Y.K. Ramadass and A.P. Chandrakasan, "Voltage-scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications," *IEEE Power Electronics Specialists Conference*, pp. 2353-2359, June 2007.

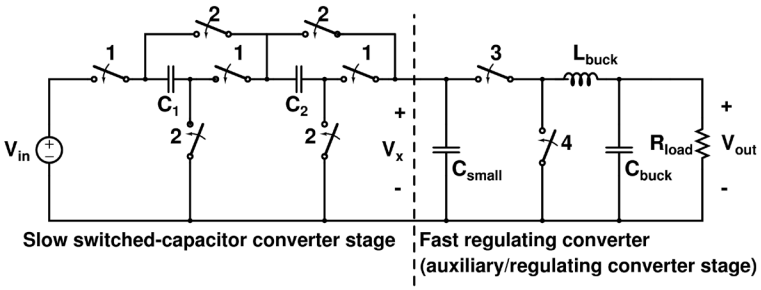
Multi-stage Converter Architectures for Microprocessor Power Delivery

R. Pilawa-Podgurski, D.J. Perreault
Sponsorship: SRC/FCRP IFC

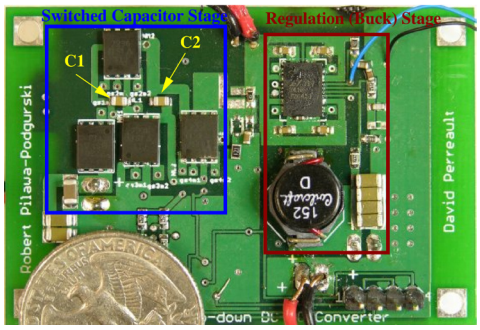
Today's low processor operating voltages and high currents result in increased ohmic losses in the interconnect between the voltage regulator and the processor. To reduce these losses, it is desirable to place a large step-down voltage regulator in close proximity to the processor. This research investigates power converter architectures that make use of available on-die device characteristics to provide large voltage step-down and high bandwidth regulation.

In a given CMOS process, we typically have access to slow devices with a moderate blocking voltage and fast devices with low blocking voltage. Figure 1 shows a proposed multi-stage converter architecture that makes use of these different device characteristics. A switched-capacitor transformation stage utilizing slow, high-voltage switches provides efficient unregulated voltage step-down. This stage is followed by a high-bandwidth magnetic regulation stage, which utilizes fast low-voltage devices. Excellent efficiency and power density can be achieved through this technique, as can large voltage step-down and fast transient response.

Coupling the fast magnetic regulating stage to the switched-capacitor stage in a novel manner can eliminate the current spikes associated with conventional switched–capacitor converters. This "merged two-stage" architecture also improves overall efficiency and drastically reduces the total required capacitance. Figure 2 shows a photograph of a prototype implemented with discrete components [1]. Experimental measurements demonstrate the benefits of the merged two-stage architecture, and this proof-of-concept converter verifies the validity of the approach.



▲ Figure 1: Schematic of proposed merged two-stage converter.



▲ Figure 2: Photograph of merged two-stage converter prototype implemented with discrete components.

Reference

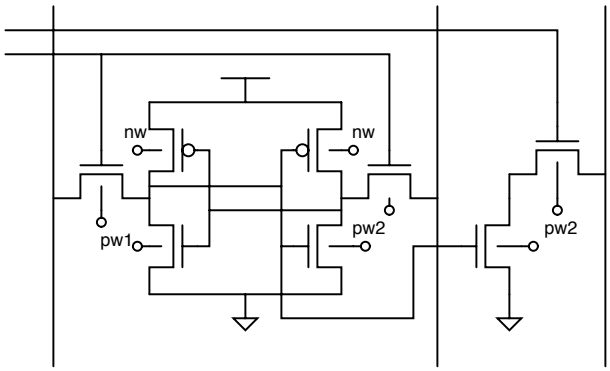
[1] R. Pilawa-Podgurski, D. Giuliano, and D. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," *IEEE Power Electronics Specialists Conference*, Rhodes, Greece, June 2008.

Enhanced Low-voltage 8T SRAM with Body Bias Adjustment

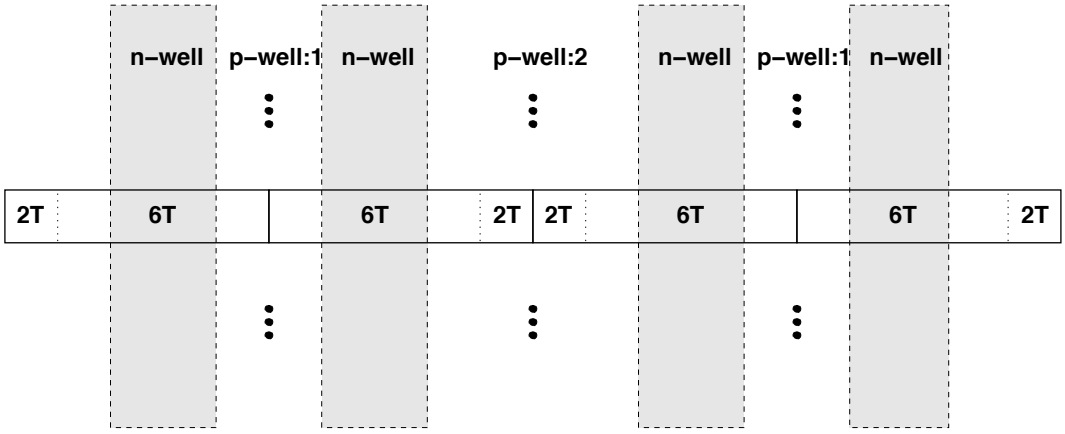
M. Qazi, A.P. Chandrakasan
Sponsorship: SRC/FCRP C2S2

Body bias presents an attractive—albeit low-frequency—mechanism to correct for mean deviations in device parameters because the electrical manipulation in a global fashion of the body terminals of bulk CMOS devices incurs minimal area overhead over standard body contacts. See Figure 2 for the illustration of minimal area penalty for 8T SRAM. Conventional work on body biasing in SRAM [1] focuses on improving yield by optimizing the strength ratio between pfet and nfet for static functionality of the 6T cell. This work focuses on the compelling advantages of 8T SRAM (cell schematic shown in Figure 1) to enable lower VDD operation, akin to prior low-VDD body biasing work on static CMOS digital circuits [2].

The key challenges relate to detecting the optimum body bias. Not only do accelerated leakage currents and junction currents at forward bias and gate oxide reliability degradation at very negative biases set maximum limits for the p-well and n-well voltages, but active retention failures have to be delicately balanced with active write errors. A technique to detect and set the optimum body bias is being developed and implemented in IBM 65-nm bulk CMOS technology.



▶ Figure 1: Shown to the right is the schematic for one 8T cell with the body terminals explicitly marked for each device.



▲ Figure 2: Shown above is the physical layout of the 8T cell array. The nwell and pwell run vertically in alternating strips.

References

[1] S. Mukhopadhyay, K. Kim, H. Mahmoodi and K. Roy, "Design of a process variation tolerant self-repairing SRAM for yield enhancement in nanoscaled CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 1370-1382, 2007.

[2] G. Ono and M. Miyazaki, "Threshold-voltage balance for minimum supply operation," *IEEE Journal of Solid-State Circuits*, vol. 38, pp. 830-833, 2007.

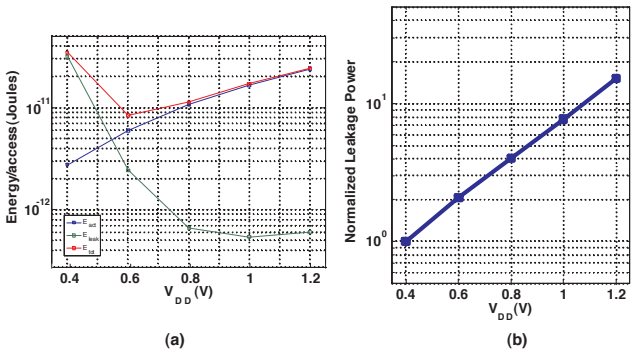
SRAM Design for Ultra-low-power Systems

M.E. Sinangil, N. Verma, A.P. Chandrakasan
Sponsorship: DARPA

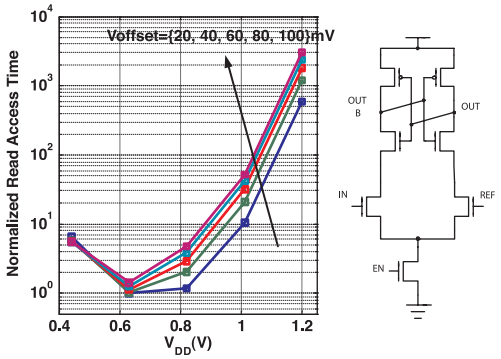
Low-power circuit design has been an important research area because of the ever-increasing need for longer battery life in energy-starved applications. Most digital systems require on-chip memory blocks that dominate not only area but also power consumption. Hence, lowering SRAM voltage is critical. First, this reduces the active energy, which is given by CV_{DD}^2. Figure 1a shows energy/access vs. V_{DD} plot for a 64-kbit SRAM block. The total energy makes a minimum around 400mV because of the opposing trends in the active energy and leakage energy components. Second, leakage-currents also decrease at lower supply voltages, resulting in reduced leakage-power. Figure 1b shows the leakage power vs. V_{DD} plot. The leakage power decreases by ~50X over the range. This significant decrease is due not only to scaling in V_{DD} but also to alleviation of drain-induced barrier lowering (DIBL).

Designing functional SRAMs at lower supply voltages is, however, extremely challenging due to the increasing effects of local variation with device scaling. To maximize density, the bit-cell is designed to be very small, aggravating its variability. Hence, as the supply voltage decreases, read and write failures begin to be highly prominent. Peripheral assists to address these and new bit-cell topologies have been proposed recently in [1] and [2]. However, architectural innovations are also required.

Operating voltage of an SRAM is often bounded by the performance requirement of the system. In such a scenario, the operating voltage can be brought down only if the performance of the SRAM is improved. Figure 2 shows the normalized read access time vs. V_{DD} with different offset voltages for the sense amplifier shown. Since the sense amplifier is in the critical path, its offset directly determines the discharge time, and hence a larger offset translates into a longer access period. In order to acquire the same performance at a lower V_{DD}, sense-amplifier offset voltage should be analyzed. [3] analyzes a very commonly used sense amplifier structure but does not provide a model for the offset. An offset compensation scheme that would trim the reference voltage value to minimize the offset can be implemented. This scheme should be implemented with a reasonable area overhead in order to be applicable to SRAMs.



▲ Figure 1: Simulated energy/access vs. V_{DD} plot (a) and leakage power vs. V_{DD} (b) plot for a 64-kbit SRAM in 65-nm technology.



▲ Figure 2: Normalized read access time vs. V_{DD} plot with different offset voltages for the sense amplifier shown.

References

[1] N. Verma and A.P. Chandrakasan, "A 65-nm 8-T Sub-V_t SRAM employing sense-amplifier redundancy," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2007, pp. 328-329.

[2] T.-H. Kim, J. Liu, J. Keane, and C.H. Kim, "A high-density sub-threshold SRAM with data-independent bitline leakage and virtual ground replica scheme,"*IEEE Int. Solid-State Circuits Conf. (ISSCC) Digest of Technical Papers*, Feb. 2007, pp. 330-331.

[3] B. Wicht, T. Nirschl, and D. S-Landsiedel, "Yield and speed optimization of a latch-type voltage sense amplifier," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1148-1158, July 2004.

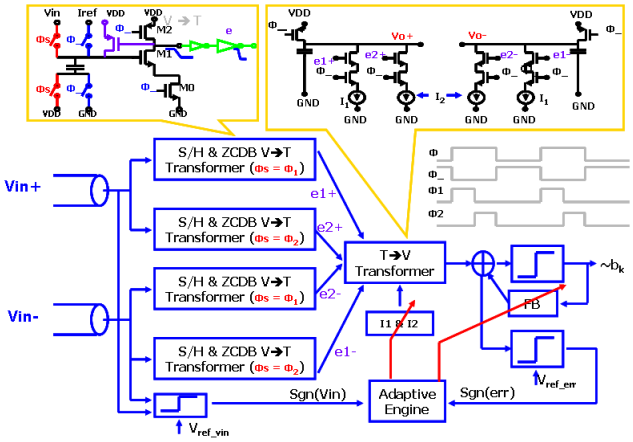
An Adaptive Fractionally Spaced Receive Equalizer

S. Song, V. Stojanović

Sponsorship: National Semiconductor

Based on voltage-to-time conversion technique [1], a pseudo-differential two-way-interleaved adaptive receive equalizer with two 2x-oversample feed-forward taps and one feedback tap has been designed in 90-nm CMOS process. It integrates equalization and phase interpolation functions into one unit to simultaneously address intersymbol-interference cancellation and phase synchronization in a link receiver. According to post-layout simulation, the receiver can operate at 6 Gbps with 6.48 mW of power. The filter is two-way interleaved to overcome technology speed limitations. Figure 1 shows block and circuit diagrams for one direction. The zero-crossing-detector circuit functions as a voltage-to-time converter followed by a dynamic discharger stage that works as a multiplying time and voltage converter. In comparison with [1], a positive feedback PMOS with gate connected to the drain of M1 can reduce t_f by more than 15%. Buffers are placed at the output to increase the driving ability. A data-conditioned sign-sign least-mean squares algorithm has been developed off-chip, to tune the filter coefficients and overcome the convergence issues due to strong signal correlation. Figure 2 shows the power partition from the post-layout simulation, indicating a 1-pJ/bit overall energy-cost for the receiver.

Tuning the external discharge currents I_1, I_2, and bias current for the slicer adjusts the feed-forward/feedback tap weights. On the band-limited channels, 2x oversampling is enough to reconstruct the signal sample completely, regardless of the phase. Tuning the tap weights I1 and I2 makes it possible to reopen the eye, no matter what the phase offset between Tx and Rx. Therefore, it not only equalizes the channel but also alleviates the requirement for an explicit phase synchronization loop. In links that employ decision-feedback equalization at the receiver, these phase synchronization loops are difficult to design due to the excessive amount of intersymbol-interference-induced jitter at symbol edges (i.e., the points at which the circuit derives the timing error information), leading to poor performance of synchronization.



▲ Figure 1: System structure for one way of equalizer. The adaptive engine's inputs are from one direction but its outputs, including I1, I2 and FB tap weight, are shared between the two branches, enabling fully differential operation.

CLK buffer and regeneration	2.88mW
V→T and T→V conversion	1.92mW
Signal and error detectors	0.18mW
DFE	1.5mW
Total	6.48mW

▲ Figure 2: Power partition based on post-layout simulation with 6- Gbps data rate and 1.2-V supply.

Reference

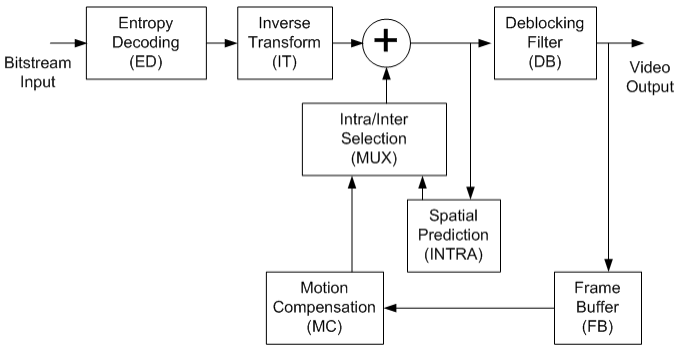
[1] L. Brooks and H.-S. Lee, "A zero-crossing-based 8b 200 MS/s pipelined ADC," *IEEE Journal of Solid-state Circuits*, vol. 42, no. 12, Dec. 2007.

Algorithms and Architectures for Ultra-low-power Video Compression

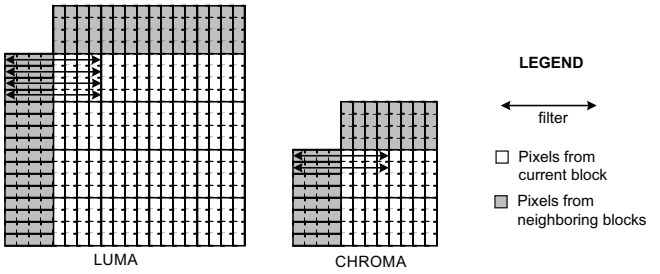
V. Sze, D. Finchelstein, A.P. Chandrakasan
Sponsorship: Nokia, Texas Instruments

Multimedia applications, such as video playback, are becoming increasingly pervasive. Since the platforms are often energy-constrained devices (cell phones, iPods), the user experience is enhanced by extending the battery life during video decoding. The latest video coding standard is H.264 [1], and it is used in DVB-H and HDTV. While it provides a 50% improvement in compression efficiency over previous standards, this coding efficiency comes at the cost of increased decoder complexity of 4X over MPEG-2 and 2X over MPEG-4 Visual Simple Profile. This increased complexity translates to increased energy consumption, which is a critical concern for mobile and handheld devices.

Our aim is to build an ASIC decoder that exploits techniques such as memory optimization, pipelining, parallelism, ultra-low-voltage operation, and ultra-dynamic voltage scaling [2]. For instance, the Deblocking Filter computation can be parallelized as shown in Figure 2. In video decoders, memory consumes a large portion of overall system power. As a result, the number of redundant memory transfers must be minimized and caching data in on-chip SRAMs/registers is paramount. Using these techniques, the goal is to reduce system power even further than previously published decoders [3]. In addition to optimizing the hardware architecture of the H.264 decoder (Figure 1), we will also focus on the design of next-generation video coding algorithms, e.g., "H.265." We envision that these algorithms will account for the energy and complexity costs of their hardware implementations. By incorporating the energy-awareness into the algorithm, future video coders can provide an explicit energy/PSNR trade-off, along with the existing bitrate/PSNR trade-off curves.



▲ Figure 1: H.264 video decoder architecture.



▲ Figure 2: Parallel Deblocking Filters

References

[1] ITU-T Study Group, "Series H: Audiovisual and multimedia systems: Infrastructure of audiovisual services – coding of moving video," in *General Secretariat and Telecom Radiocommunication (ITU-R) Standardization (ITU-T)*, sec. H, no. 264, Sept. 2005.

[2] B.H. Calhoun and A.P. Chandrakasan, "Ultra-dynamic voltage scaling using sub-threshold operation and local voltage dithering in 90nm CMOS," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2006, pp. 300-301.

[3] C.D. Chien et. al., "A 252kgate/71mW multi-standard multi-channel video decoder for high-definition video applications," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb 2007, pp. 282-283.

A High-density 45-nm SRAM Using Small-signal Non-strobed Regenerative Sensing

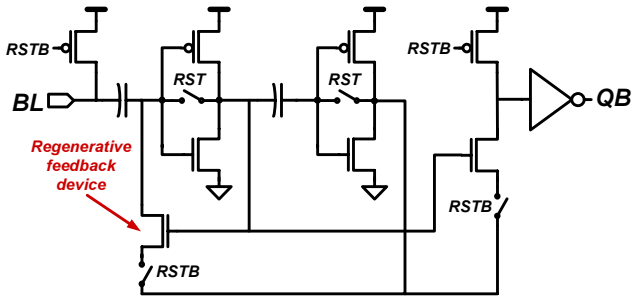
N. Verma, A.P. Chandrakasan

Sponsorship: CICS, Intel Foundation Ph.D. Fellowship Program

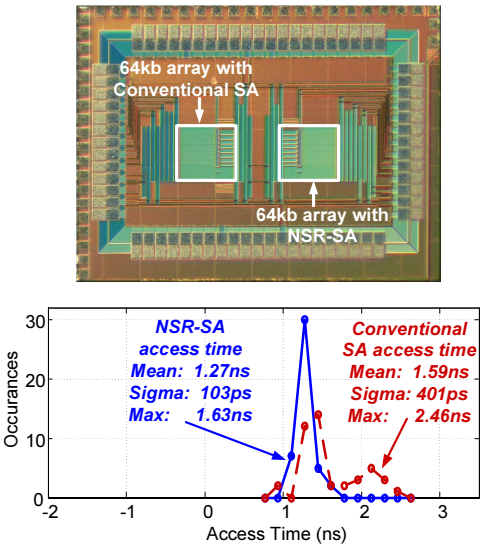
High-density embedded SRAMs are critical enablers of the tremendous integration trends benefiting integrated circuits every technology node. Their wide use of aggressive minimum-sized features, however, severely aggravates variability, leading to numerous limitations across the entire array. Some of the most critical among these include highly degraded static-noise-margin (SNM) [1] and cell read-current due to the use of small bit-cells; the need to increase sense-amplifier area in order to reduce its variation and input-offset [2] to withstand the lower read-currents; and finally, excessive margining in the sense-amplifier strobe signal, which is required to overcome its severe tracking divergence across operating corners, with respect to the array read-path.

In order to simultaneously address all of these issues, we present the non-strobed regenerative sense-amplifier (NSR-SA), shown in Figure 1 [3]. It performs very simple offset compensation to overcome the sense-amplifier offset-area trade-off without significantly loading the high-speed nodes. The resulting improvement in stability, even in the presence of extreme variation, implies that a small cell read-current can be accommodated for the same array performance, and, accordingly, the bit-cell can be optimized for other parameters, such as read SNM. Lastly, the presence of stable internal voltage references, generated thanks to the offset compensation, is exploited to trigger self-regeneration with respect to the input bit-line voltage itself, rather than to an explicit external control path. The test-chip, fabricated in 45-nm CMOS, employs high-density 0.25-μm² bit-cells and is shown in Figure 2. Measurements from 53 die show an improvement in the sigma of the delay distribution by a factor of four compared to a conventional sense-amplifier, confirming the benefit of offset-compensation and self-regeneration.

IC fabrication is provided by Texas Instruments.



▲ Figure 1: Non-strobed regenerative sense-amplifier circuit schematic.



▲ Figure 2: Test-chip die photo and measurement results from 53 chips.

References

[1] A. Bhavnagarwala, X. Tang, and J. Meindl, "The impact of intrinsic device fluctuations on CMOS SRAM cell stability," *IEEE Journal of Solid-State Circuits*, vol. 36, no. 4, pp. 658-665, Apr. 2001.

[2] K. Zhang, K. Hose, V. De, and B. Senyk, "The scaling of data sensing schemes for high speed cache design in sub-0.18μm technologies," in *Proc. IEEE Symposiumon VLSI Circuits*, June 2000, pp. 226-227.

[3] N. Verma and A.P. Chandrakasan, "A high-density 45nm SRAM using small-signal non-strobed regenerative sensing," *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, Feb. 2006, pp. 328-329.

Systematic Information-fusion Methodology for Static and Dynamic Obstacle-detection in ITS

Y. Fang, B.K.P. Horn, I. Masaki

Sponsorship: Intelligent Transportation Research Center, MTL

Environment-understanding technology is very vital for intelligent vehicles that are expected to respond automatically to fast-changing environments and dangerous situations. To obtain perception abilities, we should automatically detect static and dynamic obstacles and obtain their related information, such as locations, speed, possibility of collision or occlusion, and other dynamic current or historic information. Conventional methods independently detect individual information, which is normally noisy and not very reliable. Instead we propose fusion- and layered-based information-retrieval methodologies to systematically detect obstacles and obtain their location and timing information for visible and infrared sequences. The proposed obstacle-detection methodologies take advantage of connections among different pieces of information and increase the computational accuracy of obstacle information estimation, thus improving environment-understanding abilities and driving safety. Figures 1 and 2 show two examples.

▲ Figure 1: Segmentation result for urban daytime driving environment.

▲ Figure 2: Segmentation result for night driving environment.

References

[1] A.R. Bruss and B.K.P. Horn, "Passive navigation," *Computer Vision, Graphics, and Image Processing*, vol. 21, no. 1, pp. 3-20, Jan. 1983.

[2] J.E. Tanner, "Integrated optical motion detection," Ph.D. Thesis, California Institute of Technology, Pasadena, CA, Technical Report 5223:TR:86, 1986.

[3] J.E. Tanner and C.A. Mead, "An integrated analog optical motion sensor," *VLSI Signal Processing II, (Proc. of the ASSP Conference on VLSI Signal Processing)*, UCLA, Nov. 5-7, 1986, pp. 59-76..

[4] B.K.P. Horn and S.Negahdaripour, "Direct passive navigation," *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. PAMI-9, no. 1, pp. 168-176, Jan. 1987.

[5] B.K.P. Horn, "Motion fields are hardly ever ambiguous," *International Journal of Computer Vision*, vol. 1, no. 3, pp. 259-274, Oct. 1987.

[6] B.K.P. Horn and E.J. Weldon, Jr., "Direct methods for recovering motion," *International Journal of Computer Vision*, vol. 2, no. 1, pp. 51-76, Jun. 1988.

[7] Y. Fang, K. Yamada, Y. Ninomiya, B.K.P. Horn, and I. Masaki, "Comparison between infrared-image-based and visible-image-based approaches for pedestrian detection," *Proc. IEEE Intelligent Vehicles Symposium*, 2003, pp. 505--510.

[8] Y. Fang, K. Yamada, Y. Ninomiya, B.K.P. Horn, and I. Masaki, "A shape-independent-method for pedestrian detection with Far infrared-images," special issue on "In-Vehicle Computer Vision Systems" of *IEEE Transactions on Vehicular Technology*, vol. 53, no.6, pp. 1679-1697, Nov. 2004.

[9] B.K.P. Horn, Y. Fang, and I. Masaki, "Time to contact relative to a planar surface," presented at the *IEEE Intelligent Vehicles Symposium*, 2007.

2

Electronic Devices & Emerging Technologies

MTL microsystems technology laboratories
massachusetts institute of technology

Annual Research Report
September 2008

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GaN-Based DNA Detectors

J. Wu, O. Saadat, T. Palacios
Sponsorship: MIT, MIT-France Program

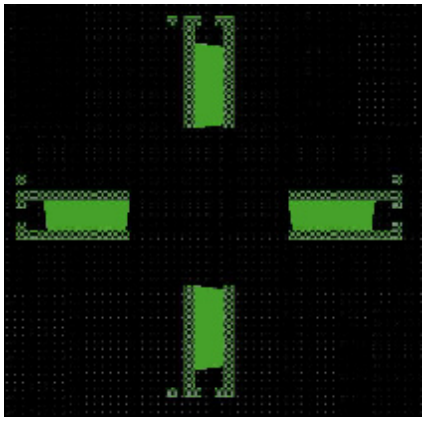
The ability to detect DNA hybridization is an extremely useful tool that can be used in a variety of biological and medical tests. Currently, the use of microarrays and optical detection is the predominant technology to detect hybridization. However, this technology is slow, requires extensive optical systems and alignment as well as, in many cases, special labeling of at least one of the strands. Although electrical detection of DNA hybridization could overcome many of these problems, no reliable method has yet been developed.

Our group is exploring three new technologies to electrically detect DNA hybridization: surface acoustic wave (SAW) two-dimensional tomography, a quantum-dot conductance sensor and a high electron mobility transistor (HEMT) –based sensor. These technologies primarily rely on the charge and mass changes that occur when single strands hybridize and are based on the excellent properties of nitride semiconductors. These materials are excellent for biological sensors due to their biocompatibility, excellent transport properties and unprecedented chemical stability.

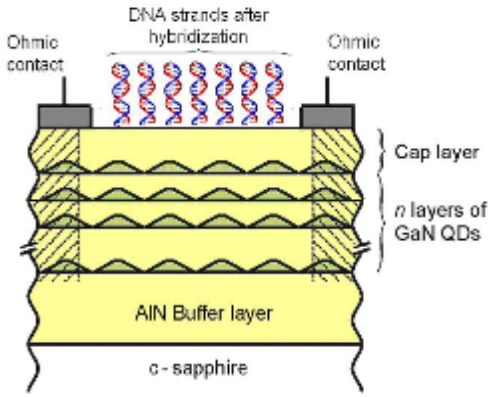
The SAW sensor takes advantage of the piezoelectric properties of GaN to generate acoustic waves which travel along the surface of the semiconductor. These waves are affected by the material through which they travel and the mass of the molecules on top (i.e., DNA). The magnitude of the signal generated by the receiving electrode at varying frequencies allows for a measurement of the mass of the molecule on the surface. In the new devices being developed in our group, both the input and output electrodes are tapered in order to achieve spatial selectivity.

In collaboration with CEA-Grenoble (France), we are also developing a new kind of conductance sensor, which measures the effect of charges' electric field on a semiconductor. To increase the sensitivity of the device, an AlN layer containing layers of GaN quantum dots very close to the sensing surface has been fabricated. The exponential dependence in the hopping conduction through the quantum dot layer is expected to allow unprecedented levels of sensitivity in this new device.

The third sensing device being developed is based on GaN HEMTs. Conventional transistor-based sensors operate in a similar way to conductance sensors, and are thus subject to similar problems. Using an entirely different method of measurement may increase the signal to noise ratio. Instead of using the charged DNA to change the gate voltage and resulting current, we are positioning the DNA in the drain access region of the device in order for a change in charge to affect the parasitic capacitance of the transistor and, consequently, the switching frequency. We can then detect whether the single strand of DNA has successfully hybridized by checking if the maximum switching frequency has increased.



▲ Figure 1: Top view of the SAW-based two-dimensional DNA sensor.



▲ Figure 2: Cross-section of the quantum-dot conductivity sensor being developed in our lab.

Transport Properties and Advanced Device Simulation of AlGaN/GaN Transistors

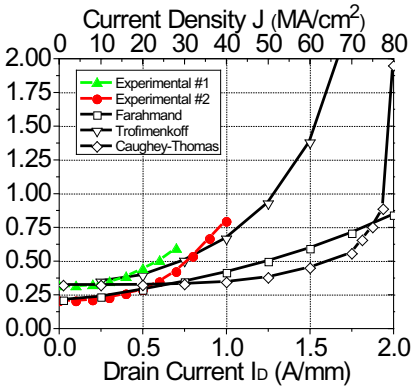
J.M. Tirado, Z. Xu, B. Lu, T. Palacios
Sponsorship: ONR, DARPA

The small signal access resistance (r_s) of AlGaN/GaN high-electron mobility transistors (HEMTs) plays a critical role in the performance of these transistors. Its importance increases with drain current limits the transconductance, frequency performance, linearity, and efficiency of GaN transistors [1]. This work studies the origin of this increase through a combination of theoretical and experimental approaches. The quasi-saturation of the electron velocity with the electric field due to the emission of optical phonons has been identified as the main reason for the increase.

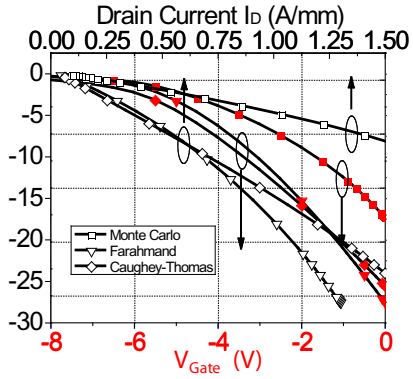
We have solved the Poisson equation in the channel on an AlGaN/GaN HEMT to calculate the variation of the longitudinal electric field in the source access region as a function of distance and current density. Three different transport models have been analyzed: (a) Farahmand [2], (b) Trofimenkoff [3], and (c) Caughey-Thomas [4]. The source access resistance in an AlGaN/GaN HEMT with a source to gate distance of 0.8 μm was evaluated as a function of drain current. There is an important nonlinear behavior of the resistivity as the current density is increased. The small signal access resistance of several devices was experimentally measured and compared to theoretical results as it is plotted in Figure 1. Two AlGaN/GaN HEMT devices grown by MOCVD on SiC substrates and different layer compositions were considered. As shown in this figure, excellent agreement between the experimental and the theoretical results has been obtained.

To get more insight into the reasons for the increasing access resistance, a two-dimensional commercial device simulator (Silvaco Atlas) has been used to calculate the electric field in the source access region of a GaN HEMT. The three different transport models were added to the Atlas simulations. Figure 2 shows the results of these simulations. In all the cases, the longitudinal electric field in the source access region is in the 10-30 KV/cm range, a region where the differential mobility is changing very rapidly. From our simulations and modeling, this change in mobility is the dominant cause of the increase of r_s.

In conclusion, our theoretical model, simulations and experimental work indicate that the electron transport in the 30-40 KV/cm range is better described by a Trofimenkoff model than by the different Monte Carlo simulations reported in literature, which indicates that current Monte Carlo techniques are overestimating the mobility at moderate electric fields.



▲ Figure 1: Small signal access resistance, r_s versus drain current I_D (and current density J) calculated for the three transport models considered in this work. The experimental values measured in two different samples are also plotted for comparison.



▲ Figure 2: Electric field versus gate voltage V_G (and drain current I_D) extracted from simulations using Atlas. Each curve belongs to a different transport model: (a) Monte Carlo, (b) Farahmand, and (c) Caughey-Thomas. Values are extracted from the middle point of the distance between S-G contacts.

References

[1] T. Palacios, S. Rajan, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, and U.K. Mishra, "Influence of the dynamic access resistance in the g_m and f_T linearity of AlGaN/GaN HEMTs," *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2117-2123, Oct. 2005.

[2] M. Farahmand, C. Garetto, E. Belloti, K.F. Brennan, M. Goano, E. Ghillino, G. Ghione, J.D. Albrecht, and P.P. Ruden, "Monte Carlo simulation of electron transport in the III-nitride wurtzite phase materials system: Binaries and ternaries," *IEEE Transactions on Electron Devices*, vol. 48, no. 3, pp. 535-542, Mar. 2001.

[3] F.N. Trofimenkoff, "Field-dependent mobility analysis of the field-effect transistor," *IEEE Proceedings*, vol. 53, no. 11, Nov. 1965, pp. 1765-1766.

[4] D.M. Caughey and R.E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," *IEEE Proceedings*, vol. 55, no. 12, Dec. 1967, pp. 2192-2193.

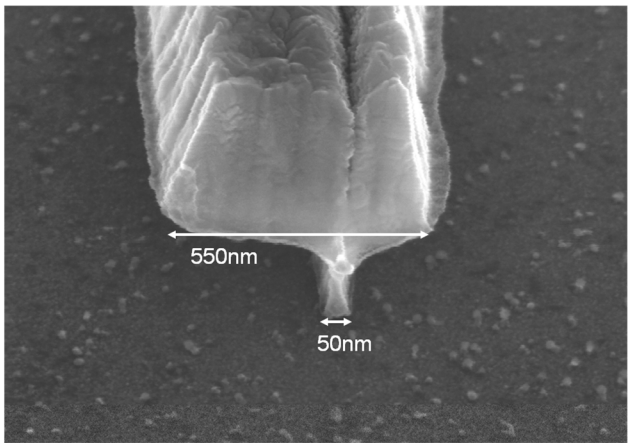
GaN Transistors for W-band Applications

O. Saadat, J.W. Chung, F. Miéville, T. Palacios
Sponsorship: ONR

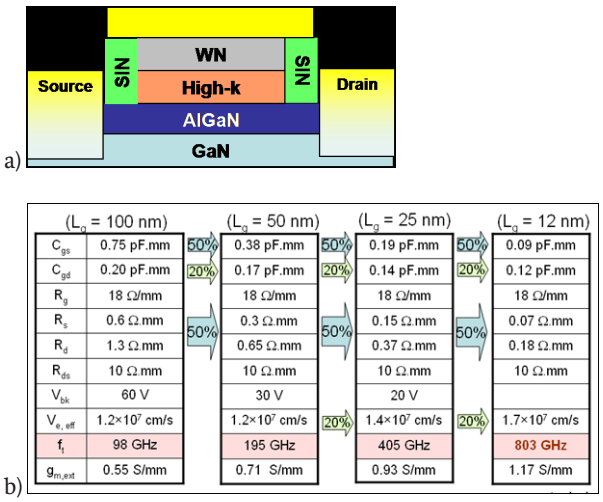
Many applications await the development of compact solid-state amplifiers at frequencies above 30 GHz. Satellite transponders, anti-collision car radars, high-speed point-to-point wireless transmitters, and highly efficient radars for the Navy are only a few of the many civil and military applications that would benefit from these amplifiers in the 30- to 94-GHz range. The basic requirements are common to all these applications: small, reliable, efficient, and low-noise solid-state amplifiers to substitute traveling-wave-tube amplifiers currently used at these frequencies.

GaN-based high electron mobility transistors (HEMTs) are the most promising option for power amplification at frequencies above 30 GHz. However the use of AlGaN/GaN HEMTs at these high frequencies requires the aggressive shrinking of several critical dimensions of transistors. For example, reducing the gate length is crucial for increasing high frequency performance. Therefore, we have fabricated AlGaN/GaN HEMTs with gates with L_g = 50 nm. These devices, shown in Figure 1, have gates defined by the Raith 150 e-beam lithography system.

In addition to reducing the gate length, we need to reduce the source and drain access resistances by reducing the distances between the source and gate and the drain and gate, respectively [1]. Self-aligned gates will reduce these distances. However, we need a gate stack that can stand the 870°C anneal required to form ohmic contacts. Since the standard Ni/Au/Ni rectifying gate stack does not survive these high temperature anneals, we are developing new gate stacks based on the integration of a high-k dielectric like HfO_2 and a refractory metal like WN. Similar gate stacks for Si devices are able to stand more than 900°C anneals, which makes them promising for self-aligned gates on AlGaN/GaN HEMTs [2]. The dielectric and the gate metal used in this project are deposited in situ by atomic layer deposition, which allows for both atomic layer precision and a clean interface between the high-k dielectric and the gate metal. After the gate is defined, insulating sidewalls are deposited to isolate the gate from the source and drain before depositing the source and drain metal and annealing the metal. A proposed structure for the completed self-aligned gate appears in Figure 2a.



▲ Figure 1: Scanning electron micrograph of an AlGaN/GaN HEMT with a 50-nm gate fabricated at MTL.



▲ Figure 2: a) Proposed structure for a self-aligned AlGaN/GaN HEMT and b) performance roadmap for sub-mm-wave GaN HEMTs.

References

[1] P.J. Tasker and B. Hughes, "Importance of source and drain resistance to the maximum fT of Millimeter-Wave MODFET's," *IEEE Electron Device Letters*, vol. 10, no. 7, pp. 291-293, July 1989.

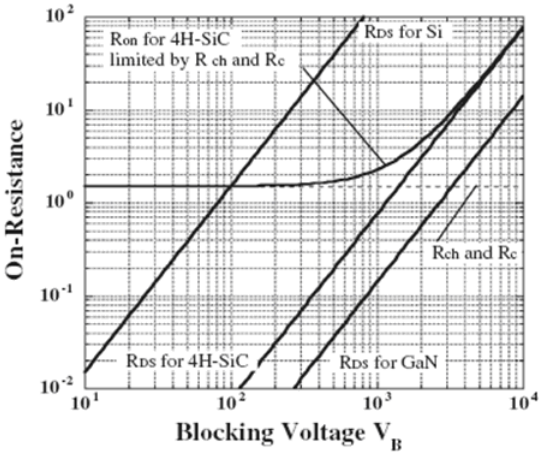
[2] J.K. Schaeffer, "Hafnium dioxide gate dielectrics, metal gate electrodes and phenomena occurring at their interfaces," Ph.D. thesis, University of Texas, Austin, 2004.

Nitride-based Power Electronics

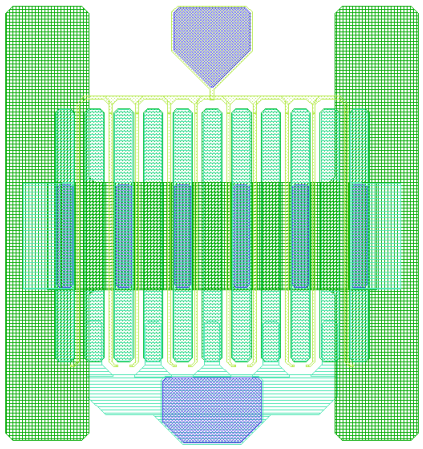
B. Lu, D.J. Perreault, T. Palacios
Sponsorship: MIT, MTL, MITEI

The wide-band-gap III-nitride semiconductors are extremely promising materials for power electronic applications where power switches with high breakdown voltage and ultra-low on-resistance are required. The AlGaN/GaN transistor has unprecedented current-carrying capability due to the extremely high 2-dimensional electron gas density (>1.3×10^{13}cm^{-2}) and mobility (>2000cm^2/V·s) at the heterojuction [1]. The same material system has a very high critical electric field of more than 5 MV/cm. This combination significantly reduces the loss of GaN-based power transistors. Since the total loss (conduction loss and switching loss) of a power switch is reversely proportional to $\mu^{1.5}E_c$ [2], theoretically the total loss of the GaN-based power switches will be about 14 times smaller than Si-based transistors and the switching frequency will be 200 times higher. Figure 1 compares the blocking voltage and on-resistance of GaN with Si and 4H-SiC.

In spite of the great interest of the industry and academia in this material system, its application in power electronics has been hindered until now due to the normally-on character of the state-of-the-art AlGaN/GaN heterojunction field effect transistors. Also, traditionally they are horizontal devices, which are not preferred in power electronics. Our group is working on the design and fabrication of new transistor structures to overcome these two important limitations. Some of the applications of the vertical normally-off GaN-based power devices in our group include the power inverters for hybrid vehicles and power converters for new power delivery systems in microprocessors.



▲ Figure 1: Blocking voltage V_B vs. on-resistance R_{on} for Si, 4H-SiC and GaN [3].



▲ Figure 2: Structure of multi-finger power transistor developed at MIT.

References

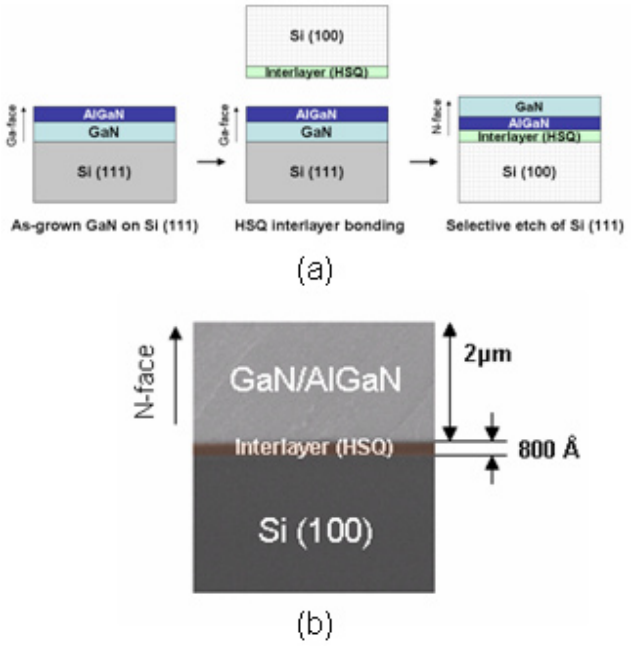
[1] T. Palacios, "Optimization of the high-frequency performance of nitride-based transistors," Ph.D. thesis, University of California at Santa Barbara, 2006.
[2] B.J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455-457, Oct. 1989.
[3] H. Okumura, "Present status and future prospect of widegap semiconductor high-power devices," *Japanese Journal of Applied Physics*., vol. 45, no. 10A, pp. 7565-7586, 2006.

N-face GaN/AlGaN HEMTs on Si (100) Substrate

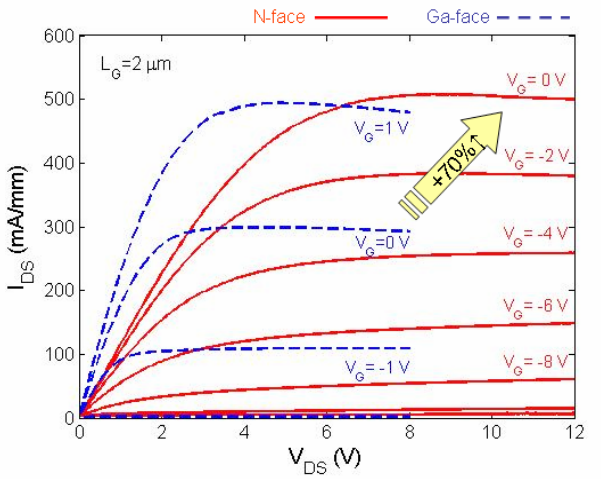
J.W. Chung, T. Palacios
Sponsorship: DARPA, MIT, MTL

Nitride-based transistors are revolutionizing power electronics and high-frequency amplifiers due to their combination of high current densities and large breakdown voltage. Although most of the reported GaN devices have been fabricated on nitride structures grown along the c-direction (i.e., the Ga-face), N-face GaN/AlGaN transistors have the potential for higher electron confinement and lower contact resistances. However, in spite of this promise, the performance of N-face devices is still much lower than in Ga-face devices due to the inferior material quality. Although N-face devices have been grown by molecular beam epitaxy and, recently, by metal-organic chemical vapor deposition (MOCVD), the growth of N-face nitrides is much more challenging than the growth of the more stable Ga-face structure. In this paper, we present a new method to fabricate N-face GaN/AlGaN HEMTs based on the substrate removal of a Ga-face AlGaN/GaN layer grown on Si.

The Ga-face AlGaN/GaN transistor structures used in this work were grown on Si (111) substrates by MOCVD at Nitronex. To have access to the N-face of these samples, we have developed the substrate transfer technology shown in Figure 1a. First, the Ga-face surface was bonded to a Si (100) carrier wafer by using a hydrogen silsesquioxane (HSQ) interlayer. After the wafer bonding, the original Si (111) substrate is completely removed by dry etching using an SF_6-based plasma. Figure 1b shows a scanning electron micrograph of the AlGaN/GaN layer transferred to the Si (100) substrate. After the substrate transfer, the N-face GaN buffer is etched by electron cyclotron resonance-reactive ion etching (ECR-RIE) with Cl_2/BCl_3 gas mixture until the desired distance between the N-face GaN surface and the AlGaN/GaN interface is achieved. The N-face GaN/AlGaN structures fabricated through the substrate removal process have been used in the fabrication of N-face high electron mobility transistors (HEMTs). In this sample, the distance between the N-face surface and the 2DEG was reduced to 1000 Å by ECR etch. Figure 2 shows the drain current versus drain voltage characteristic of the N-face device and it is compared to a Ga-face HEMT used as a reference. For a gate voltage of 0 V, the maximum current in the N-face device is almost 70% higher than in the Ga-face device. This difference is mainly due to the higher charge density in the N-face device.



▲ Figure 1: (a) Main processing steps in the fabrication of N-face GaN on Si (100) substrate through substrate removal. (b) Cross-section scanning electron microscope (SEM) picture of the AlGaN/GaN layer transferred to the Si (100) substrate. False color has been added to highlight the HSQ interlayer in the structure.



▲ Figure 2: The DC current-voltage characteristics of N-face (solid line) and Ga-face (dashed line) HEMTs with a gate length (L_G) of 2 μm. Almost 70% higher maximum current at V_G=0 V is achieved in N-face HEMTs. Higher on-resistance (R_{on}) in N-face HEMTs is due to unoptimized ohmic contacts.

Suitability of GaN Semiconductors for Digital Electronics

F. Miéville, J.W. Chung, T. Palacios
Sponsorship: MIT, MTL

In this work, we study the suitability of nitride-based high electron mobility transistors (HEMTs) for a beyond-Si digital electronic scenario. Table 1 shows some of the formidable challenges that Si devices face in the next few years as well as some of the new solutions offered by GaN-based electronics.

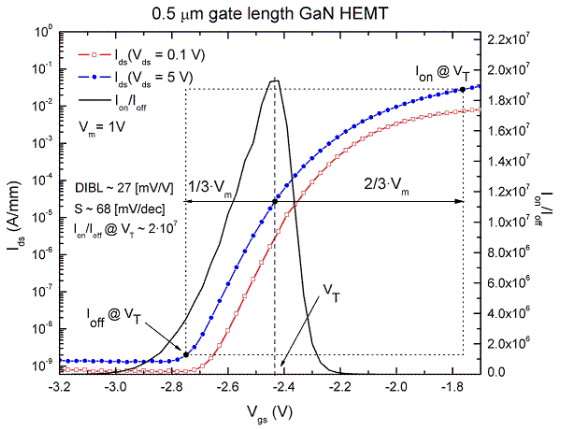
The outstanding properties of nitride semiconductors could be extremely useful in ultra-scale digital electronics. For example, the large bandgap of nitrides allows a significant reduction in the band-to-band tunneling leakage current with respect to Si and other III-V devices. The high dielectric constant of AlN in combination with its very high polarization coefficients allows the fabrication of nitrides devices with an equivalent thickness (EOT) of only 0.6 nm and a charge density in excess of $2{\cdot}10^{13}$ electrons/cm^{-2} (without random dopant fluctuations). Moreover, the very high electron velocity, (> $2.5{\cdot}10^{7}$ cm/s) coupled with the charge density has already allowed the demonstration of current densities above 3 mA/μm in short channel devices.

Our first generation of submicron GaN HEMTs (0.5-μm gate length) for digital electronics grown on Si substrate has already shown excellent performance through the figures-of-merit for logic [1]. Indeed sub-threshold slope *S*, ratio *Ion/Ioff* and drain-induced barrier lowering *DIBL* extracted in Figure 1 are better than in the actual state-of-the-art 65-nm gate length Si nMOS transistors: S = 85 mV/dec, DIBL = 120 mV/V and $I_{on}/I_{off} = 3.1{\cdot}10^{4}$ [2]. Regarding the high-frequency performance, a maximum current gain cut-off frequency (f_T) of 163 GHz and a power gain cut-off frequency (f_{max}) of 230 GHz were already achieved in 90-nm gate length GaN HEMTs on silicon carbide (SiC) substrate [3]. The characterization of below-50-nm devices is part of our ongoing work,

In conclusion, the unique properties of nitrides combined with advanced technologies make nitride materials very attractive options for addressing some of the formidable challenges of digital electronics and for continuing Moore's law beyond the 22-nm node.

	Si Roadmap Challenges	Solutions offered by GaN-based electronics
Low power dissipation	Drain to source and Band to Band tunneling	Large E_g (3.4 eV) reduces tunneling
	Low gate leakage	Crystalline AlN cap layer, low interface state density, high-k barrier, fluorine treatment
Excellent channel control	Enhanced gate control	High effective mass, quantum capacitance
High current	Discrete dopant fluctuations	Polarization doping
	Parasitic resistance	Highly doped InN and polarization grading
	Electron velocity and mobility	V_e ~ 3x10^7 cm/s For L_g < 10 nm → $v_{ballistic}$ ~ 7 x10^7 cm/s
	High current density	> 2 A/mm already achieved on large devices 1.3 A/mm in E-mode devices

▲ Table 1: Main challenges for Si technology, according to the International Technology Roadmap for Semiconductor, and some solutions offered by a nitride-based electronics.



▲ Figure 1: Main logic-related figures of merit for a 0.5–μm gate length GaN HEMT. The definitions used are proposed by Chau *et al.* [1].

References

[1] R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, "Benchmarking nanotechnology for high-performance and low-power logic transistor applications," *IEEE Transactions on Nanotechnology*, vol. 4, no. 2, pp. 153-158, Mar. 2005.

[2] C. Jan, P. Bai, J. Choi, G. Curello, S. Jacobs, J. Jeong, K. Johnson, D. Jones, S. Klopcic, J. Lin, N. Lindert, A. Lio, S. Natarajan, J. Neirynck, P. Packan, J. Park, I. Post, M. Patel, S. Ramey, P. Reese, L. Rockford, A. Roskowski, G. Sacks, B. Turkot, Y. Wang, L. Wei, J. Yip, I. Young, K. Zhang, Y. Zhang, M. Bohr, and B. Holt, "A 65-nm ultra-low-power logic platform technology using uni-axial strained silicon transistors," in *Proc. 2005 IEEE International Electron Devices Meeting*, Washington, USA, Dec. 2005, pp. 60-63.

[3] T. Palacios, A. Chakraborty, S. Heikman, S. Keller, S.P. DenBaars, and U.K. Mishra, "AlGaN/GaN high electron mobility transistors with InGaN back-barriers," *IEEE Electron Device Letters*, vol. 27, no. 1, pp. 13-15, Jan. 2006.

Reliability of GaN HEMTs Grown on Si Substrate

S. Demirtas, J.A. del Alamo
Sponsorship: ARL

GaN has attracted great attention recently as a new material for high electron mobility transistors (HEMT) due to its wide band gap (3.4 eV) and high breakdown field value (>3x10^6 V/cm). These unique properties enable high-voltage, high-power RF operation. The main hindrance to the deployment of GaN HEMTs in such applications is their limited reliability. Recent reliability studies on GaN HEMTs grown on SiC substrates have helped identify the physical mechanisms responsible for degradation [1]. However, silicon, due to its low cost, availability in large diameters and well characterized electrical and thermal characteristics, is a very attractive substrate alternative to SiC. The problem is that with greater lattice and thermal mismatch than in the case of a SiC substrate, GaN layers grown on silicon substrates tend to have many more dislocations. This brings additional concerns to the reliability of GaN HEMTs fabricated on Si substrates.

Our research is focused on the electrical reliability of GaN HEMTs on silicon substrates. We perform our reliability experiments on industrial devices provided by our collaborator, Nitronex Corporation. In these experiments, various stress biases are applied to the devices, which are characterized by a benign characterization suite. Important figures of merit such as the maximum drain current (I_{DMAX}), gate leakage current in the OFF state (I_{GOFF}), drain resistance (R_D) and source resistance (R_S) are monitored before, during and after the stress tests by means of this characterization suite.

Our first observation in GaN HEMTs grown on Si substrate is the relatively high critical voltage for I_{GOFF} degradation as compared to those built on SiC substrate. I_{GOFF} is found to degrade permanently by several orders of magnitude around V_{DG} = 60 V when V_{DS} is set to 0 V (Figure 1). No such I_{GOFF} degradation is observed either in the OFF state, where we stepped V_{DS} up to 60 V while maintaining I_D = 10 mA/mm, or under high power stress conditions where we stepped V_{DS} up to 35 V while maintaining I_D = 400 mA/mm. These results may be attributed to the reduced elastic energy in the GaN buffer due to relaxation by the greater size and number of dislocations that are present on layers grown on a Si substrate [1]. Initial strain in the GaN buffer layer is a factor in the degradation of GaN HEMTs on SiC substrate through the inverse piezoelectric effect.

As the lattice and thermal mismatches between GaN and Si are larger as compared to GaN and SiC, we have investigated I_{DMAX} response of a device at rest to a diagnostic pulse before and after electrical degradation. In effect the diagnostic pulse can be considered an injection of carriers to fill the traps associated with dislocations in the fresh device and possibly additional traps created during the electrical stress. As carriers are trapped, we expect I_{DMAX} to decrease and then increase as these carriers are detrapped over time. Indeed, trapping is observed in both virgin and stressed devices (Figure 2). The amount of current collapse in response to such a carrier injection is proportional to the number of traps. These traps reduce I_{DMAX} under steady state conditions and even more so after the application of a diagnostic pulse. Clearly, electrical stress has increased the number of traps through the inverse piezoelectric effect.

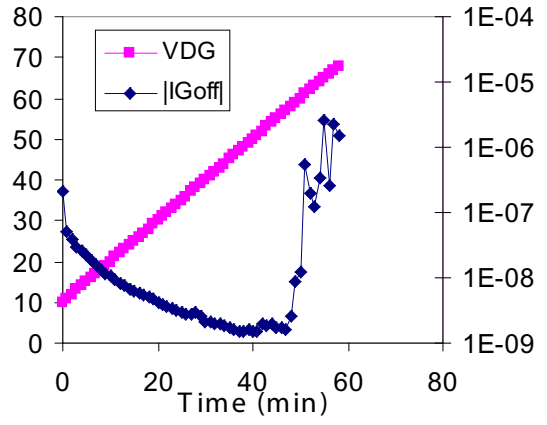


Figure 1: Electrical degradation of gate current in an electrical step-stress with V_{DS} =0 V. Gate voltage is stepped down by 1V starting from -10 V. Gate leakage current degrades by several orders of magnitude starting around V_{DG} = 60 V.

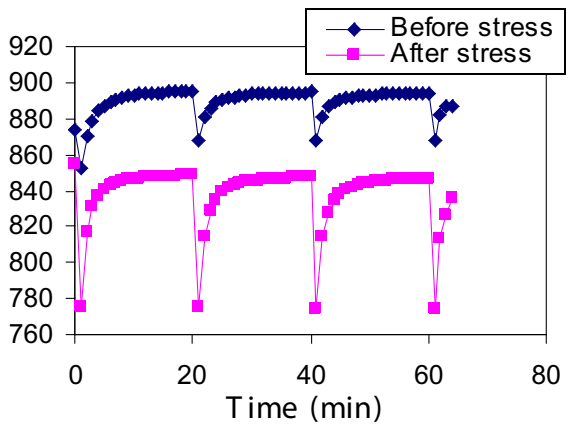


Figure 2: I_{DMAX} response of a device to a -10 V pulse at its gate before and after a V_{DS} = 0 V stress test where gate voltage was stepped down to -80 V. The pulse is applied every 20 minutes when the device is at rest and the current is monitored for more than 60 min. Duration of the pulse is 10 sec.

Reference

[1] J. Joh and J.A. del Alamo, "Mechanisms for electrical degradation of GaN high-electron mobility transistors," *IEEE IEDM Tech. Digest*, 2006.

Degradation Mechanisms of GaN High-electron-mobility Transistors

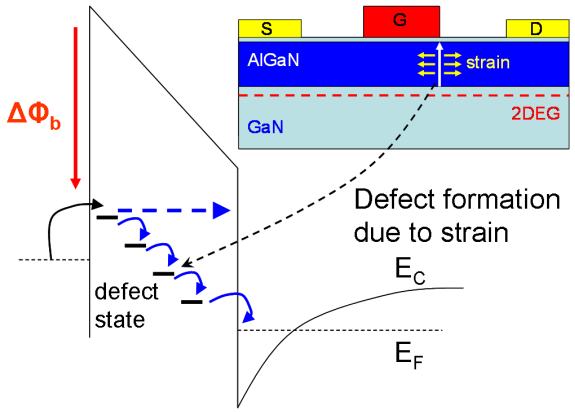
J. Joh, L. Xia, J.A. del Alamo
Sponsorship: ARL

Recently, GaN-based electronic devices have attracted great interest because of their high breakdown electric field (>3x10^6 V/cm). Also, due to the strong piezoelectric effect and spontaneous polarization of both GaN and AlN, a high sheet carrier density (~10^{13} cm^{-2}) can be easily achieved in the AlGaN/GaN heterostructure without any doping. In addition, high electron mobility (~1500 cm^2/V-s) and high saturation velocity (~2x10^7 cm/s) make GaN-based devices, especially GaN high-electron-mobility transistors (HEMT), suitable for high-power and high frequency RF power applications, such as WiMAX or WLAN base stations and radars.

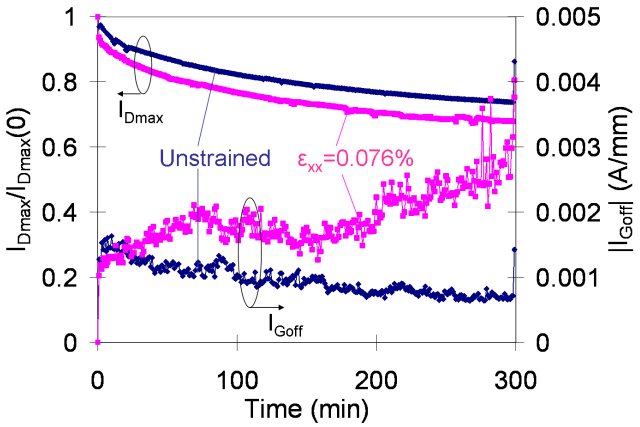
Although promising performance results have been demonstrated, GaN HEMTs still have limited reliability. In RF power applications, GaN HEMTs must operate at high voltage where good reliability is essential. Physical understanding of the fundamental reliability mechanisms of GaN HEMTs is still lacking today. In this research, we perform systematic reliability experiments on GaN HEMTs provided by our industrial collaborators, TriQuint Semiconductor and BAE systems. In our study, GaN HEMTs have been electrically stressed at various bias conditions. During the stress experiments, they were periodically characterized by a benign characterization suite that we have developed.

In previous studies, we have found that one of the main degradation mechanisms in GaN HEMT is crystallographic defect formation in the AlGaN barrier layer due to tensile strain produced by the inverse piezoelectric effect [1]. These introduced defect states decrease the channel carrier density by trapping electrons, which in turn decreases I_D. In our recent research, we have found that a large gate current increase that is widely observed during stress tests is also related to the same mechanism [2]. The defect states in the AlGaN barrier not only trap channel electrons but also provide a path that helps gate current conduction (Figure 1). In order to confirm our hypothesis, we have fabricated a jig through which external mechanical strain can be applied to a chip. In our hypothesis, additional tensile strain should accelerate degradation in I_D and I_G because it adds to the strain produced by the inverse piezoelectric effect. In fact, as Figure 2 shows, degradation in both I_D and I_D is accelerated under external tensile mechanical strain.

Our hypothesis suggests that device design that minimize elastic energy and peak vertical electric field in AlGaN can improve the electrical reliability of GaN HEMTs.



▲ Figure 1: Conceptual I_G degradation mechanism for bias stress. Crystallographic defects produced by the inverse piezoelectric effect provide a leakage path across the AlGaN barrier.



▲ Figure 2: Change in I_{Dmax} and I_{Goff} of OFF-state stress experiments. The devices are stressed at V_{GS}=-7 V and V_{DS}=35 V. The device stressed under tensile mechanical strain shows larger degradation in both I_D and I_G.

References

[1] J. Joh and J.A. del Alamo, "Mechanisms for electrical degradation of GaN high-electron mobility transistors," in *IEEE Int. Electron Devices Meeting Proc.*, 2006, pp. 415-418.

[2] J. Joh, L. Xia, and J.A. del Alamo, "Gate current degradation mechanisms of GaN high electron mobility transistors," in *IEEE Int. Electron Devices Meeting Proc.*, 2007, pp. 385-388.

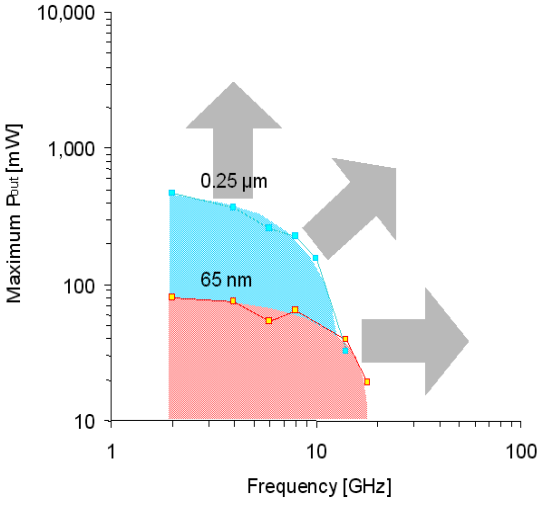
RF Power CMOS for Millimeter-wave Applications

U. Gogineni, J.A. del Alamo, D.R. Greenberg (IBM)
Sponsorship: SRC, IBM

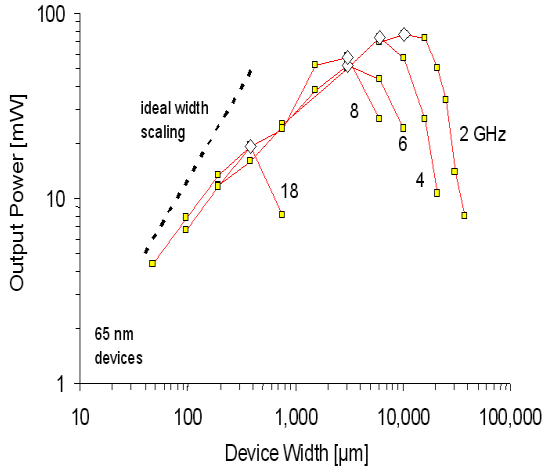
Radio frequency (RF) power amplifiers are core components of almost all wireless systems. Traditionally III-V, SiC, or SiGe devices have been used in power amplifiers because of their ability to deliver high power and operate at high frequencies. Recently there has been an increased interest in using Si CMOS for designing single-chip integrated systems for operation in the millimeter-wave regime. Specific applications in this regime include wireless LAN and collision-avoidance radar. A key concern in using CMOS for these applications is the inability of CMOS to yield high-efficiency power amplifiers with power levels over 10mW in the 60-80 GHz regime.

Previous research in our group at MIT into the RF power performance of 65-nm and 90-nm Si CMOS devices [1-2] has shown that it is not possible for currently available Si CMOS to operate significantly beyond 20 GHz (Figure 1). The effective cut-off frequency for power (frequency at which the output power drops below 10 mW) is around 20 GHz for 0.25-um, 90-nm, and 65-nm CMOS. This suggests that further scaling is unlikely to improve the situation despite improvements in f_T and f_{max}. The reason for this saturation in the effective power cut-off frequency is that the optimum device width that delivers the maximum power at any frequency scales down as the frequency goes up (Figure 2). This effect suggests that the bottleneck for power is the device layout, especially the back-end wiring.

In this research, we are investigating options for device optimization with the goal of pushing the power operation of Si CMOS into the millimeter-wave regime. Small-signal equivalent circuits are extracted from S-parameter measurements on devices with different widths to identify the main power gain detractors. A parasitic-aware layout approach is then employed to design new test structures with minimized parasitics, thus resulting in an improvement in the effective power cut-off frequency for a given technology. Some of the design ideas being explored include (a) alternate ways of connecting elemental devices in parallel, (b) use of multiple levels and thicker levels of metal to reduce interconnect resistance and (c) design of on-chip bias and matching circuits. These designs are being implemented on IBM's 65-nm and 45-nm CMOS technologies.



▲ Figure 1: Maximum power (at peak PAE) vs. frequency of operation obtained in nominal 0.25-um devices (V_{dd}=2.5 V) and 65-nm devices (V_{dd} =1 V) fabricated in a 65-nm process [1].



▲ Figure 2: Maximum power (at peak PAE) vs. device width for different frequencies for 65-nm devices (V_{dd} =1 V) [1].

References

[1] J. Scholvin, D.R. Greenberg, and J.A. del Alamo, "Fundamental power and frequency limits of deeply-scaled CMOS for RF power applications," in *Proc. International Electron Device Meeting 2006*, **pp. 217-220.**

[2] J. Scholvin, D.R. Greenberg, and J.A. del Alamo, "Performance and limitations of 65-nm CMOS for integrated RF power applications," in *Proc. International Electron Device Meeting 2005*, pp. 369-372.

Small-signal Equivalent Circuit Modeling for Si RF Power LDMOSFETs on SOI

Y. Ikura, J.A. del Alamo

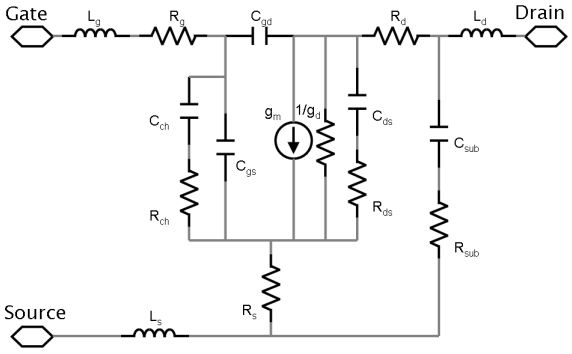
Sponsorship: Fuji Electric Device Technology

Small-signal equivalent circuits are used to model a transistor's high-frequency performance and to design RF power amplifier circuits. Historically the equivalent circuit of Si LDMOSFETs is borrowed from that of compound semiconductor MESFETs. However, the circuit components are not the same in Si LDMOSFETs, especially in the case of those on SOI. The purpose of our work is to develop an equivalent circuit based on the physical understanding of Si LDMOSFETs on SOI and to identify a suitable small-signal parameter extraction procedure.

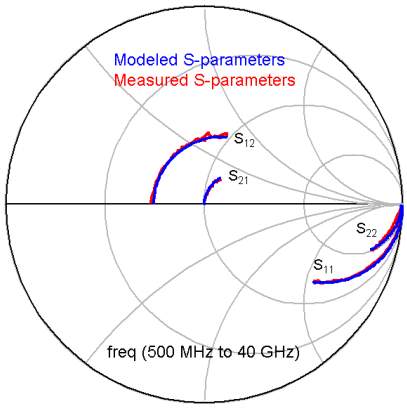
In our model, we employ a substrate network and a channel network that is distributed (see Figure 1). The substrate network (C_{sub}, R_{sub}) models the inversion layer that appears at the interface between the Si substrate and the buried oxide and is affected by the gate, drain, and substrate bias, especially in the case of a high resistivity SOI substrate [1]. The channel network (C_{ch}, R_{ch}) models the inversion layer that appears underneath the gate oxide and constitutes a capacitive coupling with the gate.

The parameters are extracted using an optimizer that minimizes the least-squares error function between the measured S-parameters and the modeled ones. If there are too many parameters, the extraction becomes time-consuming and the extracted values are not necessarily consistent with the physical characteristics. We developed a novel parameter extraction procedure that consists of two steps. In each step, there are fewer parameters and they are extracted more accurately than in the case of a single step extraction method. First, the gate-bias independent parameters are extracted from S-parameters measured under zero gate bias (V_{gs}=0 V, V_{ds}=5 V). In the second step, the remaining parameters are extracted from the S-parameters measured under a gate bias that turns on the transistor and a drain bias that is the same as in the first step (V_{ds}=5 V).

Using our model and procedure, we observed excellent fit between the modeled S-parameters and the measured ones from 0.5 to 40 GHz (Figure 2). The cut-off frequency (f_T) and the maximum frequency of oscillation (f_{max}) are determined as the frequency at which the current-gain $|H_{21}|^2$ and the maximum available gain (MAG) become 0 dB, respectively. We also observed an excellent match between the modeled data (f_T =16.5 GHz, f_{max} =30.5 GHz) and the measured data (f_T =16 GHz, f_{max} =30.5 GHz).



▲ Figure 1: Small-signal equivalent circuit of LDMOSFET on SOI. A distributed substrate network and a distributed channel network are employed.



▲ Figure 2: Modeled S-parameters (blue lines) and measured ones (red lines) of LDMOSFET on SOI.

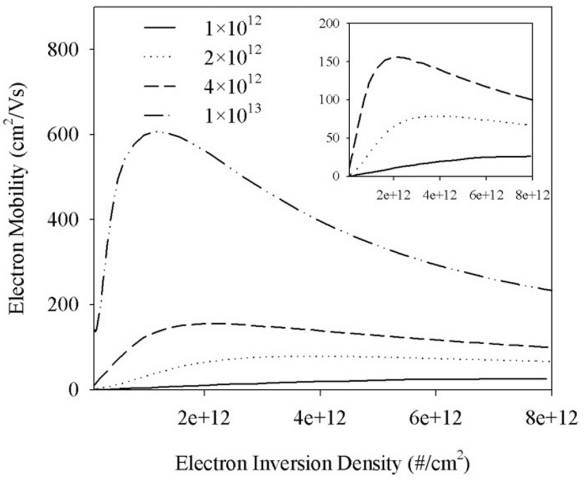
Reference

[1] J. Scholvin, J.G. Fiorenza, and J.A. del Alamo, "Impact of substrate-surface potential on the performance of RF power LDMOSFETs on high-resistivity SOI," *IEEE Transactions on Electron Devices*, vol. 53, no. 7, pp. 1705-1711, July 2006.

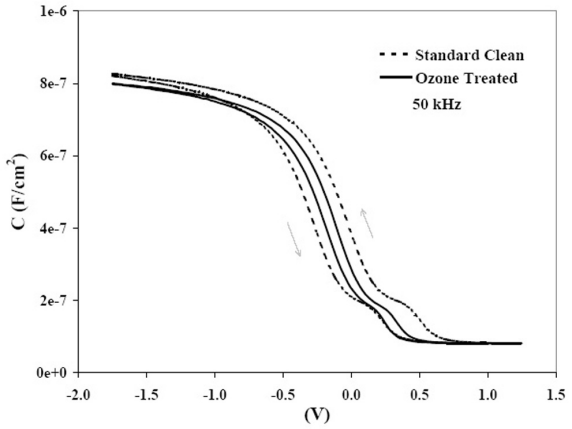
ALD Gate Dielectrics for High-mobility Materials

J. Hennessy, A. Ritenour, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

Maintaining historical performance trends for CMOS devices requires semiconductors with high carrier mobility. Germanium offers significant enhancements in bulk electron and hole mobility relative to silicon; however, past work on surface-channel Ge n-MOSFETs has shown poor performance. In this work, high-k gate dielectrics were deposited on germanium using atomic layer deposition (ALD) in order to explore methods for improving the electrical quality of the gate interface. Figure 1 shows the extracted electron mobility of phosphorous-implanted Ge n-FETs fabricated with an Al_2O_3/AlN gate stack [1]. It is seen that n-FETs that received the highest dose implant exhibit buried channel behavior and show a large increase in peak mobility. This demonstrates that the gate/channel interface is the primary contributor to degraded Ge n-FET performance. Figure 2 illustrates an example of the ongoing effort towards improving the electrical characteristics of the Ge/high-k interface. MOS capacitors were fabricated with an Al_2O_3/AlN gate deposited by ALD. Substrates treated only with a wet clean show capacitance-voltage characteristics with minimum mid-gap density of interface states (D_{it}) of ~$2x10^{12}$ #/cm². Substrates that received the same wet clean plus in-situ exposure to ozone immediately prior to gate deposition show a substantial reduction in both Dit (~$4x10^{11}$ #/cm²) and hysteresis.



▲ Figure 1: Effective carrier mobility for Ge and n-FETs that received 1×10^{12}, 2×10^{12}, 4×10^{12}, and 1×10^{13} cm^{-2} phosphorous channel implants. Inset shows electron mobilities for the devices that showed no buried-channel operation [1].



▲ Figure 2: MOS capacitors on p-Ge with an Al_2O_3/AlN dielectric. Both samples received a wet clean in HCl → NH_4OH/H_2O_2 → HCl prior to deposition. The ozone treated sample received a 30-min exposure to O_3 (20% wt in O_2) immediately prior to dielectric deposition.

Reference

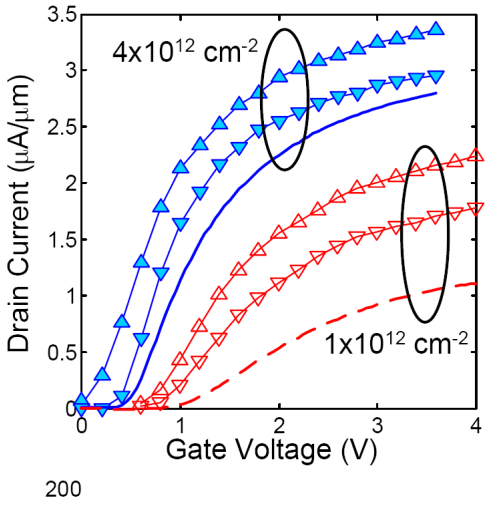
[1] A. Ritenour, J. Hennessy, and D.A. Antoniadis, "Investigation of carrier transport in germanium MOSFETs with WN/Al_2O_3/AlN gate stack," *IEEE Electron Device Letters*, vol. 28, no. 8, pp. 746-749, Aug. 2007.

Pulsed I-V and Q-V Characterization of Germanium MOSFETs

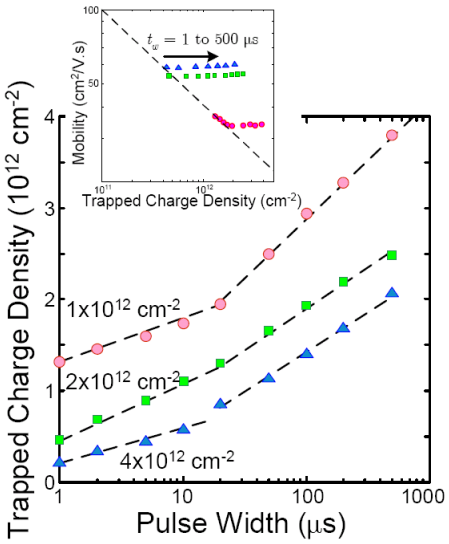
A. Khakifirooz, A. Ritenour, J. Hennessy, D.A. Antoniadis

Sponsorship: SRC/FCRP MSD

Despite significantly higher electron and hole mobility in bulk germanium compared to silicon and the early reports of very high carrier mobility in Ge-channel NMOS and PMOS transistors [1], recent efforts to demonstrate high-performance germanium MOSFETs have not been successful. Carrier mobility is generally much lower than what is expected in germanium inversion layers. While hole mobility improvement as high as 2.5× compared to the silicon universal curve has been observed with an epitaxially grown silicon passivation layer [2], reported values of electron mobility are still disappointing. This low mobility is believed to be in part due to the presence of high concentration of interface traps near the conduction band [3]. In this work, pulsed *I-V* and *Q-V* measurements are used to characterize carrier transport and charge trapping in germanium-channel NMOS transistors. Charge trapping is shown to be significant in these transistors and the "intrinsic" electron mobility extracted from pulsed *I-V* measurements can be much higher than what extracted from DC measurements, as Figure 1 shows. As Figure 2 shows, phosphorus passivation of the germanium-dielectric interface reduces the density of fast traps near the Ge-dielectric interface. Analysis of the relationship between electron mobility and trapped charge density reveals that mobility depends only on the density of fast traps.



▲ Figure 1: Comparison of I_d-V_g characteristics from DC (lines) and pulsed (symbols) measurements for devices that received different doses of phosphorus implantation prior to high-k deposition. Measurements were performed on ring transistors with W/L = 180/5μm. Pulsed measurements were done by applying a train of pulses with increasing pulse height, t_r = t_f =100 ns, and t_w= 100 μs. The △ represents the measurements at the beginning of the pulse, while ▽ indicates the values after t_w.



▲ Figure 2: Pulse-width dependence of the density of trapped charges for Ge NMOSFETs with different doses of phosphorous passivation implant and at a constant inversion charge density of about 1.7 ×$10^{13}$$cm^{-2}$ at the beginning of the pulse (corresponding to a pulse amplitude of about 3 V). The inset shows the relation between mobility and density of trapped charges and demonstrates that electron mobility depends only on the density of fast traps.

References

[1] J.J. Rosenberg and S.C. Martin, "Self-aligned germanium MOSFET's using a nitrided native oxide gate insulator," *IEEE Electron Device Letters*, vol. 9, no. 12, pp. 639-641, 1988.

[2] P. Zimmerman, G. Nicholas, B. De Jaeger, B. Kaczer, A. Stesmans, L.-A. Ragnarsson, D.P. Brunco, F.E. Leys, M. Caymax, G. Winderickx, K. Opsomer, M. Meuris, and M.M. Heyns, "High-performance Ge pMOS devices using a Si-compatible process flow," in *IEDM Technical Digest*, 2006, pp. 655-658.

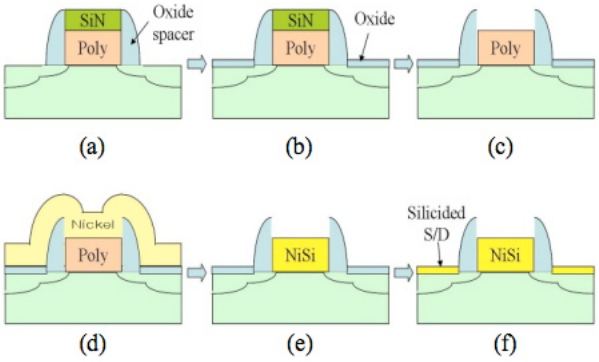
[3] K. Martens, B. De Jaeger, R. Bonzom, J. Van Steenbergen, M. Meuris, G. Groeseneken, and H. Maes, "New interface state density extraction method applicable to peaked and high-density distributions for Ge MOSFET development," *IEEE Electron Device Letters*, vol. 27, no. 5, pp. 405-407, 2006.

Low-temperature NiSi-gate, -source/drain Si/SiGe Heterostructure MOSFETs

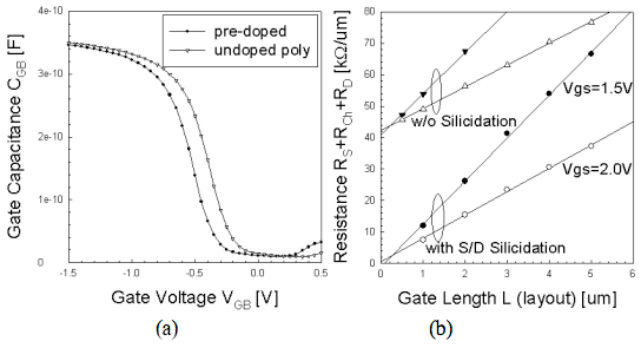
J. Lee, J.L. Hoyt, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

The development of integrated circuits and devices faces many technological challenges, which are related to material and process integration [1]. This work presents a nickel silicidation as a low-temperature process for the fabrication of heterostructure MOSFETs. Low-temperature processing is necessary for heterostructure devices with high germanium contents (>50%) in order to maintain the source/drain and channel structure.

Nickel silicide (NiSi) has been widely studied in recent years for use as a contact material, and now it has been widely used as a gate material. NiSi gates offer higher gate capacitance, lower sheet resistance and superior scalability compared to conventional polysilicon gates [2,3]. Low source/drain (S/D) series resistance is also important for nano-scale devices due to their higher current densities. The nickel silicidation process can be done with simple heat treatment at temperatures lower than 450°C, which is necessary in order to preserve the shallow junctions and hetero channel structure of high-performance, short-channel devices. This work shows the integration of a nickel fully silicided (FUSI) gate and silicided source/drain regions with a Si/SiGe heterostructure MOSFET device (see Figure 1). Figure 2 shows the modulation of gate work function (a) and the reduction of S/D resistance (b) by the nickel silicidation process.



▲ Figure 1: CMP-free FUSI gate fabrication: (a) gate stack and oxide spacer; (b) reoxidation of S/D; (c) SiN removal; (d)nickel deposition; (e) anneal and Ni removal; (f) S/D silicidation.



▲ Figure 2: (a) Flat-band voltage shift due to modulation of the gate work function, which is done by pre-doping the poly gate. (b) NiSi source/drain silicidation effect on Si/SiGe heterostructure MOSFETs.

References

[1] W.P. Maszara, "Fully silicided metal gates for high-performance CMOS technology: A review," *Journal of the Electrochemical Society*, vol. 152, no. 7, pp. G550–G555, 2005.

[2] M. Qin, V.M.C. Poon, and C.H. Ho, "Investigation of polycrystalline nickel silicide films as a gate material," *Journalof the Electrochemical Society*, vol. 148, no. 5, pp. 271–274, 2001.

[3] W.P. Maszara, Z. Krivokapic, P. King, J.-S. Goo, and M.-R. Lin, "Transistors with dual work function metal gates by single full silicidation (FUSI) of polysilicon gates," in *IEDM Technical Digest*, Dec. 2002, pp. 367–370.

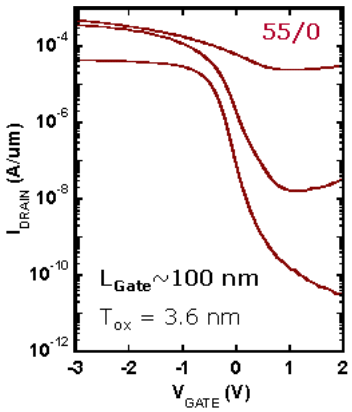
Fabrication of Strained-SiGe and Strained-Ge Short Channel p-MOSFETs on Insulator

L. Gomez, P. Hashemi, J.L. Hoyt

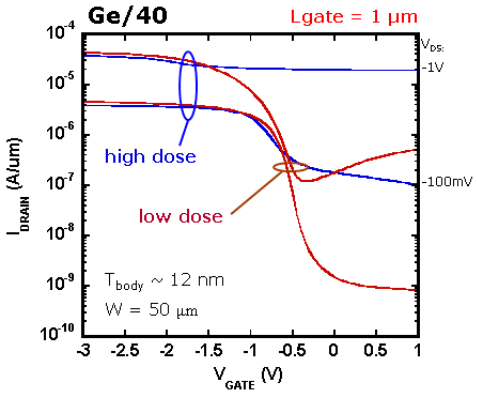
Sponsorship: NSF Graduate Student Research Fellowship, SRC/FCRP MSD

Scaling of device dimensions can no longer provide the necessary current drive enhancements to continue historic performance gains. The use of strain and novel channel materials provides enhanced transport characteristics to increase device performance. Thin-body on-insulator substrate configurations can also be utilized to offer improved electrostatic control in deeply scaled MOSFETs. In this work these two performance enhancers are combined onto a single substrate to realize the performance benefits of strained-Si/strained-Ge heterostructures on insulator (Ge HOI). Hole mobility enhancements as high as 10x have been observed for an 8-nm-thick buried Ge channel strained to $Si_{0.5}Ge_{0.5}$ at an inversion charge density of $7x10^{12}$ [1]. The goal of this work is to determine if significant performance enhancement can be observed at shorter gate lengths. A short-channel process has been developed to characterize the performance of p-MOSFETs fabricated in this material.

Short channel process development was conducted on substrates with strained $Si_{0.45}Ge_{0.55}$ channels pseudomorphic to unstrained SOI. Devices were fabricated with gate lengths down to ~100 nm. Figure 1 presents the ID-VG characteristics for a 100-nm p-MOSFET with reasonable electrostatic behavior. Further work was conducted to investigate the effect of source/drain doping and damage on off-state leakage in strained-Ge channel devices. Figure 2 presents ID-VG characteristics for 1-um-long devices fabricated on Ge/40 HOI. The use of a low-mass (Boron) and low-dose implant condition is observed to provide a significant reduction in off-state leakage. Work is in progress to utilize the developed short channel process to fabricate strained-Ge p-MOSFETs that incorporate the modified implant condition to reduce the off-state leakage.



▲ Figure 1: Drain current vs. gate bias for 100-nm 55/0 strained SiGe channel device. The strained-SiGe channel thickness is ~7 nm. The V_{DS} was biased at -100mV, -1V, and -2V.



▲ Figure 2: Drain current vs. gate bias for 1-um-long p-MOSFET fabricated on Ge/40 HOI substrates with two different implant conditions. The high-dose implant conditions are BF_2, 4e15 cm^{-2}, at 17 keV. The low-dose implant conditions are Boron, 2e14 cm^{-2}, at 6keV.

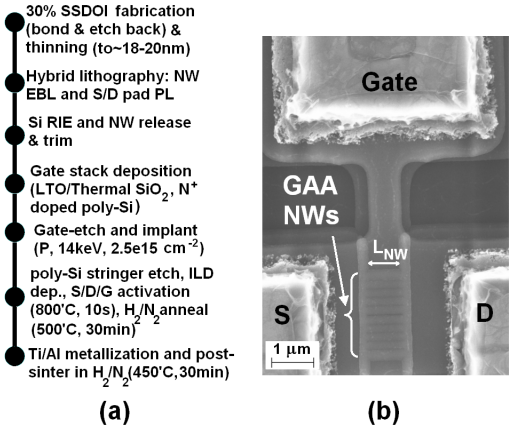
Reference

[1] C. Ní Chléirigh, "Strained-SiGe channel p-MOSFETs: Impact of heterostructure design and process technology," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.

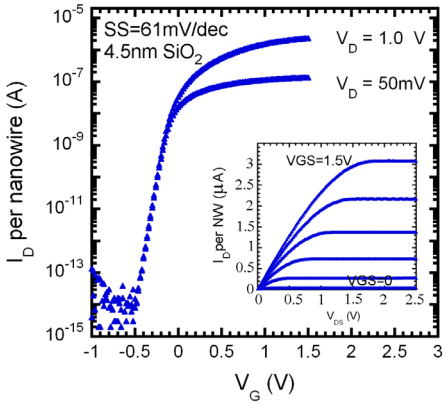
Fabrication and Characterization of Uniaxially Strained-Si Gate-all-around n-MOSFETs

P. Hashemi, L. Gomez, M. Canonico (Freescale Semiconductor), J.L. Hoyt
Sponsorship: SRC/FCRP MSD

Gate-all-around nanowire (NW) MOSFETs are of great interest for future CMOS technology generations due to the enhanced scalability compared to conventional planar MOSFETs [1]. Strain engineering is mandatory to improve the mobility and drive current of these devices. Among possible strain configurations, uniaxial tension in the [110] direction is most favorable to enhance NMOS performance due to reduction of the electron effective mass [2]. In this work, fabrication of uniaxially strained-Si NW n-MOSFETs with a gate-all-around (GAA) architecture is reported. Figure 1(a) shows the MOSFET fabrication process flow. The starting material was 18-20-nm-thick Strained-Silicon-Directly-on-Insulator (SSDOI) substrate (with high biaxial stress level of 2.2GPa), fabricated using a bond and etch-back technique. Unstrained, commercial SOI was also thinned to the same thickness as the SSDOI films, by successive dry oxidation and oxide removal. The device mesa isolation was performed using hybrid lithography, after a photolithography (PL) step to create e-beam alignment marks. For this purpose, a XR-1541™ NW hard mask layer was created using e-beam lithography at a dose of 1.2mC/cm² and energy of 30keV, followed by development in TMAH. The S/D regions were then patterned using photolithography and the Si was etched in an RIE system. The hard-mask removal and nanowire suspension were performed using dilute HF solution. This nano-scale patterning is shown to transform the biaxial stress to uniaxial tension (~2.2GPa), as confirmed by UV-micro Raman spectroscopy. After RCA cleaning, which further trims the NWs, a poly-Si (~80-nm)/SiO_2 gate stack was formed all around the wires. Two sets of gate oxides were created: 14-nm deposited LTO and 4.5-nm thermally grown oxide. The gate was then patterned using SEM-corrected photolithography with alignment error of less than 50 nm. Next, S/D phosphorous ion implantation was performed at 14 keV with a dose of 2.5e15 cm^{-2}. The poly-Si stringers on S/D regions were removed by photolithography followed by an RIE step. After interlayer dielectric deposition, the implant was activated at 800˚C for 10sec. A hydrogen anneal at 500˚C significantly improves the subthreshold characteristics. Contact vias were opened, followed by Ti/Al contact metallization, metal patterning, and H_2/N_2 annealing. Figure 1(b) shows a SEM micrograph of 0.8-µm-long GAA strained-Si NW n-MOSFET with 10 parallel NWs (each ~20nm wide). Figure 2 shows the transfer characteristics of a -µm-long strained-Si NW n-MOSFET (W_{NW}~15nm and t_{NW}~13nm) with 4.5-nm thermal oxide dielectric. The inset shows the output characteristics of this MOSFET. The device shows excellent long channel characteristics with ideal subthreshold swing of 61mV/dec and high on-to-off ratio of ~10^8. The drain current is scaled per NW. Further analysis is in progress to study the effect of the uniaxial strain on the performance of GAA NW n-MOSFETs.



▲ Figure 1: (a) Fabrication process and (b) SEM image of GAA NW n-MOSFET (W_{NW}~20nm, L_{NW}=0.8µm).



▲ Figure 2: Transfer and output (inset) characteristics of 1-um-long GAA strained-Si NW n-MOS (W_{NW}~15nm and t_{NW}~13nm) with 4.5-nm thermal oxide dielectric.

References

[1] Suk *et al.*, "High-performance 5-nm-radius twin silicon nanowire MOSFET (TSNWFET): Fabrication on bulk Si Wafer, characteristics, and reliability," in *IEDM Technical Digest*, 2005, pp. 717–720.

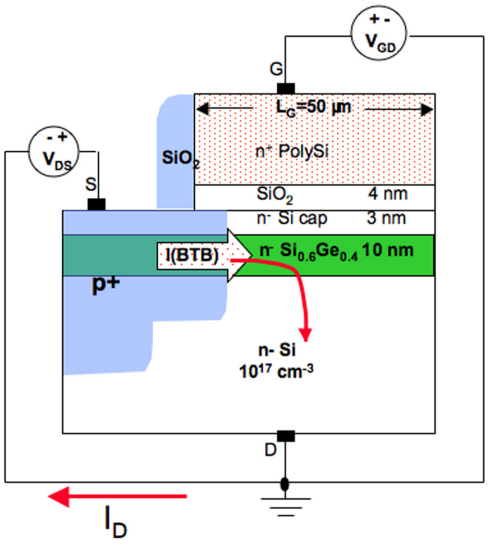
[2] A. Khakifirooz, "Transport enhancement techniques for nanoscale MOSFETs" Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.

Measurement and Analysis of Enhanced Gate-controlled Band-to-band Tunneling in Highly Strained Silicon-Germanium Diodes

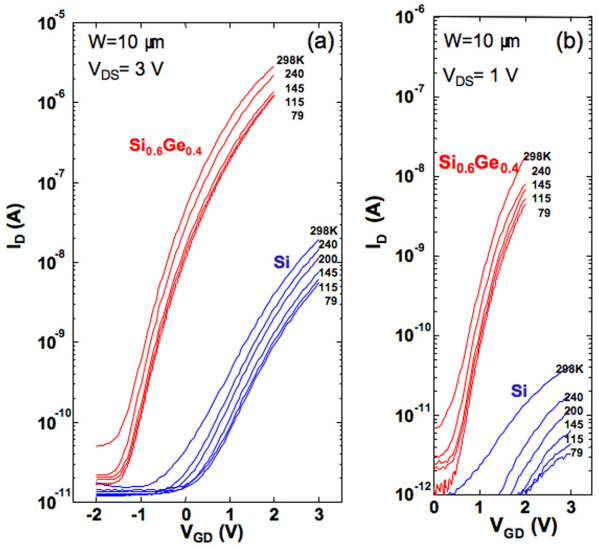
O.M. Nayfeh, C. Ni Cheirigh, J.L. Hoyt, D.A. Antoniadis

Sponsorship: SRC/FCRP MSD, Singapore-MIT Alliance, Intel Fellowship

Strained silicon-germanium ($Si_{0.6}Ge_{0.4}$) gated diodes have been fabricated and analyzed. The devices exhibit significantly enhanced gate-controlled tunneling current over that of co-processed silicon control devices. The current characteristics are insensitive to measurement temperature in the 80- to 300-K range. The independently extracted valence band offset at the strained $Si_{0.6}Ge_{0.4}$/Si interface is 0.4 eV, yielding a $Si_{0.6}Ge_{0.4}$ bandgap of 0.7 eV, much reduced compared to that of Si. The results are consistent with device operation based on quantum mechanical band-to-band tunneling rather than on thermal generation. Moreover, simulation of the strained $Si_{0.6}Ge_{0.4}$ device using a quantum mechanical band-to-band tunneling model is in good agreement with the measurements. The results are important for the realization of tunneling field-effect transistors with large current drive and steep sub-threshold swing.



▲ Figure 1: Schematic cross-section of the gated strained $Si_{0.6}Ge_{0.4}$ diode and measurement biasing.



▲ Figure 2: Measured characteristics for p+ $Si_{0.6}Ge_{0.4}$/n Si and p+ Si/n Si gated-diode structures, for various temperatures from 300 down to 80K, at reverse diode biases of (a) 3V, and (b) 1V. The doping profiles are similar for both the $Si_{0.6}Ge_{0.4}$ and Si devices. The significant increase in tunneling rate, due to the smaller bandgap, is evident in the measurements of the $Si_{0.6}Ge_{0.4}$ gated diodes.

Reference

[1] O.M. Nayfeh, C. Ni Chleirigh, J.L. Hoyt, and D.A. Antoniadis, "Measurement of enhanced gate-controlled band-to-band tunneling in highly strained silicon-germanium diodes," *IEEE Electron Device Letters*, vol. 29, no.5, pp. 468-470, 2008.

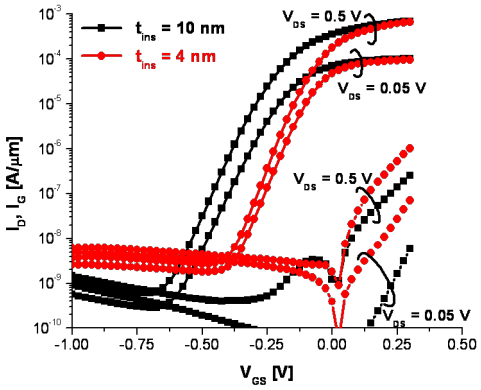
Logic Potential of 40-nm InAs HFETs

D.-H. Kim, J.A. del Alamo

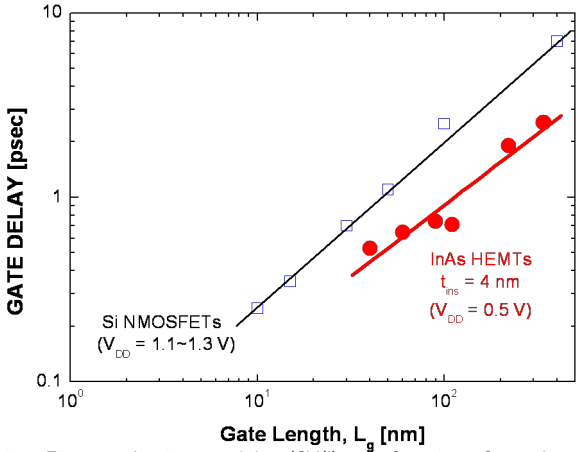
Sponsorship: Intel Corporation, SRC/FCRP MSD

Scaling of Si CMOS has been the cornerstone of the microelectronics revolution during the past 30 years. While a matter of considerable debate, CMOS scaling now seems to be fast approaching the end of the roadmap. It is therefore of great importance to find a new technology that would allow the extension of Moore's law beyond the point where Si can reach. Indium Arsenide (InAs), with a room temperature bulk electron mobility in excess of 20,000 cm^2/V-s, is a promising candidate for channel material in a future III-V CMOS technology [1]. In our work, we are investigating the logic potential of InAs heterostructure-FETs (HFETs) as a model device for a future InAs MOSFET with a high-k gate dielectric [2].

We have fabricated pseudomorphic InAs HFETs on InP substrate with two different values of InAlAs insulator thickness (t_{ins} = 10 nm and 4 nm). Our shortest device has a gate length of 40 nm. We have evaluated the logic performance of these devices. Figure 1 shows sub-threshold and gate leakage (I_G) characteristics of representative 40-nm InAs HFETs with two different values of t_{ins}, at V_{DS} of 0.05 and 0.5 V. As t_{ins} decreases, V_T shifts positive and sub-threshold slope improves considerably. Excellent S = 70 mV/dec and DIBL = 80 mV/V are obtained for the t_{ins} = 4 nm device. This sharp sub-threshold characteristics yield an I_{ON}/I_{OFF} ratio in excess of 10^4 at V_{DD} = 0.5 V. Figure 2 shows the logic gate delay (CV/I) as a function of gate length of InAs HFETs with t_{ins} = 4 nm. For comparison, values of state-of-the-art Si CMOS are also shown. Our InAs HFETs exhibit significantly better logic delay than Si-CMOS, in spite of the lower voltage of operation. Also, the logic delay scales gracefully down to a 40-nm gate length regime, suggesting further scaling potential. This outstanding performance of our InAs HFETs stems from the excellent transport properties of the InAs channel. Our research reveals that InAs is a material with great potential for applications beyond Si CMOS logic.



▲ Figure 1: Subthreshold and gate leakage characteristics of 40-nm InAs HFETs with two different values of t_{ins} at V_{DS} = 0.05 and 0.5 V. The t_{ins} = 4 nm devices exhibit excellent subthreshold behavior.



▲ Figure 2: Logic gate delay (CV/I) as a function of gate length for InAs HFETs with t_{ins} = 4 nm, as well as Si CMOS. Our InAs HFETs exhibit much lower values of CV/I than those of Si CMOS even at the lower supply voltage of 0.5 V.

References

[1] D.-H. Kim and J. del Alamo, "Scaling Behavior of $In_{0.7}Ga_{0.3}As$ HEMTs for Logic," *International Electron Devices Meeting Technical Digest*, Dec. 2006, pp. 837-840.
[2] D.-H. Kim and J. del Alamo, "Logic performance of 40 nm InAs HEMTs," *Electron Devices Meeting Technical Digest*, Dec. 2007, pp. 629-632.

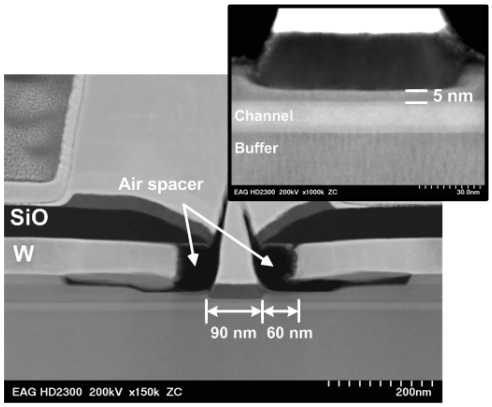
90 nm Self-aligned InGaAs HEMT for Logic Applications

N. Waldron, J.A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel

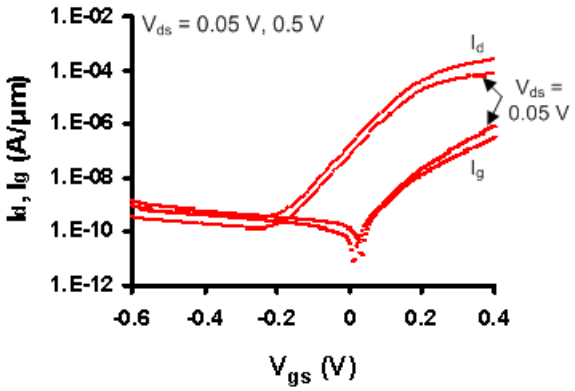
As conventional CMOS scaling approaches the end of the roadmap, identifying a new logic device technology is becoming a matter of great urgency. With a room temperature electron mobility easily in excess of 10,000 cm^2/V.s, InGaAs represents a very attractive proposition as a channel material. Previously it has been shown that InGaAs-based high-electron-mobility transistors (HEMT) show great promise for logic applications [1]. However, the conventional design of HEMTs is not well suited for VLSI applications. The gate is not self-aligned and is typically separated from the source/drain by a distance of around 1 µm. This results in a large device footprint and associated parasitics. Also the exposed surface area and alloyed contacts represent a reliability concern.

To address these issues we have developed a self-aligned process that reduces the gate to source/drain distance to less than 60 nm [2]. This distance is about a 15x improvement over the conventional design. We start by depositing a layer of W to form the non alloyed source drain regions which is followed by a SiO deposition. The gate is formed by a two step electron-beam lithographic process. In the first step, the gate foot is defined by etching the SiO and W. At this point the W is co-incident with the edge of the SiO. The W is then pulled back from the edge of the SiO by means of a selective etch thus forming an "air-spacer". The second litho is then aligned back to this etched foot, the recess etch is carried out and gate metal is deposited and lifted off. In this process we achieve device enhancement mode operation by thinning the insulator by means of a dry etch. Figure 1 shows a TEM of a completed device with a gate length of 90 nm. The self-aligned devices exhibit excellent logic figures of merit. The 90 nm devices in which the barrier was thinned to 5 nm have a V_T of 60 mV, maximum transconductance of 1.3 mS/um, subthreshold (SS) swing of 70 mV/dec and drain-induced barrier lowering (DIBL) of 55 mV/V with an I_{on}/I_{off} ratio of 1.8 x 10^3 (Figure 2).

The self-aligned architecture developed in this work should allow us to map out the ultimate logic potential of III-V FETs.



▲ Figure 1: TEM of a completed 90-nm gate length self-aligned device. The gate is separated from the W source/drain ohmics by an "air-spacer" of 60 nm. This is about a 15x improvement over conventional designs. The barrier thickness has been thinned by means of a dry etch to 5 nm (see inset). This vertical scaling results in enhancement mode devices with excellent electrostatic integrity.



▲ Figure 2: Subthreshold characteristics of a 90-nm self-aligned device where the barrier thickness has been scaled to 5 nm. At a V_{ds} of 0.5 V, the device has a threshold voltage of 60 mV, SS of 70 mV/V, DIBL of 55 mV/V and a maximum transconductance of 1.3 mS/µm.

References

[1] D-H. Kim and J.A. del Alamo "Scaling behavior of $In_{0.7}Ga_{0.3}As$ HEMTs for logic," *International Electron Devices Meeting Technical Digest*, Dec 2006

[2] N. Waldron, D-H. Kim and J.A. del Alamo, "90 nm self-aligned, enhancement mode InGaAs HEMT for logic applications," *International Electron Devices Meeting Technical Digest*, Dec. 2007, p. 636.

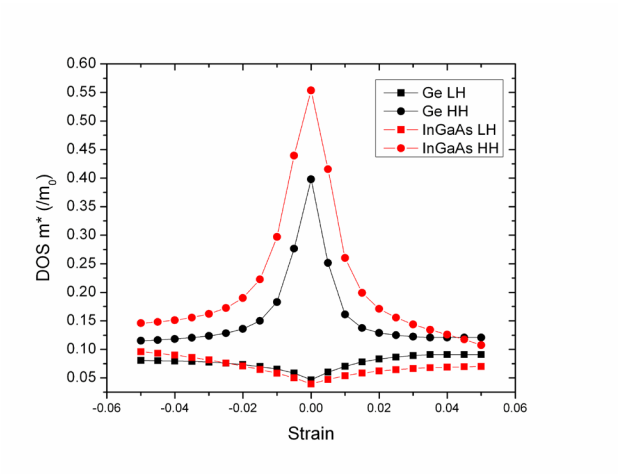
P-channel InGaAs HEMTs for Beyond-Si Complementary Logic

L. Xia, J.A. del Alamo
Sponsorship: SRC/FCRP MSD

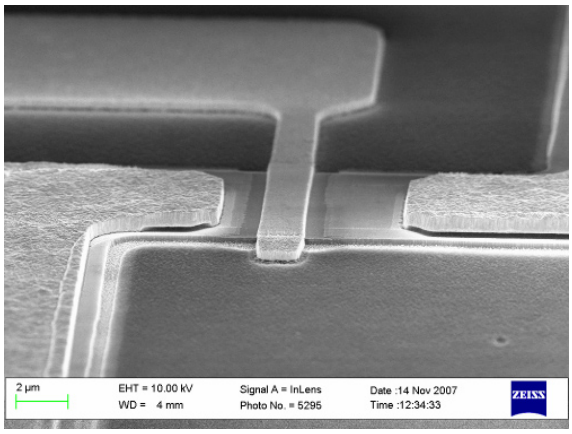
As the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches the end of the roadmap, its performance improvement brought by size-scaling will reach a limit. Among beyond-Si logic alternatives, InGaAs shows superior potential for n-channel FET-type devices. [1] However, to match the performance of n-channel InGaAs FETs, great efforts are needed to improve current p-channel InGaAs devices. The goal of our study is to enhance the transport properties in p-channel InGaAs FETs, to ultimately implement complementary logic based on InGaAs as a successor to modern Si technology.

In order to boost the speed of p-channel InGaAs FETs, we are studying the possibility of enhancing the hole mobility through the application of mechanical strain to the channel. Strain-induced enhancements have been used in Si and Ge devices for some time. Compared with their unstrained counterparts, strained Ge and Si showed 6× and 2× higher hole motilities, respectively [2, 3]. Theoretical studies have shown that in Si, Ge and compound semiconductors such as InGaAs, strain can split the heavy-hole and light-hole valence bands, which are degenerate at the Γ-point in the unstrained semiconductor. This can lead to preferential occupation of holes into the lighter band, so that the conductivity effective mass of the holes decreases. What is more, strain can also reduce the density-of-states (DOS) effective mass of holes. In Figure 1, the change of DOS effective mass due to strain is calculated by the 8x8 k.p method for both Ge and InGaAs. It can be seen that the effect in InGaAs follows a trend similar to that of Ge. It is therefore reasonable to expect a sizable improvement in the hole mobility in InGaAs through the application of mechanical strain.

To experimentally verify the potential enhancement, we are exploring two threads. Along the first thread, a chip-bending apparatus has been fabricated. This apparatus has four ridges whose vertical and horizontal positions are controlled by micrometers. By manipulating the micrometers, we can use the ridges to apply either tensile or compressive uniaxial strain on an InGaAs chip down to the size of 4mm×4mm. At the same time, we can conduct electrical measurements on the strained devices. Our second thread is to fabricate p-channel InGaAs high-electron-mobility transistors. In these devices, spatial separation between dopants and a two-dimensional hole gas results in reduced ionized impurity scattering and high mobility. Figure 2 shows an example of a fabricated device. By combining the two threads, we hope to provide understanding of the speed-enhancing effects of strain in p-channel InGaAs FETs.



▲ Figure 1: The density-of-states effective mass of Ge and InGaAs under different amount of compressive (-) and tensile (+) strain.



▲ Figure 2: An SEM image of a fabricated InGaAs FET.

References

[1] D.-H. Kim and J. A. del Alamo, "Scaling behavior of $In_{0.7}Ga_{0.3}As$ HEMTs for logic applications," *International Electron Devices Meeting Technical Digest*, pp. 837-840, Dec. 2006.

[2] H. Shang, J. O. Chu, X. Wang, P. M. Mooney, K. Lee, J. Ott, K. Rim, K. Chan, K. Guarini, and M. Ieong, "Channel design and mobility enhancement in strained germanium buried channel MOSFETs," *Symposium on VLSI Technology Digest of Technical Papers*, June 2004, pp. 204-205.

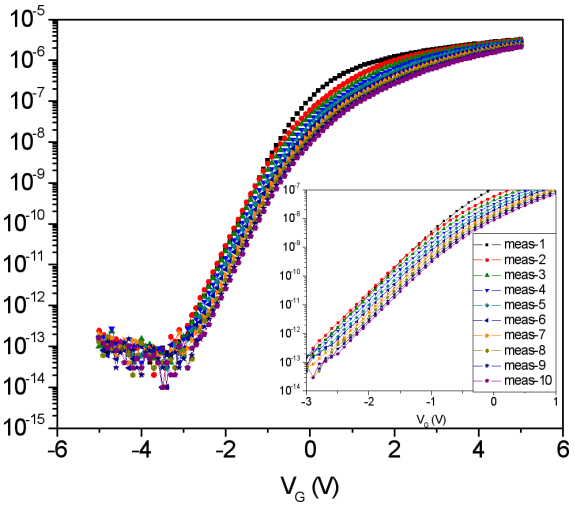
[3] S. Tyagi, *et al.* "An advanced low power, high performance, strained channel 65nm technology," *International Electron Devices Meeting Technical Digest*, Dec. 2005, pp. 1070-1072.

Stability of Metal Oxide-based Field-effect Transistors

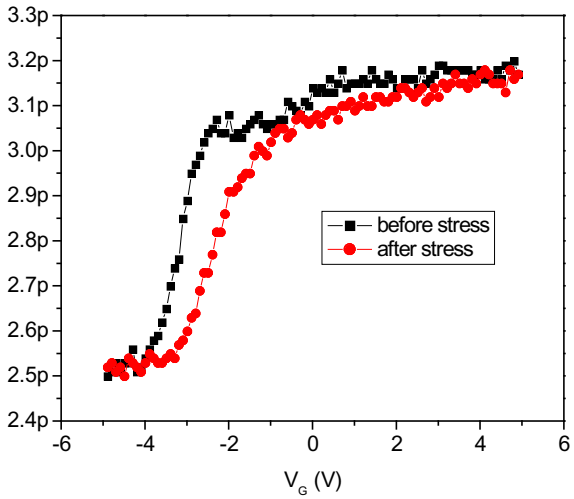
B. Yaglioglu, A. Wang, K. Ryu, H. Tang, C.G. Sodini, A.I. Akinwande, V. Bulović
Sponsorship: Hewlett-Packard, DARPA

Over the last few years, there has been a considerable effort to understand the behavior of metal-oxide-channel field-effect transistors (FETs) in order to produce devices for low-cost, large-area electronic applications [1-3]. Field-effect mobility, sub-threshold slope, and threshold voltage of FETs are the main parameters that need to be characterized to design circuits made of amorphous oxide semiconductors. Just as important as these characteristics is the endurance of FETs over repeated switching cycles, which determines the reliability of the transistors.

In this study we test the stability of FETs that have a polymer dielectric, parylene, and an oxide semiconductor ($ZnO:In_2O_3$). The devices are processed lithographically at low temperatures ($T \leq 100\ ^oC$). Figure 1 shows transfer characteristics that are obtained by repetition of current-voltage (I-V) sweeps under a gate bias between measurements. Preliminary results of I-V tests along with capacitance-voltage (C-V) measurements (see Figure 2) show a positive shift in the threshold voltage. Two possible mechanisms that are originally proposed for similar shifts in amorphous Si FET's are metastable state generation in the semiconductor and charge trapping in the dielectric [4]. Operation of stability experiments at different temperatures and bias gate voltages are conducted to elucidate the instability mechanisms in these hybrid (inorganic/organic) devices. The outcome of these experiments will provide a path for increasing the performance and lifetime of transistors based on oxide semiconductors.



▲ Figure 1: Transfer characteristics of a transistor under a bias stress, V_{GS}= 10V and V_{DS}= 0V, between measurements (stress time = 20s). Data are taken from -5V to 5V with 0.1V steps while V_{DS}= 1V. The sub-threshold regime of curves is enlarged in the inset.



▲ Figure 2: Quasi-static C-V measurements collected from the same device before and after bias stress test.

References

[1] P.F. Carcia, R.S McLean, M.H. Reilly, and G. Nunes, "Transparent ZnO thin film transistors fabricated by rf magnetron sputtering," *Applied Physics Letters*, vol. 82, no. 7, pp. 1117-1119, Feb. 2003.

[2] N.L. Dehuff, E.S. Kettenring, D. Hong, H.Q. Chiang, J.F. Wager, R.L. Hoffman, C.H. Park, and D.A. Keszler, "Transparent thin film transistors with zinc indium oxide channel layer," *Journal of Applied Physics*, vol. 97, no. 6, pp. 064505:1-5, Mar. 2005.

[3] H. Kumomi, K. Nomura, T. Kamiya, and H. Hosono, "Amorphous oxide channel TFTs," *Thin Solid Films*, vol. 516, no. 7, pp.1516-1522, Feb. 2008.

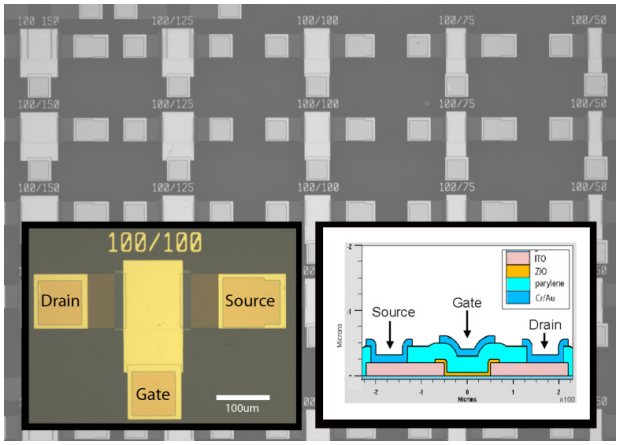
[4] M.J. Powell, C. van Berkel, and J R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," *Applied Physics Letters*, vol. 54, no. 14, pp. 1323-1325, Jan. 1989.

Lithographically Patterned Metal Oxide Transistors for Large-area Electronics

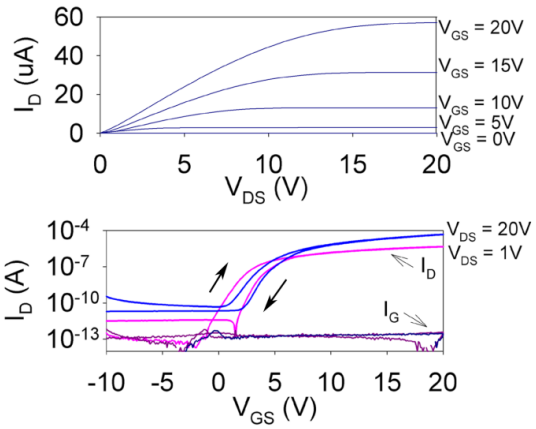
A. Wang, B. Yaglioglu, H. Tang, C.G. Sodini, V. Bulović, A.I. Akinwande
Sponsorship: Hewlett-Packard, DARPA

Recently, sputtered metal-oxide-based field-effect transistors (FETs) have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1-3]. Because the optically transparent semiconducting oxide films can be deposited at near-room temperatures, these materials are compatible with future generations of large-area electronics technologies that require flexible substrates [4]. It is possible to process FETs by shadow-mask patterning, but this method limits the range of feature sizes, accuracy of pattern alignment, and scalability of the process to large substrates. Consequently, our project aims to develop a low-temperature, lithographic process for metal oxide-based FETs that can be integrated into large-area electronic circuits.

We have fabricated top-gate, fully lithographic FETs of varying channel lengths on 100-mm glass wafers with a sputtered ZnO: In_2O_3 channel layer, using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts. All layers were subtractively patterned by a combination of dry- and wet-etch processes. Figure 1 shows a micrograph of several completed FETs. Current-voltage characteristics for a single device (pictured in inset of Figure 1) appear in Figure 2. From the current-voltage and capacitance-voltage curves, device- and circuit parameters such as threshold voltage, subthreshold slope, gate leakage, and channel capacitance can be extracted and also used to monitor the reproducibility of our process. These measurements are used as a guide to determine processing conditions for the fabrication of oxide-based field-effect transistors and circuits.



▲ Figure 1: Micrograph of fabricated array of single devices with varying channel lengths. The left inset gives a larger view of a single field effect transistor (W/L = 100µm / 100µm). The right inset shows a schematic cross-section of the device.



▲ Figure 2: Electrical characteristics of lithographically patterned FET (W/L = 100µm / 100µm). Output curves are plotted in the top graph; double-swept transfer curves taken in saturation and triode regions are plotted on the bottom. As the bottom graph shows, gate leakage current through the parylene dielectric is low.

References

[1] R.L. Hoffman, B.J. Norris, and J.F. Wager, "ZnO-based transparent thin-film transistors," *Applied Physics Letters*, vol. 82, no. 5, pp. 733-735, Feb. 2003.

[2] P.F. Carcia, R.S. McLean, M.H. Reilly, and G. Nunes, "Transparent ZnO thin film transistors fabricated by RF magnetron sputtering," *Applied Physics Letters*, vol. 82, no. 7, pp. 1117-1119, Feb. 2003.

[3] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature*, vol. 432, pp. 488-492, Nov. 2004.

[4] E. Fortunato, P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martins, "Fully transparent ZnO thin-film transistor produced at room temperature," *Advanced Materials*, vol. 17, pp. 590-594, Mar. 2005.

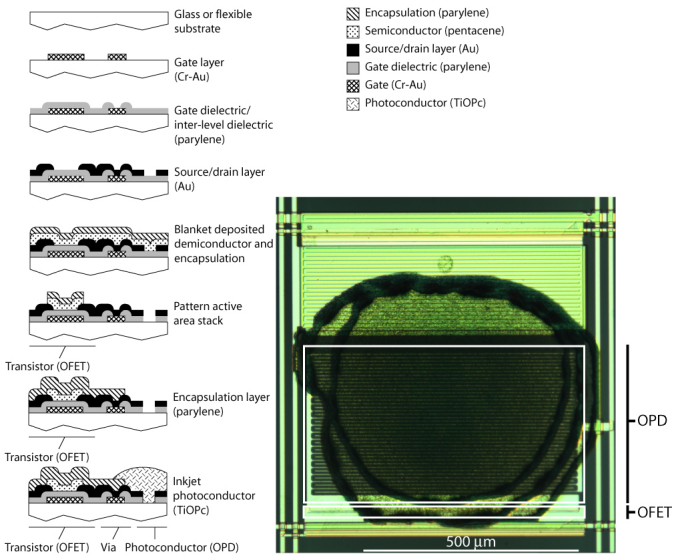
Engineering the Flatband Voltage in Organic Field-effect Transistors for Enhancement-depletion Mode Logic

I. Nausieda, D. He, K. Ryu, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

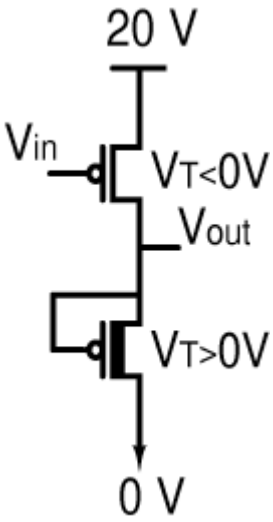
Organic semiconductors could enable large-area, mechanically flexible electronic systems such as e-paper, large-area imagers, and rollable displays due to their low processing temperatures and suitable electronic properties. We have developed a near-room-temperature (≤ 95 °C), scalable process to fabricate integrated organic field-effect transistors (OFETs) [1].

The OFET's semiconducting layer is a thin (15-nm) film of pentacene - chosen for its air-stability and high hole mobility (≈1 cm^2/Vs) [2]. Since there exists no air-stable, electron-transporting organic semiconductor with comparable mobility, our process produces p-channel transistors only. The nominal process pictured in Figure 1 yields enhancement-mode OFETs with threshold voltages of -1V.

The goal of this project is to achieve enhancement and depletion mode devices on a single substrate. The OFET flatband voltage, nominally the difference between the gate and semiconductor work functions, may be shifted by changing the gate metal work function. With the use of two gate metals, enhancement and depletion mode devices can be obtained. Such a process would enable the creation of high-noise margin inverters, robust to process variation (see Figure 2). Connecting the gate to the source permits use of the depletion-mode transistors as current sources, making possible a variety of analog circuits such as high-gain amplifiers and comparators.



▲ Figure 1: Integrated process for OFETs and organic photoconductors (OPDs) developed at MIT.



▲ Figure 2: Inverter/common-source amplifier with enhancement-mode driver and depletion-mode load.

References

[1] I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C.G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 527-532, Feb. 2008.

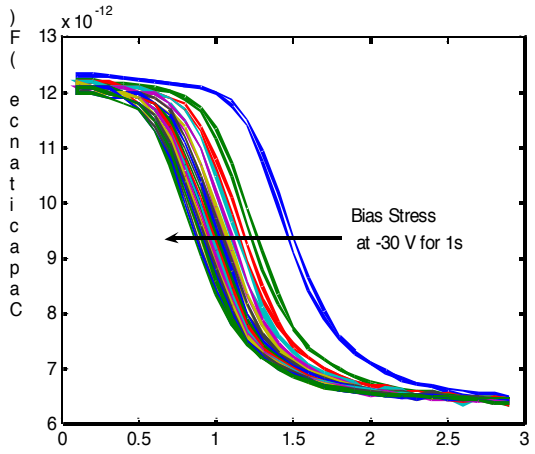
[2] H. Klauk et al., "High-mobility polymer gate dielectric pentacene thin film transistors," *Journal of Applied Physics*, vol. 92, no. 9, pp. 5259-5263, Nov. 2002.

Bias-induced Instability in Pentacene and Zinc Oxide Thin-film Transistors

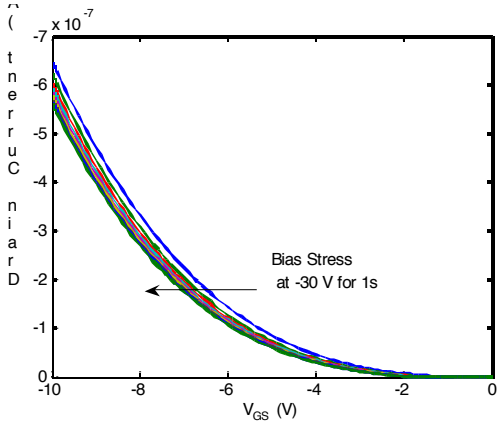
K. Ryu, D. He, I. Nausieda, A. Wang, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

Thin-film transistors (TFTs) are a type of field-effect transistor made by depositing a thin film of semiconductor as the active layer over a substrate that provides mechanical support. This thin semiconductor layer is polycrystalline or amorphous, which results in trap states in the bandgap and therefore exhibits poorer carrier mobility than single crystal films. However, TFTs can enable large-area electronics because they are not limited by the substrate materials. The TFTs based on semiconducting organic small molecules (e.g., pentacene) and metal oxides (e.g., zinc oxide) offer near-room-temperature processing, which makes them compatible with lightweight, flexible plastic substrates. These new devices have been employed to make paper-like flexible displays that are commercially available. Although TFTs' primary function has been limited to the switching elements in displays, there is significant interest in expanding their function to integrate new digital and analog circuit blocks such as display decoders, multiplexers, and OLED drivers. Operational stability is required for these new applications, but both organic TFTs and metal oxide TFTs have been reported to have bias-stress stability problems. Figures 1 and 2 show that for gate bias stress of -30V for ten seconds, the flatband voltage shifts 0.6 V.

The goal of this work is to investigate the mechanisms that cause bias-induced instability in pentacene and zinc oxide transistors and use the knowledge to develop a method of quenching bias-instability for thin-film transistors at low processing temperatures. The work involves physical modeling of I-V, and C-V characteristics of TFTs to identify the changing physical parameters. Electrical characterization methods such as 1/f noise, I-V, and C-V measurements will be employed to determine the mechanisms that cause bias instability.



▲ Figure 1: A C-V graph of a pentacene TFT (1000/25 μm), which shows V_{FB} shift as the bias-stress is applied.



▲ Figure 2: An I-V graph of a pentacene TFT (1000/25 μm), which shows V_{FB} shift as the bias-stress is applied.

References

[1] K. Ryu, I. Kymissis, V. Bulović, and C.G. Sodini, "Direct extraction of mobility in pentacene OFETs using C-V and I-V measurements," *IEEE Electron Device Letters*, vol. 26, no. 10, pp. 716-718, Oct. 2005.

[2] I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C.G. Sodini, "An organic imager for flexible large area electronics," *IEEE International Solid-State Circuits Conference Digest*, San Francisco, Feb. 2007, pp. 72–73.

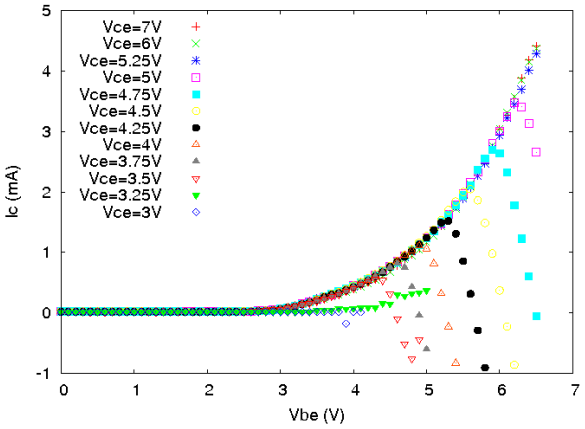
Fabrication of the Ferromagnetic Kisaki Transistor

M. van Veenhuizen, J. Chang, J.S. Moodera
Sponsorship: DARPA, KIST-MIT project

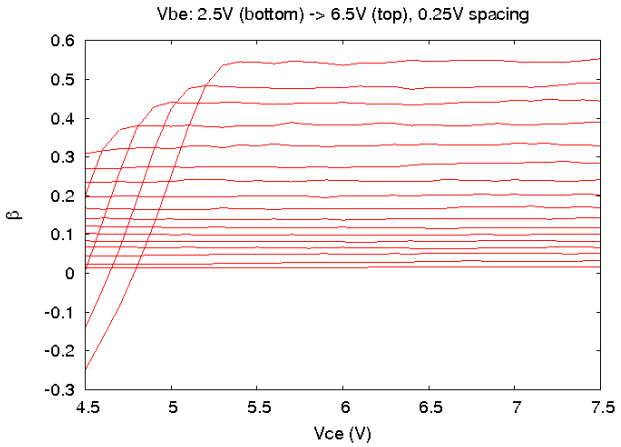
The research field of spintronics, which aims at creating electronic devices based on the spin quantum number of the charge carriers, has seen a major advancement since its invention two2 decades ago, culminating in this year's Nobel Prize for the GMR spin-valve. The current emphasis is on semiconductor spintronics, which, owing to the long spin-coherence lengths as well as engineering feasibility, is promising for new or better device technology. Conventional sources of spin-polarization are the 3-d ferromagnets whose high Curie temperatures as well as ease of fabrication make them a logical choice as sources of spin-current into semiconductors. However, the incorporation of ferromagnetic metals with semiconductors is hampered by the conductivity mismatch that hinders efficient spin-injection[1], and also by Schottky-barrier formation.

This project aims at realizing efficient spin-injection into silicon. Silicon has a very long spin-coherence length [2] and is therefore especially suitable for spintronics applications. The electrical spin-injection is achieved by means of a ferromagnetic Kisaki transistor [3], a scheme that overcomes both the conductivity mismatch as well as Schottky barrier formation. The Kisaki transistor is a bipolar transistor with the n-type emitter being a metal, separated from the p-type base by a tunnel junction. Figures 1 and 2 demonstrate the transistor action for an early version of the transistor. The current emphasis is on improving the device performance.

We gratefully thank Siltronic for the generous donation of silicon wafers.



▲ Figure 1: Emitter current as a function of base-emitter voltage for different values of collector-emitter voltages.



▲ Figure 2: Current ratio as a function of collector-emitter voltage for different values of base-emitter voltages.

References

[1] G. Schmidt, D. Ferrand, L.W. Molenkamp, A.T. Filip, and B.J. van Wees, "Fundamental obstacle for electrical spin injection from a ferromagnetic metal into a diffusive semiconductor," *Physical Review B*, vol. 62, no. 8, pp. 4790-4793(R), Aug. 2000.

[2] B. Huang, D.J. Monsma, and I. Appelbaum, "Coherent spin transport through a 350 micron thick silicon wafer," *Physical Review Letters*, vol. 99, no. 17, pp. 177209:1-4, Oct. 2007.

[3] H. Kisaki, "Tunnel transistor," in *Proc. IEEE*, vol. 61, pp. 1053-1054, July 1973.

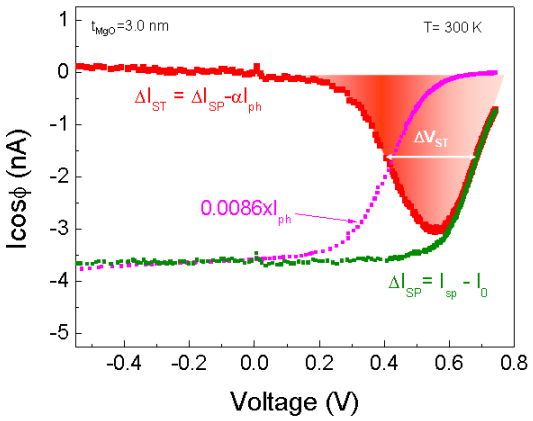
Spin-dependent Photocurrent Transport in GaAs/MgO/Fe Structure

Y.J. Park, M. van Veenhuizen, D. Heiman, C.H. Perry, J.S. Moodera
Sponsorship: KIST-MIT project

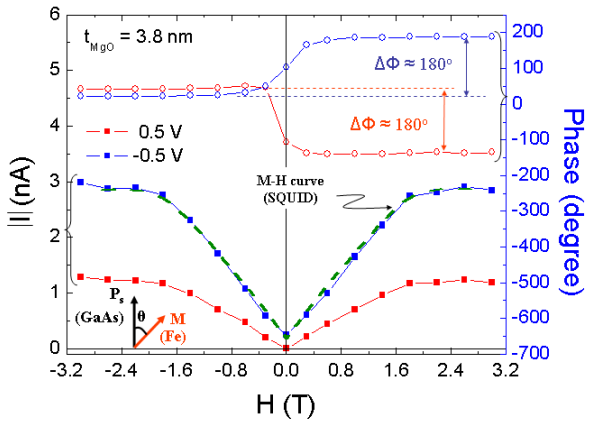
Our approach employs MgO/Fe as a spin injector/detector on a GaAs semiconductor. To understand the spin filtering effect of this GaAs/MgO/Fe structure, we used the measurement technique of spin-dependent photo-current (SDPC)[1] to create a spin-imbalance in the GaAs by optical means that is subsequently detected electrically through the MgO/Fe structure. The growth of 2-4 nm MgO/7 nm Fe/4 nm Au layers on n+(001) GaAs substrates was performed in a molecular beam epitaxy (MBE) system with a base pressure ~ $2x10^{-10}$ torr. The layers were deposited at room temperature with typical deposition rates of 0.01-0.02 nm/s. Post-annealing was conducted in the growth chamber under UHV conditions.

Figure 1 shows one of the results, the bias dependent in-phase component of photocurrent. Here, ΔI_{ST} represents the spin-transferred photocurrent, which is defined by $\Delta I_{SP} - \alpha I_{ph}$, where ΔI_{SP} is a net spin-dependent photocurrent and αI_{ph} is a magneto-optical background, such as MCD (magnetic circular dichroism), contribution. The MCD fit parameter, α, is estimated to be 0.0086, as Figure 1 shows. The I_{ph} represents unpolarized light-induced total photocurrent. The net SDPC, ΔI_{SP}, is obtained by subtracting the zero field photocurrent I_0. A simple manipulation of the measured photocurrents leads to a clear spin current transferred region (shaded area in Figure 1) at $0.2V \le V \le 0.75$ V, which is much broader (i.e., ΔV_{ST} ~0.3V, determined by full width at half maximum of bias dependent spin transferred photocurrent) than those of Schottky barrier (~0.08V)[2] and AlGaAs barrier cases (~0.1V)[3]. This is closely related to the carrier transport processes associated with MgO tunnel barrier.

Figure 2 shows the photocurrent amplitude and phase as a function of applied magnetic field. The M-H curve of the Fe layer is in good agreement with the photocurrent. This finding indicates that the SDPC varies with the P_s (spin polarization of photo-excited carriers in the GaAs) and M (magnetization of Fe layer). Also shown is the phase dependence of the photocurrent: a clear phase shift of approximately 180° depending on the bias can be observed as the magnetic field sweeps from minus to plus. Finally, the GaAs/MgO/Fe structure unambiguously showed a spin-filtering effect, which is useful for the device application.



▲ Figure 1: Spin-dependent photocurrent measured at 300K. The shaded area represents the spin-filtered photocurrent region. The MCD fit parameter α was estimated to be 0.0086.



▲ Figure 2: Magnetic field-dependence of spin-dependent photocurrent (left axis) and phase change (right axis). The dotted line is the M-H curve obtained from SQUID measurement. Bottom left inset shows the definition of angle θ between Ps and M.

References

[1] A. Hirohata, S.J. Steinmueller, W.S. Cho, Y.B. Xu, C.M. Guertler, G. Wastlbauer, J.A.C. Bland, and S.N. Holmes, "Ballistic spin filtering across ferromagnet/semiconductor interfaces at room temperature," *Physical Review B*, vol. 66, pp. 035330:1-11, July 2002.

[2] S.J. Steinmuller, C.M. Gurtler, G. Wastlbauer, and J.A.C. Bland, "Separation of electron spin filtering and magnetic circular dichroism effects in photoexcitation studies of hybrid ferromagnet/GaAs Schottky barrier structures," *Physical Review B*, vol. 72, pp. 045301:1-5, July 2005.

[3] S.E. Andresen, S.J. Steinmuller, A. Ionescu, G. Wastlbauer, C.M. Guertler, and J.A.C. Bland, "Role of electron tunneling in spin filtering at ferromagnet/semiconductor interfaces," *Physical Review B*, vol. 68, pp. 073303:1-4, Aug. 2003.

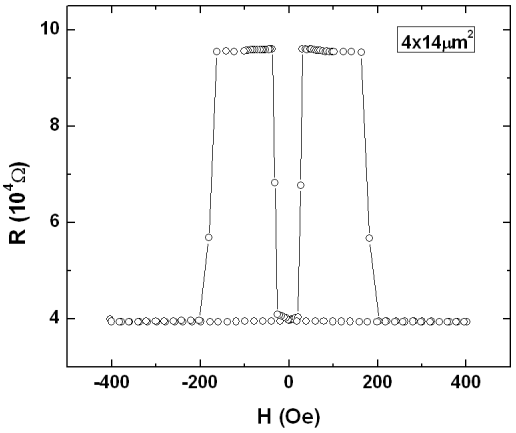
Spin Torque Transfer Study in Fully Epitaxial Fe/MgO/Fe MTJs for MRAM Applications

G.X. Miao, J.S. Moodera

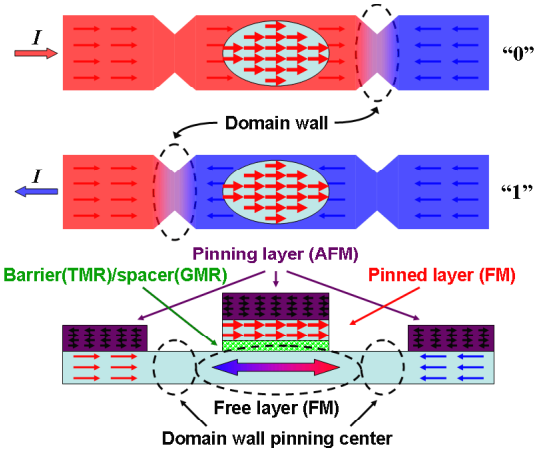
Sponsorship: NSF, ONR, KIST-MIT project

Magnetic Random Access Memory (MRAM) is the new generation of universal memory unit, and it has all the advantages of high density, high speed, non-volatility, and high endurance for harsh environments. The newly discovered memory "writing" mechanism based on spin transfer torque (STT) [1] has shown promise to further increase memory density. In our lab, we use a UHV MBE system to deposit the fully epitaxial Fe/MgO/Fe magnetic tunnel junction (MTJ) stacks on top of etched Si (100), and we use the MTL facilities for the micro-fabrications. Due to the presence of coherent tunneling in such epitaxial systems [2] (i.e., the tunneling electrons conserve both their spins and the angular momentum), a giant TMR of 150% has been achieved at room temperature (see Figure 1).

In order to bypass the large current density required for an STT-based switching mechanism, we fabricate the domain wall storage unit as illustrated in Figure 2. The writing current now flows completely inside the free layer and the spin transfer torque from this current can toggle the domain wall between the "left" and the "right" pinning positions when the current is flowing towards left, or right, respectively, thus enabling the writing of the "0" and "1" memory states. This novel writing technique can dramatically reduce the probability of tunnel barrier breakdown and increase the durability of the device.



▲ Figure 1: An example of Fe/MgO/Fe-based MTJ at RT. The top Fe layer is magnetically hardened with Co in order to achieve the desired magnetic separation.



▲ Figure 2: The domain wall position can be toggled between the pinning centers, by alternating the driving current direction, and the TMR stack on top will read the memory state of the unit. The free layer is one electrode of the MTJ.

References

[1] E.B. Myers, D.C. Ralph, J.A. Katine, R.N. Louie, and R.A. Buhrman, "Current-induced switching of domains in magnetic multilayer devices," *Science*, vol. 285, pp. 867-870, Aug. 1999.

[2] W.H. Butler, X.-G. Zhang, T.C. Schulthess, and J.M. MacLaren, "Spin-dependent tunneling conductance of Fe|MgO|Fe sandwiches," *Physical Review B*, vol. 63, pp. 054416-054427, Jan. 2001.

Development of MgB2 Superconductor-based Electronics: Basic and Device Studies

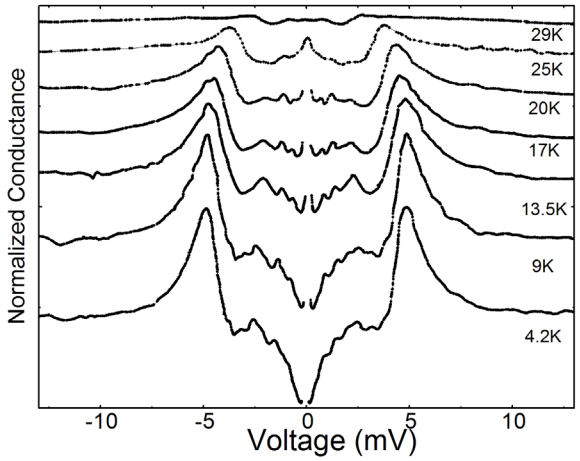
M.V. Costache, G. Miao, J.S. Moodera
Sponsorship: ONR

Magnesium diboride (MgB_2), a material known since the 1950s, was recently discovered to be superconductor at a remarkably high critical temperature *Tc* = 40 K for a binary compound, its high *Tc*, simple crystal structure, large coherence lengths, and high critical current densities and fields indicate that MgB_2 has potential for superconducting devices that operate at 20-30 K, the temperature reached by current commercial cryocoolers. Furthermore, the larger superconducting gap allows for higher operating speeds (up to 3.5 THz) than Nb-based junctions.

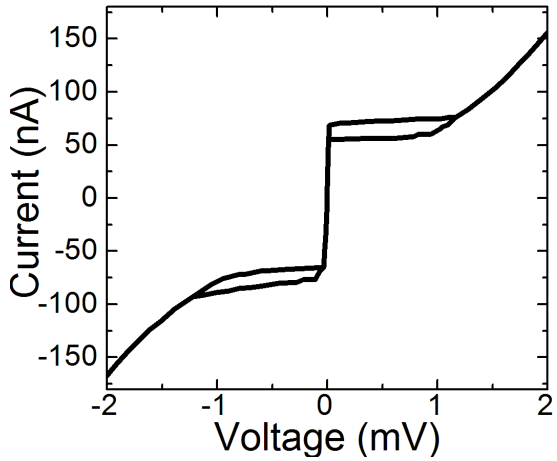
The goal of the project is to growth epitaxial superconducting MgB_2 thin films by molecular beam epitaxy (MBE) suitable for fabrication of all-MgB_2 Josephson junctions. Using MBE technique we have fabricated MgB_2/I/MgB_2 tunnel junctions [1, 2] where the tunnel barrier (I) is natural (by oxidation of base electrode) or artificial (e.g., Al_2O_3, MgO and AlN).

Figure 1 shows the conductance vs. voltage at selected temperatures for a MgB_2/native oxide/MgB_2 tunnel junction defined using shadow mask techniques. In spite of the presence of superconducting energy gaps to over 30 K, the junction exhibited sub-gap characteristics and no supercurrent was observed. Furthermore, we have fabricated MgB_2/MgO/MgB_2 tunnel junctions using photolithography and etching techniques. As expected, the dc Josephson effect was observed for this junctions, as Figure 2 shows. For the fabrication of all-MgB_2 Josephson junctions-based devices, our results demonstrate that the junction oxidation process is less reliable in contrast to growing an artificial barrier.

We acknowledge the Office of Naval Research for providing financial support.



▲ Figure 1: Normalized conductance vs. voltage at selected temperatures for a MgB_2/natual oxide/MgB_2 junction.



▲ Figure 2: The I-V characteristics for a MgB_2/MgO/MgB_2 junction, showing dc Josephson effect.

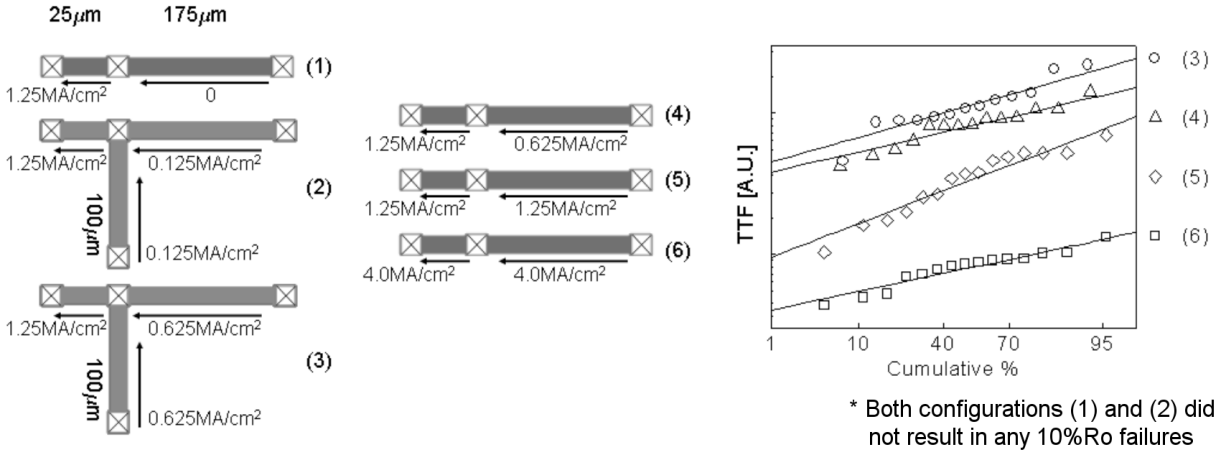
References

[1] H. Shim, K.S. Yoon, and J.S. Moodera, "All MgB2 tunnel junctions with Al_2O_3 or MgO tunnel barriers," *Applied Physics Letters*, vol. 90, no. 21, pp. 212509:1-3, May 2007.
[2] M.V. Costache and J.S. Moodera, in preparation.

Effects of Active Atomic Sinks and Reservoirs on the Reliability of Cu/low-*k* Interconnects

F.L. Wei, C.S. Hau-Riege (AMD), A.P. Marathe (AMD), T.J. Park, T. Chookajorn, C.V. Thompson
Sponsorship: Intel, AMD, Texas Instruments, SRC

Electromigration experiments using Cu/low-*k* interconnect tree structures (as in Figure 1) were carried out in order to study the effects of active atomic sinks and reservoirs on interconnect reliability. In all cases, failures occurred after a long period of void growth. Kinetic parameters were extracted from resistance versus time data, giving $(Dz^*)_{0,eff}$ = 3.9 x 10^{-10} m^2/s and z^* = 0.40± 0.12. Using these values, the evolution of stress in each of the interconnect tree segments could be calculated and correlated with the rate of void growth and failure times for all test configurations. It is demonstrated that segments that serve as atomic sinks and reservoirs for the failing segments affect the lifetime by modifying the conditions for stress-induced migration. Reservoirs can lead to increased lifetimes, while sinks can lead to reduced lifetimes. We made quantitative predictions of the times required for failure for Cu/low-*k* interconnect trees as a function of the effective bulk elastic modulus of the interconnect system, *B*. As the Young's modulus of the inter-level dielectric (ILD) films decreases, *B* decreases; further, the positive effects of reservoirs are diminished and the negative effects of sinks are amplified [1].



▲ Figure 1: Simple multi-segment interconnect trees were tested with different currents in each segment. In the case shown above, tests were carried out to determine effects of both active (with current) and inactive (without current) segments serving as atomic reservoirs for the short segment. The arrows indicate the direction of electron transport. Both active and inactive reservoirs lead to improved reliability. Interconnect trees were also tested with long segments serving as atomic sinks for short test segments. These atomic sinks led to a degradation in reliability.

Reference

[1] F.L. Wei, C.S. Hau-Riege, A.P. Marathe, and C.V. Thompson, "Effects of active atomic sinks and reservoirs on the reliability of Cu/low-*k* interconnects," *Journal of Applied Physics*, 2008, to be published.

Surface Electromigration, Void Dynamics, and the Reliability of IC Interconnects

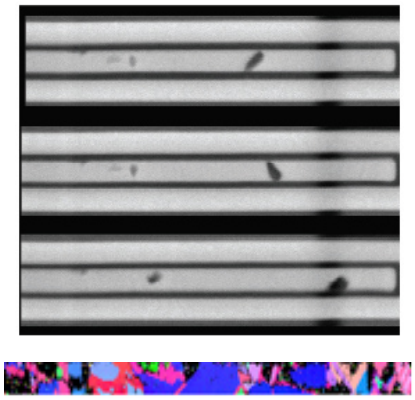
Z.-S. Choi, R. Monig, T. Chookajorn, T.J. Park, C.V. Thompson
Sponsorship: Intel, AMD, SRC

Electromigration is atomic diffusion due to a momentum transfer from conducting electrons. Electromigration of metallic IC interconnects is and will remain a major reliability concern as future technologies demand increasing device and wire densities as well as higher current densities. In Cu-based metallization, electromigration occurs by diffusion of Cu at the interface between polycrystalline Cu and the dielectric overlayer, and it leads to formation of voids that cause an increase in resistance and to failure. The rate of failure is therefore highly dependent on the Cu atomic diffusivity, which is affected by the grain structure of the Cu, as well as the stress conditions.

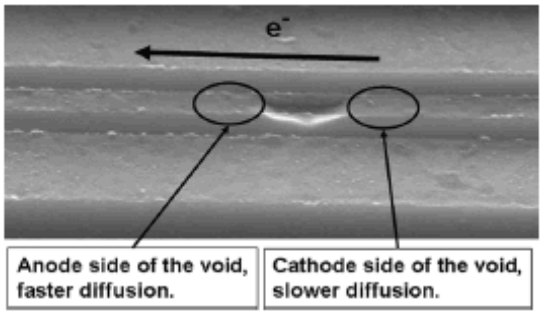
In situ scanning electron microscope observations have been performed on passivated Cu interconnects of different widths during accelerated electromigration tests. In some cases, voids form and grow at the cathode. However, an alternative failure mode is also observed, during which voids form distant from the cathode and drift toward the cathode, where they eventually lead to failure. The number of observations of this failure mode increased with increasing line width. During void motion, the shape and the velocity of the drifting voids varied significantly. Postmortem electron backscattered diffraction (EBSD) analysis was performed (see Figure 1), and a correlation of EBSD data with the *in situ* observations reveals that locations of voids, their shape evolution, and their motion all strongly depend on the locations of grain boundaries and the crystallographic orientations of neighboring grains. [1]

A separate experiment determined surface electromigration rates on oxide-free surfaces of unpassivated damascene Cu interconnect segments through electromigration testing under vacuum. Electromigration-induced voids grew at the cathode end of the segments due to a flux divergence at refractory-metal-lined vias to the lead lines below the test segment. Diffusivity on a clean Cu surface was determined by measuring the size of the voids as a function of time and test temperature at a fixed current. An activation energy of 0.45±0.11 eV and a pre-factor of 3.35 x 10^{-12} m^2/s were found for the product of the effective charge z^* and the surface diffusivity D_s [2]. Through correlations of void growth rates with the crystallographic textures of adjacent grains (Figure 2), relative surface diffusivities for grains with different crystallographic orientations have been determined [3].

Data acquired in the experiments described above are being used in simulations of electromigration-induced failure, to develop improved methods for reliability projections based on accelerated electromigration tests.



▲ Figure 1: *In situ* SEM images of the cathode of a test structure, showing void drift toward cathode end. The test line is surrounded by a Cu-extrusion monitor. Bottom image is a texture mapping by EBSD obtained after EM test.



▲ Figure 2: EBSD has been used to determine the crystallographic orientations of grains adjacent to voids. Correlation with void growth rates allows determination of relative values of the surface diffusivity.

References

[1] Z.-S. Choi, R. Mönig, and C.V. Thompson, "Dependence of the electromigration flux on the crystallographic orientations of different grains in polycrystalline copper interconnects," *Applied Physics Letters*, vol. 90, p. 241913, 2007.

[2] Z.-S. Choi, R. Mönig, and C.V. Thompson, "Activation energy and pre-factor for surface electromigration and void drift in Cu interconnects," *Journal of Applied Physics*, vol. 102, p. 083509, 2007.

[3] Z.-S. Choi, R. Mönig, and C.V. Thompson, "Effects of microstructure on the formation, shape, and motion of voids during electromigration in passivated copper interconnects," *Journal of Materials Research*, vol. 23, p. 383-391, 2008.

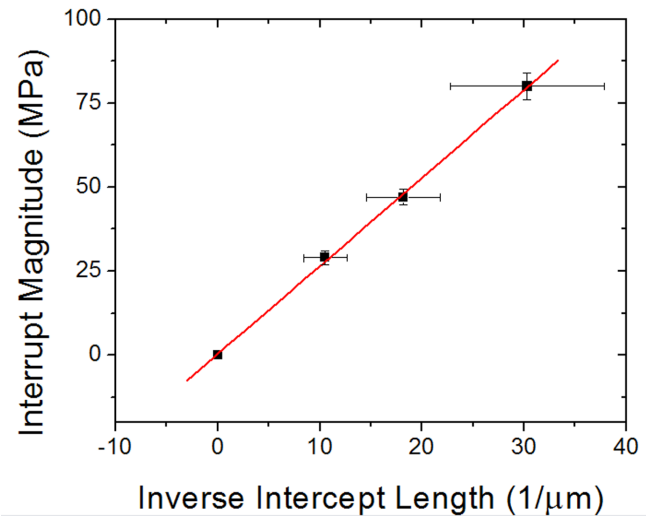
Grain Structure and Residual Stress in Polycrystalline Metallic Films

J. Leib, C.V. Thompson
Sponsorship: NSF

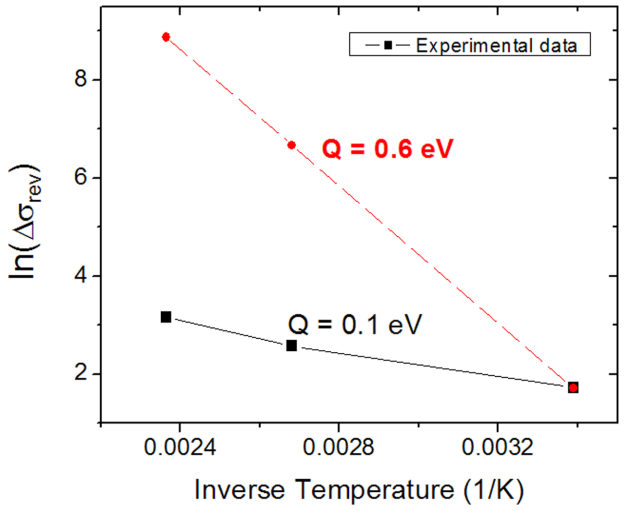
In thin metal films deposited for various applications, there are obvious advantages to both understanding and controlling the intrinsic stresses in the films as-deposited. For high-mobility metal films (e.g., Au, Ag, Al, Cu) deposited on amorphous substrates, much of the observed stress can be attributed to the grain structure that evolves as the Volmer-Weber film transitions from individual islands to a continuous film. The stress behavior during this process shifts from tensile (during island coalescence) to compressive (as the film grows past continuity). Initially, the grain size of the continuous film is equal to the island size at coalescence.

The role of grain boundaries in the post-coalescence compressive stress has been debated extensively in the literature [1-4], but no experimental research has been performed to quantify the relationship between grain size and stress in polycrystalline films. In-situ stress monitoring and transmission electron microscopy (TEM) have been used to investigate stress and grain size in gold films deposited on silicon nitride. When films were treated to different grain sizes, stress-measured, and then imaged in TEM, the inverse of grain size and corresponding tensile rise was found to be linear, with zero stress at infinite grain size. This relationship indicates that grain boundaries are critical to the formation of compressive stress in these films, with the stress proportional to the grain boundary perimeter line length per area of film (see Figure 1).

While this result supports a model for compressive stress arising from trapping of an excess population of self-interstitials at grain boundaries (as in reference [3]), the expected relaxation of these defects would be their diffusion back to the surface and attachment to surface steps. However, the thermal activation for grain boundary diffusion (~0.6 eV) was not observed in the corresponding stress relaxation (see Figure 2). Current investigations focus on identification of mechanisms consistent with the observed small activation energy (~0.1eV).



▲ Figure 1: Stress as a function of inverse grain size. As the grain size increases, the stress trends towards zero.



▲ Figure 2: Activation plot of log stress as a function of inverse temperature. The black line shows experimental data, while the red line shows the expected trend for self-interstitial grain boundary diffusion in gold. The difference at the highest temperature is more than two orders of magnitude.

References

[1] F. Spaepen. "Interfaces and stresses in thin films," *Acta. Materialia*, vol. 48, pp. 31-42, 2000.

[2] R.C. Cammarata, T.M. Trimble, and D.J. Srolovitz. "Surface stress model for intrinsic stresses in thin films," *Journal of Materials Research*, vol. 15, no. 11, pp. 2468-2474, Nov. 2000.

[3] E. Chason, B.W. Sheldon, L.B. Freund, J.A. Floro, and S.J. Heame, "Origin of compressive residual stress in polycrystalline thin films," *Physical Review Letters*, vol. 88, no. 15, p. 156103, Apr. 2002.

[4] C. Friesen and C.V. Thompson, "Correlation of stress and atomic-scale surface roughness evolution during intermittent homoepitaxial growth of (111)-oriented Ag and Cu," *Physical Review Letters*, vol. 93, no. 5, p. 056104, July 2004.

12-Watt Thermoelectric Generator Powered by Combustion

P. Santhanam, R.J. Ram

Sponsorship: ONR Thermo-Electric Conversion MURI Program

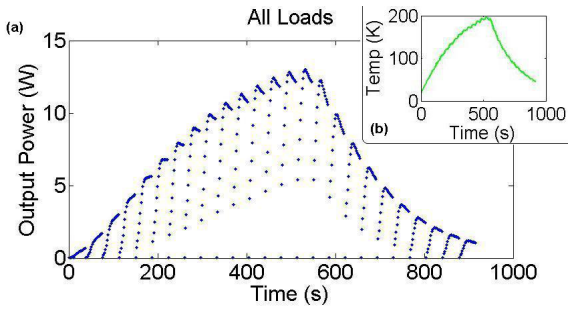
As part of a recent effort to demonstrate the capability of newly-developed thin-film thermoelectric (TE) materials to generate macroscopic quantities of electrical power, we have constructed a 12-watt TE generator.

Both the efficiency of TE generators and the coefficient of performance for TE coolers are closely tied to a quantity Z, which depends on the material's Seebeck coefficient (S), electrical conductivity (σ), and thermal conductivity ($\kappa = \kappa_e + \kappa_{ph} \approx \kappa_{ph}$). For this reason, when evaluating TE materials it is common to define the figure-of-merit ZT, where T is the absolute temperature, as $ZT = \left(S^2\sigma/\kappa\right)T$. Despite much initial excitement over the potential for semiconductors in the field during the 1950s, the limited application of thermoelectricity has been due in great part to the decades-long stagnation of the maximum achievable room-temperature ZT (~1 for Bi_2Te_3) [1]. Recently, however, new nanostructured materials have shown promise to break this trend [2, 3], and there is strong evidence that the gains thus far are due to a reduction in phonon-dominated thermal conductivity [4].

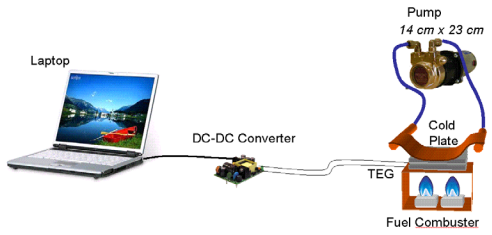
In the past five years, our MURI collaboration has developed a superlattice material formed with layers of InGaAs doped with Er beyond the solubility limit interleaved with undoped InGaAs. The material's doped layers contain amorphous ErAs islands that scatter short-wavelength phonons, while the superlattice structure scatters long-wavelength phonons. Together, these properties impede the phonon thermal transport, substantially decreasing the overall thermal transport and increasing the material's ZT.

While an increased ZT in theory implies electrical power generation efficiency, numerous system-level challenges become more prominent for thin-film materials being used in macroscopic generators. For instance, due to geometry alone, for a given thermal power flux, thin-film materials will see substantially smaller temperature drops from hot-side to cold than will their thicker bulk counterparts. On a system level, it is also possible for interfacial thermal impedances elsewhere in the generator to dominate the TE material in the overall thermal impedance of the generator, causing reduction of the thermal power flow between a given pair of fixed-temperature reservoirs. Together these issues can substantially reduce the temperature drop across the TE module itself and, since the generated electrical power is proportional to the square of the temperature drop, the overall power output as well.

In order to mitigate these concerns, we have chosen to first demonstrate thin-film thermoelectrics within a module that also contains a traditional bulk TE material. Our initial generator designs have implemented a commercial bulk TE module, which we have used to produce upwards of 12 W of DC electrical power (Figure 1a) due to a temperature drop of around 200K (Figure 1b). Our intentions are to replace this commercial bulk module with a segmented thin-film and bulk module, and use the generator to drive a low-power computer (Figure 2).



▲ Figure 1a: Electrical power output as a function of time. The peaks of the oscillations represent the impedance-matching condition for maximum power. The peak observed value is 12.99W. Figure 1b: Temperature difference across the module with time. Electrical power is proportional to the square of this temperature difference.



▲ Figure 2: Schematic for final demonstration system, set to include a module containing both thin-film and bulk TE materials.

References

[1] A. Majumdar, "Thermoelectricity in semiconductor nanostructures," *Science*, vol. 303, no. 5659, pp. 777-778, Feb. 2004.

[2] R. Venkatasubramanian, E. Siivola, T. Colpitts, and B. O'Quinn, "Thin-film thermoelectric devices with high room-temperature figures of merit," *Nature*, vol. 413, pp. 597-602, Oct. 2001.

[3] T.C. Harman, P.J. Taylor, M.P. Walsh, and B.E. LaForge, "Quantum dot superlattice thermoelectric materials and devices," *Science*, vol. 297, no. 5590, pp. 2229-2232, Sept. 2002.

[4] G. Chen, A. Narayanaswamy, and C. Dames, "Engineering nanoscale phonon and photon transport for direct energy conversion," *Superlattices and Microstructures*, vol. 35, no. 3-6, pp. 161-172, June 2004.

Bonded-wafer Process for Optimized InP Avalanche Photodetectors

H. Li, D. Oakley, J. Donnelly, V. Diadiuk, S. Groves

Fabrication of low-dark-count, low-after-pulsing InP avalanche photodetectors (APD) may require a "n-on-p" epilayer structure, whereas the crystal growth requirements favor a "p-on-n" sequence. The primary limitation in crystal growth is related to diffusion of the p-type dopant (Zn) that is normally used in organometallic vapor phase epitaxy (OMVPE).

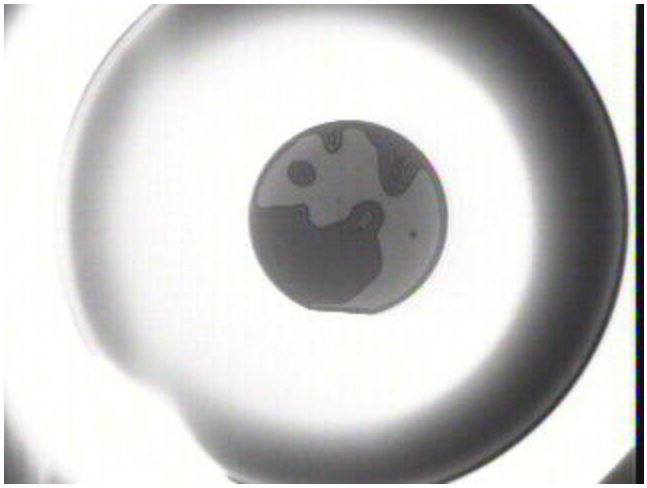
A possible way to overcome these limitations and achieve optimum conditions for both crystal growth and device structure capitalizes on MTL's extensive wafer bonding experience. The basic concept consists of growing the preferred InP epilayer structure (p-on-n) and then bonding the top layer of that wafer to a virgin InP wafer (the "handle wafer"), which becomes the new device substrate. After bonding, the original InP substrate is ground off by chemo-mechanical polishing (CMP) or wet-etched away and the APDs are fabricated on the composite wafer (which contains the transferred epilayers).

Preliminary experiments yielded bonded-wafer InP APDs that showed dark count rates (DCR) comparable to standard APDs, indicating that the bonding step does not damage the epi-layers or p-n junction; in addition, the bonded-wafer InP APDs, which have minimum Zn diffusion, are likely to exhibit reduced after-pulsing. Recently, epi-wafers that had substantially fewer particles on the surface were successfully bonded to virgin InP wafers without CMP, in spite of a few surface inclusions and non-uniformities. This is an important step forward, since InP is very fragile and easily damaged. Figure 1 shows an infra-red image of the two wafers in contact but not bonded; Figure 2 shows this bonded-pair after annealing at 300 ˚C for 3 hours; diffraction rings show where the surface is NOT bonded. There are many large well-bonded areas suitable for detector fabrication.

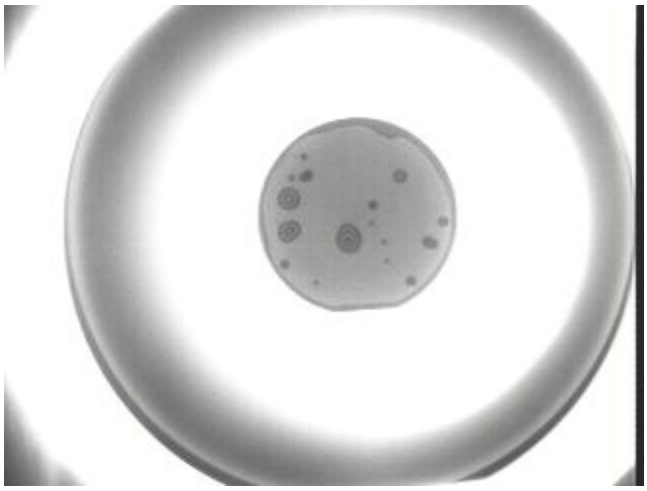
Wet etching in HCl , rather than grinding, was successful for removing the original substrate. Given the presence of the InGaAs layer, which serves as an etch stop, wet etching is very effective and it increases process robustness and reproducibility. APDs have been fabricated and measurement of DCR and after-pulsing show that there is no degradation in the device performance due to either the bonding step or substrate removal. Epi wafers with better surfaces and different epi-layer composition will be grown to optimize detector performance.

Future plans include replacing the InP handle wafer with a GaP wafer in which a lenslet array has been fabricated. This would provide several fabrication and device performance advantages such as elimination of the air gap between the detector and lenslet arrays, wafer-level alignment of detector and lenslet arrays, and increased detection efficiency.

This work is supported by a grant from the Lincoln Laboratory Advanced Concepts Committee.



▲ Figure 1: An infra-red image of InP wafer 377-A, in contact with a new InP substrate; large dark areas indicate gaps between the 2 surfaces.



▲ Figure 2: An infra-red image of bonded-pair 377-A, annealed at 300˚C for 3 hrs; diffraction rings show where the surface is NOT bonded.

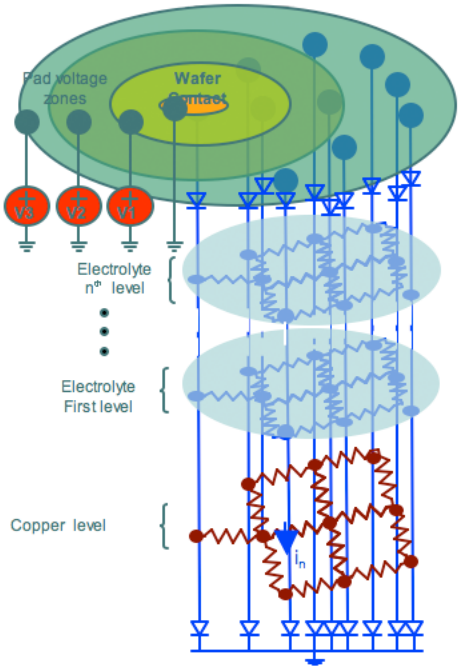
Modeling of Electrochemical-mechanical Planarization (eCMP)

J .Johnson, W. Fan, Z. Li, D.S. Boning

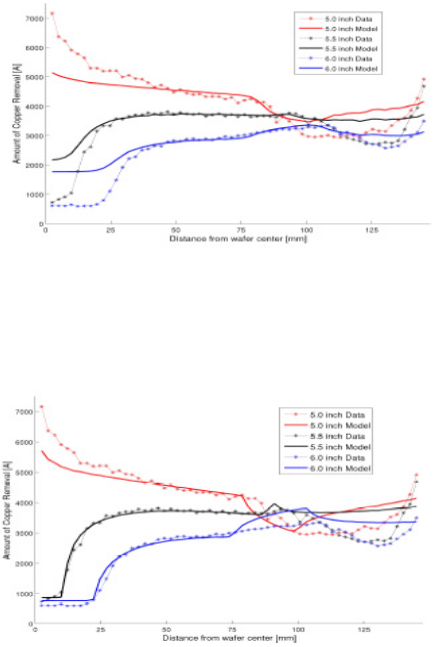
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

The process of electrochemical-mechanical polishing (eCMP) is well established for the removal of bulk copper. In previous work, a wafer-level physically-based eCMP model accounting for time-averaged current-density distributions across a wafer due to multiple cathodic voltage zones was proposed. An extension of this purely ohmic model to a non-ohmic model accounting for the exponentional dependence of current on overpotential at the electrode/electrolyte interface has been developed. As Figure 2 shows, the model captures the nonlinear dependence of removal rate on applied voltage in different voltage zones across the wafer. We are seeking to extend and complete this non-ohmic model to account for the electrochemical reactions occurring at both the anode (wafer) and cathode as well as the lateral coupling/current contributions. Figure 1 shows the new extended model, which accounts for the electrical current distributions on the wafer surface and in the electrolyte, yielding the copper removal rate at each location on the wafer. We are also examining the effects of passivation layer formation and removal on the time-averaged voltage.

This enhanced eCMP model will attempt to adequately characterize the full removal of copper physically and electrochemically, in hopes of optimizing the process to remove the entire copper layer as well as the barrier metal, reducing the need for traditional CMP. Ultimately we seek to model the eCMP process on the wafer, chip, and feature scale, capturing both layout pattern dependency and tool uniformity effects.



▲ Figure 1: Modified wafer-level modeling approach for eCMP, accounting for the distribution of current at the wafer and platen electrodes and through the electrolyte.



▲ Figure 2: Amount of copper removal for head positions of 5.0, 5.5, and 6.0 inches, and voltage zone settings of V1,V2, and V3 = 2, 1, and 3V, respectively. (Top) Basic ohmic model versus data. The RMS error of this fit is 531 Å. (Bottom) Non-ohmic model versus data. The RMS error of this fit is 412 Å, a 22% improvement.

Reference

[1] Z. Li, D. Truque, D. Boning, R. Caramto, and C. Borst, "Modeling wafer level uniformity in electrochemical-mechanical polishing (ECMP)," *Advanced Metallization Conference*, Albany, NY, Oct. 2007.

3

Molecular & Nanotechnology

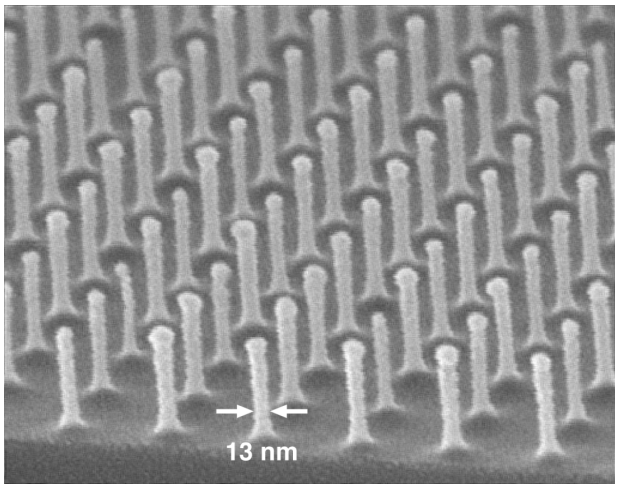
Table of Contents

Interference Lithography

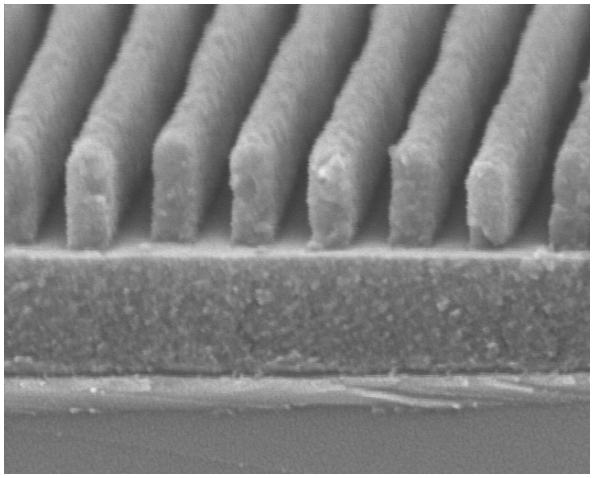
T.B. O'Reilly, H.I. Smith
Sponsorship: Singapore-MIT Alliance

The NanoStructures Laboratory has conducted research on interference lithography (IL) for many years, developing tools and techniques to create periodic structures (such as gratings and grids) over a wide range of spatial periods. The lab currently operates three IL systems. Two of them, the Lloyd's mirror and Mach-Zehnder IL systems use 325 nm light from helium-cadmium lasers. The Lloyd's mirror IL system can be quickly and easily configured to produce gratings with periods as small as 165 nm or as large as many microns. The flexibility and ease of use of this system enables its use by a large number of researchers to produce periodic and quasiperiodic structures for use in a wide range of research programs. The Mach-Zehnder IL system, while less flexible than the Lloyd's mirror, produces higher quality gratings that are suitable for metrological applications. The third system, the Achromatic IL system (AIL) is a grating-based interferometer that writes 100 nm-period gratings using 193 nm light from an ArF excimer laser. In addition, the NSL has close ties to the Space Nanotechnology Lab at MIT, which operates the NanoRuler. The NanoRuler is the most precise IL systems in the world.

We are currently developing a method to characterize photoresist performance by double-exposing a sample on an IL system; the sample is rotated slightly between the two exposures. By analyzing the resulting pattern one can determine how linewidth varies with exposure dose and dose modulation in fewer exposures than are required by previously described methods. The new method is currently being extended to make it possible to model variation of linewidth across the exposure area in systems such as the Lloyd's mirror or Mach-Zehnder IL systems.



▲ Figure 1: Scanning electron micrograph of a 100 nm-period grid produced with the AIL system. PMMA was exposed on top of an antireflection coating and the pattern was transferred into Si by reactive ion etching.



▲ Figure 2: Micrograph of 165 nm period grating produced with the Lloyd's mirror in photoresist above an antireflection coating. The Lloyd's mirror system can be used to produce patterns with spatial periods ranging from 165 nm up to several microns.

Reference

[1] T.B. O'Reilly and H.I. Smith, "Photoresist characterization using double exposures with interference lithography," *Journal of Vacuum Science and Technology B*, vol. 26, no. 1, pp. 128-131, 2008.

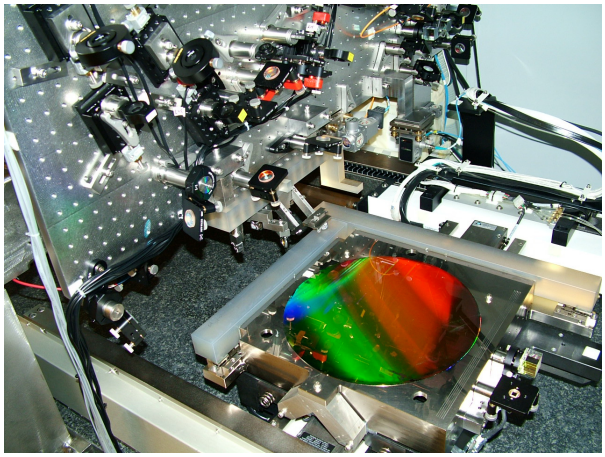
Scanning Beam Interference Lithography

M. Ahn, C.-H. Chang, R. Heilmann, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA

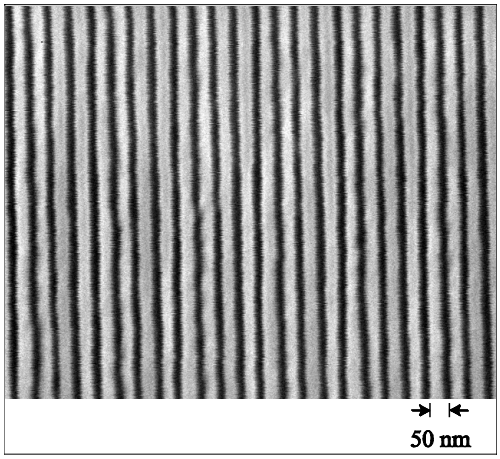
Traditional methods of fabricating gratings, such as diamond-tip ruling, electron and laser-beam scanning, or holography, are generally very slow and expensive and result in gratings with poor control of phase and period. More complex periodic patterns, such as gratings with chirped or curved lines, or 2D and 3D photonic patterns, are even more difficult to pattern. This research program seeks to develop advanced interference lithography tools and techniques to enable the rapid patterning of general periodic patterns with much lower cost and higher fidelity than current technology.

Interference lithography (IL) is a maskless lithography technique based on the interference of coherent beams. Interfering beams from an ultra-violet laser generates interference fringes that are captured in a photo-sensitive polymer resist. Much of the technology used in modern IL practice is borrowed from technology used to fabricate computer chips. Traditional IL methods result in gratings with large phase and period errors. We are developing new technology based on interference of phase-locked scanning beams, called scanning beam interference lithography (SBIL). The SBIL technique has been realized in a tool called the MIT Nanoruler, which recently won a R&D 100 Award (Figure 1). Large gratings can be patterned in a matter of minutes with a grating phase precision of only a few nanometers and a period error in the ppb range.

Current research efforts seek to generalize the SBIL concept to pattern more complex periodic patterns, such as variable period (chirped) gratings, 2D metrology grids, and photonic patterns [1]. Important applications of large, high fidelity gratings are for high-resolution x-ray spectroscopes on NASA x-ray astronomy missions, high-energy laser pulse compression optics, and length metrology standards. We have recently developed a new grating patterning technique called aligned multiple overlay SBIL, which uses multiple (up to four) precisely overlaid IL images to divide the fundamental grating pattern down to very short periods, in this case 50-nm-pitch, over large areas (Figure 2). This type of pattern has many applications including nanomagnetics, semiconductor, and nanobiologic manufacturing.



▲ Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.



▲ Figure 2: A 50-nm-pitch (25-nm-line/space) grating pattern fabricated by 4X overlaid interference lithography.

References

[1] G.S. Pati, R.K. Heilmann, P.T. Konkola, C. Joo, C.G. Chen, E. Murphy, and M.L. Schattenburg, "A generalized scanning beam interference lithography system for patterning gratings with variable period progressions," *Journal of Vacuum Science Technology B*, vol. 20, pp. 2617-2621, 2002.

[2] P. Konkola, C. Chen, R.K. Heilmann, C. Joo, J. Montoya, C.-H. Chang, and M.L. Schattenburg, "Nanometer-level repeatable metrology using the Nanoruler," *Journal of Vacuum Science Technology B*, vol. 21, pp. 3097-3101, 2003.

[3] J. Montoya, C.-H. Chang, R.K. Heilmann, and M.L. Schattenburg, "Doppler writing and linewidth control for scanning beam interference lithography," *Journal of Vacuum Science Technology B*, vol. 23, pp. 2640-2645 (2005).

[4] Y. Zhao, C.-H. Chang, R.K. Heilmann, and M.L. Schattenburg, "Phase control in multiexposure spatial frequency multiplication," *Journal of Vacuum Science Technology B*, vol. 25, pp. 2439-2443, 2007.

[5] C.-H. Chang, R.K. Heilmann, M.L. Schattenburg, and P. Glenn, "Design of a double-pass shear mode acousto-optical modulator," *Review of Scientific Instruments*, vol. 79, pp. 033104:1-5, 2008.

Immersion-Achromatic-Interference Lithography for Sub-100 nm-Period Structures

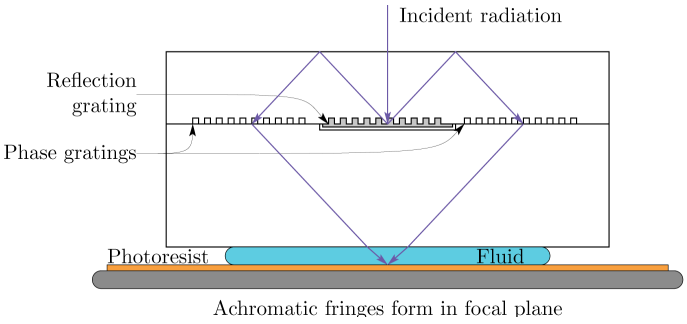
T.B. O'Reilly, H.I. Smith

Sponsorship: Singapore-MIT Alliance, Lincoln Laboratory

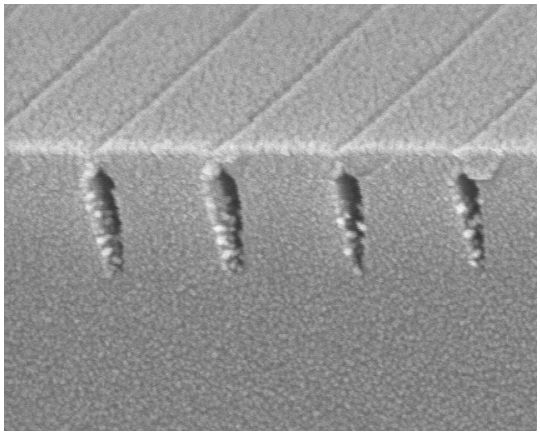
Interference lithography (IL) is a means of using the coherent interference of light to produce periodic patterns. The spatial period, *P*, produced is dependent on the interference angle θ, wavelength of light, λ, and the refractive index of the incident medium, *n*, and is given by: $P = \lambda / 2n\sin(\theta)$. Reducing the period of the pattern is most commonly accomplished by reducing λ or increasing θ. As the interference angle cannot exceed 90°, and the selection of suitable short-wavelength sources is limited, reduction of *P* below λ/2 requires the use of an immersion fluid to reduce the effective wavelength of the light.

We are presently developing an immersion achromatic interference lithography system to extend our capability to produce fine-period patterns. The system being developed is similar to the lab's existing achromatic IL system, which produces 100 nm-period gratings, in that the new immersion system will use diffraction gratings to split and recombine 193 nm light from an ArF excimer laser. The addition of an immersion fluid, initially water, will allow the system to write patterns with periods of 70 nm. Use of higher index fluids will make it possible to write even finer patterns. Development of fabrication processes for the gratings is currently underway.

Gratings and grids produced with this tool will likely find applications similar to those produced by the existing AIL system, which includes templates for self assembly and gratings for atom-interferometry. The system could also be used to test materials including photoresists and immersion fluids at periods smaller than are possible with other lithography systems.



▲ Figure 1: Schematic diagram of immersion achromatic IL system under development. Light from an excimer laser enters vertically at the top of the interferometer and is diffracted by a reflection grating. The light reflects off the top of the interferometer where a pair of transmission gratings diffract the light back toward the focal plane where it exposes a photosensitive substrate.



▲ Figure 2: Transmission grating fabricated in glass with a period of 266 nm. The geometry of the grating must be carefully controlled to get reasonable diffraction efficiency into the desired orders, which presents a fabrication challenge.

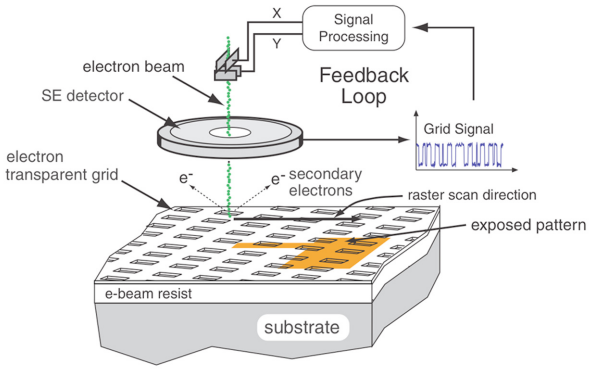
Spatial-phase-locked Electron-beam Lithography

E.E. Moon, H.I. Smith, J.T. Hastings (U. Kentucky)
Sponsorship: NSF

Our research in spatial-phase-locked electron-beam lithography (SPLEBL) is conducted in collaboration with the University of Kentucky. It is aimed at reducing pattern-placement errors in electron-beam-lithography systems to the sub-1 nm level. Such high precision is essential for certain applications in photonics and nanoscale science and engineering. SPLEBL is currently the only approach capable of achieving such pattern-placement accuracy. As shown in Figure 1, SPLEBL uses a periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid placed directly on the substrate, to continuously track the position of the beam while patterns are being written. Any deviation of the beam from its intended location on the substrate is sensed, and corrections are fed back to the beam-control electronics to cancel beam-position errors. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate.

The research effort at MIT is now focused on developing the materials and processes for producing the fiducial grid, with the objectives of: maximizing the signal-to-noise of the secondary-electron signal derived from the grid; minimizing electron scattering from the grid, which would be deleterious to precision lithography; maximizing the area and absolute accuracy of the grid; and minimizing the cost and inconvenience of producing the grid on substrates of interest. We have determined that signal levels are maximized when the grid is formed from nanoparticles. Substrates have been patterned with in-situ Faraday cups to make accurate measurements of signal-to-noise for a wide variety of nanoparticle types. To minimize electron scattering, the nanoparticles must be composed of low-atomic-number materials. Fullerenes may be the optimal nanoparticle, but achieving uniform thickness of layers and attaching the fullerenes along the grid lines represents a challenge of attachment chemistry. Scanning-beam interference lithography will be used to produce master grids. A special form of imprint lithography that maintains long-range spatial-phase coherence and conformal contact will be used to transfer attachment-chemistry grid patterns onto substrates of interest.

The research effort at the University of Kentucky is focused on processing of the signal from the grid. Specifically, new approaches are being developed that enable spatial-phase locking while e-beam writing in a vector-scan mode. Previous approaches utilized only the raster-scan mode.



▲ Figure 1: Schematic of the global-fiducial-grid mode of spatial-phase-locked electron-beam lithography. The periodic signal detected from the fiducial grid, which includes both X and Y components, is used to measure placement error, and a correction signal is fed back to the beam deflection system.

References

[1] J.T. Hastings, F. Zhang, and H.I. Smith, "Nanometer-level stitching in raster-scanning e-beam lithography using spatial-phase locking," *Journal of Vacuum Science and Technology B*, vol. 21, no. 6, pp. 2650-2656, Nov/Dec 2003.

[2] F. Zhang, H.I. Smith and J.F. Dai, "Fabrication of high-secondary-electron-yield grids for spatial-phase-locked electron-beam lithography," *Journal of Vacuum Science and Technology B*, vol. 23, no. 6, pp. 3061-3064, Nov/Dec 2005.

Optimum Exposure Parameters for High-resolution Scanning Electron-beam Lithography

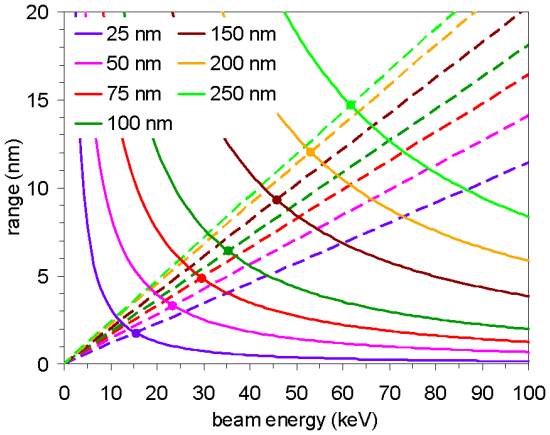
B. Cord, J. Yang, K.K. Berggren

Sponsorship: NRI, King Abdulaziz City for Science and Technology and Alfaisal University, MIT

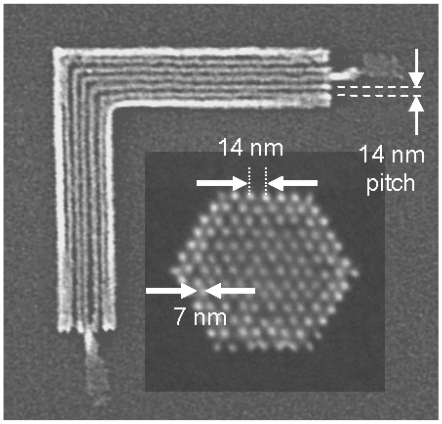
The resolution of a scanning electron-beam lithography (SEBL) exposure process is primarily limited by two processes: (1) the range of forward scattering of the incident beam and (2) the range of secondary electrons produced by interactions between the primary beam and the resist [1, 2]. The forward-scattering behavior has been well-characterized, and its extent is known to be proportional to the resist thickness and inversely proportional to the primary beam energy [3]. The behavior of the secondary electrons is less well-documented, but their approximate range is thought to be independent of resist thickness and either independent of [2] or weakly proportional to [4] the primary beam energy.

The dependencies of these two limiting factors suggest that, for a given resist thickness, there exists a "crossover" energy at which the process is balanced between the forward-scattering- and secondary-electron-limited regimes and any further increase in the beam energy results in no increased resolution. While it has been hypothesized that secondary-electron range is the main resolution limiter in most thin-resist applications [1], the energies at which forward scattering becomes irrelevant have never been determined.

Using Monte Carlo simulations [5], we have calculated both the forward-scattering length and average secondary electron range over a range of beam energies and resist thicknesses (see Figure 1). The results suggest that, for resists thinner than 100 nm, the crossover beam energy occurs at approximately 30-40 keV, suggesting in turn that thin-resist lithographic resolution on relatively low-cost 30 keV SEBL tools may be equal or superior to that attainable on high-end, high-beam-energy systems. This hypothesis is partially supported by the micrographs in Figure 2, which demonstrate sub-10-nm lithographic resolution in 35-nm-thick films of HSQ [6] using MIT's 30 keV Raith-150 SEBL tool.



▲ Figure 1: Curve fits of Monte Carlo results for the forward-scattering length α (solid lines) and the secondary electron range λ (dashed lines) as a function of beam energy for various resist thicknesses. The crossover points, indicating the beam energy at which the resolution is maximized, are marked with dots.



▲ Figure 2: A 7-nm-wide nested "L" and dot (inset) features on a 14-nm-pitch, exposed in 35 nm of HSQ at 30 keV using the Raith-150 SEBL tool at MIT.

References

[1] A.N. Broers, "Resolution limits for electron-beam lithography," *IBM Journal of Research and Development*, vol. 32, no. 4, pp. 502-513, 1988.

[2] D.C. Joy, "The spatial resolution limit of electron lithography," *Microelectronic Engineering*, vol. 1, no. 2, pp. 103-119, Oct. 1983.

[3] R.J. Hawryluk, "Exposure and development models used in electron beam lithography," *Journal of Vacuum Science and Technology*, vol. 19, no. 1, pp. 1-17, May 1981.

[4] M. Bolorizadeh and D.C. Joy, "Effects of fast secondary electrons to low-voltage electron beam lithography," *Journal of Micro/Nanolithography, MEMS and MOEMS*, vol. 6, no. 2, pp. 023004:1-7, Apr.-June 2007.

[5] P. Hovington, D. Drouin, and R. Gauvin, "CASINO: A new Monte Carlo code in C language for electron beam interaction - Part I: Description of the program," *Scanning*, vol. 19, no. 1, pp. 1-14, 1997.

[6] J.K.W. Yang and K.K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2025-2029, Nov. 2007.

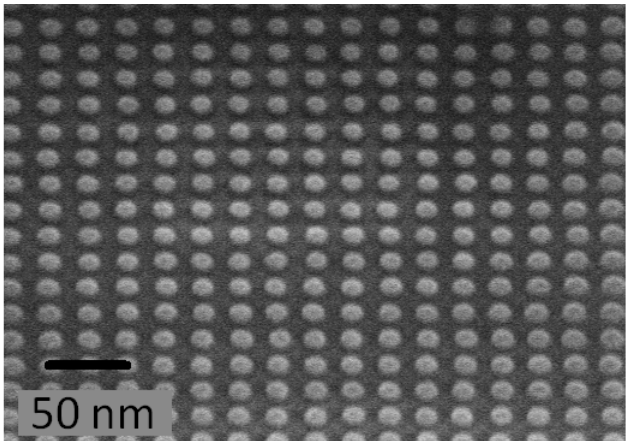
High-resolution Nanoimprint Lithography

D. Morecroft, J.K.W. Yang, K.K. Berggren
Sponsorship: Quantum Nanostructures and Nanofabrication Group, RLE, MIT

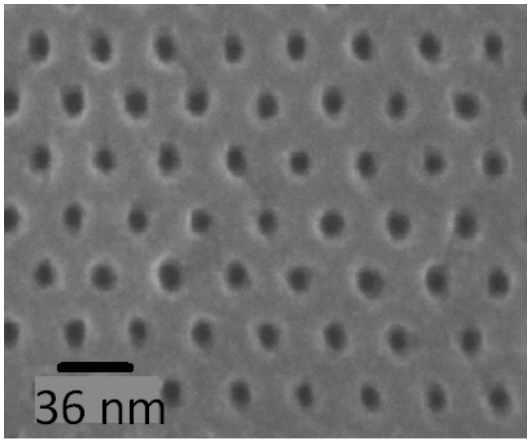
Nanoimprint lithography (NIL) is quickly maturing as a next-generation patterning technique that offers the combined advantages of high resolution, low cost and high throughput [1]. Unlike conventional optical lithography techniques, NIL physically imprints a 3D-structured mold into resist. The mold imprints the inverse pattern, which can then be transferred into the substrate by reactive-ion etching. While nanoimprint lithography is attractive as a low-cost high-throughput technique, the fabrication of its imprint mold still depends on other lithography methods. A key issue to resolve is the ultimate pitch resolution of the patterns since this factor determines the upper limit of the density. In this work we combine the high-resolution capabilities of electron-beam lithography with the high throughput of nanoimprint to obtain densely packed nanostructures over a large surface area.

Previously results have shown that negative tone resist can be used in combination with a salty developer technique to enhance contrast [2]. With this technique, hydrogen silsesquioxane (HSQ) resist was spun onto silicon substrate with a thickness of 20 nm, and electron-beam lithography was carried out using a Raith 150 EBL tool with a 30-kV acceleration voltage. The patterns were developed in an aqueous solution of 1% NaOH, 4% NaCl, and pattern transfer into the silicon was carried out using reactive-ion etching in a Plasma Therm 770 with a HBr plasma. Figure 1 shows a tilted scanning electron micrograph of 25-nm-pitch square-packed dots after reactive ion etching with a depth profile of 35 nm. The results show good profile transfer between the HSQ and silicon. The patterned silicon substrate was then used as a mold for nanoimprint lithography, and Figure 2 shows a 36-nm-pitch hexagonal dot array successfully transferred into the nanoimprint resist.

There are many potential applications for this patterning process, for example nanopatterned electrodes for fuel cells and batteries, where the increased surface area may enhance the catalytic activity.



▲ Figure 1: Tilted scanning micrograph of 25-nm-pitch pillars after reactive-ion etching with a hydrogen bromide plasma into the silicon substrate.



▲ Figure 2: Scanning electron micrograph of 36-nm-pitch dots imprinted into nanoimprint resist with 4-nm Ti for imaging.

References

[1] S.Y. Chou, P.R. Krauss, and P.J. Renstrom, "Imprint lithography with 25-nm resolution," *Science*, vol. 272, pp. 85–87, Apr. 1996.

[2] J.K.W. Yang and K.K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2025-2029, Nov. 2007.

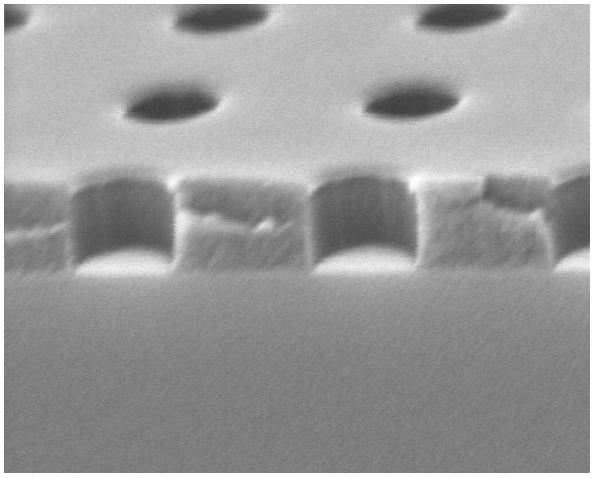
Fabrication of Inverted-Pyramid Arrays in Si for Templated Self Assembly

T. Savas, T.B. O'Reilly, H.I. Smith
Sponsorship: Singapore-MIT Alliance

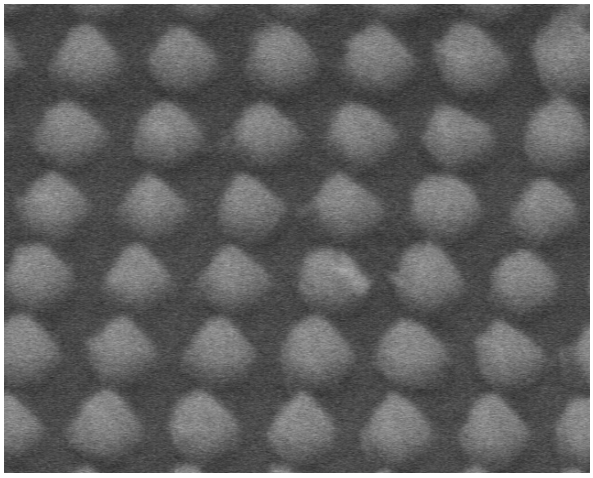
Recently, in support of the Singapore-MIT Alliance, the lab's interference-lithography (IL) was used to fabricate two types of patterned substrates for use in research on templated self-assembly.

The first set of substrates was fabricated to support research on the interaction of materials with inverted pyramids etched into silicon. The fabrication begins by depositing a thin layer of SiO_2 on a (100) silicon wafer. A tri-layer resist stack is deposited on the substrate, and the resist is patterned by interference lithography, in this case using the Lloyd's mirror IL system. Following development of the exposed resist, the pattern is transferred to the substrate using reactive-ion-etching, forming a grid of holes in the SiO_2 layer. The Si substrate is then etched in KOH, which preferentially etches into the <100> direction much faster than into the <111> direction, resulting in the formation of inverted-pyramids where each of the holes in the SiO_2 was located. Various materials can then be deposited or grown on the patterned substrate to determine how the surface patterning affects the material response.

A second set of substrates was fabricated for use in experiments on nanoporous aluminum oxide, which is formed by oxidizing aluminum under certain conditions. The process leads to the formation of many nanoscale pores perpendicular to the surface which generally have some characteristic spacing, but no long-range order. To provide long-range order in the pattern of pores, a silicon-rich silicon-nitride membrane was patterned using interference lithography. Reactive-ion-etching and liftoff were used to form an array of chromium cones on the membrane. By pressing the membrane into an aluminum surface with air-pressure on the backside the cones could be used to form small dents in the surface to determine if that would affect the location of the pores that would form when the aluminum was later oxidized.



▲ Figure 1: Micrograph of a stage in the preparation of a substrate containing an array of inverted-pyarmids, for use in research on templated self-assembly. A pattern consisting of a grid of holes, with a spatial period of 200 nm, was written using interference lithography and has been transferred to the substrate by reactive ion etching. Due to differences in the etch rates of different crystal planes, etching this substrate in KOH will form inverted pyramids in the silicon substrate.



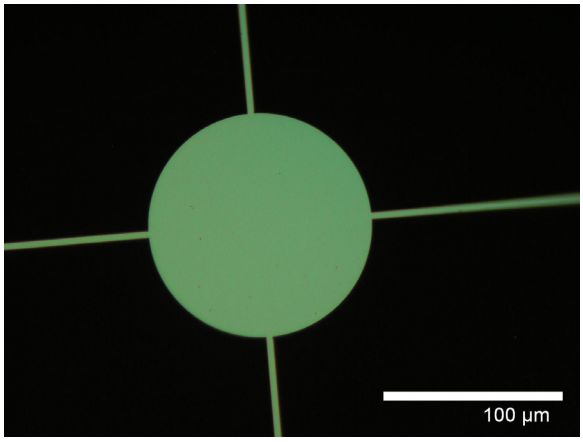
▲ Figure 2: Micrograph showing a 200 nm-period grid of chrome cones on a silicon-nitride membrane. The pattern was created by interference lithography, and the cones were formed by a combination of etching and liftoff. These cones were formed for use in indenting an aluminum surface to control the positions of the pores in nanoporous aluminum oxide.

Fabrication of Suspended Discs in Si_3N_4 Membranes for Observation of the Poisson Spot with Deuterium

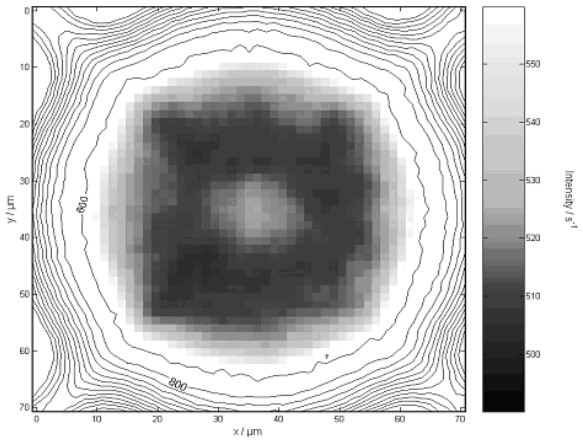
A.A. Patel, T. Reisinger (Univ. Graz, Austria), B. Holst (Univ. Graz, Austria), H.I. Smith
Sponsorship: Univ. Graz, Austria, internal funds

The observation of a bright central spot in the shadow of an opaque circular object, the so-called Poisson Spot, was an historically important experiment establishing the wave nature of light. The same interference phenomenon should occur with material particles. To conduct an experiment to observe the Poisson Spot with monochromatic deuterium molecules, we fabricated free-standing discs of silicon nitride, shown in Figure 1.

The discs had a diameter of 100 µm and a thickness of 500 nm, centered within a 400 µm-diameter window and supported by four 3µm-wide support bars. The key parameters for the disc include thickness, ellipticity and edge roughness. Scanning-electron-beam lithography was used to pattern the area of the disc and the support bars on a Si_3N_4 membrane. PMMA was used as the electron-beam resist, and the pattern was transferred to a chromium hardmask via a wet etch. The area of the disc and in between the support bars was etched away using reactive ion etching. Figure 1 shows a final device in Si_3N_4. Figure 2 shows the observation of the Poisson Spot through experiments run by our colleagues at the University of Graz in Austria.



▲ Figure 1: Optical micrograph of the most recently fabricated free-standing disc. (There is no material in the dark regions.) The disc obstruction is 100 µm in diameter and about 500 nm thick. SEM metrology showed that edge roughness was under 50 nm.



▲ Figure 2: Deuterium Poisson Spot. Shown is the first Poisson Spot realized with molecules. The central part of the shadow is amplified as a grey image plot. The image is the sum of 24 images recorded consecutively at a sampling distance of 321 mm.

Reference

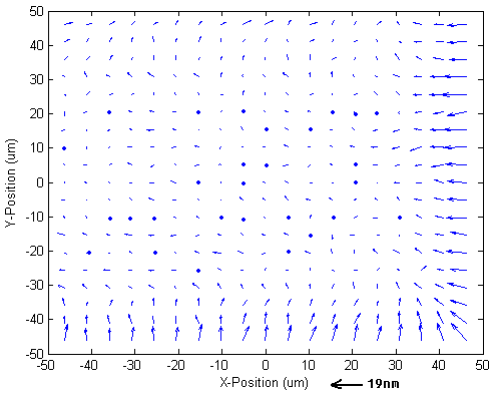
[1] T. Reisinger, G. Bracco, S. Rehbein, S. Schmahl, W. E. Ernst, B. Holst, "Direct Images of the Virtual Source in a Supersonic Expansion," *Journal of Physical Chemistry* vol. A76, pp. 12620-12628, 2007.

Correction of Intrafield Distortion in Scanning-Electron-Beam Lithography and Confirmation via Optical Ring-Resonator Filters

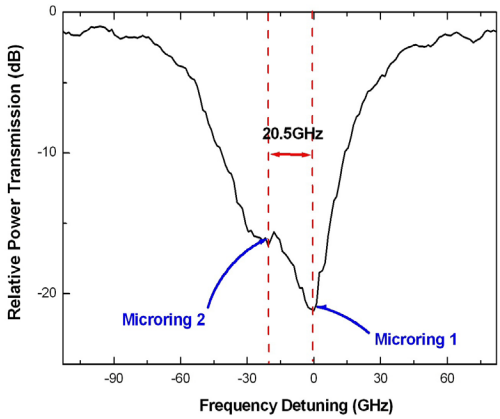
J. Sun, C.W. Holzwarth, J.T. Hastings (U. Kentucky), H.I. Smith
Sponsorship: DARPA

In scanning-electron-beam lithography (SEBL), distortion in the electron-beam deflection field (i.e., intrafield distortion) leads to systematic pattern-placement errors. These are particularly detrimental to photonic devices, which depend on coherent interference. Intrafield distortion arises from imperfections in the electron optics, and errors in the digital-to-analog conversion and field-calibration electronics. The intrafield distortion of our Raith 150 SEBL system was measured by comparing a written grid to a precision reference grid, generated by interference lithography. Figure 1 is a map of the Raith's intrafield distortion for a 100μm field.

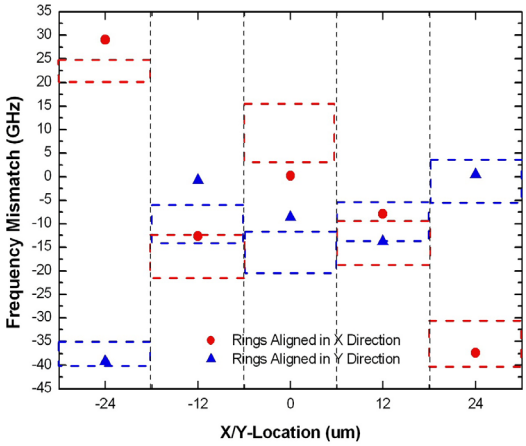
Optical microring-resonator filters in high-index-contrast materials, such as Si or Si_3N_4, require 1-nm-level pattern-placement precision. In fabricating such devices with SEBL, intrafield distortion is manifested in the deviation of resonant frequency from design values. Figure 2 shows a typical transmission spectrum of a 2nd-order microring-resonator filter in which the resonant frequencies of the two rings are shifted by 20.5 GHz. Based on the measured distortion map, we calculated the expected resonant-frequency mismatch as a function of position and orientation in the SEBL exposure field. Figure 3 shows the results, with the boxes enclosing experimental resonant-frequency shifts. The near agreement between our model and experiments confirms the earlier measurement of intrafield distortion. Given this correlation of intrafield distortion with frequency mismatch, we will be able to correct the mismatch by feeding appropriate corrections to the beam-deflection electronics.



▲ Figure 1: Map of the Raith 150's intrafield distortion in a 100μm deflection Field. The maximum distortion is 19 nm, which is in the lower left corner of the field.



▲ Figure 2: A typical through-port spectrum of a 2nd-order microring filter, with 20.5 GHz frequency mismatch caused by the intrafield distortion.



▲ Figure 3: Frequency mismatch of 2nd-order microring resonators. The red dots represent two rings aligned in the X direction, while the blue triangles represent alignment in the Y direction. The boxes with corresponding colors enclose measured frequency mismatches.

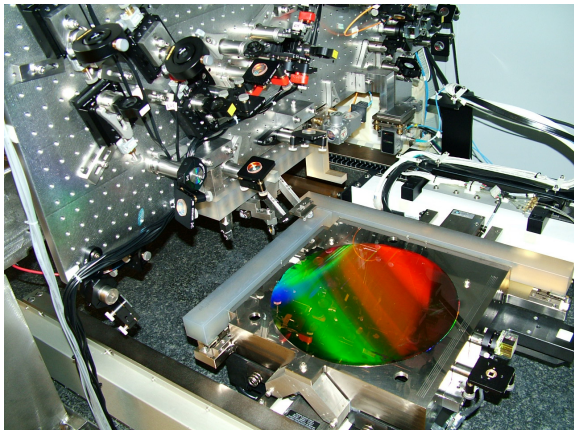
Nanometrology

R. Heilmann, Y. Zhao, D. Trumper, M.L. Schattenburg
Sponsorship: NSF

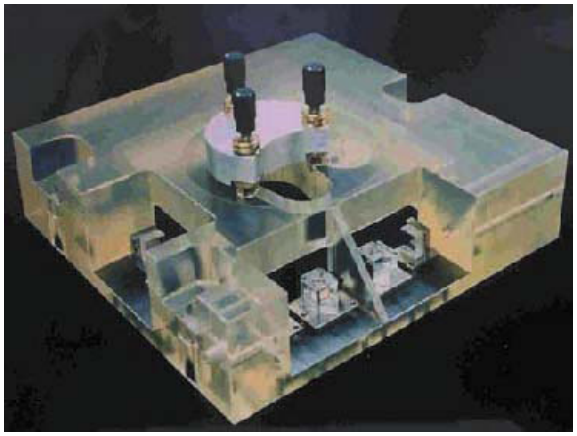
Manufacturing of future nanodevices and systems will require accurate means to pattern, assemble, image and measure nanostructures. Unfortunately, the current state-of-the-art of dimensional metrology, based on the laser interferometer, is grossly inadequate for these tasks. While it is true that when used in carefully-controlled conditions interferometers can be very precise, they typically have an accuracy measured in microns rather than nanometers. Achieving high accuracy requires extraordinarily tight control of the environment and thus high cost. Manufacturing at the nanoscale will require new technology for dimensional metrology that enables sub-1-nm precision and accuracy in realistic factory environments.

A recently formed MIT-UNC–Charlotte team is developing new metrology technology based on large-area grating patterns that have long-range spatial-phase coherence and ultra-high accuracy. Our goal is to reduce errors in gratings by 10-100 times over the best available today. These improved gratings can be used to replace interferometers with positional encoders to measure stage motion in a new nanomanufacturing tools and to calibrate the dimensional scales of existing nanofabrication tools. This increased precision and accuracy will enable the manufacturing of nanodevices and systems that are impossible to produce today. Improved dimensional accuracy at the nano-to-picometer scale will have a large impact in many nanotechnology disciplines including semiconductor manufacturing, integrated optics, precision machine tools, and space research.

As part of this effort, we will utilize a unique and powerful tool recently developed at MIT called the Nanoruler that can rapidly pattern large gratings with a precision well beyond other methods. Another unique high-precision tool, the UNCC-MIT-built Sub-Atomic Measuring Machine (SAMM), is being brought to bear to research new ways to quantify and reduce errors in the gratings. Recent work at MIT focuses on improving the thermal controls in the Nanoruler lithography enclosure and developing an improved interferometer system to reduce errors in the stage metrology frame. At UNCC the SAMM is undergoing extensive refurbishment and improvements designed to boost accuracy of the interferometer.



▲ Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.



▲ Figure 2: Photograph of reference block/sample holder for the Sub-Atomic Measuring Machine at the University of North Carolina – Charlotte.

References

[1] P. Konkola, C. Chen, R.K. Heilmann, C. Joo, J. Montoya, C.-H. Chang, and M.L. Schattenburg, "Nanometer-level repeatable metrology using the Nanoruler," *Journal of Vacuum Science Technology B*, vol. 21, pp. 3097-3101, 2003.

[2] R.K. Heilmann, C.G. Chen, P.T. Konkola, and M.L. Schattenburg, "Dimensional metrology for nanometer-scale science and engineering: Towards sub-nanometer accurate encoders," *Nanotechnology*, vol. 15, pp. S504-S511, 2004.

[3] J. Montoya, R.K. Heilmann, and M.L. Schattenburg, "Measuring two-axis stage mirror non-flatness using linear/angular interferometers," *Proc. of the 19th Annual Meeting of the American Society for Precision Engineering*, 2004, vol. 34, pp. 382-385.

[4] Y. Zhao, D.L. Trumper, R.K. Heilmann and M.L. Schattenburg, "Optimization and temperature mapping of an ultra-high thermal stability environmental enclosure," *Journal of Precision Engineering*, 2007, to be published.

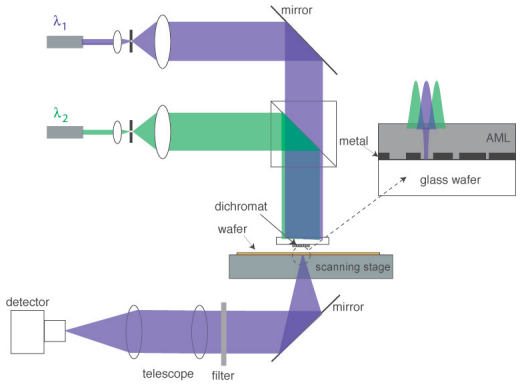
Microscopy Beyond the Diffraction Limit Using Absorbance Modulation

H.Y. Tsai, R. Menon, H.I. Smith

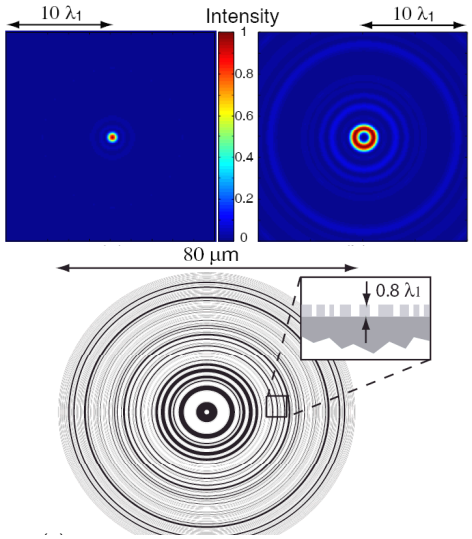
Sponsorship: Deshpande Center for Technological Innovation

Absorbance Modulation Imaging (AMI) is an approach to overcome the optical diffraction limit in the far–field, thereby achieving macro-molecular resolution with photons. Preliminary experiments show promising results that agree well with theoretical predictions [1].

AMI relies on an absorbance-modulation layer (AML), composed of photochromic molecules. Illumination at one wavelength, λ_2, renders the AML opaque, while illumination at a shorter wavelength, λ_1, renders it transparent. When illuminated with a ring-shaped spot at λ_2 co-incident with a focused spot at λ_1, the dynamic competition results in a nanoscale aperture, through which λ_1 can penetrate to the substrate beneath. The size of the aperture is limited only by the photo-kinetic parameters of the AML, and the intensity ratio of the two illuminating wavelengths, not the absolute intensities [2]. By scanning this dynamic nanoscale aperture over the sample, resolution beyond the far-field diffraction limit is achieved. A related technique was demonstrated in stimulated-emission-depletion (STED) fluorescence microscopy [3]. However, while STED requires high power pulsed illumination and fluorescent markers, AMI can operate at low illumination intensity. A schematic of an AMI microscope is shown in Figure 1. Collimated lights at λ_1 and λ_2 illuminate the *dichromat*, a binary phase element, which creates a ring-shaped spot at λ_2 and a round spot at λ_1. Figure 2 shows the phase transmission function of a dichromat and the intensity distributions in its focal plane for the two wavelengths.



▲ Figure 1: Schematic of absorbance-modulation imaging (AMI) microscope. The ring illumination at λ2 creates a local subwavelength aperture for λ1 in the AML through which the underlying object is illuminated and the scattered light collected. Multiple dichromats generate separate signals enabling parallelism and enhanced throughput. The inset shows the schematic of a resolution test structure consisting of metal lines on a glass wafer.



▲ Figure 2: Output light intensity distributions at (a) λ1 = 400nm, (b) λ2 = 532nm, and (c) the phase transmission function of the dichromat. The phase step in this case is 0.8λ1 as shown in the inset of (c). The dichromat creates ring-shaped illumination for λ2 and a focal spot for λ1.

References

[1] R. Menon, H-Y Tsai, and S.W. Thomas III, "Far-field generation of localized light fields using absorbance modulation," *Physical Review Letters*, vol. 98, no. 4, pp. 043905, Jan. 2007.

[2] R. Menon and H.I. Smith, "Absorbance modulation optical lithography," *Journal of the Optical Society of America A*, vol. 23, no. 9, pp. 2290-2294, Sept. 2006.

[3] S.W. Hell and J. Wichmann, "Breaking the diffraction resolution limit by stimulated emission: Stimulated-emission-depletion fluorescence microscopy," *Optics Letters*, vol.19, no. 11, pp. 780-782, June 1994.

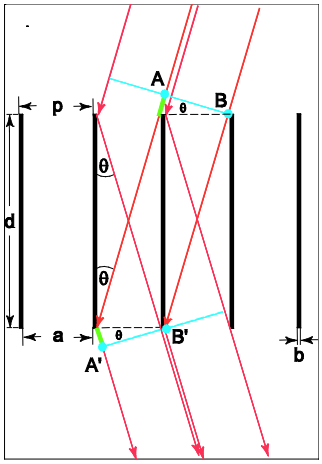
Nanofabricated Reflection and Transmission Gratings

M. Ahn, C.-H. Chang, R.K. Heilmann, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA

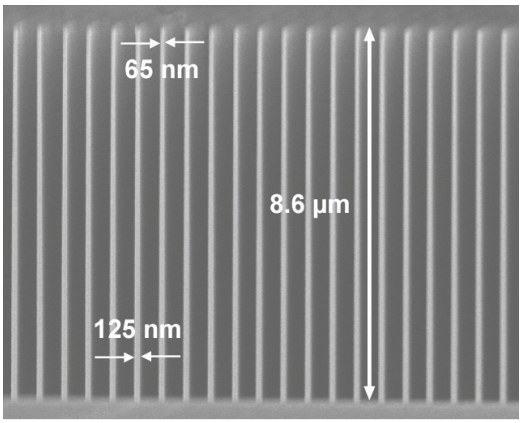
Diffraction gratings and other periodic patterns have long been important tools in research and manufacturing. Diffraction is due to the coherent superposition of waves—a phenomenon with many useful properties and applications. Waves of many types can be diffracted, including visible and ultraviolet light, x-rays, electrons, and even atom beams. Periodic patterns have many useful applications in fields such as optics and spectroscopy; filtering of beams and media; metrology; high-power lasers; optical communications; semiconductor manufacturing; and nanotechnology research in nanophotonics, nanomagnetics, and nanobiology.

Diffraction gratings can be divided into reflection gratings, which use diffracted waves on the same side as the incident waves, and transmission gratings, which use waves that are transmitted through the grating. Both have their strength and weaknesses, depending on the application. A long-standing problem with transmission gratings is the strong absorption of extreme-ultraviolet (EUV) and soft x-ray photons upon transmission, and thus a low diffraction efficiency in this important wavelength band. We have recently solved this problem with the invention and fabrication of critical-angle transmission (CAT) gratings. This new design for the first time combines the high broadband efficiency of blazed grazing-incidence reflection gratings [1] with the superior alignment and figure tolerances, and the low weight of transmission gratings [2]. CAT gratings consist of ultrahigh aspect ratio, nm-thin freestanding grating bars with sub-nm smooth sidewalls that serve as efficient mirrors for photons incident at graze angles below the angle for total external reflection (see Figures 1 and 2). Most photons are not absorbed since they propagate only through vacuum. Blazing can concentrate diffracted power into a single or a few desired diffraction orders. Blazing also enables the use of higher diffraction orders and leads to manifold increases in spectral and spatial resolution in spectrometer or focusing applications, respectively.

Fabrication of these challenging structures is described in [3]. X-ray tests on a 574-nm-period prototype have shown outstanding > 50% and > 30% on-blaze diffraction efficiency in the 17-49-nm- and 2.75–10.6-nm-wavelength bands, respectively. Shorter period gratings will provide higher efficiency at shorter wavelengths.



▲ Figure 1: Schematic of the CAT grating principle. Diffraction peaks appear where the path length difference AA'-BB' equals an integer multiple of the wavelength.



▲ Figure 2: Scanning electron micrograph of a cleaved cross section through a 574-nm-period silicon CAT grating that was (intentionally) not etched all the way through. The grating bar aspect ratio is close to 100 and is increased to ~ 150 for the final grating.

References

[1] J.F. Seely, L.I. Goray, B. Kjornrattanawanich, J.M. Laming, G.E. Holland, K.A. Flanagan, R.K. Heilmann, C.-H. Chang, M.L. Schattenburg, and A.P. Rasmussen, "Efficiency of a grazing-incidence off-plane grating in the soft x-ray region," *Applied Optics*, vol. 45, no. 8, pp. 1680-1687, Mar. 2006.

[2] K. Flanagan, M. Ahn, J. Davis, R.K. Heilmann, D. Huenemoerder, A. Levine, H. Marshall, G. Prigozhin, A. Rasmussen, G. Ricker, M.L. Schattenburg, N. Schulz, and Y. Zhao, "Spectrometer concept and design for x-ray astronomy using a blazed transmission grating," *Proc. SPIE*, vol. 6688, 66880Y, pp. 1-12, Sept. 2007.

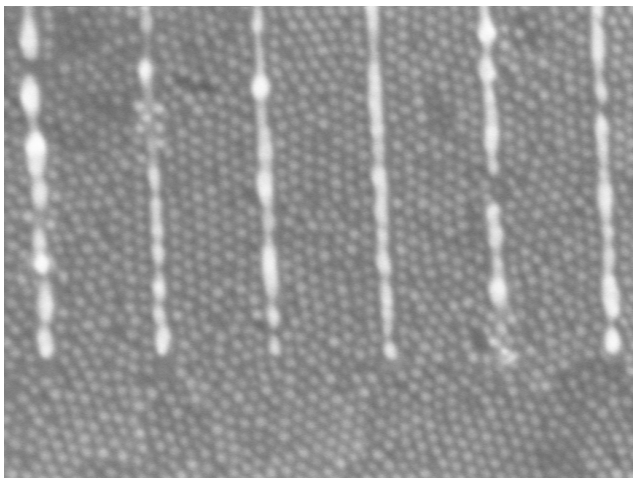
[3] M. Ahn, R.K. Heilmann, and M.L. Schattenburg, "Fabrication of ultrahigh aspect ratio freestanding gratings on silicon-on-insulator wafers," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6 , pp. 2593-2597, Nov. 2007.

Templated Self-Assembly of Sub-10-nm Quantum Dots

J. Leu, B. Cord, P. Anikeeva, J. Halpert, M. Bawendi, V. Bulović, K.K. Berggren
Sponsorship: SRC/FCRP MSD, NRI, IBM

Patterned templates can guide the self-assembly of nanoparticles into ordered arrays [1]. Our motivation in pursuing templated self-assembly is to develop a robust method for the creation of ordered structures at length scales below ten nanometers. The basic process entails creating surface relief templates via electron-beam lithography and spin-coating a suspension of colloidal nanoparticles onto the template. As the solvent evaporates, the quantum dots self-assemble primarily through the capillary forces created by the dewetting of the template [2].

We demonstrated this technique at sub-10-nm-length scales by spin-coating a solution of organically-capped CdZnS semiconducting quantum dots onto nanopatterned grating structures on silicon substrates. We observed the geometric confinement of the quantum dots via physical templating and capillary forces into well-ordered monolayer aggregates with defined lattice orientations. While recent research has demonstrated the ability to self-assemble sub-10-nm metallic nanoparticles via capillary forces into physical templates of similar size [2], this work is unique in the demonstration of lattice orientation control via physical templating at sub-10-nm-length scales.



▲ Figure 1: Scanning electron micrograph of a self-assembled quantum dot monolayer on a templated silicon substrate. The vertical lines visible are part of a template grating, with 10-nm-wide, Au lines with height varying from 20-80 nm at a pitch of 80 nm. The spheres are organically capped 8-nm CdZnS semiconducting quantum dots.

References

[1] Y. Yin, Y. Lu, B. Gates, and Y. Xia, "Template-assisted self-assembly: A practical route to complex aggregates of mondispersed colloids with well-defined sizes, shapes, and structures," *Journal of the American Chemical Society*, vol. 123, pp. 8718-8729, 2001.

[2] J.A. Liddle, Y. Cui, and P. Alivisatos, "Lithographically directed self-assembly of nanostructures," *Journal of Vacuum Science and Technology B*, vol. 22, no. 6, pp. 3409-3414, Nov./Dec. 2004.

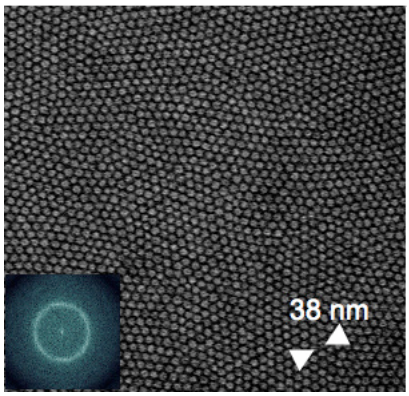
Hydrogen Silsesquioxane Nano-posts as Decoys for Guiding the Self-assembly of Block Copolymers

J.K.W. Yang, Y.S. Jung, I. Bita, E.L. Thomas, C.A. Ross, K.K. Berggren
Sponsorship: MIT

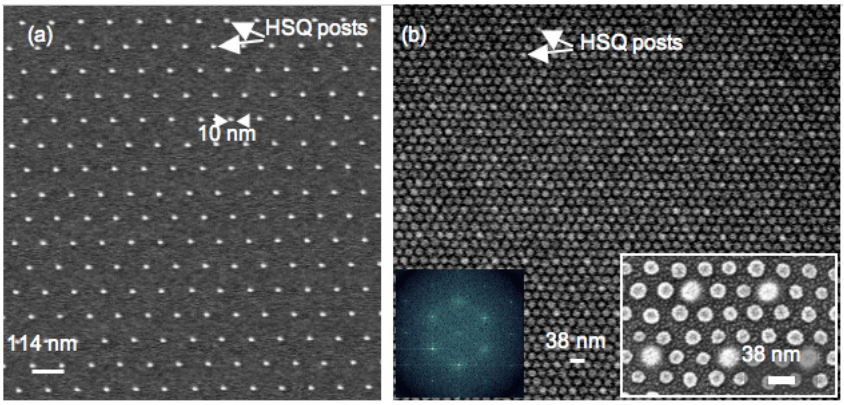
According to the International Technology Roadmap for Semiconductors, semiconductor companies are expected to produce memory cells with a half-pitch of 22 nm by the year 2011. Fabricating such small structures is a huge challenge even with today's most advanced photolithography methods. However, the technology for making sub-20-nm nanostructures is already available in the self-assembly of block-copolymers (BCP). This bottom-up technique is scalable to even smaller dimensions by choosing tinier BCP molecules, making it an attractive "next-generation lithography" method for creating dense periodic structures over large areas. Major challenges still remain in (1) the accurate control of the order and position of the nanostructures, and (2) the formation of arbitrary structures using BCPs. In this work, we focus on solving the first problem.

Figure 1 shows the randomly oriented, hexagonally-packed nanostructures formed in a BCP film on a flat Si substrate. This pattern was formed after annealing a thin layer of polystyrene-b-polydimethylsiloxane (PS-b-PDMS) BCP and selective etching of the PS majority block [2]. These nanostructures that lack order have limited use as most applications such as bit-patterned media require long-range order. To induce long-range order in the BCP, we first introduced topography on the flat surface by fabricating a periodic array of posts in hydrogen silsesquioxane (HSQ) resist by electron-beam lithography (see Figure 2a). These posts, ~10 nm in diameter and 35 nm tall, acted as decoys (or substitutes) for single BCP spheres. Figure 2b shows that order and orientation control were achieved when the BCP self-assembled about the array of posts. In contrast to previous work [1] where the topographical structures (e.g., trenches) used for guiding the BCP were large and clearly identifiable after processing, our nano-posts blend in among the BCP spheres while physically pinning down the BCP lattice position in 2D. As a result, the template of posts allows efficient use of the surface area of the substrate.

Adjusting the lattice spacing of the HSQ posts produced formation of different BCP packing orientations that were commensurate with the HSQ lattice. We therefore have control over the packing order and orientation of the BCP spheres. The resultant PDMS and HSQ nanostructures were etch-resistant and could be used for pattern transfer into underlying functional materials such as magnetic films for high-density data storage applications.



▲ Figure 1: SEM image of randomly oriented spheres formed by BCP self-assembly on a flat surface. The Fourier transform (inset) shows a circular halo characteristic of randomly oriented grains.



▲ Figure 2: (a) SEM image of a periodic array of 35-nm-tall, 10-nm-diameter HSQ posts fabricated by electron-beam lithography and developed in a high-contrast salty developer [3]. b) Ordered packing of BCP spheres guided by the lattice of HSQ posts. HSQ posts blend in with the BCP spheres but are visible as slightly brighter dots in the image and bottom-right inset. The Fourier transform (left inset) shows an arrangement of bright spots characteristic of a hexagonally packed crystal.

References

[1] J.Y. Cheng, A.M. Mayes, and C.A. Ross, "Nanostructure engineering by templated self-assembly of block copolymers," *Nature Materials*, vol. 3, no, 11, pp. 823-828, Nov. 2004.

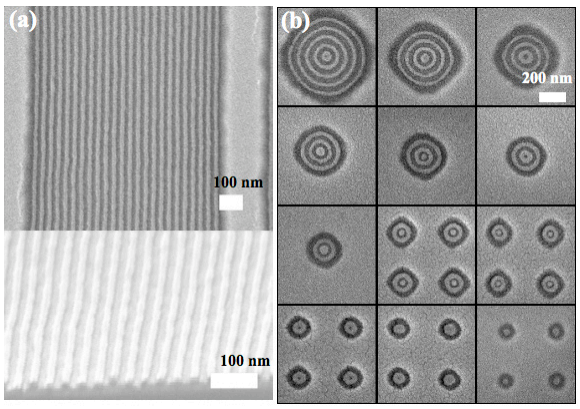
[2] Y.S. Jung and C.A. Ross, "Orientation-controlled self-assembled nanolithography using a polystyrene-polydimethylsiloxane block copolymer," *Nano Letters*, vol. 7, no. 7, pp. 2046-2050, July 2007.

[3] J.K.W. Yang and K.K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science & Technology B*, vol. 25, no. 6, pp. 2025-2029, Nov. 2007.

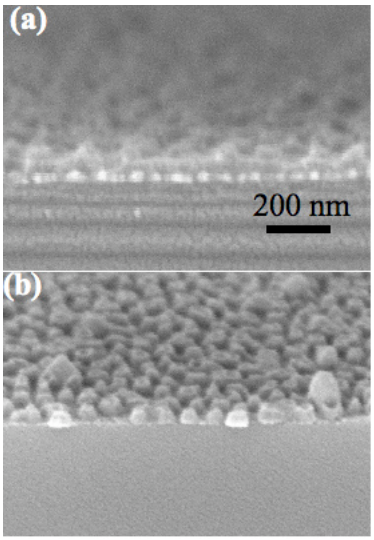
Templated Self-assembly of Block Copolymers for Nanolithography

C.A. Ross, H.I. Smith, K.K. Berggren, E.L. Thomas, F. Ilievski, V. Chuang, Y.S. Jung
Sponsorship: NSF, CMSE, Singapore-MIT Alliance, SRC

Self-organized macromolecular materials can provide an alternative pathway to conventional lithography for the fabrication of devices on the nanometer scale. In particular, the self-assembly of the microdomains of diblock copolymers within lithographically-defined templates to create patterns with long-range order has attracted considerable attention, with the advantages of cost-effectiveness, large area coverage, and compatibility with pre-established top-down patterning technologies. Block copolymers consist of two covalently bound polymer chains of chemically distinct polymer materials. The chains can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction [1]. On the one hand, with the purpose of fabricating arrays of magnetic nanosized dots, which are a potential candidate for magnetic hard-drive media, we are working on templating the block copolymers in a removable template. Previously, sphere-forming polystyrene-b-ferrocenyldimethylsilane (PS-PFS) diblock copolymers were successfully aligned in 2-D [2] or 3-D [3] templates. On the other hand, cylindrical morphology of block copolymers can be used for defining nanoscale line patterns, as demonstrated in Figure 1a. Poly(styrene-b-dimethylsiloxane) (PS-PDMS) diblock copolymers have a large interaction parameter and a high etch contrast between two blocks, which are desirable for long-range ordering and pattern-transfer into functional materials [4]. Concentric ring patterns can also be obtained by using circular templates, as shown in Figure 1b. Beyond rather limited morphologies of diblock copolymers, an appropriate combination of block sequence, interaction parameter of the adjacent blocks, volume fraction, and molecular weights of ABC triblock polymer thin films provides a diversity of new structures. For example, core-shell structured triblock terpolymer can be obtained by designing the block sequence and volume fraction of the blocks. Figure 2 presents vertically oriented high-density nanorings from PB-PS-PMMA polymers after the selective removal of PB and PMMA and after pattern-transfer onto a SiO_2 film.



▲ Figure 1: (a) Line patterns from PS-PDMS diblock copolymers under linear confinement and (b) concentric ring patterns under circular confinement



▲ Figure 2: (a) Vertically oriented hollow cylinders of PS from PB-PS-PMMA triblock copolymers. (b) RIngs after CHF_3 RIE for patterning a SiO_2 film.

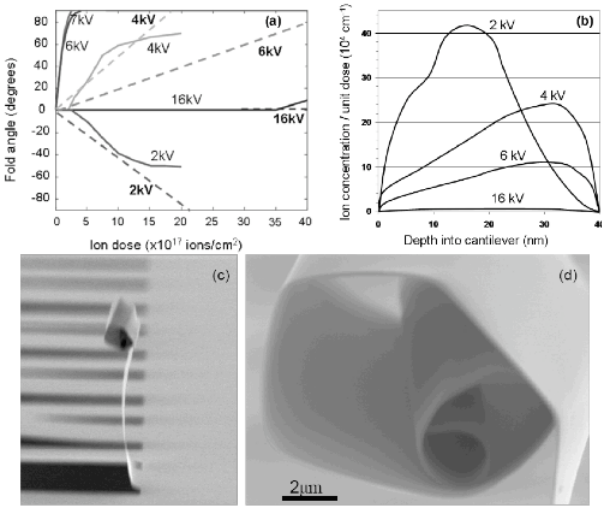
References

[1] E.L. Thomas and R.L. Lescanec, "Phase morphology in block copolymer systems," *Philosophical Transactions of the Royal Society A,* vol. 348, pp. 146-164, 1994.
[2] J. Cheng, C.A. Ross, and A. Mayes, "Nanostructure engineering by templated self-assembly," *Nature Materials*, vol. 3, pp. 823-828, 2004.
[3] V.P. Chuang, J.Y. Cheng, T.A. Savas, and C.A. Ross, "Three-dimensional self-assembly of spherical block copolymer domains into V-shaped grooves," *Nano Letters*, vol. 6, pp. 2332-2337, 2006.
[4] Y.S. Jung and C.A. Ross, "Orientation-controlled self-assembled nanolithography using a polystyrene-polydimethylsiloxane block copolymer," *Nano Letters*, vol. 7, no. 7, pp. 2046-2050, June 2007.

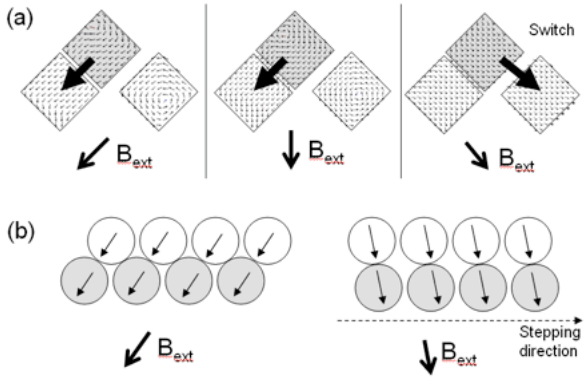
Building Three-dimensional Nanostructures via Membrane Folding

W.J. Arora, A.J. Nichol, G. Barbastathis, H.I. Smith
Sponsorship: ISN, NSF Graduate Research Fellowships

In Nanostructured Origami[1] thin membranes are patterned in 2D and are then automatically folded in sequence to produce a 3D configuration. We have developed methods of both folding actuation and folded-structure alignment for patterned silicon-nitride membranes. We have demonstrated that ion implantation can be used to fold membranes. Figure 1 shows data from membranes implanted with high doses of helium. The implanted ions create stress, forcing the membrane to bend. A minimum bend radius of 1 μm using 100 nm-thick silicon nitride was achieved. The resulting 3D structure remains folded unless heated above 400C, at which point the helium diffuses out and the structure unfolds. In addition to experimental demonstration, we model the physics of the ion implantation to show that the ion-implant profile correlates to the observed folding. This is most clearly evidenced by the fact that membranes given low energy (shallow depth) implants fold downwards while membranes given high energy (large depth) implants fold upwards. Magnetic forces are an alternate actuation method to fold, and to align and reconfigure nanopatterned membranes.[2] After folding, the membranes accurately self-align when brought into close proximity due to the interactive magnetic force between the arrays of nanomagnets. Since the self-alignment accuracy is better than the lithographic resolution, the membranes may be self-aligned to nanometer precision. We are also developing a nanomagnetic stepper that utilizes the force between arrays of nanomagnets to precisely move a nanopatterned membrane along a substrate. After folding and magnetically aligning two membranes, the system is actuated by an external magnetic field that rotates or flips the magnetization of the nanomagnets, thus changing the equilibrium position. Figure 2a shows a micromagnetic simulation of a bi-stable switcher that changes between two positions by rotating the external field. Figure 2b shows a schematic of the nanomagnet switcher, which uses circular nanomagnets that shift one step per full rotation of the external magnetic field. The stepper is wirelessly controlled and is non-hysteretic so the need for feedback is eliminated. We are exploring the stepper's use for reconfigurable photonic systems and wireless nano-device control.



▲ Figure 1: a) Fold angle vs dose for different 40-nm-thick silicon nitride cantilevers implanted with helium (solid lines are experimental; dashed lines are prediction. b) Corresponding ion profiles within the cantilever. c, d) Experimental demonstration of folding.



▲ Figure 2: (a) Micromagnetic model of a nanomagnetic switcher. (b) schematic of a nanomagnet stepper motor that moves one period with each full rotation of the external magnetic field.

References

[1] H.J. In, W.J. Arora, T. Buchner, S.M. Jurga, H.I. Smith, and G. Barbastathis. *2004 4th IEEE Conference on Nanotechnology (IEEE Cat. No.04TH8757)*, 2004, p 358-60 JVSTB:

[2] A.J. Nichol, Paul S. Stellman, W.J. Arora, George Barbastathis. "Two-step magnetic self-alignment of folded membranes for 3D nanomanufacturing." Accepted: *Journal of Microelectronics Engineering*, Dec. 2006.

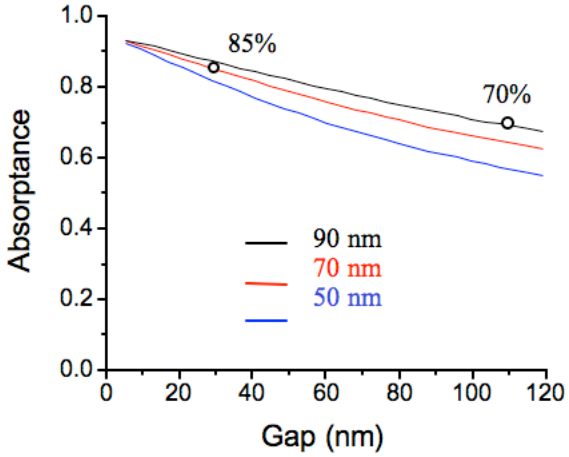
Fabrication of Superconducting Nanowire Single-photon Detectors with High Fill-factors

J.K.W. Yang, A.J. Kerman, V. Anant, E.A. Dauler, K.K. Berggren
Sponsorship: AFOSR, MIT

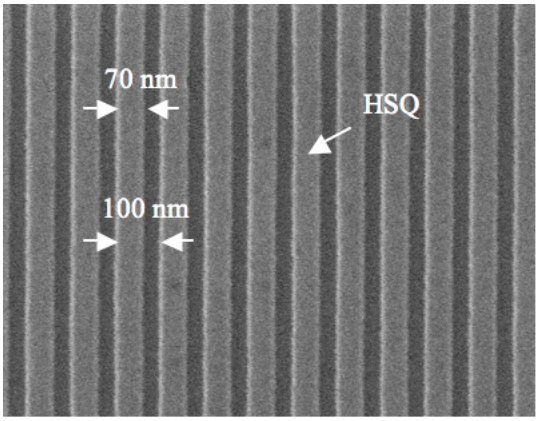
In the past, we have fabricated superconducting nanowire single-photon detectors (SNSPDs) with detection efficiencies (DE) as high as 57% at 1550-nm wavelengths [1]. The nanowires in these SNSPDs were 90 nm wide and were separated by 110 nm (i.e., a 45% fill factor) in a meander structure patterned in NbN films. While a 57 % DE is acceptable for many applications, a much higher DE will be valuable (if not necessary) in certain applications such as linear-optics quantum computing and photon number resolution. One approach to increasing the DE of SNSPDs is to increase the optical absorption of the device by increasing the fill factor of the meander structure.

Figure 1 shows numerical calculations of the absorptance in the SNSPD meander structure, indicating that reducing the gap width between wires in the meander can significantly increase photon absorptance and hence the DE. For example, we can predict that by increasing the fill factor from the current value of 45% to 70%, we would increase the device DE from 57% to ~70%.

Recently we developed a high-resolution nanofabrication method using a combination of a high-contrast resist process and electron-beam lithography to achieve sub-10-nm nanostructure dimensions [2]. This technique could be used to fabricate SNSPDs with fill factors as high as 80 % and wire widths as narrow as 40 nm. Figure 2 shows an example of a grating structure with 70% fill factor that has been fabricated in HSQ resist using this method.



▲ Figure 1: Numerical calculations show that the photon absorptance in the SNSPD meander increases with decreasing gap width between the nanowires. Our original SNSPD design of 90-nm-wide wire with a 110-nm-wide gap has an absorptance of ~70%. However, increasing the fill factor through better lithography to achieve 70-nm-wide wires and a gap width of 30 nm will result in an increase in absorptance to 85%, leading to higher detection efficiencies.



▲ Figure 2: Top-down SEM image of HSQ structures on Si with a fill factor of 70%, which could potentially be used for making SNSPDs with higher DE.

References

[1] K.M. Rosfjord, J.K.W. Yang, E.A. Dauler, A.J. Kerman, V. Anant, B.M. Voronov, G.N. Gol'tsman, and K.K. Berggren, "Nanowire single-photon detector with an integrated optical cavity and anti-reflection coating," *Optics Express*, vol. 14, no. 2, pp. 527-534, Jan. 2006.

[2] J.K.W. Yang and K.K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science & Technology B*, vol. 25, no. 6, pp. 2025-2028, Nov. 2007.

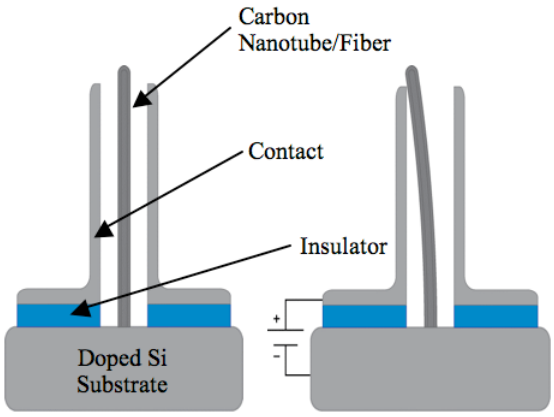
Carbon Nano-Switches for Low-leakage Circuit Applications

K.M. Milaninia, C.E. Schmitt, A.I. Akinwande, M.A. Baldo, A.P. Chandrakasan
Sponsorship: SRC/FCRP IFC, DARPA

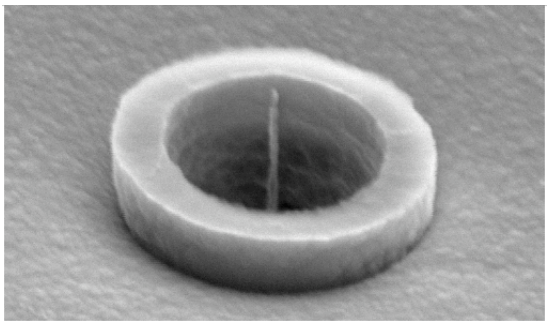
Nanoelectromechanical switches (NEMS) exhibit minimal leakage current in the off state. Consequently, they may find application in low-power electronics. This work focuses on the fabrication of a vertically oriented nano-switch using a carbon fiber or nanotube as the active component. Figure 1 shows the device schematic, and Figure 2 shows an SEM image of the self-aligned fabrication process used to create the nano-switch [1]. The device consists of a carbon nanotube/fiber grown directly on a highly doped silicon substrate between two contacts that are electrically isolated from the substrate by an insulator. The device is actuated when a voltage is applied between the substrate and one of the contacts. This voltage causes the nanotube to be pulled into and eventually make physical contact with one of the contacts, which allows current to flow between the substrate and the contact.

One of the primary benefits of the nano-switch is that it has extremely low leakage current because a physical gap separates the nanotube from the contact during the off state. One possible application that takes advantage of the reduced leakage is power-gating idle circuit blocks. The nano-switch is connected as a header switch between the power supply and the load circuit. During normal operation, the nano-switch acts as a short circuit and power is supplied to the load circuit. When the circuit is not in use, the nano-switch is opened and the supply voltage is disconnected to reduce power consumption. This technique is similar to power-gating with a high threshold CMOS device, but the nano-switch provides extra power savings because it has even less leakage current.

A test chip has been designed to quantify the power savings of the nano-switch for this power-gating application. The chip also implements proof-of-concept SRAM and reconfigurable interconnect circuits that explore other potential benefits of the nano-switch.



▲ Figure 1: Left) Schematic of a vertically oriented carbon nano-switch. Right) Carbon nano-switch upon actuation using an applied voltage between the substrate (i.e., tube) and a contact.



▲ Figure 2: An SEM image of a carbon nano-based field-emitter produced by the self-aligned fabrication process [1].

Reference

[1] L.-Y. Chen, L.-F. Velasquez-Garcia, X. Wang, K. Teo, and A.-I. Akinwande, "A micro ionizer for portable mass spectrometers using double-gated isolated vertically aligned carbon nanofiber arrays," *International Electron Devices Meeting*, pp. 843-846, Dec. 2007.

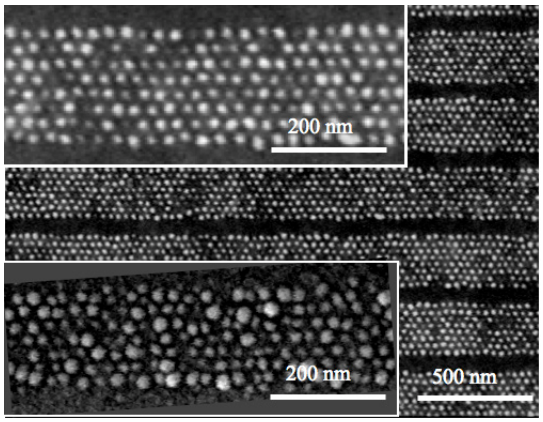
Magnetic Nanostructures for Data Storage

Y. Oh, M. Ciria, D. Navas, F. Ilievski, V.P. Chuang, C.A. Ross
Sponsorship: Fulbright Fellowship, NSF

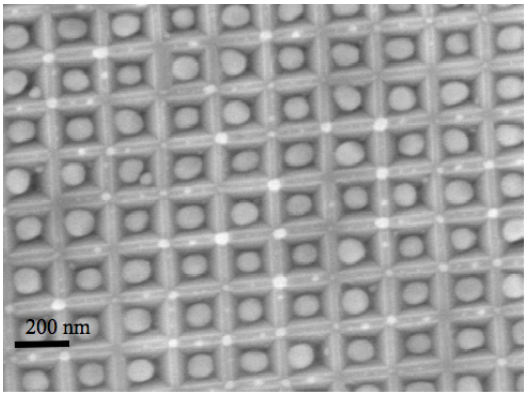
We are investigating the fabrication and magnetic properties of various types of magnetic nanostructures made using non-conventional lithography and self-assembly processes, for applications in patterned magnetic recording media and other data storage devices. In one set of experiments, we use block copolymer lithography to pattern arrays of magnetic "dots" with perpendicular anisotropy [1]. The dots form arrays with periodicity of 30 – 50 nm and the magnetization of each dot can point up or down, to represent one bit of data. By investigating the thermally activated reversal process, we can show that the dots switch independently and coherently, which is desirable for a patterned recording medium. The block copolymer can be templated using surface relief to create arrays with long range order (Figure 1).

We have also examined the formation of periodic arrays of Co nanoparticles by the templated dewetting of a Co film deposited over a substrate with inverted pyramidal pits etched into it. The dewetting, achieved by a high temperature anneal, produces a uniform array of Co particles (Figure 2) with an f.c.c. crystal structure and consequently low magnetic anisotropy. This process is now being explored for other magnetic alloys. Another self-assembly process that can be used to form magnetic arrays is the use of anodic alumina films, which are created from aluminum metal by anodization, and which contain ordered arrays of pores that can be used as templates to form arrays of magnetic nanowires [2].

Finally, we have investigated the magnetic properties of narrow lines patterned from a single-crystal epitaxial Cu/Ni/Cu film using interference lithography. The Ni film is highly strained, and as a result it develops a magnetization perpendicular to the film plane. Patterning the film relieves stress and leads to stripes with an in-plane magnetization that is perpendicular to the stripe length – an unusual magnetization orientation.



▲ Figure 1: Top inset and background: Scanning electron micrographs of an array of W dots on a CoCrPt perpendicular-anisotropy film. The W dots were made using a block copolymer that had been ordered into rows using a removable topographic template. Bottom inset: An array of magnetic dots formed by using the W dots as an etch mask for patterning the CoCrPt with Ne ion-beam etching.



▲ Figure 2: Array of Co nanoparticles formed within 200-nm-period pits etched in a silicon substrate. The 15-nm as-deposited film was dewetted by annealing at 850° C in a reducing atmosphere.

References

[1] F. Ilievski, C.A. Ross, and G.J. Vancso, "Magnetic reversal phenomena of perpendicular magnetic islands fabricated by block copolymer lithography," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07C520:1-3, Apr. 2008.

[2] D. Navas, K.R. Pirota, P. Mendoza Zelis, D. Velazquez, C.A. Ross, and M. Vazquez, "Effects of the magnetoelastic anisotropy in Ni nanowire arrays," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07D523:1-3, Apr. 2008.

Organic Floating-gate Memory Devices

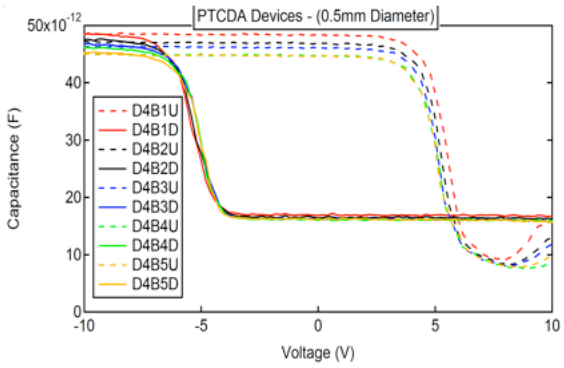
H. Abdu, S. Paydavosi, O.M. Nayfeh, D.A. Antoniadis, V. Bulović
Sponsorship: SRC/FCRP MSD

Conventional non-volatile flash memories face obstacles to continued scaling, such as the inability to use thinner tunneling oxides and poor charge retention due to defects in the tunneling oxide [1]. A possible solution is to replace the continuous floating gate, where the charge is stored, with a segmented charge storage film, so that defects in the structure would affect only a few of the many segments that comprise the floating gate [2]. From our earlier work on nanocrystal thin films as floating gates, we established the need for the smallest possible segmented structures, which led us to the use of organic films as floating gates in non-volatile flash memories. As an example, a single organic molecule of 3,4,9,10 –parylene tetracarboxylic dianhydride (PTCDA) occupies 1 nm² in area and is capable of storing and retaining a single charge. A thin film of PTCDA molecules would therefore provide 10^{14} distinct charge storage sites per cm², a remarkably high number of storage sites, even when we take into account the fact that only a few percent of these would be occupied when the floating gate is charged. If a defect were present in the tunneling oxide below the floating gate, only a few discreet molecules of PTCDA would be affected due to poor lateral conduction between PTCDA molecules. We can, therefore, project that such a molecular thin film of PTCDA is likely to meet the demanding size and packing density requirements of the advancing flash memory technology.

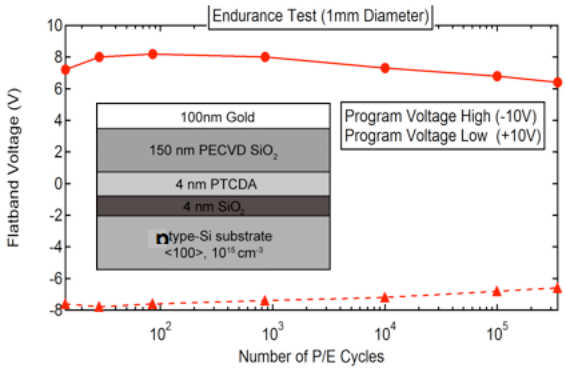
To demonstrate charge retention in an organic thin film, we construct an organic floating gate capacitor, shown in Figure 2 (inset), by depositing 4 nm of PTCDA as the floating gate. As for the gate dielectric, SiO_2 was deposited using Plasma Enhanced CVD (PECVD), which allowed for low temperature oxidation and minimal damage to the organic film below. This capacitor structure is a first step to demonstrating a floating-gate memory cell, as it proves significant in understanding the organic molecular film's ability to be written (charged), erased (discharged), and read (retain charge).

Figure 1 demonstrates the functionality of the organic floating gate capacitor. The capacitance voltage (C-V) plot exhibits hysteresis, which indicates the flatband voltage shift that exists due to charge storage. Also, as Figure 2 shows, the device performs well in endurance tests, withstanding over 300,000 program/erase cycles without much deterioration in the flatband voltage shift.

This initial set of data signifies the potential for organic floating-gate memories as an advancement of flash memory devices. With the scaling enabled by the nano-segmented molecular floating gate, this technology has the potential to achieve **higher memory density,** decreased **power consumption, and increased read/write/erase** speeds, all of which are important benchmarks for future non-volatile memory devices [3].



▲ Figure 1: C-V plot of several organic floating-gate capacitors with characteristic hysteresis. Electron charging at -10V and hole charging at +10V.



▲ Figure 2: Schematic diagram of an organic floating-gate capacitor (subset). Endurance test demonstrating over 300,000 program/erase cycles without significant loss in device performance.

References

[1] K. Kinam, "Technology for sub-50nm DRAM and NAND flash manufacturing," *International Electronic Devices Meeting*, 1609340, pp. 323-326, Dec. 2005.

[2] O. Nayfeh, D. Antoniadis, K. Mantey, and M. Nayfeh, "Memory effects in metal-oxide-semiconductor capacitors incorporating dispensed highly monodisperse 1-nm silicon nanoparticles," *Applied Physics Letters*, vol. 90, p. 153105, 2007.

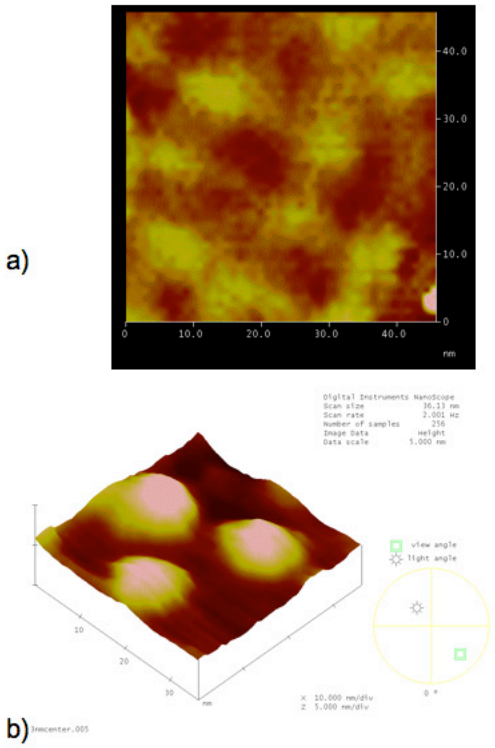
[3] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells--an overview," *Proc. IEEE*, vol. 85, no. 8, Aug. 2007, pp. 1248-1271.

Uniform Delivery of Si Nanoparticles on Device-quality Substrates for Nonvolatile Memory Applications Using Spin-coating from Isopropyl Alcohol Colloids

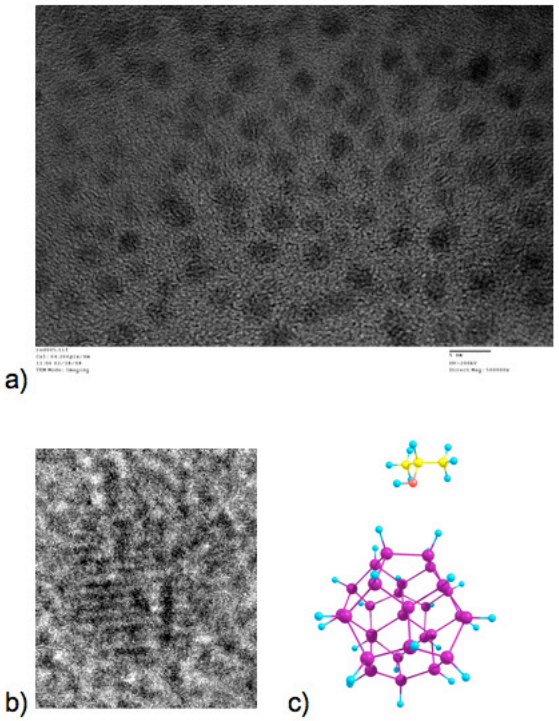
O.M. Nayfeh, D.A. Antoniadis, K. Mantey, M.H. Nayfeh

Sponsorship: SRC/FCRP MSD, Singapore-MIT Alliance, Intel Fellowship

Colloidal dispersions of as-prepared hydrogen-terminated silicon nanoparticles of predominately 2.9 nm in diameter in isopropyl alcohol are spin-coated directly on device-quality thermally grown silicon-dioxide (SiO_2) layers across the entire 150-mm substrates. Atomic force microscopy (AFM) is used to image the nanoparticle distributions and low levels of agglomeration with some signs of nanoparticle ordering are observed. The AFM depth profiling of the nanoparticle size is in agreement with independent high-resolution transmission electron microscopy (HRTEM) measurements. Hartree Fock (HF)-based atomistic simulations confirm the possible formation of Si nanoparticle/isopropanol complexes with a calculated electrostatic binding energy of 30 meV, slightly larger than the room temperature thermal agitation energy. The much-reduced agglomeration can be explained in terms of such complexes that may regulate the inter-nanoparticle and nanoparticle–solvent interactions. The results are of importance for the fabrication of nonvolatile memory devices that use silicon nanoparticles for charge storage.



▲ Figure 1: a) Top-view AFM images of silicon nanoparticles in near-array formation on a device-quality thermally grown SiO2 layer. b) Surface-view AFM of silicon nanoparticles. The lateral dimension via AFM is limited by the tip-effect, but AFM resolves the vertical dimension correctly.



▲ Figure 2: a) High-resolution TEM images of predominately 2.9-nm silicon nanoparticles on a TEM grid showing minimal agglomeration. The size of the nanoparticles is in agreement with the vertical AFM measurements in Figure 1. b) Closeup of single silicon nanoparticle with lattice visible. c) Atomistic simulation structure of a silicon nanoparticle with isopropyl alcohol used for calculation of binding energy.

Reference

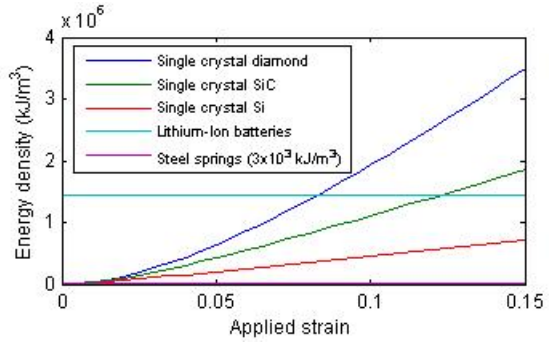
[1] O.M. Nayfeh, D.A. Antoniadis, K. Mantey, and M.H. Nayfeh, "Memory effects in metal-oxide-semiconductor capacitors incorporating dispensed highly monodisperse 1 nm silicon nanoparticles,"*Applied Physics Letters*, vol. 90, no. 15, pp. 153105:1-3, Apr. 2007.

Elastic Energy Storage in Carbon Nanotubes

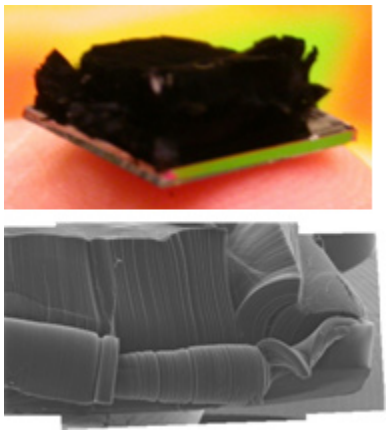
F.A. Hill, T.F. Havel, A.J. Hart, C. Livermore
Sponsorship: Deshpande Center for Technological Innovation, NSERC

The focus of this project is to study the potential of storing energy in the elastic deformation of carbon nanotubes (CNTs) as a step towards lightweight, high-density energy storage. The unique mechanical properties of CNTs, namely a high stiffness of 1 TPa, high strength, high flexibility, and low defect density, make springs made of CNTs a promising medium for elastic energy storage. Theoretical models have shown that CNTs can be stretched reversibly up to 15% [1], while lower strains of up to 6% have been reached experimentally to date [2, 3]. Our initial work has used models to predict the energy density that can be stored in CNTs under different modes of mechanical deformation. The obtainable energy density is predicted to be highest under tensile loading, with an energy density in the springs themselves about 1000 times greater than the maximum energy that can be stored in steel springs, and ten times greater than the energy density of lithium-ion batteries. Practical systems will have lower overall stored energy density once the mass and volume of the spring's supporting structure are taken into account, with a maximum achievable overall stored energy density predicted to be comparable to lithium-ion batteries (see Figure 1). Nonetheless, springs made of CNTs offer a number of advantages over conventional energy storage in electrochemical batteries. In addition to their competitive energy density, CNT springs are based on stretching chemical bonds rather than breaking and reforming chemical bonds, so an energy storage medium based on CNT springs has the potential to operate at higher power densities, under harsher conditions, to deeper discharge levels, and through a larger number of charge-discharge cycles without degradation. In addition, CNT springs have significant potential for storing mechanical energy to drive a mechanical load directly.

Our ongoing research focuses on demonstrating energy storage in CNT springs. While energy can be stored with high density in a single carbon nanotube, grouping individual carbon nanotubes into larger assemblies of densely-packed bundles and ropes offers the advantages of storing larger amounts of energy in a single spring and the ability to couple the resulting spring to a macroscopic load. The proposed springs are composed of well-ordered, aligned, densely-packed CNT groupings in order to ensure effective load transfer within the assembly. The starting material for the springs is CNT forests, highly-ordered, vertically aligned arrangements of millimeter length CNTs grown on a substrate (see Figure 2). The resulting springs will be loaded and characterized to investigate how energy density can be maximized using different spring formation techniques.



▲ Figure 1: Energy density of CNTs under tensile loading with different support structure materials compared to the energy density of conventional storage technologies.



▲ Figure 2: Dense arrays of CNTs in vertically aligned forests [4].

References

[1] M.R. Falvo, G.J. Clary, R.M. Taylor, V. Chi, F.P. Brooks, S. Washburn, and R. Superfine, "Bending and buckling of carbon nanotubes under large strain," *Nature*, vol. 389, no. 12, pp. 582-584, Oct. 1997.

[2] D.A. Walters, L.M. Ericson, M.J. Casavant, J. Liu, D.T. Colbert, K.A. Smith, and R.E. Smalley, "Elastic strain of freely suspended single-wall carbon nanotube ropes," *Applied Physics Letters*, vol. 74, no. 25, pp. 3803–3805, June 1999.

[3] M. Yu, B.S. Files, S. Arepalli, and R.S. Ruoff, "Tensile loading of ropes of single-wall carbon nanotubes and their mechanical properties," *Physical Review Letters*, vol. 84, no. 24, pp. 5552–5555, 2000.

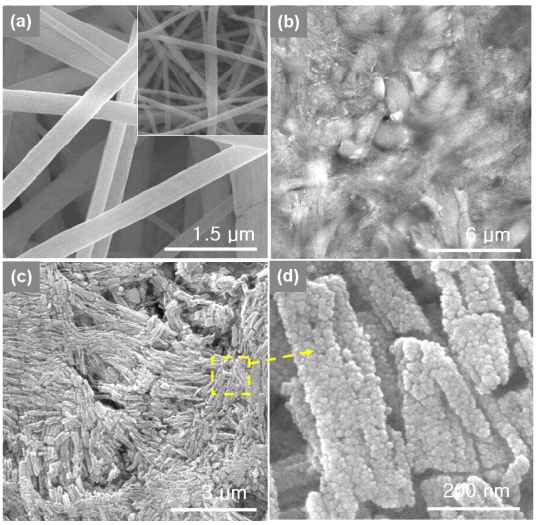
[4] A.J. Hart, L. Laake, and A.H. Slocum, "Desktop growth of carbon nanotube monoliths with in situ optical imaging," *Small*, vol. 3, no. 5, pp. 772-777, 2007.

Nanowire and Thin-film Gas Sensors

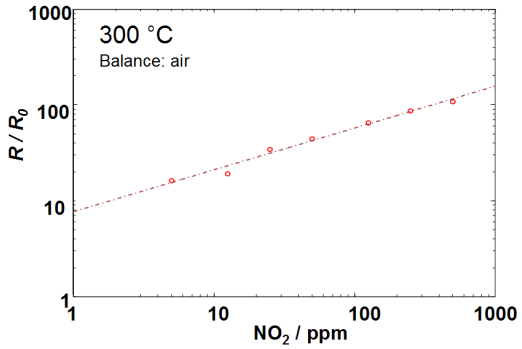
K. Sahner, G. Whitfield, Y.S. Jin, H.L. Tuller (in collaboration with I.D. Kim, KIST; A. Rothschild, Technion; J. Lewis, U. Illinois)
Sponsorship: NSF, US-Israel Binational Science Foundation

Gas sensors play a vital role in public health and safety, industrial process control, and in reduction of toxic emissions into the environment [1]. Conductometric gas sensors based on semiconducting metal oxide thin films are of high interest in many applications due to their high sensitivity, small size, and simplicity of measurement. Sensors based on individual nanowires further improve device sensitivity due to the increased area of the chemically active free surface. However, challenges arise due to limited process control and reproducibility during integration of nanowires with conventional microfabrication techniques.

Gas sensors based on interconnected nanowire networks enable improved sensitivity while avoiding typical challenges in integration. The TiO_2 and SnO_2 based nanowire meshes were deposited by collaborators at KIST and U. Illinois onto microfabricated interdigitated electrodes via electrospinning [2] and direct-write [3] techniques. Both techniques enable rapid integration of inorganic nanowire networks with microfabricated structures, via deposition from organic precursor solution (Figure 1). The structures were characterized at MIT over a range of temperatures and gas compositions to confirm high chemical sensitivity (Figure 2). Analytical and numerical models are being developed, to understand coupling between surface chemisorption and electronic properties. Thin-film-based gas sensors are being fabricated and studied in parallel, for comparison.



▲ Figure 1: SEM images of SnO_2 nanowires at various stages of the electrospinning process. (a) As-spun poly(vinyl acetate) / SnO_2 precursor. (b) After hot-pressing at 120°C. (c) After calcination at 450°C. (d) Magnified image, after calcination.



▲ Figure 2: Gas sensitivity of SnO_2 nanowire network, defined by resistance in presence of NO_2 (R) over resistance in dry air (R_0), illustrating 10-100x change in resistance for 10-1000 ppm concentration NO_2.

References

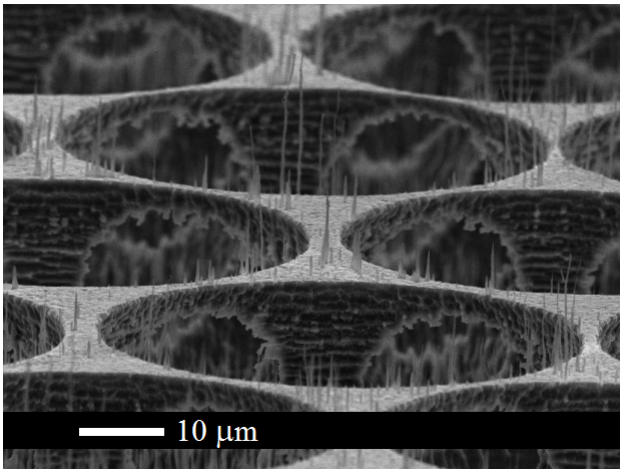
[1] F. Rock, N. Barsan, and U. Weimar, "Electronic nose: Current status and future trends," *Chemical Reviews*, vol. 108, pp. 705-725, Feb. 2008.
[2] I.D. Kim, A. Rothschild, T. Hyodo, and H.L. Tuller, "Microsphere templating as means of enhancing surface activity and gas sensitivity of $CaCu_3Ti_4O_{12}$ Thin Films," *Nano Letters*, vol. 6, no. 2, pp. 193-198, Feb. 2006.
[3] J.A. Lewis and G.M. Gratson, "Direct writing in three dimensions," *Materials Today*, vol. 7, no. 7-8, pp. 32-39, July-Aug. 2004.

CNT-Based Open Architecture Ionizer for Portable Mass Spectrometry

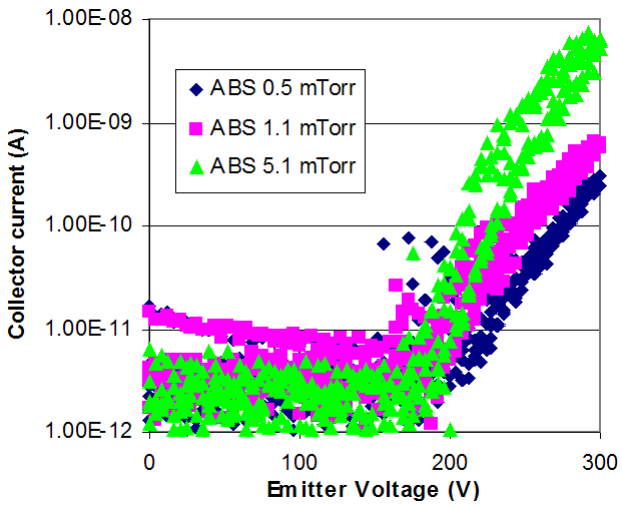
L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

Mass spectrometers need to ionize the sample that they are analyzing to determine its chemical composition. Traditional ionizers for gases use either chemical ionization (CI) or electron impact ionization (EII). In the latter case, electrons from thermionic sources produce ions by colliding with neutral molecules. More efficient carbon nanotube-based field-emitted electron impact ionizers have been developed [1]. However, one of the drawbacks of EII is that the sample is transformed into small fragmentation products. Several samples could have similar fragmentation spectra but be quite different compounds, with radically different properties. (For example, one substance can be a poisonous agent while another is a harmless material). Therefore, an approach to reduce the fragmentation products would improve the informational power of the mass spectrometer.

Field ionization soft-ionizes molecules, thus reducing the fragmentation products. The field ionization scheme creates ions by directly tunneling electrons from the outer shell of neutral molecules by virtue of a very high electric field [2]. The electric field is produced by high-aspect-ratio field enhancers and the application of a large (up to 1 kV) bias voltage. Carbon nanotubes (CNTs) are ideal field enhancers because of their high aspect ratio and their nanometer-sized tip radius. In the case of the EIIs, a closed architecture is implemented because it is intended to protect the field enhancers from back-streaming positive ions [3]. However, this protection is not needed in a field ionizer because in this case the field enhancers are biased at a positive voltage with respect to the gate. Also, an open architecture, where the field enhancers are accessible by the neutral molecules from all directions, is a more suitable approach to produce field ionization because it increases the ion current. We have implemented the emitting substrate of an open architecture single-gated field ionizer array [4]. The substrate is a micro-fabricated 3D foam-like silicon structure (μfoam). The μfoam is fabricated using deep reactive ion-etching (DRIE). On top of the μfoam, there is a sparse array of plasma-enhanced chemical-vapor-deposited (PECVD) CNTs (Figure 1) that act as field enhancers. The CNTs are sparsely grown to avoid field enhancer shadowing. The substrate has been tested with a triode setup. The data shows a startup ionization voltage as low as 175 V (Figure 2). Current research efforts focus on developing a gated version of the ionizer.



▲ Figure 1: Detail of sparse PECVD CNT cluster on the μfoam. The CNTs have 80-nm-diameter tips and are up to 14 μm tall.



▲ Figure 2: The IV characteristics of the field ionizer. The collector is a smooth ball of 2 mm diameter hovering about 4 mm above the gate. The collector was biased at –1100 V. The gate is biased at 0 V.

References

[1] L.-Y. Chen, "Double-gated field emission arrays," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.
[2] R. Gomer, *Field Emission and Field Ionization*, New York: American Institute of Physics, 1961, rpt. 1993.
[3] L. Dvorson, I. Kymissis, and A.I. Akinwande, "Double-gated silicon field emitters," *Journal of Vacuum Science and Technology B*, vol. 21, no. 1, pp. 486-494, Jan. 2003.
[4] L.F. Velásquez-García and A.I. Akinwande, "A PECVD CNT-based open architecture field ionizer for portable mass spectrometry," *Technical Digest 21st IEEE International Conference on Microelectromechanical Systems*, Tucson AZ, Jan. 2008, pp. 742-745.

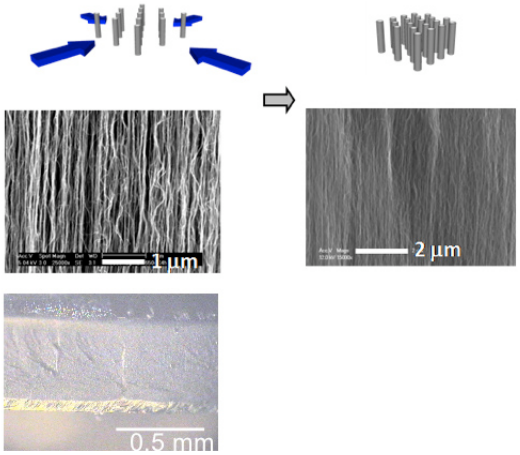
Aligned CNT-based Micro-structures and Nano-Engineered Composite Macro-structures

B.L. Wardle, R. Guzman de Villoria, N. Yamamoto, H. Cebeci, K. Ishiguro, S.A. Steiner III, S. Wicks, S. Figueredo, E.J. Garcia, A.J. Hart, H. Duong, D. Saito (in collaboration with A.H. Slocum)

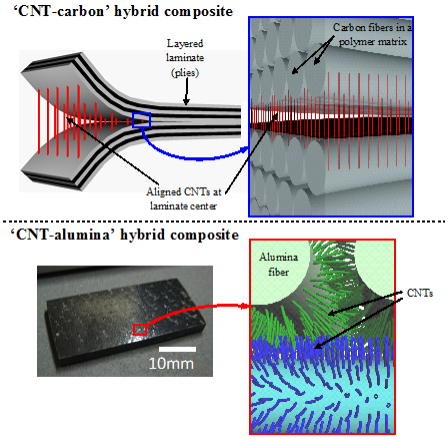
Sponsorship: NECST Consortium, NSF

Carbon nanotube (CNT) composites are promising new materials for structural applications thanks to their mechanical and multifunctional properties. We have undertaken a significant experimentally-based program to understand both micro-structures of aligned-CNT nanocomposites and nano-engineered advanced composite macro-structures hybridized with aligned CNTs.

Aligned nanocomposites were fabricated by mechanical densification and polymer wetting of aligned CNTs [1]. Unmodified high-grade epoxy resins were used as a matrix. As reinforcement, aligned-CNT forests were grown to mm-heights on a Si substrate using a modified chemical-vapor-deposition process. The forests were grown on 1-cm² Si substrates and then released from the substrate. The volume fraction of as-grown CNTs is about 1%; however, the distance between the CNTs (and thus the volume fraction of the forest) can be varied by applying a compression force in both directions of the plane of the forest, resulting in volume fractions of CNTs exceeding 20%. Nanocomposites were fabricated by infusion of the matrix into the CNT forest via capillary-induced wetting [2, 3], the rate of which depends on properties of the CNT forest (e.g., volume fraction) and the polymer (viscosity, contact angle, etc.). Variable-volume fraction-aligned CNT nanocomposites were characterized using optical, scanning electron (SEM), and transmission electron (TEM) microscopy to analyze dispersion and alignment of CNTs as well as overall morphology. Nano-engineered composite macro-structures hybridized with aligned CNTs were prepared by placing long (>20 μm) aligned CNTs at the interface of advanced composite plies as reinforcement in the through-thickness axis of the laminate. Three fabrication routes were developed: transplantation of CNT forests onto preimpregnated plies [4] (the "nano-stitch" method), placement of detached CNT forests between two fabrics followed by subsequent infusion of matrix, and *in situ* growth of aligned CNTs onto the surface of ceramic fibers followed by impregnation and hand lay-up [5]. Aligned CNTs are observed at the composite ply interfaces. Significant improvement appears in interlaminar strength and electrical properties over composites without aligned CNTs . Analysis of the multifunctional properties of and nanoscale interactions between the constituents in both the nanocomposites and hybrid macrostructures is underway.



▲ Figure 1: Aligned CNT nanocomposites via biaxial mechanical densification of CNT forests.



▲ Figure 2: Aligned CNT nano-engineered composite macro-scale architectures.

References

[1] B.L. Wardle, D.S. Saito, E.J. Garcia, A.J. Hart, and R. Guzman de Villoria, "Fabrication and characterization of ultra-high volume fraction aligned carbon-nanotube-polymer composites," *Advanced Materials*, vol. 20, 14, pp. 2707-2714, July 2008.

[2] E.J. García, A.J. Hart, B.L. Wardle, and A.H. Slocum, "Fabrication of composite microstructures by capillarity-driven wetting of aligned carbon nanotubes with polymers," *Nanotechnology, vol. 18*, pp. 165602:1-11, 2007.

[3] E.J. García, A.J. Hart, B.L. Wardle, and A.H. Slocum, "Fabrication and nanocompression testing of aligned carbon-nanotube-polymer nanocomposites," *Advanced Materials*, vol. 19, pp. 2151, 2007.

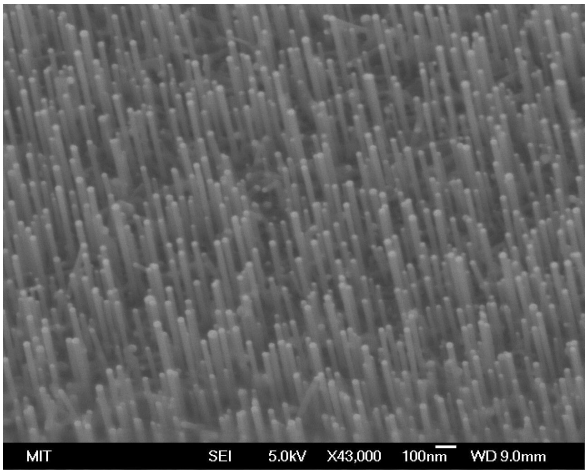
[4] E.J. Garcia, B.L. Wardle, and A.J. Hart, "Joining prepreg composite interfaces with aligned carbon nanotubes," *Composites Part A*, vol. 20, 14, pp. 2707-2714, June 2008.

[5] E.J. Garcia, B.L. Wardle, A.J. Hart, and N. Yamamoto, "Fabrication and multifunctional properties of a hybrid laminate with aligned carbon nanotubes grown in situ," *Composites Science and Technology*, vol. 68, 9, pp. 2034-2041, July 2008.

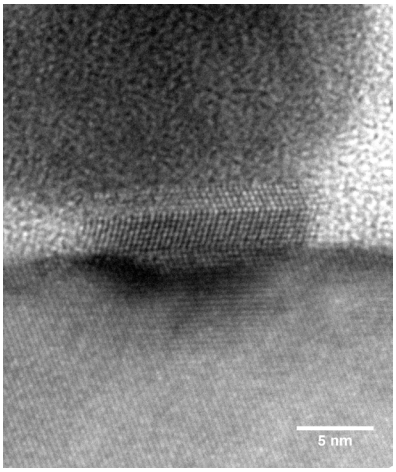
Catalyst Engineering and Growth Mechanisms of Si and III-V Nanowires

S.T. Boles, O.M. Nayfeh, C.K.F. Ho, D.A. Antoniadis, E.A. Fitzgerald, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

The vapor-liquid-solid mechanism for growth of single crystal whiskers and wires was originally discovered in the 1960s but has only recently been rediscovered as a way to fabricate high-performance nanoscale electronic devices, with dimensions below those attainable with photolithography. Although a great deal of attention has been focused on the electronic properties of Si and III-V nanowires, many of the physical mechanisms involved in growing these single crystal wires remain unclear. We have been investigating the importance of catalyst size and shape for wire growth morphology by using evaporated island catalysts, catalysts derived from dewetted thin films, and commercially available nanoparticles. Optimizing catalyst processing conditions and combining them with specific topographies or templates, such as inverted pyramid arrays or silicon dioxide gratings, achieves precise control over catalyst placement and subsequent nanowire placement. Also in this study, the role of growth conditions has been investigated by controlling the growth temperature, the partial pressures of reactants and the conditions of pre-growth annealing. These parameters have been determined to be critical not only to stable and repeatable growth of Si and III-V nanowires, but also to controlling the relative orientation and defect generation at the substrate-wire interface.



▲ Figure 1: Si nanowires grown on Si <111> substrates using Au catalysts.



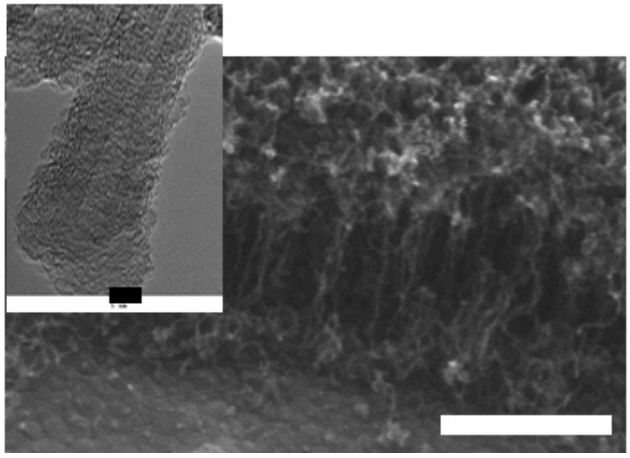
▲ Figure 2: GaP nanowire grown on Si <111> substrate using Ag catalyst.

Carbon Nanotube Growth for I.C. Interconnects

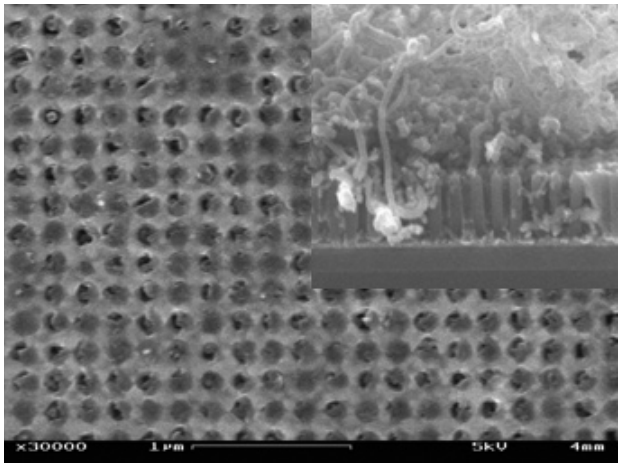
G.D. Nessim, Y. Wang, A.J. Hart, D. Acquaviva, J. Oh, J.S. Kim, C. Morgan, N. Abate, M. Seita, C.V. Thompson
Sponsorship: SRC/FCRP IFC, Intel

As integrated circuit technology is developed at dimensions below 32 nm, carbon nanotubes (CNTs) represent an ideal replacement for copper interconnects as they can carry higher current densities, do not need liners, and do not suffer from electromigration. However, fabrication issues such as growing the desired type of CNTs, using CMOS-compatible processes (e.g., ideally at temperature below 400°C) and making electrical contacts and interconnections, remain major technical challenges. For electrical applications, it is important to grow CNTs on conductive substrate [1, 2]. Using appropriate catalyst/substrate metallic thin films, we have grown vertically-aligned, crystalline CNTs using thermal chemical vapor deposition at 475°C (Figure 1). Preliminary electrical measurements show ohmic contact of the CNTs with the metallic substrate.

We have also grown CNTs on conductive substrates into an insulating alumina scaffold with regularly spaced pores (Figure 2). The insulating scaffold is fabricated using interference lithography and anodization of aluminum. This structure simulates an array of nanometer-scale vias filled with CNTs. In order to have CNTs with uniform height (length) and to make electrical contact with all the walls in the multi-wall tubes, we ion-milled the tops after CNT growth. The electrical properties of these CNTs can be collectively characterized through deposition of a conducting overlayer on all the CNTs or individually characterized using an AFM on uncapped CNTs. We plan to characterize electrical properties as a function CNT diameter and length and as a function of contact metallurgy.



▲ Figure 1: Carpet of vertically-aligned CNTs on conductive substrate grown at 475°C (scale bar 500 nm). The catalyst/underlayer system is Fe/Ta. The HRTEM image on the inset shows the crystalline nature of the CNTs (scale bar 5 nm).



▲ Figure 2: The CNTs grown into alumina scaffold with pores regularly spaced. The CNTs are flush with the top surface after ion milling. The inset shows the CNTs prior to ion milling.

References

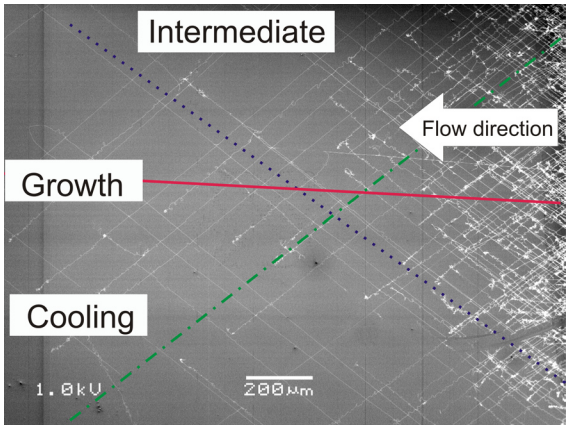
[1] H.T. Ng, B. Chen, J.E. Koehne, A.M. Cassell, J. Li, J. Han, and M. Meyyappan, "Growth of carbon nanotubes: A combinatorial method to study the effects of catalysts and underlayers," *Journal of Physical Chemistry B*, vol. 107, no. 33, pp. 8484-8489, 2003.

[2] S. Talapatra, S. Kar, S.K. Pal, R. Vajtai, L. Ci, P. Victor, M.M. Shaijumon, S. Kaur, O. Nalamasu, and P.M. Ajayan, "Direct growth of aligned carbon nanotubes on bulk metals," *Nature Nanotechnology*, vol. 1, no. 2, pp. 112-116, 2006.

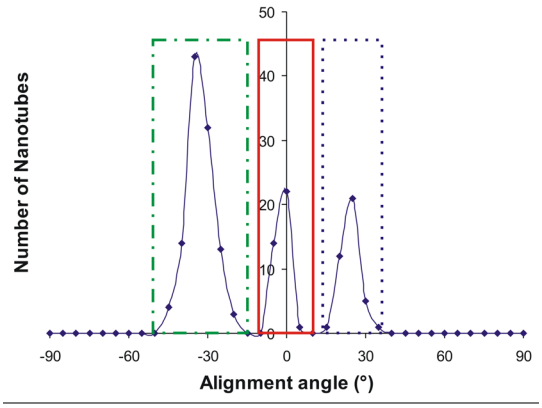
In-situ Sample Rotation as a Tool to Understand CVD Growth of Long Aligned Carbon Nanotubes

M. Hofmann, D. Nezich, A. Reina Cecco, J. Kong
Sponsorship: SRC/FCRP IFC, Intel

A new tool for studying the process of carbon nanotube chemical vapor deposition (CVD) synthesis is described. Rotating the substrate *in-situ* during the CVD process changes the orientation of floating nanotubes with respect to the substrate and nanotubes attached to the substrate by interaction with the gas stream (see Figure 1). Defining a time window in between consecutive rotation steps makes it is possible to study carbon nanotube behavior during CVD growth in a time-resolved manner (Figure 2). As an example, the settling process (i.e., the sinking of the nanotube to the substrate) is investigated. The analysis of forces acting on a floating nanotube shows that a vertical gas stream due to thermal buoyancy over the sample can keep long nanotubes floating for extended times. A stochastic process, indicated by a constant settling rate over time, forces the nanotube into contact with the substrate and this process is attributed to flow-induced instability. Our study reveals additional information on the floating and settling process. The authors acknowledge the support of the Interconnect Focus Center, one of five research centers funded under the Focus Center Research Program, a DARPA and Semiconductor Research Corporation program [1-4].



▲ Figure 1: An SEM picture of the aligned nanotubes after rotation with indication of corresponding experimental phases.



▲ Figure 2: Histogram of angular distribution of nanotubes with indication of corresponding phases.

References

[1] A. Reina, M. Hofmann, D. Zhu, and J. Kong, "Growth mechanism of long and horizontally aligned carbon nanotubes by chemical vapor deposition," *Journal of Physical Chemistry C*, vol. 111, no. 20, pp. 7292-7297, May 2007.

[2] L.X. Zheng, M.J. O'Connell, S.K. Doorn, X.Z. Liao, Y.H. Zhao, E.A. Akhadov, M.A. Hoffbauer, B.J. Roop, Q.X. Jia, R.C. Dye, D.E. Peterson, S.M. Huang, J. Liu, and Y.T. Zhu, "Ultralong single-wall carbon nanotubes," *Nature Materials*, vol. 3, no. 10, pp. 673-676, Oct. 2004.

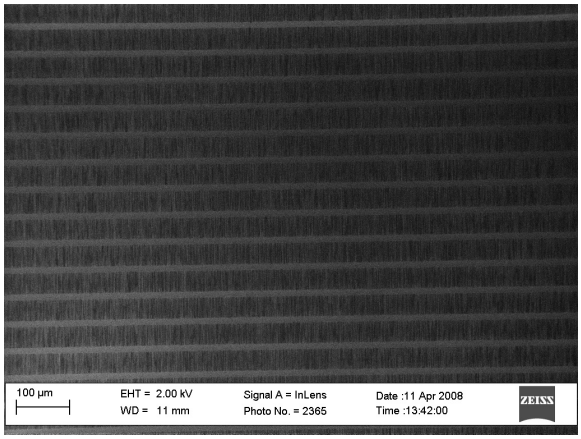
[3] L.M. Huang, Z. Jia, and S. O'Brien, "Orientated assembly of single-walled carbon nanotubes and applications," *Journal of Materials Chemistry*, vol. 17, no. 37, pp. 3863-3874, June 2007.

[4] D. Takagi, Y. Homma, S. Suzuki, and Y. Kobayashi, "*In-situ* scanning electron microscopy of single-walled carbon nanotube growth," *Surface and Interface Analysis*, vol. 38, nos. 12-13, pp. 1743-1746, Dec. 2006.

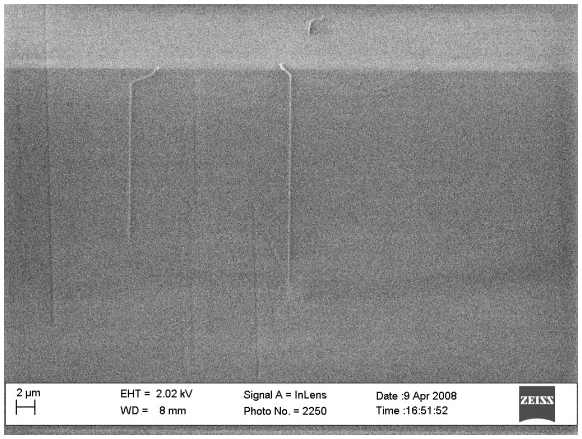
Growth Studies of In-plane and Out-of-plane SWNTs for Electron Devices

L.F. Velasquez-Garcia, D. Akinwande (Stanford), P. Wong (Stanford), A.I. Akinwande
Sponsorship: DARPA

Carbon nanotubes (CNTs) are currently massively investigated due to their remarkable mechanical, thermal, chemical, and electrical properties [1]. CNTs are seamless graphite tubes that can be grown using diverse methods such as arc deposition, chemical vapor deposition (CVD), and plasma-enhanced chemical-vapor-deposition (PECVD) [2]. The best performance comes from CNTs made of a single graphite sheet, i.e., single-walled carbon nanotubes (SWNTs). SWNTs are 1 – 2 nm in diameter and can have lengths over several centimeters [3]. Both in-plane and out-of-plane SWNTs are useful in the device industry. In-plane SWNTs can be used as the channel in transistors, while out-of-plane SWNTs can be used in circuit vias. We are currently investigating the growth of CVD SWNTs using our PECVD reactor. A forest of in-plane SWNTs can be grown using a methane/hydrogen chemistry at 200 Torr and 880°C if 2 Å Fe is used as a catalyst on top of quartz substrates (Figure 1). Sparse forests can be formed at lower pressures and temperatures (Figure 2). Current research focuses on investigating the growth space for in-plane SWNTs and developing growth recipes for out-of-plane SWNTs. With this information, devices will be designed and implemented.



▲ Figure 1: A forest of in-plane SWNTs grown at 880ºC and 200 Torr if iron is used as catalyst with a hydrogen/methane mix. The substrate is quartz.



▲ Figure 2: Sparse growth of in-plane SWNTs occurs if iron is used as a catalyst in a hydrogen/methane mix at 825ºC and 100 Torr. The substrate is quartz.

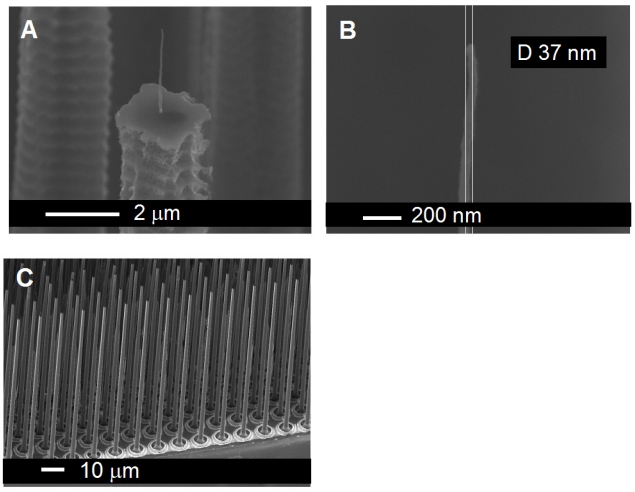
References

[1] S. Iijima, "Helical microtubules of graphitic carbon," *Nature*, vol. 354, no. 6348, pp. 56-58, 1991.
[2] K.B.K. Teo, S.-B. Lee, M. Chhowalla et al., "Plasma-enhanced chemical vapour deposition carbon nanotubes/nanofibers –How uniform do they grow?" *Nanotechnology*, vol 14, pp. 204-211, 2003.
[3] H.W. Zhu, C.L. Xu, D.H. Wu, B.Q. Wei, R. Vajtai, and P.M. Ajayan, "Direct synthesis of long single-walled carbon nanotube strands," *Science*, vol. 296, no. 5569, pp. 884-886, 2002.

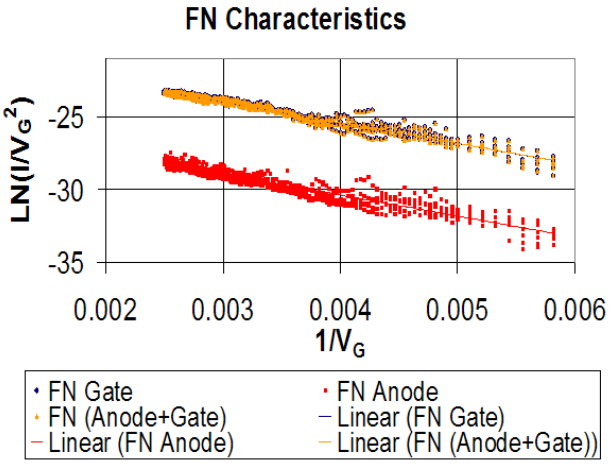
High-current CNT FEAs on Si Pillars

L.F. Velásquez-García, Y. Niu, A.I. Akinwande
Sponsorship: DARPA, AFOSR

Electrons are field-emitted from the surface of metals and semiconductors when the potential barrier (work function) that holds electrons within the metal or semiconductor is deformed by the application of a high electrostatic field. Field emitters use high-aspect-ratio structures with tips that have nanometer dimensions to produce a high electrostatic field with a low applied voltage. Small changes in the tip radius result in huge changes in the current density because of the exponential dependence of the emitted current on the bias voltage, as described by the Fowler-Nordheim theory. Also, tip radii variation in an array results in non-uniform turn-on voltages. If the emitters are ballasted, the spatial non-uniformity can then be substantially decreased. Furthermore, ballasting individual emitters prevents destructive emission from the sharper tips, resulting in higher overall current emission because of the inclusion of duller tips. Ballasting also results in more reliable operation. The use of large resistors in series with the field emitters is an unattractive ballasting approach because of the resulting low emission currents and power dissipation in the resistors. A better approach for ballasting field emitters is the use of ungated field-effect transistors (FETs) that effectively provide high dynamic resistance with large saturation currents [1]. In the past our research group demonstrated the use of a MOSFET to ballast the emission of electrons from silicon tips [2]. We have implemented a large and dense array of plasma-enhanced chemical-vapor-deposited (PECVD) carbon nanotubes (CNTs) (1-million elements in 1 cm2), in which each emitter is individually ballasted by a high-aspect-ratio column that acts as an ungated FET (Figure 1) [3]. For an n-Si substrate with a high-enough doping level, the Fowler- Nordheim (FN) plot of the data shows no saturation (Figure 2). Current research focuses in systematically studying the dependence of the ballasting on the doping level, showing current limiting data using CNT FEAs, and implementing a gated version of the field-emitter array.



▲ Figure 1: A PECVD CNT on top of a high-aspect-ratio Si column that acts as an ungated FET to limit the emitter current (A). The CNT is about 4 μm tall and it has 37-nm diameter (B). The FETs are 100 μm tall and have less than 1 μm × 1 μm cross-section (C).



▲ Figure 2: Fowler-Nordheim plot for a 10^6 CNT emitter array that uses an n-Si substrate with doping level equal to 1×10^{15} cm^{-3}. The FN model describes the electron current of the device because the doping level of its FETs is not low enough to produce current limitation.

References

[1] C.-Y. Hong and A.I. Akinwande, "Temporal and spatial current stability of field emission arrays," *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2323-2328, Oct. 2005.

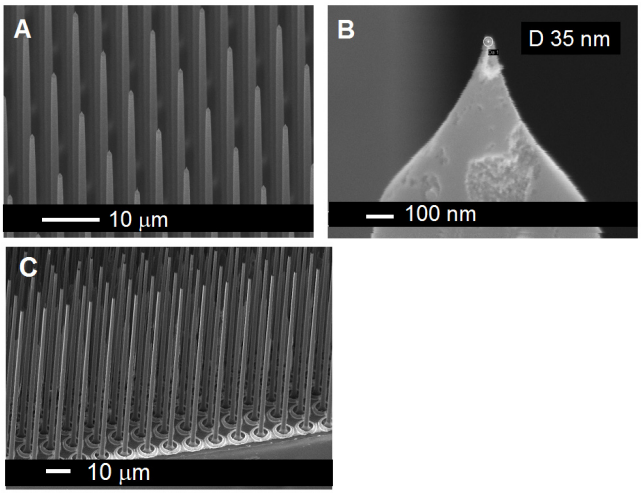
[2] H. Takemura, et. al., "A novel vertical current limiter fabricated with a deep-trench-forming technology for highly reliable field emitter arrays," *Technical Digest of the IEEE International Electron Device Meeting*, Dec. 1997, pp. 709-712.

[3] L.F. Velásquez-García, B. Andeoti, Y. Niu, and A.I. Akinwande, "Uniform high-current field-emission of electrons from Si and CNF FEAs individually controlled by Si pillar ungated FETs," *Technical Digest IEEE International Electron Device Meeting*, Washington DC, Dec. 2007, pp. 599-602.

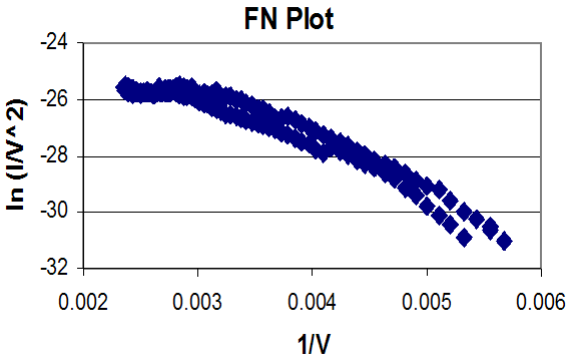
High-current Si FEAs on Si Pillars

L.F. Velásquez-García, Y. Niu, A.I. Akinwande
Sponsorship: DARPA, AFOSR

Electrons are field-emitted from the surface of metals and semiconductors when the potential barrier (work function) that holds electrons within the metal or semiconductor is deformed by the application of a high electrostatic field. Field emitters use high- aspect-ratio structures with tips that have nanometer dimensions to produce a high electrostatic field with a low applied voltage. Small changes in the tip radius result in huge changes in the current density because of the exponential dependence of the emitted current on the bias voltage, as described by the Fowler-Nordheim theory. Also, tip radii variation in an array results in non-uniform turn-on voltages. If the emitters are ballasted, the spatial non-uniformity can then be substantially decreased. Furthermore, ballasting individual emitters prevents destructive emission from the sharper tips, resulting in higher overall current emission because of the inclusion of duller tips. Ballasting also results in more reliable operation. The use of large resistors in series with the field emitters is an unattractive ballasting approach because of the resulting low emission currents and power dissipation in the resistors. A better approach for ballasting field emitters is the use of ungated field-effect transistors (FETs) that effectively provide high dynamic resistance with large saturation currents [1]. In the past our research group demonstrated the use of a MOSFET to ballast the emission of electrons from silicon tips [2]. We have implemented a large and dense array of conical Si tips (1 million elements in 1 cm^2), where each emitter is individually ballasted by a high-aspect-ratio column that acts as an ungated FET (Figure 1) [3]. The Fowler- Nordheim (FN) plot of the data for lowly doped arrays shows that the ungated FETs limit the emitter current because the slope of the curve becomes horizontal for high-enough current levels (Figure 2). We have obtained electron currents as large as 10 mA, the largest field-emitted currents reported from Si tips. Current research focuses on systematically studying the dependence of the ballasting on the doping level and implementing a gated version of the array.



▲ Figure 1: An array of silicon field emitters individually ballasted by vertical ungated FETs (A). The field emitter diameter is about 35 nm (B). The FETs are 100 μm tall and have a less than 1 μm × 1 μm cross-section (C).



▲ Figure 2: Fowler-Nordheim plot for a 4000 Si emitter array that uses an n-Si substrate with doping level equal to 2×10^{13} cm^{-3} For unballasted field emitters, the curve is a straight line. The current is limited to the point that the curve becomes horizontal for high enough voltages.

References

[1] C.-Y. Hong and A.I. Akinwande, "Temporal and spatial current stability of field emission arrays," *IEEE Transactions on Electron Devices*, vol. 52, no. 10, pp. 2323-2328, Oct. 2005.

[2] H. Takemura, et. al., "A novel vertical current limiter fabricated with a deep-trench-forming technology for highly reliable field emitter arrays," *Technical Digest of the IEEE International Electron Device Meeting*, Dec. 1997, pp. 709-712.

[3] L.F. Velásquez-García, B. Andeoti, Y. Niu and A.I. Akinwande, "Uniform high-current field-emission of electrons from Si and CNF FEAs individually controlled by Si pillar ungated FETs," *Technical Digest IEEE International Electron Device Meeting*, Dec. 2007, pp. 599- 602.

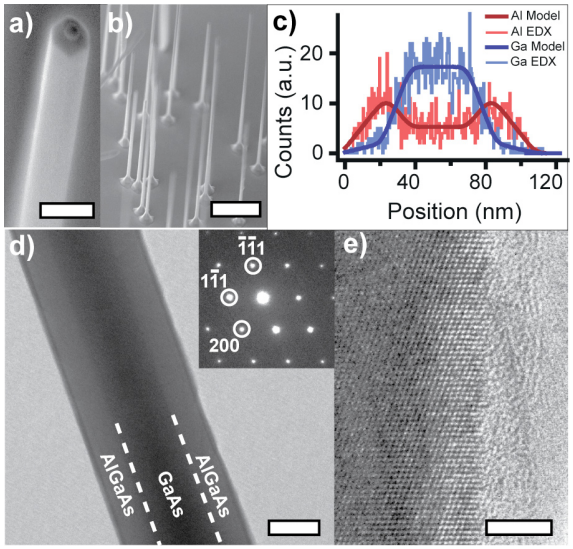
Compound Semiconductor Nanowire Heterostructures for High-mobility Electronics

M.J. Tambe, S. Gradečak

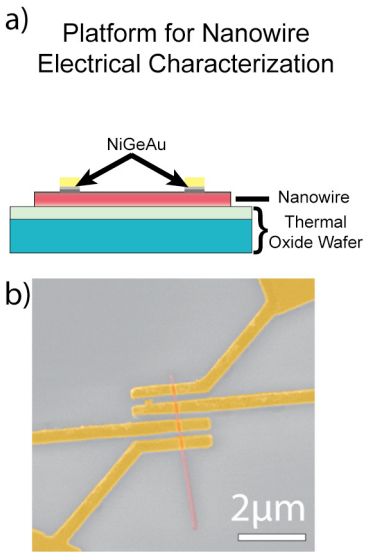
Sponsorship: 3M Inc., SRC/FCRP IFC 674.017

Semiconductor nanowires have emerged as a promising new platform for nanoscale electronics. With improved interfacial properties, more efficient strain relaxation, and reduced dimensionality, nanowire heterostructures have been predicted to be synthesizable with carrier mobilities significantly greater than bulk values. Since the carrier mobility of GaAs-based materials is intrinsically high, GaAs/AlGaAs nanowire heterostructures are an ideal candidate for nanowire high-mobility transistor applications. We propose to synthesize core-shell GaAs/AlGaAs nanowire heterostrucutres to study the potential benefits of nanostructuring on electronic transport properties as well as develop techniques to fabricate modulation-doped high-mobility nanowire transistors.

Radially-modulated core-shell GaAs/AlGaAs nanowire heterostructures have been synthesized by metal-organic chemical vapor deposition (MOCVD). Scanning electron microscopy (SEM) images show these wires grow vertically aligned with over 80% of the deposited catalyst nanoparticles yielding core-shell nanowires (Figure 1a, Figure 1b). Chemical analysis by energy dispersive X-Ray spectroscopy (EDS) reveals the composition of the core and shell to be GaAs and $Al_{0.9}Ga_{0.1}As$, respectively (Figure 1c). Structural analysis of the nanowires by transmission electron microscopy (TEM) confirms epitaxial shell deposition free of structural defects such as dislocations, stacking faults, and twin planes (Figure 1d, Figure 1e). The electronic transport properties of nanowires are studied by forming basic transistor structures. The nanowires are deposited onto degenerately doped Si/SiO_2 wafers and then Ohmic NiGeAu contacts are defined by e-beam lithography and deposited by e-beam evaporation. The top contacts serve as source and drain contacts while the gate contact is placed on the backside of the wafer using the top oxide as the gate oxide (Figure 2).



▲ Figure 1: a) SEM image of core-shell nanowire tip. b) SEM image of vertically aligned nanowires. c) EDX linescan analysis of a core-shell nanowire in planview. d) Bright-field TEM image of a core-shell nanowire showing clear core-shell contrast. (inset is SAD pattern along 011 zone axis) e) High-resolution TEM image of defect-free epitaxial AlGaAs shell.



▲ Figure 2: a) Schematic of a nanowire transistor for materials electrical characterization. b) False-colored SEM image of fabricated nanowire device.

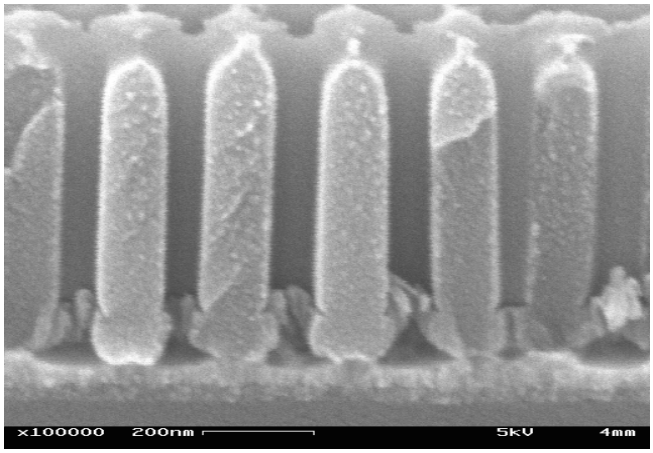
Anodic Aluminum Oxide Scaffolds and Metallic Nanowires for Sensor Applications

J. Oh, S. Cui, C.V. Thompson
Sponsorship: FCRP, Singapore-MIT Alliance

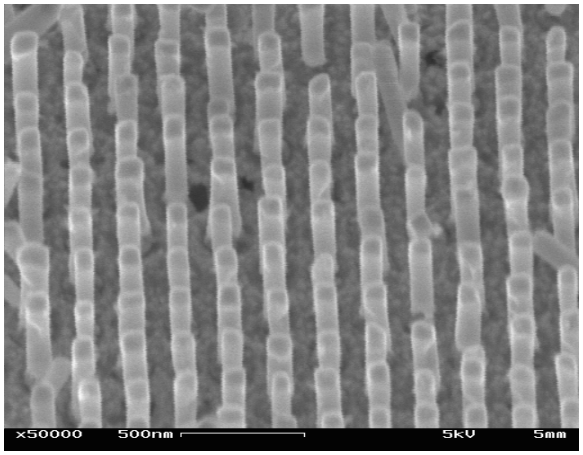
Metallic nanowires are core building blocks for advanced functional devices such as chemical and biochemical sensors [1]. To integrate nanowires into devices, it is desirable to fabricate them with controlled sizes and locations on device-applicable substrates. As a strategy for this goal, we are developing templated self-assembly methods that combine top-down (lithography) and bottom-up (self-assembly) approaches for fabrication and assembly of metallic nanowires for chemical and biochemical sensor applications, including a glucose biosensor [2].

Ordered porous alumina (OPA) is a nano-structured material that self-orders with domains and has been widely used as a template for growth of metallic nanowires, using electrochemical deposition techniques. However, growth of nanowires in OPA to make electrical contact to conducting underlayers is blocked by thin insulating barrier-oxide layers at the base of the pores, and removing these barriers without pore-widening due to etching [3-4] is desirable.

A new method for perforation of the OPA barrier layer has been developed based on anodization of Al/W multilayer films on substrates. When Al/W multilayer films are anodized and pores approach the Al/W interface, tungsten oxide forms and penetrates the alumina barrier oxide. By selectively etching the tungsten oxide, the barrier oxide can be removed and the base of the pores opened, without etching of the OPA (Figure 1). With this technique, we demonstrated that it is possible to perforate OPA barrier layers for porous structures with small-diameter pores at small spacings and fabricated free-standing metallic nanowires of materials such as Ni, Au, and Pt on Si substrates (Figure 2) by selectively removing the OPA template [5]. By modifying the surface of those nanowires, we are building a biosensor to detect glucose for diagnostics of diabetes.



▲ Figure 1: Cross-sectional SEM image of OPA after removal of thin barrier oxide.



▲ Figure 2: An SEM image of free-standing Ni nanowires on conducting layer on Si substrates.

References

[1] F. Favier, E.C. Walter, M.P. Zach, T. Benter, and R.M. Penner, "Hydrogen sensors and switches from electrodeposited Pd mesowire arrays," *Science*, vol. 93, pp. 2227-2231, Sept. 2001.

[2] R. Krishnan and C.V. Thompson, "Monodomain high-aspect-ratio 2D and 3D ordered porous alumina structures with independently controlled pore spacing and diameter," *Advanced Materials*, vol. 19, pp. 988-992, Apr. 2007.

[3] O. Rabin, P.R. Herz, Y.-M. Lin, A.I. Akinwande, S.B. Cronin, and M.S. Dresselhaus, "Formation of thick porous anodic alumina films and nanowire arrays on silicon wafers and glass," *Advanced Functional Materials*, vol. 13, pp. 631-638, Aug. 2003.

[4] K. Nielsch, F. Müller, A.P. Li, and U. Gösele, "Uniform nickel deposition into ordered alumina pores by pulsed electrodeposition," *Advanced Materials*, vol. 12, pp. 582-586, Apr. 2000.

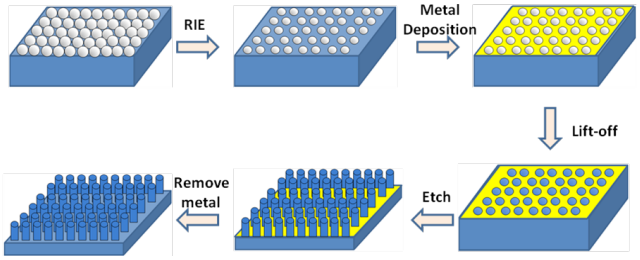
[5] J. Oh and C.V. Thompson, "Selective barrier perforation in porous alumina anodized on substrates," *Advanced Materials*, vol. 20, pp. 1368-1372, Apr. 2008.

Silicon Nanowire Fabrication by Metal-assisted Etching

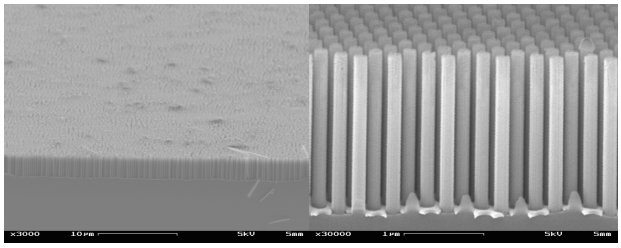
S.-W. Chang, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

Pore formation under anodic conditions is a well-known phenomenon for many semiconductors. However, the anodization approach to etching requires conductive substrates and independent control of a relatively large number of process parameters. To circumvent these problems, an electrochemical etching method known as metal-assisted etching (MAE) has recently received significant attention. In this approach metal catalysts are used to enhance local Si etching at the metal-silicon interface, in a mixture of hydrofluoric acid and an oxidant. The process can be used to fabricate high-aspect-ratio Si structures through patterned etching of silicon wafers. For example, we and others have used this technique to develop a relatively simple method for producing ordered arrays of one-dimensional silicon nanostructures over large areas via the combination of nanosphere lithography (NSL) and MAE.

In this approach, NSL is used to fabricate an ordered array of nanoscopic holes perforated in metal thin films. The process begins with the formation of a two-dimensional, self-assembled monolayer of monodisperse nanospheres. Typical domain sizes are in the 10-100-μm range [1]. A dry etching step is carried out to reduce the diameter of the nanospheres. A metal thin film is subsequently deposited through the nanosphere mask using electron beam (e-beam) evaporation. After metal deposition, the nanospheres can be selectively removed to leave behind only the metal deposited through the mask. Using this nanoporous film as a catalyst for silicon etching produces an ordered array of silicon nanopillars with the same diameter as the original pores. Figure 1 shows a schematic of the process flow. Figure 2 shows SEM images of a silicon nano-pillar array after etching. As can be seen in the lower magnification image on the left, the wires are very uniform in length, suggesting a uniform etch rate over large areas.



▲ Figure 1: Process flow for the fabrication of unpatterned 1D Si nano-pillars.



▲ Figure 2: Silicon nano-pillars fabricated using NSL and metal-assisted etching.

Reference

[1] G. Schmid, *Clusters and Colloids from Theory to Applications*.. New York, NY: Wiley-VCH, 1994.

Nano-particle Formation via Solid-state Dewetting

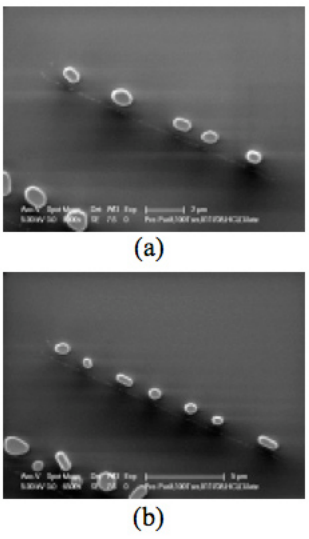
A.L. Giermann, J. Ye, Y. Wang, D. Kim, H. Yu, T.H. Liew, J. Yun, W.K. Choi, C.V. Thompson
Sponsorship: Singapore-MIT Alliance, NSF

We are investigating solid-state dewetting of thin films as a technique for producing ordered arrays of metal nanoparticles over large areas. Such arrays are used as catalysts for nanowire and nanotube growth and may also be of interest in memory or plasmon device applications.

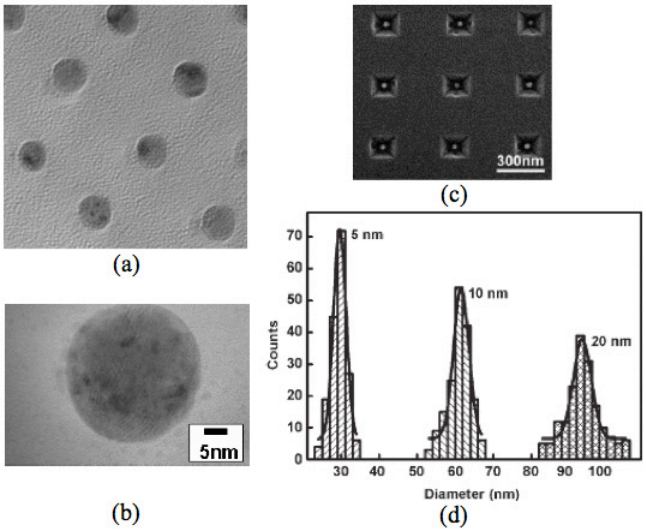
When we begin with a single crystalline film, the dewetted nanoislands align along specific crystallographic orientations and show regular patterns. We observe a strong dependence of the morphological evolution of single crystalline nickel thin films on the thickness of the film and on the crystallographic orientation of the film, which is determined by an epitaxial relationship with a magnesium oxide substrate. The resulting nanoparticles remain epitaxial and thus share both in- and out-of -plane crystallographic alignment.

In order to obtain similarly ordered dewetting with polycrystalline films, we employ physical templates. One technique is to physically constrain the area of film that dewets by pre-patterning a polycrystalline gold film on silicon dioxide. We observe that certain geometries lead to self-alignment of the dewetted nanoparticles (see Figure 1). Ongoing investigations will further characterize how film thickness and pattern dimensions affect the self-alignment.

Another technique for ordered dewetting of polycrystalline films is the use of topographic templates to modulate the curvature of as-deposited films. Gold films dewetted on di-periodic arrays of oxidized pyramidal pits in silicon result in one-to-one self-assembly of ordered arrays of gold particles over large areas. Compared to dewetting on flat substrates, the templates impose a significant decrease in average particle size and ensure a narrow size and spatial distribution. In this case, this technique results in crystallographic ordering of the particles, imposing an in-plane texture and changing the out-of-plane texture [1]. We observe similar spatial ordering behavior with other materials, including nickel (see Figures 2a and 2b) and cobalt; however, these materials have not demonstrated the crystallographic ordering effect. We have also combined pre-patterning with dewetting on topography to produce monodisperse Au particles. Heating allows controlled evaporation to produce populations of particles with smaller average size and a narrowed distribution of sizes (see Figures 2c and 2d) [2].



▲ Figure 1: Rows of Au particles formed by dewetting of 30-nm-thick films as a) 1.3 μm x14.5 μm and b) 1.3 μm x18 μm.



▲ Figure 2: Solid-state dewetting on substrates with inverted pyramid array topographies. (a and b) Transmission electron micrographs of ordered Ni nanoparticles. (c) Scanning electron micrograph of Au nanoparticles. (d) Distribution of nanoparticle diameters obtained by annealing Au layers with thicknesses of 5 nm, 10 nm and 20 nm at 1000 °C for 60 min.

References

[1] A.L. Giermann and C.V. Thompson, "Solid-state dewetting for ordered arrays of crystallographically oriented metal particles," *Applied Physics Letters*, vol. 86, p. 121903, Mar. 2005.

[2] W.K. Choi, T.H. Liew, H.G. Chew, F. Zheng, C.V. Thompson. Y. Wang, M.H. Hong, X.D. Wang , L. Li, and J. Yun, "A combined top-down and bottom-up approach for precision placement of metal nanoparticles on silicon," *Small*, vol. 4, no. 3, p. 330, 2008.

4

MEMS& BioMEMS

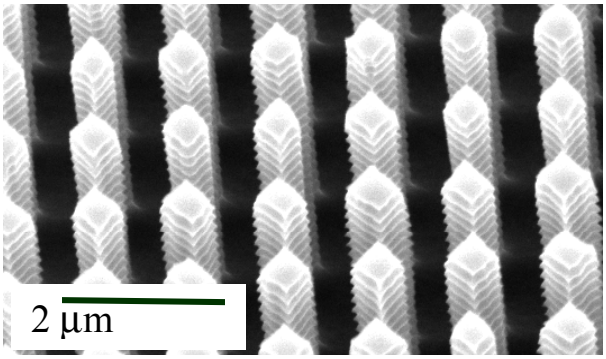
Table of Contents

Superhydrophilic and Superhydrophobic Nanostructured Surfaces for Microfluidics and Thermal Management

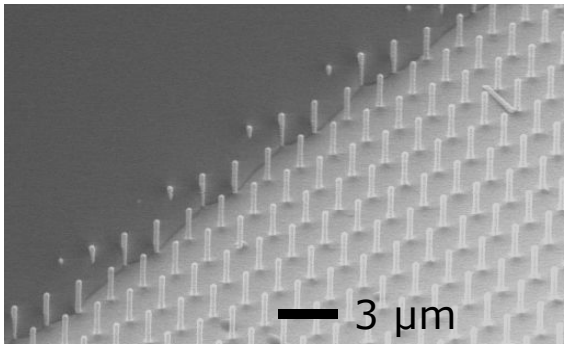
R. Xiao, K. Chu, E.N.Wang

Nanostructured features can be used to magnify the intrinsic hydrophobicity or hydrophilicity of a material to create superhydrophobic and superhydrophilic surfaces [1, 2]. There has been particular interest in these surfaces for a variety of applications including self-cleaning and drag reduction with superhydrophobic surfaces [3-5]. Superhydrophilic surfaces are of interest in anti-fogging and thermal management [6-8]. Past work has demonstrated significant changes in contact angle with minimal hysteresis with the introduction of nanostructured surface features [9]. Current efforts, however, focus on the dynamic robustness and spreading of liquids on such surfaces

We have fabricated silicon pillar arrays with cross sections of 500 nm × 500 nm, spacings between pillars of 800 nm, and heights of 5 μm (Figure 1). The pillar arrays are naturally oxidized in air to make them hydrophilic. The interaction of the spreading liquid with the fabricated pillars was studied using diffraction limited microscopy and with an environmental scanning electron microscope (Figure 2). The preliminary data (Figure 2) shows that the liquid-air interface is pinned diagonally. Using an energy minimization approach, theory is currently being developed to understand the effect of pillar spacing, height, and diameter on spreading dynamics. We have also concurrently coated the silicon pillars with a silane chemistry to create superhydrophobic surfaces. The effect of shape and size of the nanostructures on hydrophobic robustness is currently being investigated.



▲ Figure 1: Scanning electron micrograph of a silicon nanopillar array where the side length of the pillars is 500 nm, spacing between pillars is 800 nm, and height of the pillar is 5 μm. Due to the deep reactive etching process, scallops of tens of nanometers are present along the side walls of the pillars.



▲ Figure 2: Scanning electron micrograph of liquid spreading on a superhydrophilic surface. The contact line is pinned diagonally.

References

[1] W. Barthlott, C. Neinhuis, "Purity of the sacred lotus, or escape from contamination in biological surfaces," *Planta*, vol. 202, no. 1, pp. 1-8, 1997.
[2] R.D. Hazlett, "Fractal applications: Wettability and contact angle," *Journal of Colloid Interface Sci*ence, vol. 137, no. 2, pp. 527, 1990.
[3] N.A. Patankar, "Transition between superhydrophobic states on rough surfaces," *Langmuir*, vol. 20, no. 17, pp. 7097-7102, 2004.
[4] Z. Yoshimitsu, A. Nakajima, T. Watanabe, K. Hashimoto, "Effects of surface structure on the hydrophobicity and sliding behavior of water droplets," *Langmuir*, vol. 18, no. 15, pp. 5818-5822, 2002.
[5] J. Jopp, H. Grull, and R. Yerushalmi-Rozen, "Wetting behavior of water droplets on hydrophobic microtextures of comparable size," *Langmuir*, vol. 20, no. 23, pp. 10015-10019, 2004.
[6] A. Fujishima, D.A. Tryk, T. Watanabe, and K. Hashimoto, "Self-cleaning glass," *International Glass Review—Flat Glass Processing*, no. 2, pp. 114-6, 1998.
[7] Y. Takata, K. Tanaka, K. Kaijima, T. Ito, T. Watanabe, and M. Shimohigoshi, "Enhancement of heat transfer with liquid-vapor phase change by photo-induced hydrophilicity, " in *Proc. of the 33rd National Heat Transfer Conference (CD-ROM)*. Albuquerque, NM, 1999.
[8] Y. Takata, K. Tanaka, K. Kaijima, T. Ito, T. Watanabe, and M. Shimohigoshi, "Enhancement of boiling and evaporation heat transfer by superhydrophilic photocatalyst," in *Proc. of the 6th UK National Conference on Heat Transfer*, Edinburgh, UK. 1999, pp. 323-8.
[9] C. Extrand, "Model for contact angles and hysteresis on rough and ultraphobic surfaces," *Langmuir*, vol. 18, pp. 7991-7999, 2002.

Design of a Micro-breather for Venting Vapor Slugs in Two-phase Microchannels

B. Alexander, E. Wang

Sponsorship: Department of Mechanical Engineering, Intel Higher Education grant, Northrop Grumman Corporation

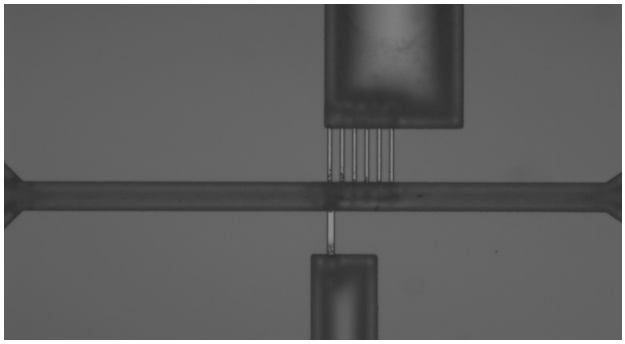
Boiling is currently used in a variety of industries as an efficient method of cooling. Boiling, and phase-change in general, are attractive because the latent heat of vaporization can be used to carry and dissipate large heat fluxes. Two-phase microchannels have been of recent interest because they promise compact and efficient solutions [1].

However, phase-change in microchannels leads to challenges that are not present in macroscale counterparts because the governing forces are different. Surface tension forces become dominant at the microscale whereas buoyancy forces can be neglected. As a result, flow instabilities, large pressure fluctuations, and local liquid dry-out occur in microchannels, which severely limits the overall thermal performance.

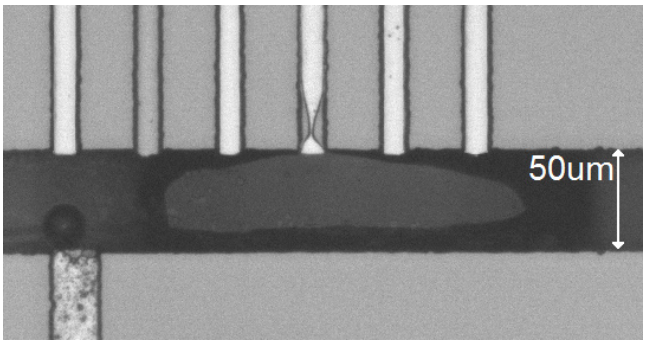
To address these problems, a few solutions have been proposed [2, 3], including the use of porous membranes or hydrophobic ports that allow vapor bubbles to escape from the microchannels as they form. The proposed solutions have drawbacks, including the inability to sufficiently remove vapor bubbles effectively and eliminate dry-out within the channels.

We propose a design for a microscale breathing device that uses the combination of surface chemistry and geometry to separate vapor from a liquid flow. To better understand the physics and governing parameters for the microscale breather, we designed a test device that allows for cross-sectional visualization of a breathing microchannel (Figure 1). We have conducted various experiments and collected image data to help direct our vapor breather design to achieve high vapor removal efficiencies with minimal fabrication effort and control requirements (Figure 2).

The successful implementation of a microchannel with an efficient breather will allow for new cooling technologies with higher heat removal capacities that can be effectively used by the semiconductor industry. The breathers also have significant promise as liquid vapor separators for use in micro-fuel cells and other applications that require phase separation at the microscale.



▲ Figure 1: Image of the entire breathing test device under low magnification. The entry and exit portions of the channel are visible at both ends of the picture. The breathing structure is above the main channel near the center of the image, and the air inlet is below the main channel near the center of the image.



▲ Figure 2: Image of a gas bubble breathing in the channel. The gas slug is attached to the breathing structure and venting as more gas is added from the air inlet port just upstream (bottom left of image).

References

[1] J. Thome, "The new frontier in heat transfer: Microscale and nanoscale technologies," *Heat Transfer Engineering*, vol. 27, no. 9, pp. 1-3, 2006.

[2] D. Meng and C. Kim, "Self-aligned micro bubble arrays by using surface tension," in *Proc. of ASME International Mechanical Engineering Congress and Exposition*, 2004.

[3] A. Kosar, C. Kuo, and Y. Peles, "Suppression of boiling flow oscillations in parallel microchannels by inlet restrictors," *Journal of Heat Transfer*, vol. 128, pp. 251-260, Mar. 2006.

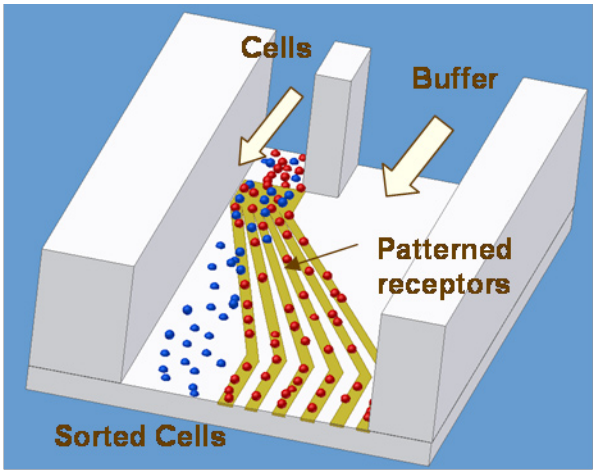
Microfluidic Patterning of P-Selectin for Cell Separation through Rolling

S. Bose, S. Hong, R.S. Langer, J.M. Karp, R. Karnik
Sponsorship: NIH

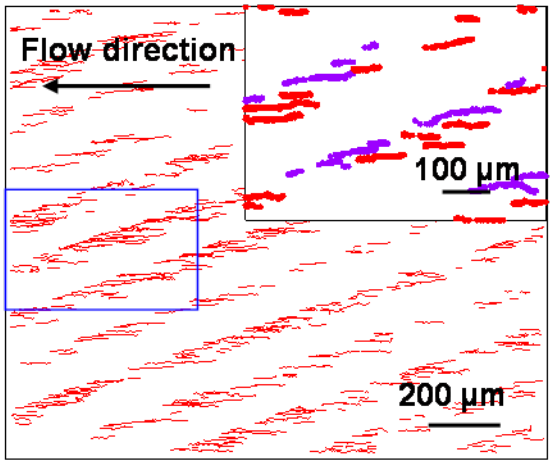
Cell separation based on markers present on the cell surface has extensive biological applications. However, current separation methods involve labeling cells and label removal steps that are often slow and intrusive. Recently, we discovered that it is possible to steer cells interacting transiently with the surface through patterning of receptors on the surface [1]. In this paper we report microfluidic patterning of P-selectin receptors to control cell rolling for label-free separation of cells. We envision a microfluidic device that would perform label-free separation of cells by rolling them on receptor patterned surfaces (Figure 1). The present work is the first step towards realizing these devices.

A microchannel defining the pattern was fabricated in PDMS and reversibly bonded onto a polystyrene substrate. Human P-Selectin was filled inside the microchannel and left overnight for physisorbtion to complete. Later the PDMS mask was removed, and the surface was washed with PBS and finally incubated in Fetal Bovine Serum to block non-specific interactions. HL-60 myeloid cell suspension was flowed over the surface to verify patterning of P-selectin. We observed that cells interacted selectively with the P-selectin region, showing that the patterning technique was successful (Figure 2). Rolling was clearly observed on the selectin-coated bands and some deflection of cells at the edge was also observed. A few cells were also seen to detach from one band and reattach at another selectin band downstream.

This work demonstrates microfluidic patterning of P-selectin that is essential for a device for cell separation based on cell rolling. In the future, these patterns will be incorporated in a smaller microfluidic flow chamber with multiple inlets and outlets for label-free, continuous-flow cell separation.



▲ Figure 1: Schematic of the proposed cell separation device. Cells are introduced from one side in a buffer flow. Rolling of cells on patterned receptors causes them to separate laterally, from where they can be collected in different conduits.



▲ Figure 2: Tracks of HL-60 cells rolling on P-selectin patterns. Closer observation (magnified inset showing selected tracks) shows that some cells get slightly deflected before detaching from the P-selectin regions.

References

[1] R. Karnik, S. Hong, H. Zang, Y. Mei, D. Anderson, J. Karp, and R. Langer, "Nanomechanical control of cell rolling in two dimensions through surface patterning of receptors," *Nano Letters 8*, 2008, to be published.

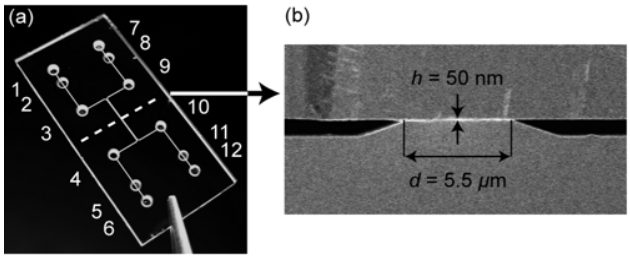
Electrical Detection of Fast Reaction Kinetics in Nanochannels with an Induced Flow

L.F. Cheow, R.B. Schoch, J. Han

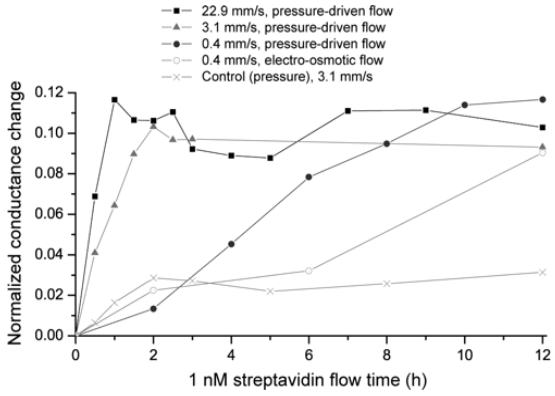
Sponsorship: DuPont-MIT Alliance, NIH

Nanofluidic channels can be used to enhance surface binding reactions, since the target molecules are closely confined to the surfaces that are coated with specific binding partners. Moreover, diffusion-limited binding can be significantly enhanced if the molecules are steered into the nanochannels via either pressure-driven or electrokinetic flow. Monitoring the nanochannel impedance, which is sensitive to surface binding, has led to electrical detection of low analyte concentrations in nanofluidic channels within response times of 1-2 h [1]. This finding represents a ~54 fold reduction in the response time using convective flow compared to diffusion-limited binding [2]. At high flow velocities, the presented method of reaction kinetics enhancement is potentially limited by force-induced dissociations of the receptor-ligand bonds [3]. Optimization of this scheme could be useful for label-free, electrical detection of biomolecule binding reactions within nanochannels on a chip.

We acknowledge MTL for support during the fabrication process.



▲ Figure 1: Design of the device, consisting of two microchannels joined by nanochannels. (a) Photograph of the 12 × 25 mm chip showing the two microchannels and access holes. (b) The cross-sectional view along the dotted line, with a scanning electron microscope image showing two microchannels (with electrodes at their bottom) which are connected by nanochannels with height h = 50 nm and length d = 5.5 μm.



▲ Figure 2: Decrease of the response time of 1 nM streptavidin from ~12 to ~1 h by increasing the flow velocity through the nano-channel, presented by the normalized conductance change vs. streptavidin flow time. The control measurement was made with a 1-nM streptavidin solution and a protein-resistant channel coating under pressure-driven flow. The connecting lines are for guidance only.

References

[1] R.B. Schoch, L.F. Cheow, and J. Han, "Electrical detection of fast reaction kinetics in nanochannels with an induced flow," *Nano Letters*, vol. 7, no. 12, pp. 3895-3900, Nov. 2007.

[2] R. Karnik, K. Castelio, R. Fan, P. Yang, and A. Majumdar, "Effects of biological reactions and modifications on conductance of nanofluidic channels," *Nano Letters*, vol. 5, no. 9, pp. 1638-1642, July 2005.

[3] A. Pierres, D. Touchard, A.M. Benoliel, and P. Bongrand, "Dissecting Streptavidin-biotin interaction with a laminar flow chamber," *Biophysics Journal*, vol. 82, no. 6, pp. 3214-3223, June 2002.

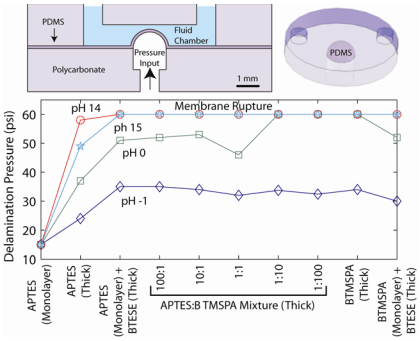
Integration of Actuated Membranes in Thermoplastic Microfluidic Devices

K.S. Lee, R.J. Ram
Sponsorship: NSF

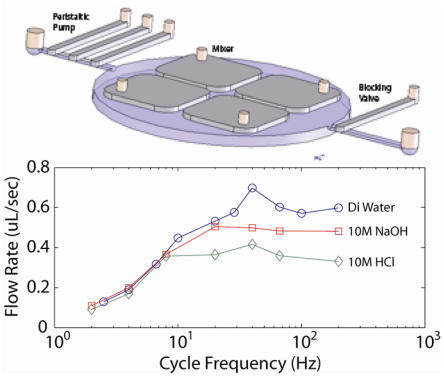
PolyDiMethylSiloxane (PDMS) is a common material for fabrication of microfluidic devices. Elasticity provided by PDMS enables the creation of active devices that utilize pressurized membranes such as pumps and mixers. However, for structures requiring dimensional stability, rigidity, or disposability, plastics have the required properties [1]. Plastics can be manufactured using mass fabrication technologies such as injection molding and hot embossing with established bonding processes [2], but at the cost of sacrificing active device functionality. A new fabrication process combining plastic substrates with PDMS membranes enables the creation of active microfluidic devices inside dimensionally stable systems, merging the functionality of PDMS with established plastic fabrication technologies.

Irreversible bonding between PDMS and plastics for fluidics requires interfaces that can handle high pressure and harsh chemical environments. Hydrolytic stability under acidic or basic conditions is particularly important. Direct bonding between PMMA and PDMS has been explored [3], but interfaces withstood only 2.5 psi before failure. Surface modification of polycarbonate and PMMA surfaces with AminoPropylTriEthoxySilane (APTES) [4] has also been shown to enable PDMS plasma bonding [5], but no data on hydrolytic stability was shown.

To improve hydrolytic stability, two additional silanes were explored, BisTriEthoxySilylEthane (BTESE) and Bis(TriMethoxySilylPropyl) Amine (BTMSPA), for thin and thick primer coatings, respectively. Devices with PDMS membranes suspended over 25-µL fluid reservoirs were fabricated in PC and PMMA to test interface robustness. For all devices, membrane ruptures occurred instead of delamination at 60 psi, making the devices suitable for active valves. Blisters were then subjected to NaOH and HCl solutions from the PDMS side at 70 C for 2 hours, followed by pressure testing. Figure 1 shows that hydrolytic stability improves over APTES with addition of BTMSPA to the primer solution for thick coatings or BTESE for monolayer coatings. A test chip containing peristaltic pumps and mixers was then fabricated, and pump rate versus frequency was measured as shown in Figure 2.



▲ Figure 1: Schematic of the aqueous blister test structure utilized to test hydrolytic bond failure. PDMS membranes were 70 µm thick over 915-µm-diameter circles. Plot of the delamination pressure versus primer type at pH extremes. Hydrolytic stability increases with addition of BTMSPA or protection by BTESE.



▲ Figure 2: Schematic of the test device fabricated in PC with a 70-µm PDMS membrane for pressure based actuation. Flow rate versus frequency for different pH at 15 psi for an 800x600 µm^2 cross-section membrane-based peristaltic pump is plotted. Performance degradation at higher frequencies most likely results from valve sticking due to acid/base induced modification of the PDMS and silane surfaces.

References

[1] H. Becker and C. Gartner, "Polymer microfabrication technologies for microfluidic systems," *Analytical Bioanalytical Chemistry*, vol. 390, pp. 89-111, 2008.

[2] L. Brown, T. Koerner, J.H. Horton, and R.D. Oleschuk, "Fabrication and characterization of poly(methylmethacrylate) microfluidic devices bonded using surface modifications and solvents," *Lab on a Chip*, vol. 6, pp. 66-73, 2006.

[3] W.W.Y. Chow, K.F. Lei, G. Shi, W.J. Li, and Q. Huang, "Micro fluidic channel fabriation by PDMS-interface bonding," *Smart Materials and Structures*, vol. 15, pp. S112-S116, 2006.

[4] C. Li and G.L. Wilkes, "The mechanism for 3-aminopropyltriethoxysilane to strengthen the interface of polycarbonate substrates with hybrid organic-inorganic sol-gel coatings," *Journal of Inorganic Organometallic Polymers*, vol. 7, pp. 203-215, 1997.

[5] M.E. Vlachopoulou, A. Tserepi, and K. Misiakos, "A novel process for irreversible bonding of PDMS and PMMA substrates," *MNE'06 Micro- and Nano- Engineering*, 2006.

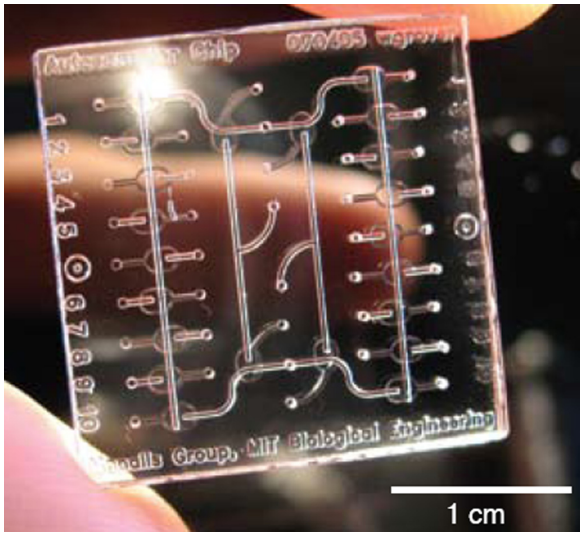
Teflon Films for Chemically-inert Microfluidic Valves and Pumps

W.H. Grover, M.G. von Muhlen, S.R. Manalis

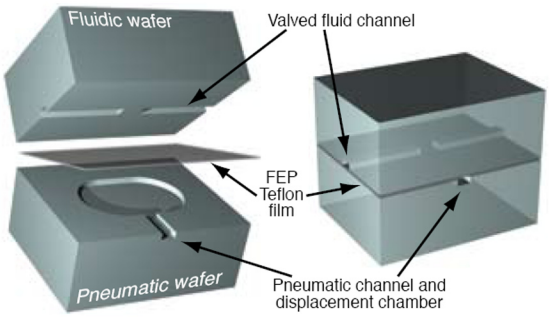
Sponsorship: NIH, ARO

Like transistors in electronic microprocessors, microfluidic valves and pumps are the fundamental elements of logic and control in many lab-on-a-chip devices. Flexible elastomers make good candidates for the moving parts in valves and pumps, and elastomers like polydimethylsiloxane (PDMS) have found widespread use in a variety of normally-open and normally-closed microfluidic valves. Unfortunately, the limited chemical compatibility of PDMS has complicated its use in many microfluidic applications. Many chemicals commonly used in organic synthesis readily swell PDMS devices or dissolve PDMS oligomers from the elastomer. Small hydrophobic molecules readily partition into and out of bulk PDMS, complicating the determination of their on-chip concentration. Some reusable glass microfluidic devices must be equipped with removable, disposable valves because the PDMS valves would be destroyed by the harsh acid used to clean the device before reuse. For these reasons, a large variety of interesting and useful chemistries may be unsuitable for use in native PDMS devices.

We have developed a simple alternative method for fabricating Teflon monolithic membrane valves and pumps in glass microfluidic devices [1]. We have found that inexpensive, commercially-available fluorinated ethylene-propylene (FEP) Teflon films can be bonded between etched glass wafers to form chemically-inert monolithic membrane valves and pumps. Both FEP and polytetrafluoroethylene (PTFE) are comprised entirely of carbon and fluorine and are similarly inert. But while PTFE is opaque and must be cut or skived to make rough thin sheets, FEP is transparent and available as a smooth, uniform thin film. Chemical compatibility data from nearly 50 years of use as a commercial product show that FEP is resistant to virtually all chemicals except "molten alkali metals, gaseous fluorine, and certain complex halogenated compounds such as chlorine trifluoride at elevated temperatures and pressures."[2] The resulting glass-FEP-glass devices are optically transparent and suitable for imaging or fluorescence applications (Figures 1, 2). The FEP Teflon valves permit unimpeded (0.9 µL/s) flow while open and negligible (< 250 pL/s) leakage while closed against 14 kPa fluid pressure. The FEP pumps can precisely meter nanoliter-scale volumes at up to microliter/second rates. The pumps also show excellent long-term durability with < 4% change in pumping rate after 13 days of continuous operation. By combining ease of fabrication with extreme chemical inertness, these Teflon monolithic membrane valves and pumps enable research involving a vast array of chemistries that are incompatible with native PDMS microfluidic devices.



▲ Figure 1: Photograph of an Autosampler Chip containing 22 monolithic membrane FEP Teflon valves. The Autosampler Chip can deliver extremely caustic piranha solution (concentrated sulfuric acid and hydrogen peroxide) to clean an off-chip sensor without causing any detectable damage to the chip or its valves.



▲ Figure 2: Exploded and assembled illustrations of a single FEP valve.

References

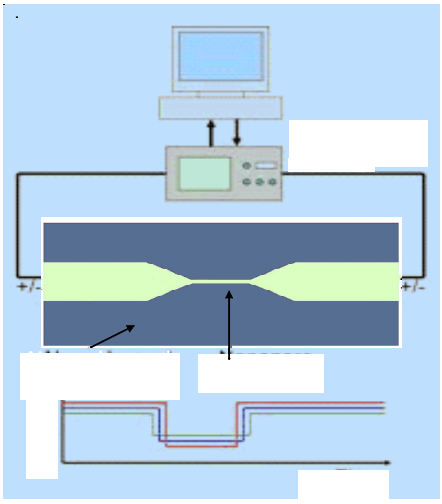
[1] W.H. Grover, M.G. von Muhlen, and S.R. Manalis, "Teflon films for chemically-inert microfluidic valves and pumps," *Lab on a Chip*, vol. 8, pp. 913-918 May 2008.

[2] DuPont. (2008). FEP Fluorocarbon Film Properties Bulletin. [Online] Available: http://www2.dupont.com/Teflon_Industrial/en_US/assets/downloads/h55008.pdf.

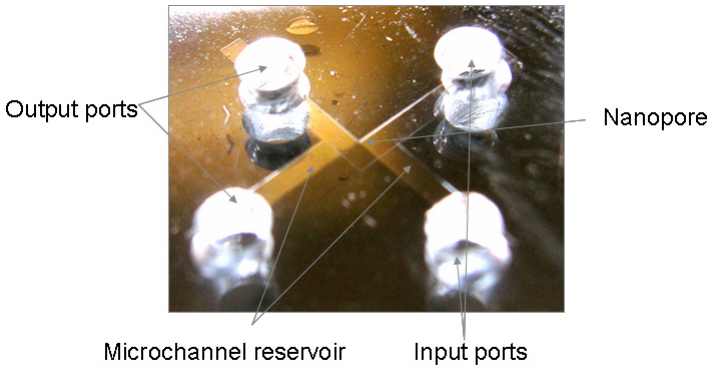
Nanofluidic System for Single-particle Manipulation and Analysis

Y.H. Sen, R. Karnik
Sponsorship: MIT

Nanopores are versatile sensors for detection of single molecules and particles in solution. When a molecule passes through a nanopore with a voltage bias applied across it, the resulting transient blockage of the nanopore yields a detectable current change that enables single-molecule sensing [1, 2]. Different molecules may exhibit different current blockage and duration profiles, which may be used to characterize the molecules. However, the sensing ability of nanopores is often limited by the quick transit times of molecules through the nanopore that result in poor signal-to-noise ratio. To address this issue, we are developing a nanofluidic system to manipulate single particles and molecules that will enable multiple measurements on the same molecule (Figure 1). Nanofluidic channels will function as traps to localize the molecule in the system after its translocation (transit) through the nanopore. When the electric field across the nanopore is reversed, the same molecule will travel through the nanopore again. Feedback control will be used to reverse the applied voltage bias and thus ensure multiple translocations of a molecule through the nanopore. This technique will enable integration of a signal over multiple translocations, thereby improving the signal-to-noise ratio. For proof-of-concept, translocation signals of DNA molecules through a PDMS (polydimethylsiloxane) nanopore will be measured using a patch-clamp amplifier. Techniques of E-beam lithography and UV lithography are adopted to create a master mold of the device consisting of nanopores and reservoirs. Soft lithography with PDMS will be used for rapid and reproducible fabrication of nanopores connecting two reservoirs (Figure 2) [3]. This approach will demonstrate a new paradigm in sensing by using nanopores, and it may enable an unprecedented level of characterization of nanoparticles and biomolecules.



▲ Figure 1: Experiment setup and expected current signal profile for the passage of a molecule through the nanopore. The amplifier serves as a clamped voltage source and measures the corresponding current signal. Data will be obtained from multiple translocations of a single molecule through a nanopore enabled by feedback control. The nanochannel reservoir will prevent escape of the molecule of interest into the solution



▲ Figure 2: Details of a nanopore molecule sensing device. The PDMS device is fabricated using E-beam lithography and UV lithography, followed by soft-lithography. Two reservoirs are connected with one nanopore.

References

[1] J.J. Kasianowicz, E. Brandin, D. Branton, and D.W. Deamer, "Characterization of individual polynucleotide molecules using a membrane channel,"in *Proc. National Academy of Sciences USA*, vol. 93, pp. 13770–13773, Nov. 1996.

[2] D. Fologea, J. Uplinger, B. Thomas, D.S. McNabb, and J.L. Li, "Slowing DNA transportation in a solid-state nanopore," *Nano Letters*, vol. 5, no. 9, pp. 1734-1737, 2005.

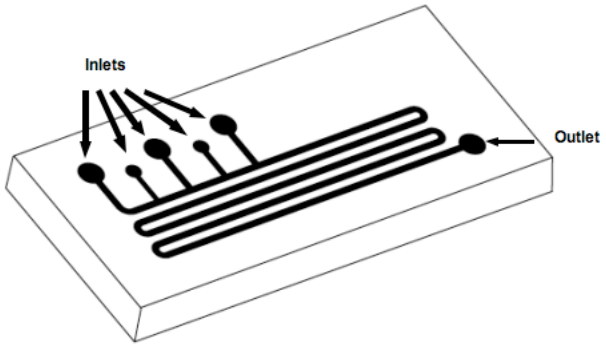
[3] A.O. Saleh and L.L. Sohn, "An artificial nanopore for molecular sensing," *Nano Letters*, vol. 3, no. 1, pp. 37-38, 2003.

Microfluidic Systems for Continuous Crystallization

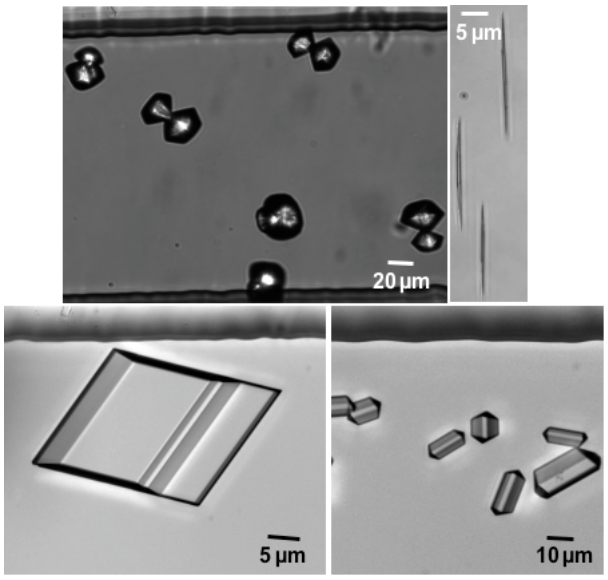
M. Sultana, K.F. Jensen
Sponsorship: Merck, Lucent Technologies

Microfluidic systems offer a unique toolset for discovering new crystal polymorphs and for studying the growth kinetics of crystal systems because of well-defined laminar flow profiles and online optical access for measurements. Traditionally, crystallization has been achieved in batch processes that suffer from non-uniform process conditions across the reactors and chaotic, poorly controlled mixing of the reactants, resulting in polydisperse crystal size distributions (CSD) and impure polymorphs. This reduces reproducibility, increases difficulty in obtaining accurate kinetics data, and manufactures products with inhomogeneous properties. The short length scale in microfluidic devices allows for better control over the process parameters, such as the temperature and the contact mode of the reactants, creating uniform process conditions across the reactor channel. Thus, these devices have the potential to generate more accurate kinetics data and produce crystals with a single morphology and a more uniform size distribution. In addition, microfluidic systems decrease waste, provide safety advantages, and require only minute amounts of reactants, which is most important when dealing with expensive materials such as pharmaceutical drugs.

Figure 1 shows a microfluidic device used for crystallization and Figure 2 shows optical images of different polymorphs of glycine crystals grown in reactor channels. A key issue for achieving continuous crystallization in microsystems is to eliminate heterogeneous crystallization – irregular and uncontrolled formation and growth of crystals at the channel surface-- and aggregation of crystals, which ultimately clogs the reactor channel. We have developed a microcrystallizer using soft lithography techniques that introduces the reagents to the reactor channel in a controlled manner, preventing heterogeneous crystallization and aggregation. We have also integrated an online spectroscopy tool for *in situ* polymorph detection. Our ultimate goal is to develop an integrated microfluidic system for continuous crystallization with the ability to control and detect the crystal morphology, as well as obtain kinetics of crystallization through online detection.



▲ Figure 1: Microfluidic device used for crystallization.



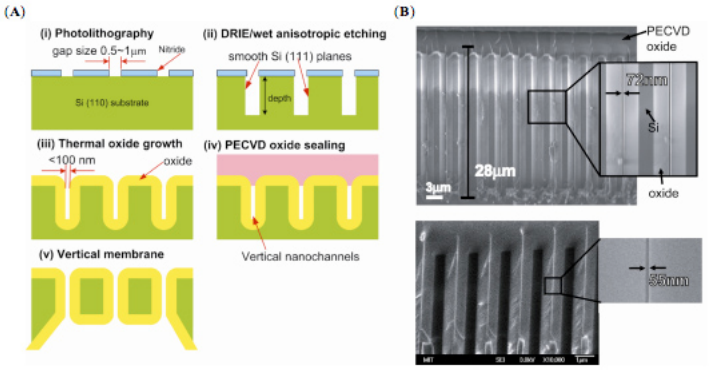
▲ Figure 2: Different sizes and shapes of glycine crystals produced in reactor channel.

Massively-parallel Ultra-high-aspect-ratio Nanochannels for High-throughput Biomolecule Separation

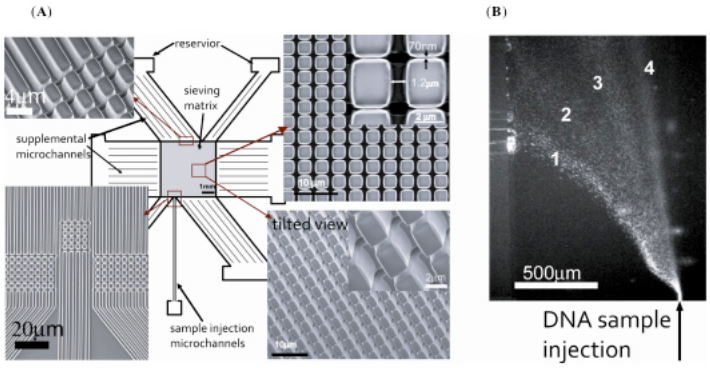
P. Mao, J. Han

Sponsorship: KIST IMC, NIH

Many bottom-up approaches have been used to build nano/mesoporous materials/filters with a good size control, but the integration of these systems into a microsystem format has been a challenge. Top-down nanofilter fabrications, on the other hand, suffered from small open volume and low throughput. For this paper, we developed a top-down fabrication strategy for massively-parallel, regular vertical nanochannel membranes with a uniform, well-controlled gap size of ~50 nm and a depth up to ~40 μm, by using only standard semiconductor fabrication techniques [1]. The vertical nanofilter membranes were fabricated into an anisotropic nanofilter array, which demonstrates the ability to integrate nanofilters and micron-sized channels/pores seamlessly. We demonstrated efficient continuous-flow separation of large DNAs in a two-dimensional vertical nanochannel array device as shown in Figure 2. Compared with planar nanofilter systems [2], an important feature of our device is a sample processing rate as high as ~ 1 μL hour^{-1}, and further improvement of throughput can be achieved simply by upscaling the channel depths. These ultrahigh-aspect-ratio nanochannels have the advantage of large open volume, enabling high-throughput applications.



▶ Figure 1: (A) Schematic diagram of fabricating massively-parallel vertical nanofluidic channels. (B) Cross-sectional SEM micrograph of slit-like vertical nanochannels with a uniform gap size of 72 nm and 55 nm. The channels are etched by KOH etching and have a depth of 28 μm. The channels are completely sealed by depositing 3-μm-thick PECVD oxide.



▶ Figure 2. Continuous fractionation of long DNAs through the two-dimensional anisotropic pillar array device. (A) The device includes a sieving matrix and surrounding microfluidic channels. The pillar array consists of horizontal nanochannels with a width of 70 nm and longitudinal channels with a width of 1.2 μm. Supplemental microchannels connecting sieving matrix and reservoirs are 1.5 μm in width. They are all 15 μm deep. (B) Fluorescence micrographs show separation of the mixture of λ-DNA Hind III digest. Electrical fields applied both in horizontal and longitudinal directions in sieving matrix are 80 V cm^{-1} and 30 V cm^{-1}, respectively. Band assignment: (1) 23.13 kbp; (2) 9.4 kbp; (3) 6.58 kbp; (4) 4.36 kbp.

References

[1] P. Mao and J. Han, "High-throughput continuous-flow separation of biomolecules in a high-aspect-ratio nanofilter array," in *Proc. Biomedical Engineering Society Annual Fall Meeting*, Chicago, IL, 2006.

[2] J. Fu, R.B. Schoch, A.L. Stevens, S.R. Tannenbaum, and J. Han, "A patterned anisotropic nanofluidic sieving structure for continuous-flow separation of DNA and proteins," *Nature Nanotechnology*, vol. 2, pp. 121-128, 2007.

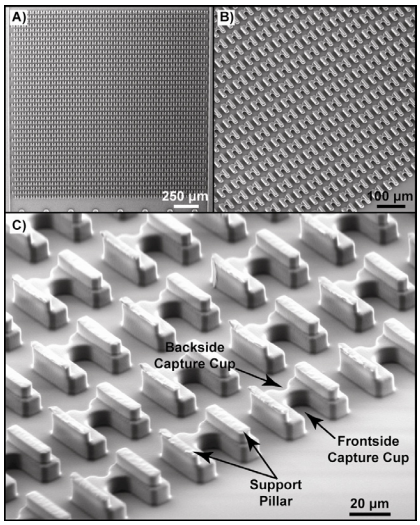
Microfluidic Control of Cell Pairing and Fusion

A. Skelley, J. Voldman
Sponsorship: NIH

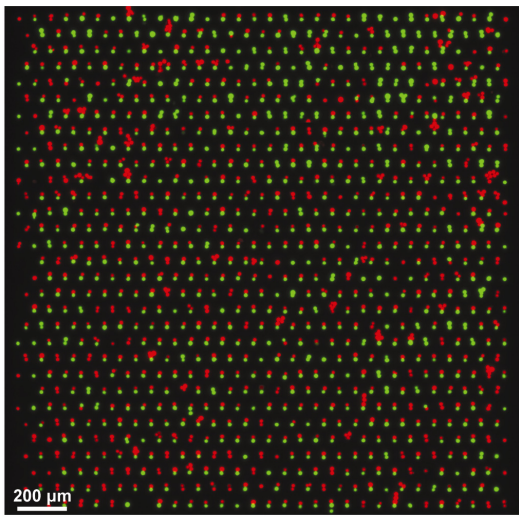
Currently, several different methods have been used to reprogram somatic cells to an embryonic stem cell-like state. Nuclear transfer and fusion methods [1] use either oocytes or embryonic stem cells (ESCs) as a source of reprogramming factors. Recently, defined factors have been identified that are capable of inducing pluripotency in somatic cells[2] [2]. While all three approaches can be used successfully for reprogramming, cell lines generated are not yet suitable for potential therapeutic applications in humans and many questions remain about the process of nuclear reprogramming.

We have developed a microfluidic system in which thousands of ESCs and somatic cells (SCs) are properly paired and immobilized, resulting in a high number of one-to-one fusions that can be clearly identified for further studies [3]. The device consists of thousands of cell traps in a millimeter-sized area, accessed by microfluidic channels (Figure 1). The traps consist of larger frontside and smaller backside capture cups made from a transparent biocompatible polymer. Cells are loaded sequentially in a 3-step loading protocol enabling capture and pairing of two different cell types. The geometry of the capture comb precisely positions the two cells, and flow through the capture area keeps the cells in tight contact in preparation for fusion. Pairing efficiencies of ~70% are possible over the entire device (Figure 2).

The device is compatible with both chemical and electrical fusion. The PEG-mediated fusion is initiated by flowing PEG past the cells for 3 minutes and then rinsing with warm media. With 4 doses of PEG, we have observed that 15 % of the traps contain cells that have exchanged fluorescent proteins, and 25 % of the traps contain cells whose membranes have reorganized. A control protocol done in a standard conical tube yielded only 6 ± 4 % fusion of the same fluorescent cells. Electrofusion is made possible by bonding the PDMS device to a glass slide with pre-patterned metal electrodes that are then connected to a standard fusion power supply. We have observed membrane fusion efficiencies up to 90% and can achieve > 50% properly paired and fused cells, based on exchange of fluorescence, over the entire device. Control fusion protocols, performed using the same power supply with a commercial electrofusion chamber, obtained only 11 +/- 9 % fusion. We have demonstrated pairing and fusion of mESCs and mEFs and are currently using the device to explore fusion-based reprogramming.



▲ Figure 1: A PDMS device for cell capture and pairing. (A) The device is 2 mm x 2 mm and contains ~ 1000 cell traps. (B,C) The traps are arrayed densely in the device, and each trap consists of frontside and backside capture cups along with support pillars.



▲ Figure 2: Fluorescent overlay image of red and green fluorescent 3T3 mouse fibroblasts captured and paired in the device. Pairing efficiencies up to ~ 70% are possible.

References

[1] C.A. Cowan, J. Atienza, D.A. Melton, and K. Eggan, "Nuclear reprogramming of somatic cells after fusion with human embryonic stem cells," *Science*, vol. 309, pp.1369-1373, 2005.

[2] K. Takahashi, K. Tanabe, M. Ohnuki, M. Narita, T. Ichisaka, K. Tomoda, and S. Yamanaka, "Induction of pluripotent stem cells from adult human fibroblasts by defined factors," *Cell*, vol. 131, pp. 861-872, 2007.

[3] A.M. Skelley, O. Kirak, R. Jaenisch and J. Voldman, "Studying reprogramming of somatic cells via fusion with embryonic stem cells: A massively parallel device for cell fusion," *MicroTotal Analysis Systems*, vol. 1, pp. 581-582, 2007.

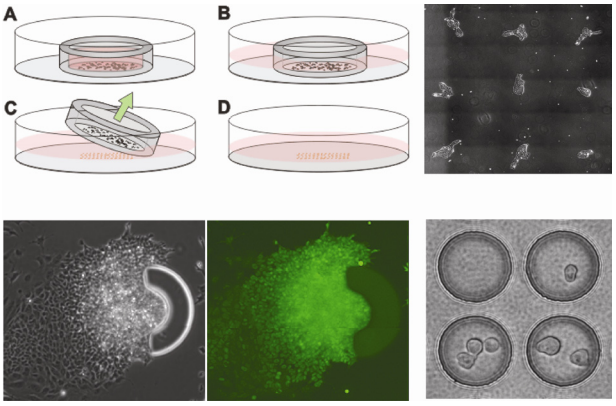
BioMEMS for Modulating Stem Cell Signaling

K Blagović, L.Y. Kim, N. Mittal, L. Przybyla, S. Sampattavanich, J. Voldman
Sponsorship: NIH, NSF Graduate Research Fellowship, SNSF Fellowship for Prospective Researchers

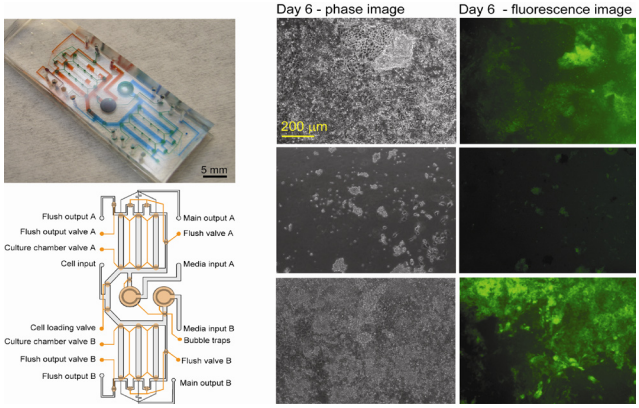
The stem cell microenvironment is influenced by several factors including cell-cell, cell-matrix, and cell-media interactions. Although conventional cell-culture techniques have been successful, they provide incomplete control of the cellular microenvironment. To enhance traditional techniques, we have developed several microscale systems for adherent cell culture of mouse embryonic stem cells (mESCs) while controlling the microenvironment in novel ways [1].

We are using stencil cell patterning and microscopic analytical tools to investigate cell-cell interactions, in particular the role of colony-colony interactions in self-renewal of mESCs. Since autocrine signaling in mESCs has not been thoroughly characterized, we validate our platform using a model autocrine cell line, A431 epidermoid carcinoma cells. By precisely controlling the colony size, spacing, and the medium replenishing frequency, we modulate the degree of colony-colony interactions (Figure 1). We are also using the Bio Flip Chip to investigate cell-cell signaling in mESCs. The chip is made from PDMS using replica molding, and it contains hundreds-to-thousands of microwells, each sized to hold either a single cell or small numbers of cells (Figure 1) [2]. A microscale cellular manipulation technique for cell-matrix interactions involves the patterning of specific protein signals around live mESC colonies in order to study the local effects of signal presentation. A photopolymerizable polymer (PEG-diacrylate) with attached proteins has been used to pattern structures around growing cell colonies in vitro, thereby exposing them to a very controlled microenvironment. Using these methods, we have patterned a known regulator of pluripotency, LIF, around mESC colonies and analyzed how far this signal propagated through the colony (Figure 1).

To control cell-media interactions we have developed a two-layer PDMS microfluidic device that contains two sets of triplicate chambers, allowing implementation of different culture conditions on the same chip. The device incorporates a valve architecture modeled after Irimia et al. [3], which enables different parts of the device to be fluidically isolated during different stages of the experiment. Using our system, we demonstrated that microfluidic perfusion can affect the soluble microenvironment. We showed that defined serum-free media (N2B27), sufficient for differentiating cells into neuronal precursors in static culture [4], did not allow cells to proliferate or differentiate on-chip. On the same chip we cultured cells in N2B27 that had been supplemented with media containing cell-secreted factors from a static culture. In this media, we were able to restore growth and differentiation (Figure 2).



▲ Figure 1: Stencil patterning procedure: A) Load cells. B) Fill dish with media. C) Remove stencil. D) Rinse with medium to remove unattached cells (top, left). Patterned A431 colonies (top, right). PEGDA structures with attached LIF surrounding a mESC colony. Immunostaining is for Oct4, a stem cell pluripotency marker (bottom, left). Bio Flip Chip (bottom, right).



▲ Figure 2: Image of the perfusion device filled with dye to illustrate the different layers (top, left,). Schematic of the device (bottom, left). Images of cells in static N2B27 culture (top, right), in N2B27 on-chip culture (middle, right) and on-chip N2B27 culture supplemented with the media from a static culture (bottom, right). Green fluorescence indicates expression of an early neuronal differentiation marker Sox1.

References

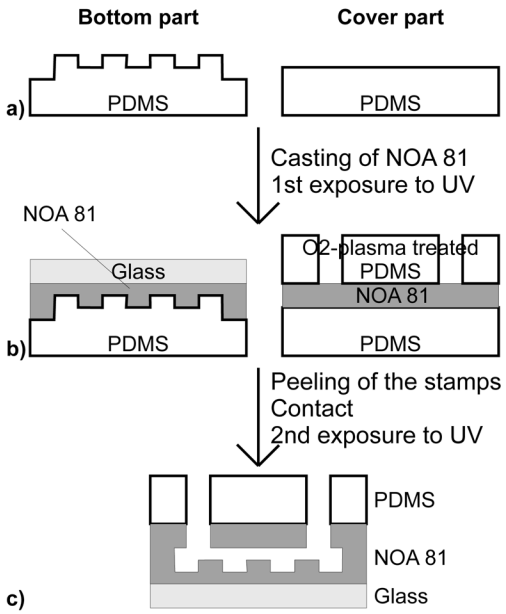
[1] L. Kim, Y.C. Toh, J. Voldman, and H. Yu, "A practical guide to microfluidic perfusion culture of adherent mammalian cells," *Lab on a Chip*, vol. 7, pp. 681-694, June 2007.
[2] A. Rosenthal, A. Macdonald, and J. Voldman, "Cell patterning chip for controlling the stem cell microenvironment," *Biomaterials*, vol. 28, pp. 3208-3216, Mar. 2007.
[3] D. Irimia and M. Toner, "Cell handling using microstructured membranes," *Lab on a Chip*, vol. 6, pp. 345-352, Mar. 2006.
[4] Q.L. Ying, M. Stavridis, D. Griffiths, M. Li, and A. Smith, "Conversion of embryonic stem cells into neuroectodermal precursors in adherent monoculture," *Nature Biotechnology*, vol. 21, pp. 183-186, Feb. 2003.

Microfabricated Slits in Series: A Simple Platform to Probe Differences in Cell Deformability

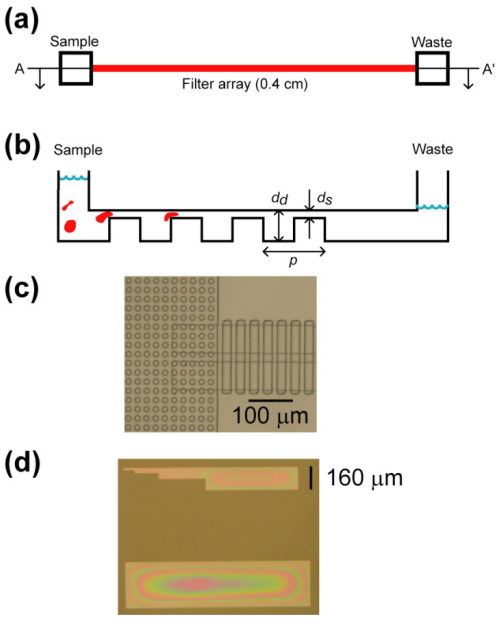
H. Bow, P. Abgrall, J. Han
Sponsorship: Singapore-MIT Alliance

Change in cell stiffness is a characteristic of blood cell diseases, such as sickle cell anemia [1], malaria [2], and leukemia [3]. Often, increases in blood cell stiffness lead to loss of the cells' ability to squeeze through capillaries, resulting in organ failure, coma, and ultimately death [4]. The goal of this project is to create a microfluidic device that can quickly and accurately screen, diagnose, and treat disorders involving cell deformability. We report the creation of a microfabricated device consisting of a series of 1-2 μm wide polymeric slits, as Figures 1 and 2 show. This device can potentially be used to screen and diagnose disorders involving cell deformability.

The device fabrication process is depicted in Figure 1 and follows approaches similar to those in [5]. First, a 2-level negative PDMS stamp was made using soft lithography techniques from a silicon template, Figure 1a. A droplet of UV-sensitive prepolymer NOA 81 was stamped on a glass slide and exposed to UV, Figure 1b. Similarly, a droplet of NOA was stamped using a flat PDMS slab and exposed to UV on a PDMS cover sheet treated with oxygen plasma to improve the adhesion. After the stamps were peeled off , the two pieces were brought in contact and bonded by completing the crosslinking with a second exposure to UV, as in Figure 1C. Figure 1 details the device's operation and results of fabrication.



▲ Figure 1: Fabrication details.



▲ Figure 2: (a) Device schematic. (b) Cross-section through A-A'. (c) Picture from top of actual device near entrance. (d) Test structures indicating 2-μm-deep features with aspect ratio of up to 2/320 did not collapse.

References

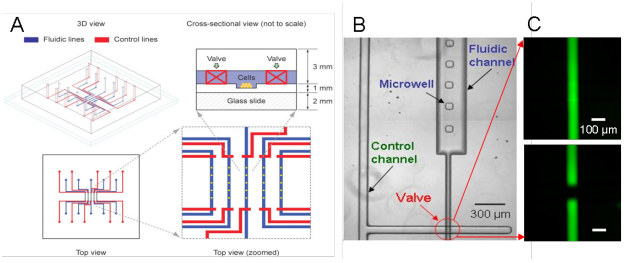
[1] E. Evans, N. Mohandas, and A. Leung, "Static and dynamic rigidities of normal and sickle erythrocytes," *Journal of Clinical Investigation*, vol. 73, pp. 477-488, 1984.
[2] J.P. Shelby, J. White, K. Ganesan, P.K. Rathod, and D. Chiu, "A microfluidic model for single-cell capillaryobstruction by plasmodium falciparum-infected erythrocytes," *Proc. National Academy of Sciences*, vol. 100, no. 25, pp. 14618-14622, 2003.
[3] M.J. Rosenbluth, W.A. Lam, and D.A. Fletcher, "Force microscopy of nonadherent cells: A comparison of leukemia cell deformability," *Biophysical Journal*. vol. 90, pp. 2994-3003, 2006.
[4] V. Kumar, A.K. Abbas, and N. Fausto, *Robbins and Cotran Pathologic Basis of Disease*, Philadelphia: Saunders, 2004.
[5] S.H. Kim, Y. Yang, M. Kim, S.W. Nam, K.M. Lee, N.Y. Lee, Y.S. Kim, and S. Park, "Simple route to hydrophilimicrofluidic chip fabrication using an ultraviolet (Uv)-cured polymer," *Advanced Functional Materials*. vol. 17, no. 17, pp. 3493-3498, Nov. 2007.

Microfluidic System for Screening Stem Cell Microenvironments

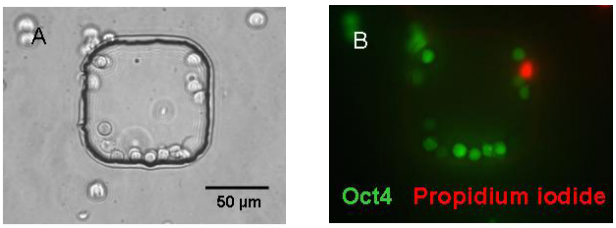
W.G. Lee, B.G. Chung, A. Khademhosseini
Sponsorship: NIH, CIMIT

Embryonic stem cell (ESC) differentiation is a potentially powerful approach for generating a renewable source of cells for regenerative medicine. It is known that the microenvironment greatly influences ESC differentiation and self-renewal. Most biological studies have aimed at identifying individual molecules and signals. However, it is becoming increasingly accepted that the many kinds of signals in the ESC microenvironment interact in a synergistic and antagonistic manner based on their temporal and spatial expression, dosage, and specific combinations. This interplay of microenvironmental factors regulates the ESC fate decisions to proliferate, self-renew, differentiate, and migrate. Despite this complexity, the systematic study of stem cell cues is technologically challenging, expensive, slow, and labor-intensive. Here we propose to develop a high-throughput microfluidic based system that overcomes many of these challenges. We will subsequently analyze the resulting high-throughput system in elucidating specific aspects of mesodermal and endodermal differentiation in a systematic manner.

A simple microfluidic screening device consisted of fluidic channels, control channels, and poly(ethylene glycol) (PEG) microwells has been developed (Figure 1). A microfluidic screening device was fabricated by multi-layer soft lithography technique [1]. The fluidic channel made by positive photoresist (AZ 4620) is 10-μm-thick pattern with a round shape and the pneumatically actuated control channel fabricated by negative photoresist (SU-8 2150) is a 40-μm-thick pattern. To obtain a round profile of a fluidic channel, the positive photoresist (AZ 4620) was reflowed at 200°C for 120 sec after development. A replica of the fluidic channel was obtained by spin-coating poly(dimethylsiloxane) (PDMS) at 1700 rpm for 1 min followed by baking at 70 °C for 1.5 hours. This process resulted in a 20-μm-thick PDMS membrane containing the fluidic channel. The crossing of the control channel over the fluidic channel formed the on-chip barrier valve. We used ES-green fluorescent protein (GFP) cells that can express Octamer-4 (Oct4), a homodomain transcription factor. The ES-GFP cells were seeded into a fluidic channel and localized within PEG microwells in a flow-based microfluidic screening device (Figure 2). The ES cells were well docked and patterned within a microwell, while cells that were not localized within a microwell were flowed into a reservoir. The ES cells expressed by Oct4 (green) maintained self-renewal during media perfusion (0.3 μl/min). The ES cells docked within a microwell showed high cell viability (> 90%).



▲ Figure 1: A simple microfluidic screening device. (A) Schematic design of a microfluidic device. (B) Phase contrast image of a microfluidic screening device integrated with fluidic channel, control channel, and PEG hydrogel microwell (100×100 μm). (C) Actuation of on-chip valve. FITC-dextran images in a fluidic channel as valve is opened and closed.



▲ Figure 2: Cell viability of mouse ES cells exposed to media for 2 hours in a microfluidic screening device. ES cells were expressed by Oct-4 (green) and dead cells (red) were indicated by propidium iodide.

Reference

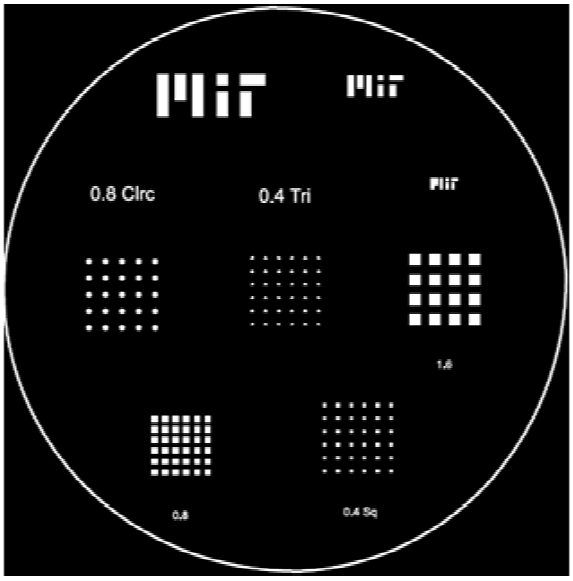
[1] B.G. Chung, F. Lin, and N.L. Jeon, "A microfluidic multi-injector for gradient generation," *Lab on a Chip*, vol. 6, no. 6, pp. 764-768, June 2006.

Self-assembly of Cell-laden Microgels with Defined 3D Architectures on Micro-patterned Substrate

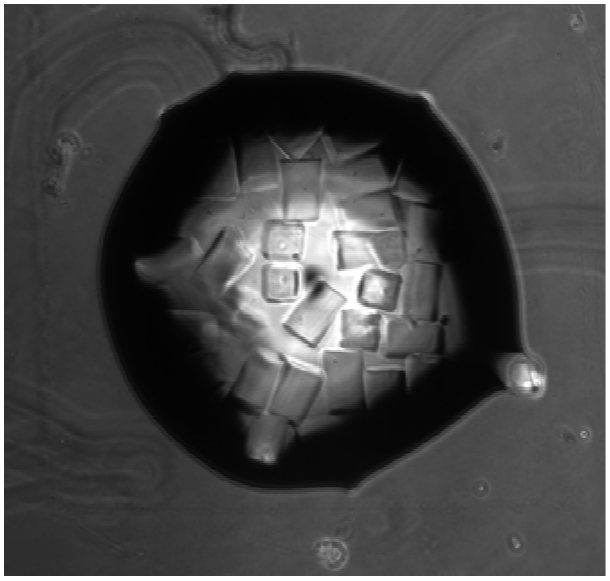
Y. Du, A. Khademhosseini
Sponsorship: NIH, CIMIT

Most living tissues are composed of repeating units on the scale of hundreds of microns; these units are ensembles of different cell types with well-defined three-dimensional (3D) microarchitectures and tissue-specific functional properties (i.e., islet, nephron, or sinusoid) [1]. To generate engineered tissues, the recreation of these repeating structural features is of great importance in enabling the resulting tissue function. Here, we tried to self-assemble cell-laden microscale hydrogel (microgel) units as 3D tissue constructs with defined architecture by using hydrophobic/hydrophilic interactions. By micro-contact printing [2], we patterned the glass slides with specific hydrophobic and hydrophilic regions [3]. We hypothesized that the hydrophilic microgels tend to stick to the hydrophilic patterns, while not on the hydrophobic patterns. Therefore, we could control the architecture of the microgel assembly by creating different hydrophilic patterns.

To achieve microcontact printing, we first created different SU 8 patterns on the silicon wafer based on the photomask by using standard photolithography. The SU 8 patterns were transferred to the PDMS mold, which was soaked with the hydrophobic ink. The ink was printed with specific patterns on the glass slide by microcontact printing. Afterwards, the slides were covered in DPBS (~600 μL of DPBS) containing microgels (approximately 1500 gel units each patterned slide). After a few minutes, the slides were tilted over, to allow the liquid to drain off the slide. Microgels remained on only the hydrophilic glass surfaces, as predicted. Below are images of microgel assembly on a 1600-um square pattern on the glass slide.



▲ Figure 1: Photomask containing various patterning designs.



▲ Figure 2: Phase-contrast image of self-assembled microgel building blocks on a hydrophilic pattern.

References

[1] L. Costanzo, *Physiology (3rd edition)*. Philadelphia: Saunders, 2006.
[2] L. Lauer, C. Klein, and A. Offenhausser, "Spot compliant neuronal networks by structure optimized micro-contact printing," *Biomaterials*, vol. 22, pp. 1925-1932, July 2001.
[3] E. Kokkoli and C.F. Zukoski, "Interaction forces between hydrophobic and hydrophilic self-assembled monolayers," *Journal of Colloid Interface Science*, vol. 230, pp. 176-180, Oct. 2000.

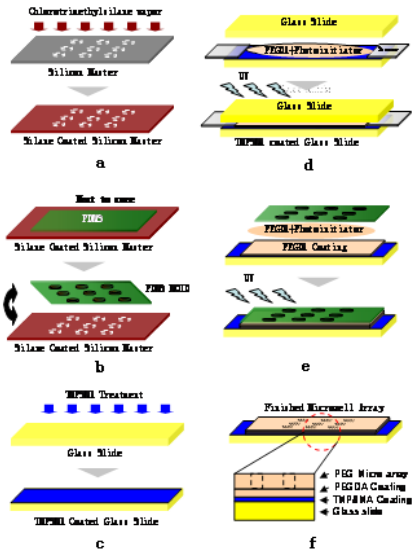
High-throughput Study of Cell-ECM Interactions in 3D Environment Using Microwell Arrays

L. Kang, J. Shim, S. Lee, A. Khademhosseini

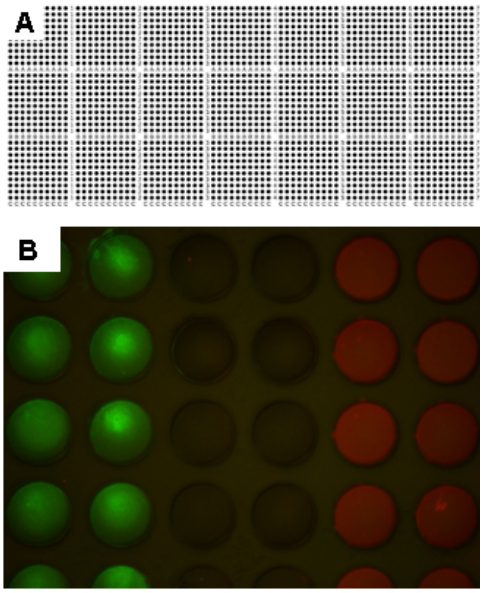
Sponsorship: NIH, CIMIT

The extracellular matrix (ECM) is critical in developing an integrated picture of the role of the microenvironment in the fate of many cells. A two-dimensional (2D) microarray method was reported for cell-ECM interaction study [1]. These 2D approaches can be complemented by three-dimensional (3D) approaches such as embedding cells within ECM gels [2]. However, 3D microarray methods are difficult to develop due to difficulties such as ECM array fabrication and nanolitre liquid handling. To overcome these difficulties, microwell array and robotic spotting may be useful.

In this study, we develop an approach using a microarrayer (Piezorray) and microwell arrays for cell-ECM interaction study with high throughput. The microwell array was fabricated with soft lithography (Figure 1). The diameter of a microwell was 400 μm with a pitch of 600 μm. In total, 2100 microwells were fabricated on a single slide with numbers and alphabets in between for identification (Figure 2A). As a proof-of-concept experiment, it was shown that dye solutions can be printed accurately into these microwells preloaded with collagen solution (Figure 2B). For future study, we will print the ECM component in a combinatorial manner into the microwell array preloaded with cells in prepolymer solutions. Then, the mixtures will be UV-crosslinked to immobilize the ECM mixture inside each isolated microwell for cell-ECM interaction study.



▲ Figure 1: The schematic representation of fabricating a microwell array containing 2100 microwells on a single glass slide.



▲ Figure 2: A) The layout of the microwell array. B) FITC-BSA (green) and Rhodamine-dextran (red) dyes were printed into the microwells using a microarrayer (well diameter = 400μm).

References

[1] C.J. Flaim, S. Chien, and S.N. Bhatia, "An extracellular matrix microarray for probing cellular differentiation," *Nature Methods*, vol. 2, pp. 119–125, Jan. 2005.

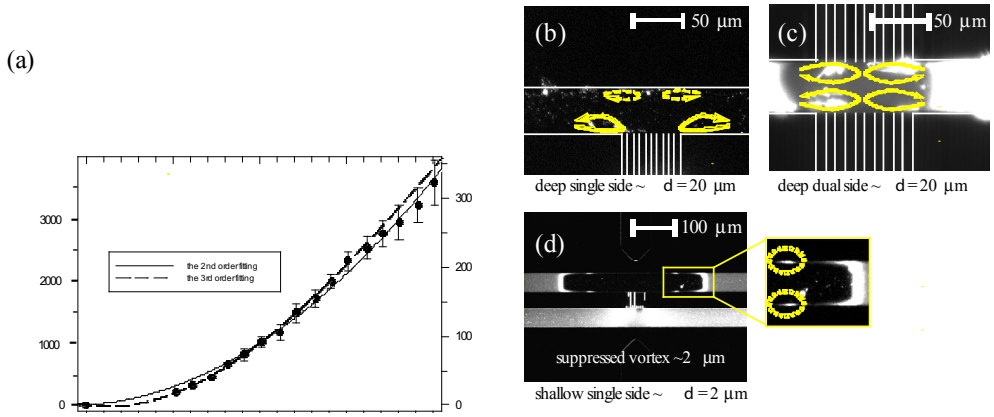
[2] M.Y., Lee, R.A. Kumar, S.M. Sukumaran, M.G. Hogg, D.S. Clark, and J.S. Dordick, "Three-dimensional cellular microarray for high-throughput toxicology assays," *Proceedings of the National Academy of Sciences*, vol. 105, pp. 59-63, Jan. 2008.

Amplified Electrokinetic Response by Concentration Polarization near Nanofluidic Channel

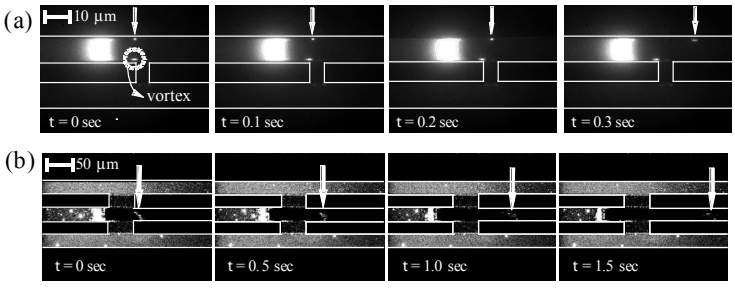
S.J. Kim, J. Han

Sponsorship: NIH

Due to a strong electrokinetic response inside an ion-depletion region created by concentration polarization, **the velocity of non-equi**librium electroosmotic flows (EOF) inside the ion-depletion zone can be 10 times faster than any equilibrium EOFs. **[1, 2] Fast fluid** vortices were generated at the anodic side of the nanochannel due to the non-equilibrium EOF. The vortex flow speed was estimated to be usually about 1000 μm/sec, which is about ~10X higher than that of primary EOF under the same electrical potential, and was proportional to the square of applied voltage, as shown in Figure 1(a). At the steady state, we can clearly observe the two counter-rotating vortices beside the nanochannel, as Figure 1(b) shows. In the dual-sided nanochannel device, since the ions were depleted through both walls, the four independent vortices were formed in the four divided regions, as shown in Figure 1(c). One can independently suppress the convective part of the phenomena by decreasing the microchannel thickness. As Figure 1(d) shows, the size of the vortex in the dotted circle was approximately 2μm, which corresponded to the depth of the microchannels. We also observed that, once the particles pass the depletion zone and entered the downstream low concentration zone, they travel 25 times faster than in the buffer zones, as Figure 2 shows. These results indicate that the concentration polarization (depletion) can be utilized to make efficient and novel electrokinetic pumps and fluid switching devices, at an efficiency that has never been demonstrated.



▲ Figure 1: (a) The translational and angular speed of the vortex as a function of applied voltage. The speed was 10 times or even higher than equilibrium EOFs. The data was fitted by the second order polynomial to reveal the proportionality to $|E|^2$. (b) A fast vortex at steady state in single-sided nanochannel device. (c) Four independent strong vortices in dual-sides nanochannel device. (d) Suppressed vortices in a shallow single-sided nanochannel device.



▲ Figure 2: The electrokinetic migration of charged particles in (a) single-sided and (b) dual-sided nanochannel devices. Estimated velocity of pointed particles was approximately (a) 140 μm/sec and (b) 500 μm/sec at E_T =5V/cm.

References

[1] S.J. Kim, Y.C. Wang, J.H. Lee, H. Jang, and J. Han, "Concentration polarization and nonlinear electrokinetic flow near a nanofluidic channel," *Physical Review Letters*, vol. 99, no. 4, pp. 044501:1-4, July 2007.

[2] A. Holtzel, and U. Tallarek, "Ionic conductance of nanopores in microscale analysis systems: Where microfluidics meets nanofluidics," *Journal of Separation Science*, vol. 30, no. 10, pp. 1398-1419, July 2007.

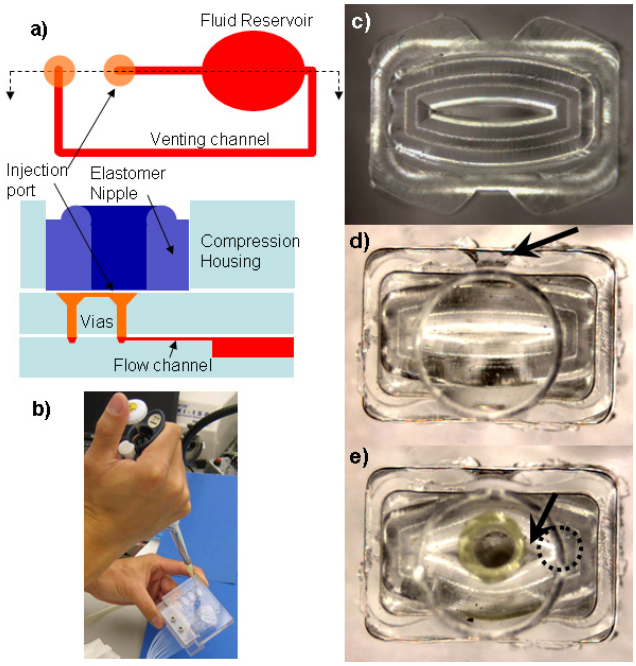
Micropipette Interfaces for Lab-on-a-Chip Systems

H. Lee, R.J. Ram, P. Boccazzi, A. Sinskey
Sponsorship: Lincoln Laboratory

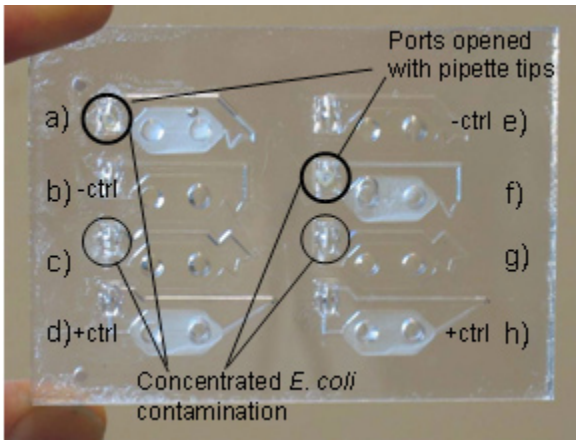
We have developed a simple to use, pipette-compatible, integrated fluid injection port to interface closed microfluidic chambers for applications such as cell culture or microchamber PCR that are sensitive to external contamination. In contrast to open systems where fluid can be easily loaded into wells or flow-through microfluidic systems where interfacing involves bridging millimeter scale tubing with micrometer scale channels [1], filling closed chambers requires either first applying vacuum or venting the chamber. We have fabricated a pipette interface that automatically vents and seals upon insertion and removal of a pipette tip that can be directly integrated into fluidic devices.

The injection port is composed of a deformable elastomer nipple, compression housing, and flow and vent channels that interface with the fluid chamber. A schematic of the components is shown in Figure 1a and photographs are shown in Figures 1b through 1e. When the elastomer nipple (Figure 1c) is inserted in the compression housing (Figure 1d), the slit of the elastomer nipple is sealed closed, isolating the fluidic chamber from the external environment. Insertion of the pipette tip into the slit (Figure 1e) causes the nipple to deform, which opens the venting channel to the air while the pipette tip seals against the fluid flow channel. Actuation of the pipette plunger forces fluid into the chamber while air is vented around the pipette tip. Removing the tip reseals the port to prevent external contamination. The seal can withstand at least 15psi of backpressure.

The integrity of the injection port seal against bacterial contamination was tested using the device shown in Figure 2, which comprised eight closed chambers of 150µL in volume interfaced with an integrated injection port. By visual inspection and plating, the sealed ports prevented contamination while the negative controls were clearly contaminated.



▲ Figure 1: a) Top and cross-section schematic representation of injection port. b) Photograph demonstrating fluid injection into a closed fluid reservoir using standard pipette. c) Elastomer nipple. d) Elastomer nipple inserted into compression housing. Arrow highlights open region to allow deformation upon pipette tip insertion. e) Port with 200uL pipette tip inserted. Arrow highlights opening in slit around the pipette where air is vented. Dotted circle outlines underlying vent port.



▲ Figure 2: Photograph of contamination test device. Eight 150-uL reservoirs are each interfaced with an integrated fluid injection port. A 70-um-thick PDMS membrane covers the reservoir to allow oxygenation. Reservoirs were prepared and then incubated for 24 hours at 37°C.

Reference

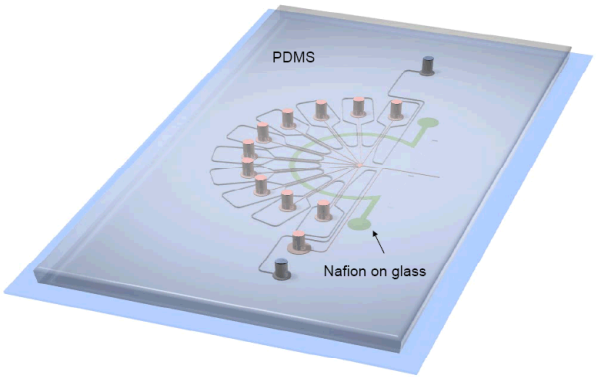
[1] C.K. Fredrickson and Z.H, Fan, "Macro-to-micro interfaces for microfluidic devices," *Lab on a Chip*, vol. 4, pp. 526-533, Apr. 2004.

Multiplexed Proteomic Sample Preconcentration Chip Using Surface-patterned Ion-selective Membrane

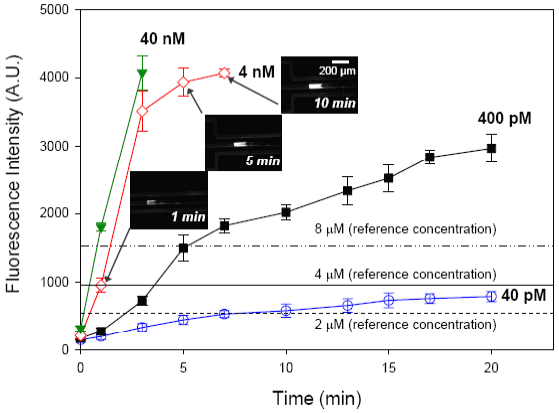
J.H. Lee, Y.-A. Song, J. Han

Sponsorship: NIH grants R01-EB005743 and P30-ES002109-28 (MIT CEHS)

We report a new method of fabricating a high-throughput protein preconcentrator in poly(dimethylsiloxane) (PDMS) microfluidic chip format. We print a submicron-thick ion-selective membrane on the glass substrate by using standard patterning techniques. By simply plasma-bonding a PDMS microfluidic device on top of the printed glass substrate, we can integrate the ion-selective membrane into the device and rapidly prototype a PDMS preconcentrator without complicated microfabrication and cumbersome integration processes. The PDMS preconcentrator showed a high preconcentration efficiency with a factor as high as ~10^4 in just 5 min., which was 12x higher than our previous PDMS preconcentrator fabricated by junction gap breakdown [1]. Moreover, we have demonstrated a fabrication of 10 single preconcentrators in an array format which increased the preconcentrated volume by 3 orders of magnitude compared to our previous result obtained with the silicon nanofluidic preconcentrator [2]. The ability to build a massively parallel array using this technique is significant in terms of the integration of our preconcentrator to an external sensing unit such as mass spectrometer. In addition to a shorter preconcentration time, the array can offer a sufficient amount of the concentrated sample volume to transfer it to an external sensing unit. Due to this capability, we expect a high potential of our PDMS preconcentrator chip as a signal enhancement tool for a mass spectrometer to detect low-abundance proteins and peptides. Furthermore, the PDMS microfluidic format of this device would allow the integration of preconcentrator into many different BioMEMS platforms, including cellular BioMEMS devices.



▲ Figure 1: Schematic of 10 array preconcentrators using integration of ion-selective membrane into PDMS preconcentrator by plasma bonding.



▲ Figure 2: Preconcentration of β-Phycoerythrin protein versus electrokinetic trapping time. This result shows that we can achieve a preconcentration factor of ~10^4 in 5 min. Fluorescence images of 4 nM protein shown next to the graph indicate an increase of the concentrated plug in size and concentration with trapping time.

References

[1] J.H. Lee, S. Chung, S.J. Kim, and J. Han, "Poly(dimethylsiloxane)-based protein preconcentration using a nanogap generated by junction gap breakdown," *Analytical Chemistry*, vol. 79, no. 17, pp. 6868-6873, Sept. 2007.

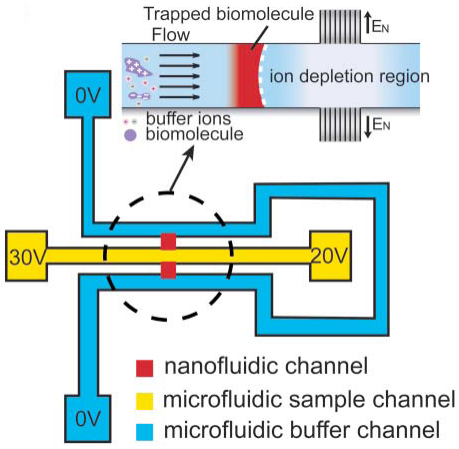
[2] Y.C. Wang, A.L. Stevens, and J. Han, "Million-fold preconcentration of proteins and peptides by nanofluidic filter," *Analytical Chemistry*, vol. 77, no. 14, pp. 4293-4299, July 2005.

Improving the Sensitivity and Binding Kinetics of Surface-based Immunoassays

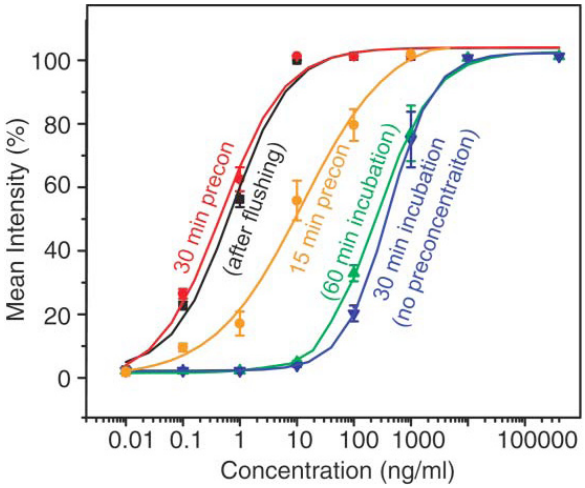
V. Liu, Y.-C. Wang, J. Han
Sponsorship: NIH

Immunoassays are currently among the most widely used diagnostics tools in the healthcare industry. The usage of current immunoassays is limited by the availability of good antigen-antibody pairs, time-consuming incubation, and sensitivity limits. In particular, the sensitivity and binding kinetics are limited by the usually low concentration of molecules that we are trying to detect. One of the most common methods to overcome the limitations of sensitivity is by adding a post-binding amplification step, meaning that signals get enhanced after molecules are bound to capture antibodies. This method helps improve the sensitivity of the assay, but it fails to reduce the time required for the sensor to reach an equilibrium value because the low concentration of molecules still takes the same time to saturate the sensor. An alternative to post-binding amplification is pre-binding amplification. By increasing concentration of molecules of interest prior to their capture by antibodies, pre-binding amplification improves both the sensitivity of the sensor and kinetics of binding.

Our lab has developed and integrated a nanofluidics-based concentrator and has successfully integrated the device with an immunoassay [1]. The principle behind the concentrator, electrokinetic trapping, is a space-charge induced phenomenon that can be fine-tuned using external voltage controls. After application of appropriate voltages, a charge-depletion zone forms near the nanochannels and excludes all charged species. If the analyte-containing fluid is continuously moved into this zone, the analytes would accumulate and their concentration increase (Figure 1). The concentrator can be combined with an on-chip assay for improved assay sensitivity. In our lab, a 1,000-fold increase in sensitivity of assays has been demonstrated with fluorescent proteins in simple buffers (Figure 2). Currently, efforts are underway to adapt the system for use with non-natively fluorescent proteins in a more complex background such as serum. Development of a surface-coating method and a pre-concentration scheme for non-natively fluorescent proteins is currently the main focus of this project.



▲ Figure 1: A schematic diagram of the concentrator and operating principles.



▲ Figure 2: Graph showing increase in sensitivity with pre-binding amplification.

Reference

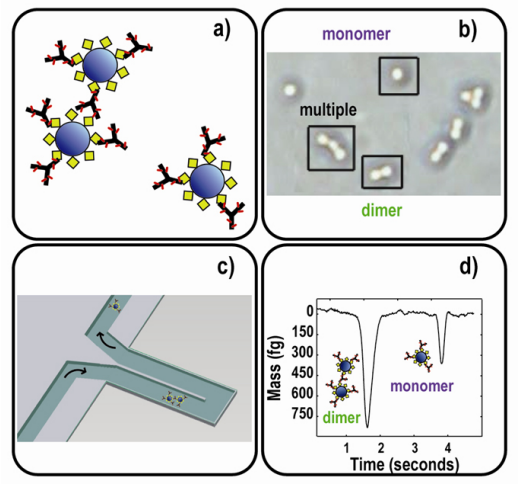
[1] Y.-C. Wang and J. Han, "Pre-binding dynamic range and sensitivity enhancement for immuno-sensors using nanofluidic preconcentrator," *Lab on a Chip*, vol. 8, no. 3, pp. 392-394, Mar. 2008.

Mass-based Readout for Agglutination Assays

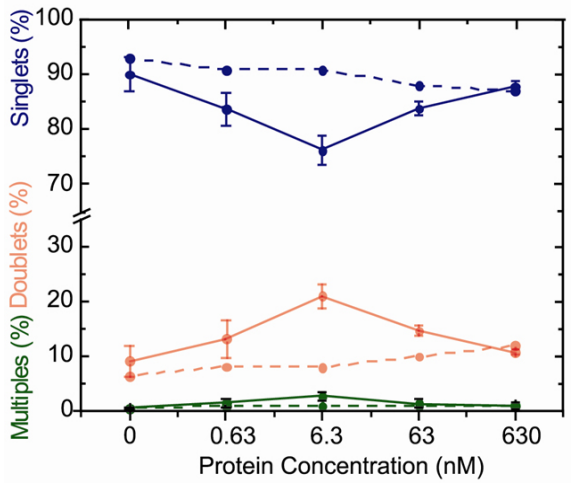
R. Chunara, M. Godin, S.M. Knudsen, S.R. Manalis
Sponsorship: ARO, NIH

Agglutination assays based on nanometer- and micrometer-sized particles were originally inspired by natural agglutination of cells [1] and provide a simple, rapid means for diagnostic testing. There are several commercial examples of agglutination assays used for clinical diagnostics applications. These assays are typically straightforward to administer and provide fast response times. Techniques for measuring agglutination include turbidity, dynamic light scattering, and UV – Vis spectroscopy. In some cases, particle-counting techniques such as flow cytometry and image analysis can improve sensitivity by quantifying small aggregates that are produced during the initial stages of aggregation, allowing a reduction of the required incubation times. Additionally, particle-counting enables gathering of more specific information about the agglutination distribution in a population, rather than reliance on the average agglutination information typically obtained by ensemble measurement techniques. Furthermore, microfluidic approaches for particle-counting can reduce the required sample volume from milliliters to microliters and enable integration with sample treatment steps.

We have developed a non-optical alternative for particle counting in which early-stage aggregation is quantified by measuring mass with the suspended microchannel resonator (SMR) [1]. In SMR detection, each aggregate is weighed in real-time by measuring transient changes in resonant frequency as it flows through the vibrating microchannel (Figure 1). Using a model system of streptavidin-functionalized microspheres and biotinylated antibody as the analyte, we obtain a dose-response curve showing particle agglutination over a concentration range of 630 pM to 630 nM (Figure 2). We show that the results are comparable to what has been previously achieved by image analysis and conventional flow cytometry.



▲ Figure 1: a) Streptavidin (SA)-coated microspheres are incubated with the capture protein (SA is illustrated by diamonds). The analyte (biotinylated antibody) creates agglutination by binding to two different SA receptors located on separate microspheres. b) Optical micrograph of monomer, dimer, and multimer structures that are formed by agglutination of 0.97 μm SA microspheres with 0.63 nM of analyte. c) Schematic of the suspended microchannel resonator (SMR) for counting aggregates by weighing them one at a time. The resonance frequency of the SMR is sensitive to the presence of particles whose mass density differs from that of the solution in the microfluidic channel. d) The SMR is used to classify a monomer (right) and a dimer (left); it classifies anything larger as a multimer (not shown). The transient frequency shift from each structure is converted to a mass by using a calibration factor and accounting for the buffer density.



▲ Figure 2: Mass-based dose response curve obtained by weighing aggregates with the SMR. Each data point represents the mean obtained from three experiments, and at 0.63 nM, five experiments. The dependence of structure proportion is shown versus analyte concentration (biotinylated antibody in solid lines and pure antibody in dashed lines). Each data point represents the mean percentage of structures obtained from three separate experiments at each concentration. In each experiment approximately 2000 aggregates were weighed, and error bars represent the standard deviation from the mean.

Reference

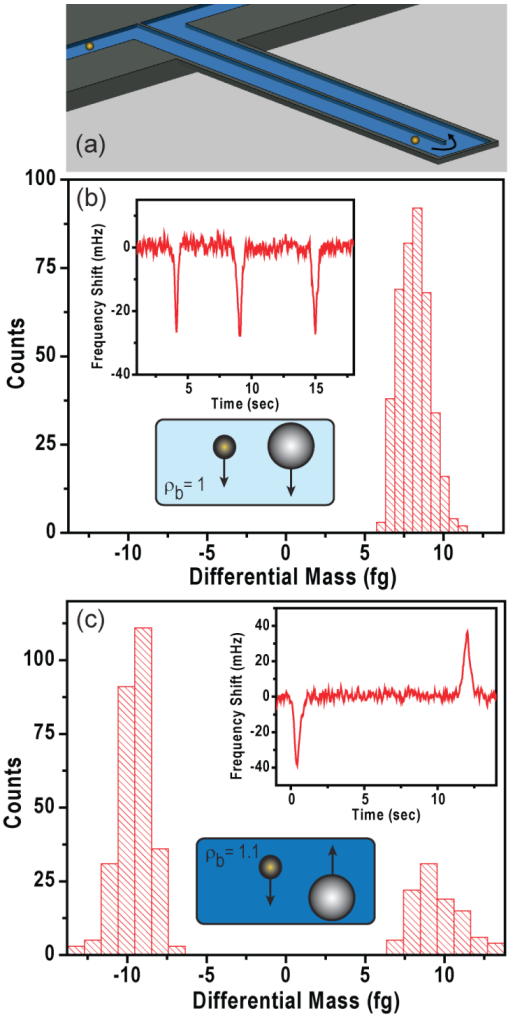
[1] R. Chunara, M. Godin, S.M. Knudsen, and S.R. Manalis, "Mass-based readout for agglutination assays," *Applied Physics Letters*, vol. 91, no.19, pp. 193902:1-3, Nov. 2007.

Measuring the Mass, Density, and Size of Particles and Cells Using a Suspended Microchannel Resonator

M. Godin, A.K. Bryan, T. Burg, S.R. Manalis
Sponsorship: ARO

Nano- and micro-scale particles and colloidal solutions are central to numerous applications in industrial manufacturing, nanotechnology, and the life sciences. We demonstrate the measurement of mass, density, and size of cells and nanoparticles using suspended microchannel resonators (SMRs) [1]. The masses of individual particles are quantified as transient frequency shifts while the particles transit a microfluidic channel embedded in the resonating cantilever. Mass histograms resulting from these data reveal the distribution of a population of heterogenously sized particles. Particle density is inferred from measurements made in different carrier fluids, since the frequency shift for a particle is proportional to the mass difference relative to the displaced solution (Figure 1). We have characterized the density of polystyrene particles, Escherichia coli and human red blood cells with a resolution down to 10-4 g/cm3.

The SMR's particle measurement capabilities are a valuable complement to light scattering and other particle sizing methods currently used in numerous industrial and research applications. Of particular note is the SMR's ability to directly measure the mass/density of individual particles with high precision and accuracy. These capabilities provide a counterpoint to optical "ensemble" techniques such as laser diffraction, which are sensitive to the shape and optical properties of the target particles, and which for some samples are prone to artifacts and irreproducibility. In its current incarnation, the SMR excels for particles from ~ 50 nm to ~ 10 μm. Future improvements in mass resolution may allow measurement of particles down to the ~10-nm scale. The SMR's ability to measure particle density is unique among particle size analyzers and may be applied to applications such as the measurement of porosity and capacity of drug-loaded microspheres; the characterization of engineered porous silica used in coatings, slurries, and optoelectronics; and examination of the structure of submicron-sized particles.



◀ Figure 1: (a) Particles flow through the suspended microfluidic channel contained within the resonating cantilever (the channel is completely enclosed within the beam). (b) A mixture of 99.5 nm gold and 708.6 nm polystyrene nanoparticles is measured in PBS. The differential mass of both particles is positive and the mass histograms overlap. The inset shows the time course of the frequency signal as particles flow through the device, but no peak can be assigned to either gold or polystyrene. The schematic indicates that both particles have a positive differential mass since their densities are larger than that of the surrounding fluid. (c) The differential mass of gold in a 44% glycerol/H2O solution remains positive, but it is negative for polystyrene, as immediately discerned from the time course data shown in the inset. The two histograms are now clearly distinct.

Reference

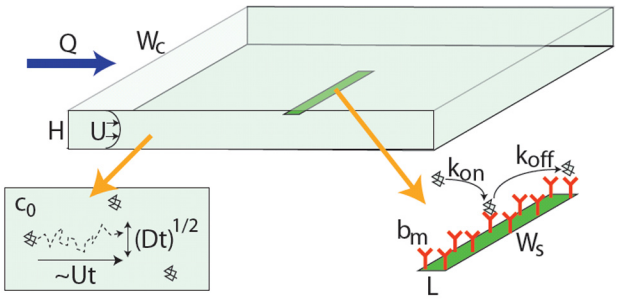
[1] M. Godin, A.K. Bryan, T. Burg, and S.R. Manalis, "Measuring the mass, density and size of particles and cells using a suspended microchannel resonator," *Applied Physics Letters*, vol. 91, no. 12, pp. 123121:1-3, Sept. 2007.

Making it Stick: Convection, Reaction and Diffusion in Surface-based Biosensors

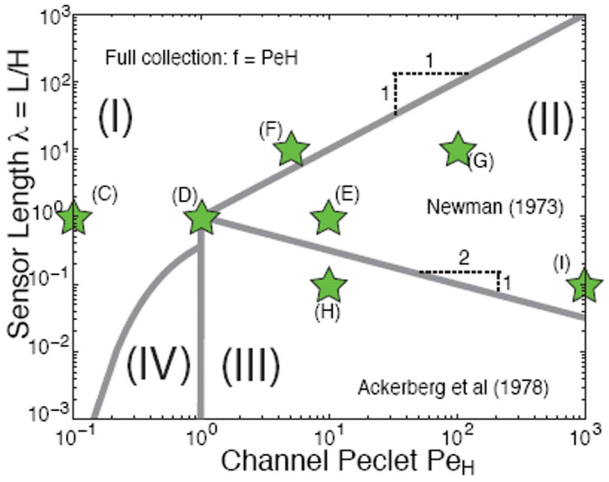
T.M. Squires, R.J. Messinger, S.R. Manalis
Sponsorship: NIH

The past decade has seen researchers from a diverse range of disciplines develop and apply novel technologies for biomolecular detection, at times approaching hard limits imposed by physics and chemistry. In nearly all types of biomolecular sensors, the diffusive and convective transport of target molecules to the sensor can play as critical a role as the chemical reaction itself in governing binding kinetics and, ultimately, performance. This is particularly true as ever-smaller sensors are developed to interrogate ever-more-dilute solutions. Yet rarely does an analysis of the interplay between diffusion, convection and reaction motivate experimental design or data interpretation.

We have developed a physically intuitive and practical understanding of analyte transport for researchers who develop and employ biosensors based on surface capture [1]. Using a model sensor embedded within a microfluidic channel (Figure 1), we explore the qualitatively distinct behaviors that can result (Figure 2), develop rules of thumb to quickly determine how a given system will behave, and derive scaling relations that give order-of-magnitude estimates for fundamental quantities of interest, such as fluxes, collection rates, and equilibration times. We pay particular attention to collection limits for micro- and nano-sensors and highlight unexplained discrepancies between reported values and theoretical limits.



▲ Figure 1: Model system studied here. Solution with target concentration c_0 flows with rate Q ~ H Wc U through a channel of height H and width Wc over a sensor of length L and width Ws that is functionalized with bm receptors per unit area. The kinetic rate constants for the (first-order) binding reaction are k_{on} and k_{off}, and the diffusivity of the target molecules is D.



▲ Figure 2: "Phase diagram" for mass transport in our model sensing system. "Full collection" occurs at sufficiently low Pe_H, corresponding to region I. In region II, a depletion zone forms that is thin compared to both the sensor length L and the channel height H. In region III, the depletion zone is thinner than the channel, but thicker than the sensor. Region IV has not, to our knowledge, been studied thus far. The boundaries between these regions are described in Supplementary Notes of [1]. Stars correspond to concentration profiles (C)-(I) shown in Figure 3 of [1].

Reference

[1] T.M. Squires, R.J. Messinger, and S.R. Manalis, "Making it stick: convection, reaction and diffusion in surface-based biosensors," *Nature Biotechnology*, vol. 26, no. 4, pp. 417-426, Apr. 2008.

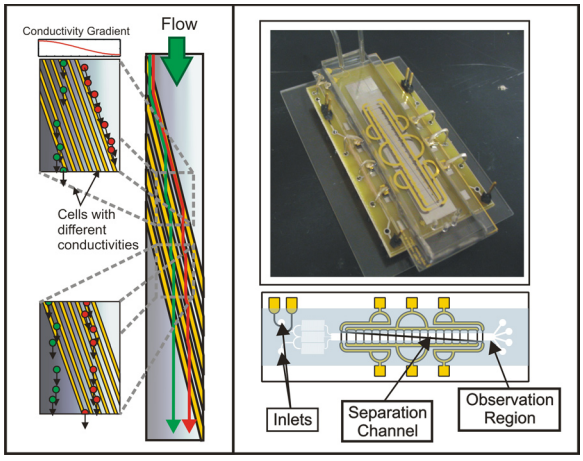
Iso-dielectric Separation of Cells and Particles

M.D. Vahey, J. Voldman

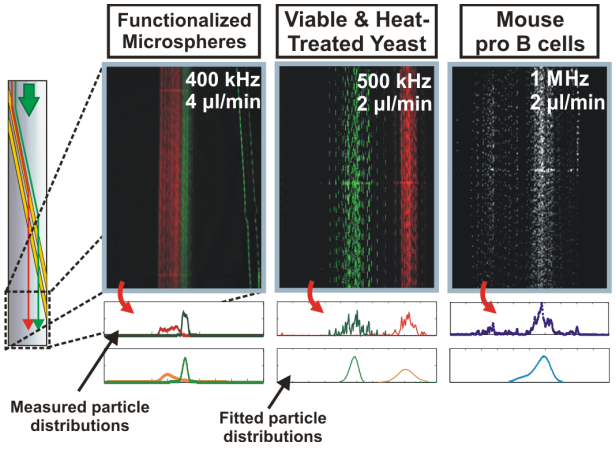
Sponsorship: NIH NIBIB, MIT Buschbaum Fund, Singapore-MIT Alliance, CSBi/Merck Graduate Fellowship

The electrical properties of cells and particles offer insight into their composition and structure as well as provide an intrinsic handle upon which separations can be based. Over the past several decades, dielectrophoresis (DEP) [1], electrorotation [2], and impedance spectroscopy [3] have been used to characterize the electrical properties of cells. Not surprisingly, these techniques – in particular, DEP - have also proven effective for cell sorting [1]. One significant barrier in developing effective electrical sorts of cells, however, is our relatively poor understanding of cells' electrical properties and how they vary under different environmental conditions. Better understanding of how phenotype and genotype manifest themselves through the electrical properties of a cell under different environmental conditions is crucial for developing new screens. Towards this end, we have created a separation method – iso-dielectric separation, or IDS – that separates continuous streams of cells and particles according to their intrinsic dielectric properties [4, 5].

Iso-dielectric separation uses dielectrophoresis (DEP) and a medium with spatially varying conductivity to sort cells according to their effective conductivity (Figure 1). It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis to concentrate cells and particles to the region in a conductivity gradient where their polarization charge vanishes [6]. The IDS leverages many of the advantages of microfluidics and equilibrium gradient separation methods to create a device that is continuous-flow, capable of parallel separations of multiple (>2) subpopulations from a heterogeneous background, and label-free. Additionally, because IDS offers analog separation of cells and particles according to their intrinsic properties, it can be also be used as a platform to characterize particles. We have demonstrated the separation and characterization of particles ranging from polystyrene beads, to the budding yeast Saccharomyces cerevisiae, to mouse pro B cells (Figure 2), representing three orders of magnitude in particle volume (~1-1000 μm^3) and conductivity (~0.001–1 S/m).



▲ Figure 1: (Left) Illustration of IDS, depicting cells with different electric properties following different trajectories in a conductivity gradient. (Top right) Photograph of an assembled device. (Bottom right) Schematic of the device highlighting its primary components.



▲ Figure 2: Separation and characterization of cells and particles using IDS. By measuring the spatial distribution of cells as they exit the device under different conditions and fitting to these distributions, we are able to quantify physical and physiological properties.

References

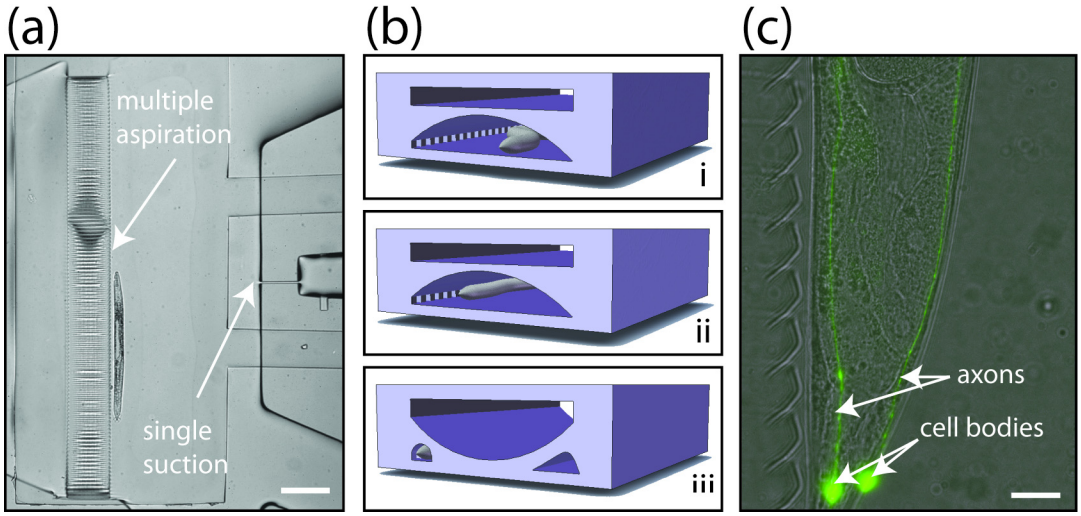
[1] P.R.C. Gascoyne and J. Vykoukal, "Particle separation by dielectrophoresis," *Electrophoresis*, vol. 23, pp. 1973-1983, 2002.
[2] R. Holzel, "Electrorotation of single yeast cells at frequencies between 100 Hz and 1.6 GHz," *Biophysical Journal*, vol. 73, pp. 1103-1109, 1997.
[3] T. Sun, D. Holmes, S. Gawad, N.G. Green, and H. Morgan, "High speed multi-frequency impedance analysis of single particles in a microfluidic cytometer using maximum length sequences," *Lab on a Chip*, vol. 7, no. 8, pp. 1034-1040, Aug. 2007.
[4] M.D. Vahey and J. Voldman, "An equilibrium method for continuous-flow cell sorting using dielectrophoresis," *Analytical Chemistry*, doi: 10.1021/ac7020568.
[5] M.D. Vahey and J. Voldman, "Iso-dielectric separation: A new method for the continuous-flow screening of cells," *Micro Total Analysis Systems '06*, vol. 2, pp. 1058-1060, 2006.
[6] H.A. Pohl and J.S. Crane, "Dielectrophoresis of cells," *Biophysical Journal*, vol. 11, pp. 711-727, 1971.

Sub-cellular, Precision, On-chip Immobilization, Imaging, Manipulation, and Sorting of Small Animals

C.B. Rohde, F. Zeng, C.L. Gilleland, M.F. Yanik
Sponsorship: NIH, Merck/CSBi, NSF, NSERC

Today, pharmacological drug and genetic screens require use of in-vitro cell cultures due to the absence of high-throughput technologies for studying whole animals. However, isolated cells do not represent truly the physiology of live animals, and many multi-cellular processes cannot be screened using cell cultures alone. Although small-animal studies have significantly impacted cellular biology and continue to do so, the lack of techniques for rapid and high-throughput observation and manipulation of sub-cellular features in live animals has significantly limited the use of small-animal assays for drug/genetic discoveries. We have recently invented and developed the first technologies to conduct critical high-throughput drug/genetic studies on whole animals at cellular resolution at unprecedented speeds [1, 2]. These technologies can greatly accelerate drug discovery using small animals for target identification and validation as well as compound mode-of-action screens.

Using microfluidic large-scale-integration techniques, we enable sub-cellular precision high-throughput screening of *C. elegans*, a small semi-transparent nematode that is a powerful model organism for studying a wide variety of biological phenomena. We have created a whole-animal sorter (Figure 1a), which makes use of single and multiple suction channels and an additional control layer to isolate and immobilize a single animal from a group. A microfluidic valve is opened at the input, and the circulating animals enter the sorter. A single small suction channel held at a low pressure is used to capture a single worm, and the remaining animals are washed away. The single worm is then partially immobilized in a straight configuration using multiple aspiration channels on the opposite site of the sorter. The aspiration immobilizes animals only partially, and it is not sufficient to completely restrict their motion. In order to fully immobilize the animals, we create a seal around them that restricts their motion completely. This is done by using a flexible sealing membrane that separates a press-down channel from the flow channel underneath. The press-down channel can be rapidly pressurized to expand the thin membrane downwards. The membrane flexes on top of the captured animals, wrapping around them and forming a tight seal that completely constrains their motion in a linear orientation (Figure 1b). Although the animals are constrained by the PDMS membrane from the top and bottom, they still have access to liquid media via the multiple aspiration channels on the side. The stability of the immobilization is comparable to that achieved using anesthesia, which allows imaging using high-magnification optics (Figure 1c) as well as the use of advanced techniques including femtosecond microsurgery and multi-photon imaging, both of which we have demonstrated on-chip [2]. The ability to flow worms at a high density, combined with the high actuation speed of the valves, means that animals can be isolated and immobilized for analysis very quickly and sorted based on highly complex phenotypes.



▲ Figure 1: Microfluidic immobilization of *C. elegans*. (a) Microfluidic worm sorter structure, illustration of single suction and multiple aspiration ports (scale bar 250 µm). (b) Illustration of the immobilization process. (c) Close-up of immobilized pmec-4::gfp animal, showing gfp-labeled fluorescent posterior lateral mechanosensory (PLM) neurons (scale bar 20 µm).

References

[1] C.B. Rohde, F. Zeng, R. Gonzalez-Rubio, M. Angel, and M.F. Yanik, "Microfluidic system for on-chip high-throughput whole-animal sorting and screening at sub-cellular resolution," *Proc. of the National Academy of Sciences*, vol. 104, no. 35, pp. 13891-13895, Aug. 2007.

[2] F. Zeng, C.B. Rohde, and M.F. Yanik, "Sub-cellular precision on-chip small-animal immobilization, multi-photon imaging and femtosecond laser manipulation," *Lab on a Chip*, 2008, DOI: 10.1039/b804808h.

High-throughput pI-based Fractionation of Biological Samples in Microfluidic Chip for Mass Spectrometry

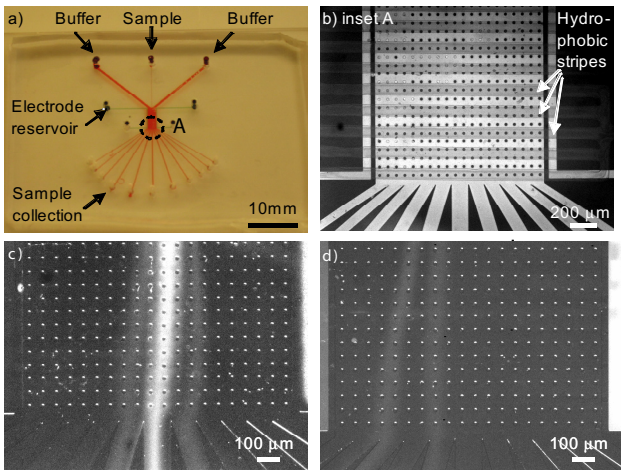
Y.-A. Song, J. Han

Sponsorship: NSF (CTS-0347348), IMC-KIST, CSBi/Merck Postdoctoral Fellowship

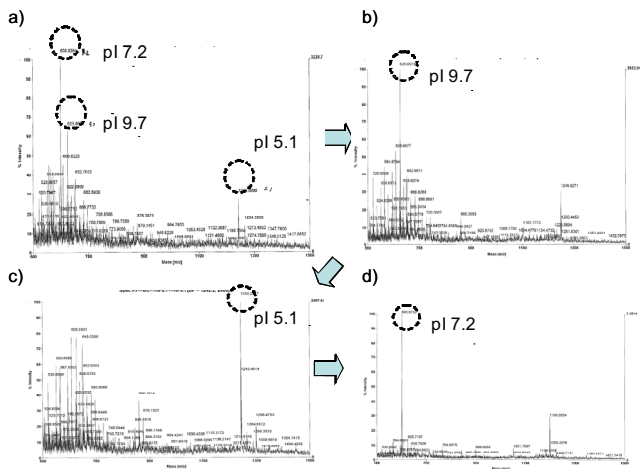
We have developed a microfluidic chip for pI (isoelectric point)-based fractionation of peptides and proteins as a sample preparation step for mass spectrometry (MS). The sorting chip with its multiple outlets allows continuous-flow binary sorting of the proteomic samples into positively and negatively charged molecules without using any carrier ampholytes (Figure 1a). When coupled with pH titration, two fractionation steps enable us to isolate molecules within a predetermined pI range from proteomic sample mixtures [1]. The pI information of the isolated molecules that is not provided by the standard ion-exchange chromatography can lead to a substantial reduction of peptide sequencing time in shotgun proteomics [2].

The electrical junction inside the sorting chip was created simply by patterning multiple submicron-thin hydrophobic layers on glass substrate prior to plasma bonding with the PDMS chip (Figure 1b). To demonstrate the sorting capability, we used three pI markers, 10.3, 8.7 and 6.6, in 20mM phosphate buffer solution with pH 8.4. As Figure 1c) shows, three bands were clearly visible in presence of an electric field of 200 V/cm. We could also separate two different proteins, GFP and R-Phycoerythrin, differing by only 0.5 pI units, into two streams (Figure 1d). In addition, we demonstrated the high-throughput capability of the device by processing raw samples at 1 µL/min, which is sufficient for downstream, standard biomolecule assays such as MS.

We validated the two-step sorting result of a peptide mixture, pI 9.7, pI 7.2 and pI 5.1, into three different fractions with the MALDI-MS. As Figure 2 shows, pI 7.2 (falling between pI 6-8) could be isolated from the mixture. The test of the device with more complex samples such as human serum will ultimately demonstrate its potential in sample preparation for mass spectrometry. Its successful development will have a significant impact on MS-based bioanalysis.



▲ Figure 1: a) The pI-based sorting chip in PDMS with multiple outlets for collection of fractionated sample. b) Multiple hydrophobic layers patterned on glass substrate create electrical junctions. c) Separation of three pI markers (pI 10.3, 8.7 and 6.6) at pH 8.4, 1 µL/min sample flow rate, 4 µL/min sheath flow rate, applied field strength of 200 V/cm at 500 µA. d) Continuous-flow separation of GFP and R-phycoerythrin at pH 6.0, 200 V/cm and 0.5 µL/min.



▲ Figure 2: The MALDI-MS result for the two-step sorting of three peptides (pI 9.7, 7.2 and 5.1). a) Original mixture with 100nM concentration for each peptide. b) In the first sorting step at pH 8.0, the positively charged peptide, pI 9.7, was removed from the mixture. c) In the second sorting step at lower pH value, pH 6.0, negatively charged pI 5.1 was removed from the mixture. d) The remaining pI 7.2, which falls between pI 6-8, was collected out of the peptide mixture.

References

[1] Y.-A. Song, C. Celio, and J. Han, " Continuous-flow pi-based sorting of proteins and peptides for isolation of basic pI range molecules," in *Proc. Eleventh MicroTAS 2007 Symposium*, Paris, France, Oct. 2007, pp. 811-813.

[2] M. Washburn, D. Wolters, and J.R.Yates III, "Large-scale analysis of the yeast proteome by multidimensional protein identification technology," *Nature Biotechnology*, vol. 19, pp. 242-247, Mar. 2001.

Microfabricated Devices for Sorting Cells Using Complex Phenotypes

S. Desai, J. Kovac, B. Taff, J. Voldman

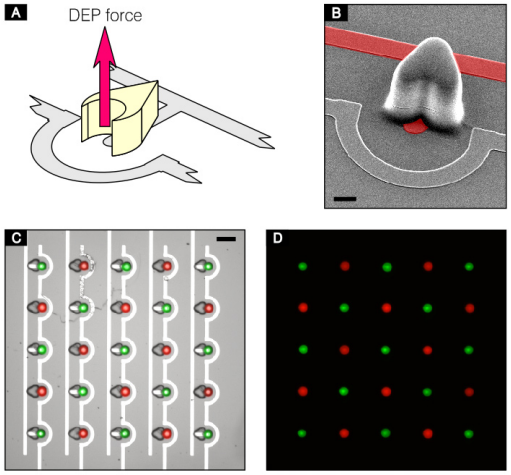
Sponsorship: NIH, Department of Defense Graduate Research Fellowship, Singapore-MIT Alliance

This research involves the development of sorting cytometer architectures for genetic screening of complex phenotypes in biological cells. Our approaches combine the ability to observe and isolate individual mutant cells within surveyed populations. In this work we merge the benefits of microscopy and flow-assisted cell sorting (FACS) to offer unique capabilities in a single platform. Biologists will leverage this flexibility to isolate cells based upon imaged dynamic or intracellular responses

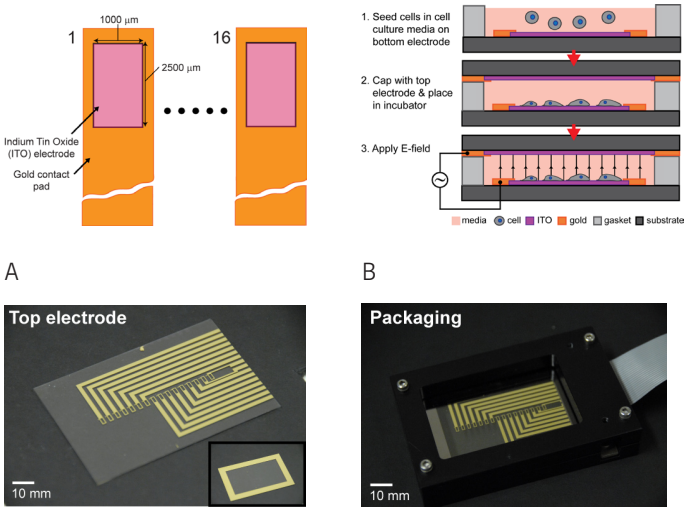
Our most recent electrical approach to image-based sorting [1] combines microfabricated weir structures and their efficient single-cell capture mechanics with negative dielectrophoretic (n-DEP) actuation (Figure 1). In these designs, we "pin" individual cells in designated on-chip locations using "capture cups" formed from a photopatterned silicone polymer [2]. Negative DEP forces then operate as a switch to unload targeted subgroups of the weirs and prevent site-specific loading altogether in arrayed weir grouping. This functionality enables the placement of multiple cell types in organized single-cell patterns on a common substrate, permitting new screening and response assays for cell-cell signaling dynamics. With this platform, manipulations prove feasible in standard cell-culture media, thus avoiding cell health concerns associated with comparative p-DEP approaches.

We have also continued developing our optical approach to image-based cell sorting. In this approach, cells are captured in a 10,000-site silicone microwell array. Following imaging, we use an infrared laser to levitate and thus sort cells out of microwells. Over the past year we have demonstrated the ability to purify cell populations up to >150× as well as sort cells based upon a localization-based phenotype [3].

Additionally, we are investigating the effects of DEP manipulation on cell physiology using a microfabricated, high-content screening (HCS) platform that applies electrical stimuli to cells and monitors the resulting subcellular molecular responses via automated fluorescence microscopy. The platform consists of a chip with individually addressable arrayed electrodes and peripheral support electronics (Figure 2). We seed cells onto the chip and then expose them to a variety of electrical stresses. By monitoring the response of the cells via a fluorescent reporter cell line, we can assess how cells respond to the electric fields.



▲ Figure 1: A combined n-DEP/weir cell-sorting platform.(A) Schematic showing cell "capture cups" (yellow) aligned to underlying electrodes (gray). Cells flow into the "cups" via fluid flow and n-DEP forces enable unloading. (B) An SEM of (A) - scale bar = 10 µm. (C) Dual-color bead patterning as enabled by this new achitecture: merged bright field (BF) and fluorescence signals, scale bar = 50 µm. (D) Highlighted version of image (C) showing fluorescence alone.



▲ Figure 2: HCS platform. (A) Top-down schematic of 16 individually addressable transparent indium-tin oxide (ITO) electrodes. (B) Seeding of cells on electrodes and running the screening assay. (C) Images of bottom electrode (left panel) and top electrode chips (inset). Image of packaged device (right panel), showing bottom electrode chip visible through transparent top electrode.

References

[1] B.M. Taff, S.P. Desai, and J. Voldman, "Dielectrophoretically switchable microfluidic weir structures for exclusion-based single-cell manipulation," in *Proc. of Eleventh International Conference on Miniaturized Systems for Chemistry and Life Sciences*, Paris, France, Oct. 2007, pp. 8-10.

[2] S.P. Desai, B.M. Taff, and J. Voldman, "A photopatternable silicone for biological applications," *Langmuir*, vol. 24, no. 2, pp. 575-581, Jan. 2008.

[3] J.R. Kovac and J. Voldman, "Intuitive, image-based cell sorting using optofluidic cell sorting," *Analytical Chemistry*, vol. 79, no. 24, pp. 9321-9330, Nov. 2007.

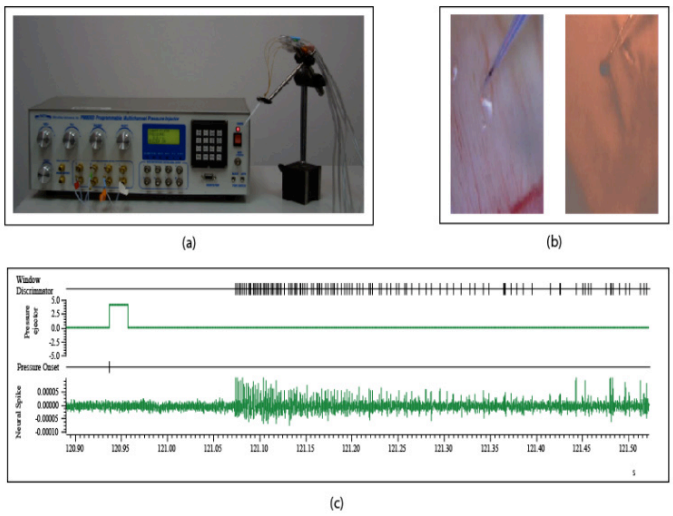
Inkjet Stimulation of Neurons

L. Theogarajan, M.A. Baldo

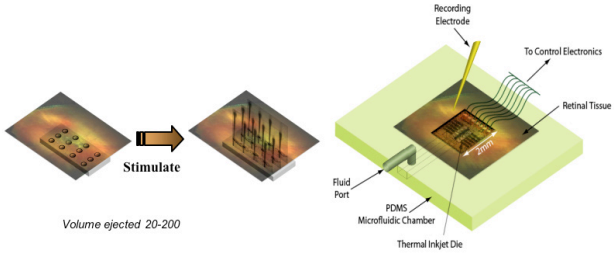
Electrical excitation is the standard method for stimulating neural tissue [1]. Although widely used, it is not the most efficient method. We have been investigating the use of potassium ions as a method of stimulating neural tissue. The use of ionic stimulation allows for a more biocompatible and low-power method of stimulation. Initial in-vitro experiments on rabbit retina show that a modest increase (~10mM) of extracellular potassium ion concentration elicits neural responses.

Our initial experiments were performed by pressure ejection of KCl using a multi-barrel glass pipette and performed on the epi-retinal side of the retina [2], as in Figure 1. However, the final envisioned device will be situated in the sub-retinal space. Furthermore, a different in-vitro experimental platform needs to be designed to overcome the limitations of the existing setup. Furthermore, a device that allows for ejection of very small volumes (pL compared to nl) and also allows for accurate estimation of volumes ejected would greatly enhance the development of a prosthetic device using this concept. An additional advantage of ionic stimulation over electrical stimulation, as an investigation tool for neuroscience, is that ionic stimulation does not induce a stimulus artifact that allows for simultaneous recording from multiple neurons.

Thus, it would be advantageous to build an ionic stimulation platform that has the capability of array stimulation. Inkjet printing technology naturally lends itself to this endeavor and is the platform of choice for our device. Figure 2 illustrates the scheme . However, our initial experiments using thermal inkjet technology met with failure for reasons including inkjet head construction and chamber size. Simple experiments performed using a piezoelectric inkjet head showed more promise and we are currently building a custom in-vitro stimulation platform using a piezoelectric inkjet head controlled by custom electronics and using a software platform based on LabView.



▲ Figure 1: a) Experimental setup used for the K+ stimulation. b) Snapshots of the pipette positioned over the retina; the figure with a red shading is the pipette under red light illumination and shows the KCl solution being ejected with the dark stain caused by the Azure B dye used for visualization. The red light was used to prevent the retina from responding to the ambient light since it is known that rabbit retinae do not respond to red light. c) Typical response to K+ stimulation. Shown is the response to concentration of 30mM KCl. The square pulse is the onset of the ejection.



▲ Figure 2: Inkjet stimulation platform for accurate determination of ejected volumes and multi-point stimulation. (See text for more details.)

References

[1] L. Theogarajan et al., "Minimally invasive retinal prosthesis," ISSCC Digest of Technical Papers, 2006, pp. 99-102.

[2] L. Theogarajan, R. Jensen and J.F. Rizzo, "Stimulation of rabbit retinal ganglion cells by altering K+ ion gradients: Dose-response curve," *Investigative Ophthalmology & Visual Science*, vol. 45, sup. 2, pp. U401-U401, Apr. 2004.

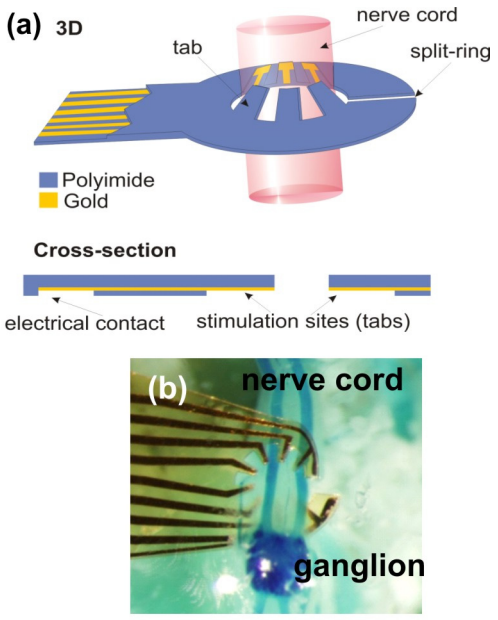
Flexible Multi-site Electrodes for Moth Flight Control

W.M. Tsang, A.I. Akinwande, J. Voldman
Sponsorship: DARPA

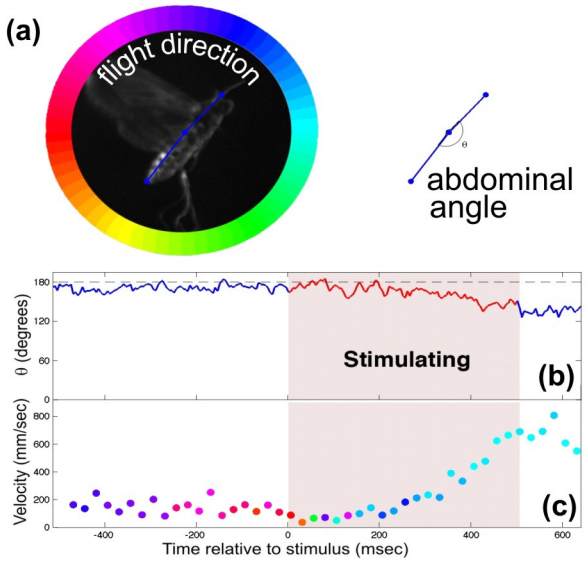
Significant interest exists in creating insect-based Micro-Air-Vehicles (MAVs) that would combine advantageous features of insects—small size, relatively large payload capacity, navigation ability—with the benefits of MEMS and electronics—sensing, actuation and information processing. In this work, we have developed a flexible electrode array that provides multi-site stimulation in the moth's abdominal nerve cord. These flexible multi-site electrodes (FMEs) are implanted into moth (Manduca Sexta) pupae and directly interface with the central nervous system (CNS) of the moths for flight control.

The FMEs are composed of two layers of polyimide with gold sandwiched in between and have 4 – 8 stimulation sites (Figure 1). The FMEs have a split-ring design that allows the FME to encircle the nerve cord, and the electrodes on the FME are on flexible tabs that protrude into the split ring and can bend back to make good contact with the nerve cord. The split-ring and tab design makes the FME adaptable to a wide range of nerve cord diameters, maintaining good contact as animals undergo metamorphosis and the nerve cord diameter increases.

These FMEs were inserted into pupae as early as 7 days before the adult moth emerges and could stimulate pupae and adult moths. In pupae, we observed abdominal flexion using square wave pulses of ≥4 volts at various pairs of the stimulation sites, and similar behavior was observed in tethered adult moths. The electrode implantations and stimulation experiments were performed by our collaborators at the University of Arizona and University of Washington, respectively. Finally, in loosely tethered flight, we have used this abdominal ruddering to cause the normally hovering moth to change its abdominal angle, leading to a change in flight direction (Figure 2). This demonstrates our ability to create MEMS-based electrodes that can be implanted in pupae, directly interface with the CNS, and enable control of insect flight.



▲ Figure 1: (a) Schematic and (b) photograph show the electrode inserted in the CNS of a pupa.



▲ Figure 2: Flight control of a loosely tethered adult moth: (a) Definitions of flight direction (colored circle) and abdominal angle (θ) of the moth; (b) Variation of the abdominal angle and (c) The magnitude and direction of the moth's velocity (the colors indicate the direction) with stimulation. Upon stimulation of the insect, the velocity increases and the flight direction of the moth changes from up-and-to-the-left to directly right, and both coincide with a change in angle caused by the flexion of the abdomen.

Protein Separation by Free-flow Isoelectric Focusing

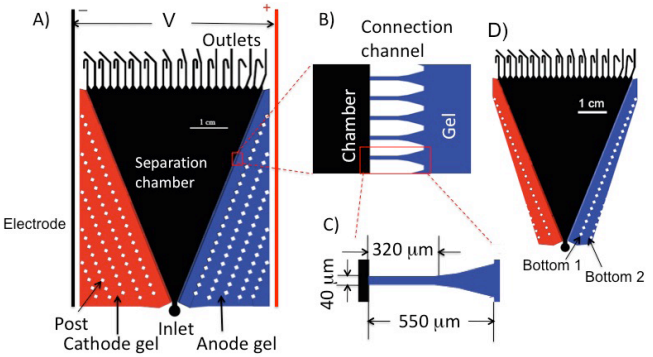
J. Wen, J. Albrecht, E. W. Wilker, M.B. Yaffe, K.F. Jensen

Sponsorship: Department of Chemical Engineering, Center for Cancer Research, Department of Biology

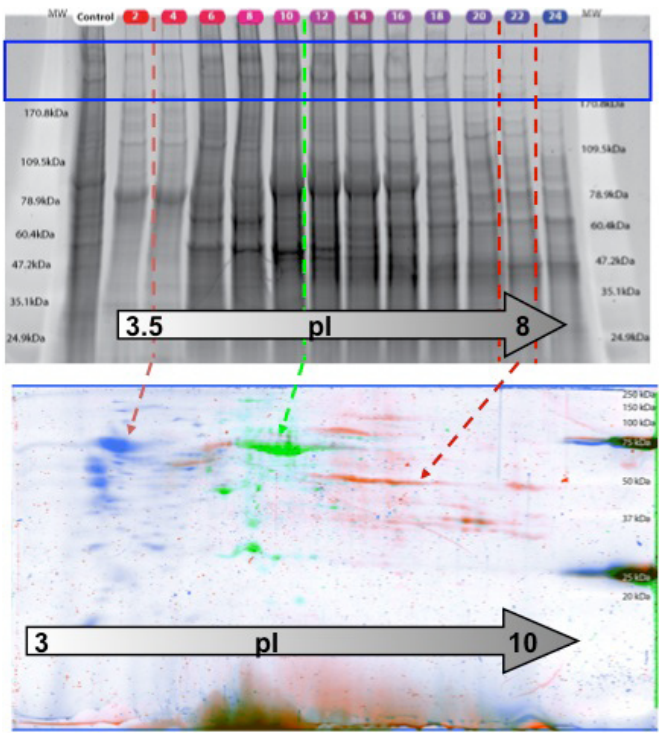
Disposable, inexpensive microfluidic devices have the potential to become a robust new tool for proteomic research involving difficult proteins and protein complexes. In this work, a preparative scale free-flow IEF isoelectric focusing (FF-IEF) device was designed, investigated, and optimized. Prior work on micro FF-IEF has described devices with volumes in the range of 1-2 μL [1] and a flow rate of sub-microliters per minute. A larger FF-IEF device was developed to address the needs of molecular biologists working with samples of milligrams in mass and milliliters in volume. Earlier work [1] with IEF simulations has confirmed the advantages of using non-rectilinear channel geometries. Here we present a triangular-shaped preparative IEF device fabricated by soft lithography in PDMS and having 24 outlets. The triangular design facilitates the development of the pH gradient with a corresponding increase in separation efficiency and decrease in focusing time.

The unique design of a triangular separation channel required the electric fields across the central channel to be optimized. After the shaping of the PDMS prior to the device binding, a functionalized polyacrylamide gel region at the bottom of the device was selectively controlled to adjust the ratio of the applied potential across the separation channel (Figure 1). At the device depth of 160 mm, the electric fields of as high as over 300 V/cm could be achieved. To further investigate the separation of the protein complex mixture on the microdevice, whole cell lysate of U20S was applied and separated under denaturing conditions. To validate the performance of the free-flow IEF separation, selective fractions representing the acidic, neutral, or basic region were run on a traditional 2D gel. As Figure 2 shows, effective isolation of acidic (blue), neutral (green), and basic (orange) proteins from the whole cell lysate was achieved. High-molecular-weight proteins were retained by FF-IEF (shown in the blue box), but they are mostly missing from the 2D gel separation.

Thus using the IEF device is an advantage for biologists interested in high-molecular-weight proteins, which presently are difficult to isolate with conventional IEF-strip 2D gel techniques. The devices can process complex biological samples and fractionate whole cell lysate at rates between 10-30 uL/min while providing greater separation of traditionally difficult proteins. These findings show the promise of inexpensive, disposable microfluidic FF-IEF devices in proteomics research.



▲ Figure 1: A) Mask design of free-flow IEF device. The device was 5 cm by 7.5 cm with the center triangle separation chamber of 4 cm in width and 5.2 cm in height. Functionalized pH gradient cathode (pK=9.3) and anode (pK=3.6) polyacrylamide gels were polymerized into the gel regions, which were connected to the separation chamber. B) Detail of channel array. C) Channel dimensions: 0.32 by 0.04 mm. D) The regions of functionalized gels can be adjusted for individual devices.



▲ Figure 2: Focusing of U20S cell lysate with FF-IEF followed by 2-D electrophoresis. Acidic, neutral, and basic fractions of 3, 11, and 21+23 were further run on a conventional 2D gel to show the effectiveness of the FF-IEF separation.

Reference

[1] J.W. Albrecht, J. El-Ali, and K.F. Jensen. "Cascaded free-flow isoelectric focusing for improved focusing speed and resolution," *Analytical Chemistry*, vol. 79, no. 24, pp. 9364-9371, 2007.

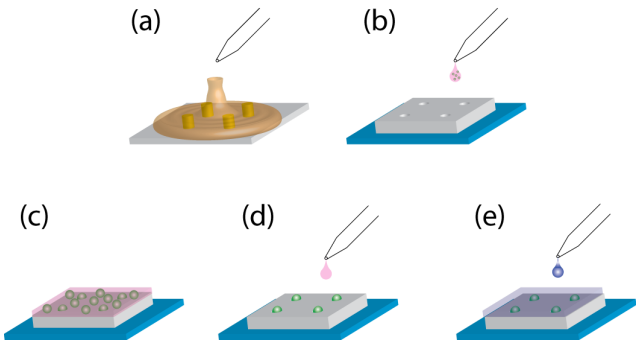
Multiplexed Comet Assay for DNA Damage and Repair

D.K. Wood, D.M. Weingeist, J.T. Mutamba, B.P. Engelward, S.N. Bhatia

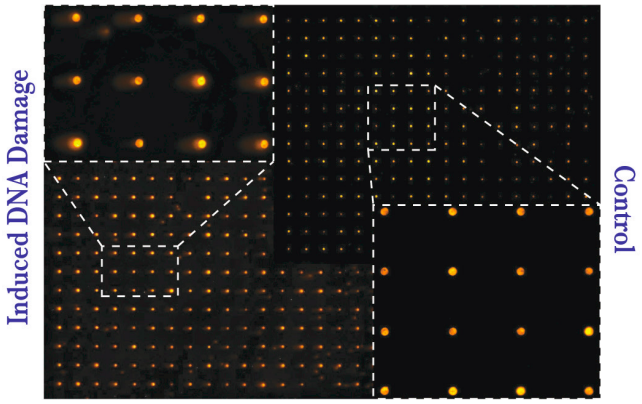
Sponsorship: Biological Response Indicators of Environmental Stress (U01), National Institute of Environmental Health Sciences

The use of DNA damage as a biomarker with predictive value for cancer and other diseases requires the development of a robust assay that enables routine assessment of DNA damage levels in human samples. Many applications, such as toxicity testing and epidemiological studies, require an assay that is capable of testing many conditions or many samples in parallel. To this end, we are developing a high-throughput version of the comet assay, a well-known assay for DNA damage. The basic principle of the assay is that undamaged DNA is supercoiled and highly compact, whereas damaged DNA is composed of relaxed loops and fragments and is more mobile when electrophoresed in an agarose gel. Our assay offers many distinct advantages over other DNA damage assays, including a high level of sensitivity and the ability to detect multiple damage types. The assay can also be implemented as a measure of DNA repair kinetics. Despite the assay's apparent benefits, it has been underutilized because of poor reproducibility, both from laboratory to laboratory and from user to user, and the time- and labor-intensive process of performing the assay. The major goal of this project is to overcome this assay's limitations, such as its low throughput and poor reproducibility, to create a multiplexed assay for DNA damage and repair. The goal is a new tool that will be useful in a broad range of clinical, epidemiological, and experimental settings.

Cell micropatterning enables spatial encoding of assay conditions, and it vastly improves spatial utilization of chips over the case with randomly placed cells. Both of these features are critical to a truly multiplexed assay platform. We have implemented single-cell micropatterning using microwells[1-2] fabricated directly into agarose gel (Figure 1). A negative relief mold of the microwells is fabricated using photolithography of SU-8 on a silicon substrate. Molten agarose is applied to the mold and allowed to solidify, resulting in an agarose gel with patterned microwells. A cell suspension with $1-2\times10^6$ cells/ml is applied to the gel, and cells are allowed to settle into the wells by gravity. Afterwards excess cells are rinsed, leaving only cells contained in the microwells. Finally, another agarose layer is applied to encapsulate the cells and to contain the DNA during the comet assay. Examples of microarrayed comets appear in Figure 2. The size of the well is a tunable parameter, which allows us to control the number of cells trapped in a single well. Additionally, this method places the cells in the same focal plane, which facilitates automated imaging, and it gives control over the cell microenvironment. We are currently developing a method for applying multiple chemical damaging agents to a single comet chip. With 100% filling efficiency, 200-μm cell spacing requires only 4 mm² for 100 cells/condition, which would allow 200 conditions on a single comet chip (20×50 mm² imaged area). Combining a platform for applying multiple conditions with the existing comet chip would provide the first truly multiplexed assay for DNA damage.



▲ Figure 1: (a) Single cell micropatterning using agarose microwells. Molten agarose is allowed to solidify on a master of silicon with SU-8 posts. (b) Single cell suspension is applied to agarose microwells. (c) Cells are allowed to settle into wells. (d Excess cells are washed away. (e) The microwells are capped with an agarose capping layer.



▲ Figure 2: Arrayed comets created using cell micropatterning method. Dose response is shown for TK6 lymphoblastoid cells treated with 1X DPBS (control) and 98 μM H_2O_2. Cells are arrayed with a 200-μm pitch, which was empirically determined to allow sufficient space for the comet tail. This demonstrates our ability to spatially encode DNA damage using micropatterning.

References

[1] J.R. Rettig and A. Folch, "Large-scale single cell trapping and imaging using microwell arrays," *Analytical Chemistry*, vol. 77, no. 17, pp. 5628-5634, Sept. 2005.

[2] A. Rosenthal, A. MacDonald, and J. Voldman, "Cell patterning chip for control of the stem cell microenvironment," *Biomaterials*, vol. 28, no. 21, pp. 3208-3216, July 2007.

Microfluidic Devices for Studying Early Response of Cytokine Signaling

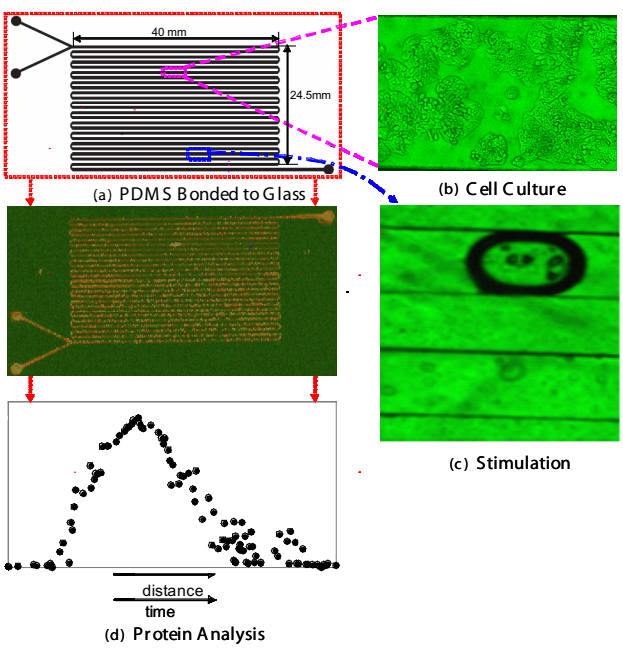
L.L Ye, K.F. Jensen

This study presents the design, fabrication, and characterization of a microfluidic device (as shown in Figure 1) integrated with cell culture, cell stimulation, and protein analysis as a single device towards efficient and productive cell-based assay development. In particular, it demonstrates the feasibility of culturing human cancer cells in microliter-volume reactors in batch and fed-batch operations, stimulating the cell under well-controlled and reproducible conditions at early stages, and detecting the protein signals with an immunocytochemical (In-Cell Western) assay.

These microfluidic devices take advantage of microfabrication techniques to create an environment suitable for cell culture, biomechanical and biochemical stimulation of cells, and protein detection and analysis. The microfluidic approach greatly reduces the amounts of samples and reagents necessary for these procedures and the required process time compared with their macroscopic counterparts. Moreover, the technique integrates unit operations, such as cell culture, stimulation, and protein analysis, in a single microchip.

The microfluidic technique presented in this study correlates the space in the microchannels with the biological process time (cell stimulation time). Thus, a single experiment in one microfluidic device is capable of generating a multiple experimental complete temporal cell response curve, which otherwise would have required multiple experiments and manual assays by standard microwells and pipetting techniques. The developed method also provides high time-resolution and reproducible data for studies of cell signaling events, especially at early stages. These cell signaling events are difficult to investigate by conventional techniques.

This study reports the development not only of a cell population analysis method, but also of a single-cell detection and analysis technique to explore cell-to-cell variations. In this study, a new microscope stage holder was designed and machined, and an auto cell counting algorithm was developed for single-cell analysis. This single-cell method provided data on cell-to-cell variations and showed that the average cell signaling profiles were consistent with those by population-based analysis. The integration of single-cell imaging and microfluidic-enabled measurements shows promise as a technique for exploring cell signaling with single-cell resolution.



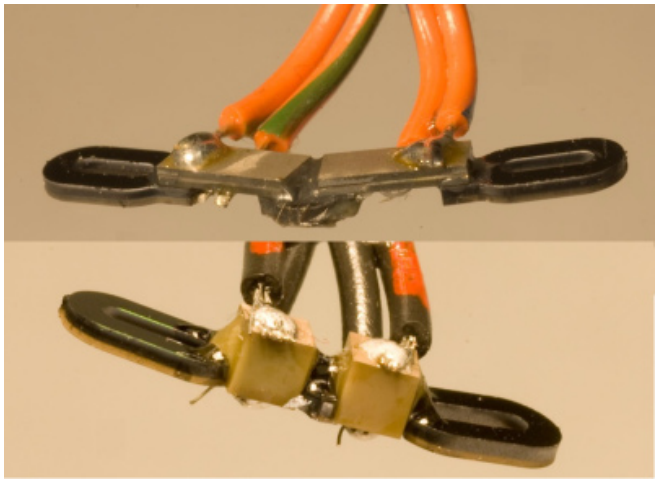
▲ Figure 1: Schematic of the microfluidic system

Micromechanical Actuators for Insect Flight Mechanics

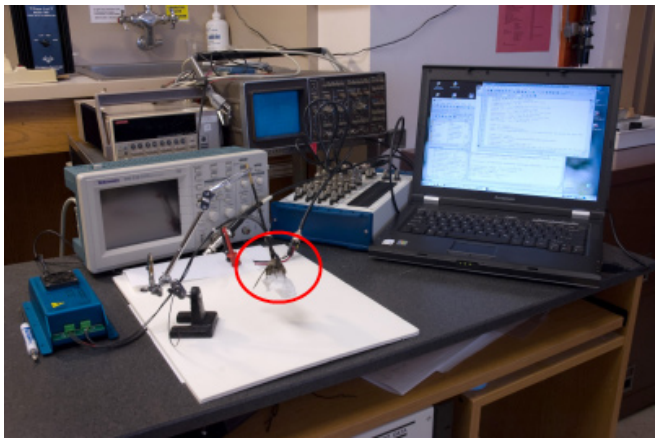
H. Zhou, M.A. Schmidt (in collaboration with T.L. Daniel, University of Washington)
Sponsorship: DARPA

This project aims to develop MEMS actuators to aid in the study of insect flight mechanics. Specifically, we are developing actuators that can stimulate the antennae of the crepuscular hawk moth *Manduca Sexta*. The possible mechanosensory function of antennae as airflow sensors has been suggested [1], and recent discoveries of our collaborators reveal that mechanosensory input from the antennae of flying moths serves a similar role to that of the hind wings of two-winged insects, detecting Coriolis forces and thereby mediating flight stability during maneuvers [2]. Early evidence suggests that mechanical stimulus of the antennae may enable flight control. In addition, the crepuscular hawk moth *Manduca Sexta* has a wide wingspan (~110 mm) and is capable of carrying at least one quarter of its own weight. Thus, studying the flight of *Manduca Sexta* by attachment of microsystems seems plausible. The goal of our project is to design and fabricate micromechanical actuators, which will be mounted onto the moth antennae. Our collaborators will study the flight control mechanism by mechanical stimulation.

Our first step was to fabricate "dummy" silicon rings for our biologist collaborators for implant experimentation. Due to the nature of the moth antennae, ring-beam-ring construction was designed and fabricated, like a "shackle," to meet the mounting requirements [3]. Our current work focuses on integrating actuators onto the mounting kit. A piezoelectric-bender and piezoelectric-stack are considered the actuator (Figure 1). Live testing is also done while the moth is resting or flipping its wings (Figure 2). The moth apparently responds to the mechanical stimulus under both circumstances by swinging its wings and abdomen. Future work will refine the actuator design and quantitatively analyze the moth's reaction to the mechanical stimulation, which might lead to successful flight control of the moth.



▲ Figure 1: Mounting kits made of silicon bases and piezoelectric benders (top) and piezoelectric stacks (bottom).



▲ Figure 2: Experimental setup for live testing (the moth is highlighted by a red circle, wearing the piezoelectric-stack "shackle").

References

[1] M. Gewecke, "Antennae: Another wind-sensitive receptor in locusts," *Nature*, vol. 225, no. 5239, pp. 1263-1264, Mar. 1970.
[2] S.P. Sane, A. Dieudonné, M.A. Willis, and T.L. Daniel, "Antennal mechanosensors mediate flight control in moths," *Science*, vol. 315, pp. 863-866, Feb. 2007.
[3] H. Zhou and M.A. Schmidt, "Micromechanical actuators for insect flight mechanics," Massachusetts Institute of Technology, Cambridge, MA, MTL Annual Research Report, 2007.

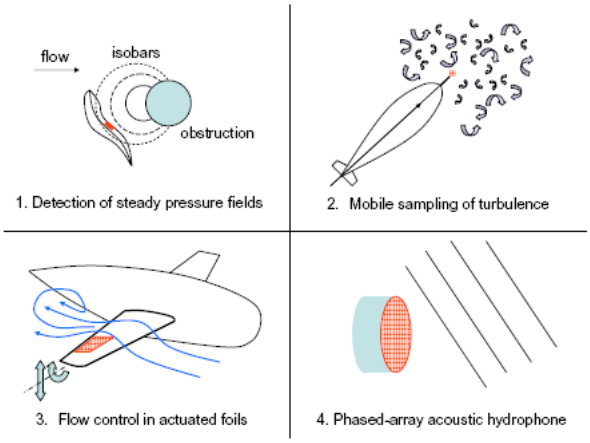
Biomimetically Inspired MEMS Pressure Sensor Assays for Passive Underwater Navigation

V.I. Fernandez, S.M. Hou, F.S. Hover, J.H. Lang, M.S. Triantafyllou
Sponsorship: NOAA: MIT Sea Grant College Program

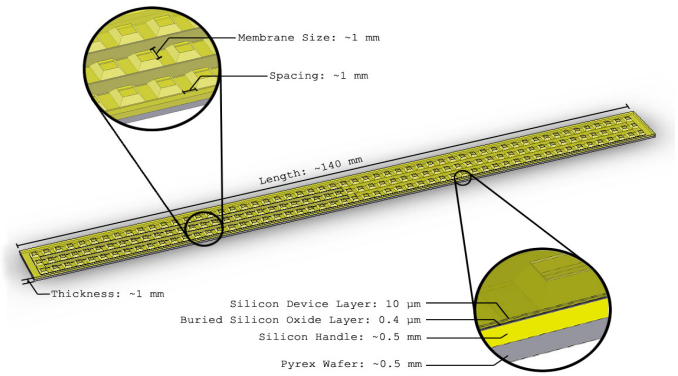
A novel sensing technology for unmanned undersea vehicles (UUVs) is under development. The project is inspired by the lateral line sensory organ in fish, which enables some species to form three-dimensional maps of their surroundings [1, 2]. The canal subsystem of the organ can be described as an array of pressure sensors [3]. Interpreting the spatial pressure gradients allows fish to perform a variety of actions, from tracking prey [4] to recognizing nearby objects [2]. It also aids schooling [5]. Similarly, by measuring pressure variations on a vehicle surface, an engineered dense pressure sensor array allows the identification and location of obstacles for navigation (Figure 1). We are demonstrating proof-of-concept by fabricating such MEMS pressure sensors by using KOH etching techniques on SOI wafers to construct strain-gauge diaphragms.

The system consists of arrays of hundreds of pressure sensors spaced about 2 mm apart on etched silicon and Pyrex wafers. The sensors are arranged over a surface in various configurations (Figure 2). The target pressure resolution for a sensor is 1 Pa, which corresponds to the noiseless disturbance created by the presence of a 0.1-m-radius cylinder in a flow of 0.5 m/s at a distance of 1.5 m. A key feature of a sensor is the flexible diaphragm, which is a thin (20 μm) layer of silicon attached at the edges to a silicon cavity. The strain on the diaphragm due to pressure differences across the diaphragm is measured. At this stage, the individual MEMS pressure sensors are being constructed and tested.

In parallel to the construction of a sensor array, techniques are being developed to interpret the signals from a dense pressure array by detecting and characterizing wake structures such as vortices and building a library of pressure distributions corresponding to basic flow obstructions. In order to develop these algorithms, experiments are being performed on coarse arrays of commercial pressure sensors.



▲ Figure 1: Pressure-sensor array applications.



▲ Figure 2: Diagram of pressure-sensor array with basic structure depicted.

References

[1] J.C. Montgomery, S. Coombs, and C.F. Baker, "The mechanosensory lateral line system of the hypogean form of *Astyanax fasciatus*," *Environmental Biology of Fishes*, vol. 62, pp. 87-96, 2001.

[2] C. von Campenhausen, I. Riess, and R. Weissert, "Detection of stationary objects by the blind cave fish *Anoptichthys jordani* (Characidae)," *Journal of Computational Physiology A*, vol. 143, pp. 369-374, 1981.

[3] S. Coombs, "Smart skins: Information processing by lateral line flow sensors," *Autonomous Robots*, vol. 11, pp. 255-261, 2001.

[4] K. Pohlmann, J. Atema, and T. Breithaupt, "The importance of the lateral line in nocturnal predation of piscivorous catfish," *Journal of Experimental Biology*, vol. 207, pp. 2971-2978, 2004.

[5] T.J. Pitcher, B.L. Partridge, and C. S. Wardle, "A blind fish can school," *Science*, vol. 194, pp. 963-965, 1976.

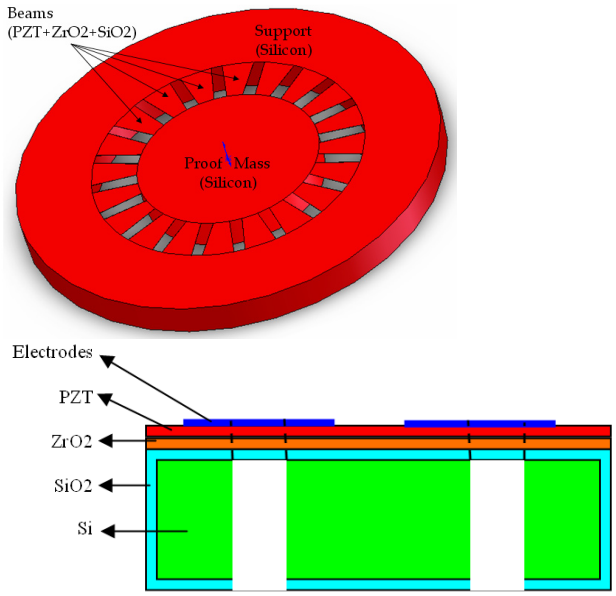
Piezoelectric Micro-power-generator: MEMS Energy-arvesting Device for Self-powered Wireless Monitoring Systems

A. Hajati, S.-G. Kim

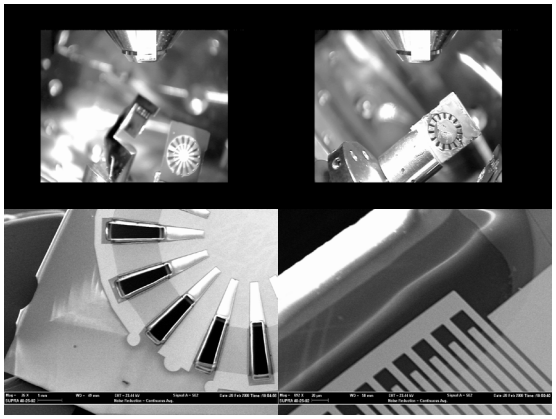
Sponsorship: NSF, Korean Institute of Machinery and Material

A novel thin-film lead zirconate titanate $Pb(Zr,Ti)O_3$ (PZT) MEMS energy-harvesting device is designed and developed for powering autonomous wireless sensors. It is designed to harvest energy from parasitic vibrational energy sources and convert it to electrical energy via the piezoelectric effect [1-4]. The new pie-shaped design always generates positive tension on the PZT layer and then positive charge output throughout vibration cycles. It produces mono-polarity output charge without using any additional bridge rectifier circuitry, which will be a huge cost saving for commercial production of scaled-up products. Contrary to the high-Q cantilever designs, the new design has a low-Q, doubly anchored beam design, which provides a wide bandwidth of operational frequency. This will enable more robust power generation even if the frequency spectrum of the source vibration varies unexpectedly. Furthermore, the beam shape is optimized to achieve uniform strain throughout the PZT layer [5].

In this new design, the whole thickness of the silicon wafer is used as the proof mass to increase the power of the generator. The fabrication includes CVD of 10-micron-thick oxide, followed by spin-coating, patterning, wet-etching, and annealing a thin ZrO2 layer as the diffusion barrier layer, followed by three layers of PZT. The top interdigitated electrodes are patterned by the lift-off method out of gold. A long BOE etching through the oxide followed by a DRIE of silicon from the wafer's back finalizes the device structure and releases the beams and proof mass (Figure 1). The SEM images of the released multi-beam cantilever beam design with a common heavy proof mass (an improved version of type-I PMPG) and a pie-shaped device with a center proof mass (type-II device) are imaged using scanning electron microscope (SEM) as shown in Figure 2.



▲ Figure 1: The structure of the pie-shaped PMPG.



▲ Figure 2: SEM pictures of the released PMPG.

References

[1] Y.B. Jeon, R. Sood, J.H. Jeong, and S.-G. Kim, "MEMS power generator with transverse mode thin film PZT," *Sensors and Actuators A: Physical*, vol. 122, no. 1, pp. 16-22, July 2005.

[2] W.J. Choi, Y. Xia, J.A. Brewer, and S.-G. Kim, "Energy harvesting MEMS device based on thin-film piezoelectric cantilevers," in *Proc. of INSS05*, San Diego, CA, June 27-28, 2005.

[3] R. Xia, C. Farm, W. Choi, and S.-G. Kim, "Self-powered wireless sensor system using MEMS piezoelectric micro power generator," *Proc. IEEE Sensors 2006*, Daegu, Korea, 2006.

[4] W.J. Choi, Y. Jeon, J.-H. Jeong, R. Sood and S.-G. Kim, "Energy harvesting MEMS devices based on thin film piezoelectric cantilevers," *Journal of Electroceramics*, vol. 17, nos. 2-4, p. 543, 2006.

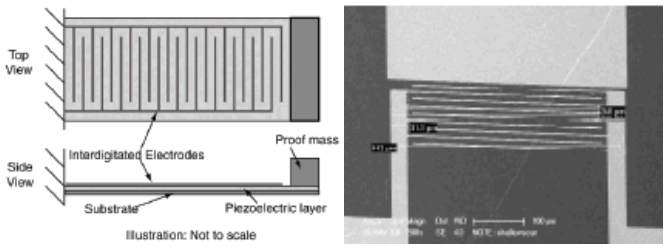
[5] A. Hajati and S.-G. Kim, "Rectifierless piezoelectric micro power generator," *SPIE Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring 2008*, San Diego, CA, 2008

MEMS Vibration Harvesting for Wireless Sensors

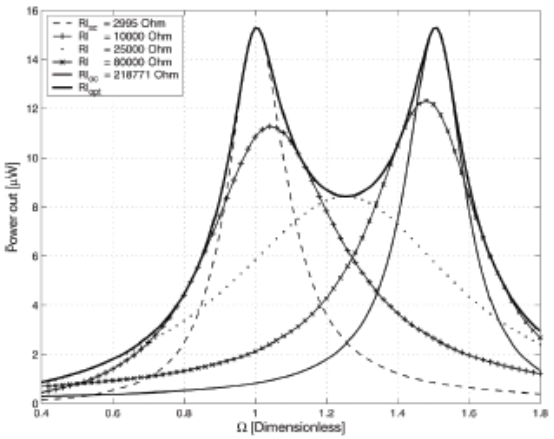
W.S. Kim, M. Kim, M.Hoegen, F. Fachin, S.-H. Kim, A. Mracek, B.L. Wardle (in collaboration with S.-G. Kim)
Sponsorship: AFOSR, NSF Fellowship, Samsung Fellowship

The recent development of "low-power" (10's-100's of μW) sensing and data transmission devices, as well as protocols with which to connect them efficiently into large, dispersed networks of individual wireless nodes, has created a need for a new kind of power source. Embeddable, non-life-limiting power sources are being developed to harvest ambient environmental energy available as mechanical vibrations, fluid motion, radiation, or temperature gradients [1]. While potential applications range from building climate control to homeland security, the application pursued most recently has been that of aircraft structural health monitoring (SHM).

This SHM application and the power levels required favor the piezoelectric harvesting of ambient vibration energy, compared to other transduction principles. Current work focuses on harvesting this energy with MEMS resonant structures of various geometries. Coupled electromechanical models for uniform beam and plate structures have been developed to predict the electrical and mechanical performance obtainable from ambient vibration sources. The optimized models have been validated by comparison to prior published results [2] and verified by comparison to tests on a macro-scale device [3]. A non-optimized, uni-morph beam prototype (Figure 1) has been designed and modeled [4-5]. Dual optimal frequencies with equal peak power and unequal voltages and currents are characteristic of the response of such coupled devices when operated at optimal load resistances (Figure 2). Design tools to allow device optimization for any given vibration environment have been developed for both geometries. Future work will focus on fabrication and testing of optimized uni-morph and proof-of-concept bimorph prototype beams. This work will include system integration and development, including modeling the power electronics.



▲ Figure 1: Illustration of uni-morph energy-harvester configuration (left) and SEM of a prototype device.



▲ Figure 2: Power vs. normalized frequency with varying electrical load resistance [4].

References

[1] S. Roundy, P.K. Wright, and J.M. Rabaey, *Energy Scavenging for Wireless Sensor Networks with Special Focus on Vibrations*, Norwell, MA: Kluwer Academic Publishers, 2004.

[2] H.A. Sodano, G. Park, and D.J. Inman, "Estimation of electric charge output for piezoelectric energy harvesting," *Strain*, vol. 40, no. 2, pp. 49-58, May 2004.

[3] N.E. duToit and B.L. Wardle, "Experimental verification of models for microfabricated piezoelectric vibration energy harvesters," *AIAA Journal*, vol.45, no.5, pp.1126-1137, May 2007.

[4] N.E. duToit, B.L. Wardle, and S.-G. Kim, "Design considerations for MEMS-Scale piezoelectric mechanical vibration energy harvesters," *Integrated Ferroelectrics*, vol. 71, pp. 121-160, 2005.

[5] N.E. duToit and B.L. Wardle, "Performance of microfabricated piezoelectric vibration energy-harvesters," *Integrated Ferroelectrics*, vol. 83, pp.13-23, 2007.

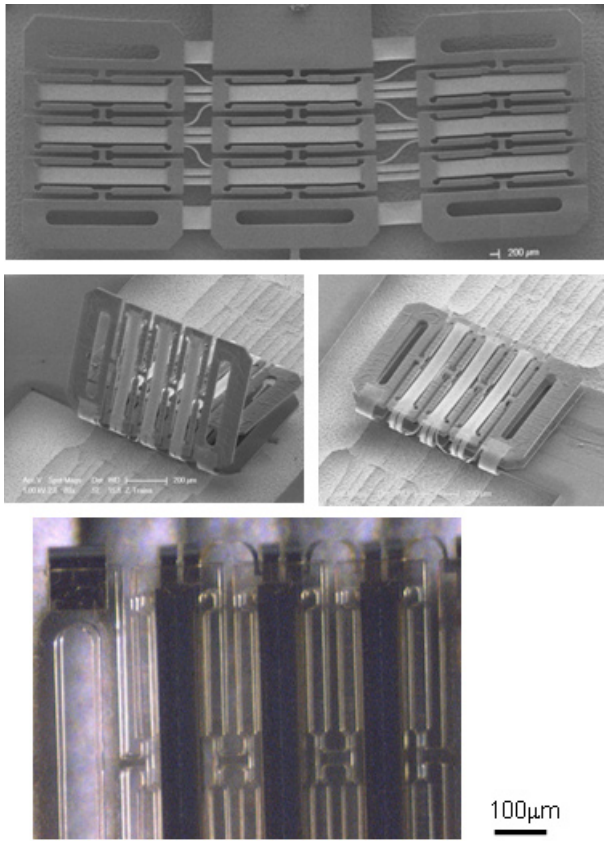
A Muscle-inspired Cellular Piezo Actuator

H.J. Lee, H. Lee, S.-G. Kim

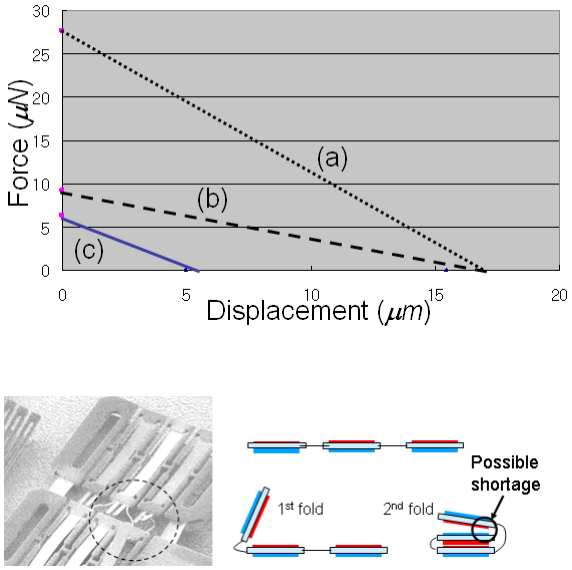
Sponsorship: Korea Institute of Metallurgy and Manufacturing

A muscle-inspired linear actuator that combines many piezoelectric micro-actuator "cells" into a single functional collection is designed and fabricated via a folding assembly technique. A triplet of individually contractive MEMS actuator cells is designed and fabricated in series and three triplets are assembled by folding them out-of-plane around gold ribbon hinges. A triplet demonstrates peak unblocked displacement of 15.24μm, which is about 30 times amplification of the PZT strain at 10V stimulus. The loaded displacement measurements predict the 9.21μN blocking forces for the single triplet. Since the motion of the end effecter is linear and in plane, the device is arrayable in series. The use of flexible gold ribbon hinges and the folding method out-of-plane allows assembly of strings of actuators around the hinges [1].

The final goal of this study is to array these actuators massively in series and in parallel to make a linear actuator like an artificial muscle bundle. An improved folding assembly method such as a stacking assembly will be used to assemble hundreds of discrete piezoelectric MEMS actuators. This muscle-like actuator can be attached directly to the skeletal structure without tendon wires and additional transmission mechanisms, simplifying micro-robot systems.



▲ Figure 1: Three unfolded triplet actuators (top), folding process (middle), and folded triplet actuators (bottom).



▲ Figure 2: Actuator performance curves of single triplet actuator (b), calculated (a) and measured (c) folded three triplet actuators (up), and possible defects (disconnection or shortage) causing low performance of actuator (below).

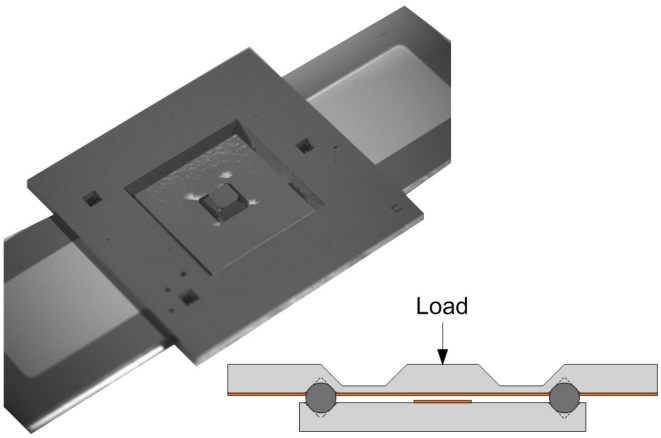
Reference

[1] S.-G. Kim, Z. Traina and H.W. Lee, "Folding assembly of microactuators," *Annals of the Journal of Manufacturing System*, 2008, to be published.

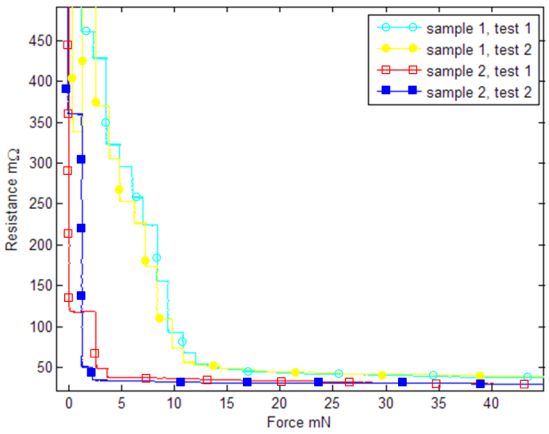
A System for Measuring Micro-scale Contact Resistance

M. Read, A. Weber, R. Martens, A.H. Slocum, J.H. Lang
Sponsorship: NSF

Designing devices utilizing micro-scale electrical contacts requires a precise knowledge of the relationship between contact force and contact resistance [1]. This relationship must be obtained experimentally because traditional contact theory does not always hold at the micro-scale, particularly at very low contact forces [2]. Additionally, this relationship has been shown to change with repeated cycling. The changes in this relationship are linked to physical changes of the contacts [3]. A system has been developed that measures the relationship between contact force and contact resistance for flat-on-flat micro-scale electrical contacts and also permits the contacts to be observed intermittently during testing [4]. This system is composed of two separate coupons, each containing a metal trace of the contact material and three KOH-etched pits. The coupons are assembled by placing stainless steel ball bearings into the KOH-etched pits of the bottom coupon and then placing the pits of the top coupon over the balls. An integrated flexure on the top coupon allows the metal traces to be brought into and out of contact, as shown in Figure 1. This kinematic coupling configuration allows the coupons to be assembled and reassembled with a repeatability on the order of a few microns [5]. During testing the metal traces are brought into contact while a load cell measures force and an integrated Kelvin structure measures contact resistance, as Figure 2 shows. This type of measurement has previously been used to measure the contact resistance of carbon nanotubes [6]. The contact surfaces are then separated and observed with an SEM. The cycle of repeated measurements and observation of the contact surface can be used to quantify the relationship between contact resistance and contact force and describe how this relationship and the physical attributes of the contact surface change with cycling.



▲ Figure 1: An image of the completed device along with a schematic that shows how the metal traces are brought into and out of contact with each other when a load or displacement is applied to the integrated flexure within the top coupon.



▲ Figure 2: The measurement of contact resistance versus contact force for two different devices with each test repeated twice. The contact material for both devices was 7000 Å of evaporated Au with a contact area of 4 mm^2. The differences between devices were attributed to contaminants found on device 1.

References

[1] A.C. Weber, J.H. Land, and A.H. Slocum, "The {111} Si etched planar electrical contacts for power MEMS-relays," in *Proc. 53rd IEEE Holm Conference on Electrical Contacts*, Pittsburg, PA, Sept. 2007, pp. 156-159.

[2] R.S. Timsit, "Electrical conduction through small contact spots," *IEEE Transactions on Components and Packaging Technologies*, vol. 26, no. 4, pp. 727–734, Dec. 2006.

[3] D. Hyman and M. Mehregany, "Contact physics of gold microcontacts for MEMS switches," *IEEE Transactions on Components and Packaging Technologies*, vol. 22, no. 3, pp. 357-364, Sept. 1999.

[4] M.B. Read, A.C. Weber, R. Martens, O. Yaglioglu, J.H. Lang, and A.H. Slocum "A highly repeatable MEMS based electrical contact test system," in *Proc. 10th EUSPEN International Conference*, Zürich, Switzerland, May 2008.

[5] M.B. Read, A.C. Weber, R. Martens, O. Yaglioglu, J.H. Lang, and A.H. Slocum, "A two-coupon system for the repeatable measurement of flat on flat microscale contact resistance," presented at *Proc. 24th International Conference on Electrical Contacts*, Saint Malo, France, June 2008.

[6] O. Yaglioglu, A.J. Hart, R. Martens, and A.H. Slocum, "Method of characterizing electrical contact properties of carbon nanotube coated surfaces," *Review of Scientific Instruments*, vol. 77, pp. 095105:1-3, Sept. 2006.

A MEMS-Relay for Make-Break Power-Switching Applications

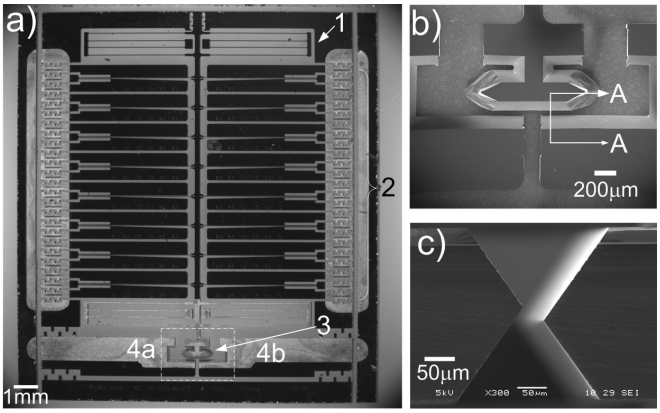
A.C. Weber, J.H. Lang, A.H. Slocum

Sponsorship: NSF

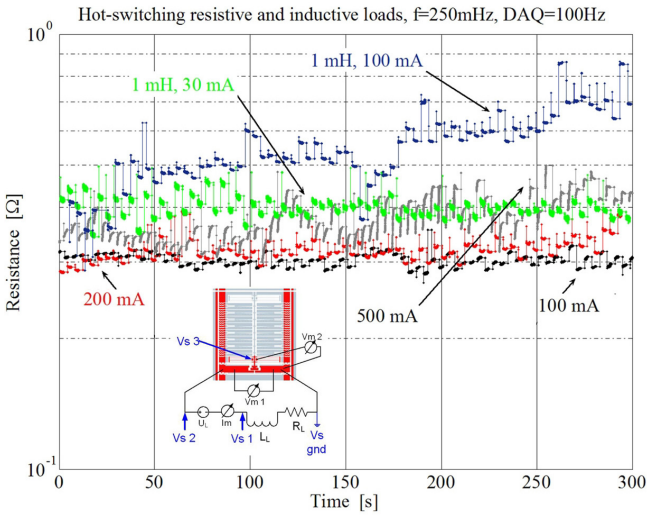
We present a horizontal-displacement, electrostatically-actuated, MEMS relay for make-break power switching applications. The relay features {111}-plane silicon-etched electrical contacts. Experimental relays exhibit a minimum total on-state contact resistance of 130 mΩ, a response time of 750 µs, a theoretical electrical isolation in excess of 1 kV (tested to 450 V with available equipment), and a current-carrying capacity of 800 mA. The MEMS relay has been hot-switched in excess of 10^5 cycles without signs of performance degradation [1].

The relay, shown in Figure 1, is composed of four double-parallelogram flexures (1) that serve as bearings, eight pairs of engaging and disengaging electrostatic "zipper" actuators (2), one moving {111} contact (3), and a pair of static {111} contacts (4a, 4b). The {111}-plane contacts [2] offer several advantages over traditional MEMS-relay metal contacts: they provide large travel, on the order of 70 µm, which exceeds the 30 µm required to withstand contact erosion and the 10 µm required to prevent arcing while operating in air at atmospheric pressure; the oblique contact geometry introduces contact wipe, which is known to enhance the contact reliability; and the contact geometry allows for an enhanced metallization process that provides low on-state contact resistance. The relay is etched in (100) Si through a combination of KOH etching and DRIE using nested masks. After evaporation of a gold seed-layer on the contacts using a shadow mask, the silicon is bonded to a glass substrate. Next, the contacts are plated with a 10-µm-thick copper and a 2-µm-thick palladium-cobalt film. The device is released by dicing and packaged in a pin grid array for testing.

During testing, voltages and currents were continuously monitored as the relay cycled, and the instantaneous total contact resistance was computed, as shown in Figure 2. The load current and voltage were increased until the relay showed any signs of temporary contact-sticking during any actuation cycle throughout the test. The maximum hot-switched current achieved without any signs of contact sticking was 800 mA with a resistive load and 350 mA with a 1 mH inductive load. While operating at or below these currents, the MEMS relay was hot-switched in excess of 10^5 cycles without signs of performance degradation. While the device operated at higher currents than the threshold, the sticking phenomenon was found to occur sporadically and to be reversible. Once stuck, the contacts recovered after the relay was cycled with the load disconnected.



▲ Figure 1: Fabricated relay. (a) Die top view. (b) Contact detail, prior to metal deposition. (c) Contact cross-section A-A, as shown in Figure 1b, without the metal film.



▲ Figure 2: Continuous sampling of total contact resistance during hot-switching. Inset: Experimental setup.

References

[1] A.C. Weber, J.H. Lang, and A.H. Slocum, "A MEMS-relay for Make-Break Power Switching Applications," to be presented at the *Solid State Sensor and Actuator Workshop*, Hilton Head, SC, June, 2008.

[2] A.C. Weber, J.H. Lang, and A.H. Slocum, "{111} Si Etched Planar Electrical Contacts for Power MEMS Relays," in *Proc. 53rd IEEE Holm Conference on Electrical Contacts*, Pittsburgh, PA, 2007, pp. 156-159.

Fabrication and Testing of a Fully-Integrated Multiwatt TurboGenerator

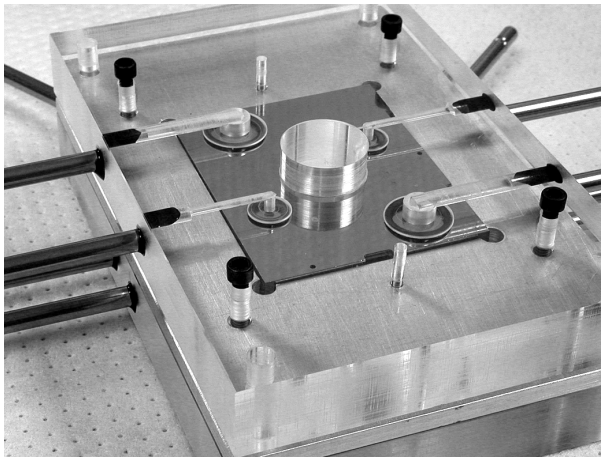
B.C. Yen, M. Allen, F.F. Ehrich, A.H. Epstein, F. Herrault, K.J. Hillman, L.C. Ho, S. Jacobson, J.H. Lang, H. Li, Z.S. Spakovszky, C.J. Teo, D. Veazie

Sponsorship: US Army Research Laboratory Collaborative Technology Alliance

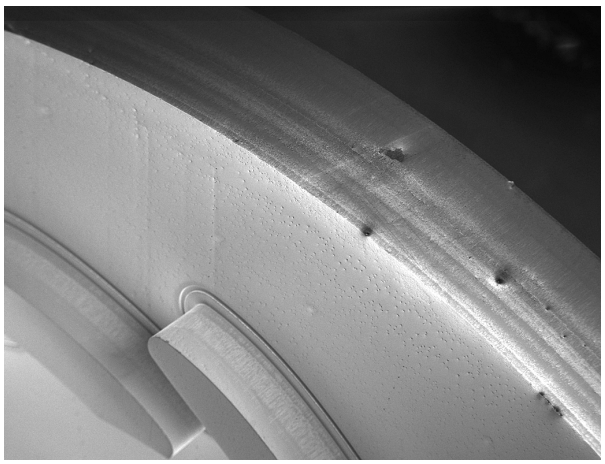
There is a need for compact, high-performance power sources that can outperform the energy density of modern batteries for use in portable electronics, autonomous sensors, robotics, and other applications. The current research aims to produce a fully-integrated, synchronous permanent magnet microturbogenerator capable of generating 10 W DC output power using compressed air as its energy source. Past conference abstracts by Yen, et al. [1, 2] focused on the theoretical design as well as core fabrication procedures and techniques. Presently, all the silicon die fabrication is complete, and the magnetic components are being integrated onto the die in preparation for power generation testing.

While the magnetic integration is in progress, efforts are underway to separately test and qualify the gas-lubricated bearings that will support the magnetic rotor to very high speeds. To make the tests relevant, they are conducted on silicon dies similar to the final generator dies, with the only differences being the lack of surface windings and a laminated magnetic stator. Figure 1 shows a bearing rig die enclosed in an acrylic package, as well as the metal tubulations and o-rings used to bring nitrogen into the die.

Three sets of bearing rig tests are currently planned. A light rotor made purely of silicon and shown in Figure 2 will be used to assess the nominal imbalance, defined as the distance between the geometric and mass center of the rotor, introduced by the fabrication process. This rotor has approximately half the mass of the magnetic rotor, so a solder-filled rotor twice as heavy will be tested next to determine whether the bearings perform well with a massive rotor. After these two sets of experiments are complete, the magnetic rotor, which has permanent magnets and a soft magnetic back iron embedded in it, will be characterized. Because the silicon die can be easily opened along its eutectic interface [2], it is anticipated that the magnetic rotor can be removed from the die after testing and reused for the generator die.



▲ Figure 1: A fully bonded heavy bearing rig silicon die enclosed in an acrylic package ready for testing. Nitrogen required for pressurizing the gas bearings and accelerating the rotor is fed in through an array of metal tubulations attached to the package using epoxy.



▲ Figure 2: Close-up SEM photo showing the journal bearing etch around the silicon rotor. A few recessed craters are visible, but the 900-µm sidewall is otherwise straight as expected. The rotor blades, created using a halo etch, are visible on the rotor surface.

References

[1] B.C. Yen, M. Allen, F.F. Ehrich, A.H. Epstein, F. Herrault, K.J. Hillman, L.C. Ho, S. Jacobson, J.H. Lang, H. Li, Z.S. Spakovszky, C.J. Teo, and D. Veazie, "An integrated multiwatt permanent magnet turbine generator," in *Proc. MTL Annual Research Conference,* January 2006.

[2] B.C. Yen, *et al.*, "Fabrication of a fully-integrated multiwatt µturbogenerator," in *Proc. MTL Annual Research Conference*, January 2007.

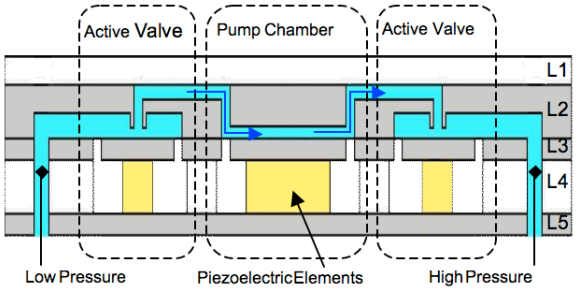
MEMS Micro-vacuum Pump for Portable Gas Analyzers

V. Sharma, M.A. Schmidt
Sponsorship: DARPA

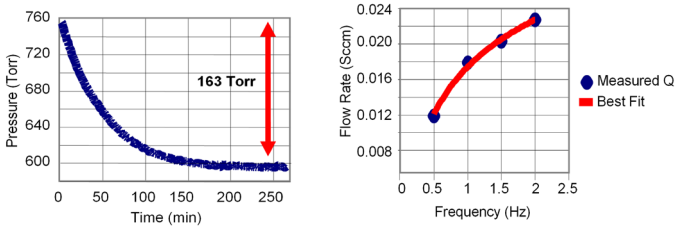
There are many advantages to miniaturizing systems for chemical and biological analysis. Recent interest in this area has led to the creation of several research programs, including a Micro Gas Analyzer (MGA) project at MIT. The goal of this project is to develop an inexpensive, portable, real-time, and low-power approach for detecting chemical and biological agents. Elements entering the MGA are first ionized, then filtered by a quadrupole array, and sensed using an electrometer. A key component enabling the entire process is a MEMS vacuum pump, responsible for routing the gas through the MGA and increasing the mean free path of the ionized particles so that they can be accurately detected.

A great deal of research has been done over the past 30 years in the area of micro pumping devices [1, 2]. We are currently developing a displacement micro-vacuum pump that uses a piezoelectrically driven pumping chamber and a pair of piezoelectrically driven active-valves; the design is conceptually similar to the MEMS pump reported by Li et al. [3]. We have constructed an accurate compressible mass flow model for the air flow [4] as well as a nonlinear plate deformation model for the stresses experienced by the pump parts [5]. Using these models, we have defined a process flow and fabricated five generations of the MEMS vacuum pump over the past years and are currently working on improving the overall design.

Figure 1 shows a schematic of the pump. For ease in testing we have initially fabricated only layers 1-3 and have constructed a testing platform which, under full computer control, drives the pistons and monitors the mass flows and pressures at the ports of the device. The lessons learned from the first four generations of the pump have led to numerous improvements. Every step from the modeling, to the etching and bonding, to the testing has been modified and improved along the way. The most recent fifth generation pump test data appears in Figure 2. Figure 2a shows the measurements of the vacuum being generated in an external volume (5.6cm^3) by the micropump operating at 2Hz. The pump was able to reduce the external volume pressure by 163 Torr. Figure 2b shows the micropump-generated flow rate as a function of pumping frequency (driven in a 6-stage cycle by a controlling microprocessor to move the gas from the input to the output). The performance of this pump compares very well with that of other similar scaled micropumps in the literature. Next, we plan to fabricate and test an improved overall design and develop a final set of models to fabricate any future micropumps to the desired specifications.



▲ Figure 1: The MEMS vacuum pump schematic. Layers 1 and 4 are glass, layers 2 and 5 forming the chambers, channels, and support are silicon, and layer 3 forming the pistons and tethers is SOI silicon



▲ Figure 2: a) The vacuum generation performance of the micropump. b) The pump-generated flow rate as a function of the pumping frequency.

References

[1] D.J. Laser and J.G. Santiago, "A review of micropumps," *Journal of Micromechanics and Microengineering*, vol. 14, no. 6, pp. 35-64, 2004.

[2] P. Woias, "Micropumps--past, progress and future prospects," *Sensors and Actuators B: Chemical*, vol. 105, no. 1, pp. 28-38, 2005.

[3] H.Q. Li, D.C. Roberts, J.L. Steyn, K.T. Turner, J.A. Carretero, O. Yaglioglu, Y.-H. Su, L. Saggere, N.W. Hagood, S.M. Spearing, M.A. Schmidt, R. Mlcak, and K. Breuer, "A high-frequency, high flow rate, piezoelectrically driven MEMS micro-pump," *IEEE Solid State Sensors and Actuators Workshop*, Hilton Head SC, June 2000.

[4] A.K. Henning, "Improved gas flow model for micro-valves," *Proceedings of Transducers 2003*, Boston, MA, pp. 1550-1553, June 2003.

[5] D.C. Roberts, O. Yaglioglu, J.Carretero, Y.-H Su, L. Saggere, and N.W. Hagood, "Modeling, design, and simulation of a piezoelectrically driven microvalve for high pressure, high frequency applications," in *Proc. SPIE–The International Society for Optical Engineering, Smart Structures and Materials 2001–Smart Structures and Integrated Systems*, Newport Beach, CA, Mar. 2001, pp. 366-380.

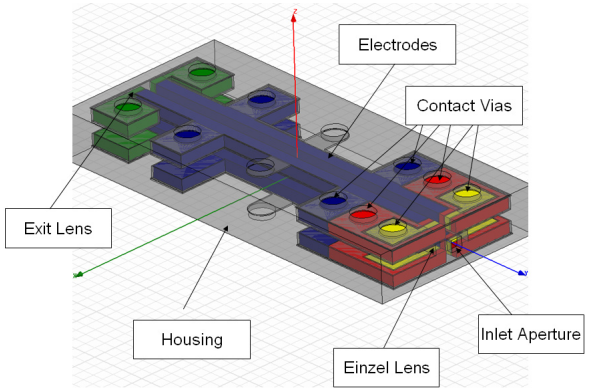
Batch-fabricated Linear Quadrupole Mass Filters

K. Cheung, L.F. Velasquez-Garcia, A.I. Akinwande
Sponsorship: DARPA

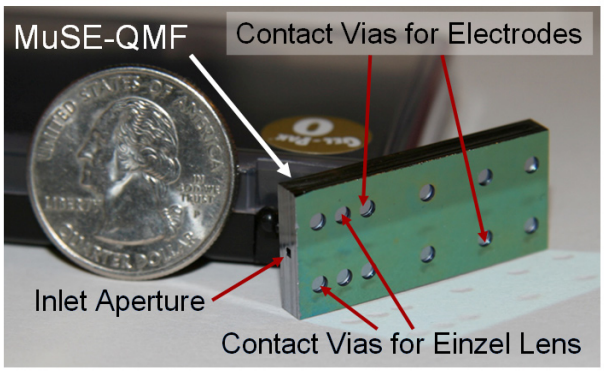
In recent years, there has been a desire to scale down linear quadrupoles. The key advantages of this miniaturization are the portability it enables and the reduction of pump power needed due to the relaxation on operational pressure. Attempts at making microelectromechanical systems-based linear quadrupoles met with varying degrees of success [1-3]. Producing these devices involved some combination of precision machining or microfabrication and downstream assembly. For miniature quadrupole mass filters to be mass-produced cheaply and efficiently, manual assembly should be removed from the process.

A purely microfabricated quadrupole mass filter consisting of a planar design and a rectangular electrode geometry has been made. Rectangular rods were utilized since they are most amenably shaped for planar microfabrication. This deviation from the conventional round rod geometry required optimization and analysis. After we minimized unwanted effects through various simulations, we proposed a design (Figure 1), conceived a process flow, and fabricated the Micro-Square Electrode Quadrupole Mass Filter (MuSE-QMF) (Figure 2). The process requires the bonding of five silicon wafers and the use of deep reactive ion etching to pattern the features. It is a relatively simple process, furthering the case for mass-production of these devices.

This non-conventional design will introduce non-linear resonances that manifest as peak splitting in the mass spectrum. Reported work involving linear quadrupoles operated in the second stability region shows improved peak shape without these splits [3]. It is believed that operating this device in the second stability region will provide a means to overcome the nonlinear resonances introduced by the square electrode geometry. Successful implementation of this device will lead into arrayed configurations for parallel analysis and aligned quadrupoles operated in tandem for enhanced resolution.



▲ Figure 1: Schematic of proposed device.



▲ Figure 2: Fabricated device.

References

[1] M. Gear, R.R.A. Syms, S. Wright, and A.S. Holmes, "Monolithic MEMS quadrupole mass spectrometers by deep silicon etching," *Journal of Microelectromechanical Systems*, vol. 14, no. 5, pp. 1156-1166, Oct. 2005.

[2] J.J Tunstall, S. Taylor, R.R.A. Syms, T. Tate, and M.M. Ahmad, "Silicon micromachined mass filter for a low-power, low-cost quadrupole mass spectrometer," in *Proc. IEEE Eleventh Annual International Workshop on Micro Electro Mechanical Systems*, Heidelberg, Germany 1998, pp. 438-442.

[3] L.F. Velazquez-Garcia, K. Cheung, and A.I. Akinwande, "An application of 3D MEMS packaging: Out-of-plane quadrupole mass filters," *Journal of Microelectromechanical Systems*, submitted for publication.

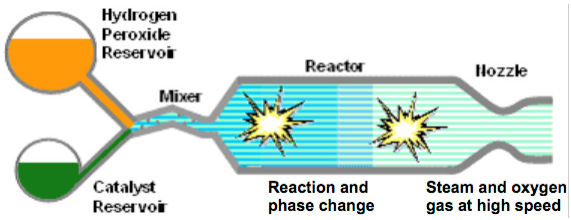
MEMS Ejector Pumps Driven by MEMS Steam Generators

F. Eid, L.F. Velasquez-Garcia, C. Livermore
Sponsorship: DARPA, MDA, AFRL

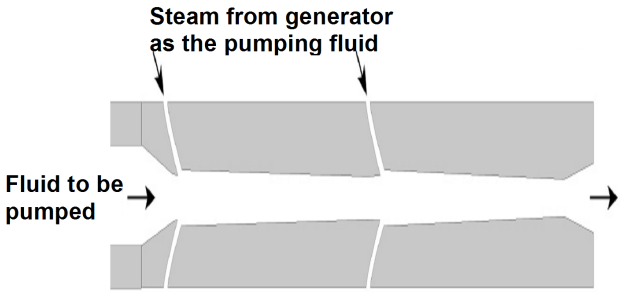
Vacuum pumping of gases at the MEMS scale is an ongoing challenge; MEMS pumps typically have pressures far above and pumping rates far below those of their macroscale counterparts. To meet this challenge, we are creating high-mass-flow-rate MEMS steam-ejector pumps that are driven by MEMS-based steam generators. Ejector pumps scale favorably to the MEMS scale because the entrainment of the flow to be pumped by the driving fluid takes place over a much shorter distance in a narrow, millimeter-scale channel than in a wide macroscale channel [1]. However, delivering driving fluid from a compact source remains a significant challenge. Our solution to this challenge is MEMS steam generators that decompose hydrogen peroxide with a liquid catalyst in order to produce the ejectors' driving fluid. The creation of MEMS steam generators enables the creation of systems of high-performance MEMS pumps.

One important objective of this work is the design, fabrication, and demonstration of the MEMS steam generator to drive the pumps. The generator decomposes hydrogen peroxide using a homogeneous (liquid) catalyst to produce steam, which is then accelerated through a nozzle to the high velocities required for effective pumping. Hydrogen peroxide is selected for its availability and environmental friendliness. The use of a liquid catalyst eliminates common problems of catalyst poisoning and aging, and the system is sized and designed to minimize thermal losses and enable complete decomposition of the peroxide.

Our work to date has primarily focused on the design and modeling of the steam generator and its interface with the pumps. Conceptually, the MEMS steam generator consists of a microscale mixer, a reactor, and a converging-diverging nozzle to accelerate the exiting flow, as shown in Figure 1. One or more steam generators would be coupled to a MEMS ejector as shown in Figure 2. Liquid H_2O_2 is mixed with the catalyst in the generator's "engulfment" mixer [2] and then injected into the reactor, where the peroxide decomposes into steam and oxygen gas. The mixing timescale is much less than the reaction timescale, so that the reaction and vaporization take place in uniformly-mixed fluid inside the reaction chamber. The gaseous products are then accelerated to supersonic velocities through the converging-diverging nozzle. Models predict adequate thermal management and high performance for the generator-driven MEMS pumping system. The research now focuses on the realization and experimental demonstration of the MEMS steam generator to drive the MEMS pumping system.



▲ Figure 1: Schematic diagram of a hydrogen peroxide-based MEMS steam generator, showing the mixer, reactor, and nozzle



▲ Figure 2: Integration of MEMS steam generators with an ejector unit

References

[1] B.A. Wilhite, C. Livermore, Y. Gong, A.H. Epstein, and K.F. Jensen, "Design of a MEMS-based microchemical oxygen-iodine laser (mCOIL) system," *IEEE Journal of Quantum Electronics*, vol. 40, pp. 1041-1055, Aug. 2004.

[2] N. Kockmann and P. Woias, "Flow regimes and mass transfer characteristics in static micromixers," *Proc. of SPIE*, vol. 4982, pp. 319, 2003.

Micro-Reaction Technology for Energy Conversion

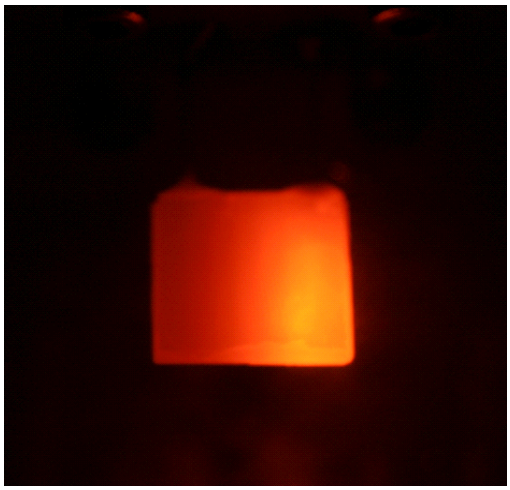
B. Blackwell, K. Deshpande, J. Keybl, C. Marton, M.A. Schmidt, K.F.Jensen

The development of portable-power systems remains an important goal, with applications ranging from the automobile industry to the portable electronics industry. The focus of this work is to develop microreaction technology that converts fuels – such as light hydrocarbons and their alcohols-- to hydrogen for use in solid oxide fuel cells or directly into electricity. Developing high-efficiency devices requires addressing difficulties in high temperature operation: specifically, thermal management, material integration, and improved packaging techniques. In addition, recent work has included efforts to harness energy rejected to the environment as heat.

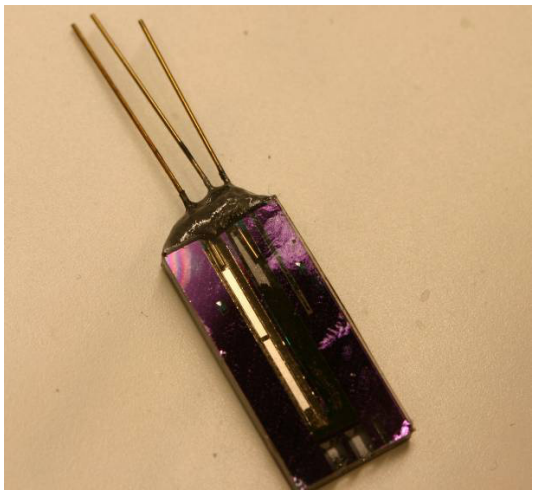
The microreactor designed for combustion has been improved, resulting in longer residence times within the reactor. This longer residence time ensures full combustion of propane fuel over a platinum catalyst. The channels within the reactor are etched using wet potassium hydroxide, which is the most economical etch technique available. The reactor remains suspended via thin-walled glass tubes, reducing conductive heat losses and allowing the reactor to operate at high temperatures. The tubes are brazed to the microreactor using a thermally-matched glass braze technique that was developed in-house. The coupling of two reactors has allowed for combustion to occur in one and ammonia cracking in the other, resulting in autothermal hydrogen generation.

A combined reforming/separation device has been developed and demonstrated. Specifically, the hydrogen generation unit combines a 200-nm-thick palladium-silver film with a methanol reforming catalyst, e.g., LaNiCoO3. The catalytic combustion unit employs a platinum catalyst. Both units are formed in a silicon wafer by bulk silicon micromachining techniques. The energy generated in the combustion unit is efficiently transferred to the hydrogen production unit in the thermal conduction of silicon support. With a modified brazing technique, the reactor is thermally insulated from its environment. The system has been demonstrated to purify hydrogen at elevated pressures (up to 2 atm). Joint combustion/purification of the system has also been demonstrated, in which combustion and reforming occur simultaneously with the purification of the resulting hydrogen.

Recent work has also included efforts to harness waste heat in the form of electrical energy. Thermophotovolatics (TPV) cells are being integrated to harness radiation energy. Work is also ongoing to integrate thermoelectric (TE) devices to harness waste heat through intimate contact of the TE device with the microreactor.



▲ Figure 1: Autothermal, steady-state combustion of 9.5-sccm butane over 2.5 mg of 1wt% Pt on Al_2O_3. The temperature of the hotspot was 830°C.



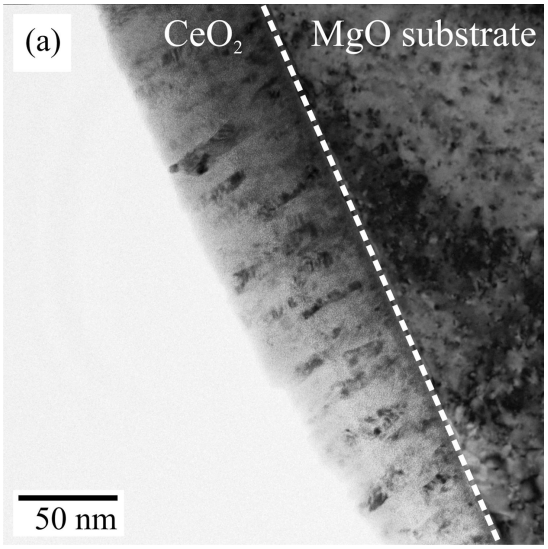
▲ Figure 2: Combined reforming/separation device. The three fluidic connections are for reactant gases, combusted gases, and purified hydrogen.

Microfabricated Thin-film Electrolytes and Electrodes for Solid Oxide Fuel-cell Electrodes

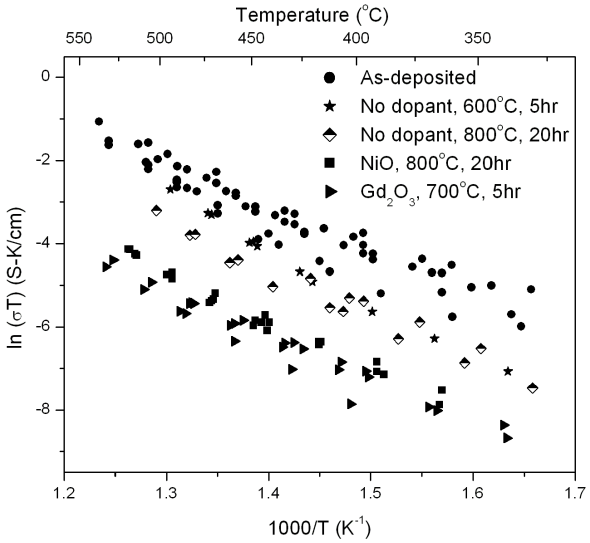
S.J. Litzelman, W.C. Jung, K. Sahner, H.L. Tuller
Sponsorship: National Science Foundation, DMR-0243993

Micro-solid oxide fuel cells (SOFCs) are currently under intense investigation for portable power applications, such as notebook computers and mobile phones [1, 2]. While thin-film nanostructured solid electrolytes result in lower cell losses due to ohmic resistance, grain boundaries may serve as fast diffusion pathways for cations, resulting in poorer long-term stability. The effects of grain boundary chemistry and interdiffusion on ionic transport have yet to be systematically investigated.

To explore the relationship between performance and stability, CeO_2 thin films were grown by pulsed laser deposition (PLD), as shown in a transmission electron micrograph (TEM) in Figure 1 [3]. Thin diffusion sources of NiO and Gd_2O_3 were deposited, and samples were annealed in the temperature range of 700-800 °C to in-diffuse the Ni cations heterogeneously along the grain boundaries. Confirmation of diffusion along the grain boundaries was achieved via time-of-flight secondary ion mass spectrometry (ToF-SIMS). After modification, the diffusion source was removed by a wet etching process, and Pt microelectrodes were prepared via a photolithographic lift-off process. The electrical conductivity was measured by impedance spectroscopy and two-point DC techniques, and it decreased 10x following grain boundary in-diffusion. These results are being modeled by examination of changes in charge-carrier profiles induced by the in-diffusion in the space charge region adjacent to the boundary.



▲ Figure 1: Cross-sectional TEM image of CeO_2, showing parallel columnar grain boundaries and grain sizes of approximately 25-40 nm.



▲ Figure 2: Electrical conductivity of as-deposited and modified CeO_2, which decreases upon in-diffusion but without any clear change in the thermal activation energy.

References

[1] C.D. Baertsch, K.F. Jensen, J.L. Hertz, H.L. Tuller, S.T. Vengallatore, S.M. Spearing, and M.A. Schmidt, "Fabrication and structural characterization of self-supporting electrolyte membranes for a micro solid-oxide fuel cell," *Journal of Materials Research*, vol. 19, no. 9, pp. 2604-2615, Sept. 2004.

[2] D. Nikbin, "Micro SOFCs: Why small is beautiful," *The Fuel Cell Review*, vol. 3, no. 2, pp. 21-24, Apr. 2006.

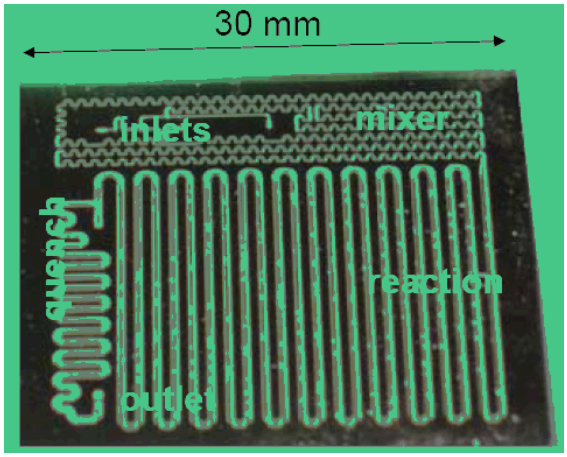
[3] S.J. Litzelman, R.A. De Souza, B. Butz, H.L. Tuller, M. Martin, and D. Gerthsen, "Heterogeneously doped nanocrystalline ceria films by grain boundary diffusion: Impact on transport properties," *Journal of Electroceramics*, DOI: 10.1007/s10832-008-9445-y, 2008.

Chemical Synthesis with Online Optimization in Microreactor Systems

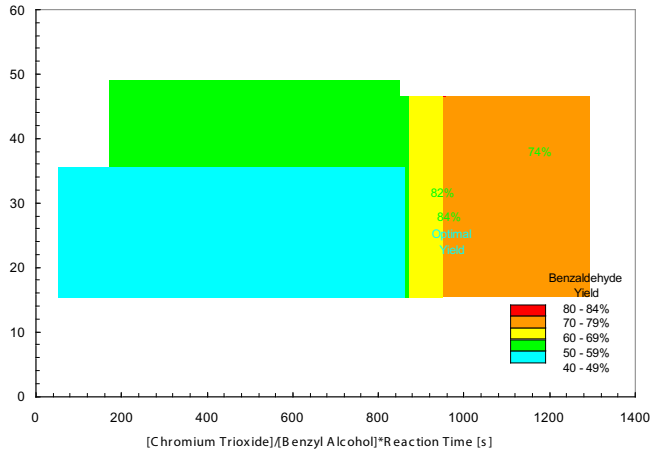
J.P. McMullen, N. Zaborenko, H.R. Sahoo, K.F. Jensen
Sponsorship: MIT Microreactor Consortium

Microreactors are powerful instruments for scanning and optimizing chemical reactions due to their enhanced heat and mass transfer, reduced reaction volume, and the ability to run several experiments in parallel. Applying fabrication principles that have been developed for integrated circuits, such as lithography, deep reactive ion etching (DRIE), oxidation, anodic bonding, and electron beam metal deposition, microreactors can be designed to accommodate a comprehensive set of chemistries. In addition to the study of chemical reactions under these enhanced conditions, such as high temperature and high pressure, use of other process components such as mixers, heat exchangers, and phase separators can be incorporated on a chip to provide a multifunctional microreactor (Figure 1). Previous work in our group has focused on exploiting these benefits in order to determine optimal reaction conditions (e.g., temperature, pH, etc.) quickly, as well as to accurately evaluate the reaction kinetics for chemical syntheses related to pharmaceutical and fine chemistry sectors.[1, 2]

Microreactors can also be integrated with physical sensors to provide online measurement of process variables. Pressure sensors can be used to determine liquid flow rates, and temperature sensors are readily integrated by using thin film resistors or by incorporating a thin thermocouple. The progress of the chemical reaction can be monitored on-chip through UV/Vis, infrared, or Raman spectroscopy. Incorporating these measurements with traditional feedback control and optimization algorithms enables the optimization procedure to be completely automated. Such an 'intelligent' microreactor system was applied experimentally for a multi-step reaction, the oxidation of benzyl alcohol by chromium trioxide to benzaldehyde with further oxidation to benzoic acid, to determine the conditions that maximize the yield of the intermediate, benzaldehyde. In a multi-parameter (e.g., reaction temperature and reagent flow rates) optimization approach, the system performed approximately 30 experiments in a completely automated fashion to determine the optimal yield of 82 – 84% (Figure 2).



▲ Figure 1: Microreactor is integrated with mixer and quench zone for accurate optimization and kinetic studies. Mixing channels are 200 x 400 µm and reaction channels are 400 x 400 µm in cross section.



▲ Figure 2: Benzaldehyde yield for experimental conditions automatically performed by multiple parameter optimization platform. Contours of benzaldehyde yield are shown for different reaction temperatures and for a lumped variable defined by the product of the ratio of the initial concentrations of chromium trioxide to benzyl alcohol and reaction time for 2-D representation of data collected over a 4-parameter (4D) optimization.

References

[1] E.R Murphy, J.R. Martinelli, N. Zaborenko, S.L. Buchwald, and K.F. Jensen, "Accelerating reactions with microreactors at elevated temperatures and pressures: Profiling aminocarbonylation reaction," *Angewandte Chemie, International Edition*, vol. 46, pp. 1734-1737, 2006 .

[2] D.M. Ratner, E.R. Murphy, M. Jhunjhunwala, D.A. Snyder, K.F. Jensen, and P.H. Seeberger, "Microreactor-based reaction optimization in organic chemistry – Glycosylation as a challenge," *Chemical Communications*, vol. 5, no. 5, pp. 578-580, 2005.

Novel Synthesis of Polymeric Nanoparticles for Drug Delivery Applications Using Microfluidic Rapid Mixing

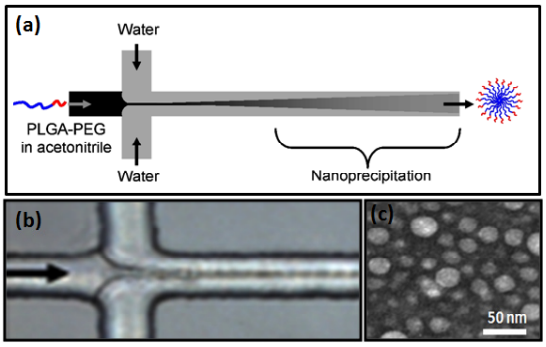
P. Valencia, F. Gu, P. Basto, L. Zhang, C. Cannizzaro, R.S. Langer, O. Farokhzad, R. Karnik

Sponsorship: National Cancer Institute

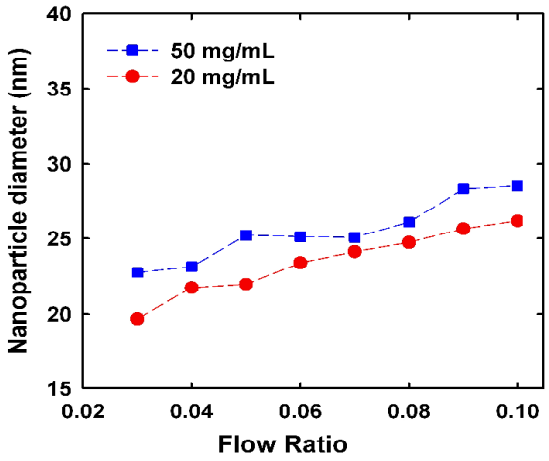
The development of smart targeted nanoparticles (NPs) that can deliver drugs at a sustained rate directly to specific cells may provide better efficacy and lower toxicity for treating many diseases. For these applications, control of the NP properties such as size and polydispersity is of utmost importance for the particles' end therapeutic effects. Here we report the use of rapid microfluidic mixing using hydrodynamic flow focusing to control self-assembly of polymeric NPs. Self-assembly occurs through nanoprecipitation, a process that involves dilution of a block copolymer from a solvent to an anti-solvent resulting in the precipitation of NPs [1]. We demonstrated that through the rapid mixing of precursors with anti-solvent (i.e., water), the particle size could be tuned and more homogeneous NPs could be synthesized. This work is the first implementation of nanoprecipitation on a microfluidic platform.

The PDMS microfluidic devices were used to synthesize PLGA-PEG NPs by mixing PLGA7400-PEG3500 in acetonitrile (50 mg/ml) with water (anti-solvent). Hydrodynamic focusing was achieved by controlling flow rates with syringe pumps. Figure 1 shows the polymer stream being focused by two water streams as well as a TEM image of the resulting NPs. Figure 2 shows the change in PLGA-PEG particle size as mixing time is varied. Mixing time (~ 1-10 ms) can be tuned by changing the flow ratio of the solvent to anti-solvent. These results agree with the idea that self-assembly of block copolymers into NPs by nanoprecipitation yields smaller particles as mixing time is decreased [2].

This work demonstrates that microfluidic synthesis of polymeric nanoparticles with rapid mixing allows for tuning of NP size and distribution through control of flow rates. These results lay the foundations of a microfluidic platform for controlled synthesis of NPs that may result in improved performance in drug delivery applications.



▲ Figure 1: (a) Schematic of synthesis of nanoparticles by nanoprecipitation using hydrodynamic flow focusing. (b) Micrograph of the 20x60-µm device in operation. Flow rates of the polymer and water streams are 2 µl/min and 20 µl/min (total), respectively. (c) A TEM image of nanoparticles synthesized



▲ Figure 2. Effect of flow ratio on nanoparticle size. Increasing the polymer stream flow rate and keeping the water stream flow rate constant (20 µl/min) results in larger nanoparticles. Mixing time increases as the polymer stream flow rate increases.

References

[1] J. Cheng, B.A. Teply, I. Sherifi, J. Sung, G. Luther, F. Gu, E. Levy-Nissenbaum, A.F. Radovic-Moreno, R. Langer, and O.C. Farokhazad, "Formulation of functionalized PLGA-PEG nanoparticles for in vivo targeted drug delivery," *Biomaterials*, vol. 28, pp. 869-873, Oct. 2006.

[2] B.K. Johnson and R.K. Prud'homme, "Mechanism for rapid self-assembly of block copolymer nanoparticles," *Physical Review Letters*, vol. 91, no. 11, pp. 118302: 1-4, Sept. 2003.

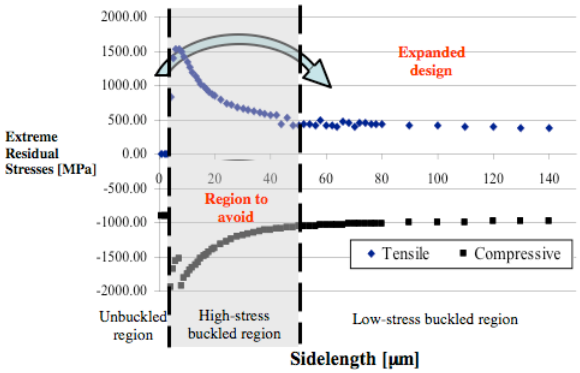
Design, Fabrication, and Testing of Multilayered, Microfabricated Solid Oxide Fuel Cells (SOFCs)

N. Yamamoto, D. Quinn, P. Capozzoli, N. Wicks, B.L. Wardle, S.M. Spearing (in coll. with B.A. Wilhite, J. Hertz, J. Cui, K.F. Jensen, H.L. Tuller, M.A. Schmidt)

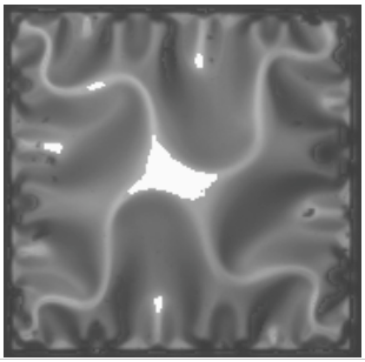
Sponsorship: ARO

Microfabricated solid oxide fuel cells were investigated for portable power applications requiring high energy densities [1]. The thickness of the electrolyte, the travel length of oxygen ions, was reduced down to ~150nm. The tri-layers (yttria-stabilized zirconia (YSZ) as an electrolyte and platinum-YSZ cermet as cathode/anode) were sputter-deposited on a silicon wafer, and then they were released as square plates by KOH-etching the silicon through patterned silicon nitride masks on the back side. High intrinsic and extrinsic (thermal) stresses due to fabrication and operation (25-600°C) [2], respectively, require careful thermomechanically stable design of μSOFCs.

First, material properties of the ultra-thin YSZ were characterized experimentally and found to be significantly different than those of bulk YSZ [3]. Second, based on the obtained properties, maximum stresses in the plates at 625°C were analyzed using non-linear von Karman plate theory [4]. The stresses showed three regions with sidelength variation: un-buckled regime, buckled regime with high stresses, and post-buckling regime with lower stresses (see Figure 1). The μSOFCs were fabricated in the post-buckling regimes with ~80-~180-μm sidelength and total ~450-nm thickness. With the plates buckled as shown in Figure 2, the μSOFCs produced power output of 0.008mW/cm, lower than the expected power from their electrochemical test. Given the high-performance predicted for the underlying nano-structured ultra-thin electrolyte, anode, and cathode layers, additional studies are needed to improve specimens and test setup and to assess μSOFCs' long-term operational stability.



▲ Figure 1: Maximum stress evolution with sidelength of YSZ square membranes with ~450nm thickness cycled to 600°C.



▲ Figure 2: Top-view of highly buckled, but unfailed, square membrane.

References

[1] C.D. Baertsch, et al., "Fabrication and structural characterization of self-supporting electrolyte membranes for a μSOFC," *Journal of Materials Research*, vol. 19, pp. 2604-2615, 2004.

[2] D.J. Quinn, M.S. Spearing, and B.L. Wardle, "Residual stress and microstructural evolution in thin film materials for a micro solid oxide fuel cell (SOFC)," *Materials Research Society Meeting*, Boston, MA, Nov. 2004.

[3] N. Yamamoto, "Thermomechanical properties and performance of microfabricated solid oxide fuel cell (μSOFC) structures," Masters' thesis, Massachusetts Institute of Technology, Cambridge, MA, 2006.

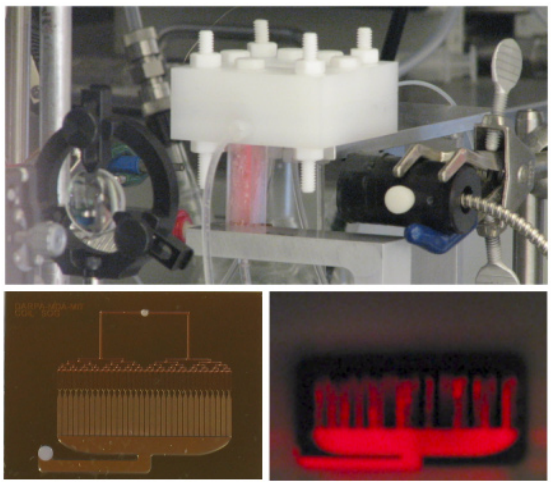
[4] N. Yamamoto, N. Wicks, and B.L. Wardle, "Twice-buckled cermet composite laminate under equibiaxial compression," in *Proc. 48th AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics, and Materials Conference*, Honolulu, HI, Apr. 2007.

Microscale Singlet Oxygen Generator for MEMS-based COIL Lasers

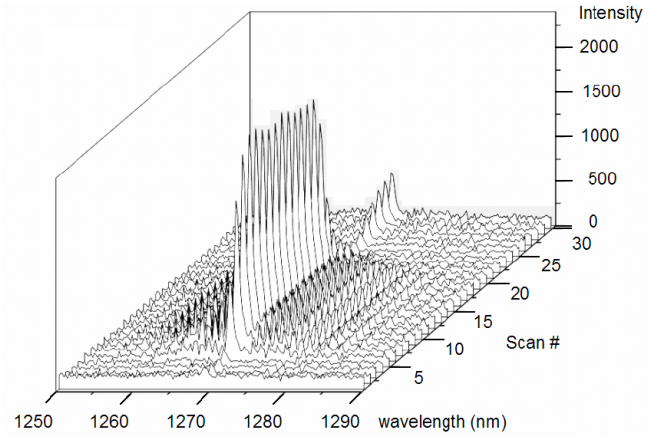
T. Hill, L.F. Velásquez-García, A.H. Epstein, K.F. Jensen, C. Livermore
Sponsorship: DARPA, MDA, AFRL

Conventional chemical oxygen iodine lasers (COIL) offer several important advantages for materials processing, including short wavelength (1.3 μm) and high power. However, COIL lasers typically employ large hardware and use reactants relatively inefficiently. This project is creating an alternative approach called microCOIL. In microCOIL, most conventional components are replaced by a set of silicon MEMS devices that offer smaller hardware and improved performance. A complete microCOIL system includes microchemical reactors, microscale supersonic nozzles, and micropumps. System models incorporating all of these elements predict significant performance advantages in the microCOIL approach [1].

Initial work is focused on the design, microfabrication, and demonstration of a chip-scale singlet oxygen generator (SOG), a microchemical reactor that generates singlet delta oxygen gas to power the laser. Given the extensive experience with micro-chemical reactors over the last decade [2], it is not surprising that a microSOG would offer a significant performance gain over large-scale systems. The gain stems from basic physical scaling; surface-to-volume ratio increases as the size scale is reduced, which enables improved mixing and heat transfer. The SOG chip being demonstrated in this project employs an array of microstructured packed-bed reaction channels interspersed with microscale cooling channels for efficient heat removal [3]. To date the device has produced oxygen concentrations of 10^{17} cm^{-3}, yields approaching 80%, and molar flowrates in excess of $600x10^{-4}$ moles/L/sec [4]. The yield and molar flowrates indicate a significant improvement over the macroscale SOG designs.



▲ Figure 1: A) View of chip surface showing glow resulting from singlet-oxygen production. B) View of packaging and optics surrounding microSOG. C) Photograph of microSOG.



▲ Figure 2: The IR spectra measured at the μSOG gas outlet versus time. The peak at 1268 nm indicates the spontaneous decay of singlet oxygen into its triplet state.

References

[1] B.A. Wilhite, C. Livermore, Y. Gong, A.H. Epstein, and K.F. Jensen, "Design of a MEMS-based microchemical oxygen-iodine laser (mCOIL) system," *IEEE Journal of Quantum Electronics*, vol. 40, pp. 1041-1055, Aug. 2004.

[2] M.W. Losey, M.A. Schmidt, and K.F. Jensen, "Microfabricated multiphase packed-bed reactors: Characterization of mass transfer and reactions," *Ind. Eng. Chem. Res.*, vol. 40, pp. 2555-2562, June 2001.

[3] L.F. Velásquez-García, T.F. Hill, B.A. Wilhite, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator – Part I: Device fabrication and proof of concept demonstration," submitted to *IEEE Journal of Microelectromechanical Systems*, 2007.

[4] T.F. Hill, L.F. Velásquez-García, B.A. Wilhite, W.T. Rawlins, S. Lee, S.J. Davis, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator- Part II: Experimental exploration of the performance space," submitted to *IEEE Journal of Microelectromechanical Systems*, 2007.

Templated Assembly by Selective Removal

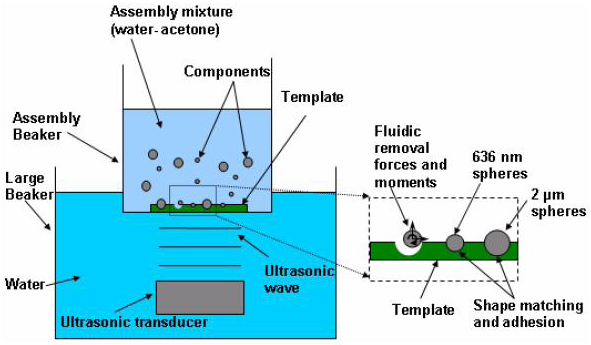
G. Agarwal, F. Eid, C. Livermore

Sponsorship: NSF Career Award, Pappalardo Graduate Fellowship

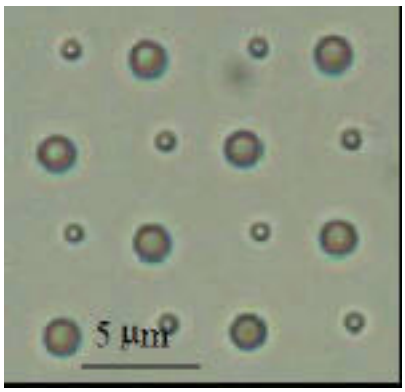
Templated assembly by selective removal (TASR) is an effective technique for site-selective multi-component assembly at the nano- and micro-scales. In this project, the TASR approach has been created, demonstrated and quantitatively modeled; work to expand the technology and exhibit practical applications is now underway. The TASR approach offers great promise for assembling arbitrary (not necessarily periodic) systems of multiple different types of nanoscale components, such as electronics and biological or chemical sensing devices. It also offers a path to a new kind of shape- and size-selective chromatography.

TASR employs a combination of chemistry, surface topography and controllable ultrasonically-induced fluid forces to assemble diverse sets of objects selectively from fluid into designated sites on a 2D surface [1]. Figure 1 shows a schematic layout of the process set-up. The components and the substrate, after undergoing chemical surface modification by a coating of an adhesion promoter, are placed in a fluid environment for the assembly process and megahertz frequency ultrasound is applied to the fluidic bath. Competition between the chemical adhesive effects and fluidic removal forces takes place in which adhesive forces emerge as stronger for components in a well-matched site. The selectivity is based on the degree to which the component to be assembled matches the shape and dimensions of the surface topography at that location. Figure 2 is an optical micrograph showing the successful assembly of 600 nm and 2 mm diameter silica microspheres using TASR. Experiments are now being conducted to extend the technique to a variety of different materials such as biological cells, polymers and nanorods which vary markedly not only in their physical configuration and properties but also in their chemical interaction with the substrate onto which they are to be assembled.

Thus, TASR can be used as a low-cost nanofabrication method with the ability to create complex, arbitrary patterns. We are also investigating the extension of TASR to a shape- and size-sensitive separation mechanism enabling the fabrication of a filtering device with chromatography applications. Present work focuses on the extension of TASR to smaller size scales, a diverse set of component shapes and materials, and improved template fabrication techniques with the goal of demonstrating numerous practical applications enabled by this approach.



▲ Figure 1: Concept schematic of Templated Assembly by Selective Removal (TASR).



▲ Figure 2: Silicon microspheres self assembled on a templated silicon-silicon dioxide substrate.

References

[1] S. Jung and C. Livermore, "Achieving selective assembly with template topography and ultrasonically induced fluid forces," *Nanoletters*, vol. 5, no. 11, pp. 2188-2194, Nov. 2005.

Transplanting Assembly of Individual Carbon Nanotubes to MEMS Devices

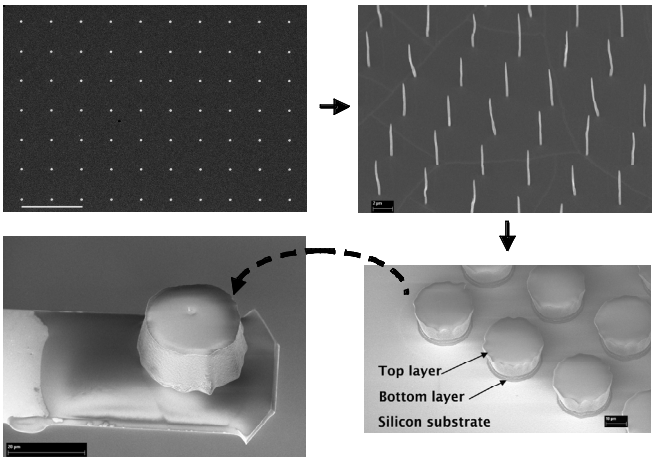
S. Kim, H.W. Lee, S.-G. Kim

Sponsorship: Intelligent Microsystems Center

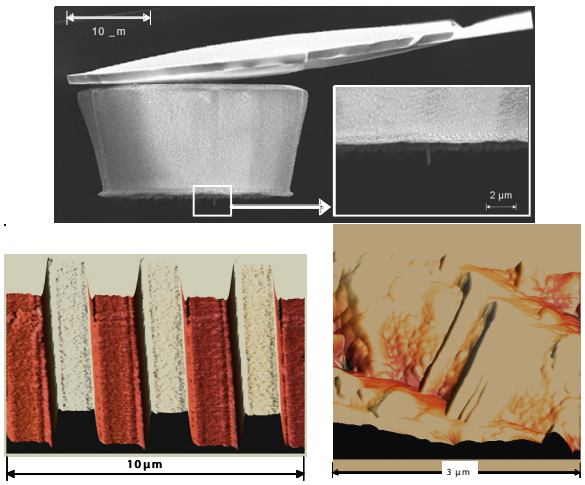
The biggest challenge in integrating nanostructures to MEMS is how to handle and assemble individual nanostructures. We demonstrate a novel assembly method for fabricating CNT-tipped atomic force microscopy (AFM) probes at a high rate and controllable quality via integrating the CNT into MEMS. Its key idea is to grow individual CNTs on a separate substrate and to transplant a well-grown CNT to the target location on a MEMS cantilever (Figure 1). This assembly concept transforms the scale of CNT assembly from nano-scale to micro-scale, which enables even manual assemble of individual CNTs in a deterministic way.

An array of CNTs is grown from the nickel (Ni) nano-dots defined on Si substrates using electron-beam lithography followed by metal deposition and lift-off processes. Each CNT is embedded into a MEMS scale polymer block that serves as a CNT carrier. A double polymeric layer encapsulation process with SU8 (top) and PMGI (bottom) enables an easy release from the substrate and a deterministic length control of the CNT tip. Manual assembly of a polymer block to the end of a tipless AFM cantilever forms a CNT-tipped AFM probe. No laborious weeding, trimming, or welding process was required, and the transplanting assembly technique enables reliable assembly of CNT tips on various AFM cantilevers. The exposed CNT tip normal to the sample surface is 1.5 μm long, which corresponds to the thickness of the bottom layer (Figure 2, top).

The scanning results over a grating with 3-μm pitch and 100-nm-deep vertical trenches shows that our CNT-tipped AFM probe scans the vertical trenches close to their vertical walls. The scanning on a biological sample (filament actins) demonstrates the potential of a CNT-tipped AFM probe for use with soft biological samples (Figure 2, bottom). This technology makes readily feasible massive parallel assembly, which will be pursued in the future.



▲ Figure 1: Transplanting assembly procedure in fabricating CNT-tipped AFM probes. A single CNT strand is grown and transplanted at the end of an AFM cantilever in a deterministic and repeatable manner.



▲ Figure 2: An AFM probe with a single CNT tip normal to the sample surface (top). An AFM scanning result on a standard grid with 3-μm pitch and 100-nm-deep trenches (bottom left) and on filament actins (bottom right).

Reference

[1] T. El-Aguizy, J.H. Jeong, Y.B. Jeon, W.Z. Li, Z.F. Ren, and S.-G. Kim, "Transplanting carbon nanotubes," *Applied Physics Letters*, vol. 85, no. 25, pp. 5995-5597, Dec. 2004.

Surface Micromachining via Digital Patterning

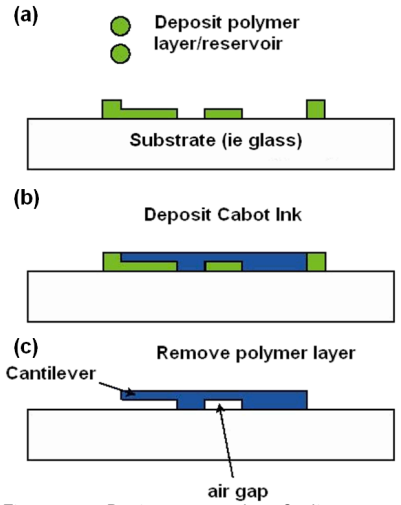
E.W. Lam, J. Chen, V. Leblanc, V. Bulović, M.A. Schmidt
Sponsorship: DARPA, Hewlett-Packard

Conventional microelectromechanical systems (MEMS) fabrication relies heavily on the semiconductor manufacturing paradigm. While this model is well-suited for planar devices such as integrated circuits, it is drastically limited in the design and fabrication of three-dimensional devices such as MEMS. From a commercial viewpoint, this paradigm also poorly fits MEMS because the lower market demand makes it harder to offset the high production costs. Ridding MEMS fabrication of its reliance on such techniques may introduce several advantages, namely a wider base of substrate materials as well as decreased manufacturing costs.

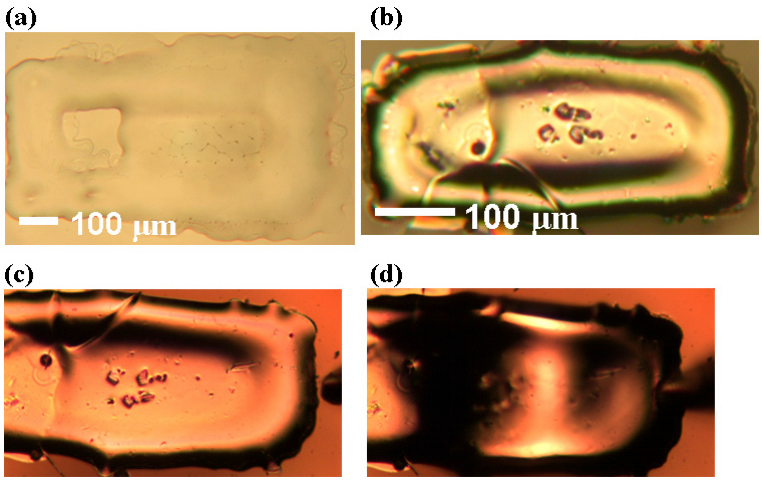
Our project investigates severing MEMS fabrication from the traditional paradigm via digital patterning technologies. We have previously shown how MEMS can be used for the direct patterning of small molecular organics [1]. Using similar concepts, we have shown that surface micromachining can also be achieved.

In 2007-2008, we identified a viable material set for our surface micromachining process' sacrificial and structural layers: poly-methylmethacrylate (PMMA) and silver nanoparticles. To account for surface non-uniformity of the deposited PMMA, we employed solvent vapors to effectively lower the polymer's glass transition temperature and cause reflow at room temperatures [2]. To limit surface wetting and increase material loading of the silver nanoparticles, we deposited a PMMA reservoir to contain the silver nanoparticle solution (Figure 1). Free-standing cantilevers were fabricated (Figure 2), confirming that these techniques can be used for a surface micromachining process.

The next stage will be to fabricate additional MEMS structures and test the silver nanoparticle's mechanical properties. These properties will be used to design and fabricate a demonstration system based on our surface micromachining process. Subsequent stages will consist of creating a library of digital fabrication processes so that entire MEMS devices can be fabricated without the use of semiconductor manufacturing techniques.



▲ Figure 1: Basic approach of direct surface micromachining. (a) PMMA layer (green) is deposited. (b) Metal silver ink (blue) is deposited and sintered. (c) PMMA is removed to release structure.



▲ Figure 2: Proof-of-concept displaying the feasibility of using the process for surface micromachining. (a-c) Pictures corresponding to the cartoons in Figure 1 which outline the fabrication process. (d) Cantilever being mechanically deflected by a probe, showing that the cantilever is free-standing.

References

[1] J. Chen, V. Leblanc, S.-H. Kang, M.A. Baldo, P.J. Benning, V. Bulović, and M.A. Schmidt, "Direct patterning of organics and metals using a micromachined printhead," in *Proc. MRS Spring 2005*, San Francisco, CA, Mar./Apr. 2005, pp. H1.8:1-7

[2] J. Feng, M. Winnik, R.R. Shivers, and B. Clubb, "Polymer blend latex films: morphology and transparency," *Macromolecules*, vol. 28, no. 23, pp. 7671-7682, Nov. 1995.

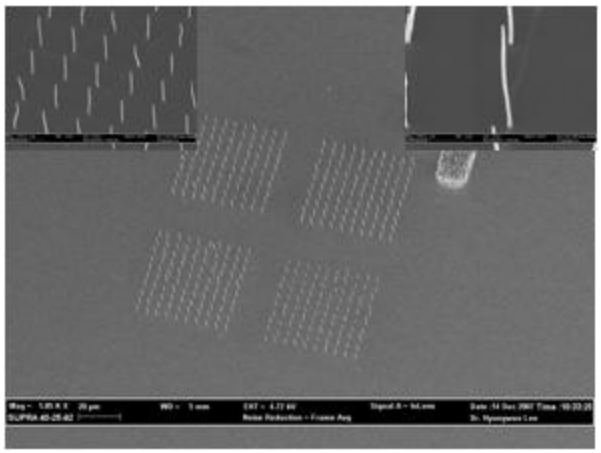
Vertical Growth of Individual CNTs/CNFs as Building Blocks for Functional Nano-devices

H.W. Lee, S. Kim, M. DeVolder, S.-G. Kim
Sponsorship: Intelligent Microsystems Center

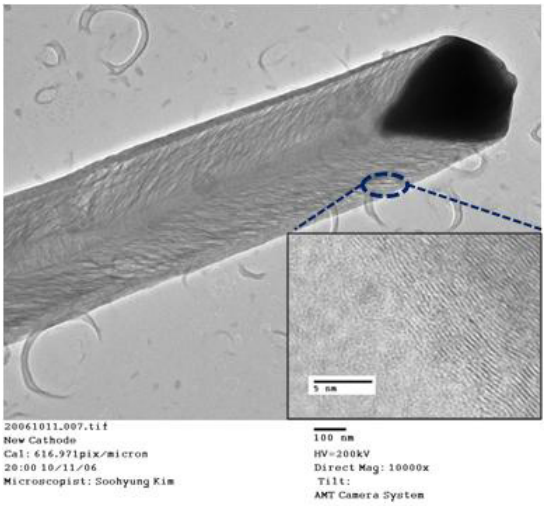
We grow the vertically aligned single-strand CNT/CNF with the plasma-enhanced chemical vapor deposition (PECVD) machine we developed [1]. We found that ammonia (NH_3) gas etching is one of the key process parameters in growing vertically aligned CNTs/CNFs. The NH_3 gas etches Ni catalyst layers to form nanoscale islands while the NH_3 plasma etches deposited amorphous carbon.

A 30-nm-thick Ni layer is deposited on top of a 25-nm-thick titanium layer where CNT/CNF forest can grow vertically. For individual CNT/CNF growth at deterministic locations, 100~200-nm-sized nano dots were made by the E-beam lithography process (Raith, SEBL). The individual CNT/CNF growth requires shorter NH_3 etching time than is needed for a large-area forest growth. We obtained a well-grown array of vertically aligned individual CNTs/CNFs with 5~10 μm in length (Figure 1). High-resolution transmission electron microscopy (HRTEM) images show fishbone structures with multiple layers parallel to the etched surface of a Ni dot and the spacing between the layers is measured as 0.34 nm, which confirms that they are stacked graphene layers (Figure 2).

In this research, we obtained vertically aligned individual CNTs/CNFs on predefined location. We found that NH3 time in gas state is one of important parameters which affect in growing CNTs by PECVD. These individual CNTs/CNFs will be excellent candidates as building blocks for functional nano-devices such as an AFM tip, photovoltaic cell, super capacitor, and so on.



▲ Figure 1: Arrays of vertically aligned 5~10μm-long CNTs/CNFs grown from arrays of the Ni nano dots. The 5-μm spacing between the dots was predefined by electron beam lithography, and Ni dots were formed through heating to 580°C followed by introducing NH_3 gas for 5~10 minutes.



▲ Figure 2: An HRTEM image shows the internal fishbone structures with multiple graphene layers parallel to the outer surface. The spacing between the layers is 0.34 nm, as shown in the inset figure.

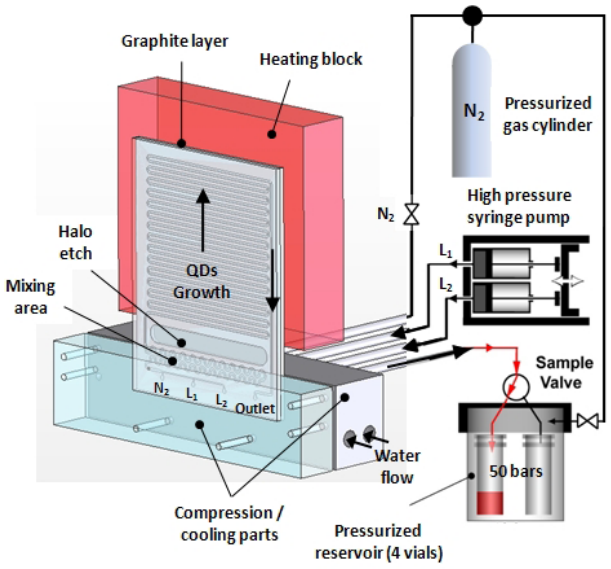
Reference

[1] C. Mueller-Falcke, S.D. Gouda, S. Kim, and S.-G. Kim, "A nanoscanning platform for bio-engineering: In-plane probe for switchable stiffness," *Nanotechnology*, vol. 17, pp. S69-S76, Jan. 2006.

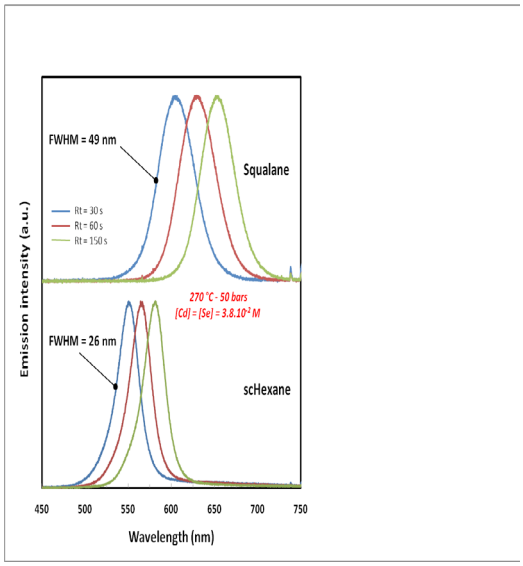
High-pressure, High-temperature, Continuous Micro-flow Synthesis of Narrow Size-distribution Quantum Dots

S. Marre, J.Park, M.G. Bawendi, K.F. Jensen
Sponsorship: ISN, NSF

We have developed a high-pressure, high-temperature continuous-flow Silicon-Pyrex microreactor for the synthesis of CdSe quantum dots (QDs). The microreactor consists of a 400-µm-wide and 250-µm-deep channel with a 0.1- m-long mixing zone maintained at room temperature and a 1-m-long reaction zone heated up to 350°C. The two zones are separated by a thermally isolating halo etch that allowed for a temperature gradient of over 250°C. High-pressure modular compression fluidic connections are realized by compressing the microreactor between two stainless steel parts using silicone O-rings. In this configuration, the set-up allows reaching high pressure (up to 15 MPa) and temperature (up to 350 °C in the heated section). The entire set-up (Figure 1) is first pressurized from the inlet to the outlet using a pressurized nitrogen gas cylinder. Thereafter, the nitrogen valve is closed and the two precursor solutions are delivered independently using a high pressure syringe pump, insuring good control of the flow rate. Applying pressure allows the use of more conventional solvents like hexane, instead of high-boiling-point solvents (squalane) used previously [1]. One can even reach the low-viscosity supercritical fluid phase of hexane (T_c = 234.7 °C and p_c = 3.03 MPa, 20 < η < 70 µPa.s). In contrast to viscous single-phase flow reactors, the supercritical fluid flow approach enables narrow distribution of residence time, factors which have strong influence on the ultimate QD size distribution, as well as higher nucleation rates. Cadmium and selenium precursor solutions are delivered separately in the cooled mixing region and are thereafter allowed to react in the heated region. The use of supercritical hexane has a strong effect on the size distribution of the QDs and consequently the Full Width at Half Maximum (FWHM) of the emission peak (Figure 2). The size distribution for QDs synthesized in hexane, 4 - 5% (FWHM: 25 - 26 nm), is much smaller than for those synthesized in liquid squalane, 9 - 11% (FWHM: 45 - 49 nm).



▲ Figure 1: Experimental set-up including a high pressure high temperature microreactor (Silicon – Pyrex), a compression-cooling aluminum part, a high-pressure syringe pump (Harvard Apparatus model: PHD 2000), 5-way high-pressure valve and a highpressure reservoir containing 4 vials.



▲ Figure 2: The PL spectra at different residence times (Rt) obtained for CdSe QDs synthesized in Squalane and Hexane at 270 °C, 50 bars with [Cd] = [Se] = 3.8.10^{-2}M.

References

[1] B.K.H. Yen, A. Günther, M.A. Schmidt, K.F. Jensen, and M.G. Bawendi, "A microfabricated gas-liquid flow reactor for high-temperature synthesis: The case of CdSe quantums dots," *Angewandte Chemie, International Edition*, vol. 44, no. 34, pp. 5447-5451, Aug. 2005.

[2] B.K.H Yen, N.E. Stott, K.F. Jensen and M.G. Bawendi, "A continuous-flow microcapillary reactor for the preparation of a size series of CdSe nanocrystals," *Advanced Materials*, vol. 15, pp. 1858-1861, 2003.

[3] S. Marre, J. Park, J. Rempel, J. Guan, M.G. Bawendi, and K.F. Jensen, "Supercritical continuous-microflow synthesis of narrow size distribution quantum dots," *Advanced Materials*, to be published.

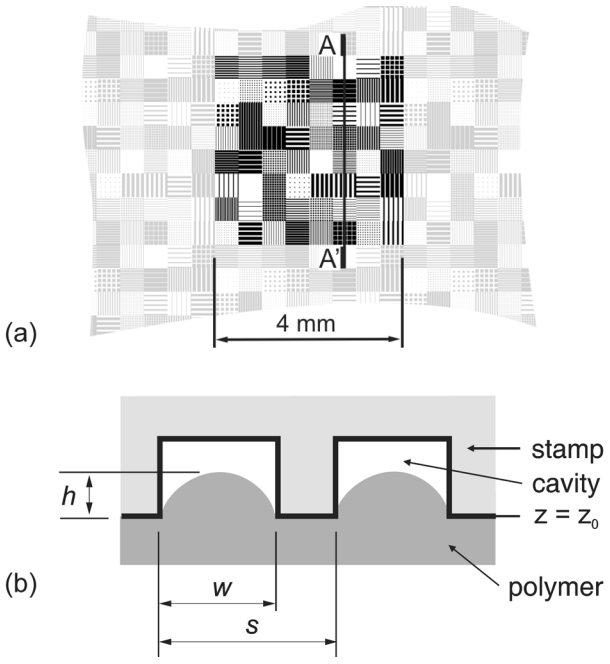
Modeling of Pattern Dependencies in Hot Embossing Processes

H. Taylor, D.S. Boning

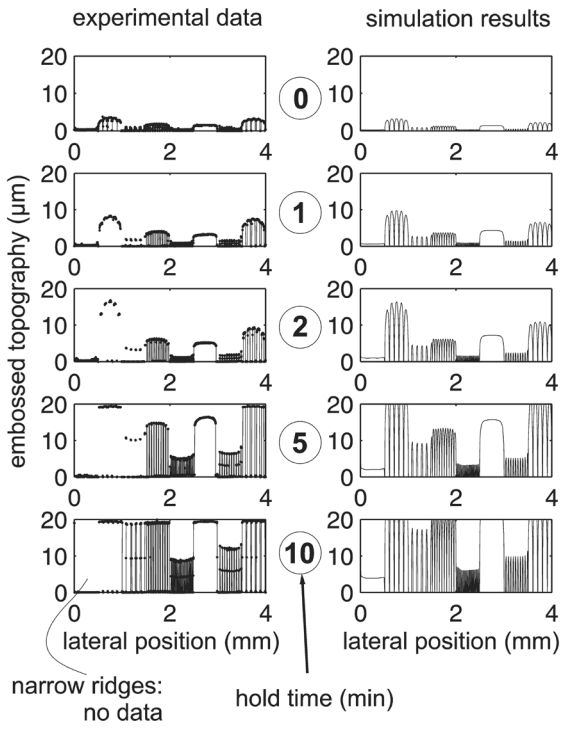
Sponsorship: Singapore-MIT Alliance

The embossing of thermoplastic polymeric layers has proved to be both a lithographic technique with exceptional lateral resolution and a promising approach to high-volume microfabrication. Understanding of the mechanics of hot embossing is well developed thanks to experimentation and meticulous finite-element modeling [1], but it is not practicable to extend such approaches to the feature-rich embossed patterns of real devices. What is needed is a computationally efficient simulation technique that can predict the fidelity of an embossed topography, given an arbitrary stamp layout and a chosen embossing temperature, pressure, and loading duration. Previous attempts to develop efficient embossing simulators have modeled the polymer as a Newtonian fluid [2], an assumption that neglects the elasto-plastic and rubbery behavior that is present between the glass-transition and melting temperatures of popular embossing materials such as polymethylmethacrylate (PMMA).

We present a highly computationally efficient way of simulating the deformation of a polymeric layer when embossed with an arbitrarily patterned stamp [3]. Our approach takes a discretized stamp design and iteratively finds the distribution of stamp–polymer contact pressure that is consistent with the stamp's remaining rigid while the polymer deforms. We model the polymer in its rubbery regime as a perfectly elastic layer with a temperature-sensitive Young's modulus; we find the overall embossed topography by convolving the pressure distribution with the response of the polymeric surface to unit pressure applied in one cell of the discretized region. This topography is assumed to be "frozen" in place by cooling before unloading. The simulation is implemented in Matlab and the convolution uses Fast Fourier Transforms so that we can complete simulations containing ~10^6 elements within a few minutes using a standard desktop computer. We can additionally represent plastic flow of the polymer during embossing by scaling the point-load-response function and performing a time-stepped simulation.



▲ Figure 1: (a) Embossing test pattern. Shaded features correspond to recesses in the silicon stamp. (b) Nomenclature of embossed features.



▲ Figure 2: Experimental and simulated topographies for the section A–A' shown in Figure 1a, after zero to ten minutes' loading duration at 110 °C and 8 MPa. Embossed material: PMMA.

References

[1] H.-C. Scheer, N. Bogdanski, M. Wissen, T. Konishi, and Y. Hirai, "Polymer time constants during low temperature nanoimprint lithography," *Journal of Vacuum Science and Technology B: Microelectronics and Nanometer Structures*, vol. 23, pp. 2963–2966, 2005.

[2] V. Sirotkin, A. Svintsov, H. Schift, and S. Zaitsev, "Coarse-grain method for modeling of stamp and substrate deformation in nanoimprint," *Microelectronic Engineering*, vol. 84, pp. 868–871, 2007.

[3] H. Taylor, D. Boning, B. Chen, and C. Iliescu, "Computationally efficient modeling of pattern dependencies in the micro-embossing of thermoplastic polymers," *Microelectronic Engineering*, DOI:10.1016/j.mee.2008.01.015, 2008.

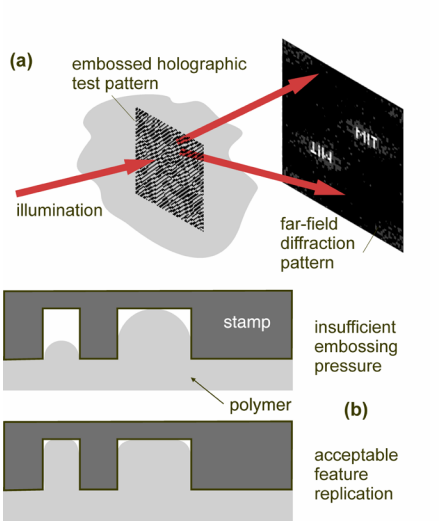
Inexpensive Metrology Approaches for Process Variation in Polymeric MEMS

H. Taylor, Z. Xu, D.S. Boning
Sponsorship: Singapore-MIT Alliance

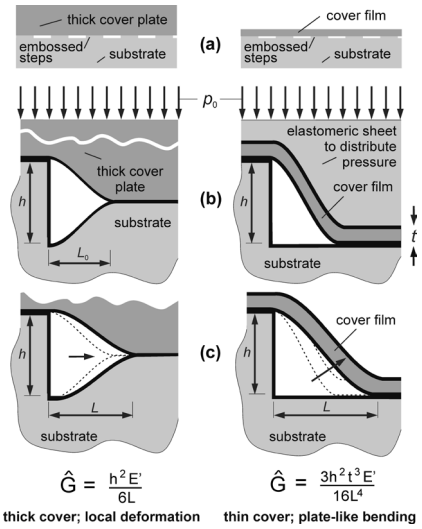
Polymeric materials, often inexpensive, tough and transparent, are attractive for manufacturing micro- and nano-fluidic devices. Here we describe three projects to develop tools for monitoring polymeric microstructure production. The first uses diffraction to identify dimensional defects in embossed thermoplastic components. A collimated laser beam is shone through a component whose microembossed structure includes a specially designed holographic test pattern that spatially modulates the phase of the transmitted light (Figure 1). A far-field diffraction pattern is formed, yielding information about the embossed topography without requiring precise alignment of, or contact with, the manufactured part [1].

The second project uses moiré interference to study distortions of hot-embossed polymeric substrates. The only apparatus required is a desktop image scanner and a precisely printed reference grid. The reference grid and a substrate embossed with a grid of the same target pitch are placed on the scanner and rotated by hand until moiré fringes are seen. At least two scans are made, each with a different relative reference–part rotation. These rotations are extracted from the images and, together with the moiré fringes' orientations and spacings, reveal the part's distortions.

Thirdly, we are designing a way of testing the toughness of bonds between polymeric layers. The UV/ozone- and plasma-activated bonding of polymeric layers is appealing because, unlike with thermal fusion bonding, microstructures at the interface remain intact [2]. However, the lack of a simple bond test method has impeded the development of these processes. Our approach is to pattern one of the layers with one or more steps to ~1 μm deep. The bonding process is then performed and, immediately after bonding, the layers peel apart locally around each step (Figure 2). The lengths of the resulting cracks are measured with optical microscopy, revealing the bond's toughness. Interfacial cracks are usually shorter than a millimeter, meaning that these test structures can be interspersed with functional devices.



▲ Figure 1: Use of holographic test patterns for contact-free determination of dimensional defects in embossed parts. (a) Overview of scheme: a dedicated test pattern embossed alongside the functional device perturbs the phase of transmitted light, imparting information about the topography. (b) Cross-sections of typical embossed topographies that would need to be distinguished: inadequate embossing pressure would cause different elements of the hologram to be filled to different heights, thereby perturbing phase differently.



▲ Figure 2: Two configurations of the bonding test method. On the left, both layers are substantially thicker than the length L of the crack, and material deforms locally around the step. On the right, one layer is a film that bends over the step as a plate. (a) Several steps in cross-section. (b) During bonding, pressure p_0 is applied, causing the layers to compress and a bond to form where the layers make contact. In (c), the bonding pressure is released and the cracks extend to an equilibrium length yielding an estimate, $\hat{G}$, of the bond toughness. E' is the plate modulus.

References

[1] H.K. Taylor and D.S. Boning, "Diffraction-based approaches to the *in-situ* measurement of dimensional variations in components produced by thermoplastic micro- and nano-embossing," in *Proc. International Symposium on Nanomanufacturing*, Singapore, Jan. 2008.

[2] A. Bhattacharyya and C.M. Clapperich, "Mechanical and chemical analysis of plasma and ultraviolet–ozone surface treatments for thermal bonding of polymeric microfluidic devices," *Lab on a Chip*, vol. 7, pp. 876–882, 2007.

Relationship between Pad Properties and CMP Planarization

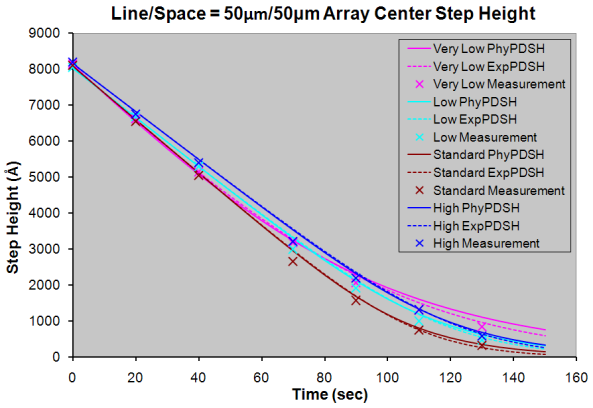
W. Fan, D.S. Boning

Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, JSR Micro

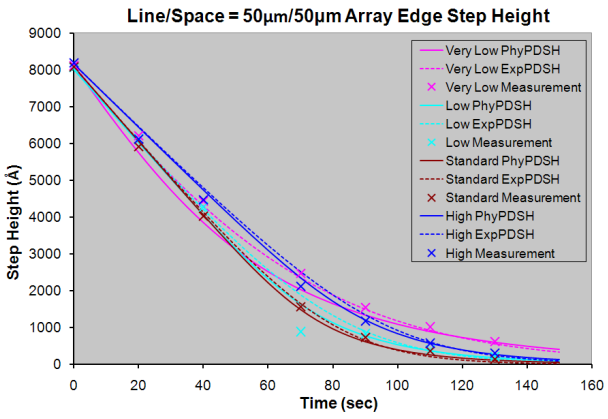
Chemical mechanical polishing (CMP) is a key technology in semiconductor and micromachining processes. In previous work, our group proposed semi-empirical and physically-based die-level CMP models to understand and optimize the dielectric planarization process [1]. In this work, we seek to understand how planarization model parameters relate to specific pad properties. In particular, we are interested in how pad bulk stiffness and pad surface properties affect both within-chip planarization and step-height reduction or planarization efficiency.

Our recent work has investigated pad hardness effects on polishing performance by fitting experimental data from the polishing of patterned wafers and by extracting model parameters related to effective pad Young's modulus and height distribution of surface asperities. We polished wafers with the same pattern-density arrays and the same initial oxide thickness using four pads with different hardness (standard, high, low and very low), and measured the oxide thickness and step-height evolution during the process.

From the data fitting and model prediction, we conclude that the standard hardness pad achieves faster planarization and has better linear step-height removal for a longer time than the other pads, as shown in Figure 1. All pads have a pattern-density dependency effect; however, the stiffer pads show less oxide thickness variation across the chip. Figure 2 shows the evolution of step height at the test point on a 50% pattern density array boundary next to a 10% layout pattern density area. This edge planarizes faster than the array center point because of the lower effective pattern density. We also see that the very low hardness pad has substantially different step-height removal behavior than the other pads, indicating that the pad surface asperity height distribution may be substantially different for this pad. Current work is seeking to make direct pad physical measurements in order to verify the relationship between both pad surface (asperities) and bulk effective modulus and the resulting planarization performance.



▲ Figure 1: Step height evolution for different pad hardness at the center test point of a 50% pattern density array in the middle region of the wafer. Data points show optical measurements. The line shows physically-based pattern-density/step-height (PDSH) model prediction. Dashed line shows exponential PDSH model prediction.



▲ Figure 2: Step-height evolution for different pad hardness at the edge test point of 50% pattern density array in the middle region of the wafer. Data points show optical measurements. Line shows physically-based PDSH model prediction. Dashed line shows exponential PDSH model prediction.

Reference

[1] X. Xie, "Physical understanding and modeling of chemical mechanical planarization in dielectric materials," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.

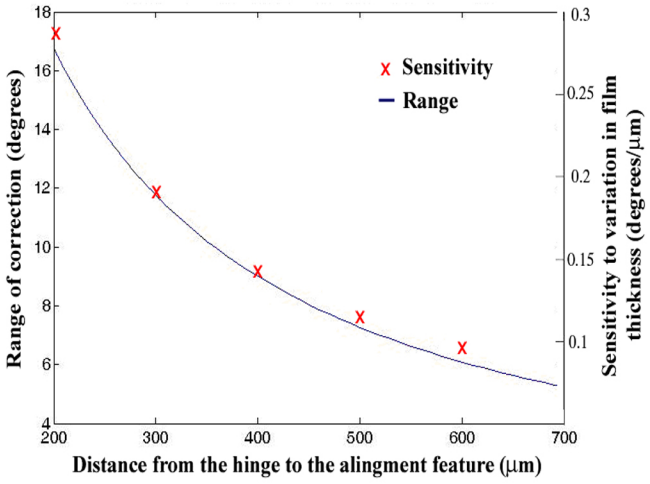
Cascaded Mechanical Alignment for 3D MEMS Assembly

N.S. Shaar, G. Barbastathis, C. Livermore
Sponsorship: ISN

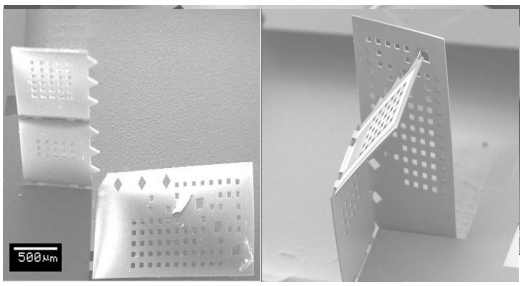
The fabrication of MEMS devices relies, for the most part, on tools and processes developed originally for the fabrication of electronic chips in the IC industry. However, in contrast to electrical circuits, functional micro-electro-mechanical systems need features that are three-dimensional (3D) in structure. To capitalize on the well-developed techniques and equipment of 2D-patterning technologies, we have developed a method to create 3D MEMS devices by folding, aligning and latching 2D micro-fabricated films.

The folding process is relatively well developed. Various methods for bending films out-of-plane have been demonstrated, including thermal contraction [1], stress gradients [2], surface tension [3], and external magnetic forces [4]. However, aligning the folded segments and latching them, while maintaining the structural integrity of the MEMS devices, remain challenges.

We have designed, fabricated, and tested a mechanical alignment mechanism that enables the precise angular positioning of 2D membranes to form 3D structures. The alignment system is based on a cascaded set of triangular protrusions on the *target segment* and rhombic holes on its corresponding *aligning segment*. Upon folding, the protrusion-hole pairs start to engage sequentially, starting with the pair closest to the fold. The alignment progresses in a zipper-like manner, allowing a large range of correction as well as high alignment accuracy (Figure 2). We have demonstrated our alignment mechanism by assembling a corner-cube retro reflector. The alignment system's accuracy was within 16 mrad and the measured range of correction was 0.38 rad [5]. We have also demonstrated the ability to simultaneously align multiple segments at different angles (Figure 2).



▲ Figure 1: Plot of the predicted range of correction (solid line) and the sensitivity of the alignment to variations in the film thickness ('x' data points) vs. distance from the hinge to the alignment feature.



▲ Figure 2: Corner-cube with a base segment fixed to the substrate and two folded segments aligned at 90^0 (top). A sequence of two folded *target segments* aligned by one *aligning segment* to 90° and 45° relative to the substrate surface (bottom).

References

[1] T. Ebefors, E. Kälvesten, and G. Stemme, "New small radius joints based on thermal shrinkage of polyimide in V-grooves for robust Self-assembly 3D microstructures," *Journal of Micromechanical Microengineering*, vol. 8, pp. 188–194, 1988.

[2] W.J. Arora, A.J. Nichol, H.I. Smith, and G. Barbastathis. "Membrane folding to achieve three-dimensional nanostructures: Nanopatterned silicon nitride folded with stressed chromium hinges," *Applied Physics Letters*, vol. 88, no. 5, pp. 053108:1-3, Jan. 2006.

[3] Y.K. Hong, R.R.A. Syms, K.S.J. Pister, and L.X. Zhou. "Design, fabrication and test of self-assembled optical corner cube reflectors," *Journal of Micromechanical Microengineering*, vol. 15, pp. 663-672, 2005.

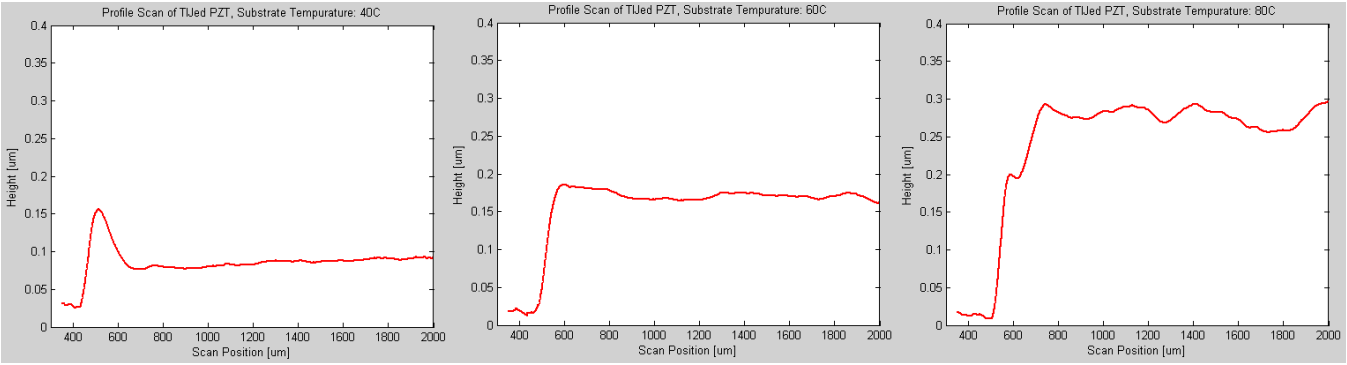
[4] H.J. In, W. Arora, T. Buchner, S.M. Jurga, H.I. Smith, and G. Barbasathis, "The nanostructured Origami™ 3D fabrication and assembly process for nanomanufacturing," in *Proc. Fourth IEEE Conference on Nanotechnology*, Munich, Germany, Aug. 2004, pp. 358-360.

[5] N.S. Shaar, G. Barbastathis, and C. Livermore, "Cascaded mechanical alignment for assembling 3D MEMS," in *Proc. 21st IEEE International Conference on Microelectomechanical Systems*, Tucson, AZ, Jan. 2008, pp. 1064-1068.

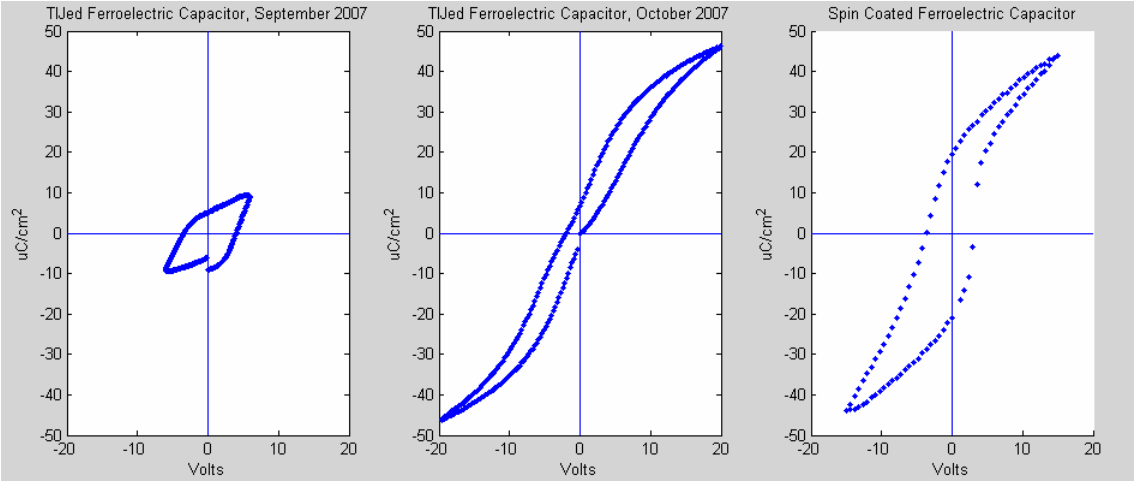
Direct Printing of PZT Thin Films for MEMS

S. Bathurst, H.W. Lee, S.-G. Kim
Sponsorship: DARPA Grant HR0011-06-1-0045, Hewlett-Packard

In 2007-2008, we reported a new method for depositing piezoelectric thin films via thermal ink jet (TIJ) printing of a modified PZT sol-gel [1]. Direct printing of lead zirconate titanate (PZT) thin films eliminates the need for photolithographic patterning and etching, allows for controlled deposition over non-planar topographies, and enables the deposition of films with varied thickness. We developed conditions of deposition and crystallization for high-quality PZT thin films via thermal inkjet printing, including solution chemistry, printing conditions, and thermal processing parameters. The inks developed for this work were based on a commercially available PZT sol gel. Dilution of the sol is required to control the evaporation rate and characteristic dimensionless numbers of the ink, and our work included a jetability study of various solution chemistries. This study resulted in an ink that can be jetted reliably and is made up of 50% isopropanol, 30% 2-methoxyethanol, %15 A6 sol-gel, and 5% ethylhexanoic acid. This work also investigated factors that control the droplet size and the contact angle of the PZT ink deposited on a Pt substrate. The edge roughness of deposited lines was controlled to +/- 10μm. We further investigated the effect of droplet size, spacing, ink boiling point and substrate temperature on the deposited film uniformity. Figure 1 demonstrates the effect of substrate temperature on the film topography. Films between 100-500nm in thickness with a variation of less than 40nm were produced (Figure 1b). A capacitor test device was fabricated with approximately 400 nm of printed PZT between two platinum electrodes. The bottom electrode was 200 nm Pt/20nm Ti/200 nm SiO_2/Si. The capacitor area was $6.25 \cdot 10^{-4}$ cm². Finally, it was determined that the modified ink requires a prolonged drying step to remove added solvents, and pre-dryed films showed a drastically improved polarization performance (Figure 2).



▲ Figure 1: Profilometry of thermal ink jetted PZT, deposited at different substrate temperatures. Ink composition: 6% EHA, 15% PZT sol-gel, 50% IPA, and 29% ME.



▲ Figure 2: Polarization vs. voltage hysteresis curve for a thermal ink jetted PZT thin film a) after standard pyrolysis and b) after extended pyrolysis as well as c) for a spincoated film after standard pyrolysis.

Reference

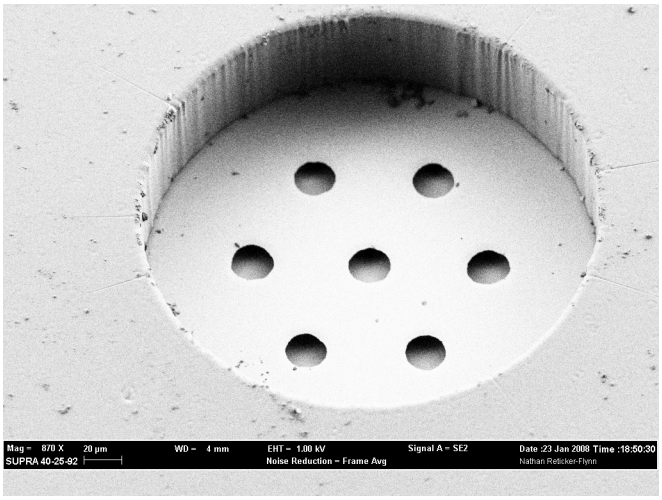
[1] S. Bathurst, H.W. Lee, and S.-G. Kim, "Direct printing of lead zirconate titanate thin films," *IEEE MEMS 2008*, Tucson, AZ, 2008.

Printable Microfluidic Valves Composed of Thermosensitive Hydrogels

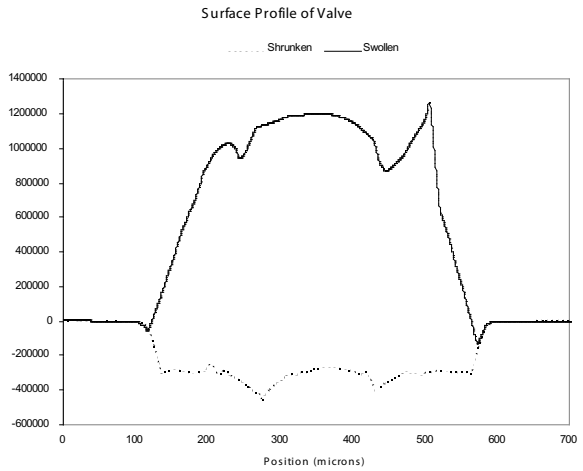
N.E. Reticker-Flynn, H.W. Lee, S.-G. Kim
Sponsorship: Hewlett-Packard, DARPA

A method for fabricating compact microfluidic valves using thermal inkjet printing is presented. Poly(N-isopropylacrylamide) (poly(NIPAAm)) is a temperature-sensitive hydrogel that shrinks when heated above a Lower Critical Solution Temperature (LCST) (~32°C). With the swelling behavior of poly(NIPAAm) as a flow control mechanism, a compact microfluidic valve has been designed and fabricated. The proposed valve provides a series of benefits over conventional microfluidic valves such as the "Quake" valves [1], in that they allow for the use of single-layer PDMS microchannels. Additionally, the need for a bulky external pump is eliminated by localized electromagnetic heating if the hydrogel valve.

The design of the proposed valve is composed of an SU-8 microwell into which the prepolymer NIPAAm solution is printed (Figure 1). The well contains micro-anchors to ensure that the hydrogel always shrinks downward in order to prevent any unintended blocking of the flow channel. After the prepolymer solution with photoinitiators has been printed into the wells, it is polymerized using ultraviolet light. Finally, the PDMS channel is placed above the well. This channel contains discontinuities at the location of the valves, which block the flow when the hydrogel is in a swollen state. When the poly(NIPAAm) valves are heated above the LCST, the hydrogel plug shrinks and allows flow (Figure 2). The amount by which the gel plug shrinks depends on monomer concentration and UV exposure energy. By fabricating the wells on a separate substrate from the channels, users can use the same valve substrate with a variety of different fluidic circuit designs. Device geometry was chosen using CFD to minimize pressure drops across the valve.



▲ Figure 1: An SEM of a microwell prior to printing NIPAAm prepolymer. The bottom of the well is composed of a metal layer with anchor holes. The underlying pyrex has been etched isotropically with HF to generate significant undercut.



▲ Figure 2: Surface profile of the swollen and shrunken poly(NIPAAm) gel after printing into a 500-µm-diameter well and prior to bonding of PDMS. The heated gel provides an average height difference between the gel surface and the top of the microwell of approximately 35 µm.

Reference

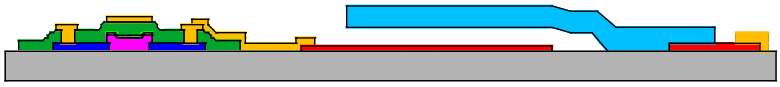
[1] T. Thorsen, S. Maerkl and S. Quake, "Microfluidic large-scale integration," *Science*, vol. 298, pp. 580-584, Oct. 2002.

Integration of Printed Devices and MEMS

H. Li, M.A. Schmidt

Sponsorship: DARPA, Hewlett-Packard

As part of an overall effort on Non-Lithographic Technologies for MEMS and NEMS, we are developing processes for the integration of printed MEMS and devices. The goal of this project is to demonstrate the power of a printed technology for microsystems. We have already developed a surface micromachined cantilever technology that utilizes silver as a structural material and a novel organic spacer. Further, we have developed a family of both inorganic and organic devices that can ultimately be printed. As an initial demonstration, we are building a MEMS capacitive accelerometer that integrates the silver surface micromachined proof mass and spring with a capacitive sense circuit fabricated using organic FETs.



▲ Figure 1: Schematic illustration of the integration of a printed MEMS cantilever with a printed electronic device.

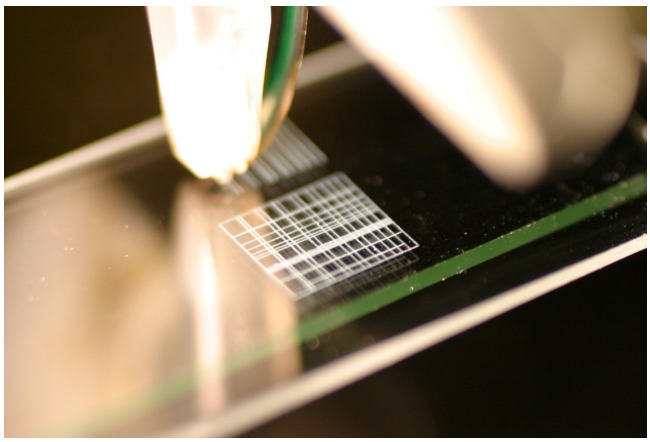
The MIT-OSU-HP Focus Center on Non-lithographic Technologies for MEMS and NEMS

M.A. Schmidt (in coll. with S.-G. Kim, C.G. Sodini, V. Bulović, MIT; D. Keszler, J. Wager, OSU; P. Benning, M. Chaparala, J. Stasiak, Hewlett-Packard)

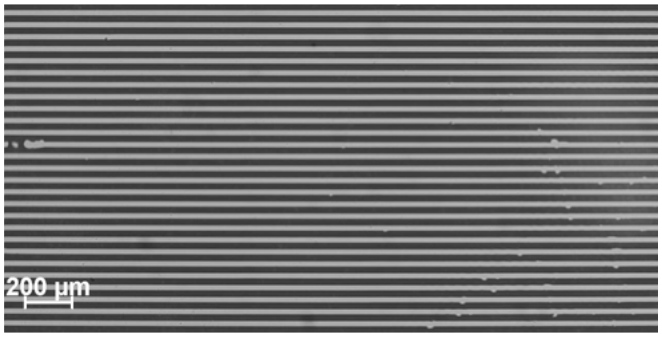
Sponsorship: DARPA, Hewlett-Packard

This center is part of a set of centers on MEMS/NEMS fundamentals supported by DARPA. The MIT-OSU-HP Focus Center aims to develop new methods for fabrication of MEMS and NEMS that do not use conventional lithographic techniques. The Center leverages the leading expertise of MIT and OSU in MEMS and printed devices, with the printing expertise of HP. The Focus Center is organized into four primary areas: tools, materials and devices, circuits, and demonstration systems.

In the area of tools, we are leveraging the existing thermal inkjet (TIJ) technology of HP and augmenting it with specific additional features, which expand the palette of available materials for printing. We are developing materials and devices over a broad spectrum from active materials and photonic and electronic materials to mechanical materials. In the circuits area, we are studying the behavior of the devices that can be realized in this technology with the goal of developing novel circuit architectures. Lastly, we intend to build several "demonstration" systems that effectively communicate the power of the new technologies that will emerge from this center. In the past year, the center has succeeded in demonstrating a number of the key "building blocks" for a fully printed system. Specifically, we have created printed transistors, printed optical elements (light emitters and photodetectors), printed active materials (piezoelectrics), and a printed MEMS structure (micro-cantilever). Looking forward, we will begin efforts to integrate some of these building blocks.



▲ Figure 1: Printing the structural layer of a MEMS cantilever. The printing is performed using a modified thermal inkjet system.



▲ Figure 2: In addition to printing by inkjet, we also explore micro-contact printing. The image shown is an illustration of the micro-contact printing of metal lines from the Bulović group at MIT.

Inkjet-printed Quantum Dot and Polymer Composites for AC-driven Electroluminescent Devices

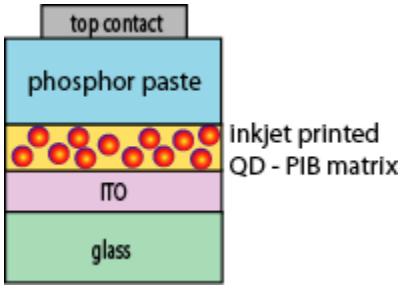
V. Wood, J. Chen, M.J. Panzer, M.S. Bradley, J.E. Halpert, M.G. Bawendi, V. Bulović

Sponsorship: ISN, PECASE, NDSEG

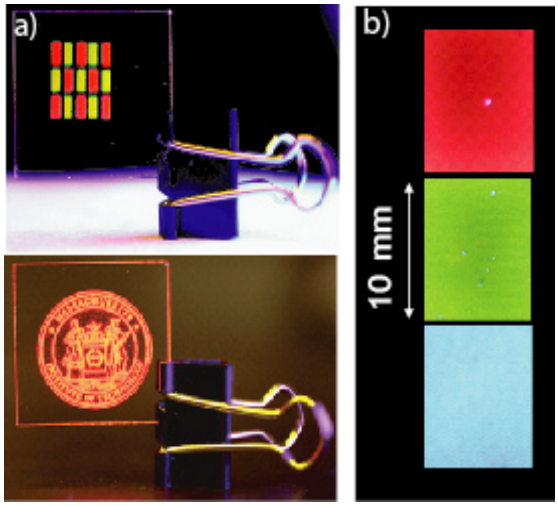
We introduce a technique for the reliable deposition of intricate, multicolored patterns using a quantum dot (QD) and polymer composite and demonstrate its application for robust AC-driven displays with high brightness and saturated colors. The AC electroluminescent (AC EL) devices are a well-established technology [1]. Their relatively simple fabrication and long operating lifetimes make them desirable for large-area displays; however, a major challenge with AC EL remains finding efficient and stable red phosphors for multicolored displays. Colloidally synthesized QDs are robust, solution-processable lumophores offering tunable and narrowband photoluminescence across the visible spectrum [2]. By integrating QDs into an AC EL device, we demonstrate patterning of saturated red, green, and blue pixels that operate at video brightness.

The concept behind the device operation is optical downconversion: red and green QDs absorb blue electroluminescence from phosphor grains and then emit at longer wavelengths. The device, pictured schematically in Figure 1, is fabricated with a layer-by-layer approach that is compatible with flexible substrates. A QD and polyisobutylene (PIB) solution is printed on conductive indium tin oxide (ITO) using a Hewlett Packard Thermal Inkjet Pico-fluidic dispensing system (TIPs). Figure 2a shows examples of the intricate and multicolored patterns possible. The electroluminescent phosphor paste (ZnS:Cu powder in a transparent binder from Osram-Sylvania) is deposited uniformly over the sample using a disposable mask and doctor-blading to define the device area. Top contacts are made with conductive tape from 3M. This basic device structure is assembled and tested entirely under atmospheric conditions.

When an AC voltage waveform is applied across the device, we measure spectrally pure QD emission in the red and green and ~100 Cd/m^2 brightness. Photographs of the red, green, and blue pixels of a working, AC-driven device appear in Figure 2b. The Commission International d'Eclairage (CIE) coordinates of the pixels device define a color triangle that is comparable to the International Telecommunication Union HDTV standard.



▲ Figure 1: Schematic showing basic device structure.



▲ Figure 2: Photographs of a) photoluminescence of QD-PIB composites inkjet-printed on 1 in. x 1 in. indium tin oxide coated glass slides and b) emission from blue, green, and red pixels of completed devices driven at 70 V_{rms} and 50 kHz.

References

[1] Y.A. Ono, *Electroluminescent Displays.* Singapore: World Scientific, 2000.

[2] C.B. Murray, D.J. Norris, and M.G. Bawendi, "Synthesis and characterization of nearly monodispersed CdE (E= S, Se, Te) semiconductor nanocrystallites," *Journal of the American Chemical Society*, vol. 115, pp. 8706-8715, 1993.

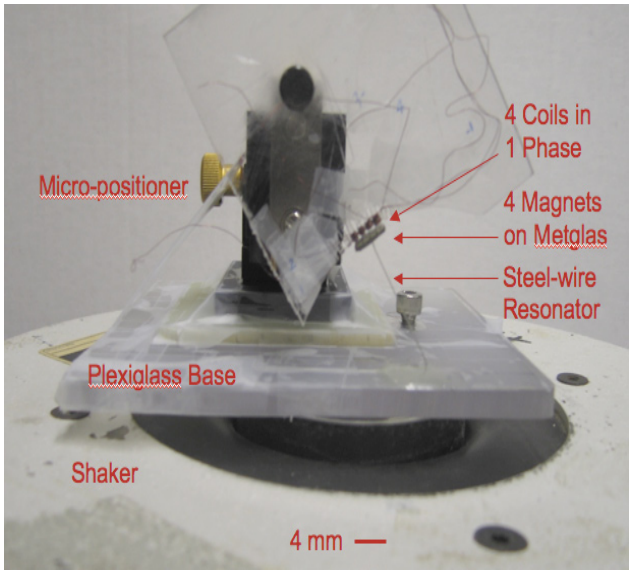
Milli-watt Energy-harvesting from Low-frequency Vibrations

S.C. Chang, A.D. Dominguez-Garcia, D. Otten, J.H. Lang
Sponsorship: DARPA

This project is part of the Hybrid Insect Microelectromechanical System MEMS (HI-MEMS) program sponsored by the Defense Advanced Research Projects Agency (DARPA). The main objective of this program is to establish the interface between adult neural systems and appropriate computational and MEMS systems. Here, insects are the first test bed, and they will be directed to fly to specific locations in real time via remote control. In order to support the flight-control systems, a local energy-harvesting power system is required on the moth. The energy-harvesting system has two ports: the mechanical port and the electrical port. Mechanical power is input from moth motion at the mechanical port, and electrical power is output for general consumption at the electrical port. Internal to the harvester between the two ports are an electromechanical energy converter (generator) and the power electronics. In the past 12 months, a 0.1-mW bench-top electromechanical energy converter, which extracts power from low-frequency vibration, was designed and fabricated. Figure 1 shows the harvester.

The electromechanical energy converter has two major components: a resonator with moving magnets and a coil. The magnets serve as a proof mass, and as the resonator vibrates, the magnets sweep past coils through which power will be harvested. In collaboration with the Daniel Group at the University of Washington, we determined the resonating frequency to be 25 Hz by tracking the three-dimensional inertial motion of a moth and taking the Fourier transform of the moth's motion. Figure 2 shows a snapshot of the moth carrying a resonator during flight. The coils are wound on a plexiglass form, such as that shown in Figure 1; future flight-qualified windings will be made with flexible printed-circuit technology. The electromechanical energy converter was tested on a shaker table, which simulates the vibration of a moth, and 0.1 mW of time average power was extracted from the output of the series coil connection.

We are now optimizing a more compact advanced energy-harvester that has flexible printed-circuit windings, neodymium iron boron magnets. Simulations indicate that 1-mW energyharvesting is achievable at a cost of 0.27g. Harvester components including the magnets and windings have been designed and are under fabrication. Currently, we are beginning the analysis and design of the power electronic circuit. The first pass will focus on switched-capacitor power electronics, and the next milestone will be testing the advanced energy-harvester on a shaker table and developing power electronics compatible with radio micro- fabrication.



▲ Figure 1: First generation energy-harvester system consisting of 4 magnets and 4 coils in phase on a shaker table capable of generating 0.1mW of power.

▲ Figure 2: A moth carrying a resonator during flight. The fine-tuned resonator will resonate with the moth's vibration frequency of 25 Hz, creating maximum swing amplitude to generate power. (Courtesy of Daniel Group at the University of Washington.)

5

Photonics

Table of Contents

Deep Submicron CMOS Photonics

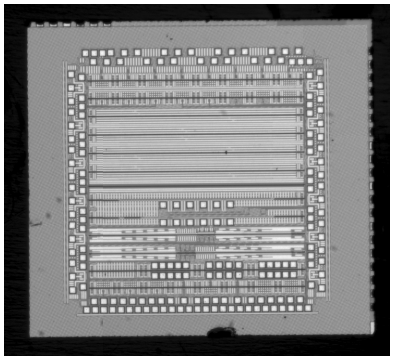
J.S. Orcutt, A. Khilo, M.A. Popović, C.W. Holzwarth, B. Moss, H. Li, M.S. Dahlem, F.X. Kärtner, E.P. Ippen, J.L. Hoyt, V. Stojanović, R.J. Ram

Sponsorship: DARPA

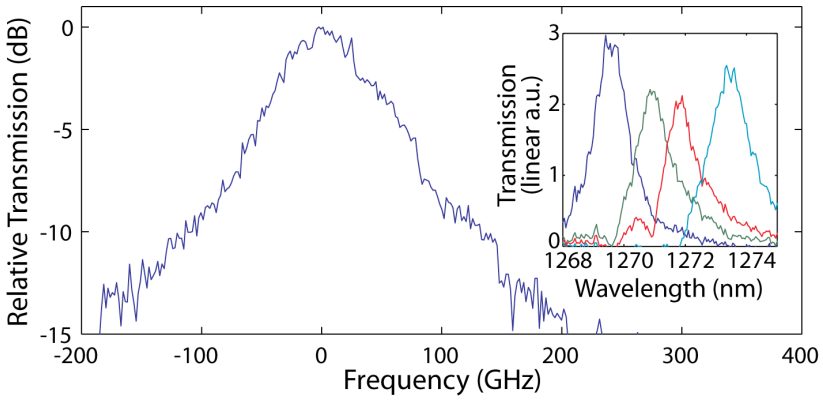
In the past decade, silicon has moved from a work bench for low-index contrast photonics to a strong-confinement (SC) photonics workhorse. The SC silicon-core waveguides have been shown to maintain low-loss while enabling micron-scale photonic structures [1] and suitability for next-generation telecom components [2]. As performance begins to rival traditional III-V telecom-grade photonics, the possibility of inter- and intrachip photonic interconnects integrated with traditional CMOS electronics has opened photonics to the VLSI community [3]. Photonic interconnects have the potential to break increasingly severe energy efficiency and bandwidth density bottlenecks of electrical interconnect in scaled CMOS microprocessors. Photonic components required for integration include SC waveguides, resonant add-drop filters for wavelength-division multiplexing (WDM), energy-efficient modulators, and integrated photodiodes. In this work, we present a general strategy for photonic integration into bulk CMOS and the first photonic test chip using this approach, which was produced in a commercial 65-nm process and is shown in Figure 1(a).

Traditional silicon-on-insulator (SOI) waveguides that use the active electronic silicon layer of SOI wafers as the waveguide core require a thick buried-oxide layer (2 to 3 μm) to enable low optical substrate leakage loss. The photonic chip presented here is produced within an existing commercial bulk CMOS flow, adding zero in-house production changes, ensuring optimal performance of integrated electronic circuits and minimizing production cost. Bulk CMOS processes, unlike SOI CMOS, have no single-crystal silicon layer patternable with a standard mask set. Multiple higher index nitride layers that could potentially be used as waveguide cores are present in the backend of the CMOS processes, but none are patternable. However, a patternable polysilicon layer in the front end of the process, referred to as a shallow trench isolation (STI), is used to form the transistor gates over a thin oxide as well as local interconnects and resistors over a thicker oxide. Traditionally, the end of line polysilicon is heavily doped and silicided to reduce electrical resistance, resulting in a material with high optical loss. However, this Si layer must first be deposited undoped since opposite polarity implant steps are used to form the n-channel and p-channel transistor gates. Additionally, the need to create accurate resistors in a mixed-signal process requires a way to block the standard silicidation step of the polysilicon. These two facts allow for the processing masks to be designed to create an undoped, unsilicided polysilicon layer for SC waveguide fabrication.

Using this platform, we designed the first bulk photonic chip in a commercial process on a 4-mm² die. Primary goals are for the chip to demonstrate integrability, characterize waveguide loss and evaluate the performance of the photonic device. Additionally, the chip includes high-speed modulator drivers with data input signal processing electronics that are designed to demonstrate integration with photonics without degrading the performance of the electronic device.



▲ Figure 1: Bulk 65-nm photonic test chip die photo. The 2x2 mm² die contains 116 devices and over 21 cm of waveguide.



▲ Figure 2: Single channel microring-resonator drop port results. Inset shows a 4-channel filter bank with 240-GHz channel spacing (preliminary measurements taken by IR camera show some distortion due to pixel saturation and limited bit depth).

References

[1] F. Xia et al., "Ultracompact optical buffers of a silicon chip," *Nature Photonics*, vol. 1, no. 1, pp. 65-71, Jan. 2007.

[2] M.A. Popović, T. Barwicz, et al., "Strong-confinement microring resonator photonic circuits," in *Proc. 20th Annual Meetingof IEEE Lasers and Electro-Optics Society*, Lake Buena Vista, Florida, Oct. 2007, paper TuCC3.

[3] C. Gunn, "Fully integrated VLSI CMOS and photonics CMOS photonics," in *Digest of Technical Papers, IEEE Symposium on VLSI Technology*, 2007, pp. 6-9.

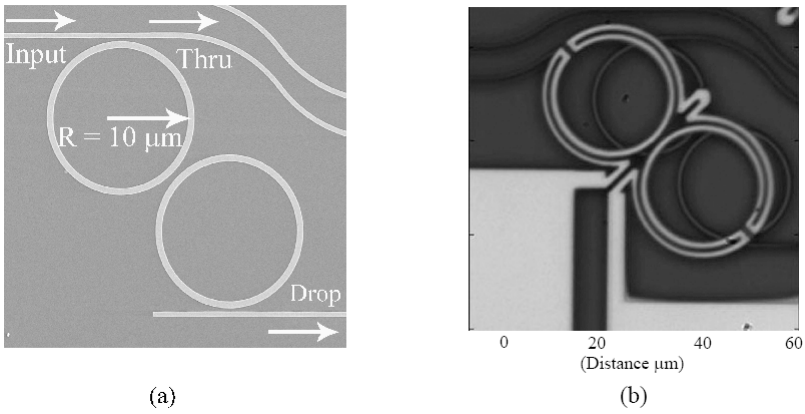
Active Control of Photonic Microring Filters

R. Amatya, R.J. Ram
Sponsorship: DARPA

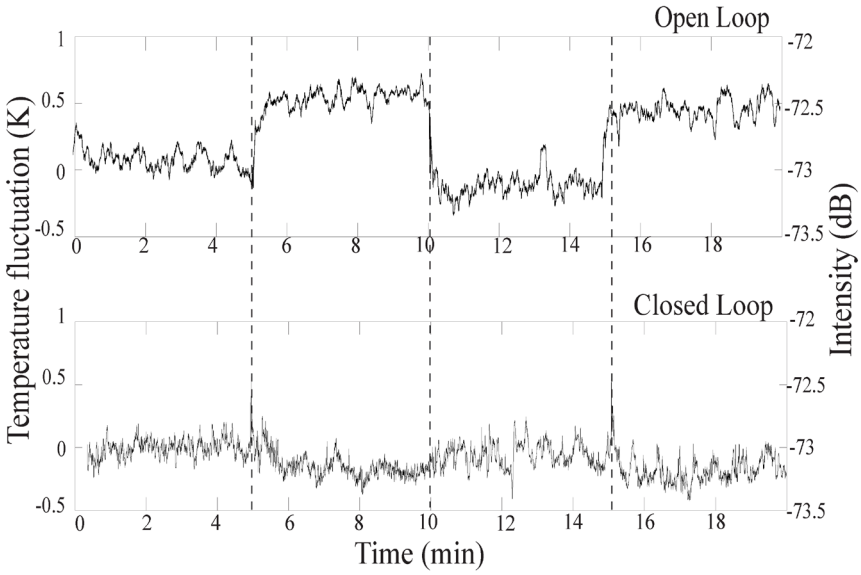
Microring resonators can be used as pass-band filters for wavelength-division demultiplexing in electronic-photonic integrated circuits for applications such as analog-to-digital converters. For high-quality signal transmission, the resonant frequency of the filter must be held at a certain value to allow minimum timing errors in the sampling of the signal. Thermal tuning is used to compensate for any fabrication errors or environmental temperature fluctuations that might lead to a shift in the resonant frequency. With an optimized heater design (Figure 1), we demonstrate efficient thermal tuning with low power (80μW/GHz) for these ring resonators. For the application of interest, wavelength stability as well as power efficiency for tuning are more important metrics than the total tuning range. A distinct disadvantage of working with silicon is the stringent need for temperature stability. Due to the larger thermo-optic coefficient of silicon, the resonant wavelength is very susceptible to temperature change.

An on-chip heater is run by a temperature controller feedback circuit, which helps in maintaining a steady temperature against environmental temperature perturbations. Due to size constraints for microring resonators (radius ~ 10 μm), a single resistive element is used both as a heater and as a temperature sensor. The feedback circuit utilizing a proportional-integral-derivative (PID) controller tries to maintain the overall balance between the voltages of the heater and the set resistor such that the error in the voltage difference measured by an instrumentation amplifier is least.

To show the thermal stability of the system, an experiment was conducted in which an external temperature perturbation was introduced by shining a white light source on the sample. When the light is on, a temperature variation of 1 K is introduced to the filter chip. With the closed-loop feedback, the temperature variation is reduced to an average fluctuation of 80 mK, which is equivalent to the frequency variation of 280 MHz (Figure 2). The speed of the feedback circuit to compensate for the temperature perturbation is on the order of a few tens of milliseconds.



▲ Figure 1: An SEM picture of the microring heater on top of the filter.



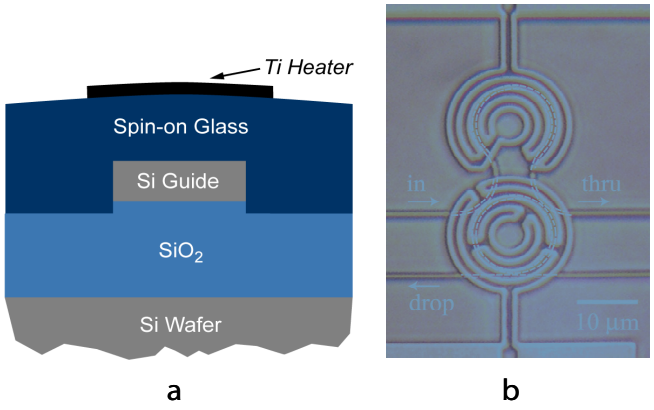
▲ Figure 2: Thermal control achieved within 80 mK of the absolute value for the second-order ring resonator using feedback control loop.

Nanofabrication of Hitless Reconfigurable Optical Add-drop Multiplexers Based on Silicon Microrings

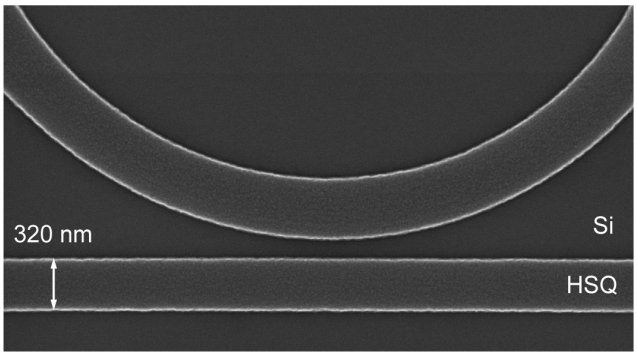
C.W. Holzwarth, T. Barwicz, M.A. Popovic, P.T. Rakich, M. Dahlem, F. Gan, E.P. Ippen, F.X. Kaertner, H.I. Smith
Sponsorship: DARPA, internal funds

Reconfigurable optical add-drop multiplexers (ROADMs) are key components of modern optical networks. Data in optical fibers is carried at numerous wavelengths, each defining a specific "channel." The ROADMs allow the rerouting ("droping") of a subset of the data channels traveling in an optical fiber, replacing these with new data streams ("adding") at the previously rerouted wavelengths. The term "reconfigurable" indicates that the subset of dropped channels can be changed "on the fly," i.e., while the ROADM is in operation. For a ROADM to be truly useful in an optical network it must be "hitless," that is, it must enable tuning from one channel to a second channel without affecting the data transmitted on any of the other channels.

In our previous work, we developed precision nanofabrication techniques that enabled us to demonstrate the most advanced microring filters reported to date in silicon-rich silicon nitride [1,2]. In the present work, we employed silicon microrings to take advantage of their lower optical loss and higher thermo-optic coefficient, allowing wide tuning of the operating wavelengths of the ROADM via integrated heaters. Figure 1 presents a cross-sectional diagram and top-view micrograph of our implementation of a silicon waveguide and a hitless ROADM with integrated microheaters. Line-edge roughness is of critical concern in silicon waveguides as it translates into significant propagation loss via scattering of the guided mode. We found that the smoothest waveguides were obtained using hydrogen silsesquioxane (HSQ) as an e-beam resist and an etch-mask for the subsequent HBr-based reactive-ion etching. Figure 2 presents a scanning-electron micrograph of a coupling region between a microring and a bus waveguide defined in HSQ. The patterning is based on scanning-electron-beam lithography.



▲ Figure 1: (a) Cross-sectional schematic of a silicon waveguide with an integrated titanium heater. Spin-on glass is used for the upper cladding of the waveguide to allow self-planarization and to avoid filling problems in narrow gaps. (b) Top-view optical micrograph of the silicon-microring hitless ROADM with titanium microheaters.



▲ Figure 2: Top-view scanning-electron micrograph of a coupling region defined in HSQ. The patterning is done with scanning-electron-beam lithography. The minimum feature size required (e.g., the gap) is ~100 nm and must be controlled to ~ 5 nm.

References

[1] M.A. Popovic, T. Barwicz, M.R. Watts, P.T. Rakich, L. Socci, E.P. Ippen, F.X. Kaertner, and H.I. Smith, "Multistage high-order microring-resonator add-drop filters," *Optics Letters*, to be published.

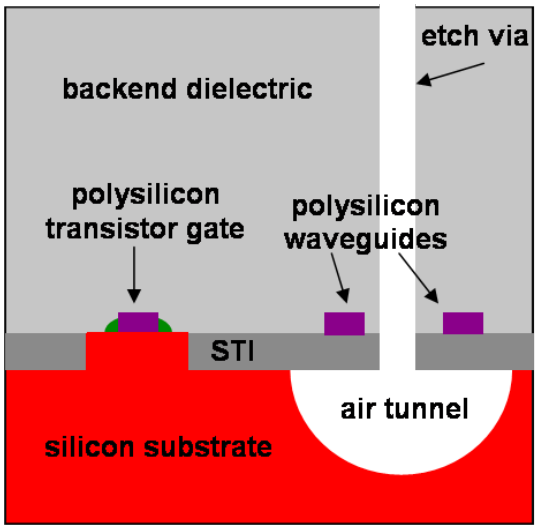
[2] T. Barwicz, M.R. Watts, M.A. Popovic, P.T. Rakich, E.P. Ippen, F.X. Kaertner, and H.I. Smith, "Polarization-insensitive optical add-drop multiplexers in silicon nitride," Massachusetts Institute of Technology, Cambridge, MA, Microsystems Technology Laboratories Annual Research Report, 2008.

Localized Substrate-Removal Technique Enabling Optical Intrachip Communication in Bulk-Silicon CMOS

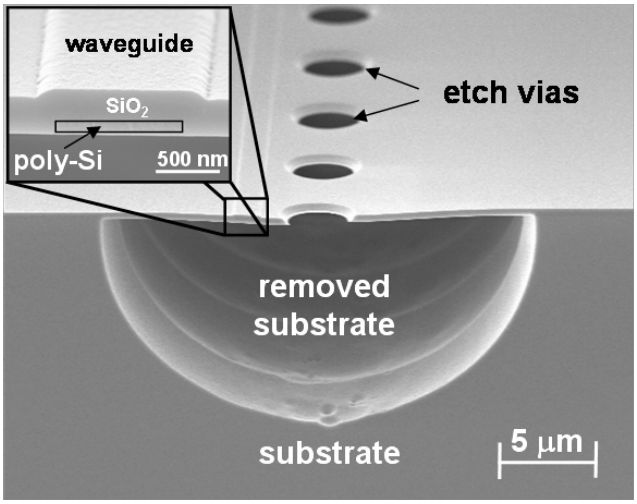
C.W. Holzwarth, J.S. Orcutt, J. Sun, H. Li, M.A. Popovic, V. Stojanović, J.L. Hoyt, R.J. Ram, H.I. Smith
Sponsorship: DARPA

Efforts elsewhere to integrate photonics with CMOS electronics requires customization of the fabrication process to provide low-loss in the photonic components [1]. This compromises electronic performance, throughput, and cost. Customizations include thick low-index cladding layers, silicon-on-insulator material and electron-beam lithography. While tolerable for some applications, such customization is considered unacceptable for microprocessors and DRAM, circuits that would benefit the most from optical intrachip communication. In order to integrate photonics with circuits produced in high volume, one must be able to work within the constraints of commercial bulk CMOS process flows by utilizing industry-standard material layers, thicknesses, processing steps and tools. Waveguides fabricated out of the polysilicon layer used for transistor gates and poly-resistors above the shallow-trench isolation (STI) layer would have a propagation loss of the order of 1000 dB/cm since the STI layer (<400 nm) is not thick enough to prevent the guided optical mode from "leaking" into the high-index Si substrate.

To overcome this problem, we have developed a novel post-processing technique using XeF_2 to locally remove the silicon underneath the STI layer, as shown in Figure 1. The creation of air tunnels under the polysilicon waveguides eliminates propagation loss due to leakage into the substrate, and minimizes impact on the electrical, thermal, and mechanical performance of the electronics. XeF_2 gas is used because it etches Si isotropically, can undercut large areas without stiction problems, and has a high silicon-to-oxide etch-rate selectivity (>1000:1). We have used this method to fabricate waveguides in polysilicon-on-oxide films (Figure 2). The propagation loss of these waveguides was measured to be ~10 dB/cm at 1550 nm. Most of this loss is attributed to material absorption and scattering from surface and sidewall roughness [2].



▲ Figure 1: Sketch of the cross-section of a bulk CMOS chip showing how electronics and photonic devices can be fabricated on the same chip with the addition of only a post-processing step to locally remove the silicon substrate beneath the polysilicon waveguides.



▲ Figure 2: Scanning-electron micrograph of fabricated poly-silicon waveguide using the XeF_2 based substrate removal technique. The inset shows a close-up of the waveguide. The SiO_2 cladding beneath the poly-silicon is only 50 nm thick, resulting in loss >1000 dB/cm before the localized substrate removal step. After removal, the loss is reduced to approximately 10 dB/cm.

References

[1] J.S. Orcutt et al., "Demonstration of the first electronic photonic integrated circuit in a commercial scale bulk CMOS Process," submitted to the *Conference of Lasers and Electro-Optics*, San Jose, California, May 2008.

[2] C.W. Holzwarth et al., "Localized Substrate Removal Technique Enabling Strong-Confinement Microphotonics in Bulk-Si CMOS Processes," submitted to the *Conference of Lasers and Electro-Optics*, San Jose, California, May 2008.

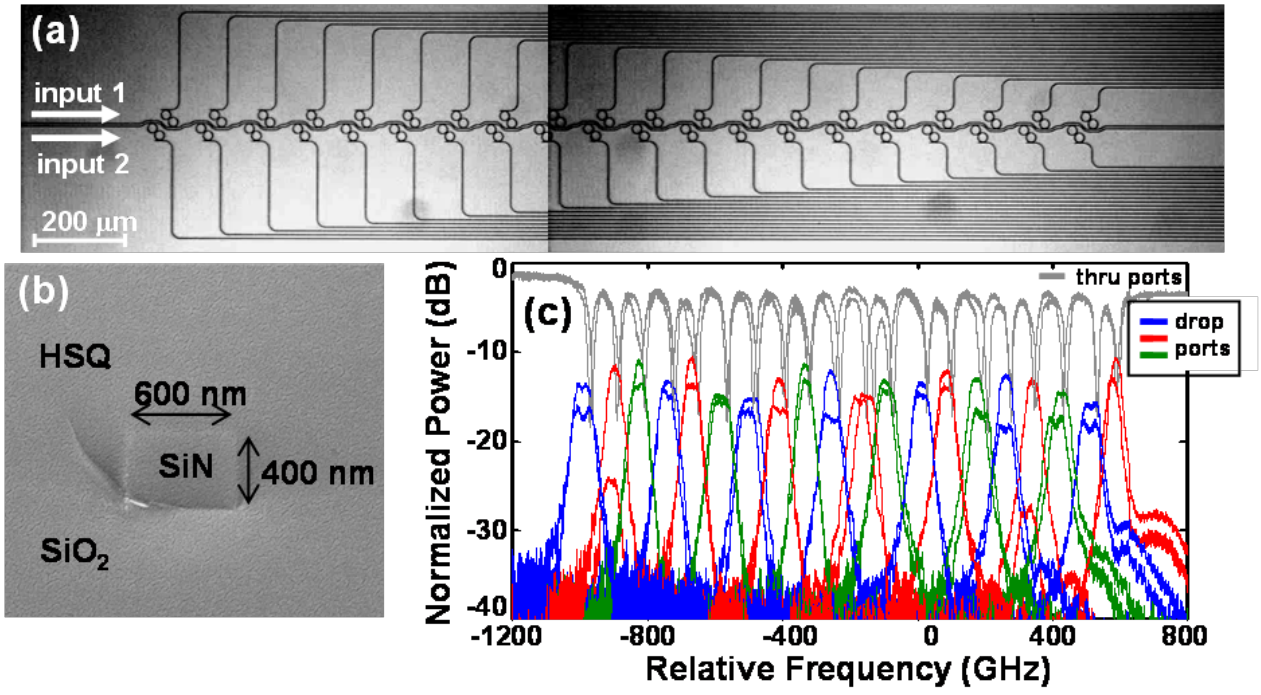
Nanofabrication of Optical Microring Filter Banks for Ultra-Fast Analog-to-Digital Converters

C.W. Holzwarth, T. Barwicz, M.A. Popović, A. Khilo, M. Dahlem, E.P. Ippen, F.X. Kärtner, H.I. Smith

Sponsorship: DARPA

Progress in designs and nanofabrication techniques for microring-resonators in high-index-contrast materials have made possible the wide spectral spacing between resonances and low loss required for electronic-photonic integrated circuits including ultra-fast analog-to-digital converters [1]. Achieving accurate resonant-frequency spacing of microring-filters is critical for these devices. In the NanoStructures Laboratory we have developed a technique using scanning-electron-beam lithography (SEBL) that is capable of accurately controlling the resonant frequency spacing in microring-resonator filter banks. The resonant wavelength of a microring-resonator filter is dependant on both the ring radius and the effective index of refraction of the ring waveguide. The effective index is controlled lithographically by controlling the width of the ring waveguide. Although it is simple to change both the width and the radius of the ring in the SEBL layout, this is limited to discrete jumps corresponding to the step size of the SEBL system. In order to have 1 GHz control of the resonant frequency for the designed filters the SEBL systems would need a step size of 30 pm. In our process this limitation of discrete step size is overcome by modulating the electron beam dose to precisely control the width of the ring waveguide [2].

In our experiment second-order microring-resonator filters, fabricated in silicon-rich silicon nitride and overcald with HSQ, were used in a microring filter banks (Figure 1a, 1b). Using dose modulation, twenty-channel dual-filter banks with a target channel spacing of 80 GHz were fabricated and tested, demonstrating control of changes in the average ring-waveguide width of 0.10 nm, despite the 6 nm SEBL step size (Figure 1c). Variations between filter responses were due to slight frequency mismatches between rings of the same filter, we demonstrated that this can be corrected by thermal trimming with integrated microheaters.



▲ Figure 1: a) Scanning-electron micrograph of fabricated second-order twenty-channel dual-filter bank and b) cross-section of overclad waveguide. c) Filter response of second-order twenty-channel dual-filter bank with an average channel spacing of 83 GHz.

References

[1] T. Barwicz, M.A. Popovic, P.T. Rakich, M.R. Watts, H.A. Haus, E.P. Ippen, and H.I. Smith, "Microring-resonator-based add-drop filters in SiN: fabrication and analysis," *Optics Express*, vol. 12, no. 7, pp. 1437-1442, Apr. 2004.

[2] C.W. Holzwarth, T. Barwicz, M. A. Popović, P. T. Rakich, F. X. Kaertner, E. P. Ippen, and H. I. Smith, "Accurate resonant frequency spacing of microring filters without postfabrication trimming," *Journal of Vacuum Science and Technology B*, vol. 24, no. 6, pp. 3244-3247, Nov. 2006.

Three-Dimensional Photonic Crystals in Si_3N_4 and Si by Assembly of Prepatterned Membranes

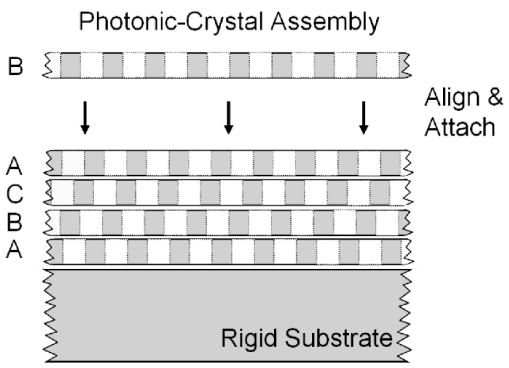
A.A. Patel, C. Fucetola, E.E. Moon, H.I. Smith
Sponsorship: NSF, DTRA

The diffraction of light within periodic structures (so-called "photonic crystals") offers a wide variety of opportunities for controlling and manipulating light. Most research to date has focused on 2-dimensional (2D) photonic crystals, because highly developed planar-fabrication techniques (i.e., lithography followed by pattern transfer) are directly applicable. However, the full potential of photonic crystals in futuristic sensing, communication and computation systems is best achieved with 3-dimensional (3D) structures. The problem is that new methods of 3D fabrication need to be developed to achieve desired complex structures over large areas with low cost and high yield.

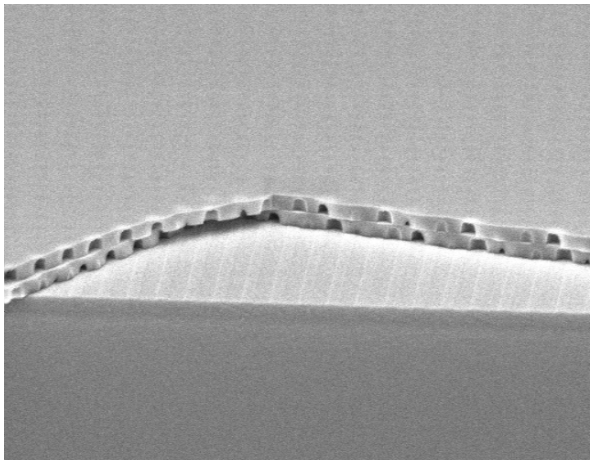
Interference lithography can produce periodic 3D structures in photosensitive polymers, but the introduction of deviations from perfect periodicity (i.e., waveguides and structures that constitute "devices" within the periodic matrix, so-called "defects") is highly problematic. Moreover, it's not clear that backfilling 3D polymeric structures is applicable to a suitable range of materials. Layer-by-layer methods the use scanning-electron-beam lithography enable the controlled introduction of defects, but such fabrication is generally tedious, slow, low yield, and covers impractically small areas (e.g., <0.1mm on edge).

We describe a novel approach in which the 3D photonic-crystal structure is fabricated by assembling membranes that are patterned in advance using conventional planar methods (Figure 1). This approach minimizes the yield problem because membranes can be inspected and selected before assembly, and the desired waveguides and devices, can be introduced at any level in the assembly. When brought into contact, membranes that are free of particulate and other contamination will bond spontaneously by van der Waals or other mechanisms.

Previously we reported using low-stress Si_3N_4 membranes as the test vehicle. 2D periodic structures were etched into free-standing membranes, and nonaligned stacking carried out (Figure 2). Currently, we are addressing the lithographic challenge of patterning a large-area photonic structure in conjunction with custom alignment marks that will assist in gap detection and lateral overlay. In addition, we are developing a process for creating 3D photonic crystals in Si, using coherent-diffraction lithography and HBr reactive-ion etching. The Si membranes are obtained from SOI wafers.



▲ Figure 1: Depiction of the layer-by-layer stacking approach to 3D photonic crystal fabrication. All the layers in the photonic crystal are fabricated in parallel. This reduces processing cycles, which will help improve yield and reduce lead times.



▲ Figure 2: Initial stacking experiment. A patterned SiN membrane is brought into contact with SiN substrate. The pitch of the array is 600nm and the membrane is 350nm thick. A second patterned membrane is brought into contact with the first.

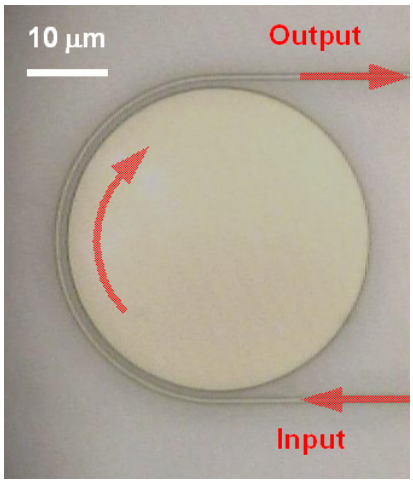
Reference

[1] A.A. Patel and H.I. Smith, "Membrane stacking: A new approach for three-dimensional nanostructure fabrication," *Journal of Vacuum Science and Technology B*, vol. 26, no. 6, pp. 2662-2664, Nov. 2007.

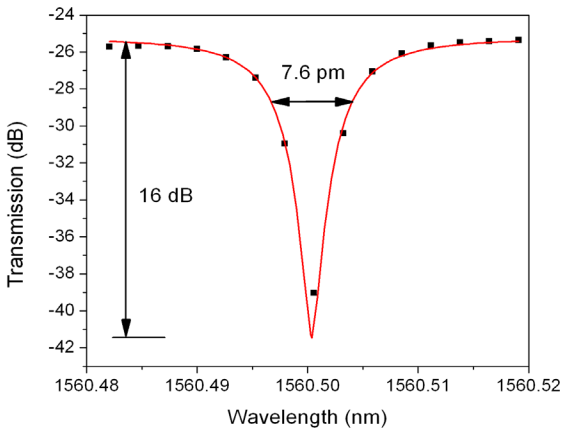
Integrated HIC High-Q resonators in Chalcogenide Glass

J.J. Hu, N. Carlie, N.N. Feng, L. Petit, A. Agarwal, K. Richardson, L.C. Kimerling
Sponsorship: DOE

Optical resonance enhancement, combined with a significantly increased optical path length, makes ring resonators an ideal device platform for both fundamental investigations and practical applications based on photon-matter interactions. To date, most planar glass resonators have been fabricated with silica. Compared to silica, chalcogenide (ChG) glasses are superior material candidates for the aforementioned applications due to their unique optical properties in the infrared wavelengths. Of particular relevance here are the reduced phonon-quenching, the large Kerr optical non-linearity, and the wide infrared transparency window of ChG materials. We report the fabrication of integrated high-index-contrast (HIC) microring and microdisk resonators using a CMOS-compatible lift-off technique [1] in thermally evaporated As_2S_3 chalcogenide glass films. We demonstrate a new pulley-type configuration for optical coupling from photonic wire waveguides into these HIC micro-resonators with improved coupling efficiency. The WGM (whispering gallery mode) in micro-disk chalcogenide resonators exhibits a cavity Q as high as 205,000. Such a high Q-value represents a 20-fold improvement compared to chalcogenide glass photonic crystal resonators [2] and our recently demonstrated racetrack rings [3], and it is 2.5 times that of non-planar chalcogenide glass microspheres [4]. We also show that such resonators can be used as ultra-sensitive probes of photosensitivity in chalcogenide glass, providing an unprecedentedly high accuracy measurement (on the order of 10^{-8} RIU) of photorefractive index change. Monte-Carlo simulations and a peak fitting algorithm are employed to quantitatively assess the performance matrices as a function of cavity Q-factor and reasonable agreement with experiments is confirmed. We show that such a high wavelength resolution projects high sensitivity for both refractometry-based biological sensing and evanescent wave-based chemical detection.



▲ Figure 1: Optical micrograph of a 20-µm-radius pulley-type As_2S_3 microdisk resonator.



▲ Figure 2: A transmission spectrum near a TM-polarization resonant peak: the black dots are experimental data points and the red curve is the fitted Lorentzian peak.

References

[1] J. Hu, V. Tarasov, N. Carlie, N. Feng, L. Petit, A. Agarwal, K. Richardson, and L. Kimerling, "Si-CMOS-compatible lift-off fabrication of low-loss planar chalcogenide waveguides," *Optics Express*, vol. 15, p. 11798, 2007.

[2] Y. Ruan, M. Kim, Y. Lee, B. Luther-Davies, and A. Rode, "Fabrication of high-Q chalcogenide photonic crystal resonators by e-beam lithography," *Applied Physics Letters*, vol. 90, p. 071102, 2007.

[3] J. Hu, N. Carlie, L. Petit, A. Agarwal, K. Richardson, and L. Kimerling, "Demonstration of chalcogenide glass racetrack micro-resonators," *Optics Letters*, vol. 33, p. 761, 2008.

[4] G. Elliott, D. Hewak, G. Murugan, and J. Wilkinson, "Chalcogenide glass microspheres: Their production, characterization and potential," *Optics Express*, vol. 15, p. 17542, 2007.

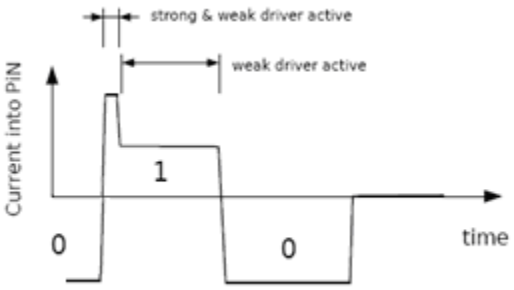
Digital Equalization of the Nonlinear Photonic Modulator Diode

B. Moss, A. Joshi, J. Orcutt, V. Stojanović
Sponsorship: DARPA, Texas Instruments

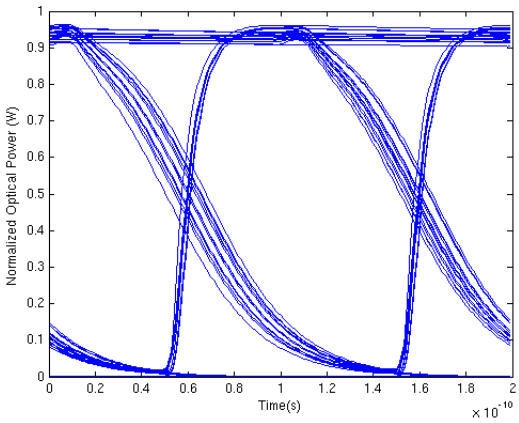
Electro-optical modulators are fundamental building blocks in on-chip photonic systems. On-chip optical waveguides can be created from thin unsilicided polysilicon tracks in a bulk CMOS process. The index of refraction of the poly waveguide depends on the charge concentration in the waveguide. Varying this charge concentration changes the phase of the light through the waveguide. In order to inject large amounts of charge into the waveguide more effectively, a P-I-N diode structure is created with the waveguide acting as the intrinsic region (I region) and N- and P-type doping added on either side of the waveguide.

We modified an existing SPICE model [1-2] of a P-I-N diode to model the photonic modulator. Figure 1 shows a digital circuit that controls the amount of charge entering the I region. This circuit uses a push-pull topology with pre-emphasis. The pre-emphasis controls the amount of charge that must enter and leave the I region for each bit, lowers the energy per bit, and prevents the ring's optical passband from shifting into the next optical channel. At the beginning of a zero-to-one transition, both the strong driver and the weak driver are active, maximizing the current into the I region. After a short time, the strong driver deactivates, lowering the current into the diode. The unbalanced weak driver has a strong NMOS and a weak PMOS. The strong NMOS ensures that the device quickly discharges through the I region for a one-to-zero transition. Figure 2 shows the simulated eye diagram for 10Gb/s.

Two flavors of this ring modulator were taped out with a 65-nm TI process. One modulator has a larger weak driver to account for varying carrier lifetimes in the diode. The energy efficiency is predicted to be approximately 50 fJ/bit.



▲ Figure 1: Abstract modulator diagram and its corresponding pre-emphasized current profile for a 010- input bit pattern. The weak driver has a very strong NMOS and a weak PMOS.



▲ Figure 2: Simulated eye diagram for 10Gb/s, assuming a 1-ns carrier lifetime.

References

[1] A.G.M. Strollo, "A new SPICE model of power P-I-N diode based on asymptotic waveform evaluation," *IEEE Transactions on Power Electronics*, vol. 12, no. 1, pp. 12-20, Jan. 1997.

[2] J. Kyhala and M. Andersson, "An advanced PIN-diode model," *Microwave Journal*, vol. 48, no. 9, pp. 206-212, Sept. 2005.

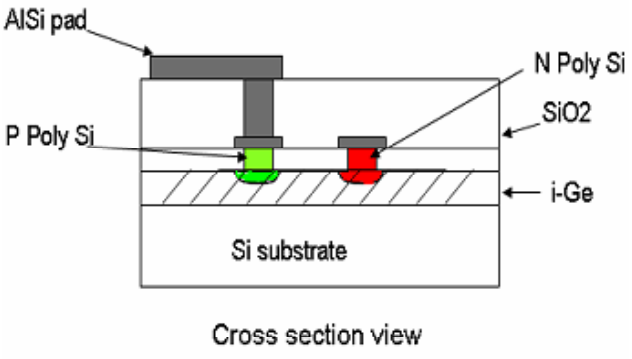
High-speed Large-area Ge Photodetectors on Si

J. Cheng, W. Giziewicz, J. Liu, C.-Y. Hong, L.C. Kimerling, J. Michel

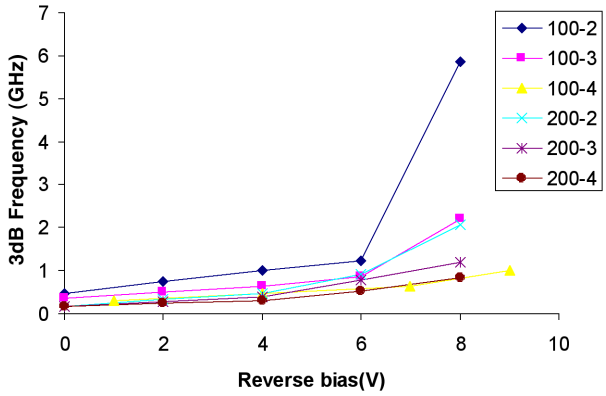
We have designed and demonstrated lateral Ge p-i-n photodiodes on Si with 100-μm and 200-μm diameters and GHz bandwidth working at 850 nm. These lateral devices demonstrate a significant bandwidth improvement compared to vertical junction devices of the same area due to the reduction of capacitance. The devices were fabricated with 500-nm CMOS process technology, which enables large scale production at relatively low cost compared to III-V devices.

Figure 1 shows the structure of a lateral Ge-on-Si photodetector schematically. A lateral detector with interdigitated electrode is chosen over vertical junction detectors because of much lower capacitance per unit device area. The simulations done by MEDICI software show that a normalized external quantum efficiency of 71% can be achieved. The bandwidths are examined for 50-, 100- and 200-μm diameter devices with different finger spacings. Devices on n-type substrates have high bandwidth due to the full depletion of the inter-finger region. For a 100-μm-diameter device, a 10-Gb/s data rate can be reached at a relatively low voltage of 3V [1].

The devices were fabricated completely on a standard 0.5-μm CMOS line[2]. The frequency responses of the detectors are carried out by an Agilent N5230A Vector Network Analyzer using a 850-nm VCSEL. Figure 2 shows the frequency response of the photodetectors with different diameters and finger spacings. The 100-μm -diameter devices reach 6-GHz bandwidth, while devices with 200 μm diameters reach 2.2 GHz. These bandwidths are about 5 times higher than ideal vertical detectors with the same Ge film thickness and contact pad area.



▲ Figure 1: Schematic structure of a lateral Ge p-i-n photodetector on Si.



▲ Figure 2: Frequency response of lateral Ge p-i-n devices.

References

[1] W. Giziewicz, "High performance photodetectors for multimode optical data links," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2006.

[2] J.F. Liu, J. Michel, W. Giziewicz, D. Pan, K. Wada, D. Cannon, L.C. Kimerling, J. Chen, F.O. Ilday, F.X. Kartner, and J. Yasaitis, "High-performance, tensile-strained Ge p-i-n photodetectors on a Si platform," *Applied Physics Letters*, vol. 87, no. 10, pp. 103501:1-3, Sept. 2005.

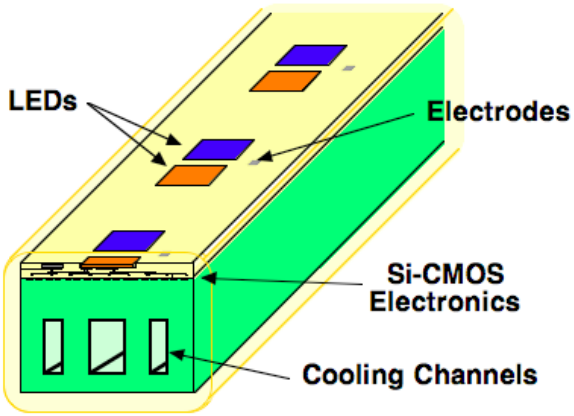
Recess Integration of GaN LEDs on Si IC Micro-probes for Optical Control of Excitable Cells

H. Soumare, C.G. Fonstad (in coll. with E. Boyden, MIT)
Sponsorship: MIT Media Lab Director's Innovator Award

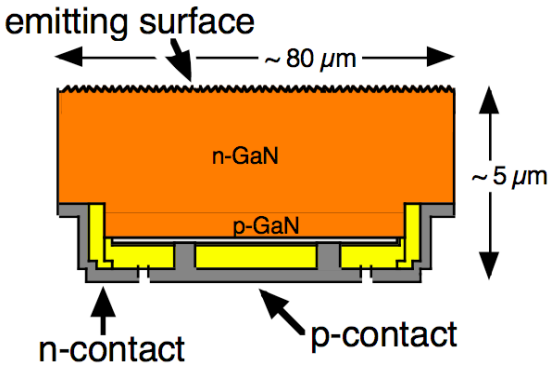
Professor Ed Boyden uses light to precisely control aberrant neuron activity. His lab has invented safe, effective ways to deliver light-gated membrane proteins to neurons and other excitable cells (e.g., muscle, immune cells, pancreatic cells, etc.) in an enduring fashion, thus making the cells permanently sensitive to being activated or silenced by millisecond-timescale pulses of blue and yellow light, respectively [1]. This ability to modulate neural activity with a temporal precision that approaches that of the neural code itself holds great promise for human health, and his lab has developed animal models of epilepsy and Parkinson's disease to explore the use of optical control to develop new therapies. His work has attracted international attention and has appeared in numerous articles, including a recent piece in the Science Times section of the New York Times [2], and a profile of his lab for the Discovery Channel's "Top 5 Science Stories of the Year."

The powerful micro-hybrid assembly and integration techniques that Professor Fonstad's group has recently developed and used to integrate vertical cavity surface emitting lasers (VCSELs) within silicon CMOS integrated circuits, and edge-emitting laser diodes with dielectric waveguides on silicon wafers, provide a path to making needle probes with many individually addressable blue and yellow micro-LEDs spaced along their length. An LED needle like this with ten to twenty micro-LED pairs would be similar in diameter to a single optical fiber like those now being used by Professor Boyden, yet it would serve the function of many fibers and, in fact, would enable researchers to conduct studies that are impossible to do with a single fiber, or even with multiple fibers. The same needle could also have electrodes along it to simultaneously monitor electrical activity in the stimulated regions, on-board CMOS electronics to control all functions, and cooling channels to eliminate all thermal impact.

Professors Boyden and Fonstad have initiated collaborative efforts to develop such a probe, with the immediate target being a simpler probe with LEDs and electrodes, with all external control and signal processing electronics. This probe will address all of the key challenges, so that future expansion to integrated electronics and cooling will be possible.



▲ Figure 1: A cartoon illustrating the LED needle probe that is the ultimate target of this research program. The initial needles will be passive without integrated electronics or cooling, and the focus of the program will be on developing micro-pill LEDs (see Figure 2) suitable for use with the recess integration technology that has been developed at MIT. The work will ultimately be extended to active IC foundations.



▲ Figure 2: A cross-sectional cartoon (not to scale) of an LED micro-pill. The pill thickness will be 5 to 6 microns and the width will be 80 to 100 microns. Both n-side and p-side contacts are made to same side of the pill and the upper emitting surface is roughened to enhance light extraction.

References

[1] X. Han and E.S. Boyden, "Multiple-color optical activation, silencing, and desynchronization of neural activity, with single-spike temporal resolution," PLoS ONE 2(3): e299. DOI: 10.1371/journal.pone.0000299.

[2] *The New York Times*, Science Section, Aug. 14, 2007, p. D1.

Co-axial Integration of III-V Ridge-waveguide Gain Elements with SiO_xN_y Waveguides on Silicon

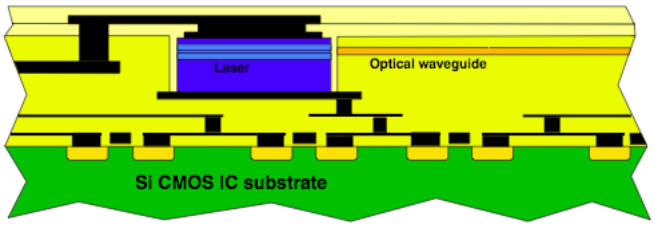
J. Diaz, S. Famenini, E. Barkley, J. Rumpler, J. Perkins, C.G. Fonstad
Sponsorship: Vitesse Chair

Our ongoing research integrating 1.55-μm III-V ridge waveguide gain elements (i.e., diode lasers and semiconductor optical amplifiers) co-axially aligned with and coupled to silicon oxy-nitride waveguides on silicon substrates has made significant strides in the past year. We are working towards the goal of co-axially coupling III-V laser diodes and semiconductor optical amplifiers with waveguides on Si wafers using techniques consistent with fabricating waveguides on Si-CMOS wafers and integrating the III-V gain elements after all standard front- and back-end Si processing has been completed.

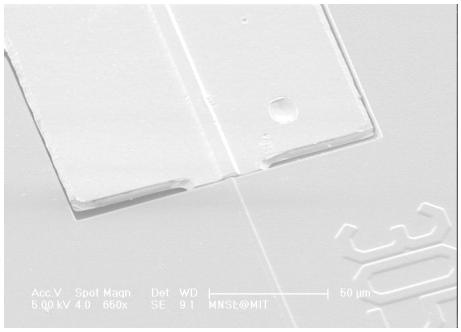
A novel micro-cleaving technique has been used to produce active ridge waveguide platelets on the order of 6 μm thick and 100 μm wide, with precisely controlled lengths (in the current work 300 ± 1.25 μm) and very high-quality end facets. Typical ridge guide platelet lasers have thresholds under 30 mA.

Passive micro-cleaved platelets have been integrated within dielectric recesses etched through the oxy-nitride (SiO_xN_y) waveguides on a wafer so the ridge and SiO_xN_y waveguides are co-axially aligned. Transmission measurements indicate coupling losses are as low as 5 db with air filling the gaps between the waveguide ends, and measurements made through filled gaps indicate that the coupling losses can be reduced to below 1.5 dB with a high index (n = 2.2) dielectric fill. Simulations indicate that with further optimization of the mode profile in the III-V waveguide the loss can be reduced to below 1 dB.

We have also performed extensive device design and optimization for co-axial recess integration and have recently completed a comparison of co-axial coupling with the evanescently coupled III-V/Si hybrid integration approach recently introduced by researchers at UCSB and Intel. The latter comparison revealed that the approach we have taken, co-axial end-fire coupling, and the UCSB/Intel approach, vertical evanescent coupling, are complementary, with each optimal for certain applications. At the same time it pointed out a number of distinct advantages for co-axial coupling of recess-integrated platelet lasers including higher operating efficiency, smaller device footprint, greater flexibility in choice of materials, lower cost, higher modularity, and easier integration of different wavelength emitters [1].



▲ Figure 1: A cartoon illustrating the recess-mounting and co-axial alignment approach to integrating III-V gain elements (edge-emitting in-plane laser diodes, EELs, and semiconductor optical amplifiers, SOAs) with silicon oxy-nitride waveguides on silicon integrated circuit chips and silicon photonic integrated circuits platforms.



▲ Figure 2: A close-up photomicrograph showing the alignment between a InGaAsP/InP ridge waveguide platelet and a buried silicon oxy-nitride waveguide. Coupling losses as low as 3 dB were measured.

References

[1] C.G. Fonstad, J.J. Rumpler, E.R. Barkley, J.M. Perkins, and S. Famenini, "Recess integration of micro-cleaved laser diode platelets with dielectric wave-guides on silicon," in *Proc. Novel In-plane Semiconductor Lasers Conference VII, Photonics West 2008,* Jan. 22, 2008; *SPIE Conference Proc.*, vol. 6909.

Magnetically-assisted Assembly, Alignment, and Orientation of Micro-scale Components

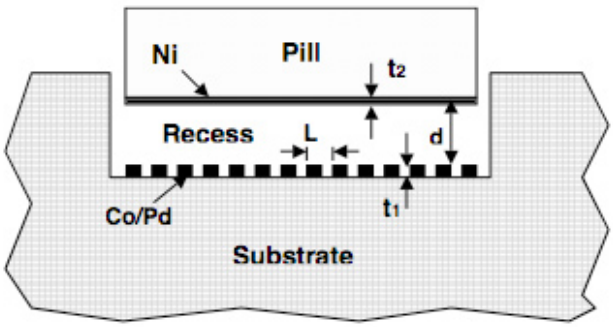
D. Cheng, J. Perkins, J. Rumpler, C.G. Fonstad (in coll. with F. Cadieu, Queens College of CUNY; M. Zahn, MIT)
Sponsorship: Vitesse Chair

The use of magnetic forces to improve fluidic self-assembly of micro-components has been investigated using Maxwell 3D to model the forces between Ni thin films on semiconductor device micro-pills and Sm-Co thin films patterned on target substrates. Orienting and restraining forces on pills far in excess of gravity are predicted, and it is found that the fall-off of these forces with pill-to-substrate separation can be engineered through the proper design of the Sm-Co patterns to retain only properly oriented pills [1].

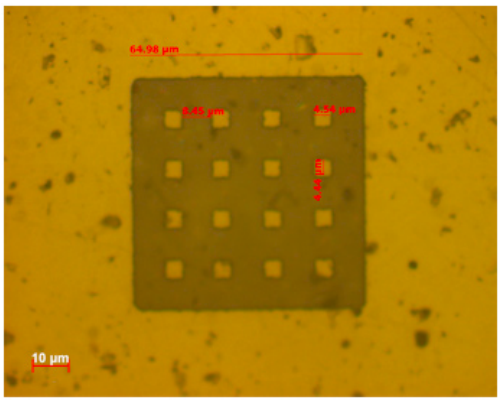
Micro-scale hybrid assembly is a potentially important way of doing heterogeneous integration, i.e., of integrating new materials on silicon integrated circuits to obtain functionality not readily available from silicon device structures alone, and fluidic self-assembly is an attractive way to automate micro-scale assembly. A serious limitation of fluidic self-assembly, however, is the lack of a good method for holding properly assembled components in place and accurately positioned until all of the components have been assembled and they have been permanently bonded in place. We have shown, based on our modeling, that suitably patterned magnetic films can be used to provide the forces necessary to retain, and to accurately orient and position, assembled micro-components.

Our motivation for pursuing micro-scale hybrid assembly is our general interest in doing optoelectronic integration, specifically of vertical cavity surface emitting lasers (VCSELS), edge-emitting lasers (EELs), and light emitting diodes (LEDs), with state-of-the-art, commercially processed Si-CMOS integrated circuits. Our ongoing research integrating these devices on silicon described elsewhere in this report provides the context for this work and illustrates the types of applications we envision for magnetically assisted self-assembly using the results of this study.

Assembly experiments to verify and demonstrate the theoretical predictions are currently in progress using two sizes of 6-μm thick pills (50 μm by 50 μm, and 50 μm by 100 μm), and a variety of magnetic thin film patterns. Recesses with different dimensions are also being studied.



▲ Figure 1: A cross-sectional cartoon illustrating the application of magnetically assisted assembly to recess integration. The variables indicated in the drawing correspond to the model used to calculate the magnetic force intensity.



▲ Figure 2: A microphotograph of a patterned samarium cobalt magnetic thin film. The abilities to, first, sputter deposit, and second, wet etch thin films like this are critical to the successful implementation of magnetic self-assembly and are unique strengths of the MIT/Queens College effort.

References

[1] D. Cheng, C.G. Fonstad, and M. Zahn, "Simulation and design of forces during magnetically assisted fluidic self-assembly," *Ansoft First-Pass System Success Application Workshop*, Oct. 19, 2007, Newton, MA (invited talk and poster).

[2] D. Cheng, "Theoretical and experimental study of magnetically assisted fluidic self assembly," Master's thesis, Massachusetts Institute of Technology, Cambridge, 2008.

Micro-cleaved Laser Diode Platelets Integrated on Silicon

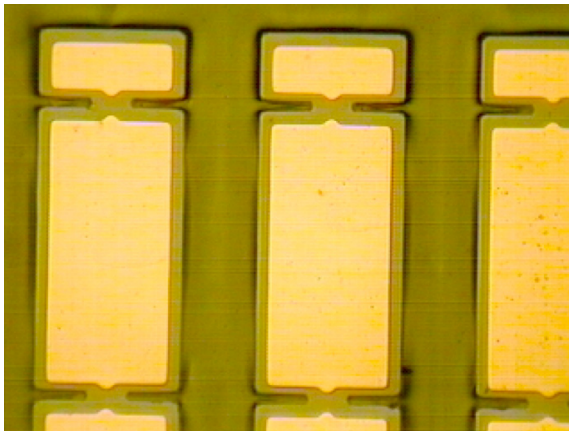
J. Rumpler, C.G. Fonstad

Sponsorship: DARPA through ARL; Lincoln Laboratory IPI Program

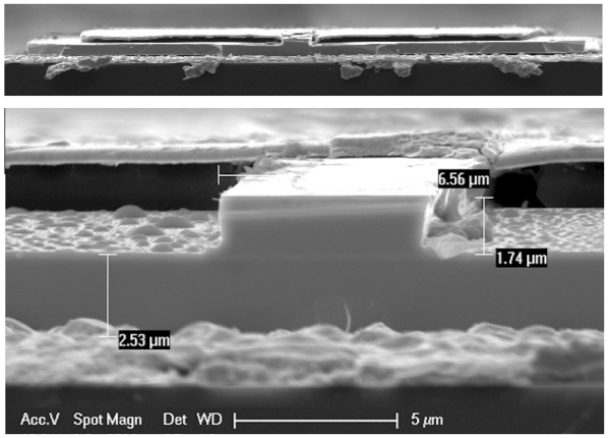
Thin (6-μm) InP-based multiple-quantum-well (MQW) ridge laser platelets emitting at a wavelength of 1550 nm have been manufactured and integrated by metal-to-metal bonding onto silicon substrates. These laser platelets can be thought of as freestanding optoelectronic building blocks that can be integrated as desired on diverse substrates. These blocks are fully processed lasers, with both top-side and bottom-side electrical contacts. The thinness of these optoelectronic building blocks and the precision with which their dimensions are defined are conducive to assembling them in dielectric recesses on a substrate, such as silicon, as part of an end-fire coupled optoelectronic integration strategy [1]. They are assembled by a micro-scale pick-and-place technique that allows the blocks to be picked up individually and placed as desired on the substrate of choice. Final integration is accomplished using pressurized polymer film to hold the platelets in place as they are metal-to-metal solder bonded to the Si substrate.

To enable the manufacture of these laser platelets, a novel micro-cleaving process technology has been developed that uses notched bars of lasers as shown in Figure 1 to accurately locate the point of cleavage. This novel micro-cleaving process is used to simultaneously obtain both smooth end facets and precisely defined cavity lengths. As a proof of concept, this process has been shown to achieve nominal cavity lengths of 300 μm +/- 1.25 μm. We believe that this micro-cleaving process can be used to make thin platelet lasers having much shorter cavity lengths and that with minor adjustments it can be used to achieve better than 1-μm length precision.

For the 300-μm-long, 6-μm-thin, micro-cleaved ridge platelet lasers integrated onto silicon substrates, as shown in Figure 2, continuous-wave lasing at temperatures as high as 55˚C and pulsed lasing at temperatures to at least 80˚C have been achieved. These lasers have output powers as high as 26.8 mW (at T = 10.3˚C), differential efficiencies as high as 81% (at T = 10.3˚C), and threshold currents as low as 18 mA (at T = 10.3˚C). The characteristic temperatures, T_0 and T_1, of the lasers on silicon were 43 K and 85 K, respectively. The thin micro-cleaved ridge platelet lasers integrated onto silicon outperformed conventionally cleaved multiple-quantum-well (MQW) ridge lasers on their native InP substrate in terms of thermal characteristics, output power, and differential efficiency [2].



▲ Figure 1: A back-side view of platelet lasers bars after front-side processing has been completed and the wafer has been mounted face-down on a carrier wafer, the substrate removed, and the back-side metal deposited and patterned. The bars will next be released and micro-cleaved to produce individual platelet lasers approximately 150-μm wide and 300-μm long.



▲ Figure 2: Close-up photomicrographs showing, in the top portion of the figure, a platelet bonded on a silicon wafer. A close-up view of the micro-cleaved end facet and the ridge waveguide is shown in the lower portion of the figure. Note also the stripe ohmic contact on top of the mesa and the broad-area top contact pad (insulated by a BCB support layer).

References

[1] C.G. Fonstad, J.J. Rumpler, E.R. Barlkley, J.M. Perkins, and S. Famenini, "Recess integration of mirco-cleaved laser diode platelets with dielectric wave-guides on silicon," in *Proc.Novel In-plane Semiconductor Lasers Conference VII, Photonics West 2008*, Jan. 22, 2008; SPIE Conference Proc. vol. 6909.

[2] J.J. Rumpler II, "Micro-cleaved ridge lasers for optoelectronic integration on silicon," Ph.D. Thesis, Massachusetts Institute of Technology, Cambridge, 2008.

Low-threshold Vertical Cavity Surface-emitting Lasers Recess Integrated within Silicon CMOS Integrated Circuits

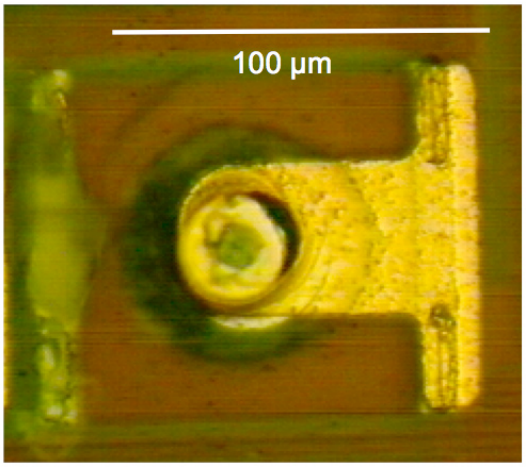
J.M. Perkins, C.G. Fonstad
Sponsorship: NSF

Optoelectronic devices intimately integrated on silicon integrated circuits have long been sought for optical intercon-nect applications in an effort to improve data transfer rates in high performance circuits. A new heterogeneous integration technique for integrating vertical cavity surface emitting lasers (VCSELs) on silicon CMOS integrated circuits for such applications has been developed and demonstrated for the first time in our group at MIT [1, 2].

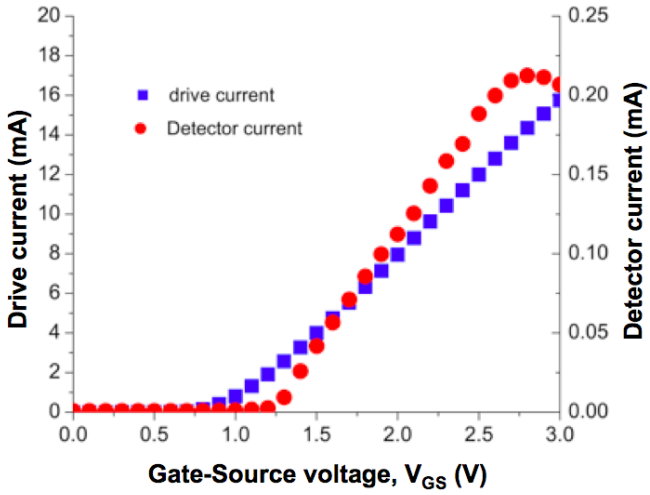
Fully processed and tested oxide-aperture VCSELs emitting at 850 nm have been fabricated as individual "pills" 55 μm in diameter and 8 μm tall with a disk contact on the n-type backside and a ring contact on the p-type, emitting top-side. With a custom micro-pipette vacuum pick-up tool, these pills are placed on contact pads at the bottom of recesses etched though the dielectric over coating on a Si-CMOS chip, and when all the recesses on the chip are filled the pills are batch-solder-bonded in place. Back-end processing of the chip then continues with surface planarization, contact via formation, and interconnect metal deposition and patterning. A completely integrated pill appears in Figure 1.

The integrated VCSEL characteristics appear in Figure 2. They have threshold currents of 1 to 2.5 mA and thermal impedances as low as 1.6 °C per mW, both of which are similar to native substrate device thresholds and impedances. Thermal modeling of these devices has also been preformed, investigating the impact of integration on VCSEL device operation. The results show potential thermal impedance improvements for both single and arrayed devices due to integration on silicon. This model also investigates the impact of integration on a dielectric stack, as well as the impact of the current aperture of the VCSEL device.

The technique demonstrated in this work integrates devices as individual pills within the dielectric stack covering a Si IC, allowing for wafer-scale monolithic processing of heterogeneous circuits. The process effectively avoids thermal expansion mismatch limitations, and it is compatible with parallel assembly techniques, such as fluidic self-assembly.



▲ Figure 1: A microphotograph of a fully integrated VCSEL in its recess on a CMOS chip showing the upper contact pattern connecting the VSCEL to the underlying circuitry. The emission comes from the small aperture in the contact pattern roughly in the center of the picture. Figure 2 shows the CW drive and output characteristics of the VCSEL.



▲ Figure 2: The CW drive and output characteristics of an integrated VCSEL driven by an on-chip transistor circuit. The diode current (left axis) and optical output (detector current, right axis) are plotted as a function of the gate-to-source voltage applied to the n-MOS drive transistor. The MOSFET threshold voltage is ~ 1 V, and the VCSEL threshold is ~ 2 mA.

References

[1] J.M. Perkins and C.G. Fonstad, " Full recess integration of small diameter low threshold VCSELs within Si-CMOS ICs," in review.

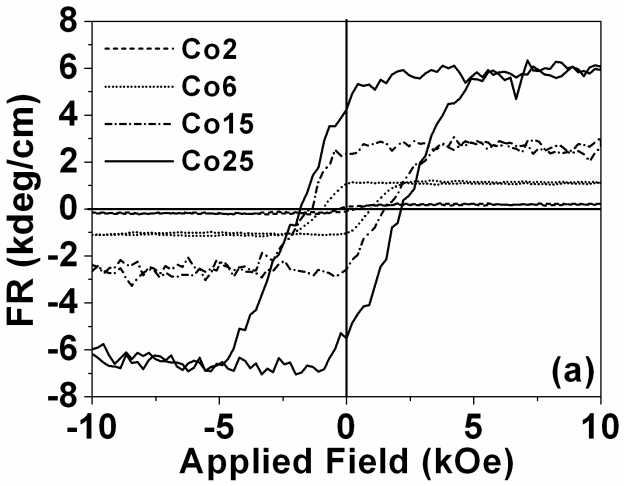
[2] J.M. Perkins, "Low threshold vertical cavity surface emitting lasers integrated onto Si-CMOS ICs using a novel hybrid assembly technique," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2007.

Magnetic Oxides for Optical Isolators and Magnetoelectronic Devices

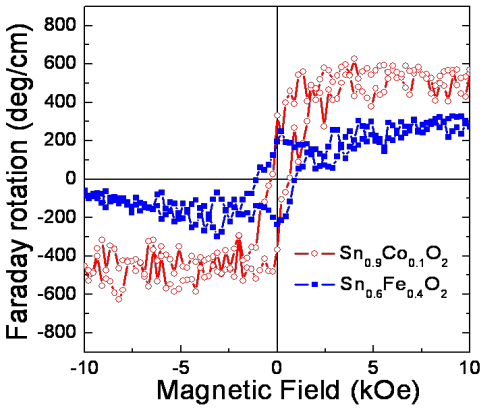
C.A. Ross, G.J. Dionne, A. Taussig, L. Bi, V. Sivakumar, H.S. Kim
Sponsorship: Lincoln Laboratory, ISN, NSF

We have established a thin-film laboratory that includes a pulsed-laser deposition (PLD) system and an ultra-high vacuum sputter/analysis system. In PLD, a high-energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. The PLD is particularly useful for making complex materials such as oxides because it can preserve the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magneto-optical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magneto-optical isolators in conventional photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite), with its high Faraday rotation, grows very well on MgO or Si, but its optical absorption is high. One way to solve this problem is to develop new magneto-optical active materials, which can grow epitaxially on Si by using buffer layers. When doped with transitional metal ions, these materials can exhibit strong Faraday rotation as well as low optical loss. Recently, we have examined Co-doped CeO_2 thin film (Figure 1) [1], which shows strong magneto-optical properties and lower optical absorption compared with iron oxide. The best figure of merit of 0.25 deg/dB, which is defined as Faraday rotation divided by optical absorption loss at 1550-nm wavelength, has been achieved in $Ce_{0.98}Co_{0.02}O_2$. Another investigation was carried out on Co- or Fe-doped SnO_2. As a material used for transparent conductive electrodes, SnO_2 can grow epitaxially on sapphire substrates. When doped with Co or Fe, this material shows Faraday rotation and low optical loss at 1550-nm wavelength. A figure of merit of 0.16 deg/dB is achieved in $Sn_{0.9}Co_{0.1}O_2$ (Figure 2). These films could be useful for waveguide isolators and other magnetoelectronic devices in which optical absorption losses are critical. A second project involves the use of electrochemical methods to control the magnetization of iron oxide spinel structure films (magnetite or maghemite) grown on conducting substrates, making a chemically-switchable material. The insertion of Li ions by electrochemical discharge changes the oxidation state of the Fe(III) to Fe(II) and can reduce the magnetization of the film by about 30%, in a reversible process. Recent experiments on nanoparticles of iron oxide show much greater changes in magnetization, up to ~80%, indicating that the process is kinetically limited. Lithiation of CrO_2 also successfully changes the magnetization, with an initial change of $5\mu_B$ per Li^+ ion insertion.



▲ Figure 1: Faraday rotation at 1550-nm wavelength vs. applied field for cobalt doped CeO_2 films grown on MgO (001) substrates. The Co2, Co6, Co15 and Co25 stand for 2 at%, 6 at%, 15 at%, and 25 at% of Co doping on the Ce sites, respectively.



▲ Figure 2: Faraday rotation of $Sn_{0.9}Co_{0.1}O_2$ and $Sn_{0.6}Fe_{0.4}O_2$ films grown on R-plane sapphire substrates.

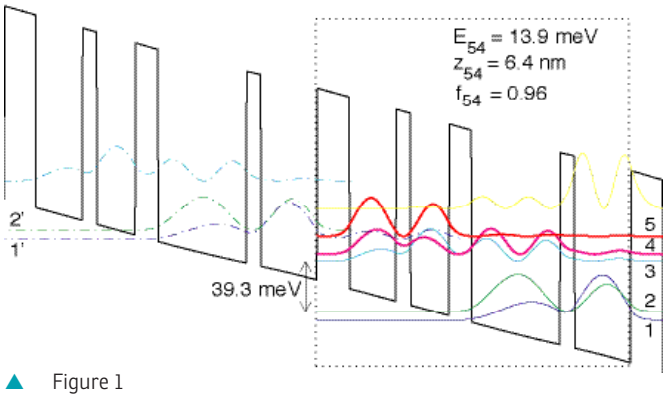
Reference

[1] L. Bi, H.-S. Kim, G.F. Dionne, S.A. Speakman, D. Bono, and C.A. Ross, "Structural, magnetic and magneto-optical properties of Co doped $CeO_{2-\delta}$ films," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07D138:1-3, Mar. 2008.

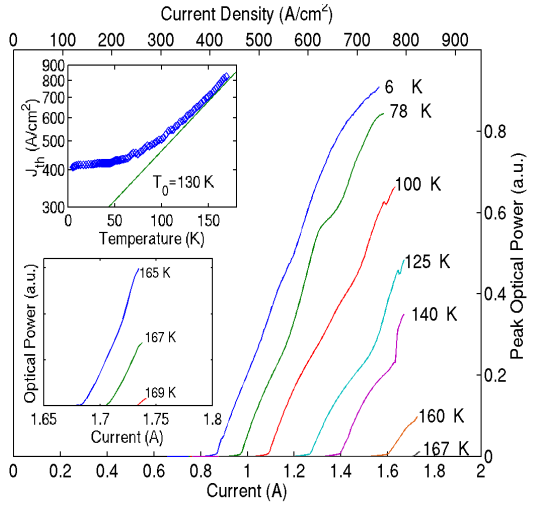
Development of Terahertz Quantum Cascade Lasers

B. Williams, S. Kumar, A. Lee, Q. Qin, W. Kao, Q. Hu (in coll. with J. Reno, Sandia National Laboratories)
Sponsorship: NSF, NASA, AFOSR

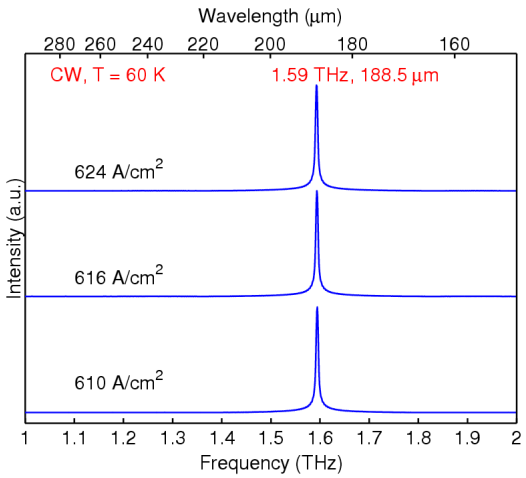
The terahertz frequency range (1-10 THz) has long remained undeveloped, mainly due to the lack of compact, coherent radiation sources. Transitions between sub-bands in semiconductor quantum wells were suggested as a method to generate long wavelength radiation at customizable frequencies. However, because of difficulties in achieving population inversion between narrowly separated sub-bands and mode confinement at long wavelengths, THz lasers based on intersub-band transitions were developed only very recently. We have developed THz quantum-cascade lasers based on resonant-phonon-assisted depopulation and using metal-metal waveguides for mode confinement. The schematics of both features are illustrated in Figure 1a. Based on the combination of these two unique features, we have developed many THz QCLs with record performance, including a maximum pulsed operating temperature at ~170 K (top-right), a maximum power of ~250 mW (bottom-right), and the longest wavelength (~190 μm) QCL to date without the assistance of magnetic fields (bottom-left).



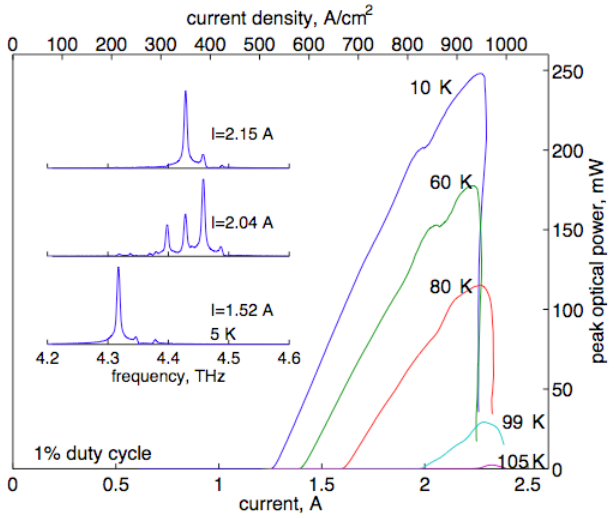
▲ Figure 1



▲ Figure 2



▲ Figure 3

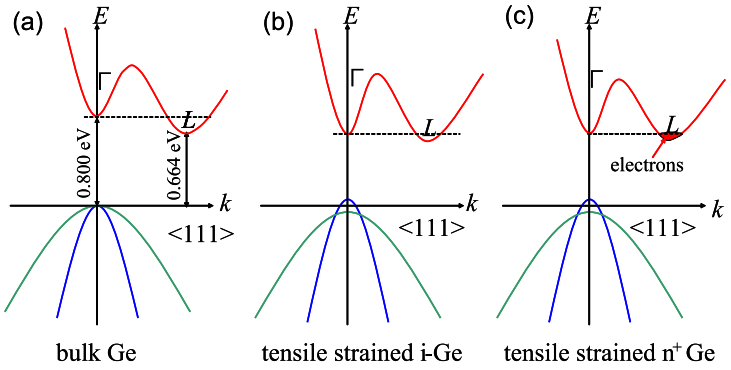


▲ Figure 4

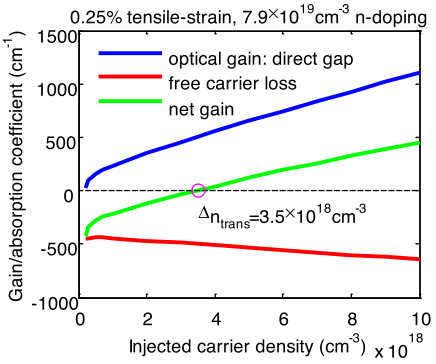
Band-engineered Ge as a Gain Medium for Si-based Laser

X. Sun, J. Liu, L.C. Kimerling, J. Michel
Sponsorship: DARPA

Electronic-photonic Integrated Circuits (EPIC) based on Si microphotonics give a potential solution to solve the "interconnect" bottleneck problem that prevents Si microelectronics from further upgrading its performance by shrinking the dimensions [1]. An Si-based light emitter is one of the most important and challenging components for this EPIC architecture. We proposed and have studied Ge as active gain medium for a Si-based laser. H. Kroemer first discussed the possibility of achieving lasing in indirect band gap materials like germanium [2]. Our recent theoretical analysis has indicated that Ge can be band-engineered to behave like a direct bandgap material by introducing tensile strain and heavy n-type doping [3]. Figure 1 shows this process : 1) applying tensile strain in Ge to decrease the difference between the direct gap and the indirect gap and 2) n-type doping to fill the indirect L valley to make the two gaps electronically equal. Tensile strain gives an additional benefit of separating the light-hole valence band and the heavy-hole valence band at the band edge, as Figure 1 shows. This split facilitates the population inversion due to the lower density of states of the light-hole band, which can be more easily filled with injected holes. Practically, tensile strain can be introduced by the large thermal mismatch between Ge and Si up-cooling from the growth temperature to room temperature [4] and an n-type donor can be incorporated either during the Ge growth or by ion implantation. Detailed calculations have shown that this band-engineered Ge can provide optical gain at carrier injection levels comparable to III-V materials [3]. For example, the modeling shows that with a combination of 0.25% tensile strain and an extrinsic electron density of 7.6×10^{19} /cm^3 from n-type doping, a net material gain of ~400 cm^{-1} can be obtained from the direct bandgap transition of Ge despite the free carrier absorption loss. Photoluminescence (PL) measurement has been performed on band-engineered Ge thin films epitaxially grown on Si. Direct bandgap PL at around 1550 nm has been observed and the intensity is over 50 times larger than that of intrinsic Ge films on Si. The increase of the PL intensity with n-type doping confirms our theoretical predictions. The results indicate that such band-engineered Ge is a good candidate for a monolithically integrated Si-based laser.



▲ Figure 1: Schematic band structure of bulk Ge shows a 136-meV difference between the direct gap and the indirect gap. This difference can be decreased by introducing tensile strain (0.25%), and the rest can be further compensated by filling electrons from n-type dopants (7.6×10^{19}/cm^3) into the L valley so that finally makes the two gaps electrically equal. [1]



▲ Figure 2: Gain coefficient at 1560 nm was calculated for the same material at different excess carrier injection levels. Free carrier absorption, which dominates the material loss, was also calculated. The difference between gain and loss shows that the positive net gain is achieved above the transparency carrier density of 3.5×10^{18}/cm3, which is highlighted [1].

References

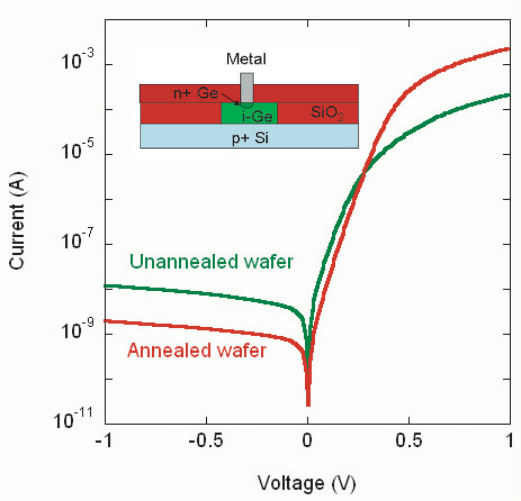
[1] L. Pavesi and D.J. Lockwood, *Si Photonics*. New York, NY: Springer, 2003.
[2] H. Kroemer, "A proposed class of heterojunction injection lasers," *Proc. of the IEEE*, vol. 51, no. 12, Dec. 1963, pp. 1782-1783.
[3] J. Liu, X. Sun, D. Pan, X.Wang, L.C. Kimerling, T L. Koch, and J. Michel, "Tensile-strained, n-type Ge as a gain medium for monolithic laser integration on Si," *Optical Express*, vol. 15, no. 18, pp. 11272-11277, Sept. 2007.
[4] D.D. Cannon, J. Liu, Y. Ishikawa, K. Wada, D.T. Danielson, S. Jongthammanurak, J. Michel, and L.C. Kimerling, "Tensile strained epitaxial Ge films on Si(100) substrates with potential application in L-band telecommunications," *Applied Physics Letters*, vol. 84, no. 6, pp. 906-908, 2004.

Electrical and Optical Characteristics of Selectively Grown Ge-on-Si Photodiodes

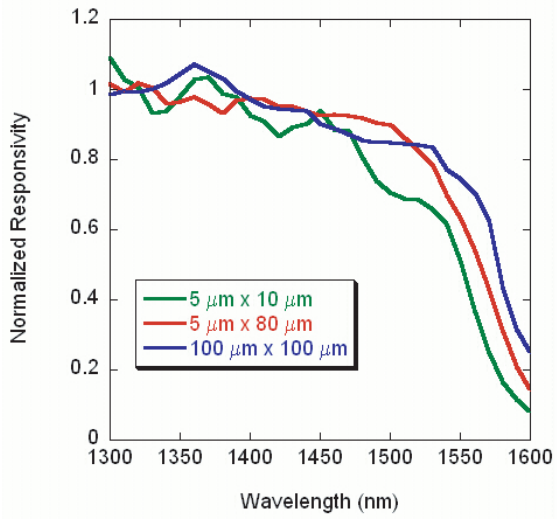
N. DiLello, J. Yoon, J.S. Orcutt, M. Kim, J.L. Hoyt
Sponsorship: DARPA, SRC student fellowship

Germanium is a promising candidate for use in CMOS-compatible photodiodes. Its strong absorption in the 1.55-μm range and relative ease of integration on silicon substrates make it suitable for telecommunications systems as well as in other high-speed electronic photonic integrated circuits. Important figures of merit in these photodiodes are the reverse leakage current and the responsivity. To reduce power consumption and improve the signal-to-noise ratio, it is important that the diodes have a low leakage current in reverse bias and a high responsivity, both typically quoted at -1 V. This study has investigated the leakage current of germanium photodiodes selectively grown by low-pressure chemical vapor deposition (LPCVD) using an Applied Materials epitaxial reactor.

To fabricate these diodes, 1 μm of germanium was grown by selective epitaxy on oxide-patterned *p+* Si wafers. Some wafers received an in-situ cyclic anneal to reduce the dislocation density, while others were unannealed. The wafers were then implanted with phosphorus to create a vertical *pin* junction and contacted with metal. Figure 1 shows a schematic diagram of the device cross-section (inset) and measured current vs. voltage characteristics for both the annealed and the unannealed wafers. The cyclic anneal reduces the leakage current at -1 V by a factor of approximately 5, on the lowest leakage diodes; however, the cyclic anneal also results in a larger distribution of the dark current. Figure 2 shows the photoresponse for various sizes of diodes from the annealed wafer with an applied bias of -1 V. The absorption edge shifts to longer wavelengths for larger devices, suggesting a smaller bandgap (shrinkage of ~25 meV) in the larger Ge areas, resulting from the induced strain in the film [1]. This behavior in the responsivity is consistent with Raman analysis, which shows higher strain in the larger-area devices.



▲ Figure 1: Current vs. voltage characteristics for 5 x 10 μm rectangular diodes. The cyclic anneal reduces the leakage current by ~5x for the best performing diodes. There is a large variation in dark current for devices on the annealed wafer. The inset shows a cross-sectional schematic of the device.



▲ Figure 2: Normalized responsivity vs. wavelength for various sizes of rectangular diodes. The photoresponse was normalized to an average of values taken in the 1300–1350-nm range. The absorption edge shifts to longer wavelengths for larger devices, corresponding to a smaller bandgap. This smaller bandgap is consistent with larger strain in the larger area devices.

Reference

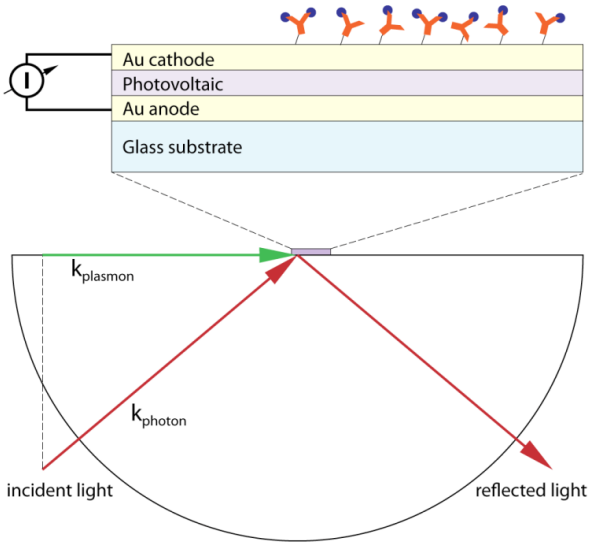
[1] Y. Ishikawa, K. Wada, D.D. Cannon, J. Liu, H-C. Luan, and L.C. Kimerling, "Strain-induced band gap shrinkage in Ge grown on Si substrate," *Applied Physics Letters*, vol. 82, no. 13, pp. 2044-2046, Mar. 2003.

Excitonic Surface Plasmon Resonance Biosensor

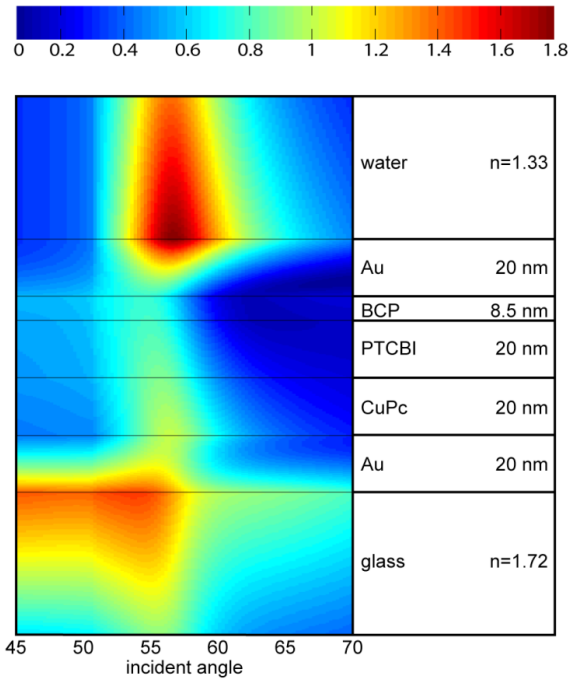
M. Bora, K. Celebi, M.A. Baldo
Sponsorship: ISN

The main disadvantages of surface plasmon resonance (SPR) biosensors are their high cost and lack of portability. We propose to solve these deficiencies by integrating a plasmon source and detector with microfluidic components for a compact, inexpensive instrument. Surface plasmons are electromagnetic waves that propagate along a metal dielectric interface. The SPR biosensors exploit the sensitivity of surface plasmons to changes in the dielectric constant immediately adjacent to a metal surface. The angular reflectivity of the metal film has a sharp plasmon resonance feature that shifts when higher dielectric constant biomolecules bind to the surface. The high sensitivity of the SPR is complemented by real-time, label-free detection that provides additional information on the chemical kinetics of the interaction.

Here, we propose a novel surface plasmon biosensor that uses a plasmonic mode bound to the anode and cathode of a thin-film organic photovoltaic (PV). The sensor design combines the sensitivity of SPR with a novel plasmon conversion mechanism in the thin-film organic PV. The plasmon resonance is detected directly in the near field by coupling the electric field of the plasmon modes with exciton formation within the adjacent PV cell. The splitting of excitons into holes and electrons at the organic heterojunction interface of the PV cell generates a short circuit photocurrent modulated by the plasmon resonance condition set by the electric properties of the thin-film structure and the adjacent medium. Measurements of reflected power and photocurrent have a strong dependence on incident light angle, similar to the typical plasmon resonance curve. Agreement between this data and numerical simulations proves the existence of plasmon modes bound to the metal layers. The photocurrent generated by plasmon absorption in the photovoltaic is considerably larger than the optical absorption background. For sensing purposes, the photocurrent measured in our devices and reflectivity measured in standard SPR instrumentation are interchangeable and yield comparable sensitivity upon binding of biological species on the surface. We expect that this approach may replace large benchtop SPR sensors by sub-1-mm² devices compatible with array-processing of biological samples.



▲ Figure 1: Device structure and experimental setup. The P-polarized light falls on the photovoltaic structure at an angle controlled by the rotation of a hemi-cylindrical prism. Reflected power and current generated between the gold anode and cathode are monitored with respect to either incident angle or time for binding events on the top gold surface.



▲ Figure 2: Relative amplitude of the electric field for the transverse magnetic mode. Numerical simulations highlight the existence of a bound mode spanning the whole device structure. Plasmon excitations have the highest amplitude on the top surface of the cathode layer and extend in the organic layers of the photovoltaic.

Reference

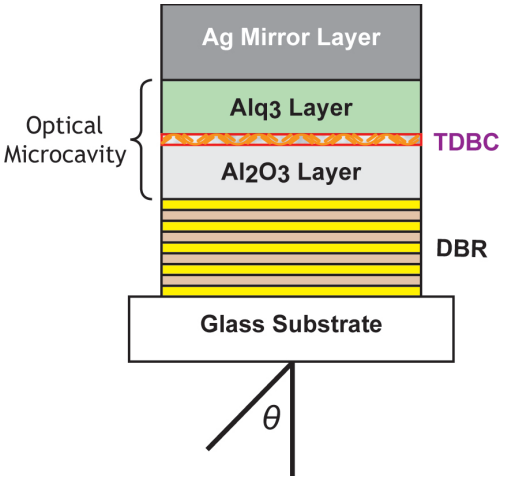
[1] J.K. Mapel, K. Celebi, M. Singh, and M.A. Baldo, "Plasmonic excitation of organic double heterostructure solar cells," *Applied Physics Letters*, vol. 90, no. 12, pp. 121102:1-3, Mar. 2007.

Exciton-polaritons at Room Temperature in Metal-dielectric Microcavities

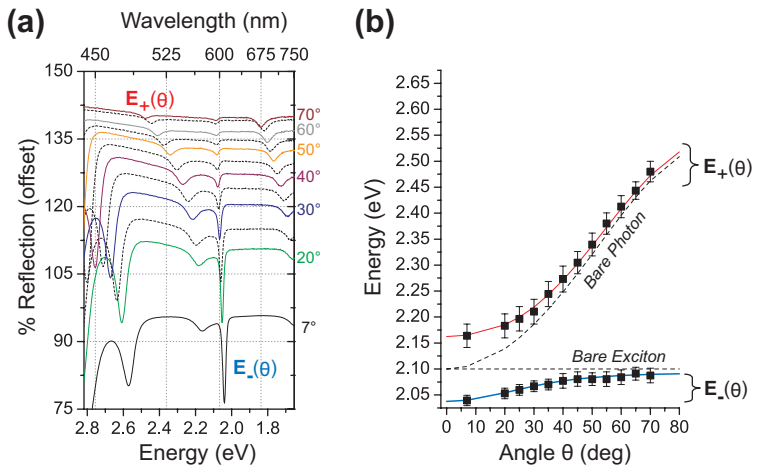
J.R. Tischler, M.S. Bradley, Y. Shirasaki, V. Bulović

Sponsorship: DARPA, NDSEG, MIT NSF MRSEC

Exciton-polariton-based photonic devices are a novel platform for realizing low-threshold lasing [1] and optical switching [2] in a scalable integrated architecture. Use of organic materials such as the excitonic component facilitates room-temperature operation of such devices [3]. Here we report room-temperature exciton-polariton devices consisting of layer-by-layer (LBL) assembled thin films of polyelectrolyte and the J-aggregates of the cyanine dye TDBC inserted in a resonantly-tuned planar $\lambda/2n$ optical microcavity with metal mirror and dielectric Bragg reflector (DBR). The device exhibits Rabi-splitting of $\Omega_R = 125 \pm 7$ meV with a polyelectrolyte/J-aggregate layer that is only 5.1 ± 0.5 nm thick [4]. Furthermore, the linewidth of the lower energy polariton state, measured on resonance, is $\Gamma = 12.1$ meV. The ratio $\Omega_R/2\Gamma = 5.1$ indicates that the device operates in a limit where the light-matter coupling (Ω_R) significantly exceeds competing dephasing processes (Γ). These figures of merit are achieved by virtue of the nanostructured film's large absorption coefficient of $\alpha \sim 1.0 \times 10^6$ cm^{-1} and by location of the 5.1 ± 0.5-nm-thick layer at the microcavity anti-node. Rabi-splitting and polaritonic dispersion are observed in the reflectance, transmittance, and photoluminescence measurements of the device. Because strong coupling is achieved with such thin films, the majority of the microcavity modal volume is available for integrating a variety of optically active materials, such as colloidal quantum dots and fluorescent polymers, into devices that could leverage the coherent properties of the strongly coupled states. Moreover, the LBL process provides nanometer-scale thickness control of ~1.7 nm per polymer/dye bilayer, suggesting that this device can be used to investigate fundamental physical phenomena such as non-radiative energy transfer and laser action in the strong coupling limit.



▲ Figure 1: Device design of polaritonic structure. Microcavity consists of a DBR and a silver mirror layer. On top of the J-aggregate layer, a film of small molecule Alq3 is thermally evaporated.



▲ Figure 2: (a) Angularly resolved reflectance measurements and (b) dispersion relation for resonantly tuned polaritonic structure. The microcavity is resonantly tuned at normal (at $\theta = 0°$) to the exciton resonance of 2.10 eV. The $E_-(\theta)$ denotes the lower energy polariton states; $E_+(\theta)$, the higher energy polariton states. Reflectance is measured with TE polarized incident light. Measurements from $\theta = 20°$ to 70° are relative values. Data at $\theta = 7°$ is absolute reflectance.

References

[1] S. Christopoulos, G.B. von Hogersthal, A.J. Grundy, P. Lagoudakis, A.V. Kavokin, J.J. Baumberg, G. Christmann, R. Butte, E. Feltin, J.F. Carlin, and N. Grandjean, "Room-temperature polariton lasing in semiconductor microcavities," *Physical Review Letters*, vol. 98, pp. 126405:1-4, Mar. 2007.

[2] N.A. Gippius, I.A. Shelykh, D.D. Solnyshkov, S.S. Gavrilov, Y.G. Rubo, A.V. Kavokin, S.G. Tikhodeev, and G. Malpuech, "Polarization multistability of cavity polaritons," *Physical Review Letters*, vol. 98, pp. 236401:1-4, June 2007.

[3] D.G. Lidzey, D.D.C. Bradley, M.S. Skolnick, T. Virgili, S. Walker, and D.M. Whittaker, "Strong exciton-photon coupling in an organic semiconductor microcavity," *Nature*, vol. 395, no. 6697, pp. 53-55, Sept. 1998.

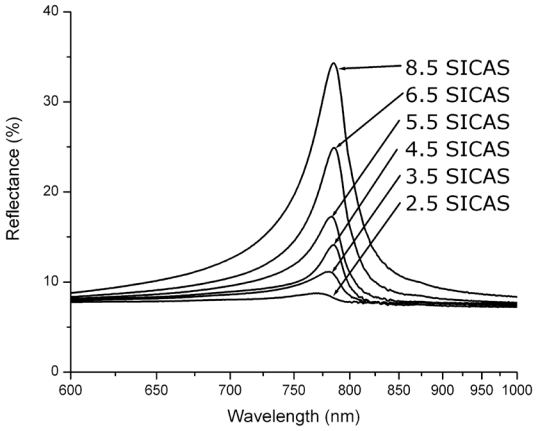
[4] M.S. Bradley, J.R. Tischler, and V. Bulović, "Layer-by-layer J-aggregate thin films with a peak absorption constant of 10^6 cm^{-1}," *Advanced Materials*, vol. 17, no. 15, pp. 1881-1886, Aug. 2005.

Near-infrared J-aggregates for Exciton-polariton Optoelectronics

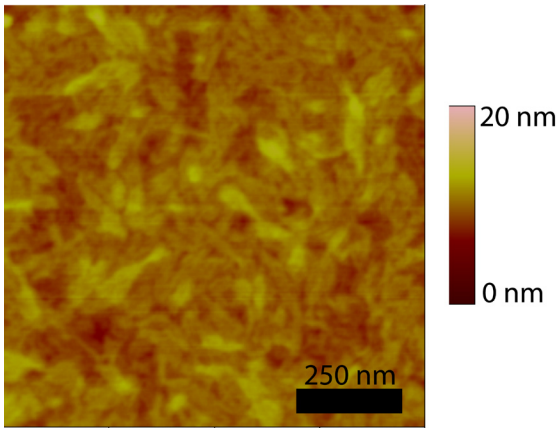
M.S. Bradley, J.R. Tischler, Y. Shirasaki, V. Bulović
Sponsorship: ISN, NDSEG, MIT NSF MRSEC

Thin films of J-aggregates of cyanine dyes, which found wide use in the 20th century in the photographic film industry, exhibit narrow linewidth and large oscillator strength, enabling their use in the first room-temperature solid-state electroluminescent devices that exhibit the strong-coupling regime of Cavity Quantum Electrodynamics (Cavity QED) [1]. As we demonstrated in a recent study, layer-by-layer (LBL)-assembled J-aggregate thin films can be precisely deposited in a specific location in a microcavity and contain a high density of aggregates, contributing to the observation of a peak thin-film absorption coefficient of 1.05 ± 0.1 x 10^6 cm^{-1}, among the highest ever measured for a neat thin film [2]. A recent study utilizing J-aggregates with exciton resonance in the near-infrared (NIR) spectral region demonstrated devices exhibiting strong coupling [3]. However, the J-aggregate films used were deposited by spin-coating, which results in nhomogeneous, thick films. In this work, we utilize the LBL deposition method to deposit thin films of these NIR J-aggregates, showing the same nanoscale thickness control and large peak thin-film absorption constant as observed in our previous studies for J-aggregates in the visible spectral region.

For deposition of thin films of NIR J-aggregates, substrates undergo sequential immersions in cationic and anionic solutions (SICAS). The cationic solution contains the very-low-molecular-weight polyelectrolyte PDAC (poly(dimethyldiallylammonium chloride)), and the anionic solution consists of the J-aggregating dye U3 (3-[(2Z)-5-chloro-2-[((3E)-3-{[5-chloro-3-(3-triethylammonium-sulfonatopropyl)-1, 3-benzothiazol-3-ium-2-yl]methylene}-2,5,5-trimethylcyclohex-1-en-1-yl) methylene]-1,3-benzqothiazol- 3(2H)-yl] propane-1-sulfonate). Figure 1 shows the reflectivity for films on glass substrates that underwent various numbers of SICAS, showing the NIR J-aggregate peak around λ=790 nm, as observed in [3] for spin-coated films. Figure 2 shows an atomic force microscopy (AFM) image of the 6.5 SICAS film, which demonstrates the remarkably-low (XYZ nm) roughness of films produced using this technique, which will allow for incorporation of these films into optical microcavities without contributing to significant inhomogeneous broadening of the cavity resonance, as needed for development of strongly-coupled Cavity QED devices.



▲ Figure 1: Reflectance of thin films of NIR J-aggregates deposited on glass substrates using the LBL deposition method.



▲ Figure 2: AFM image of the 6.5 SICAS film from Figure 1. The low roughness allows incorporation of these films into microcavities without significantly increasing the nhomogeneous linewidth of the cavity resonance.

References

[1] J.R. Tischler, M.S. Bradley, V. Bulović, J.H. Song, and A. Nurmikko, "Strong coupling in a microcavity LED," *Physics Review Letters*, vol. 95, no. 3, pp. 036401-036404, 2005.

[2] M.S. Bradley, J.R. Tischler, and V. Bulović, "Layer-by-layer J-aggregate thin films with a peak absorption constant of 10^6 cm^{-1}," *Advanced Materials*, vol. 17, no. 15, pp. 1881-1886, 2005.

[3] J. Wenus, S. Ceccarelli, D.G. Lidzey, A.I. Tolmachev, J.L. Slominskii, and J.L. Bricks, "Optical strong coupling in microcavities containing J-aggregates absorbing in near-infrared spectral range," *Organic Electronics*, vol. 8, pp. 120-126, 2007.

Materials for Electro-optic Modulation and Switching

J. Hiltunen, D. Seneviratne, H.L. Tuller (in coll. with J. Yasaitis)
Sponsorship: Analog Devices, MIT Microphotonics Center

The drive towards integrated photonics requires the integration of various optical devices on a chip, including an optical modulator. Currently optical modulation with active waveguiding structures is implemented using $LiNbO_3$ single crystals. These devices require complex and expensive fabrication processes. In addition, their relatively low electro-optic coefficient leads to large component sizes, limiting miniaturization. The current demands for an increased degree of integration with cost-efficient device fabrication can be achieved using thin films of barium titanate.

The focus is on optimizing the electro-optic response of $BaTiO_3$ and related thin-film materials deposited by pulsed laser deposition (PLD) and sputtering onto single-crystal substrates directly or with buffer layers. A waveguide Mach-Zehnder interferometer structure, using a SiN strip-loaded waveguide, was prepared. We have demonstrated an effective electro-optic coefficient of 85pm/V, considerably greater than those available with bulk $LiNbO_3$ crystals. More recently $BaTiO_3$ (BTO) – $SrTiO_3$ (STO) multilayer thin-films of ~370-nm total thickness and varying stacking periodicity between 27 and 1670 Å were grown on single crystal MgO (001) substrates by PLD. The X-ray diffraction measurements confirmed the formation of BTO-STO super-lattices with a highly strained out-of-plane lattice parameter in the BTO layers due to interface-induced stress. Lattice strain relaxed with increasing layer thickness, resulting in reduced optical birefringence. The electro-optic response reached a maximum in films with stacking periodicity of 105 Å.

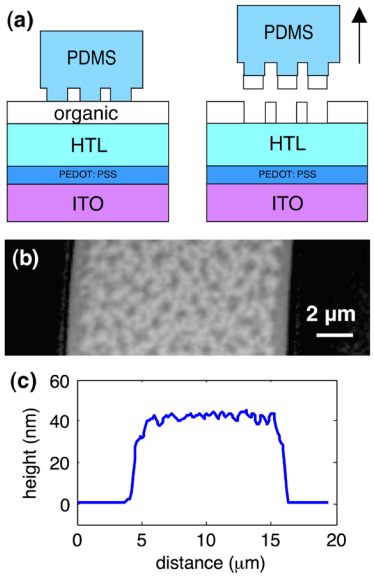
Micro-patterning Organic Thin Films via Contact Stamp Lift-off for Organic Light-emitting Device Arrays

J. Yu, V. Bulović

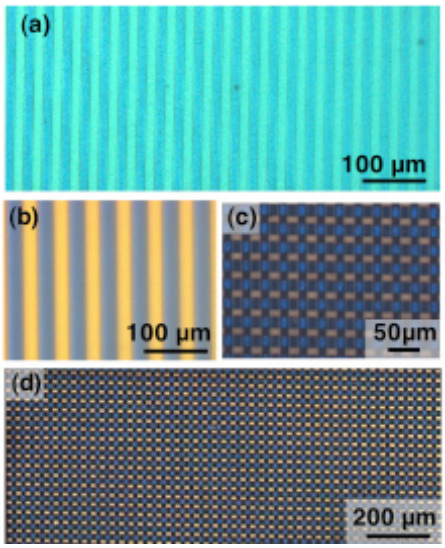
Sponsor: CMSE, PECASE

Patterning of organics in electronic devices is done primarily by techniques that are limited in resolution or scalability or are potentially damaging to the organic material. We demonstrate a simple subtractive stamping technique for patterning micron-sized features on organic thin films of nanometer-range thickness. Patterning is achieved by placing a relief-patterned polydimethylsiloxane (PDMS) stamp in contact with an organic film and peeling off the stamp (Figure 1a). The procedure is done without applied pressure or heat and can be done in an ambient environment, although a nitrogen environment is preferred for organic light-emitting device (OLED) fabrication. This technique is applied to pattern 13 micron-sized features of a two-color OLED structure.

To fabricate a two-colored OLED, a hole-blocking or emissive layer is patterned using this technique. The in-plane roughness of the patterned feature is shown in the height image of a patterned stripe (Figure 1b) and a profile of the patterned feature is shown (Figure 1c). Electroluminescence (EL) from blue-green device with 13-micron-sized features is shown (Figure 2a), and EL from blue-red devices of 25-micron-sized features is shown (Figure 2b). This technique can be applied twice to pattern blue-red devices with finer features (Figure 2c, d).



▲ Figure 1: (a) Demonstration of the subtractive stamping technique. Placing PDMS stamp to the substrate and subsequent release lifts off organic thin film from substrate surface. (b) Top view of in-plane patterned 20-nm TAZ on 50-nm TPD / PEDOT:PSS / ITO / glass substrate from AFM. (c) AFM height data to view lift-off patterned region.



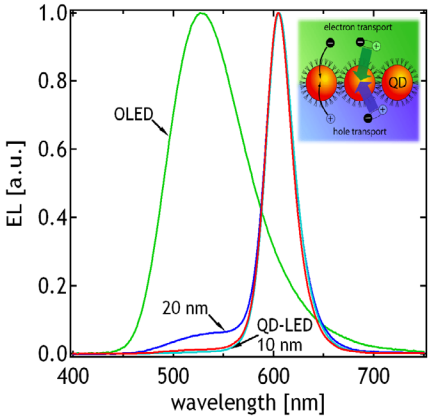
▲ Figure 2: (a) EL of green-blue OLED from patterned hole-blocking layer for AlQ_3 (green) or TPD (blue) emission. (b) EL of red-blue OLED from a patterned emissive layer DCM_2:AlQ_3 (red) or TPD (blue) emission and EL from red-blue patterned OLED by stamping twice to define finer features in (c) with a zoomed-out version (d).

Modeling of Electronic and Excitonic Processes in Quantum Dot LEDs

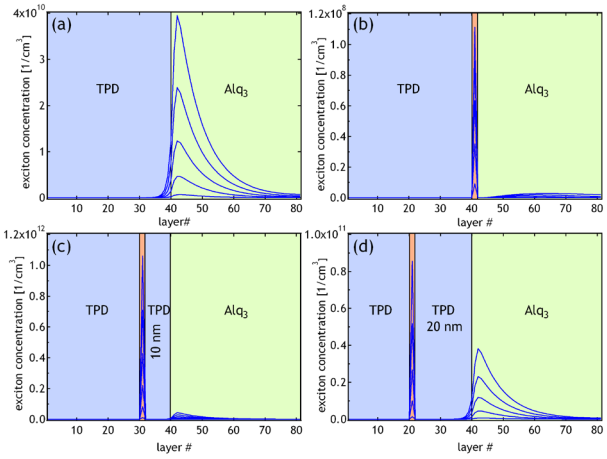
P.O. Anikeeva, C.F. Madigan, J.E. Halpert, M.G. Bawendi, V. Bulović
Sponsorship: ISN, MIT NSF MRSEC, PECASE

Hybrid light-emitting devices (LEDs), consisting of organic charge transporting layers and colloidal quantum-dot (QD) emissive layers [1], exhibit narrow electroluminescence (EL) spectra, characteristic of colloidal QD luminescence. The manifested saturated color emission is particularly desirable in flat-panel display applications and is broadly applicable to other technologies requiring high spectral quality lighting. The development of novel QD deposition techniques such as microcontact printing [2] allowed us to experimentally investigate the mechanisms of QD-LED operation by varying the position of the emitting QD monolayer within the stacked organic structure. We find that imbedding the emissive QD monolayer into the hole-transporting layer <10 nm away from the interface between hole and electron-transporting layers, improves the quantum efficiency of the device by >50%, while maintaining QD-LED spectral purity (Figure 1). These findings and additional experiments led us to the conclusion that maximizing exciton generation on organic molecules and subsequent energy transfer to QDs, while minimizing QD charging with electrons, improves QD-LED performance.

In order to verify our conclusions based on the previous experimental observations, we built a theoretical model for charge and exciton transport in organic LEDs (OLEDs) and QD-LEDs. Considering carrier drift and diffusion, we numerically simulate carrier concentration and electric field profiles in device structures; based on them, we calculate exciton concentration profiles (Figure 2). We find that the results of our model are in qualitative agreement with experimental data. We find that exciton diffusion and non-radiative energy transfer from organic thin films to QDs lead to maximum exciton concentration on QD sites, resulting in QD-LED spectra dominated by QD emission. We find that imbedding QDs into the TPD hole-transporting layer reduces electron concentration at QD sites and consequently eliminates QD luminescence quenching. It also reduces the electric field across the QDs, eliminating exciton dissociation.



▲ Figure 1: Normalized EL spectra of OLED, QD-LEDs with QDs at the TPD/Alq_3 interface, QDs imbedded into TPD 10 nm and 20 nm below the interface. Inset: Schematic diagram of the charge injection and energy transfer from organic charge transporting layers to a monolayer of colloidal QDs.



▲ Figure 2: Exciton concentration profiles obtained from numerical simulations. (a) OLED, (b) QD-LED with QDs at the TPD/Alq3 interface, (c) and (d) QDs imbedded into TPD 10 nm and 20 nm away from the interface. Theoretical exciton profiles are in qualitative agreement with experimental EL spectra shown in Figure 1.

References

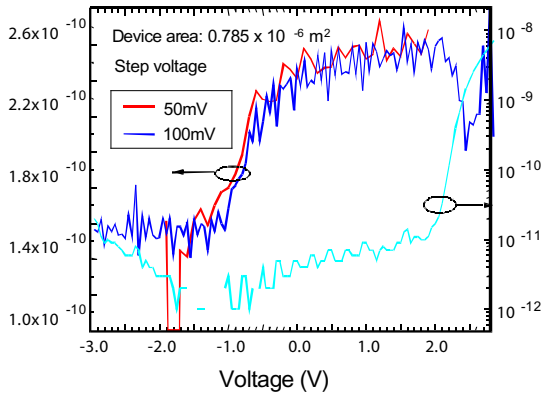
[1] S.A. Coe-Sullivan, "Hybrid organic/quantum dot thin film structures and devices," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2005.
[2] L. Kim, "Deposition of colloidal quantum dots by microcontact printing for LED display technology," M.Eng. thesis, Massachusetts Institute of Technology, Cambridge, 2006.

Cathode Metal Diffusion and Doping in Organic Light-emitting Devices

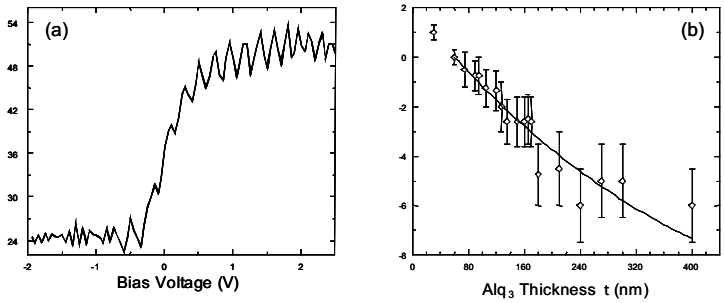
P. Jadhav, B. Limketkai, M. Baldo
Sponsorship: DuPont-MIT alliance

Organic semiconductors employed in organic light-emitting devices (OLEDs) are typically assumed to be intrinsic. There are suggestions, however, that organic semiconductors may actually be doped within OLEDs [1]. It is important to resolve the origin of the apparent doping phenomenon because: (i) doping apparently determines the operating voltage and quantum efficiency, and (ii) compositional control is a prerequisite for the rational design of stable OLEDs. Indeed, one notable characteristic – the retained negative charge in tris(8-hydroxyquinoline) aluminum (AlQ_3)-based OLEDs -- has been directly correlated to degradation [1]. The retained charge undergoes a transition from negative to positive that is linearly related to the loss of luminance.

We demonstrate that one significant origin of impurities is cathode metal diffusion. Cathode materials diffuse into the bulk of the AlQ_3, introducing free charges if the cathode material reacts with neighboring AlQ_3 molecules. In addition, the presence of reactive cathode materials stabilizes electrons on other nearby AlQ_3 molecules, forming electron traps. Thus, the diffusion of cathode species is associated with both free charge and traps in AlQ_3. We probe charge stored in electron traps using capacitance-voltage[2]. In bilayer OLEDs consisting of AlQ_3 and a hole transport layer (HTL), holes are confined at the AlQ_3/HTL interface. Thus, the capacitance is determined by the thickness of the AlQ_3. Under reverse bias, the holes are extracted and the capacitance is determined by the thickness of the entire OLED (Figure 1). In the absence of stored charge, the transition in the observed capacitance should occur at the built-in potential, V_{BI}. But we observe transitions at more negative potentials, confirming the presence of fixed negative charge. The negative charge density calculated from these measurements decreases with cathode distance from the interface (Figure 2) and exhibits a clear dependence on the cathode material, confirming that the cathode is the origin of the fixed charge.



▲ Figure 1: Quasi-static capacitance-voltage measurement for a hetero-layer AlQ_3/HTL device. As the biasing voltage is reduced from forward to reverse bias, the capacitance changes from C_{AlQ3} to that of the series sum of C_{AlQ3} and C_{HTL}. This transition would be expected to occur at $V = V_{BI}$, which is the difference in work functions of the two electrodes. Instead, it occurs at a voltage further into reverse bias, revealing the existence of trapped negative charge in the AlQ_3 layer.



▲ Figure 2: The thickness dependence of the capacitive transition voltage. It is fit by a model assuming that the fixed charge density decreases exponentially with distance from the cathode.

References

[1] D.Y. Kondakov, W.C. Lenhart, and W.F. Nichols, "Operational degradation of organic light-emitting diodes: Mechanism and identification of chemical products," *Journal of Applied Physics*, vol. 101, no. 2, p. 24512, Jan. 2007.

[2] S. Berleb, W. Brutting, and G. Paasch, "Interfacial charges in organic hetero-layer light emitting diodes probed by capacitance-voltage measurements," *Synthetic Metals*, vol. 122, no. 1, pp. 37-39, May 2001.

The Density of States in Thin-Film Copper Phthalocyanine (CuPC) as Measured by Alternating Current Kelvin Probe Force Microscopy (AC-KPFM)

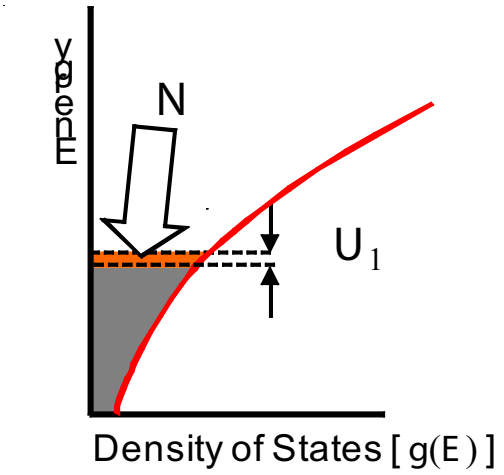
K. Celebi, K. Milaninia, P. Jadhav, M.A. Baldo

Sponsorship: DuPont-MIT alliance

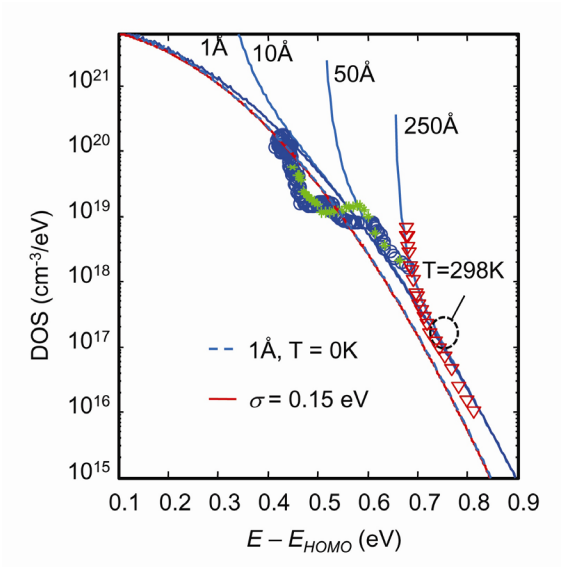
The rational design of organic electronic devices is presently complicated by our inability to directly measure the energetic disorder in the semiconductor. Consequently, many studies have sought to obtain the density of states (DOS) in organic semiconductors. Unfortunately, existing techniques such as ultraviolet photoelectron spectroscopy or thermally stimulated luminescence either lack sufficient resolution or require complicated models for interpretation. The KPFM technique can measure DOS at a resolution of at least 1:1000. We improve upon the original KPFM technique of Tal *et al.* [1] and investigate its limitations. We employ alternating current (AC-KPFM) to reduce noise, and we minimize hysteresis due to charge trapping at the semiconductor/insulator interface. Finally, we model space charge phenomena that distort the data and we demonstrate that the AC-KPFM technique is applicable beyond the low inversion density regime analyzed by Tal *et al.*

Kelvin probe force microscopy (KPFM) employs a scanning probe to measure the local surface potential difference between the probe tip and a substrate. We perform the measurements on CuPC (hole transporter) organic thin-film transistors (OTFT). The source and drain are grounded to maintain equilibrium and a constant Fermi level in the channel. Then, the gate voltage is modulated, shifting the energy levels in the semiconductor. If the DOS at the Fermi level changes, the charge density in the channel must also change. Measurements of the surface potential detect this charging and in turn detect the DOS.

Devices were made with and without octadecyltrichlorosilane (OTS) passivation of the oxide surface. Consistent with previous observations, the magnitude of the threshold voltage was significantly reduced by OTS passivation. The OTS treatment also substantially reduces hysteresis, suggesting that passivation of the oxide surface reduces the trap density at the SiO_2-CuPC interface.



▲ Figure 1: Changes in the charge density in the channel change the surface potential *U* by an amount determined by the density of states.



▲ Figure 2: The density of states calculated from AC and/or DC measurements on OTFTs of various thicknesses. The sharp increase in the DOS is due to the screening effect of accumulated charge. The solid lines are the result of simulations for a Gaussian density of states for films of the thicknesses shown.

Reference

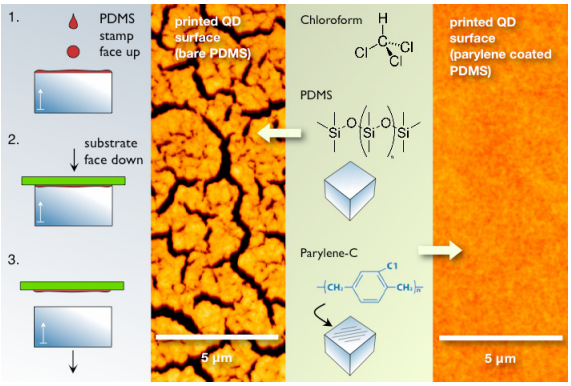
[1] O. Tal, Y. Rosenwaks, Y. Preezant, N. Tessler, C.K. Chan, and A. Kahn, "Direct determination of the hole density of states inundoped and doped amorphous organic films with high lateral resolution," *Physical Review Letters*, vol. 95, no. 25, pp. 256405, Dec. 2005..

Heterojunction Photovoltaics Using Printed Colloidal Quantum Dots as the Photosensitive Layer

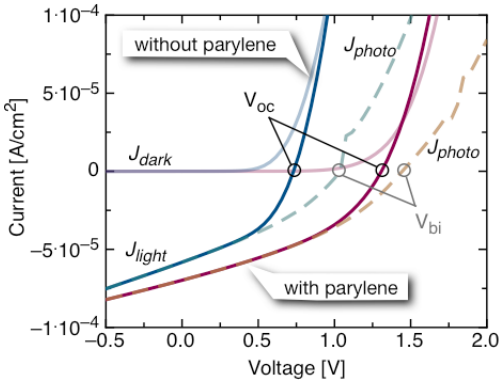
A.C. Arango, D.C. Oertel, M.G. Bawendi, V. Bulović
Sponsorship: ISN

Colloidal quantum dot (QD) systems offer distinct optical and electronic properties that are not easily attained by other nanostructured semiconductors, such as highly saturated emission in QD light-emitting-diodes, access to infrared radiation in QD photodetectors, and the prospect of optically optimized solar cell structures [1]. The prevailing deposition method for colloidal QD systems is spin casting, which introduces limitations such as solvent incompatibility with underlying films and the inability to pattern side-by-side pixels for multispectral photodetector arrays. In the present work we employ a non-destructive microcontact printing method, which allows for deposition of a thin quantum dot films onto a wide-band-gap organic hole transport layer, N,N'-Bis (3-methylphenyl)-N,N'-bis-(phenyl)-9,9-spiro-bifluorene (spiro-TPD), thus producing an inorganic/organic heterojunction that serves to enhance charge separation in the device. The top and bottom contacts are provided by ITO electrodes, allowing for near-transparency.

The performance of nanostructured devices is often critically dependent on the morphology of the constituent films in the device. Deposition of thin QD films from solution can result in rough and incomplete layers if the surface energy of the solvent is not well matched with the surface energy of the substrate. For instance, the low surface energy of a polydimethylsiloxane (PDMS) printing stamp must be modified to match the higher surface energy of the QD solvent in order to print smooth and complete QD films. When a layer of parylene-C is deposited on the PDMS stamp, a smooth and complete QD film can be printed, unlike the process in which a film is printed from a bare PDMS stamp (Figure 1). The device with a smooth and complete film yields superior performance, achieving a built-in potential (Vbi) of 1.46V for a QD band gap of 1.97eV (Figure 2). The Vbi is 74% of the band gap, one of the highest values achieved for photovoltaics of any kind. The present focus is on improving the device's performance and optimizing the photodetection response in the 1-μm to 2-μm wavelength region by utilizing different QD film chemistries.



▲ Figure 1: Printing process (far left) and AFM images of QDs deposited from bare PDMS (left) and parylene coated PDMS (right). The QD solution is spin cast onto the PDMS stamp (1) and allowed to dry under vacuum for 30 minutes; then the substrate is placed on the stamp (2) and released (3). Chloroform has less of a surface energy mismatch with parylene than with PDMS, resulting in improved wetting. Smooth and continuous QD films are achieved down to a thickness of one monolayer.



▲ Figure 2: Current-voltage characteristics for a photovoltaic device consisting of a QD film printed from a bare PDMS stamp (blue) and a parylene coated PDMS stamp (red). The short circuit current and the open circuit voltage (Voc) are improved for the QD device deposited from parylene. The built-in potential (Vbi) (the potential at which the current in light, Jlight, is equal and opposite to the current in dark, Jdark) reaches 1.46V.

Reference

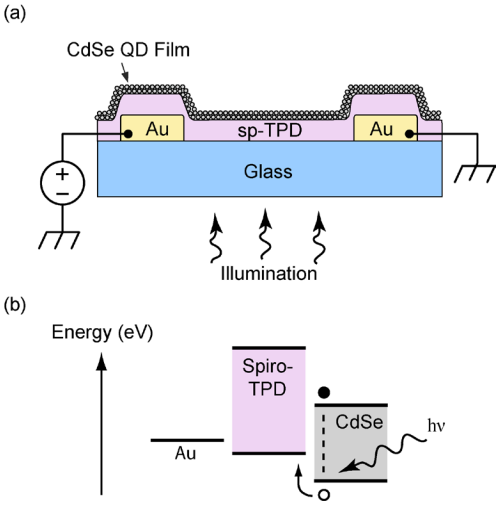
[1] D.C. Oertel, M.G. Bawendi, A.C. Arango, and V. Bulović, "Photodetectors based on treated CdSe quantum-dot films," *Applied Physics Letters*, vol. 87, no. 21, p. 213505, Nov 2005.

Organic/Quantum-dot Photoconductor

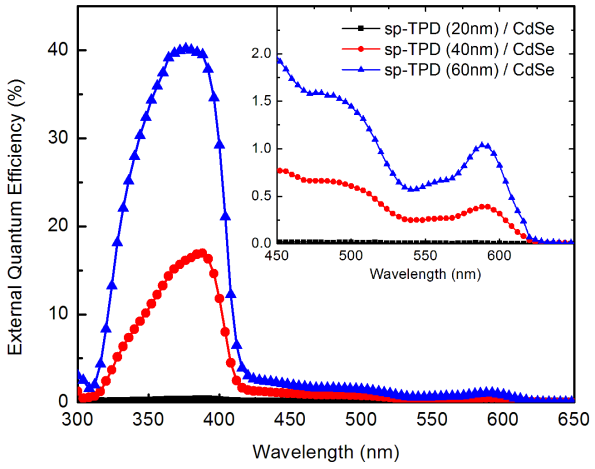
T. Osedach, J. Ho, A. Arango, S. Geyer, M. Bawendi, V. Bulović
Sponsorship: ISN, CMSE

We demonstrate an organic/quantum-dot (QD) photodetector in which charge transport is governed by a single organic layer and the optical absorption can be tuned according to quantum confinement of QDs composing a second layer. The optical and electrical characteristics of the device can be optimized independently through the modification of these two layers. A similar device composed of organic materials was previously demonstrated by our group [1]. Our work stands in contrast to the operation of conventional layered organic photodetectors in which carriers generated at a dissociating interface must travel through both heterojunction materials to reach the opposite electrodes. In such a device both layers are crucial to charge transport, making it difficult to modify the optical properties of the device, such as absorption spectrum, without significantly affecting its electrical characteristics.

The device consists of metallic interdigitated electrodes over which an organic charge transport layer is thermally evaporated (see Figure 1). Microcontact printing is then used to deposit a 50-nm-thick layer of colloidal QDs, completing the structure. The organic/QD interface manifests a type-II heterojunction suitable for dissociating excitons. Under illumination, light is absorbed throughout both layers of the device. Excitons created within an exciton diffusion length of the heterojunction interface are dissociated there, increasing in the carrier concentrations of both layers. A bias corresponding to a field of ~10^4 V/cm is applied across the electrodes to facilitate carrier collection. The increased hole density increases the organic film conductivity, which in turn manifests an increase in lateral current through the device. Figure 2 shows spectra of the external quantum efficiency exhibiting high efficiencies attributable to quantum-dot absorption. The device clearly separates the photogeneration and charge transport mechanisms and as such serves as a unique platform for studies of charge transfer at organic/QD interfaces for QD-sensitized photoactive devices.



▲ Figure 1: (a) Schematic of the device structure. (b) Energy band diagram. Excitons dissociate at the interface between the organic film and the quantum dots.



▲ Figure 2: External quantum efficiency spectrum. High efficiencies have been measured at absorption peaks corresponding to the organic layer as well as to the quantum-dot layer.

Reference

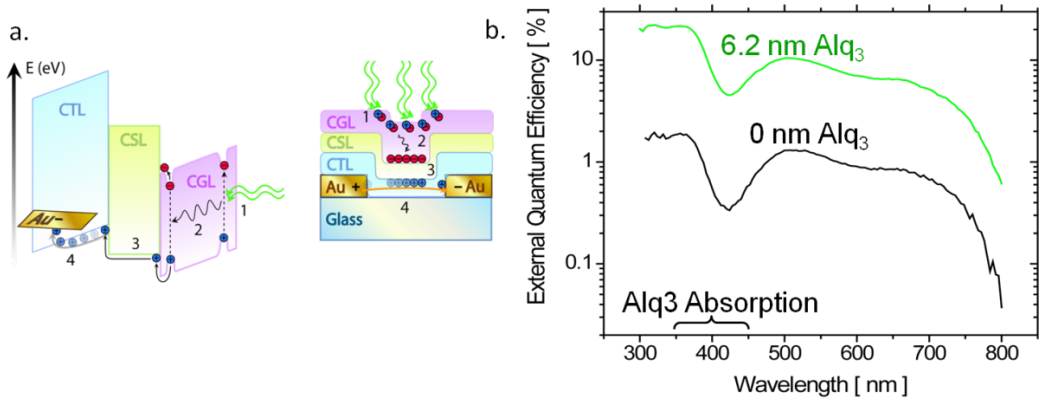
[1] J. Ho, A. Arango, and V. Bulović, "Lateral organic bi-layer heterojunction photoconductors," *Applied Physics Letters*, to be published.

Organic Multi-layer Lateral Heterojunction Phototransistors

J.C. Ho, J.A. Rowehl, V. Bulović
Sponsorship: ISN, CMSE

We fabricate a two-terminal, lateral multi-layer phototransistor [1] consisting of three molecular organic thin films with cascading energy bands (see Figure 1a): the charge transport layer is (CTL), N,N'-bis(3-methylphenyl)-N,N'-diphenyl-1,1'-biphenyl-4,4'-diamine (TPD); the charge spacer layer (CSL), tris(8-hydroxyquinoline)alumi num(III) (Alq_3); and the exciton generation layer (EGL), 3,4,9,10-perylenetetracarboxylic bis-benzimidazole (PTCBI). Placing an interstitial spacer layer between the CTL and the EGL improves the external quantum efficiency of tri-layer phototransistors over bi-layer, Type-II heterojunction phototransistors.

Light excitation acts as a pseudo "gate electrode" by generating excitons in PTCBI (EGL). Those excitons diffuse to the PTCBI/Alq_3 interface where they dissociate, leaving the electron behind in PTCBI, while the hole is initially injected into Alq_3 from where it can transfer to the more energetically favorable states in TPD. Excess holes in the TPD film raise the hole carrier concentration in the TPD film and increase the device conductance by forming a channel of excess carriers at the TPD/Alq_3 interface. The thin film of Alq_3 (CSL), between TPD (CTL) and PTCBI (EGL), spatially separates the dissociated carriers, reducing the likelihood of bimolecular recombination across the TPD/PTCBI interface. Bi-layer heterojunction phototransistors consisting of TPD and PTCBI alone have been shown to improve the external quantum efficiency over single layers of TPD and PTCBI by several orders of magnitude [2]. By introducing a CSL in a lateral tri-layer arrangement, we demonstrate an order of magnitude improvement over bi-layer lateral phototransistors without a CSL (see Figure 1b). The phototransistor contacts consist of interdigitated gold fingers that form a 30-mm-wide, 10-μm-long serpentine channel. Measurement of the photocurrent from a biased multi-layer, lateral heterojunction device [Au/TPD(47.5 ± 2) nm/Alq_3(6.2 ± 2) nm/PTCBI(52.5 ± 2) nm] reveals an internal quantum efficiency of (16 ± 1)% at an optical excitation wavelength of 573 nm. A thickness study of the Alq_3 spacer layer experimentally demonstrates the dependence of the carrier lifetime (at a heterointerface) and photoresponse efficiency on the spatial separation of dissociated charge.



▶ Figure 1: a. Energy band/cross-sectional diagrams of tri-layer phototransistors (1. absorption , 2. exciton diffusion, 3. exciton dissociation, 4. charge transport) b. Spectral response of EQE showing benefit of CSL .

References

[1] J. Ho, J. Rowehl, and V. Bulović, "Organic multi-layer lateral heterojunction phototransistors," to be presented at *Electronic Materials Conference*, Santa Barbara, CA, June 2008.

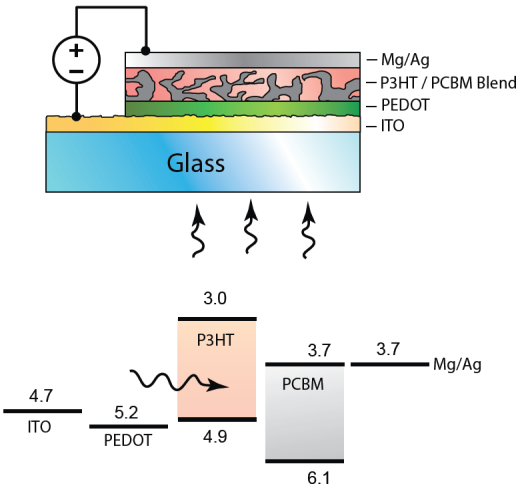
[2] J. Ho, A. Arango, and V. Bulović, "Lateral organic bi-layer heterojunction photoconductors," *Applied Physics Letters*, June 2008, to be published.

Inkjet Printing of P3HT/PCBM Solar Cells

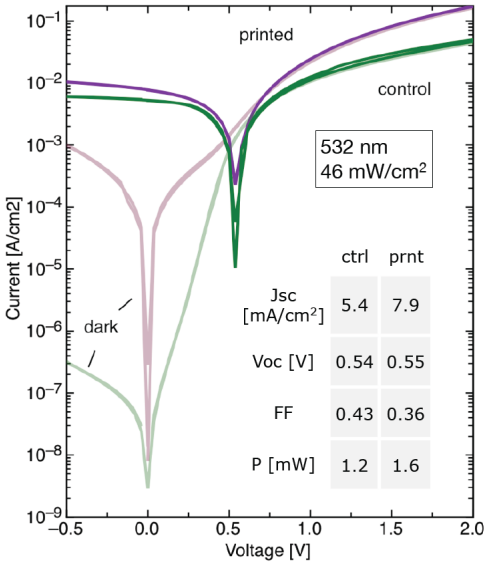
T. Osedach, A. Arango, J. Chen, V. Bulović
Sponsorship: ISN, CMSE

Polymeric solar cells offer the promise of a low-cost alternative to conventional inorganic photovoltaic devices. Particularly encouraging are solar cells consisting of blends of the polymer poly(3-hexylthiophene) (P3HT) and the fullerene derivative [6,6]-phenyl-C61-butyric acid methyl ester (PCBM) sandwiched between electrodes (see Figure 1). Recently, power efficiencies as high as 5.2% have been reported [1]. In an attempt to further improve the performance and cost-effectiveness of these solar cells so that they may become a more viable technology, we are exploring a number of variations to the standard processing procedure to fabricate them.

Presently, the processing of P3HT:PCBM devices used by most other groups involves a combination of spin-coating and thermal evaporation steps that are limited to small substrate sizes. In our study, we have used inkjet printing, a low-cost and highly scalable deposition technique, to deposit the active layers in P3HT:PCBM solar cells. The deposition of metal electrodes with inkjet printing is also currently being explored. Figure 2 shows current-voltage characteristics of a printed solar and a control device with a spin-coated active layer. The short-circuit current of the printed solar cell in this case exceeds that of the control device.



▲ Figure 1: (top) Device structure of a P3HT:PCBM solar cell. (bottom) Energy band diagram of the device. The P3HT and PCBM create a type-II heterojunction suitable for separating excitons.



▲ Figure 2: Current-voltage characteristics of an inkjet-printed solar cell versus a control device fabricated using spin-casting. The printed device exhibits a superior short-circuit current and open-circuit voltage, but a higher dark current.

Reference

[1] M.D. Irwin, D.B. Buchholz, A.W. Hains, R.P.H. Chang, and T.J. Marks, "P-type semiconducting nickel oxide as an efficiency-enhancing anode interfacial layer in polymer bulk-heterojunction solar cells," *Proc. National Academy of Sciences*, vol. 105, pp. 2783-2787, 2008.

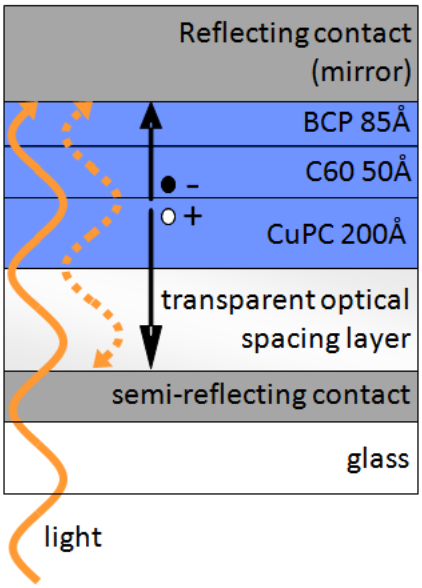
Monochromatic Organic Solar Cells

T.D. Heidel, M.A. Baldo
Sponsorship: DOE

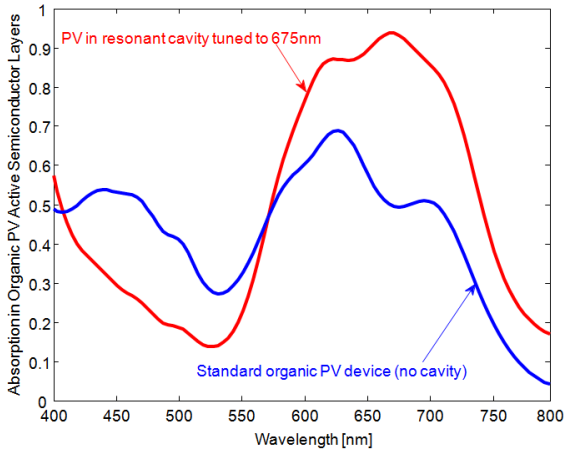
With a theoretical efficiency similar to conventional inorganic photovoltaics (PV) and the potential to be manufactured inexpensively over large areas, organic semiconductor technology offers a promising route to ubiquitous solar energy generation [1]. However, organic PVs are constrained by a tradeoff between exciton diffusion and optical absorption: as absorption is increased by fabricating thicker devices, the efficiency of charge separation decreases since excitons cannot reach the charge separation interface. Ultimately, this tradeoff limits the portion of the solar spectrum that optimized organic PVs can harness.

In our work, we increase absorption in organic solar cells within the limits of exciton diffusion by fabricating cells inside a resonant microcavity [2]. As Figure 1 illustrates, the resonant cavity devices have a semi-reflecting bottom contact and a fully reflecting mirror contact on the back. The layers between the contacts consist of a transparent optical spacing layer and a thin organic solar cell [3]. Modulating the thickness of the transparent spacing layer allows the increase in absorption to be tuned across the entire visible spectrum. The reflectivity of the contacts can also be engineered to modulate the width of the absorption resonance. Fabricating a thin organic solar cell within the cavity allows charge separation efficiencies to reach 100%. Modeling indicates that absorption in the organic semiconductor layers can be increased as much as 91% relative to absorption in optimized organic PVs with no resonant cavity; see Figure 2.

Resonant cavity monochromatic organic solar cells have applications in tandem organic solar cells and advanced solar concentrator designs. Organic tandem solar cells attempt to overcome the tradeoff between exciton diffusion and absorption by utilizing multiple heterojunctions that absorb most strongly in different regions of the solar spectrum. High-efficiency, monochromatic solar cells could increase the efficiency of these individual multiple heterojunctions. The efficiency of many solar concentrator designs could also be maximized by using solar cells optimized for specific regions of the solar spectrum.



▲ Figure 1: Resonant cavity organic solar cells consist of a thin organic PV and transparent optical spacing layer fabricated between reflecting contacts.



▲ Figure 2: The resonant cavity enhances absorption strongly in one region of the solar spectrum. The absorption peak can be tuned across the entire visible spectrum. Combining two or more cavity organic PVs will allow for enhancement across the entire visible spectrum.

References

[1] P. Peumans, A. Yakimov, and S.R. Forrest, "Small molecular weight organic thin-film photodetectors and solar cells," *Journal of Applied Physics*, vol. 93, no. 7, pp. 3693-3723, Apr. 2003.

[2] T.D. Heidel, J.K. Mapel, M. Singh, K. Celebi, and M.A. Baldo, "Surface plasmon polariton mediated energy transfer in organic photovoltaic devices," *Applied Physics Letters*, vol. 91, no. 093506, Aug. 2007.

[3] K. Walzer, B. Maennig, M. Pfeiffer, and K. Leo, "Highly efficient organic devices based on electrically doped transport layers," *Chemical Reviews*, vol. 107, pp. 1233-1271, Mar. 2007.

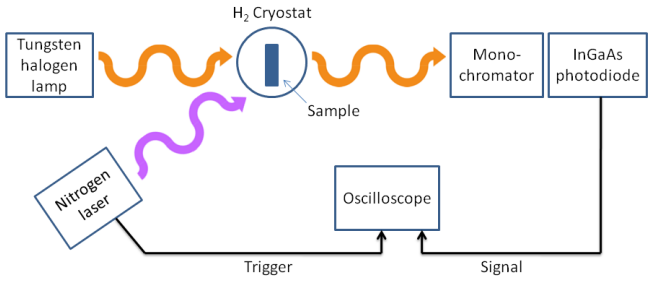
Charge Recombination in Small-molecular-weight Organic Solar Cells

J. Lee, M. Segal, M.A. Baldo
Sponsorship: SRC/FCRP MSD

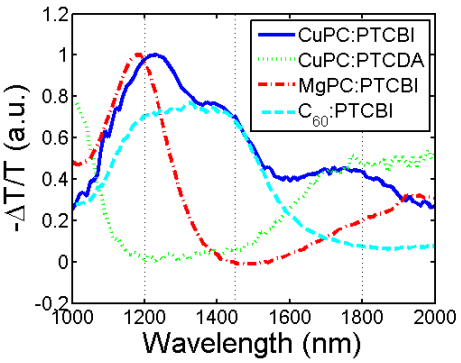
Organic solar cells promise efficient and cost-effective solar energy generation from low-cost materials and a low-temperature manufacturing process compatible with flexible plastic substrates. In organic photovoltaic cells, photon absorption creates a bound electron-hole pair, or exciton. The excitons diffuse toward the donor-acceptor (DA) heterojunction. The energy offset at the DA interface dissociates the strongly bound excitons in organic molecules with near-unity efficiency. Excitons are separated into charge transfer (CT) states, which are bound electron-hole pairs across the DA junction [1]. The CT states can be dissociated into free carriers that ultimately generate photocurrent or they may recombine into low-energy states such as ground states or triplet excitons. The recombination of CT states can cause a substantial loss in the photovoltaic efficiency depending on the CT state lifetime and the operating voltage bias.

We perform transient absorption spectroscopy to study the charge recombination dynamics of small-molecular-weight organic solar cells. The transient absorption setup was built as illustrated in Figure 1. The samples are held at the temperature of 50K. We investigate thin film bulk heterojunction of the archetype organic solar cell molecules, copper phthalocyanine (CuPC) and 3,4,9,10-perylenetetracarboxylic bis-benzimidazole (PTCBI). To assign the absorption wavelength of CuPC cations and PTCBI anions, the photoinduced absorption (PIA) spectra of related organic molecules are compared as shown in Figure 2. The CT states in CuPC/PTCBI live up to milliseconds. Also, we found that the states featuring the broad peak at 1450 nm decay much faster than the CT states with the lifetime of ~150 μs. We tentatively assign the state at 1450nm to the PTCBI triplet exciton. The evidence of triplet excitons implies that PTCBI triplet formation is an importance source of recombination loss in CuPC/PTCBI photovoltaic cells.

Further study of organic heterojunction thin films is expected to reveal the physical origin of charge recombination and should contribute to reducing the recombination loss in organic photovoltaic cells.



▲ Figure 1: Schematic diagram of the transient absorption setup. The nitrogen laser creates excitons, which we subsequently dissociated into CT states. Then, the CT states absorb the white light provided by the tungsten halogen lamp. The photodiode detects the change of the transmitted light at the selected wavelength. The setup probes the decay dynamics of CT states.



▲ Figure 2: The PIA spectrum of organic bulk heterojunction thin films that are studied in this work. PTCDA: 3,4,9,10-perylenetetracarboxylic dianhydride, MgPC: magnesium phthalocyanine.

Reference

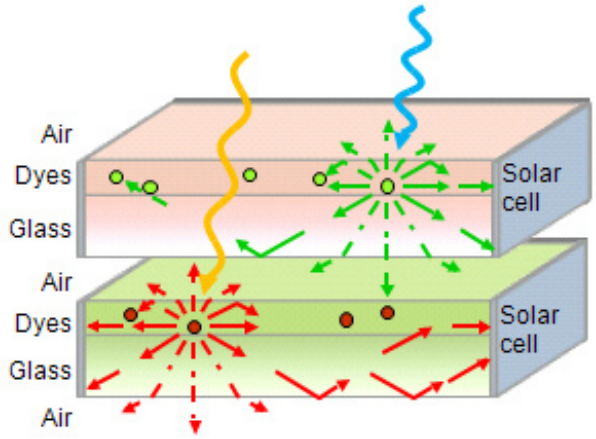
[1] P. Peumans, A. Yakimov, and S.R. Forrest, "Small molecular weight organic thin-film photodetectors and solar cells," *Journal of Applied Physics*, vol. 93, no. 7, pp. 3693-3723, Apr. 2003.

High-efficiency Organic Solar Concentrators

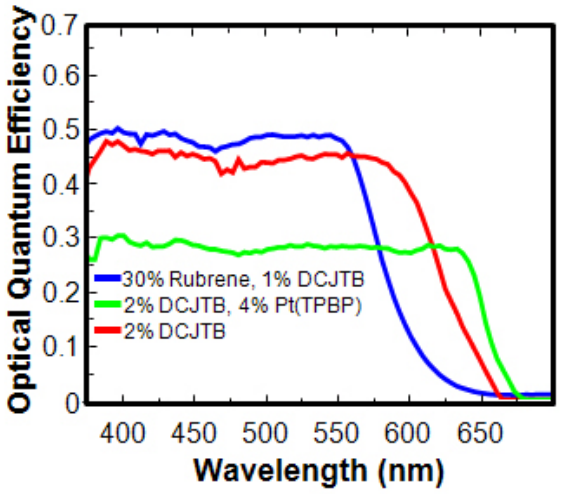
J.K. Mapel, M.J. Currie, T.D. Heidel, S. Goffri, M.A. Baldo
Sponsorship: DOE, NSF NIRT

Organic solar concentrators (OSC) are a class of luminescent solar concentrators [1] that exploit advances in thin-film organic semiconductor technology and low-cost manufacturing processes to create efficient, large-area optical concentrators for inorganic solar cells. The OSCs are dye-based light concentrators that operate through successive absorption and emission of light into confined modes of a light guide to a photovoltaic cell for electrical conversion; see Figure 1. These OSCs hold the potential to reduce the cost per generated watt of power for solar power transduction systems by separating the optical and electrical parts of a solar cell. Previous demonstrations have shown limited performance due to the high probability of re-absorption of confined light, which lowers the guided transport efficiency [2].

We have fabricated single and tandem waveguide organic solar concentrators with quantum efficiencies exceeding 50% and projected power efficiencies up to 6.8%; see Figure 2. Near field energy transfer [3], solid state solvation [4], and phosphorescence [5] are employed within a thin-film organic coating on glass to substantially reduce self-absorption losses, enabling flux gains exceeding F = 10, meaning that a photovoltaic cell attached to the concentrator generates approximately 10 × the power of the photovoltaic cell without optical concentration. Flux gains of F > 10 in organic solar concentrators should enable the economical use of high performance photovoltaic cells in low-cost systems.



▲ Figure 1: Physical processes leading to energy conversion in an OSC. Photons are absorbed by a luminescent chromophore embedded within or coating a waveguide. The chromophore can re-radiate a photon of equal or lesser energy, and some portion of the emitted radiation will be confined in the waveguide by total internal reflection. Some fraction of the trapped light will travel to another face of the guide that has a smaller cross-sectional area, where a photovoltaic element resides for the collection of the concentrated light.



▲ Figure 2: Optical quantum efficiency (OQE) spectra at a geometric gain of 3. The OQE is the fraction of incident photons that are emitted from the edges of the single waveguide OSC. In blue, the OSC utilizes near-field energy transfer from the AlQ3 matrix and rubrene dopants to pump emission through DCJTB, a laser dye. In green, light is absorbed by AlQ3, rubrene, and Pt(TBTP) and phosphoresces from Pt(TBTP). The energetic separation between absorption and emission in these OSCs enables higher flux gains than in single-material systems.

References

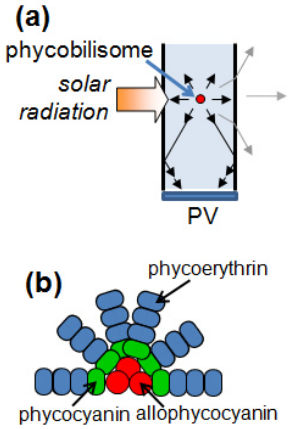
[1] W.H. Weber and J. Lambe, "Luminescent greenhouse collector for solar radiation," *Applied Optics*, vol. 15, p. 2299, 1976.
[2] J.S. Batchelder, A.H. Zewail, and T. Cole, "Luminescent solar collectors: experimental and theoretical analysis of their possible efficiencies," *Applied Optics*, vol. 20, p. 3733, 1981.
[3] T. Förster, "Transfer mechanisms of electronic excitation," *Discussions of the Faraday Society*, vol. 27, p. 7, 1959.
[4] V. Bulović *et al.*, "Bright, saturated, red-to-yellow organic light-emitting devices based on polarization-induced spectral shifts," *Chemical Physics Letters*, vol. 287, p. 455, 1998.
[5] M.A. Baldo *et al.*, "Highly efficient phosphorescent emission from organic electroluminescent devices," *Nature*, vol. 395, p. 151, 1998.

Luminescent Solar Concentrators Employing Phycobilisomes

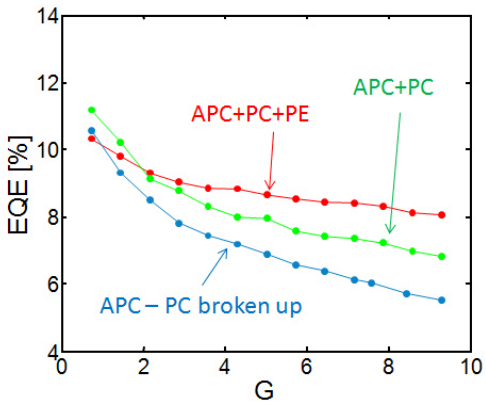
C.L. Mulder, L. Theogarajan, M. Currie, J.K. Mapel, M.A. Baldo
Sponsorship: NSF NIRT, DOE

We present luminescent solar concentrators (LSCs) employing phycobilisomes from cyanobacteria. Luminescent solar concentrators are non-tracking optical collectors that increase the effective light-capture area of a solar-energy conversion device, while reducing the size of the expensive photovoltaic (Figure 1a) [1]. The geometric gain, *G*, is an important metric of LSC performance. It is defined as the ratio of the light collection area to that of the photovoltaic. Increasing *G* increases the total power per unit cost. But at large geometric gains, photons trapped in the LSC are subject to self-absorption losses that degrade performance. In this work we employ a biological photosynthetic system to study and circumvent the effects of self-absorption.

Phycobilisomes are macromolecular antenna complexes that are responsible for collecting light in photosynthetic systems (see Figure 2b for a schematic representation) [2]. Each of these proteins serves as a scaffold for pigment molecules, also known as chromophores. The chromophores are arranged through self-assembly in cascading Förster energy transfer pathways that couple short wavelength chromophores at the extremities of the complex to long wavelength chromophores at the core of the complex, thereby enhancing the Stokes shift between absorption and emission. We have characterized the optical absorbance and photoluminescence spectra and efficiencies of several different types of phycobilisomes and compared their performance when used as the active dye in a liquid or solid state LSC. The first type of phycobilisomes consisted of allophycocyanin (APC) with short rods of phycocyanin (PC) proteins (green). The second type consisted of APC with long rods of PC and PE proteins (red), which showed an increased Stokes shift in comparison to the first type of phycobilisomes. This increase in rod length was accompanied by a better performance with geometric scaling, reflecting the suppression of self-absorbance losses achieved by reducing the overlap between the emission and absorption spectra. When the internal Förster energy transfer was shut off by breaking up the phycobilisomes into their loose protein complexes, the LSC showed an even larger drop in efficiency with increasing geometric gain (blue). At G =9.3, the efficiency was 50% lower in the broken complexes than the complete APC + PC + PE phycobilisomes. These results suggest that using resonant energy transfer from higher to lower energy chromophores might provide a route to reducing self-absorption losses in LSCs.



▲ Figure 1: (a) A schematic representation of a luminescent solar concentrator. (b) A schematic representation of a phycobilisome. These antenna complexes consist of a core of allophycocyanin (APC) that is connected to radial rods of phycocyanin (PC) billins and/or phycoerthyrin (PE) billins.



▲ Figure 2: External quantum efficiency at the peak absorption wavelength vs. geometric gain of LSCs employing phycobilisomes as the optical dye system. The complexes having the largest Stokes shift, the phycobilisomes with APC, PC and PE (red), showed the least roll-off with increasing G. The complexes with APC and short rods of PC exhibited a larger roll-off, while the dye system for which the internal Förster transfer was shut off (blue) had the poorest performance with increasing G.

References

[1] J.S. Batchelder, A.H. Zewail, and T. Cole, "Luminescent solar concentrators. 2: Experimental and theoretical analysis of their possible efficiencies," *Applied Optics*, vol. 20, pp. 3733-3754, Nov. 1981.

[2] R.E. Blankenship, *Molecular Mechanics of Photosynthesis*. Oxford: Blackwell Science Ltd., 2002.

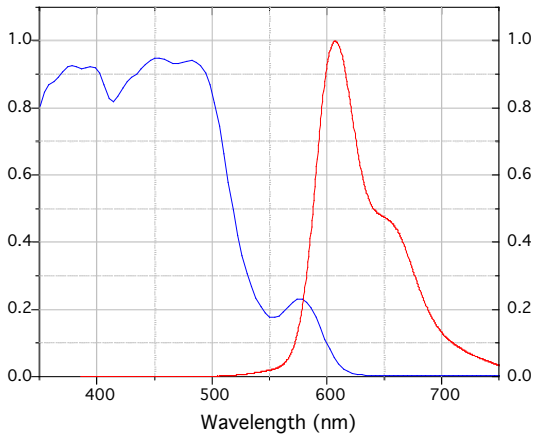
Solution-processed Organic Solar Concentrators

S. Goffri, M. Currie, J. Mapel, M.A. Baldo

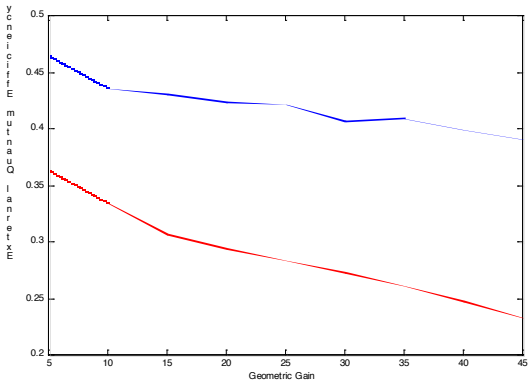
Solar energy is a clean and abundant energy source that promises to provide sustainable and economical sources of renewable power. Solar power generation is growing; however, it is still more expensive than fossil-fuel-based electricity sources. To address the cost of solar power, we are developing organic solar concentrators (OSCs) as an alternative to conventional solar concentrators. These OSCs do not require tracking of the sun or cooling of the solar cells and they require a smaller area of photovoltaic (PV) cells for the same power output.

An OSC is composed of organic chromophores to absorb sunlight and re-emit photons into a planar waveguide with PV cells attached to the edges [1-4]. The performance of an OSC is largely limited by self-absorption of the emitted photons by organic chromophores due to an overlap between their absorption and emission. We have investigated the used of novel chromophores and their compositions to reduce the overlap between emission and absorption. We coat glass flat-plate collectors using solution-processing, resulting in low-cost, thin-film solar collectors. This enables us to use recent advances in organic optoelectronics and apply near-field energy transfer to reduce the required concentration and hence the self-absorption of the emissive dye [5] (Figure 1).

The ratio of the area of the concentrator to the area of the PV cell is the geometric gain, *G*. Figure 2 shows the external quantum efficiency (EQE) as a function of geometric gain for different systems measured at $\lambda = 489$ nm for the composite perylene-based fluorescent system compared to the conventional 4-(dicyanomethylene)-2-*t-butyl*-6-(1,1,7,7-tetramethyljulolidyl-9-enyl)-4*H*-pyran(16) (DCJTB)-based fluorescent system, measured at $\lambda = 532$ nm. The DCJTB-based OSC shows the strong self-absorption. The self-absorption is lower in the composite perylene-based OSC, consistent with the spectroscopic data in Figure 1.



▲ Figure 1: Normalized absorption and emission spectra of perylene-based OSC film. The ratio between the peak absorption coefficient and the absorption coefficient at the emission wavelength provides a measure of the self-absorption in an OSC film.



▲ Figure 2: OSC efficiency as a function of geometric gain, *G*. With increasing *G*, photons must take a longer path to the edge-attached PV, increasing the probability of self-absorption losses. Blue: perylene composite system, red: single DCJTB-based system.

References

[1] J.S. Batchelder, A.H. Zewail, and T.W. Cole, "Luminescent solar concentrators. 1: Theory of operation and techniques for performance evaluation," *Applied Optics*, vol. 18, pp. 3090-3110, Sept. 1979.

[2] J.S. Batchelder, A.H. Zewail, and T.W. Cole, "Luminescent solar concentrators. 2: Experimental and theoretical analysis of their possible efficiencies," *Applied Optics*, vol. 20, pp. 3733-3754, June 1981.

[3] A. Goetzberger and W. Greubel, "Solar energy conversion with fluorescent concentrators," *Applied Physics*, vol. 14, pp. Sep. 1977.

[4] W.H. Weber and J. Lambe, "Luminescent greenhouse collector for solar-radiation," *Applied Optics*, vol. 15, pp. 2299-2300, Oct. 1976.

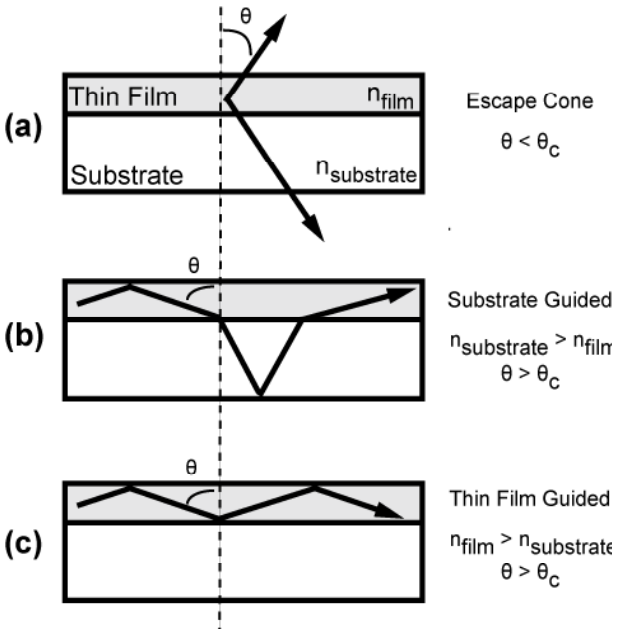
[5] T. Förster, "Transfer mechanisms of electronic excitation," *Discussions of the Faraday Society*, vol. 27, pp. 7-17, Apr. 1959.

Self-absorption Measurements of Photoluminescent Efficiency of Thin-film Organic Semiconductors

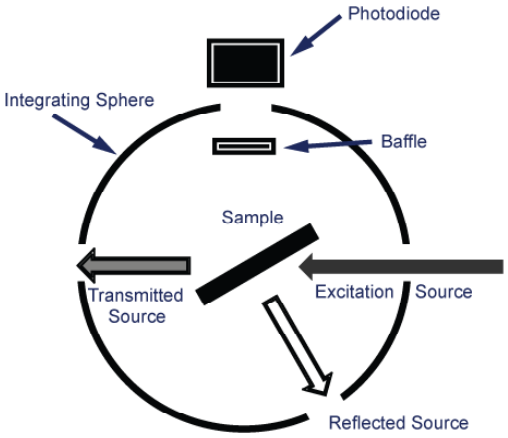
Authors: M. Currie, J. Mapel, S. Goffri, M.A. Baldo
Sponsorship: DARPA/AFOSR, NSF NIRT

Characterizing the photoluminescent (PL) efficiency of thin films is essential to ascertaining the performance limits of light-emitting devices. The PL efficiency is the fraction of photons emitted per photon absorbed. Integrating sphere measurements is a common method used to measure PL efficiencies, but we show that the substrate must possess an index of refraction greater than that of the thin film to be valid [1-3]. The substrate index restriction is demonstrated by measuring the PL of commonly used organic materials on low- and high-index substrates. Measurements on low-index substrates exhibit optical losses due to thin-film waveguiding that result in an errors up to 50%. This effect is pronounced for low Stokes-shift films with large self-absorption. Figure 1 depicts the three light-paths for a thin film deposited on a transparent substrate, and Figure 2 shows the measurement set-up.

To illustrate substrate effects on PL measurements, three films were prepared on high (n = 1.80) and low (n = 1.52) index glass substrates that are 25mm x 25mm x 2mm in size. A neat 200-nm-thick film of tris (8-hydroxyquinoline) aluminum (AlQ_3), and a 200-nm-thick film of AlQ_3 and rubrene at (50% v/v) were thermally deposited. The PL efficiency of AlQ_3 is 29.2% and 28.1% on high- and low-index substrates, respectively. The error due to thin-film waveguiding on the low-index substrate is low due to the large Stokes shift and low self-absorption in AlQ3. The PL efficiency of rubrene, however, is 43.3% and 30.2% on high- and low-index substrates, respectively demonstrated a significant error if the PL efficiency measurement is performed on low-index substrates.



▲ Figure 1: Light-paths for a thin film on a transparent substrate: There are three potential pathways for light to travel within, and eventually leave, a thin film deposited on a transparent substrate: (a) escape cone light, (b) substrate-guided light, and (c) thin-film-guided light. Light that is guided in the thin film will largely be reabsorbed and underestimate PL in these measurements.



▲ Figure 2: Schematic of Integrating Sphere Measurement: Shown is the configuration used to measure PL within an integrating sphere. The sphere and sample are aligned such that the transmitted and reflected beams of the excitation source leave the sphere through an outlet port. The baffle within the integrating sphere prevents the photodiode from sensing direct photoluminescence from the sample.

References

[1] N.C. Greenham, N.C., I.D.W. Samuel, G.R. Hayes, R.T. Phillips, Y. Kessener, S.C. Moratti, et al., "Measurement of absolute photoluminescence quantum efficiencies in conjugated polymers," *Chemical Physics Letters*, vol. 241, pp. 89-96, 1995.

[2] A.R. Johnson, S.J. Lee, J. Klein, and J. Kanicki, "Absolute photoluminescence quantum efficiency measurement of light-emitting thin films," *Review of Scientific Instruments*, vol. 78, no. 9, pp. 096101:1-3, 2007.

[3] A. Nollau, M. Hoffmann, K. Floreck, T. Fritz, and K. Leo, "A simple measurement of the absolute internal quantum efficiency of thin organic films," *Journal of Applied Physics*, vol. 87, no. 11, pp. 7802-7804, 2000.

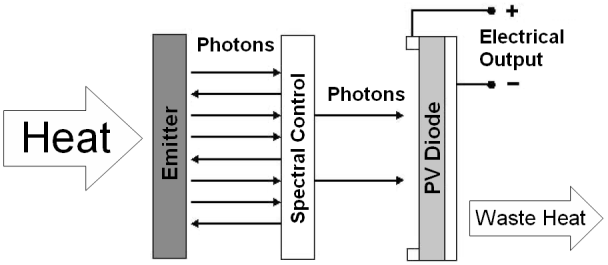
Radiative Spectrum Modification through Photonic Crystal-based Tungsten Microstructures

N. Jovanović, I. Čelanović, J. Kassakian

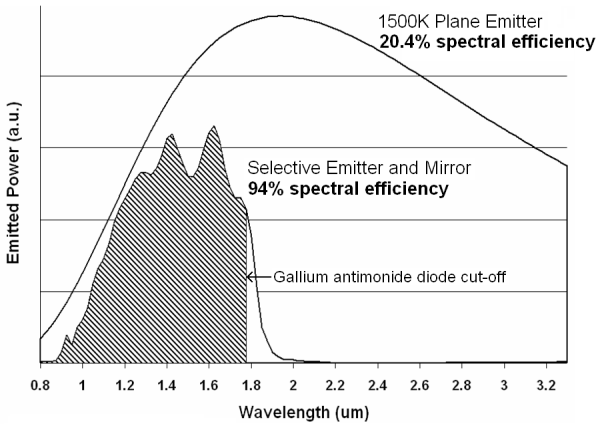
Sponsorship: Toyota Motor Corporation, MIT/Industry Consortium on Advanced Automotive Electrical/Electronic Components and Systems

This research investigates the fabrication, modeling, characterization, and application of tungsten two-dimensional (2D) photonic crystals (PhCs) as selective emitters and means of achieving higher efficiencies in thermophotovoltaic (TPV) energy conversion systems. A basic TPV system (Figure 1) consists of two parts: a thermal emitter and a photovoltaic (PV) diode. Thermal energy is provided to an emitting surface — the thermal emitter — which in turn radiates a spectrum of photons. The radiated photons are converted into free charge carriers when absorbed by the PV diode. Advantages of TPV systems include quiet operation, long lifetime, relatively low maintenance, portability, and scalability (TPV systems can be designed to meet a variety of energy needs, from watts to kilowatts). The two main shortcomings of TPV systems are low efficiency and high cost. The results of this research show that TPV systems can even exceed the efficiency of conventional power conversion mechanisms through highly-efficient spectral control.

Spectral control in TPV systems refers to the modification of the emitted spectrum to best match the PV diode sensitivity. In our particular case, spectral control is achieved through use of two components: a selective emitter and an optical filter. The optical filter, a result of our previous research project, is a one-dimensional dielectric stack [1] designed to match the gallium antimonide diode characteristics, which have become the standard in TPV systems. The selective emitter is a tungsten microstructure based on a 2D PhC pattern. Optical characterization of our selective emitter prototypes is found to be in excellent agreement with simulation and has provided an experimental confirmation of selective emitter performance (Figure 2). We show that selective emitters can substantially increase spectral efficiency, providing as much as three times the radiative power density of planar tungsten. Our measurements indicate as much as 94% combined spectral efficiency of a selective emitter and a dielectric stack mirror for TPV system applications.



▲ Figure 1: A basic thermophotovoltaic power conversion system consists of an emitter and a photovoltaic diode. The addition of spectral control components drastically increases the system efficiency.



▲ Figure 2: Radiative spectrum of a tungsten PhC-based selective emitter prototype compared to a planar black-body emitter at 1500K. Used with gallium antimonide diodes, our selective emitter and dielectric filter achieve 94% spectral efficiency.

Reference

[1] F. O'Sullivan, I. Čelanović, N. Jovanović, and J. Kassakian, "Optical characteristics of one-dimensional Si/SiO2 photonic crystals for thermophotovoltaic applications," *Journal of Applied Physics*, vol. 97, Jan. 2005.

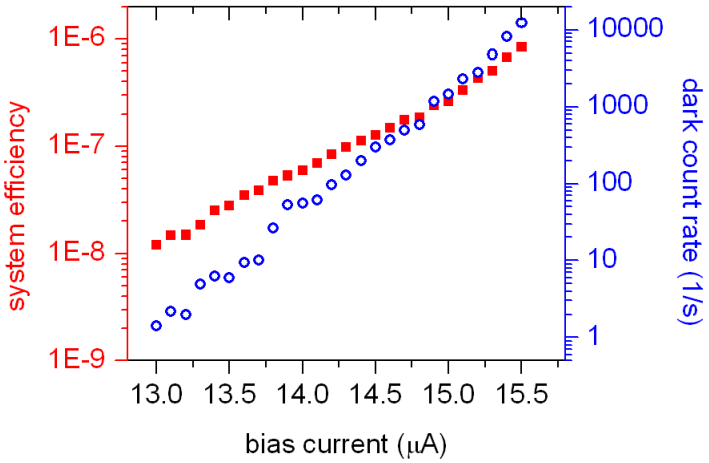
Packaging Superconductive Nanowire Single-photon Detectors

X. Hu, K.K. Berggren, F.N.C. Wong
Sponsorship: IARPA

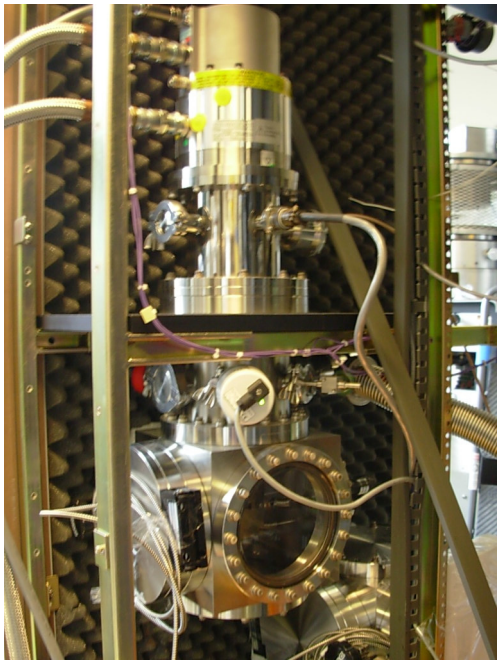
The superconductive nanowire single-photon detector (SNSPD) is an emerging ultra-sensitive photon-counting technology that can be used in quantum key distribution, deep-space optical communication and defect-detection for integrated circuits. In the past, we have successfully developed a robust process to fabricate SNSPDs and have demonstrated device-detection efficiency above 50% at near-infrared wavelengths [1]. To enable the above-mentioned applications, however, one remaining challenge must be met: packaging the SNSPDs so that the light can be efficiently coupled into the detectors. This step is difficult because of the small active area of the SNSPD and its low temperature operation.

To achieve such efficient coupling, we have designed an experimental setup to perform helium-immersed testing of SNSPDs inside a dewar. The major part of the setup is a probe in which are integrated a chip-holder, a fiber-focuser, three nanopositioners, a temperature sensor, and electrical connections. The fiber-focuser is used to shrink the spot-size of the light from a single-mode fiber down 5 μm, and the nanopositioners are used to accurately adjust the position of the spot in-situ three-dimensionally. The detector is directly connected with an SMA connector through wire bonding. Figure 1 shows some preliminary results, and further optimization is being performed.

Meanwhile, a more convenient, plug-in SNSPD system is being developed based on a closed-cycle, two-staged cryocooler that can reach 2.8 K (see Figure 2). Its main parts include a two-stage cold head, a compressor, a pump system, and a vacuum chamber. The main advantage of the cryocooler over the dewar is that it does not need liquid helium and is free to move. Therefore, this SNSPD system can facilitate many experiments in the field of quantum optics.



▲ Figure 1: System efficiency and dark count rate of a single-photon detector measured by helium-immersion testing.



▲ Figure 2: The two-stage cryocooler for the testing of superconductive nanowire single-photon detectors.

Reference

[1] K.M. Rosfjord, J.K.W. Yang, E.A. Dauler, A.J. Kerman, V. Anant, B.M. Voronov, G.N. Gol'tsman, and K.K. Berggren, "Nanowire single-photon detector with an integrated optical cavity and anti-reflection coating," *Optics Express*, vol. 14, issue 2, pp. 527-534, Jan. 2006.

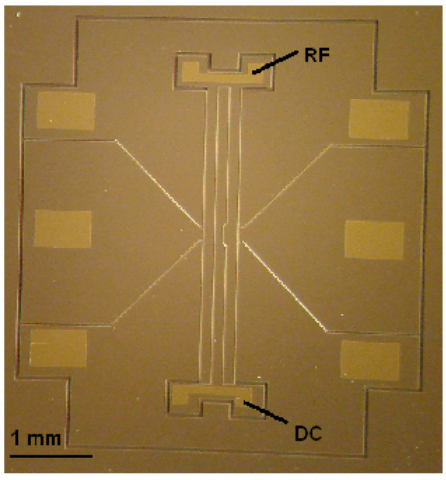
Trapping Ions with a Superconducting Ion Trap

Y. Ge, E. Dauler, J. Labaziewicz, S. Wang, I. Chuang, K.K. Berggren
Sponsorship: NSF Center for Ultracold Atoms, Japan Science and Technology Agency, MIT

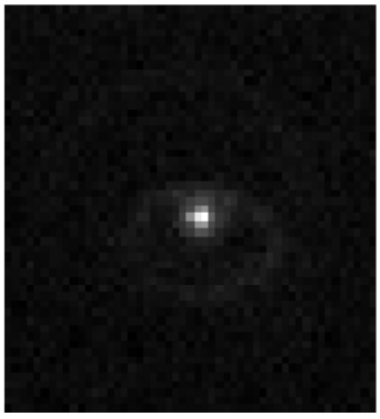
We demonstrate an approach for fabricating a superconducting surface-electrode ion trap. Surface-electrode ion traps, while promising for large-scale quantum computation, have long been challenged by ion heating rates, which increase rapidly as trap length scales are reduced [1-3]. One promising approach to solve this problem is to fabricate trap electrodes from superconductors and to operate the ion trap chip at cryogenic temperatures.

The surface-electrode superconducting ion trap was fabricated from 140-nm-thick NbN on an insulating sapphire substrate. As Figure 1 shows, the ion trap has one RF, one ground, and four DC electrodes. Ions are trapped 100 μm above the surface in the center of the central ground electrode [4]. The NbN was deposited on R-plane sapphire using DC magnetron sputtering of a Niobium target in a 12% N_2 + 88% Ar gas mixture. Before deposition, the wafer was backside-coated with Niobium and the wafer was heated on an 800°C inconel block during the NbN deposition. The resulting ~140-nm-thick NbN film was superconducting at temperatures below T_c = 13K. In order to define the electrodes, optical lithography was performed using negative photoresist (NR9-3000) and this pattern was transferred into the 140-nm-thick NbN film using reactive-ion-etching with CF_4 and O_2. Finally, gold contact pads were defined by optical lithography using positive photoresist (S1813) and a liftoff process. To preserve superconductivity, all baking procedures were performed at or below 90°C.

The superconducting NbN ion trap successfully trapped single ions at temperatures sufficiently below its critical temperature, where the superconductivity could be maintained while applying the required trapping voltages. We measured the ion heating rates while operating the superconducting NbN ion trap at 6K. A single strontium ion was sideband-cooled to its quantum ground state motion, as shown in Figure 2. One 100-μm-size superconducting NbN ion trap showed an ion heating rate of 10~20 quanta, similar to low-resistivity, non-superconducting ion traps at cryogenic temperatures. When the temperature was above T_c, the NbN ion trap failed to trap ions due to the large resistivity change of the NbN RF electrode around T_c. In the future, superconducting traps with lower normal-state resistivity will be investigated in order to study how the electrode resistivity influences the ion heating rate.



▲ Figure 1: Optical microscope photograph of a surface electrode NbN ion trap with gold contact pads. The ion trap consists of one RF, one ground, and four DC electrodes.



▲ Figure 2: A single strontium ion is trapped with the surface electrode NbN ion trap at 6K, sideband-cooled to its quantum ground state motion.

References

[1] D. Stick, W. K. Hensinger, S. Olmschenk, M.J. Madsen, K. Schwab, and C. Monroe, "Ion trap in a semiconductor chip," *Nature Physics*, vol. 2, pp. 36-39, Jan. 2006.
[2] L. Deslauriers, S. Olmschenk, D. Stick, W.K. Hensinger, J. Sterk, and C. Monroe, " Scaling and suppression of anomalous heating in ion traps," *Physical Review Letters*, vol. 97, p. 103007, Sept. 2006.
[3] S. Seidelin and J. Chiaverini, " Microfabricated surface-electrode ion trap for scalable quantum information processing," *Physical Review Letters*, vol. 96, p. 253003, June 2006.
[4] J. Labaziewcz, Y. Ge, P. Antohi, D. Leibrandt, K. Brown, and I.L. Chuang, " Suppression of heating rates in cryogenic surface-electrode ion traps," *Physical Review Letters*, vol. 100, p. 130001, 2008.

Guided-wave Devices for Holographic Video Display

D. Smalley, V.M. Bove, Jr., Q. Smithwick

Sponsorship: CELab, Digital Life, and Things That Think Research Consortia, Media Laboratory

We are developing a guided-wave optical modulator [1, 2] with 1-GHz composite bandwidth Surface Acoustic Wave (SAW) transducer arrays for use in video displays. This device is designed to diffract light horizontally and deflect it vertically through mode conversion by creating surface acoustic waves that interact with light trapped in waveguides on the surface of a lithium niobate substrate. To fabricate this modulator, we first mask a wafer of Z-cut lithium niobate with SiO_2 through a plasma-enhanced chemical vapor deposition (PECVD) process and then immerse it in heated benzoic acid and lithium benzoate to create single polarization waveguides. The waveguide is subsequently annealed to restore its acoustic properties. Finally, we pattern aluminum transducers onto the waveguides by conformal contact lithography employing a negative resist lift-off technique.

The goal of this work is to enable the inexpensive manufacturing of Scophony-architecture video displays [3] (both 2D and holographic video [4-5]) without the need for the horizontal scanning mirrors that typically limit the scalability of this technology.

Figure 1: A device undergoing testing.

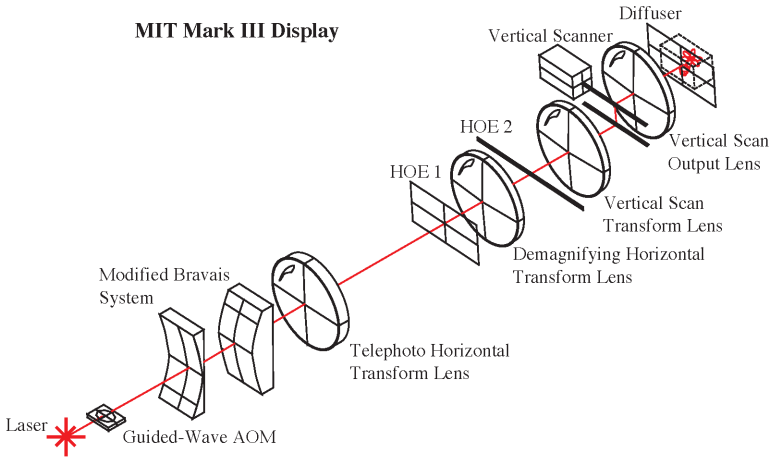


Figure 2: Architecture of our display system.

References

[1] C.S. Tsai, Q. Li, and C.L. Chang, "Guided-wave two-dimensional acousto-optic scanner using proton-exchanged lithium niobate waveguide," *Fiber and Integrated Optics*, vol. 17, pp. 57-166, 1998.

[2] D. Smalley, "Integrated-optic holovideo," Master's thesis, Massachusetts Institute of Technology, Cambridge MA, 2006.

[3] H.W. Lee, "The Scophony television receiver," *Nature*, vol. 142, pp. 59-62, July 1938.

[4] D.E. Smalley, Q.Y.J. Smithwick, and V.M. Bove, Jr., "Holographic video display based on guided-wave acousto-optic devices," *Proc. SPIE Practical Holography XXI*, vol. 6488, p. 64880L, 2007.

[5] W. Plesniak, M. Halle, V.M. Bove, Jr., J. Barabas, and R. Pappu, "Reconfigurable image projection (RIP) holograms," *Optical Engineering*, vol. 45, p. 115801, Nov. 2006.

Selective Epitaxial Growth of Ge for Photodiode Applications

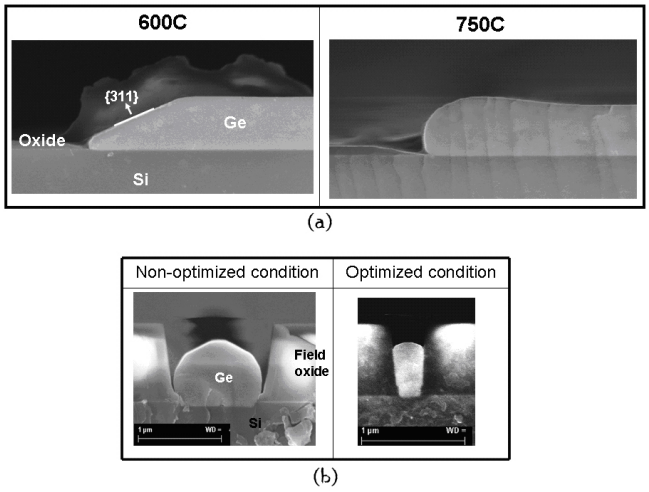
M. Kim, O.O. Olubuyide, J.L. Hoyt

Sponsorship: DARPA, NSF Graduate Research Fellowship

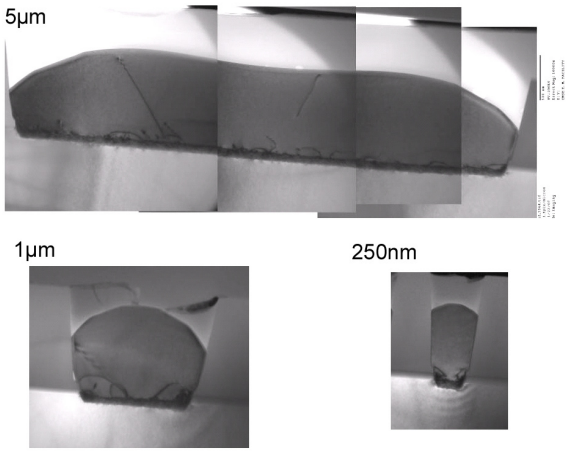
We studied and optimized the growth parameters for selective epitaxial growth of Ge-on-Si for application of photodiodes operating at 1.55 μm [1]. Approximately 1 μm-thick, relaxed Ge was grown in exposed Si regions on oxide-patterned Si wafers. Germanium morphology and threading dislocation density were studied as functions of growth and processing conditions.

The morphology of the Ge films, especially faceting, becomes an issue when the Ge growth area is defined by vertical oxide walls, and a good hole-filling behavior is desired. Unlike the selective epitaxial growth of Si, where reducing the temperature reduces the {311} facet [2], selective Ge growth shows the opposite behavior and the {311} facet is reduced for increasing temperature. With the chamber pressure kept constant, GeH_4 partial pressure was increased to further increase the lateral growth of Ge and thus improve the hole-filling behavior (see Figure 1). At the optimized growth condition of 750°C and 10T, an RMS surface roughness of 1.3 nm was obtained for 10x10μm AFM scans.

A recent study reports aspect-ratio trapping of dislocations in Ge grown on Si in narrow regions [3]. In larger-dimension structures, it has also previously been shown that the Ge threading dislocation density can be reduced by annealing the film after Ge growth [4]. For Ge SEG, cyclic annealing is more effective in reducing dislocation density as the diode size shrinks, and an etch pit density of ~$2x10^6$ cm^{-2} has been reported for square Ge mesas of sizes >18μm [4]. We have investigated the reduction of threading dislocation density in cyclic annealed Ge-on-Si for feature sizes less than 10μm using cross-sectional and plan-view transmission electron microscopy (TEM) imaging. The threading dislocation densities that were observed here by TEM are higher than those reported in [4], but the trend of decreasing dislocation density with feature size continues for Ge growth areas with widths less than 10 μm (see Figure 2). Further optimizing the annealing condition should enable improvements in Ge-on-Si material quality obtained in features with dimension less than 5 μm.



▲ Figure 1: (a) SEM images showing the reduction of Ge {311} faceting with the increase of temperature. (b) The optimized condition was used to grow Ge photodiode structures.



▲ Figure 2: Cross-sectional TEM images of SEG Ge structures with different widths. Ge film thickness is 0.8 μm. After growth the wafers were subjected to 4 cyclic anneals with minimum and maximum temperatures of 450 and 800°C. Dislocation density is significantly reduced for smaller features.

References

[1] F.X. Kärtner et al., "Photonic analog-to-digital conversion with electronic-photonic integrated circuits," in *Proc. SPIE*, vol. 6898, Feb. 2008, p. 689806.

[2] A. Talbot, J. Arcamone, C. Fellous, F. Deleglise, and D. Dutartre , "Investigation of facet formation in RTCVD Si/SiGe selective epitaxy," in *SiGe: Materials, Processing, and Devices*, D. Harame, Ed. New Jersey: The Electrochemical Society, Inc., 2004.

[3] J.-S. Park, J. Bai, M. Curtin, B. Adekore, M. Carroll, and A. Lochtefeld, "Defect reduction of selective Ge epitaxy in trenches on Si(001) substrates using aspect ratio trapping." *Applied Physics Letters*, vol. 90, Feb. 2007, p. 052113.

[4] H.-C. Luan, "Ge photodetectors for Si microphotonics," Ph.D. thesis, Massachusetts Institute of Technology, Cambridge, 2001.

6 Research Centers

Center for Integrated Circuits and Systems

Professor Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Six faculty members participate in the CICS: Hae-Seung Lee (director), Anantha Chandrakasan, Joel Dawson, David Perreault, Charles Sodini, and Vladimir Stojanovic. CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, and DC-DC converters, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. We are convinced that CICS is the conduit for such synergy. At present, participating companies include Agilent, Analog Devices, Bosch, Intel, IBM, Linear Technology, Marvell Technology Group, Maxim Integrated Products, Media Tek, National Semiconductor, NXP, Qualcomm, and Texas Instruments.

CICS's research portfolio includes all research projects that the seven participating faculty members conduct, regardless of source(s) of funding, with a few exceptions. (A very small number of projects have restrictions on information dissemination placed on them due to the nature of funding.)

Technical interaction between industry and MIT researchers occurs on both a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication between MIT faculty and students and industry. We hold two informal technical meetings per year open to participating companies. Throughout each full-day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet, giving early access to meeting attendees. Participating companies then offer valuable technical feedback, as well as suggestions for future research. We have held bi-annual meetings each year, and the response from industry has been overwhelmingly positive.

More intimate interaction between MIT researchers and industry takes place during work on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT. The result is truly synergistic, and we strongly believe that it will have a lasting impact on the field of integrated circuits and systems.

6 Research Centers

Intelligent Transporation Research Center

Dr. Ichiro Masaki, Director

Transportation is an important infrastructure for our society. It is time to propose a new transportation scheme for resolving the increasing transportation problems. In responding to social needs, MIT's Microsystems Technology Laboratories established the Intelligent Transportation Research Center (ITRC) in September 1998 as a contact point of industry, government, and academia for ITS research and development.

ITRC focuses on the key Intelligent Transportation Systems (ITS) technologies, including an integrated network of transportation information, automatic crash and incident detection, notification and response, advanced crash avoidance technology, advanced transportation monitoring and management, etc., in order to improve safety, security, efficiency, mobile access, and environment. There are two emphases for research conduced in the center:

- The integration of component technology research and system design research.
- The integration of technical possibilities and social needs.

ITRC proposes the incremental conversion and development process from current to near- and far-future systems and develops enabling key components in collaboration with the government, industries, and other institutions. Other necessary steps are the integration of technical, social, economical, and political aspects. The integration of the Intelligent Transportation Systems in different countries is also essential. The integration of vehicles, roads, and other modes of transportation, such as railways and public buses, is all imperative.

These integrations are fulfilled with the cooperation of researchers in various fields, including the Microsystems Technology Laboratory (MTL), the Research Laboratory of Electronics (RLE), the Artificial Intelligence Laboratory (AI), the Center for Transportation Studies (CTS), the Age Laboratory, the Department of Electrical Engineering and Computer Science, the Department of Civil and Environmental Engineering, the Department of Aeronautics and Astronautics, and the Sloan School of Management. The research center has 8 MIT faculty and several visiting professors and scientists. The director of the center is Dr. Ichiro Masaki.

6 Research Centers

MEMS@MIT

Professor Martin A. Schmidt, Director

The MEMS@MIT Center serves to unite the wide-ranging campus activities in micro/nano systems and MEMS with forward-looking industrial organizations. Currently, MEMS@MIT is composed of more than 150 faculty, students, and staff working on a broad research agenda and supported by more than $15 million/year in research sponsorship. The MEMS research efforts on campus focus on four overarching themes:

1) Materials, Processes, and Devices for MEMS - including work on piezoelectrics, magnetics, materials/package reliability, DRIE, wafer bonding, plastic fabrication, and printed MEMS

2) Biological and Chemical MEMS - includes cell manipulation, DNA and protein processing, biomolecule detection, medical sensors, microreactors, micro gas analyzers, and microfluidics

3) Actuators and Power MEMS - includeing switches, mirrors, pumps, turbines, fuel cells, thermophotovoltaics, chemical lasers, and energy harvesting

4) Sensors, Systems, and Modeling - includes wireless sensors, pressure sensing systems, and CAD for MEMS

Membership benefits include:

- Insight into newest ideas in MEMS
- Early access to research results
- Early awareness of IP generated for licensing
- Access to high-quality continuing education materials
- Partnering for federal or other funding opportunities
- Recruitment of leading MIT graduates

6 Research Centers

MIT Center for Integrated Photonic Systems

Professor Rajeev J. Ram, Director

The goals of the Center for Integrated Photonic Systems are:

1. To provide leadership and direction for research and development in photonics.

The core activity of CIPS is the development of a long-range vision for research and the development of integrated photonic devices and systems. CIPS will host forums and facilitate working groups with industrial consortium members to identify and discuss technology and road-mapping issues:

- technology directions
- potential disruptive technologies
- technical barriers (gaps)
- actions needed to enable future-generation systems, and
- manufacturing and market issues that drive timing of technology deployment.

As an academic institution we can work openly with a variety of different organizations in developing and gathering input for our models. Whether it is performance data for new devices "in the lab," yield data for existing manufacturing processes, planning documents, or first-hand observations of the corporate decision making process, CIPS researchers benefit greatly from the unique relationship between MIT and industry. The level of detail and intellectual rigor of the models being developed here is complemented by the high quality of data available to us. CIPS researchers are developing models of optical and electronic devices, the packages they are wrapped inside, the manufacturing processes that assemble them, the standards that define them, the market that buys them, and the policy processes that influence their deployment.

2. To foster an Institute wide community of researchers in the field of integrated photonics & systems.

The Departments of Electrical Engineering and Computer Science, Materials Science and Engineering, Mechanical Engineering and Economics are consistently ranked as the top graduate programs in the country. Likewise, the Sloan School of Management has consistently ranked first in the nation in the areas of information technology, operations research, and supply chain management. CIPS leverages MIT's strengths, by unifying the photonics researchers in these departments and laboratories to focus on technological developments in photonics. The combined volume of research funds in the photonics area at MIT exceeds $20 million dollars annually. The faculty and staff at MIT in photonics-related areas have included Claude Shannon (founder of information theory), Charles Townes (inventor of the laser), Robert Rediker (inventor of the semiconductor lasers), and Hermann Haus (inventor of the single-frequency semiconductor laser & ultrafast optical switch). CIPS-affiliated faculty and staff continue this tradition of excellence in areas ranging from optical network architectures, to novel optical devices, to novel photonic materials.

3. To integrate member companies into the MIT photonics community.

CIPS will host annual meetings and seminars in photonics. For CIPS member companies, focused visits to the Institute for individual companies will be organized with faculty and graduate students. In addition, CIPS will hold forums geared towards the creation of campus-industry teams to pursue large-scale research programs. CIPS will host poster sessions at the annual meeting so as to introduce graduate students and their research to industry. CIPS publications will include a resume book of recent graduate students in the area of photonics. Graduates of the Massachusetts Institute of Technology have founded 4,000 firms which, in 1994 alone, employed at least 1.1 million people and generated $232 billion of world sales. Photonics related companies founded by alumni include Sycamore Networks, Analog Devices, Texas Instruments, Hewlett-Packard, and 3Com as well as recent start-ups such as OmniGuide.

Member companies have the opportunity to guide the research of CIPS faculty and students through the Working Groups (WGs) and individual graduate student awards.

7 Faculty Research Staff & Publications

Akintunde I. (Tayo) Akinwande

Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

C. G. Sodini, MIT
V. Bulović, MIT
H.I. Smith, MIT
M.A. Schmidt, MIT
B.E. Gnade, UT Dallas
A.A. Seshia, University of Cambridge

RESEARCH STAFF

L.F. Velásquez-García, Res. Scientist, MTL
L.-Y. Chen, Post-Doc. Assc., MTL

GRADUATE STUDENTS

L.-Y. Chen, Res. Asst., EECS
K. Cheung, Res. Asst., EECS
M.A. Smith, Res. Asst., DMSE
A.I. Wang, Res. Asst., EECS

UNDERGRADUATE STUDENTS

Y. Niu, UROP, EECS

SUPPORT STAFF

C. Collins, Admin. Asst. II

PUBLICATIONS

L.F. Velásquez-García and A.I. Akinwande, "A PECVD CNT-based open architecture field ionizer for portable mass spectrometry," presented at the *IEEE MEMS 2008 Conference*, Tucson, AZ, Jan. 2008.

B. Gassend, L.F. Velásquez-García, A.I. Akinwande, and M. Martınez-Sanchez, "Fabrication of a fully integrated electrospray array with applications to space propulsion," presented at the *IEEE MEMS 2008 Conference*, Tucson, AZ, Jan. 2008.

I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C.G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 527-532, Feb. 2008.

L.F. Velásquez-García, B. Adeoti, Y. Niu, and A.I. Akinwande, "Uniform high current field emission of electrons from Si and CNF FEAs individually controlled by Si Pillar Ungated FETs," presented at the *IEEE International Electron Device Meeting*, 2007.

L.-Y. Chen, L.F. Velásquez-García, X. Wang, K. Teo, and A.I. Akinwande, "A Micro ionizer for portable mass spectrometers using double-gated isolated vertically aligned carbon nanofiber arrays," presented at the *IEEE International Electron Device Meeting*, 2007.

L.F. Velásquez-García, L.-Y. Chen and A.I. Akinwande, "Recent MEMS/NEMS activities at the Microsystems Technology Laboratories of MIT," presented at the *14th International Display Workshops,* Sapporo, Japan, Dec. 2007.

A. Wang, K. Ryu, J. Perkins, I. Nausieda, B. Yaglioglu, V. Bulović, C.G. Sodini, and A.I. Akinwande, "Near-room-temperature processed integrated metal oxide field effect transistor for large area electronics," *MRS 2007 Fall Meeting, Symposium, Large-Area Processing and Patterning for Active Optical and Electronic Devices*, Boston MA, USA, Nov. 2007.

B. Gassend, L.F. Velásquez-García, A.I. Akinwande, and M. Martınez-Sanchez, "A fully-integrated microfabricated externally-wetted electrospray thruster," presented at the *30th International Electric Propulsion Conference*, Florence, Italy, Sept. 2007.

L.F. Velásquez-García and A.I. Akinwande, "A MEMS CNT-based neutralizer for micro-propulsion applications," presented at the *30th International Electric Propulsion Conference*, Florence, Italy, Sept. 2007.

L.-Y. Chen, L.F. Velásquez-García, X. Wang, K. Cheung, K. Teo, and A.I. Akinwande, "Design, fabrication and characterization of double-gated vertically aligned carbon nanofiber field emitter arrays," *Technical Digest of the 20th International Vacuum Nanoelectronics Conference*, July 2007, pp. 82-83.

L.F. Velásquez-García, K. Cheung, and A.I. Akinwande, "Improvements on an out-of-plane MEMS quadrupole for portable mass spectrometry," *Technical Digest of the 20th International Vacuum Nanoelectronics Conference*, July 2007, pp. 2-3.

K. Cheung, L.F. Velásquez-García, and A.I. Akinwande, "First principles optimization of mass producible microscaled linear quadrupoles for operation in higher stability regions," *Technical Digest of the 20th International Vacuum Nanoelectronics Conference*, July 2007, pp. 214-215.

L.F. Velásquez-García, B.J. Adeoti, Y. Niu and A.I. Akinwande, "High density field emission arrays with current regulation using high aspect ratio si pillars," presented at the *20th International Vacuum Nanoelectronics Conference*, Chicago IL, July 2007.

B. Gassend, L.F. Velásquez-García, A.I. Akinwande, and M. Martınez-Sanchez, "A fully-integrated microfabricated externally-wetted electrospray thruster," in *Proc. AIAA 2007-5182, 43rd AIAA/ASME/SAE/ASEE Joint Propulsion Conference & Exhibit*, July 2007, Cincinnati, OH.

L.F. Velásquez-García and A.I. Akinwande, "An out-of-plane MEMS quadrupole for a portable mass spectrometer," in *Proc. International Solid-State Sensors, Actuators and Microsystems Conference*, Lyon, France, June 2007, pp. 2315-2320.

I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C.G. Sodini, "An organic imager for flexible large area electronics" *International Solid-State Circuits Conference 2007 Digest of Technical Papers*, Feb. 2007, pp. 72-73

Dimitri A. Antoniadis

Ray and Maria Stata Professor of Electrical Engineering
Department of Electrical Engineering and Computer Science

COLLABORATORS

T. Equi, FCRP Materials, Structures, and Devices Focus Center, Executive Director

GRADUATE STUDENTS

J. Hennessy, Res. Asst., EECS
A. Khakifirooz, Res. Asst., EECS
J-K. Lee, Res. Asst., EECS
O. Nayfeh, Res. Asst., EECS
A. Ritenour, Res. Asst., EECS

SUPPORT STAFF

W. Rokui, Admin. Asst. II

PUBLICATIONS

A. Khakifirooz and D.A. Antoniadis, "MOSFET performance scaling -- part I: historical trends," *IEEE Trans. Electron Devices*, vol. 55, no. 6, June 2008, to be published.

A. Khakifirooz and D.A. Antoniadis, "MOSFET performance scaling -- part II: future directions," *IEEE Trans. Electron Devices*, vol. 55, no. 6, June 2008, to be published.

A. Khakifirooz, A. Ritenour, J. Hennessy, and D.A. Antoniadis, "Investigation of poor carrier transport in germanium NFETs," presented at *IEEE Semiconductor Interface Specialists Conf.*, Dec. 2007.

A. Khakifirooz and D.A. Antoniadis, "Prospects of performance scaling for high-performance CMOS," to be presented at *European Solid-State Device Research Conf.*, 2008. (Invited)

O.M. Nayfeh, C. Ni Chleirigh, J.L. Hoyt, and D.A. Antoniadis, "Measurement of Enhanced Gate-Controlled Band-to-Band Tunneling in Highly Strained Silicon-Germanium Diodes," *IEEE Electron Device Letters*, 2008, to be published.

O.M. Nayfeh, and D.A. Antoniadis, "Calibrated Hydrodynamic Simulation of Well-Tempered Deeply-Scaled Nanowire Field Effect Transistors," in *Proc. IEEE Simulation of Semiconductor Processes and Devices Conference*, Vienna, Austria, Sept. 2007, pp. 305-308.

O.M. Nayfeh, D.A. Antoniadis, K. Mantey, and M.H. Nayfeh, "Memory Effects in Metal-Oxide-Semiconductor Capacitors Incorporating Dispensed Highly Monodisperse 1nm Si Nanoparticles," *Applied Physics Letters,* vol. 90, no. 15, pp. 153105:1-3, Apr. 2007.

O.M. Nayfeh, D.A. Antoniadis, K. Mantey, and M.H. Nayfeh, "Memory Effects in Metal-Oxide-Semiconductor Capacitors Incorporating Dispensed Highly Monodisperse 1nm Si Nanoparticles," in *Proc. Device Research Conference*, South Bend, IN, June 2007, pp. 219-220.

H.P. Yu, K L. Pey, W.K. Choi, M.K. Dawood, H.G. Chew, D.A. Antoniadis, E.A. Fitzgerald, and D.Z. Chi, "Effect of yttrium interlayer on Ni germanided metal gate workfunction in SiO_2/HfO_2," *IEEE Electron Device Letters,* vol. 28, no. 12, pp. 1098-1101, Dec. 2007.

H.P. Yu, K.L. Pey, W.K. Choi, D.A. Antoniadis, E.A. Fitzgerald, M.K. Dawood, K.Q. Ow and D.Z. Chi, "Full range workfunction tunning of MOSFETs using interfacial yttrium layer in fully germanided Ni gate," presented at *ECS 211th meeting*, Chicago, 2007.

Marc A. Baldo
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

T. Van Voorhis, MIT Dept of Chemistry
T. Swager, MIT Dept of Chemistry

POSTDOCTORAL ASSOCIATES

M. Segal
L. Theogarajan
S. Goffri

GRADUATE STUDENTS

J. Mapel, Res. Asst., EECS
K. Milaninia, Res. Asst., MSE
B.N. Limketkai, Res. Asst., EECS
M. Bora, Res. Asst., Physics
K. Celebi, Res. Asst., Physics
T. Heidel, Res. Asst., EECS
M. Currie, Res. Asst., EECS
P. Jadhav, Res. Asst., EECS
J. Lee, Res. Asst., EECS
C.L. Mulder, Res. Asst., EECS

SUPPORT STAFF

E. Moran, Admin. Asst. I

PUBLICATIONS

K. Celebi, T.D. Heidel, and M.A. Baldo, "Simplified calculation of dipole energy transport in a multilayer stack using dyadic Green's functions," *Optics Express*, vol. 15, no. 4, pp. 1762-1772, Feb. 2007.

J.K. Mapel, K. Celebi, M. Singh, and M.A. Baldo, "Plasmonic excitation of organic double heterostructure solar cells," *Applied Physics Letters*, vol. 90, no. 12, pp. 121102:1-3, Mar. 2007.

B.N. Limketkai, P. Jadhav, and M.A. Baldo, "Electric field dependent percolation model of charge carrier mobility in amorphous organic semiconductors," *Physical Review B*, vol. 75, no. 11, pp. 113203:1-4, Mar. 2007.

M. Bora, D. Schut, and M.A. Baldo, "Combinatorial detection of volatile organic compounds using metal-phthalocyanine field effect transistors," *Analytical Chemistry*, vol. 79, no. 9, pp. 3298-3303, May 2007.

M. Segal, M. Singh, K. Rivoire, S. Difley, T. Van Voorhis, and M.A. Baldo, "Extrafluorescent electroluminescence in organic light emitting devices," *Nature Materials*, vol. 6, no. 5, pp. 374-378, May 2007.

C.L. Mulder, K. Celebi, K.M. Milaninia, and M.A. Baldo, "Saturated and efficient blue phosphorescent organic light emitting devices with Lambertian angular emission," *Applied Physics Letters*, vol. 90, no. 15, pp. 211109:1-3, 2007.

T.D. Heidel, J.K. Mapel, K. Celebi, M. Singh, and M.A. Baldo, "Surface plasmon polariton mediated energy transfer in organic photovoltaic devices," *Applied Physics Letters*, vol. 91, no. 9, pp. 093506:1-3, Aug. 2007.

J. Chen, V. Leblanc, S.H. Kang, P.J. Benning, D. Schut, M.A. Baldo, M.A. Schmidt, and V. Bulović, "High definition digital fabrication of active organic devices by molecular jet printing," *Advanced Functional Materials*, vol. 17, no. 15, pp. 2722-2727, Oct. 2007.

T.D. Heidel, J.K. Mapel, K. Celebi, M. Singh, and M.A. Baldo, "Analysis of surface plasmon polariton mediated energy transfer in organic photovoltaic devices," in *Proc. SPIE*, San Diego, CA, Aug. 2007, vol. 6656, pp. 66560I:1-8.

Karl K. Berggren

Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

M. Bawendi, MIT
V. Bulović, MIT
S. Hamilton, Lincoln Laboratory
S. Harrer, TUM
A.J. Kerman, Lincoln Laboratory
T. Orlando, MIT
B. Robinson, Lincoln Laboratory
C. Ross, MIT
E. Thomas, MIT

POSTDOCTORAL ASSOCIATE

D. Morecroft, EECS

GRADUATE STUDENTS

V. Anant, Res. Asst., EECS
B. Cord, Res. Asst., EECS
E. Dauler, Res. Asst., EECS
X. Hu, Res. Asst., EECS
J. Leu, Res. Asst., EECS
D. Winston, Res. Asst., EECS
J. Yang, Res. Asst., EECS

UNDERGRADUATE STUDENTS

A. Chao, UROP
C. Herder, UROP
James White, UROP

VISITING STUDENTS

J. Kupec, TUM

SUPPORT STAFF

T. Kuhn, Admin. Asst.
J. Daley, Project Technician, NSL
M. Mondol, Facility Manager,SEBL
L. LaForce, Shop Helper, NSL

PUBLICATIONS

A.J. Kerman, E.A. Dauler, J.K.W. Yang, K.M. Rosfjord, K.K. Berggren, G. Gol'tsman, and B. Voronov, "Constriction-limited detection efficiency of superconducting nanowire single-photon detectors," *Applied Physics Letters,* vol. 90, no. 10, pp. 101110:1-3, Mar. 2007.

J.C. Lee, W.D. Oliver, K.K. Berggren, and T.P. Orlando, "Nonlinear resonant behavior of a dispersive readout circuit for a superconducting flux qubit," *Physical Review B,* vol. 75, no. 14, pp. 144505:1-10, Apr. 2007.

E. Dauler, B.S. Robinson, A.J. Kerman, J.K.W. Yang, K.M. Rosfjord, V. Anant, B. Voronov, G. Gol'tsman, and K.K. Berggren, "Multi-element superconducting nanowire single-photon detector," *IEEE Transactions on Applied Superconductivity,* vol. 17, no. 2, pt. 1, pp. 279-284, June 2007.

J.K.W. Yang, A.J. Kerman, E.A. Dauler, V. Anant, K.M. Rosfjord, and K.K. Berggren, "Modeling the electrical and thermal response of superconducting nanowire single-photon detectors," *IEEE Transactions on Applied Superconductivity,* vol. 17, no. 2, pt. 1, pp. 581-585, June 2007.

S. Harrer, J. Yang, G.A. Salvatore. K.K. Berggren, F. Ilievski, and C.A. Ross, "Pattern generation by using multi-step room-temperature nanoimprint lithography," *IEEE Transactions on Nanotechnology,* vol. 6, no. 6, pp. 639-644, Nov. 2007.

B. Cord, J. Lutkenhaus and K.K. Berggren, "Optimal temperature for development of poly(methylmethacrylate)," *Journal of Vacuum Science and Technology B,* vol. 25, no. 6, pp. 2013-2016, Nov. 2007.

J.K.W. Yang and K.K. Berggren, "Using high-contrast salty development of hydrogen silsesquioxane for sub-10-nm half-pitch lithography," *Journal of Vacuum Science and Technology B,* vol. 25, no. 6, pp. 2025-2029, Nov. 2007.

Sangeeta N. Bhatia

Professor
Harvard-MIT Division of Health Sciences & Technology
Department of Electrical Engineering and Computer Science

COLLABORATORS

C. Chen, UPenn
B. Engelward, MIT Biological Eng.
T. Golub, Broad Institute
C. Marcus, Harvard
L. Mahadevan, Harvard University
D. Melton, Harvard University
E. Ruoslahti, Burnham Institute
M. Sailor, UCSD
R. Sasisekharan, MIT
P. Sharp, MIT
J. Shah, Harvard
S. Suresh, MIT
K. Van Vliet, MIT
R. Weissleder, HMS

GRADUATE STUDENTS

A. Chen, Res. Asst., HST
T. Harris, Res. Asst., HST
G. von Maltzahn, Res. Asst., HST
S. Mittal, Res. Asst., EECS
J. Shan, Res. Asst., HST
Y. Ren, MD/PhD, HST

SUPPORT STAFF

S. Kangiser, Admin. Asst. II
S. Katz, Laboratory Manager
E. Loveday, Technical Assistant

PUBLICATIONS

J.H. Park, G. von Maltzahn, M.P. Schwartz, E. Ruoslahti, S.N. Bhatia, M.J. Sailor, "Magnetic iron oxide nanoworms for tumor targeting and imaging," *Advanced Materials*, vol. 20, no. 9, pp. 1630-1635, May 2008.

S.R. Khetani and S.N. Bhatia, "Microscale human liver tissue for drug development," *Nature Biotechnology*, vol. 26, no. 1, pp. 120-126, Jan. 2008.

A.M. Derfus, A.A. Chen, D.H. Min, E. Ruoslahti, and S.N. Bhatia, "Targeted quantum dot conjugates for siRNA delivery," *Bioconjugate Chemistry*, vol. 18, no. 5, pp. 1391-1396, Sept. 2007.

J.M. Higgins, D.T. Eddington, S.N. Bhatia, and L. Mahadevan, "Sickle-cell vasoocclusion and rescue in a microfluidic device," *Proc. National Academy of Sciences*, vol. 104, no. 51, pp. 20496-20500, Dec. 2007.

A.M. Derfus, G. von Maltzahn, T.J. Harris, T. Duza, K.S. Vecchio, E. Ruoslahti, and S.N. Bhatia, "Remotely triggered release from magnetic nanoparticles," *Advanced Materials*, vol. 19, pp. 3932-3936, 2007.

G. von Maltzahn, T.J. Harris, J.H. Park, A.J. Schmidt, M.J. Sailor, and S.N. Bhatia, "Nanoparticle self-assembly gated by logical proteolytic triggers," *Journal of the American Chemical Society*, vol. 129, pp. 6064-6065, 2007.

E.E. Hui and S.N. Bhatia, "Micromechanical control of cell-cell interactions," *Proc. National Academy of Sciences*, vol. 104, pp. 5722-5726, 2007.

V. Liu Tsang, A.A. Chen, L.M. Cho, K.D. Jadin, R.L. Sah, S. DeLong, J.L. West, and S.N. Bhatia, "Fabrication of 3D hepatic tissues by additive photopatterning of cellular hydrogels," *FASEB Journal,* vol. 21, pp. 790-801, 2007.

S.R. Khetani and S.N. Bhatia, "Engineering tissues for in vitro applications," *Current Opinion in Biotechnology*, vol. 17, pp. 524-531, 2006.

D.R. Albrecht, G.H. Underhill, T.B. Wassermann, R.L. Sah, and S.N. Bhatia, "Probing the role of multicellular organization in 3D microenvironments," *Nature Methods,* vol. 3, pp. 369-375, Apr. 2006.

T.J. Harris, G. von Maltazhn, A.M. Derfus, E. Rouslahti, and S.N. Bhatia, "Proteolytic actuation of nanoparticle self-assembly," *Agnewandte Chemie International Edition,* vol. 41, no. 19, pp. 3161-3165, 2006.

J.H. Park, A.M. Derfus, E. Segal, K.S. Vecchio, S.N. Bhatia, and M.J. Sailor, "Local heating of discrete droplets using magnetic porous silicon-based photonic crystals," *Journal of the American Chemical Society*, vol. 128, no. 24, pp. 7938-7946, 2006.

M.P. Schwartz, A.M. Derfus, S.D. Alvarez, S.N. Bhatia, and M.J. Sailor, "The smart petri dish: A nanostructured photonic crystal for real-time monitoring of living cells," *Langmuir*, vol. 22, pp. 7084-7090 2006.

C. Flaim, S. Chien, and S.N. Bhatia, "An extracellular matrix microarray for probing cellular differentiation," *Nature Methods,* vol. 2, no. 2, pp. 119-125, 2005.

A.A. Chen, A.M. Derfus, S.R. Khetani and S.N. Bhatia, "Quantum dots to monitor RNAi delivery and improve gene silencing," *Nucleic Acids Research,* vol. 33, no. 22, p. e190, 2005.

J.W. Allen, S.R. Khetani and S.N. Bhatia, "*In vitro* zonation and toxicity in a hepatocyte bioreactor," *Toxicological Sciences,* vol. 84, pp. 110-119, Mar. 2005.

J. Dorvee, A.M. Derfus, S.N. Bhatia and M.J. Sailor, "Manipulation of liquid droplets using amphiphilic, magnetic 1-D photonic crystal chaperones," *Nature Materials,* vol. 3, no. 12, pp. 896-899, Dec. 2004.

V. Chin, S. Sanga, P. Taupin, J. Scheel, F.G. Gage, and S.N. Bhatia, "A microfabricated platform for studying stem cell fates," *Biotechnology and Bioengineering,* vol. 88, no. 3, pp. 399-415, Mar. 2004.

D. Albrecht, R. Sah and S.N. Bhatia, "Geometric and material determinants of patterning efficiency by dielectrophoresis," *Biophysical Journal,* vol. 87, no. 4, pp. 2131-2147, Apr. 2004.

S. Khetani, G. Szulgit, J. Del Rio, C. Barlow, and S.N. Bhatia, "Exploring mechanisms of stromal-epithelial cell interactions using gene expression profiling," *Hepatology,* vol. 40, no. 3, pp. 545-554, Aug. 2004.

Duane S. Boning

Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

S.F. Yoon, NTU, Singapore

GRADUATE STUDENTS

K. Balakrishnan, Res. Asst., EECS
A. Chang, Res. Asst., EECS
N. Drego, Res. Asst., EECS (co-supervised with Prof. A.P. Chandrakasan)
W. Fan, Res. Asst., EECS
D. Lim, Res. Asst., EECS
A. Farahanchi, Res. Asst., EECS
J. Johnson, Res. Asst., EECS
H. Taylor, Res. Asst., EECS

VISITING SCIENTISTS

J. Lee, Samsung
E. Paul, Stockton College

SUPPORT STAFF

S. Blake, Admin. Asst. II

PUBLICATIONS

H.T. Pham, S.F. Yoon, K.P. Chen, and D.S. Boning, "Characterization of carbon-doped InSb diode grown by molecular beam epitaxy," *Journal of Physics D: Applied Physics*, vol. 41, no. 2, pp. 025304:1-6, Jan. 2008.

H.K. Taylor and D. S. Boning, "Diffraction-based approaches to the *in-situ* measurement of dimensional variations in components produced by thermoplastic micro- and nano-embossing," presented at the *5th International Symposium on Nanomanufacturing*, Singapore, Jan. 2008.

Z.G. Xu, S G. Li, S.F. Yoon, Z.P. Fang, K. Youcef-Toumi, D.J. Burns, V. Shilpiekandula, H.K. Taylor, and D.S. Boning, "Complete surface distinguishing and overlapping technology for three-dimensional image processing of micro devices," presented at the *5th International Symposium on Nanomanufacturing*, Singapore, Jan. 2008.

Z. Li, D. Truque, D. Boning, R. Caramto, and C. Borst, "Modeling wafer level uniformity in electrochemical-mechanical polishing (ECMP)," presented at the *Advanced Metallization Conference*, Albany, NY, Oct. 2007.

D.S. Boning, "Modeling of chip-scale pattern dependencies in interconnect fabrication processes," presented at the *Advanced Metallization Conference*, Albany, NY, Oct. 2007.

H.K. Taylor, B. Chen, C. Iliescu, and D.S. Boning, "Computationally efficient modeling of pattern dependencies in the micro-embossing of thermoplastic polymers,"presented at the *33rd International Conference on Micro- and Nano-Engineering, Copenhagen*, Denmark, Sept. 2007.

H.K. Taylor, Z. Xu, L. Shiguang, K. Youcef-Toumi, Y.S. Fatt, and D.S. Boning, "Moire fringe method for the measurement of distortions of hot-embossed polymeric substrates," presented at the *9th International Symposium on Laser Metrology*, Singapore, June-July 2008.

D.S. Boning, "Chip-scale modeling of CMP and plating processes," presented at the *Fourth International Copper Interconnect Technology Symposium*, Fudan University, Shanghai, China, May 2007. Also at Tsinghua University, Beijing, China, May 2007.

K.O. Abrokwah, P.R. Chidambaram, and D.S. Boning, "Pattern based prediction for plasma etch," *IEEE Transactions on Semiconductor Manufacturing*, vol. 20, no. 2, pp. 77-86, May 2007.

H.T. Pham, S.F. Yoon, K.H. Tan, and D.S. Boning, "Effects of nitrogen incorporation in $InSb_{1-x}N_x$ grown using radio frequency plasma-assisted molecular beam epitaxy," *Applied Physics Letters*, vol. 90, no. 9, pp. 092115:1-3, Mar. 2007.

V. Michael Bove, Jr.
Principal Research Scientist
Media Arts and Sciences Program/Media Laboratory

COLLABORATORS
W. J. Plesniak, Brigham and Women's Hospital

POSTDOCTORAL ASSOCIATES
Q. Smithwick, MIT Media Laboratory

GRADUATE STUDENTS
J. Barabas, Res. Asst., MAS
D. Smalley, Res. Asst., MAS
A. L. Santos, Res. Asst., MAS
B. Taylor, Res. Asst., MAS

SUPPORT STAFF
K. Hall, Admin. Asst. II

PUBLICATIONS

S.A. Benton and V. M. Bove. Jr., *Holographic Imaging.* New York: Wiley, 2008.

Q.Y. Smithwick, D.E. Smalley, V.M. Bove, Jr., and J. Barabas, "Progress in holographic video displays based on guided-wave acousto-optic devices," in *Proc. SPIE Practical Holography XXII: Materials and Applications,* San Jose, CA, 2008, vol. 6912, pp. 69120H:1-10.

J. Kalanithi and V.M. Bove, Jr., "Connectibles: Tangible social networks," presented at the *Proc. 2nd International Conf. on Tangible and Embedded Interaction (TEI '08), 2008.*

D.E. Smalley, Q.Y.J. Smithwick, and V. M. Bove, Jr., "Holographic video display based on guided-wave acousto-optic devices," in *Proc. SPIE Practical Holography XXI,* San Jose, CA, 2007, vol. 6488, pp. 64880L:1-7.

W. Plesniak, M. Halle, V.M. Bove, Jr., J. Barabas, and R. Pappu, "Reconfigurable image projection (RIP) holograms," *Optical Engineering*, vol. 45, no. 11, pp. 115801:1-15, Nov. 2006.

V.M. Bove, Jr., W.J. Plesniak, T. Quentmeyer, and J. Barabas, "Real-time holographic video images with commodity PC hardware," in *Proc. SPIE Stereoscopic Displays and Virtual Reality Systems XII,* San Jose, CA, 2005, vol. 5664, pp. 255-262.

D. Butler, V.M. Bove, Jr., and S. Sridharan, "Real-time adaptive foreground/background segmentation," *EURASIP Journal on Applied Signal Processing,* vol. 14, no. 11, pp. 2292-2304, Aug. 2005.

B.C. Dalton and V.M. Bove, Jr., "Audio-based self-localization for ubiquitous sensor networks," in *Proc. 118th Audio Engineering Society Convention,* Barcelona, Spain, 2005.

Vladimir Bulović

Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

A.I. Akinwande, MIT
M.A. Baldo, MIT
M. Bawendi, MIT
P. Benning, HP
T. Bloomstein, Lincoln Laboratory
M. Chaparala, HP
F. Jaworski, Raytheon
P. Mardilovich, HP
A. Nurmikko, Brown Univ.
D. Schut, HP
M.A. Schmidt, MIT
C.G. Sodini, MIT
T. Swager, MIT

POSTDOCTORAL ASSOCIATES

J. Chen
C. Madigan
M. Panzer
J. Tischler
B. Yaglioglu

GRADUATE STUDENTS

H. Abdu, Res. Asst., EECS
G. Akselrod, Res. Asst., Physics
P. Anikeeva, Res. Asst., DMSE
A. Arango, Res. Asst., EECS
S. Bradley, Res. Asst., EECS
D. Friend, Res. Asst., EECS
J. Ho, Res. Asst., EECS
Q. Hu, Res. Asst., Harvard Univ.
J. Leu, Res. Asst., EECS
I. Nausieda, Res. Asst., EECS
T. Osedach, Res. Asst., Harvard Univ.
S. Paydavosi, Res. Asst, EECS
J. Rowehl, Res. Asst, DMSE
Y. Shirasaki, Res. Asst., EECS
H. Tang, Res. Asst., EECS
V. Wood, Res. Asst., EECS
J. Yu, Res. Asst., EECS

SUPPORT STAFF

L. Kim, Asst.
M. Pegis, Admin. Asst. II

PUBLICATIONS

J. Ho, A. Arango and V. Bulović, "Lateral organic bi-layer heterojunction photoconductors," *Applied Physics Letters*, 2008, to be published.

J. Yu and V. Bulović, "Using integrated optical feedback to counter pixel aging and stabilize light output of organic LED display technology," *IEEE Journal of Display Technology*, 2008, to be published.

C. Madigan, E. Howe, V. Bulović, P. Mardilović, and P. Kornilovitch, "Planarization in electrochemically fabricated nanodimensional films," *Journal of Physical Chemistry C*, vol. 112, no. 19, pp. 7318-7325, May 2008.

J.M. Caruge, J.E. Halpert, V. Wood, V. Bulović, and M.G. Bawendi, "Colloidal quantum-dot light-emitting diodes with metal-oxide charge transport layers," *Nature Photonics*, vol. 2, no. 4, pp. 247-250, Apr. 2008.

I. Nausieda, K. Ryu, I. Kymissis, A. Akinwande, V. Bulović, and C.G. Sodini, "An organic active-matrix imager," *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 527-532, Feb. 2008.

H. Huang, A. Dorn, G.P. Nair, V. Bulović, and M.G. Bawendi, "Bias-induced photoluminescence quenching of single colloidal quantum dots embedded in organic semiconductors,"*Nano Letters*, vol. 7, no. 12, pp. 3781-3786, Dec. 2007.

J.L. Chen, V. Leblanc, S.H. Kang, P.J. Benning, D. Schut, M.A. Baldo, M.A. Schmidt, and V. Bulović, "High definition digital fabrication of active organic devices by molecular jet printing," *Advanced Functional Materials*, vol. 17, no. 15, pp. 2722-2727, Oct. 2007.

Q. Zhang, T. Atay, J.R. Tischler, M.S. Bradley, V. Bulović, and A.V. Nurmikko, "Highly efficient resonant coupling of optical excitations in hybrid organic/inorganic semiconductor nanostructures," *Nature Nanotechnology,* vol. 2, no. 9, pp. 555-559, Sept. 2007.

P.O. Anikeeva, J.E. Halpert, M.G. Bawendi, and V. Bulović, "Electroluminescence from a mixed red-green-blue colloidal quantum dot monolayer," *Nano Letters*, vol. 7, no. 8, pp. 2196-2200, Aug. 2007.

J. Yu and V. Bulović, "Micropatterning metal electrode of organic light emitting devices using rapid polydimethylsiloxane lift-off," *Applied Physics Letters,* vol. 91, no. 4, pp. 043102:1-3, July 2007.

J.R. Tischler, M.S. Bradley, Q. Zhang, T. Atay, A. Nurmikko, and V. Bulović, "Solid state cavity QED: Strong coupling in organic thin films," *Organic Electronics,* vol. 8, no. 2-3, pp. 94-113, Apr.-June 2007.

V. Bulović and C. Adachi, eds, "Special issue on coupled states of excitons, photons, and plasmons in organic structures," *Organic Electronics,* vol. 8, no. 2-3, pp. 77-292, Apr.-June 2007.

V. Leblanc, J.L. Chen, S.H. Kang, V. Bulović, and M.A. Schmidt, "Micromachined printheads for the evaporative patterning of organic materials and metals," *Journal of Microelectromechanical Systems,* vol. 16, no. 2, pp. 394-400, Apr. 2007.

C. Madigan and V. Bulović, "Exciton energy disorder in polar amorphous organic thin films: Monte Carlo calculations," *Physical Review B*, vol. 75, no. 8, pp. 081403:1-4, Feb. 2007.

H. Huang, A. Dorn, V. Bulović, and M.G. Bawendi, "Electrically driven light emission from single colloidal quantum dots at room temperature," *Applied Physics Letters*, vol. 90, no. 2, pp. 023110:1-3, Jan. 2007.

Anantha P. Chandrakasan

Joseph F. & Nancy P. Keithley Professor of Electrical Engineering
Department of Electrical Engineering and Computer Science

GRADUATE STUDENTS

M. Bhardwaj, Res. Asst., EECS
J. Bohorquez, Res. Asst., EECS (co-supervised with Prof. J.L. Dawson)
F. Chen, Res. Asst., EECS (co-supervised with Prof. V. Stojanović)
H.W. Chung, Res. Asst., EECS
D. Daly, Res. Asst., EECS
N. Drego, Res. Asst., EECS (co-supervised with Prof. D. Boning)
D. Finchelstein, Res. Asst., EECS
N. Ickes, Res. Asst., EECS
J. Kwong, TI Fellowship, Res. Asst., EECS
P. Lajevardi, Res. Asst., (co-supervised with Prof. H. Lee)
K-J. Lee, Res. Asst., EECS (co-supervised with Prof. J. Kong)
P. Mercier, Res. Asst., EECS
M. Qazi, Res. Asst., EECS
Y. Ramadass, Res. Asst., EECS
C. Schmitt, Res. Asst., EECS
M. Sinangil, Res. Asst., EECS
V. Sze, Res. Asst., EECS
N. Verma, Intel Fellowship, Res. Asst., EECS
M. Yip, Res. Asst., EECS

UNDERGRADUATE STUDENTS

H. Liang
L. Tian
T. Wen

VISITING STUDENT

Y. Koken

SUPPORT STAFF

M. Flaherty, Senior Admin. Asst.

PUBLICATIONS

J.L. Bohorquez, J.L. Dawson, and A.P. Chandrakasan, "A 350μW CMOS MSK transmitter and 400μW OOK super-regenerative receiver for medical implant communications," *IEEE Symposium on VLSI Circuits*, pp. 32-33, June 2008.

A.P. Chandrakasan, D.C. Daly, J. Kwong, and Y.K. Ramadass, "Next generation micro-power systems," *IEEE Symposium on VLSI Circuits*, pp. 2-5, June 2008.

B.P. Ginsburg and A.P. Chandrakasan, "The mixed signal optimum energy point: Voltage and parallelism," *ACM/IEEE Design Automation Conference*, Anaheim, CA, pp. 244-249, June 2008.

P.P. Mercier, D.C. Daly, and A.P. Chandrakasan, "A 19pJ/pulse UWB transmitter with dual capacitively-coupled digital power amplifiers," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, pp. 47-50, June 2008.

P.P. Mercier, D.C. Daly, M. Bhardwaj, D.D. Wentzloff, F.S. Lee, and A.P. Chandrakasan, "Ultra-low-power UWB for sensor network applications," *IEEE International Symposium on Circuits and Systems*, May 2008, pp. 2562-2565.

N. Verma and A.P. Chandrakasan, "A high-density 45nm SRAM using small-signal non-strobed regenerative sensing," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2008, pp. 380-381,

J. Kwong, Y. Ramadass, N. Verma, M. Koesler, K. Huber, H. Moormann, and A.P. Chandrakasan, "A 65nm sub-V_t microcontroller with integrated SRAM and switched-capacitor DC-DC converter," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2008, pp. 318-319.

B.P. Ginsburg and A.P. Chandrakasan, "Highly interleaved 5b 250MS/s ADC with redundant channels in 65nm CMOS," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2008, pp. 240-241.

D.C. Daly and A.P. Chandrakasan, "A 6-bit, 0.2V to 0.9V highly digital flash ADC with comparator redundancy,"in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2008, pp. 554-555.

N. Verma, J. Kwong, and A.P. Chandrakasan, "Nanometer MOSFET Variation in minimum energy subthreshold circuits," *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 163-174, Jan. 2008.

N. Verma and A.P. Chandrakasan, "A 256 kb 65 nm 8T subthreshold SRAM employing sense-amplifier redundancy," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 141-149, Jan. 2008.

Y.K. Ramadass and A.P. Chandrakasan, "Minimum energy tracking loop with embedded DC-DC converter enabling ultra-low-voltage operation down to 250 mV in 65 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 1, pp. 256-265, Jan. 2008.

F.S. Lee and A.P. Chandrakasan, "A 2.5 nJ/bit 0.65 V pulsed UWB receiver in 90 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, pp. 2851-2859, Dec. 2007.

F. Chen, A. Joshi, V. Stojanović, and A.P. Chandrakasan, "Scaling and evaluation of carbon nanotubes for VLSI applications," presented at the *2nd International Conference on Nano-Networks*, Sept. 2007.

M. Bhardwaj and A.P. Chandrakasan, "Coding under observation constraints," presented at the *45th Allerton Conference on Communications, Control and Computing*, Sept. 2007.

D.D. Wentzloff, F. S. Lee, D.C. Daly, M. Bhardwaj, P.P. Mercier, A.P. Chandrakasan, "Energy efficient pulsed-UWB CMOS circuits and systems," presented at the *IEEE International Conference on Ultra-Wideband (ICUWB)*, Sept. 2007.

T.S. Cho, K.-J. Lee, J. Kong, A.P. Chandrakasan, "A Low power carbon nanotube chemical sensor system," in *Proc. IEEE Custom Integrated Circuits Conference*, San Jose, CA, Sept. 2007, pp. 181-184.

V. Sze and A.P. Chandrakasan, "A 0.4-V UWB baseband processor," in *Proc. IEEE International Symposium Low Power Electronics and Design*,Portland, OR, pp. 262-267, Aug. 2007.

Y. Ramadass and A.P. Chandrakasan, "Voltage scalable switched capacitor DC-DC converter for ultra-low-power on-chip applications," in *Proc. IEEE Power Electronics Specialists Conference*, Orlando, FL, pp. 2353-2359, June 2007.

N. Verma and A.P. Chandrakasan, "An Ultra Low Energy 12-bit Rate-Resolution Scalable SAR ADC for Wireless Sensor Nodes," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 6, pp. 1196-1205, June 2007.

Luca Daniel
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

A. Megretski, MIT
J. White, MIT

GRADUATE STUDENTS

B. Bond, Res. Asst., EECS
T.A. El Moselhy, Res. Asst., EECS
X. Hu, Res. Asst., EECS
K.C. Sou, Res. Asst., EECS

SUPPORT STAFF

C. Collins, Admin. Asst.

PUBLICATIONS

T. Moselhy and L. Daniel, "Stochastic Integral Equation Solver for Efficient variation aware interconnect extraction," presented at the *IEEE/ACM Design Automation Conference*, Anaheim, CA, June 2008.

K.C. Sou, A. Megretski and L. Daniel, "A quasi-convex optimization approach to parameterized model order reduction," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 27, no. 3, pp. 456-469, Mar. 2008.

B.N. Bond and L. Daniel, "A piecewise-linear moment-matching approach to parameterized model-order reduction for highly nonlinear systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 26 , no. 12, pp. 2116-2129, Dec. 2007.

K.C. Sou, A. Megretski, L. Daniel, "Bounding L2 gain system error due to approximations of the nonlinear vector field," in *Proc. IEEE Conference on Computer-Aided Design*, San Jose, Nov. 2007, pp. 879-886.

B. Bond and L. Daniel, "Stabilizing schemes for piecewise-linear reduced order models via projection and weighting functions," in *Proc. IEEE Conference on Computer-Aided Design*, San Jose, Nov. 2007, pp. 860-867 (Best Paper Award Nomination).

T. Moselhy and L. Daniel, "Stochastic high order basis functions for volume integral equation with surface roughness," in *Proc. IEEE Conference on Electrical Performance of Electronic Packaging*, San Jose, CA, Oct. 2007, pp. 73-76 (Best Student Paper Award Nomination).

X. Hu, T. Moselhy, J. White, and L. Daniel, "Optimization-based Wideband Basis Functions for Efficient Interconnect Extraction," in *Proc. IEEE Conference on Design Automation and Test in Europe*, Nice, France, Apr. 2007, pp. 1-6.

T. Moselhy , X. Hu, and L. Daniel, "pFFT in FastMaxwell: A fast impedance extraction solver for 3D conductor structures over substrate," in *Proc. IEEE Conference on Design Automation and Test in Europe*, Nice, France, Apr. 2007, pp. 1-6 (Best Paper Award Nomination).

Joel L. Dawson

Carl Richard Soderberg Career Development Professor of Power Engineering
Department of Electrical Engineering and Computer Science

GRADUATE STUDENTS

J. Bohorquez, Res. Asst., EECS
S. Chung, Res. Asst., EECS
P. Godoy, Res. Asst., EECS
T. Khanna, Res. Asst., EECS
O. Ogunnika, Res. Asst., EECS
S. Rayanakorn, Res. Asst., EECS
W. Sanchez, Res. Asst., EECS

SUPPORT STAFF

S. Piccarini, Admin. Asst. II

PUBLICATIONS

S. Chung, J.W. Holloway, and J.L. Dawson, "Open-loop digital predistortion using Cartesian feedback for adaptive RF power amplifier linearization," to be presented at *IEEE MTT-S International Microwave Symposium*, Honolulu, HI, June 2007.

A. Hadiashar and J.L. Dawson, "A chopper stabilized CMOS analog multiplier with ultra-low DC offsets," in *Proc. IEEE European Solid-State Circuits Conference*, Montreux, Switzerland, Sept. 2006, pp. 364-367.

J.L. Dawson and T.H. Lee, "Cartesian feedback for RF power amplifier linearization," in *Proc. American Control Conference*, Boston, MA, July 2004, pp. 361-366.

J.L. Dawson and T.H. Lee, "Automatic phase alignment for a fully integrated Cartesian feedback power amplifier system," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 12, pp. 2269-2279, Dec. 2003.

J.L. Dawson and T.H. Lee, "Automatic phase alignment for a fully integrated CMOS Cartesian feedback power amplifier system," in *IEEE International Solid-State Circuits Conference Digest*, San Francisco, CA, Feb. 2003, pp. 262-263.

J.L. Dawson, S.P. Boyd, M. Hershenson, and T.H. Lee, "Optimal allocation of local feedback in multistage amplifiers via geometric programming," *IEEE Transactions on Circuits and Systems I*, vol 48, no. 1, pp. 1-11, Jan. 2001.

J.L. Dawson and T.H. Lee, "Automatic phase alignment for high bandwidth Cartesian feedback power amplifiers," in *Proc. IEEE Radio and Wireless Conference*, Denver, CO, Sept. 2000, pp. 71-74.

J.L. Dawson, S.P. Boyd, M. Hershenson, and T.H. Lee, "Optimal allocation of local feedback in multistage amplifiers via geometric programming," in *Proc. 43rd Midwest Symposium on Circuits and Systems*, Lansing, MI, Aug. 2000, pp. 530-533.

Jesús A. del Alamo

Donner Professor, MacVicar Faculty Fellow
Department of Electrical Engineering and Computer Science

COLLABORATORS

P.C. Chao, BAE Systems
D. Greenberg, IBM
K. Hayashi, Mitsubishi Electric
T. Hisaka, Mitsubishi Electric
A. Inoue, Mitsubishi Electric
T. Ishida, Mitsubishi Electric
J. Jimenez, Triquint Semic
A. Valdes, MIT
E. Piner, Nitronex

VISITING SCIENTISTS

Y. Ikura, Fuji Electric

POSTDOCTORAL FELLOW

D. H. Kim
N. Waldron

GRADUATE STUDENTS

U. Gogineni, Res. Asst., EECS
J. Joh, Res. Asst., EECS
A. Villanueva, Res. Asst., EECS
L. Xia, Res. Asst., EECS
S. Demirtas, Res. Asst., EECS

UNDERGRADUATE STUDENTS

A. Ojeda, EECS

SUPPORT STAFF

E. Kubicki, Admin. Asst. II

PUBLICATIONS

A.A. Villanueva, J.A. del Alamo, T. Hisaka, K. Hayashi, and M. Somerville, "Degradation uniformity of RF power GaAs PHEMTs under electrical stress," *IEEE Transactions on Device and Materials Reliabiltiiy, Special Issue on III-V Compound Semiconductor Device Reliability*, 2008, to be published.

T. Hisaka, Y. Nogami, H. Sasaki, N. Yoshida, K. Hayashi, A. Villanueva, and J.A. del Alamo, "Degradation mechanism of AlGaAs/InGaAs power pseudomorphic high-electron-mobility transistors under large-signal operation," *Japanese Journal of Applied Physics*, vol. 47, no. 2, pp. 833-838, 2008.

J. Joh and J.A. del Alamo, "Critical voltage for electrical degradation of GaN high electron mobility transistors," *IEEE Electron Device Letters*, vol. 29, no. 4, pp. 287-289, April 2008.

P. Saunier, C. Lee, J. Jimenez, A. Balistreri, H. Dumka, H. Q. Tserng, M. Y. Kao, U. Chowdhury, P. C. Chao, K. Chu, A. Souzis, I. Eliashevich, S. Guo, J. del Alamo, J. Joh, and M. Shur, "Progress in GaN devices, performance and reliability," presented at the *SPIE Photonics West Conference*, San Jose, CA, Jan. 20-24, 2008.

D.-H. Kim and J.A. del Alamo, "Impact of lateral engineering on the logic performance of sub-50 nm InGaAs HEMTs," presented at the *2007 International Semiconductor Device Symposium*, College Park, MD, Dec. 12-14, 2007.

J.A. del Alamo, "CMOS extension via III-V compound semiconductors," presented at the *2007 IEEE International Electron Devices Meeting*, Washington, DC, Dec. 2007.

A.A. Villanueva, J.A. del Alamo, T. Hisaka, and R. Ishida, "Drain corrosion in RF power GaAs PHEMTs," in *Proc. 2007 IEEE International Electron Devices Meeting, Washington*, DC, Dec., 2007, pp. 389-392.

J. Joh and J.A. del Alamo, "Gate current degradation mechanisms of GaN high electron mobility transistors," in *Proc. 2007 IEEE International Electron Devices Meeting*, Washington, DC, Dec.2007, pp. 385-388.

D.-H. Kim and J.A. del Alamo, "Logic Performance of 40 nm InAs HEMTs," in *Proc. 2007 IEEE International Electron Devices Meeting*, Washington, DC, Dec. 2007, pp. 629-632.

N. Waldron, D.-H. Kim, and J.A. del Alamo, "90 nm self-aligned InGaAs HEMT for logic applications," in *Proc. 2007 IEEE International Electron Devices Meeting,* Washington, DC, Dec. 2007, pp. 633-636.

D.-H. Kim, J.A. del Alamo, J.-H. Lee, and K.-S. Seo, "Logic suitability of 50 nm In0.7Ga0.3As HEMTs for beyond-CMOS applications," *IEEE Transactions on Electron Devices,* vol. 54, no. 10, pp. 2606-2613, Oct. 2007.

J. Joh and J.A. del Alamo, "Effects of temperature on electrical degradation of GaN high electron mobility transistors," in *Proc. 7th International Conference on Nitride Semiconductors*, Las Vegas, NV, Sept. 2007, p. 39.

J.H. Fischer, Mitchell, R., and J.A. del Alamo, "Inquiry-learning with WebLab: Undergraduate attitudes and experiences," *Journal of Science Education and Technology*, vol. 16, no. 4, pp. 337-348, Aug. 2007.

J.A. del Alamo and D.-H. Kim, "Beyond CMOS: Logic suitability of InGaAs HEMTs," Invited paper. *2007 Indium Phosphide & Related Materials Conference*, Matsue, Japan, May 2007, pp. 51-54.

Clifton G. Fonstad, Jr.
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

Y.S. Fatt, Nanyang Techno-logical University, Singapore
F.J Cadieu, Queens College of CUNY
C.S. Jin, National University of Singapore
S. Prasad, Northeastern U.
M. Zahn, MIT

GRADUATE STUDENTS

S. Faminini, Res. Asst., EECS
J. Perkins, Res. Asst., EECS
J. Rumpler, Res. Asst., EECS

UNDERGRADUATE STUDENTS

D. Cheng, EECS
J. Diaz, EECS

SUPPORT STAFF

M. Pegis, Admin. Asst II

PUBLICATIONS

C.G. Fonstad, J.J. Rumpler, E.R. Barlkley, J.M. Perkkns, and S. Famenini, "Recess integration of mirco-cleaved laser diode platelets with dielectric wave-guides on silicon," in *Proc. of the Novel In-plane Semiconductor Lasers Conference VII, Photonics West 2008*, SPIE Conference Proc. vol. 6909, Jan. 2008. Invited paper.

P.A. Postigo, F. Suarez, A. Sanz-Heras, J. Sangrador, and C.G. Fonstad, "Growth of InP on GaAs(001) by hydrogen-assisted low-temperature solid-source molecular beam epitaxy," *Journal of Applied Physics*, vol. 103, no. 1, pp. 013508:1-5, Jan. 2008.

J.M. Perkins and C.G. Fonstad, "Low threshold VCSELs recess-integrated on Si-CMOS ICs," *Technical Digest of CLEO 2007*, May 2007, to be published.

E.R. Barkley, J.J. Rumpler, J.M. Perkins, S. Famenini, and C.G. Fonstad, Jr., "Co-axial integration of micro-cleaved ridge wave-guide gain elements with SiOxNy waveguides on silicon," in *Proc. of WOCS-DICE 2007*, Venice, Italy, May 2007, to be published.

J.M. Perkins and C.G. Fonstad, "Full recess integration of small diameter low threshold VCSELs within Si-CMOS ICs," in review.

J.J. Rumpler, and C.G. Fonstad, "Continuous-wave electrically pumped ridge laser on silicon" in review.

Silvija Gradečak

Merton C. Flemings Assistant Professor of Materials Science & Engineering
Department of Materials Science and Engineering

COLLABORATORS

L. Allard, Oak Ridge NL
K. Berggren, EECS
T. Buonassisi, ME
T. Palacios, EECS
Y. Shao-Horn, ME
E. Thomas, MSE

GRADUATE STUDENTS

M. Brewster, Res. Asst., MSE
S. K. Lim, Res. Asst., MSE
M. Smith, Res. Asst., MSE
M. Tambe, Res. Asst., MSE

UNDERGRADUATE STUDENT

A. Reading, Res. Asst., MSE

VISITING STUDENT

C.-H. Tseng, National Cheng Kung University, Taiwan

SUPPORT STAFF

J. Brittan, Admin. Asst. II

PUBLICATIONS

S.K. Lim, M.J. Tambe, M.M. Brewster, and S. Gradečak, "Controlled growth of ternary alloy nanowires using metalorganic chemical vapor deposition," *Nano Letters*, vol. 8, no. 5, pp. 1386-1392, May 2008.

Y. Li, J. Xiang, F. Qian, S. Gradečak, Y. Wu, H. Yan, D.A. Blom, and C. M. Lieber, "Dopant-free GaN/AlN/AlGaN radial nanowire heterostructures as high electron mobility transistors," *Nano Letters*, vol. 6, no. 7, pp. 1468-1473, July 2006.

F. Qian, S. Gradečak, Y. Li, C.Y. Wen, and C.M. Lieber, "Core/multishell nanowire heterostructures as multicolor, high-efficiency light-emitting diodes" *Nano Letters*, vol. 5, no. 11, pp. 2287-2291, Nov. 2005.

S. Gradečak, F. Qian, Y. Li, H.G. Park, and C.M. Lieber, "GaN nanowire lasers with low lasing thresholds," *Applied Physics Letters*, vol. 87, no. 17, pp. 173111: 1-3, Oct. 2005.

P.V. Radovanovic, C.J. Barrelet, S. Gradečak, F. Qian, and C.M. Lieber, "General synthesis of manganese-doped II-VI and III-V semiconductor nanowires," *Nano Letters*, vol. 5, no. 7, pp. 1407-1411, July 2005.

J. Dorsaz, J.F. Carlin, S. Gradečak, and M. Ilegems, "Progress in AlInN-GaN Bragg reflectors: Application to a microcavity light emitting diode," *Journal of Applied Physics*, vol. 97, no. 8, pp. 084505: 1-6, Apr. 2005.

B. Lukic, J.W. Seo, E. Couteau, K. Lee, S. Gradečak, R. Berkecz, K. Hernadi, S. Delpeux, T. Cacciaguerra, F. Béguin, A. Fonseca, J.B. Nagy, G. Csányi, A. Kis, A.J. Kulik, and L. Forró, "Elastic modulus of multi-walled carbon nanotubes produced by catalytic chemical vapour deposition," *Applied Physics A*, vol. 80, no. 4, pp. 695-700, Feb. 2005.

S. Gradečak, P. Stadelmann, V. Wagner, and M. Ilegems, "Bending of dislocations in GaN during epitaxial lateral overgrowth," *Applied Physics Letters*, vol. 85, no. 20, pp. 4648-4650, no. 16, Nov. 2004.

F. Qian, Y. Li, S. Gradečak, D.L. Wang, C. J. Barrelet, and C.M. Lieber, "Gallium nitride-based nanowire radial heterostructures for nanophotonics," *Nano Letters*, vol. 4, no. 10., pp. 1975-1979, Oct. 2004.

D.C. Bell, Y. Wu, C.J. Barrelet, S. Gradečak, J. Xiang, B.P. Timko, and C.M. Lieber, "Imaging and analysis of nanowires," *Microscopy Research And Technique*, vol. 64, no. 5-6, pp. 373-389, Aug. 2004.

J. Napierala, D. Martin, H.J. Buhlmann, S. Gradečak, and M. Ilegems, "GaN laterally overgrown on sapphire by low pressure hydride vapor phase epitaxy," *Materials Science Forum*, Part 2 , vol. 457-460, pp. 1581-1584, June 2004.

J. Dorsaz, J.F. Carlin, C.M. Zellweger, S. Gradečak, and M. Ilegems, "InGaN/GaN resonant-cavity LED including an AlInN/GaN Bragg mirror," *Physica status solidi A*, vol. 201, no. 12, pp. 2675-2678, Jan. 2004.

V. Wagner, O. Parillaud, H.J. Buhlmann, M. Ilegems, S. Gradečak, and P. Stadelmann, "Influence of the carrier gas composition on morphology, dislocations and microscopic luminescence properties of selectively grown GaN by HVPE," *Journal of Applied Physics*, vol. 92, no. 3, pp. 1307-1316, Aug. 2002.

S. Gradečak, V. Wagner, M. Ilegems, T. Riemann, J. Christen, and P. Stadelmann, "Microscopic evidence of point defect incorporation in laterally overgrown GaN," *Applied Physics Letters*, vol. 80, pp. 2866-2868, Apr. 2002.

J.C. Lasjaunias, M. Saint-Paul, A. Bilsic, A. Smontara, S. Gradečak, A.M. Tonejc, A. Tonejc, and N. Kitamura, "Acoustic and thermal transport properties of hard carbon formed from C60 fullerene," *Physical Review B*, vol. 66, no. 1, pp. 014302:1-11, July 2002.

A. Smontara, A.M. Tonejc, S. Gradečak, A. Tonejc, A. Bilusic, and J.C. Lasjaunias, "Structural (XRD and HRTEM) investigations of fullerite C60 and C70 samples," *Materials Science and Engineering C*, vol. *19*, no. 1-2, pp. 21-25, Jan. 2002.

Jongyoon Han
Associate Professor
Department of Electrical Engineering and Computer Science / Biological Engineering

COLLABORATORS

S. Tannenbaum, BE, MIT
S. Manalis, BE, MIT
P. Doyle, ChemE, MIT
M. Rubner, DMSE, MIT
R. Cohen, ChemE, MIT
T.-S. Kim, KIST, Korea
N. Hadjiconstantinou, ME, MIT
Y. Chen, NUS, Singapore
N.-T. Nguyen, NTU, Singapore

GRADUATE STUDENTS

P. Mao, Res. Asst., ME
H. Bow, Res. Asst., EECS
P. Dextras, Res. Asst., BE
V. Liu, Res. Asst., EECS
L. Li, Res. Asst., EECS / HST
L.F. Cheow, Res. Asst., EECS
A. Sarkar, Res. Asst., EECS

RESEARCH STAFF

Y. Song, Ph.D.
J. Lee, Ph.D.
S. Kim, Ph.D.
M. Yamada, Ph. D.

SUPPORT STAFF

S. Chafe, Admin. Asst.

PUBLICATIONS

S. Chung, J.H. Lee, M.-W. Moon, J. Han, and R.D. Kamm, "Non-lithographic wrinkle nanochannels for protein preconcentration," *Advanced Materials*, 2008, to be published.

J.H. Lee, Y.-A. Song, S.R. Tannenbaum, and J. Han, "Enhanced reaction kinetics and sensitivity of low-abundance enzyme assay using micro/nanofluidic preconcentration chip," *Analytical Chemistry*, 2008, to be published.

S.J. Kim and J. Han, "Self-sealed vertical polymeric nanoporous-junctions for high-throughput nanofluidic applications," *Analytical Chemistry*, 2008, to be published.

J. Lee, Y.A. Song and J. Han, "Multiplexed proteomic sample preconcentration device using surface-patterned ion-selective membrane," *Lab on a Chip*, vol. 8, no. 4, pp. 596-601, Apr. 2008.

Y.C. Wang and J. Han, "Pre-binding dynamic range and sensitivity enhancement for immuno-sensors using nanofluidic preconcentrator," *Lab on a Chip*, vol. **8**, no. 3, pp. 392-394, Mar. 2008.

Z.R. Li, G.R. Liu, Y.Z. Chen, J.-S. Wang, H. Bow, Y. Cheng, and J. Han, "Continuum transport model of Ogston sieving in patterned nanofilter arrays for rod-like biomolecule separation," *Electrophoresis*, vol. 29, no. 2, pp. 329–339, Jan. 2008.

R.B. Schoch, L.F. Cheow and J. Han, "Electrical detection of fast reaction kinetics in nanochannels with an induced flow," *Nano Letters*, vol. 7, no. 12, pp. 3895-3900, Dec. 2007.

Y.-C. Wang, V. Liu, and J. Han, "Nanofluidic preconcentration device for sensitive and wide dynamic range immuno-sensing," in *Proc. μTAS 2007 Symposium*, Paris, France, Oct. 2007, pp. 1786-1788.

J.-H. Lee, Y.-A. Song, and J. Han, "High-throughput proteomic sample preconcentration in PDMS microfluidic chip using surface-patterned ion-selective membrane," in *Proc. μTAS 2007 Symposium*, Paris, France, Oct. 2007, pp. 1198-1200.

Y.-A. Song, C. Celio, and J. Han, "Continuous-flow pi-based sorting of proteins and peptides for isolation of basic pi range molecules," in *Proc. μTAS 2007 Symposium*, Paris, France, Oct. 2007, pp. 811-813.

J.H. Lee, S. Chung, S.J. Kim, J. Han, "Novel PDMS based protein preconcentration using junction gap breakdown phenomenon," *Analytical Chemistry*, vol. 79, no. 17, pp. 6868 -6873, Sept. 2007.

S.J. Kim, Y.-C. Wang, J.H. Lee, H. Jang, and J. Han, "Concentration Polarization and Nonlinear Electrokinetic Flow near Nanofluidic Channel," *Physical Review Letters*, vol. 99, no. 4, pp. 044501:1-4, July 2007.

H.-W. Shim, J.-H. Lee, T.-S. Hwang, Y.W. Rhee, Y.M. Bae, J. Choi, J. Han, and C.-S. Lee, "Patterning of proteins and cells on functionalized surfaces prepared by polyelectrolyte multilayers and micromolding in capillaries," *Biosensors and Bioelectronics*, vol. 22, no. 12, pp. 3188–3195, June 2007.

D.-H. Duc, J.-S. Wang, G.R. Liu, Y.Z. Chen, J. Han, and G. Hadjiconstantinou, "Dissipative particle dynamics simulations of electroosmotic flow in nano-fluidic devices," *Microfluidics and Nanofluidics*, vol. 4, no. 3, pp. 219-225, Mar. 2007

J. Fu, R.B. Schoch, A.L. Stevens, S.R. Tannenbaum, and J. Han, "Patterned anisotropic nanofluidic sieving structure for continuous-flow separation of DNA and protein," *Nature Nanotechnology*, vol. 2, no. 2, pp. 121-128, Feb. 2007.

J. Han, J. Fu, and R.B. Schoch, "Molecular sieving using nanofilters: Past, present and future," *Lab on a Chip*, vol. 7, no. 1, pp. 23-33, Jan. 2007.

R.B. Schoch, J. Han, and P. Renaud, "Transport phenomena in nanofluidics," *Reviews of Modern Physics*, 2007, to be published.

Judy L. Hoyt
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

D. Antoniadis, EECS
K. Berggren, EECS
F. Kartner, EECS
R. Ram, EECS
V. Stojanović, EECS
M. Canonico, Freescale
T. Lyszczarz, MIT Lincoln Laboratory
J. Yoon, MIT Lincoln Laboratory

GRADUATE STUDENTS

N. DiLello, EECS
L. Gomez, EECS
P. Hashemi, EECS
M. Kim, DMSE

RESEARCH STAFF

G. Riggott, Research Specialist

SUPPORT STAFF

M. Hudak, Admin. Asst. II

PUBLICATIONS

L. Gomez, M. Canonico, M. Kim, P. Hashsmi, and J.L. Hoyt, "Fabrication of Strained-Si/Strained-Ge Heterostructures on Insulator," *Journal of Electronic Materials*, vol. 37, no. 3, pp. 240-244, Mar. 2008.

P. Hashemi, L. Gomez, J.L. Hoyt, M.D. Robertson, and M. Canonico, "Asymmetric strain in nano-scale patterned strained-Si/strained-Ge/strained-Si heterostructures on insulator," *Applied Physics Letters*, vol. 91, no. 8, pp. 083109:1-3, Aug. 2007.

L. Gomez, I. Aberg, and J.L. Hoyt, "Electron Transport in strained-silicon directly oninsulator ultrathin-body n-MOSFETs with body thickness ranging from 2 to 25 nm," *IEEE Electron Device Letters*, vol. 28, no. 4, pp. 285-287, Apr. 2007.

G. Xia, J.L. Hoyt and M. Canonico, "Si-Ge interdiffusion in strained Si/strained SiGe heterostructures and implications for enhanced mobility metal-oxide-semiconductor field-effect transistors," *Journal of Applied Physics*, vol. 101, no. 4, pp. 044901:1-11, Feb. 2007.

T. Barwicz, H. Byun, F. Gan, C.W. Holzwarth, M.A. Popovic, P.T. Rakich, M.R. Watts, E.P. Ippen, F.X. Kartner, H.I. Smith, J.S. Orcutt, R.J. Ram, V. Stojanović, O.O. Olubuyide, J.L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, J.U. Yoon, "Silicon photonics for compact, energy-efficient interconnects," *Journal of Optical Networking*, vol. 6, no. 1, pp. 63-73, Jan. 2007.

G. Xia, M. Canonico, and J.L. Hoyt, "Interdiffusion in strained Si/strained SiGe epitaxial heterostructures," *Semiconductor Science and Technology,* vol. 22, no. 1, pp. S55-S58, Jan. 2007.

C. Ní Chléirigh, X. Wang, G. Rimple, Y. Wang, M. Canonico, N. D. Theodore, O. O. Olubuyide and J. L. Hoyt, "Laser spike annealing of strained Si/ strained Si 0.3Ge 0.7/ relaxed Si 0.7Ge 0.3 dual channel high mobility p-MOSFETs," *ECS Transactions*, vol. 3, no. 2, pp. 355-362, Oct., 2006.

C. Ní Chléirigh, O.O. Olubuyide and J.L. Hoyt, "Influence of strained $Si_{1-y}Ge_y$ Layer thickness and composition on hole mobility enhancement in heterostructure p-MOSFETs with Ge Contents y from 0.7 to 1.0," *ECS Transactions*, vol. 3, no. 7, pp. 963-972, Oct. 2006.

D.A. Antoniadis, A. Khakifirooz, I. Aberg, and J.L. Hoyt, "Channel material innovations for continuing the historical MOSFET performance increase with scaling," *ECS Transactions*, vol. 3, no. 3, pp. 3-15, Oct. 2006.

G. Xia, O.O. Olubuyide, J.L. Hoyt, and M. Canonico, "Strain dependence of Si- Ge interdiffusion in epitaxial Si/Si1-yGey/Si heterostructures on relaxed Si1-xGex substrates," *Applied Physics Letters*, vol. 88, pp. 13507:1-3, Jan. 2006.

D.A. Antoniadis, I. Aberg, C. Ní Chléirigh, O.M. Nayfeh, A. Khakifirooz, and J.L. Hoyt, "Continuous MOSFET performance increase with device scaling: The role of strain and channel material innovations," *IBM Journal of Research & Development*, vol. 50, no. 4/5, pp. 363 – 375, July/Sept. 2006.

G. Xia, M. Canonico, and J.L. Hoyt, "Interdiffusion in SiGe/Si Heterostructures," *2006 International SiGe Technology and Device Meeting*, May, 2006, pp. 286-287.

O.O. Olubuyide, D.T. Danielson, L.C. Kimerling, and J.L. Hoyt, "Impact of seed layer on material quality of epitaixal germanium on silicon deposited by low pressure chemical vapor deposition," *Thin Solid Films*, vol. 508, pp. 14-19, 2006.

I. Aberg, C. Ní Chléirigh, and J.L. Hoyt, "Ultrathin-body strained-Si and SiGe heterostructure-on-insulator MOSFETs," *IEEE Transactions on Electron Devices*, pp. 1021 - 1029, May 2006.

G. Xia, O.O. Olubuyide, J.L. Hoyt, and M. Canonico, "Strain dependence of Si-Ge interdiffusion in epitaxial Si/$Si_{1-y}Ge_y$/Si heterostructures on relaxed $Si_{1-x}Gex$ substrates," *Applied Physics Letters*, vol. 88, pp. 13507:1-3, 2006.

F.X. Kärtner, S. Akiyama, G. Barbastathis, T. Barwicz, H. Byun, D.T. Danielson, F. Gan, F. Grawert, C.W. Holzwarth, J.L. Hoyt, E.P. Ippen, M. Kim, L.C. Kimerling, J. Liu, J. Michel, O.O. Olubuyide, J.S. Orcutt, M. Park, M. Perrott, M.A. Popovic, P.T. Rackich, R.J. Ram, H.I. Smith, and M.R. Watts, "Electronic photonic integrated circuits for high speed, high resolution, analog to digital conversion," in *Proc. SPIE*, vol. 6125, pp. 612503:1-14, Jan. 2006.

Qing Hu
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

J.L. Reno, Sandia National Lab.

POSTDOCTORAL ASSOCIATE

S. Kumar, RLE

GRADUATE STUDENTS

A. Lee, Res. Asst., EECS
Qi Qin, Res. Asst., EECS
Allen Hsu, Res. Asst., EECS
Wilt Kao, Res. Asst., EECS
David Burghoff, Res. Asst., EECS

SUPPORT STAFF

C. Bourgeois, Admin. Asst.

PUBLICATIONS

A.W.M. Lee, Q. Qin, S. Kumar, B. S. Williams, Q. Hu, and J.L. Reno, "High-power and high-temperature THz quantum-cascade lasers based on lens-coupled metal-metal waveguides," *Optics Letters*, vol. 32, no, 9, pp. 2840-2842, Oct. 2007.

S. Kumar, B.S. Williams, Q. Qin, A.W.M. Lee, Q. Hu, and J.L. Reno, "Surface-emitting distributed feedback terahertz quantum-cascade lasers in metal-metal waveguides," *Optics Express*, vol. 15, no. 1, pp. 113-128, Jan. 2007.

A.W.M. Lee, B.S. Williams, S. Kumar, Q. Hu, and J.L. Reno, "Real-time imaging using a 4.3-THz quantum cascade laser and a 320×240 microbolometer focal-plane array," *IEEE Photonics Technology Letters*, vol. 18, no. 3, pp. 1415-1417, July 2006.

A. Baryshev, J.N. Hovenier, A.J.L. Adam, I. Kasalynas, J.R. Gao, T.O. Klaassen, B.S. Williams, S. Kumar, Q. Hu, and J. L. Reno, "Phase locking and spectral linewidth of a two-mode terahertz quantum cascade laser," *Applied Physics Letters*, vol. 89, no. 3, pp. 031115:1-3, July 2006.

B.S. Williams, S. Kumar, Q. Qin, Q. Hu, and J.L. Reno, "Terahertz quantum cascade lasers with double resonant-phonon depopulation," *Applied Physics Letters*, vol. 88, no. 26, pp. 261101:1-3, June 2006.

A.W.M. Lee, Q. Qin, S. Kumar, B.S. Williams, Q. Hu, and J.L. Reno, 'Real-time terahertz imaging over a standoff distance (>25 meters)," *Applied Physics Letters*, vol. 89, no. 14, pp. 141125:1-3, Oct. 2006.

B.S. Williams, S. Kumar, Q. Hu, and J.L. Reno, "High-power terahertz quantum-cascade lasers," *Electronics Letters*, vol. 42, no. 2, pp. 89-91, Jan. 2006. *Compound Semiconductor*, p. 32, Mar. 2006.

S. Kumar, B. S. Williams, Q. Hu, and J. L. Reno, "1.9-THz quantum-cascade lasers with one-well injector," *Applied Physics Letters*, vol. 88, no, 12, pp. 121123:1-3, Mar. 2006.

E.E. Orlova, J.N. Hovenier, T.O. Klaassen, I. Kasalynas, A.J.L. Adam, A. Baryshev, J. R. Gao, T.M. Klapwijk, B.S. Williams, S. Kumar, Q. Hu, and J.L. Reno, "Antenna model for wire lasers," *Physical Review Letters*, vol. 96, pp. 173904:1-3, 2006.

A.J.L. Adam, I. Kašalynas, J.N. Hovenier, T.O. Klaassen, J.R. Gao, E.E. Orlova, B.S. Williams, S. Kumar, Q. Hu, and J.L. Reno, "Beam pattern of terahertz quantum cascade lasers with sub-wavelength cavity dimensions," *Applied Physics Letters*, vol. 88, no. 15, pp. 151105:1-3, Apr. 2006.

H.C. Liu, H. Luo, D. Ban, M. Wächter, C.Y. Song, Z.R. Wasilewski, M. Buchanan, G.C. Aers, A.J. Spring Thorpe, J.C. Cao, S.L. Feng, B.S. Williams, and Q. Hu, "Terahertz semiconductor quantum well devices," *Proc. of SPIE: Materials and Nanostructures*, vol. 6029, pp. 602901:1-10, Jan. 2006.

Klavs F. Jensen
Warren K. Lewis Professor and Department Head
Department of Chemical Engineering

COLLABORATORS

M.G. Bawendi, MIT
S. Buchwald, MIT
T. Jamison, MIT
K. Gleason, MIT
D. Nocera, MIT
M.A. Schmidt, MIT
T. Swager, MIT
C.A. Wang, Lincoln Laboratory

POSTDOCTORAL ASSOCIATES

A. Adamo, ChemE
K. Deshpande, ChemE
R. Hartman, Chem. E
S. Marre, ChemE
J. Wen, ChemE

GRADUATE STUDENTS

J.Baek, Res. Asst., ChemE
L. Chao, Res. Asst., ChemE
V. Dydek, Res. Asst., ChemE
J. Keybl, Res. Asst., ChemE
P. Heider, Res. Asst., ChemE
J. Mcmullen, Res. Asst., ChemE
J. Moore, Res. Asst., ChemE
K. Nagy, Res. Asst., ChemE
J. Rempel, Res. Asst., ChemE
H. Sahoo, Res. Asst., ChemE
M. Sultana, Res. Asst., ChemE
L. Ye, Res. Asst., ChemE
N. Zaborenko, Res. Asst., ChemE

SUPPORT STAFF

A. Haverty, Admin. Asst.

PUBLICATIONS

J.W. Albrecht, J. El-Ali, and K.F. Jensen, "Cascaded free-flow isoelectric focusing for improved focusing speed and resolution," *Analytical Chemistry*, vol. 79, no. 24, pp. 9364-9371, Dec. 2007.

T.F. Hill, L.F. Velásquez-García, B.A. Wilhite, W.T. Rawlins, S. Lee, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator – Part II: Experimental exploration of the performance space," *Journal of Microelectromechanical Systems*, vol. 16, no. 6, pp. 1492-1505, Dec. 2007.

L.F. Velásquez-García, B.A. Wilhite, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator – Part I: Device fabrication and proof of concept demonstration," *Journal of Microelectromechanical Systems*, vol. 16, no. 6, pp. 1482-1491, Dec. 2007.

D.J. Quiram, K.F. Jensen, M.A. Schmidt, P.L. Mills, J.F. Ryley, M.D. Wetzel, and D.J. Kraus, "Integrated microreactor system for gas-phase catalytic reactions. 3. Microreactor system design and system automation," *Industrial & Engineering Chemistry Research*, vol. 46, no. 25, pp. 8319-8335, 2007.

D.J. Quiram, K.F. Jensen, M.A. Schmidt, P.L. Mills, J.F. Ryley, M.D. Wetzel, and D.J. Kraus, "Integrated microreactor system for gas-phase catalytic reactions. 2. Microreactor packaging and testing," *Industrial & Engineering Chemistry Research*, vol. 46, no. 25, pp. 8306-8318, Dec. 2007.

D.J. Quiram, K.F. Jensen, M.A. Schmidt, P.L. Mills, J.F. Ryley, M.D. Wetzel, and D.J. Kraus, "Integrated microreactor system for gas-phase catalytic reactions. 1. Scale-up microreactor design and fabrication," *Industrial & Engineering Chemistry Research*, vol. 46, no. 25, pp. 8292-8305, Dec. 2007.

E.R. Murphy, T. Inoue, H.R. Sahoo, N. Zaborenko, and K.F. Jensen, "Solder-based chip-to-tube and chip-to-chip packaging for microfluidic," *Lab on a Chip*, vol. 7, no. 10, pp. 1309-1314, Oct. 2007.

S.A. Khan and K.F. Jensen, "Microfluidic synthesis of titania shells on colloidal silica," *Advanced Materials*, vol. 19, no. 18, pp. 2556-2560, Sept. 2007.

H.R. Sahoo, J.G. Kralj, and K.F. Jensen, "Multi-step continuous flow microchemical synthesis involving multiple reactions and separations," *Angewandte Chemie International Edition*, vol. 46, no. 30, pp. 5704-5708, July 2007.

Z. Zhang, G. Perozziello, P. Boccazzi, A.J. Sinskey, O. Geschke, and K.F. Jensen, "Microbioreactors for bioprocess development," *Journal of the Association for Laboratory Automation*, vol. 12, no. 3, pp. 143-151, June 2007.

E.R. Murphy, J.R. Martinelli, N. Zaborenko, S.L. Buchwald, and K.F. Jensen, "Accelerating reactions with microreactors at elevated temperature and pressures: profiling aminocarbonylation reactions," *Angewandte Chemie International Edition*, vol. 46, no. 10, pp. 1734-1737, Feb. 2007.

T. Inoue, M.A. Schmidt, and K.F. Jensen, "Microfabricated multiphase reactors for the direct synthesis of hydrogen peroxide from hydrogen and oxygen," *Industrial & Engineering Chemistry Research*, vol. 46, no. 4, pp. 1153-1160, Feb. 2007.

H.-G. Choi, J.P. Amara, T.P. Martin, K.K. Gleason, T.S. Swager, and K.F. Jensen, "Directed growth of poly(isobenzofuran) films by chemical vapor deposition on patterned self-assembled monolayers as templates," *Langmuir*, vol. 23, no. 5, pp. 2483-2491, Feb. 2007.

L.R. Arana, N. de Mas, R. Schmidt, A.J. Franz, M.A. Schmidt, and K.F. Jensen, "Isotropic etching of silicon in fluorine gas for MEMS micromachining," *Journal of Micromechanics and Microengineering*, vol. 17, no. 2, pp. 384-392, Feb. 2007.

K.F. Jensen, "Microchemical systems for discovery and development," in *New Avenues to Efficient Chemical Synthesis - Emerging Technologies*, P.H. Seeberger and T. Blume, eds. New York, NY: Springer, 2007.

Rohit Karnik
Assistant Professor
Department of Mechanical Engineering

COLLABORATORS
G. Barbastathis, MIT
S. K. Das, IIT Madras
O. C. Farokhzad, Harvard
J. M. Karp, Harvard
S-G. Kim, MIT
R. Langer, MIT

GRADUATE STUDENTS
P. Basto, Res. Asst., HST
S. Bose Res. Asst., MechE
M. Raafat, Res. Asst., MechE
Yi-Heng Sen, Res. Asst., MechE
P. Valencia, Res. Asst., ChemE

SUPPORT STAFF
D. Hanna, Admin. Asst II

PUBLICATIONS

R. Karnik, "Microfluidic mixing," in *Encyclopedia of Micro- and Nano-Fluidics*, D. Li, ed., New York: Springer (in press, 2008).

R. Karnik, S. Hong, H. Zhang, Y. Mei, D. Anderson, J. Karp, and R. Langer, "Nanomechanical control of cell rolling in two dimensions through surface patterning of receptors," *Nano Letters*, vol. 8, no. 4, pp. 1153-1158, Apr. 2008.

F. Gu, R. Karnik, A.Z. Wang, F. Alexis, E. Levy-Nissenbaum, S. Hong, R.S. Langer, and O.C. Farokhzad, "Targeted nanoparticles for cancer therapy," *Nano Today*, vol. 2, no. 3, pp. 14-21, June 2007.

R. Karnik, C. Duan, K. Castelino, and A. Majumdar, "Rectification of ionic transport in a nanofluidic diode," *Nano Letters*, vol. 7, no. 2, pp. 547-551, Feb. 2007.

R. Karnik, K. Castelino, C. Duan, and A. Majumdar, "Diffusion-limited patterning of molecules in nanofluidic channels," *Nano Letters*, vol. 6, no. 8, pp. 735-1740, Aug. 2006.

M.-C. Lu, S. Satyanarayana, R. Karnik, A. Majumdar, and C.-C. Wang, "Mechanical-electrokinetic battery by using a nanoporous membrane," *Journal of Micromechanics and Microengineering*, vol. 16, no. 4, pp. 667-675, Apr. 2006.

R. Karnik, K. Castelino, and A. Majumdar, "Field-effect control of protein transport in a nanofluidic transistor circuit," *Applied Physics Letters*, vol. 88, no. 12, pp. 123114:1-3, Mar. 2006.

K. Dunphy, R. Karnik, J. Newman,and A. Majumdar, "Spatially controlled microfluidics using low-voltage electrokinetics," *Journal of Microelectromechanical Systems*, vol. 15, pp. 237-245, Feb. 2006.

A. Liau, R. Karnik, A. Majumdar, and J. Doudna-Cate, "Mixing crowded biological solutions in milliseconds," *Analytical Chemistry*, vol. 77, pp. 7618-7625, Dec. 2005.

R. Karnik, K. Castelino, R. Fan, P. Yang, and A. Majumdar, "Effects of biological reactions and modifications on conductance of nanofluidic channels," *Nano Letters*, vol. 5, no. 9, pp. 1638-1642, Sept. 2005.

R. Fan, R. Karnik, M. Yue, D. Li, A. Majumdar, and P. Yang, "DNA translocation in inorganic nanotubes," *Nano Letters*, vol. 5, no. 9, pp. 1633-1637, Sept. 2005.

R. Fan, M. Yue, R. Karnik, D. Li, A. Majumdar, and P. Yang, "Polarity switching and transient responses in single nanotube nanofluidic transistors," *Physical Review Letters*, vol. 95, no. 8, pp. 086607:1-4, Aug. 2005.

R. Karnik, R. Fan, M. Yue, D. Li, P. Yang, and A. Majumdar, "Electrostatic control of ions and molecules in nanofluidic transistors," *Nano Letters,* vol. 5, no. 5, pp. 943-948, May 2005.

K. Dunphy, R. Karnik, C. Trinkle, and A. Majumdar, "Analysis of governing parameters of silver-silver chloride electrodes in microfluidic electrokinetic devices," *Microscale Thermophysical Engineering*, vol. 9, no. 2, pp. 199-211, Apr.-June 2005.

S. Satyanarayana, R.N. Karnik, and A. Majumdar, "Stamp-and-stick room-temperature bonding technique for microdevices," *Journal of Microelectromechanical Systems*, vol. 14, no. 2, pp. 392-399, Apr. 2005.

Ali Khademhosseini

Assistant Professor of Medicine and Health Science and Technology
Division of Health Science and Technology

COLLABORATORS

R. Liao, BWH, HMS
R. Maas, HMS, BWH, HST
R.S. Langer, HMS, CHB, MIT
U. Demirci, HMS, BWH
J. Burdick, Univ. of Pennsylvania
E. Jabbari, Univ. of South Carolina
J.W. Hong, Auburn Univ.
S. Lee, Korea Univ.
K.Y. Suh, Seoul National Univ.

GRADUATE STUDENTS

H. Shin, Res. Asst., MIT
H. Tekin, Res. Asst., MIT

SUPPORT STAFF

S.D. Lorimor, Research Manager

PUBLICATIONS

A. Manbachi, S. Shrivastava, M. Cioffi, B.G. Chung, M. Moretti, U. Demirci, M. Yliperttula, and A. Khademhosseini, "Microcirculation within grooved substrates regulates cell positioning and cell docking inside microfluidic channels," *Lab on a Chip*, 2008, to be published.

S. Jinno, H.-C. Moeller, C.L. Chen, B. Rajalingam, B.G. Chung, M.R. Dokmeci, and A. Khademhosseini, "Microfabricated multilayer parylene-C stencils for the generation of patterned dynamic co-cultures," *Journal of Biomedical Materials Research*, vol. 86A, no. 1, pp. 278-288, July 2008.

D. Wright, B. Rajalingam, Y. Ling, J. Yeh, J. Karp, R. Langer, M. Dokmeci, and A. Khademhosseini, "Reusable, reversibly sealable parylene membranes for cell and protein patterning," *Journal of Biomedical Materials Research, Part A*, vol. 85A, no. 2, pp. 530-538, May 2008.

B.A. Teply, R. Tong, S.Y. Jeong, G. Luther, I. Sherifi, C.H. Yim, A. Khademhosseini, O.C. Farokhzad, R.S. Langer, and J. Cheng, "The use of charge-coupled polymeric microparticles and micromagnets for modulating the bioavailability of orally delivered macromolecules," *Biomaterials*, vol. 29, no. 9, pp. 1216-1223, Mar. 2008.

F. Tian, H. Hosseinkhani, M. Hosseinkhani, A. Khademhosseini, G. Estrada, and H. Kobayashi, "Quantitative analysis of cell adhesion on aligned micro- and nanofibers," *Journal of Biomedical Materials Research, Part A,* vol. 84A, no. 2, pp. 291-299, Feb. 2008.

H.-C. Moller, M. Mian, S. Shrivastava, B.G. Chung, and A. Khademhosseini, "A microwell array system for stem cell culture," *Biomaterials*, vol. 29, no. 6, pp. 752-763, Feb. 2008.

L. Kang, B.G. Chung, R. Langer, and A. Khademhosseini, "Microfluidics for drug discovery and development: From target selection to lifecycle management," *Drug Discovery Today*, vol. 13, no. 1, pp. 1-13, Jan. 2008.

B.G. Chung, L. Kang, and A. Khademhosseini, "Micro- and nanoscale technologies for tissue engineering and drug discovery applications," *Expert Opinion on Drug Discovery*, vol. 2, no. 12, pp. 1653-1658, Dec. 2007.

A. Khademhosseini and R. Langer, "Microengineered hydrogels for tissue engineering," *Biomaterials*, vol. 28, no. 34, pp. 5087-5092, Dec. 2007.

S. Hong, D. Lee, H. Zhang, J.Q. Zhang, J.N. Resvick, A. Khademhosseini, M.R. King, R. Langer, and J.M. Karp, "Covalent immobilization of P-selectin enhances cell rolling," *Langmuir*, vol. 23, no. 24, pp. 12261-12268, Nov. 2007.

T. Cheng, V. Yadav, S. De Leo, A. Mohadas, D. Wright, Y. Ling, S. Selvarash, M.R. Dokmeci, and A. Khademhosseini, "Cell and protein compatibility of parylene-C membranes," *Langmuir*, vol. 23, no. 23, pp. 11718-11725, Nov. 2007.

D. Wright, B. Rajalingam, S. Selvarash, M. Dokmeci, and A. Khademhosseini, "Generation of static and dynamic patterned co-cultures using microfabricated parylene-C stencils," *Lab on a Chip*, vol. 7, no. 10, pp. 1272-1279, June 2007.

J.M. Karp, J. Yeh, G. Eng, J. Fukuda, J. Blumling III, K.Y. Suh, J. Cheng, J. Borenstein, R. Langer, and A. Khademhosseini, "Controlling size, shape and homogeneity of embryoid bodies using poly(ethylene glycol) microwells," *Lab on a Chip*, vol. 7, no. 6, pp. 786-794, June 2007.

Y. Ling, J. Rubin, Y. Deng, C. Huang, U. Demirci, J.M. Karp, and A. Khademhosseini, "A cell-laden microfluidic hydrogel," *Lab on a Chip*, vol. 7, no. 6, pp. 756-762, June 2007.

C. Rivest, V. Yadav, D. Morrison, J. Rubin, B. Ni, A. Mahdavi, J.M. Karp, and A. Khademhosseini, "Microscale hydrogels: fabrication, applications and mechanical properties," *Journal of Mechanics of Materials and Structures*, vol. 2, no. 6, pp. 1103-1119, June 2007.

G.T. Franzesi, B. Ni, Y. Ling, and A. Khademhosseini, "A controlled-release strategy for the generation of crosslinked hydrogel microstructures," *Journal of American Chemical Society*, vol. 128, no. 47, pp. 15064-15065, Nov. 2006.

A. Khademhosseini, R. Langer, J. Borenstein, and J. Vacanti, "Microscale technologies for tissue engineering and biology," *Proceedings of National Academy of Sciences USA,* vol. 103, no. 8, pp. 2480-2487, Feb. 2006.

A. Khademhosseini, C. Bettinger, J. Karp, J. Yeh, Y. Ling, J. Borenstein, J. Fukuda, and R. Langer, "Biomaterials and microscale technologies: Building on each other to advance biomedical applications," *Journal of Biomaterials Science: Polymer Edition*, vol. 17, no. 11, pp. 1221-1240, 2006.

Sang-Gook Kim
Associate Professor
Department of Mechanical Engineering

COLLABORATORS

G. Chen, MIT, ME
P. So, MIT, ME
G. Barbastathis, MIT, ME
M. Schmidt, MIT, EECS
V. Bulović, MIT, EECS
C. Sodini, MIT, EECS
B. Wardle, MIT, AA

POSTDOCTORAL ASSOCIATE

H. Lee, Postdoctoral Associate

VISITING ENGINEER

M. de Volder

GRADUATE STUDENTS

S. Kim, ME
S. Bathurst, ME
A. Hajati, EECS
N. Reticker-Flynn, ME
J. Peck, ME/TPP
H. Lee, ME

SUPPORT STAFF

R. Hardin, Admin. Asst.

PUBLICATIONS

J. Peck, E.M.W. Kolb, S.-G. Kim, and T. Lee, "A discrete event simulation approach to optimizing design and use of Fast Track in an emergency department," *Health Care Management Science,* 2008, to be published.

S. Bathurst, J. Jeon, H.W. Lee and S.-G. Kim, "Ink jet printing of PZT thin films for MEMS applications," in *Proc. Digital Fabrication*, Pittsburgh, PA, Sept. 2008, to be published.

S. Bathurst, J. Jeon, H.W. Lee, and S.-G. Kim,"PZT MEMS by thermal ink jet printing," presented at the *Solid-State Sensor and Actuator Workshop*, Hilton Head, NC, June 2008.

H.J. In, A.J. Nichol, H.W. Lee, S.-G. Kim, and G. Barbastathis, "Carbon nanotube-based magnetic actuation of origami membranes," in *Proc. International Conference on Electron, Ion and Photon Beam Technology and Nanofabrication*, Portland, OR, May 2008.

A. Hajati and S.-G.Kim, "Energy harvesting piezoelectric MEMS devices for self-supportive wireless sensors," in *Proc. Innovation Conference, NSF Engineering Research Grantees' Meeting*, Knoxville, Tennessee, Jan. 2008.

A. Hajati and S.-G.Kim, "Rectifierless piezoelectric micro power generator," presented at the *SPIE Smart Structures and Materials & Nondestructive Evaluation and Health Monitoring*, 2008.

S. Bathurst, H.W. Lee and S.-G. Kim, "Direct printing of lead zirconate titanate thin films," presented at *IEEE MEMS 2008*, 2008.

S.-G. Kim, Z. Traina, and H. Lee, "Folding assembly of microactuators," *CIRP Annals-Manufacturing Technology,* vol. 57, no. 1, pp. 29-32, 2008.

Z. Traina and S.-G. Kim. "Muscle-inspired linear actuator via folding assembly of MEMS actuators," presented at the *US-Korea Conference 2007, Intelligent Robot Symposium*, 2007.

J. Peck, E. Kolb, T. Lee, and S.-G. Kim, "Towards sustainable, efficient operations of an emergency department," presented at the *First Annual Operations Research in Health Care Conference*, May 2007.

N.J. Conway, Z. Traina and S.-G. Kim, "Strain amplifying piezoelectric MEMS actuator," *Journal of Micromechanics and Microengineering*, vol. 17, no. 4, pp. 781-787, Apr. 2007.

Jing Kong
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

M. Dresselhaus, EECS
A. Chandrakasan, EECS
T. Palacios, EECS
P. Jarrillo-Herrero, Physics
F. Stellacci, DDMSE,
J. Zhang and Z.F.Liu, Chemistry, Peking University

POSTDOCTORAL ASSOCIATES

J.K. Yuan

GRADUATE STUDENTS

H. Farhat, Res. Asst., DMSE
A. R. Cecco, Res. Asst., DMSE
D. A. Nezich, Res. Asst., Physics
K. J. Lee, Res. Asst., EECS
M. Hofmann, Res. Asst., EECS

SUPPORT STAFF

E. Moran, Admin. Asst

PUBLICATIONS

H. Farhat, H. Son, G.G. Samsonidze, S. Reich, M.S. Dresselhaus, and J. Kong, "Phonon softening in individual metallic carbon nanotubes due to the Kohn anomaly," *Physical Review Letters*, vol. 99, no. 14 , pp. 145506:1-4, Oct. 2007.

X.J. Duan, H.B. Son, B. Gao, J. Zhang, T.J. Wu, G.G. Samsonidze, M.S. Dresselhaus, Z.F. Liu, and J. Kong, "Resonant raman spectroscopy of individual strained single-wall carbon nanotubes," *Nano Letters*, vol. 7, no. 7, pp. 2116-2121, June 2007.

H. Son, G.G. Samsonidze, J. Kong, Y.Y. Zhang, X.J. Duan, J. Zhang, Z.F. Liu, and M.S. Dresselhaus, "Strain and friction induced by van der Waals interaction in individual single walled carbon nanotubes," *Applied Physics Letters*, vol. 90, no. 25, pp. 253113:1-3, June 2007.

A. Reina, M. Hofmann, D. Zhu, and J. Kong, "Growth mechanism of long and horizontally aligned carbon nanotubes by chemical vapor deposition," *Journal of Physical Chemistry C*, vol. 111, no. 20, pp. 7292-7297, May 2007.

Y.Y. Zhang, H. Son, J. Zhang, J. Kong, and Z.F. Liu, "Laser-heating effect on Raman spectra of individual suspended single-walled carbon nanotubes," *Journal of Physical Chemistry C*, vol. 111, no. 5, pp. 1988-1992, Jan. 2007.

Y.Y. Zhang, H. Son, J. Zhang, M.S. Dresselhaus, J. Kong, and Z.F. Liu, "Raman spectra variation of partially suspended individual single-walled carbon nanotubes,"*Journal of Physical Chemistry C*, vol. 111, no. 5, pp. 1983-1987, Jan. 2007.

S. Bhaviripudi, E. Mile, S. Steiner, A.T. Zare, M.S. Dresselhaus, A. Belcher, and J. Kong, "CVD synthesis of single-walled carbon nanotubes from gold nanoparticle catalysts," *Journal of the American Chemical Society,* vol. 129, pp. 1516-1517, Jan. 2007.

X. Zhang, K. Jiang, C. Feng, P. Liu, L. Zhang, J. Kong, T. Zhang, Q. Li, and S. Fan, "Spinning and processing continuous yarns from 4-inch wafer scale super-aligned carbon nanotubes arrays," *Advance Materials,* vol. 18, pp. 1505-1510, May 2006.

H.B. Son, A. Reina, M.S. Dresselhaus, and J. Kong, "Characterizing the chirality distribution of single-walled carbon nanotube materials with tunable Raman spectroscopy," *Physica Status Solidi (b),* vol. 243, no. 13, pp. 3161-3165, Oct. 2006.

S. Bhaviripudi, A. Reina, J. Qi, J. Kong, and A. Belcher, "Block-copolymer assisted synthesis of arrays of metal nanoparticales and their catalytic activities for the growth of SWNTs," *Nanotechnology,* vol. 17, pp. 5080-5086, Sept. 2006.

H. Son, A. Reina, G.G. Samsonidze, R. Saito, A. Jorio, M.S. Dresselhaus, and J. Kong, "Raman characterization of electronic transition energies of metallic single-wall carbon nanotubes," *Physical Review B,* vol. 74, p. 073406, Aug. 2006.

X. Zhang, K. Jiang, C. Feng, P. Liu, L. Zhang, J. Kong, T. Zhang, Q. Li, and S. Fan, "Spinning and processing continuous yarns from 4-inch wafer scale super-aligned carbon nanotubes arrays," *Advanced Materials,* vol. 18, pp. 1505-1510, May 2006.

F. Villalpando-Paez, A. Zamudio, A.L. Elias, H. Son, E.B. Barros, S.G. Chou, Y.A. Kim, H. Muramatsu, T. Hayashi, J. Kong, H. Terrones, G. Dresselhaus, M. Endo, M. Terrones, and M.S. Dresselhaus, "Synthesis and characterization of long strands of nitrogen-doped single-walled carbon nanotubes," *Chemical Physical Letters,* vol. 424, pp. 345-352, Apr. 2006.

J. Lu, T. Kopley, D. Dutton, J. Liu, C. Qian, H. Son, M.S. Dresselhaus, and J. Kong, "Generating suspended single-walled carbon nanotubes across a large surface area via patterning self-assembled catalyst-containing block copolymer thing films," *Journal of Physical Chemistry Letters B,* vol. 110, pp. 10585-10589, Apr. 2006.

Y.Y. Zhang, J. Zhang, H.B. Son, J. Kong, and Z.F. Liu, "Substrate-induced Raman frequency variation for single-walled carbon nanotubes," *Journal of the American Chemical Society*, vol. 127, no. 49, p. 17156, Dec. 2005.

B.J. LeRoy, J. Kong, V.K. Pahilwani, C. Dekker, and S.G. Lemay, "Three-terminal scanning tunneling spectroscopy of suspended carbon Nanotubes," *Physics Review B*, vol. 72, pp. 075413:1-5, Aug. 2005.

P. Jarillo-Herrero, J. Kong, H.S.J. van der Zant, C. Dekker, L.P. Kouwenhoven, and S. De Franceschi, "Electronic transport spectroscopy of carbon nanotubes in a magnetic field," *Physics Review Letters,* vol. 94, pp. 156802: 1-4, Apr. 2005

S. Sapmaz, P. Jarillo-Herrero, J. Kong, C. Dekker, L.P. Kouwenhoven, and H.S.J. van der Zant, "Excitation spectrum of metallic carbon nanotubes," *Physics Review B*, vol. 71, pp. 153402:1-4, Apr. 2005.

Jeffrey H. Lang
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

A.I. Akinwande, MIT
M.G. Allen, Georgia Inst. of Tech.
A.P. Chandrakasan, MIT
T. Daniel, University of WA
A.H. Epstein, MIT
J.G. Hildebrand, University of AZ
F.S. Hover, MIT
S. Jacobson, MIT
A.H. Slocum, MIT
M.A. Schmidt, MIT
M.S. Triantafyllou, MIT
J. Voldman, MIT

GRADUATE STUDENTS

S. Chang, EECS
V. Fernandez, ME
S. Hou, EECS
Z. Trimble, ME
A. Weber, ME
B.C. Yen, EECS

SUPPORT STAFF

D. Bizi, Admin. Asst. I

PUBLICATIONS

H. Ma, J.H. Lang and A.H. Slocum, "Design of an electrochemical impedance test cell with servomechanically adjustable cell constant," in *Proc. IEEE Sensors Conference*, Atlanta, GA, Oct. 2007, pp. 1233-1236.

H. Ma, J.H. Lang and A.H. Slocum, "Technique for measuring the dielectric constant of liquids and gases without the use of calibration standards," in *Proc. μTAS Conference*, Paris, France, Oct. 2007, pp. 1692-1694.

A.C. Weber, J.H. Lang and A.H. Slocum, "111 Si etched planar electrical contacts for power MEMS relays," in *Proc. 53rd IEEE Holm Conference on Electrical Contacts*, Pittsburgh, PA, Sept. 2007, pp. 156-159.

V.I. Fernandez, S.M. Hou, F.S. Hover, J.H. Lang, and M.S. Triantafyllou, "Lateral line inspired MEMS-array pressure sensing for passive underwater navigation," in *Proc. Unmanned Untethered Submersible Technology Symposium*, Durham, NH, Aug. 2007, Sensors Paper #4.

J.W. Phinney, D.J. Perreault and J.H. Lang, "Synthesis of lumped transmission-line analogs," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1531-1542, July 2007.

J.W. Phinney, D.J. Perreault and J.H. Lang, "Radio-frequency inverters with transmission-line input networks," *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1154-1161, July 2007.

A.C. Weber, G. Bassiri, B.M. Dvorak, A.H. Slocum, D.A. Lucca, and J.H. Lang, "Atomic plane electrical contacts," in *Proc. Seventh International Conference for Precision Engineering and Nanotechnology*, Bremen, Germany, May 2007, vol. 2, pp. 445-448.

V.I. Fernandez, S.M. Hou, F.S. Hover, J.H. Lang, and M.S. Triantafyllou, "MEMS-array pressure sensing for underwater navigation," in *Proc. Undersea Distributed Network Systems Conference*, Newport, RI, Feb. 2007.

S.M. Hou, J.H. Lang, A.H. Slocum, A.C. Weber and J.R. White; "A high-Q widely-tunable gigahertz electromagnetic cavity resonator," *IEEE/ASME Journal of Microelectromechanical Systems,* vol. 15, pp. 1540-1545, Dec. 2006.

D.P. Arnold, S. Das, J.W. Park, I. Zana, J.H. Lang, and M.G. Allen; "Microfab-ricated high-speed axial-flux multiwatt permanent-magnet generators - Part II: design, fabrication and testing," *IEEE/ ASME Journal of Microelectromechanical Systems,* vol. 15, pp. 1351-1363, Oct. 2006.

S. Das, D.P. Arnold, I. Zana, J.W. Park, M.G. Allen and J.H. Lang; "Micro-fabricated high-speed axial-flux multiwatt permanent-magnet generators-Part I: modeling," *IEEE/ASME Journal of Microelectromechanical Systems,* vol. 15, pp. 1330-1350, Oct. 2006.

D.P. Arnold, I. Zana, F. Herrault, P. Galle, J.W. Park, S. Das, J.H. Lang, and M.G. Allen, "Design optimization of an 8-Watt microscale axial-flux permanent magnet generator," *Journal of Micromechanics and Microengineering,* vol. 16, pp. S290-S296 Aug. 2006.

H. Köser and J.H. Lang, "Magnetic induction micromachine-part I: Design and analysis," *Journal of Microelectromechanical Systems*, vol. 15, no. 2, pp. 415-426, Apr. 2006.

D.P. Arnold, S. Das, F. Cros, I. Zana, M.G. Allen, and J.H. Lang, "Magnetic induction machines integrated into bulk-micromachined silicon," *Journal of Microelectromechanical Systems*, vol. 15, no. 2, pp. 406-414, Apr. 2006.

Hae-Seung Lee
Professor, Director of Center for Integrated Circuits and Systems
Department of Electrical Engineering and Computer Science

COLLABORATORS
P. Holloway, National Semiconductor Co.

VISITING SCIENTISTS
Soon-Kyun Shin, EECS (Samsung Electronics)

GRADUATE STUDENTS
L. Brooks, Res. Asst., EECS
A. Chow, Res. Asst., EECS
J. Chu, Res. Asst., EECS
J. Feng, EECS
M. Guyton, Res. Asst., EECS
P. Lajevardi, Res. Asst., EECS
S. Lee, Res. Asst., EECS
M. Markova, Res. Asst., EECS

SUPPORT STAFF
C. Collins, Assistant to Director of Center for Integrated Circuits and Systems

PUBLICATIONS

N. Sun, H.-S. Lee and D. Ham, "Digital background calibration in pipelined ADCs using commutated feedback capacitor switching," *IEEE Transactions on Circuits and Systems*, 2008, to be published.

S.-K. Shin, Y.-S. You, S.-H. Lee, K.-H. Moon, J.-W. Kim, L. Brooks, and H.-S. Lee, "A fully-differential zero-crossing-based 1.2V 10b 26MS/s pipelined ADC in 65nm CMOS," *Digest of Technical Papers, Symposium on VLSI Circuits*, Honolulu, HI.

H.-S. Lee, "Comparator and zero-crossing based ADC's: Challenges and possible solutions," presented at the *ISSCC Special Evening Topics Session*, San Francisco, CA, Feb. 2008.

L. Brooks and H.-S. Lee, "A zero-crossing based 8 bit, 200MS/s pipelined ADC," *IEEE Journal of Solid-State Circuits*, Dec 2007.

H.-S. Lee and C. G. Sodini, "Mixed-signal integrated circuits-digitizing the analog world," *Proc. IEEE*, Dec. 2007.

H.-S. Lee, "Limits of power consumption in analog circuits," *Digest of Technical Papers, Symposium on VLSI Circuits*, Kyoto, Japan, June 2007

A. Chow and H.-S. Lee, "Transient noise analysis for comparator-based switched-capacitor circuits," in *Proc. ISCAS*, May 2007.

H.-S. Lee, "Technology scaling and analog circuits: Challenges and solutions," presented at the *ISSCC Special Evening Topics Session*, San Francisco, CA, Feb. 2007.

L. Brooks and H.-S. Lee, "A zero-crossing based 8b 200MS/s pipelined ADC," in *ISSCC Digest of Tech. Papers*, San Francisco, CA, Feb. 2007.

Carol Livermore

SMA Assistant Professor of Manufacturing
Department of Mechanical Engineering

COLLABORATORS

G. Barbastathis, MIT
T. Havel, MIT
L. Velásquez-García, MIT

GRADUATE STUDENTS

G. Agarwal, Res. Asst., ME
F. Eid, Res. Asst., ME
F. Hill, Res. Asst., ME
T. Hill, Res. Asst., EECS
N. Shaar, Res. Asst., ME

SUPPORT STAFF

N. Weaver, Admin. Asst.

PUBLICATIONS

N. Shaar, G. Barbastathis, and C. Livermore, "Cascaded mechanical alignment for assembling 3D MEMS," in *Proc. 18th IEEE International Conference on Microelectromechanical Systems*, Tuscon, AZ, Jan. 2008. pp. 1064-1068

L.F. Velásquez-García, T.F. Hill, B.A. Wilhite, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator – Part I: Device fabrication and proof of concept demonstration," *IEEE Journal of Microelectromechanical Systems,* vol. 16, no. 6, pp. 1482-1491, Dec. 2007.

T.F. Hill, L.F. Velásquez-García, B.A. Wilhite, W.T. Rawlins, S. Lee, S.J. Davis, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator–Part II: Experimental exploration of the performance space," *IEEE Journal of Microelectromechanical Systems,* vol. 16, no. 6, pp. 1492-1505, Dec. 2007.

Hill, F.A., T.F. Havel, and C. Livermore, "A portable power source based on MEMS and carbon nanotubes," in *Proc. IMECE 2007,* Seattle, WA, Nov. 2007.

C. Livermore, T.F. Hill, B.A. Wilhite, L.F. Velásquez-García, A.H. Epstein, K.F. Jensen, W.T. Rawlins, S. Lee, and S. Davis, "Singlet oxygen generator on a chip for mems-based COIL," in *Proc. LASE 2007 Symposium of SPIE Photonics West,* San Jose, CA, Jan. 2007.

L.F. Velásquez-García, T.F. Hill, B.A. Wilhite, K.F. Jensen, A.H. Epstein, and C. Livermore, "A MEMS singlet oxygen generator for a MEMS chemical oxygen iodine laser," in *Proc. Power MEMS 2006,* Berkeley, CA, Nov. 2006, pp. 117-120.

F. Eid, S.H. Jung and C. Livermore, "Templated assembly by selective removal: Mechanically-driven selective assembly at the micron and submicron scales," in *Proc. 4th International Symposium on Nanomanufacturing,* Cambridge, MA, Nov. 2006.

T.F. Hill, B.A. Wilhite, L.F. Velásquez-García, A.H. Epstein, K.F. Jensen, and C. Livermore, "A MEMS singlet oxygen generator," presented at *Solid State Sensor, Actuator, and Microsystems Workshop,* 2006.

S. Jung and C. Livermore, "Achieving selective assembly with template topography and ultrasonically induced fluid forces," *Nano Letters,* vol. 5, no. 11, pp. 2188-2194, Nov. 2005.

S.F. Nagle, C. Livermore, L.G. Frechette, R. Ghodssi, and J.H. Lang, "An electric induction micromotor," *Journal of Microelectromechanical Systems,* vol. 14, no. 5, pp. 1127-1143, Oct. 2005.

J.L. Steyn, S.H. Kendig, R. Khanna, T.M. Lyszczarz, S.D. Umans, J.U. Yoon, C. Livermore, and J.H. Lang, "Generating electric power with a MEMS electroquasistatic induction turbine-generator," in *Proc. 18th IEEE International Conference on Micro Electro Mechanical Systems,* Miami, FL, Jan./Feb. 2005, pp. 614-617.

B.A. Wilhite, C. Livermore, Y. Gong, A.H. Epstein, and K.F. Jensen, "Design of a MEMS-based microchemical oxygen iodine laser system," *IEEE Journal of Quantum Electronics,* vol. 40, no. 8, pp. 1041-1055, Aug. 2004.

C. Livermore, A. Forte, T. Lyszczarz, S.D. Umans, A.A. Ayon, and J.H. Lang, "A High-power MEMS electric induction micromotor," *IEEE Journal of Microelectromechanical Systems*, vol. 13, no. 3, pp. 465-471, June 2004.

T.C. Neugebauer, D.J. Perreault, J.H. Lang, C. Livermore, "A six-phase multilevel interter for MEMS electrostatic induction micromotors," *IEEE Transactions on Circuits and Systems II*, vol. 51, no. 2, pp. 49-56, Feb. 2004.

C. Livermore, A. Forte, T. Lyszczarz, S.D. Umans, and J. Lang, "Microscale electric induction machines for power applications," in *Proc. Electrostatics 2003,* Edinburgh, Scotland, Mar. 2003, pp. 45-52.

C. Livermore, D.S. Duncan, R.M. Westervelt, K.D. Maranowski, and A.C. Gossard, "Measuring interactions between tunnel-coupled quantum dots in the quantum Hall regime," *Journal of Applied Physics,* vol. 86, no. 7, pp. 4043-4045, Oct. 1999.

A.S. Adourian, C. Livermore, R.M. Westervelt, K.L. Campman, and A.C. Gossard, "Evolution of Coulomb blockade spectra in parallel coupled quantum dots," *Applied Physics Letters,* vol. 75, no. 3, pp. 424-426, July 1999.

C. Livermore, D.S. Duncan, R.M. Westervelt, K.D. Maranowski, and A.C. Gossard, "Conductance oscillations in tunnel-coupled quantum dots in the quantum Hall regime," *Physical Review B,* vol. 59, no. 16, pp. 10744-10747, Apr. 1999.

D.S. Duncan, C. Livermore, R.M. Westervelt, K.D. Maranowski, and A.C. Gossard, "Direct measurement of the destruction of charge quantization in a single electron box," *Applied Physics Letters,* vol. 74, no. 7, pp. 1045-1047, Feb. 1999.

C.H. Crouch, C. Livermore, R.M. Westervelt, K.L. Campman, and A.C. Gossard, "Evolution of the Coulomb gap in tunnel-coupled quantum dots," *Applied Physics Letters*, vol. 71, no. 6, pp. 817-819, Aug. 1997.

C. Livermore, C.H. Crouch, R.M. Westervelt, K.L. Campman, and A.C. Gossard, "The Coulomb blockade in coupled quantum dots," *Science,* vol. 274, no. 5291, pp. 1332-1335, Nov. 1996.

Scott R. Manalis

Professor
Department of Biological and Mechanical Engineering

COLLABORATORS

A. Amon, MIT
J. Han, MIT
S. Jiang, Univ of Washington
M. Kirschner, Harvard
M. Lang, MIT
P. Mallick, UCLA
R. Sasisekharan, MIT
T. Squires, UCSB

POSTDOCTORAL ASSOCIATES

T. Burg, BE
M. Godin, BE
W. Grover, BE
S. Knudsen, BE

GRADUATE STUDENTS

A. Bryan, BE
R. Chunara, HST and EECS
F. Delgado, BE
P. Dextras, BE
M. von Muhlen, BE
S. Son, ME
Y.C. Weng, BE

SUPPORT STAFF

L. Chapman

PUBLICATIONS

S. Son, W.H. Grover, T.P. Burg, S.R. Manalis, "Suspended microchannel resonators for ultra-low volume universal detection," *Analytical Chemistry,* 2008, to be published.

W.H. Grover, M. von Muhlen, and S.R. Manalis, "Teflon films for chemically-inert microfluidic valves and pumps" *Lab on a Chip*, 2008, to be published.

T.M. Squires, R.J. Messinger, S.R. Manalis, "Making it stick: convection, reaction, and diffusion in surface based biosensors," *Nature Biotechnology*, 2008, to be published.

R. Chunara, M. Godin, S.M. Knudsen, and S.R. Manalis, "Mass-based readout for agglutination assays," *Applied Physics Letters*, vol. 91, no. 19, pp. 193902:1-3, 2007.

M. Godin, A.K. Bryan, T. Burg, and S.R. Manalis, "Measuring the mass, density and size of particles and cells using a suspended microchannel resonator," *Applied Physics Letters*, vol. 91, no. 12, pp. 123121:1-3, 2007.

T.P. Burg, M.Godin, W. Shen, G. Carlson, J.S. Foster, K. Babcock, and S.R. Manalis, "Weighing of biomolecules, single cells, and single nanoparticles in fluid," *Nature*, vol. 446, no. 7139, pp. 1066-1069, Apr. 2007.

J. Hou, M. Godin, K. Payer, R. Chakrabarti, and S.R. Manalis, «Integrated microelectronic device for label-free nucleic acid amplification and detection," *Lab on a Chip,* vol. 7, no. 3, pp. 347-354, Mar. 2007.

Ichiro Masaki
Director
Intelligent Transportation Research Center

COLLABORATORS

J.F. Coughlin
B.K.P. Horn
H.-S. Lee
C.G. Sodini
J.M. Sussman

GRADUATE STUDENTS

Y. Fang, Res. Asst., EECS
O. Kurugol, Res. Asst., ME

VISTING SCIENTISTS

T.H. Fang
S. Yokomitsu

SUPPORT STAFF

M. Flaherty, Senior Admin. Asst.

PUBLICATIONS

Y. Fang. B.K.P Horn and I. Masaki, "Systematic information fusion methodology for static and dynamic obstacle detection in ITS," to be presented at the 15*th World Congress On ITS*, Nov. 2008.

B.K.P. Horn, Y. Fang and I. Masaki, "Time to contact relative to a planar surface," *IEEE Intelligent Vehicles Symposium*, Istanbul, Turkey, June 2007, pp. 68-74.

W.F. Herrington, Jr., B.K.P. Horn, and I. Masaki, "Application of the discrete Haar wavelet transform to image fusion for nighttime driving," in *Proc. Intelligent Vehicles Symposium 2005*, Las Vegas, NV, June 2005, pp. 273-277.

Y. Fang, K. Yamada, Y. Ninomiya, B. Horn and I. Masaki, "A shape-independent-method for pedestrian detection with far infrared-images," IEEE Transactions on Vehicular Technology, vol. 53, no. 6, pp.1679-1697, Nov. 2004.

Y. Fang, K. Yamada, Y. Ninomiya, B.K.P. Horn, and I. Masaki, "Comparison between infrared-image-based and visible-image-based approaches for pedestrian detection," in *Proc. Intelligent Vehicles Symposium 2003*, Columbus, OH, June 2003, pp. 505-510.

Y. Fang, I. Masaki, and B.K.P. Horn, "Depth-based target segmentation for intelligent vehicles: Fusion of radar and binocular stereo," *IEEE Transactions on Intelligent Transportation Systems*, vol. 3, no. 3, pp.196-202, Sept. 2002.

Y. Fang, I. Masaki, and B. Horn, "Distance/motion based segmentation under heavy background noise," *IEEE Intelligent Vehicles Symposium,* June 2002, pp. 483-488.

Y. Fang, Y. Ninomiya, and I. Masaki, "Intelligent transportation systems, challenges and opportunities," *The 2nd International Symposium on Multimedia Mediation Systems,* Mar. 2002, pp. 72-77.

Y. Fang, I. Masaki, and B. Horn, "Distance range based segmentation in intelligent transportation systems: Fusion of radar and binocular stereo," *IEEE Intelligent Vehicles Symposium,* May 2001, pp.171-176.

Tomás Palacios
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

F. Calle, ETSIT-UPM, Spain
D. Jena, University of Notre Dame
U.K. Mishra, University of California, Santa Barbara
E. Monroy, CEA-Grenoble, France
E. Munoz, ETSIT-UPM, Spain
H. Xing, University of Notre Dame
E. Wang, MIT
J. Kong, MIT
D.J. Perreault, MIT

VISITING SCIENTIST

J.M. Tirado, U-CM, Spain

VISITING STUDENT

F. Mieville, EPFL, Switzerland

GRADUATE STUDENTS

J.W. Chung, Res. Asst., EECS
Z. Xu, Res. Asst., EECS
O.I. Saadat, Res. Asst., EECS
B. Lu, Res. Asst., EECS

UNDERGRADUATE STUDENTS

J. Wu
D. Piedra
I. C. Rust
J. Negrete

SUPPORT STAFF

E. Kubicki, Admin. Asst. II

PUBLICATIONS

T. Palacios, "New structures for AlGaN/GaN high electron mobility transistors," in *Advanced Semiconductor Materials and Devices Research: III-Nitrides and SiC*, Dr. Ho-Young Cha, Ed. Kerala, India: Research Signpost, 2007.

T. Palacios and U.K.Mishra, "Modeling and simulation of AlGaN/GaN high electron mobility transistors," in *Nitride Semiconductor Devices. Principles and Simulation,* J. Piprek, ed. Weinheim, Germany: Wiley-VCH, 2007.

X. Zhao, J.W. Chung, and T. Palacios, "Atomic layer etching of AlGaN/GaN structures," in *Proc. International Conference on Nitride Semiconductors*, Las Vegas, NV, Sept. 2007, p. 42.

X. Zhao, J.W. Chung, and T. Palacios, "Increase of electron velocity in GaN HEMTs by electric field engineering," in *Proc. International Conference on Nitride Semiconductors*, Las Vegas, NV, Sept. 2007, pp. 50-51.

J.W. Chung, X. Zhao, and T. Palacios, "Effect of image charges in the drain delay of AlGaN/GaN HEMTs," in *Proc. International Conference on Nitride Semiconductors*, Las Vegas, NV, Sept. 2007, p. 50.

J.W. Chung, X. Zhao, and T. Palacios, "Estimation of trap density in AlGaN/GaN HEMTs from subthreshold slope study," *65th Device Research Conference*, University of Notre Dame, June 2007, pp. 111-112.

X. Zhao, J.W. Chung, H. Tang, and T. Palacios, "Schottky drain AlGaN/GaN HEMTs for mm-wave applications," 65th Device Research Conference, University of Notre Dame, June 2007, pp. 107-108.

Y. Pei, L. Shen, T. Palacios, N.A. Fichtenbaum, L.S. McCarthy, S. Keller, S.P. DenBaars, and U.K. Mishra, "Study of the n^+ GaN cap in AlGaN/GaN high electron mobility transistors with reduced source-drain resistance," *Japanese Journal of Applied Physics*, vol. 46, nos. 33-35, pp. L842-L844, Sept. 2007.

M.H. Wong, Y. Pei, T. Palacios, L. Shen, A. Chakraborty, L.S. McCarthy, S. Keller, S.P. DenBaars, J.S. Speck, and U.K. Mishra, "Low non-alloyed ohmic contact resistance to nitride HEMTs using N-face growth," *Applied Physics Letters*, vol. 91, no. 23, pp. 232103:1-3, Dec. 2007.

M.H. Wong, S. Rajan, R.M. Chu, T. Palacios, C.S. Suh, L.S. McCarthy, S. Keller, J.S. Speck, and U.K. Mishra, "N-face high electron mobility transistors with a GaN-spacer," *physica status solidi a*, vol. 204, no. 6, pp. 2049-2053, June 2007.

T. Palacios, "New device ideas for nitride-based mm-wave electronics," presented at the *European Heterostructure Technology Workshop*, 2007.

T. Palacios, "Recent progress in GaN HEMTs for mm-waves frequencies and beyond," presented at the *7th Topical Workshop on Heterostructure Microelectronics*, 2007.

T. Palacios *et al.*, "Mm-wave initiative for carbon electronics," presented at the *DARPA Workshop on Carbon-Based Ultra-High Speed Electronics for Wafer-Scale Integration*, 2007.

David Perreault

Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

J. Kassakian, MIT
J. Lang, MIT
T. Keim, MIT
C.R. Sullivan, Dartmouth
A.P. Chandrakasan, MIT
D. Anderson, NSC
S. Davis, Draper

GRADUATE STUDENTS

Y. Han, Res. Asst., EECS
B. Pierquet, Res. Asst., EECS
R. Pilawa, Res. Asst., EECS
A. Sagneri, Res. Asst., EECS
D. Giuliano, Draper Fellow, EECS
J. Hu, Res. Asst., EECS
W. Li, Res. Asst., EECS

SUPPORT STAFF

V. Mizuno, Admin. Asst. II

PUBLICATIONS

Y. Han, A. Li, G. Cheung, C.R. Sullivan, and D.J. Perreault, "Evaluation of magnetic materials for very high frequency power applications," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

J. Hu, A.D. Sagneri, J.M. Rivas, S.M. Davis, and D.J. Perreault, "High-frequency resonant SEPIC converter with wide input and output voltage ranges," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

R.C.N. Pilawa-Podgurski, D. Giuliano, and D.J. Perreault, "Merged two-stage power converter architecture with soft charging switched-capacitor energy transfer," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

J.M. Rivas, O. Leitermann, Y. Han, and D.J. Perreault, "A very high frequency dc-dc converter based on a Phi-2 resonant inverter," *2008 IEEE Power Electronics Specialists Conference*, June 2008.

J.R. Warren, K.A. Rosowski and D.J. Perreault, "Transistor selection and design of a VHF DC-DC power converter," *IEEE Transactions on Power Electronics*, vol. 23, no. 1, pp. 27-37, Jan. 2008.

S.C. Tang, D.M. Otten, T.A. Keim, and D.J. Perreault, "Design and evaluation of a 42 V automotive alternator with integrated switched-mode rectifier," *2007 IEEE Vehicle Power and Propulsion Conference*, September 2007.

J.W. Phinney, D.J. Perreault, and J.H. Lang, "Synthesis of lumped transmission-line analogs," *IEEE Transactions on Power Electronics,* vol. 22, no. 4, pp. 1531-1542, July 2007.

J.W. Phinney, D.J. Perreault, and J.H. Lang, "Radio-frequency inverters with transmission-line input networks," *IEEE Transactions on Power Electronics,* vol. 22, no. 4, pp. 1154-1161, July 2007.

R.C.N. Pilawa-Podgurski, A.D. Sagneri, J.M. Rivas, D.I. Anderson, and D.J. Perreault, "High-frequency resonant boost converters," *2007 IEEE Power Electronics Specialists Conference,* pp. 2718-2724, June 2007.

J.M. Rivas, Y. Han, O. Leitermann, A.D. Sagneri, and D.J. Perreault, "A high-frequency resonant inverter topology with low voltage stress," *2007 IEEE Power Electronics Specialists Conference,* pp. 2705-2717, June 2007.

B.J. Pierquet, T.C. Neugebauer, and D.J. Perreault, "A fabrication method for integrated filter elements with inductance cancellation," *2007 IEEE Applied Power Electronics Conference*, Anaheim, CA, pp. 51-62, Feb. 25 – Mar. 1, 2007.

Y. Han, O. Leitermann, D.A. Jackson, J.M. Rivas, and D.J. Perreault, "Resistance compression networks for radio-frequency power conversion," *IEEE Transactions on Power Electronics*, vol. 22, No.1, pp. 41-53, Jan. 2007.

B.J. Pierquet, T.C. Neugebauer, and D.J. Perreault, "Inductance Compensation of Multiple Capacitors with Application to Common- and Differential-Mode Filters," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1815-1824, Nov. 2006. (Also, see "Corrections to inductance compensation of multiple capacitors with application to common- and differential-mode filters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 346-347, Jan. 2007.)

D.S. Lymar, T.C. Neugebauer, and D.J. Perreault, "Coupled-magnetic filters with adaptive inductance cancellation," *IEEE Transactions on Power Electronics*, vol. 21, no. 6, pp. 1529-1540, Nov. 2006.

Y. Han and D.J. Perreault, "Analysis and design of high efficiency matching networks," *IEEE Transactions on Power Electronics*, vol. 21, no. 5, pp. 1484-1491, Sept. 2006.

J.M. Rivas, J. Shafran, R.S. Wahby, and D.J. Perreault, "New architectures for radio-frequency DC-DC power conversion," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 380-393, Mar. 2006.

T.C. Neugebauer and D.J. Perreault, "Parasitic capacitance cancellation in filter inductors," *IEEE Transactions on Power Electronics,* vol. 21, no. 1, pp. 282-288, Jan. 2006.

Rajeev Ram
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

M. Geis, Lincoln Laboratory
M. Grein, Lincoln Laboratory
X. Guo, MIT
E.P. Ippen, MIT
F.X. Kaertner, MIT
R. Kirchain, MIT
V. Stojanović, MIT
A. Sinskey, MIT
H.I. Smith, MIT
S. Spector, Lincoln Laboratory

GRADUATE STUDENTS

R. Amatya, Res. Asst., EECS
K.S.K. Lee, Res. Asst., EECS
T. Liptay, Res. Asst., EECS
P. Mayer, Res. Asst., EECS
J. Orcutt, Res. Asst., EECS
T. Zaman, Res. Asst., EECS

SUPPORT STAFF

C. Bourgeois, Admin. Asst. II

PUBLICATIONS

P. Mayer, D. Lueerssen, R.J. Ram, and J. Hudgings, "Theoretical and experimental investigation of the resolution and dynamic range of CCD-based thermoreflectance imaging," *Journal of the Optical Society of America A,* vol. 24, no. 4, pp. 1156-1163, Apr. 2007.

R.K. Huang, R.J. Ram, M.J. Manfra, M.K. Connors, L.J. Missaggia, and G.W. Turner, "Heterojunction thermophotovoltaic devices with high voltage factor," *Journal of Applied Physics,* vol. 101, no. 4, pp. 04102:1-3, Feb. 2007.

T. Barwicz, H. Byun, F. Gan, M. Geis, M. Grein, C.W. Holzwarth, J.L. Hoyt, E.P. Ippen, F.X. Kärtner, T. Lyszczarz, O.O. Olubuyide, J.S. Orcutt, M.A. Popović, P.T. Rakich, R.J. Ram, H.I. Smith, S. Spector, V. Stojanović, M.R. Watts, and J.U. Yoon "Silicon photonics for compact, energy efficient interconnects," *OSA Journal of Optical Networking*, vol. 6, no. 1, pp. 63-73, Jan. 2007.

T. Zaman, X. Guo, and R.J. Ram, "Faraday rotation in an InP waveguide," *Applied Physics Letters*, vol. 90, no. 2, pp. 023514:1-3, Jan. 2007.

T. Liptay and R.J. Ram, "Temperature dependence of the exciton transition in semiconductor quantum dots," *Applied Physics Letters,* vol. 89, no. 22, pp. 223132:1-3, Nov. 2006.

H.L.T. Lee, P. Boccazzi, R.J. Ram, and A.J. Sinskey, "Microbioreactor arrays with integrated mixers and fluid injectors for high-throughput experimentation with pH and dissolved oxygen control," *Lab On a Chip,* vol. 6, no. 9, pp. 1229-1235, Sept. 2006.

E. Fuchs, E.J. Bruce, R.J. Ram, and R.E. Kirchain, "Process based cost modeling of photonics manufacture: The cost competitiveness of monolithic integration of a 1550 nm DFB laser and an electro-absorptive modulator on an InP platform," *IEEE Journal of Lightwave Technology*, vol. 24, no. 8, pp. 3175-3186, Aug. 2006.

T. Zaman, X. Guo, and R.J. Ram, "Proposal for a polarization independent integrated optical circulator," *IEEE Photonics Technology Letters*, vol. 18, no. 12, pp. 1359-1361, June 2006.

P. Mayer and R.J. Ram, "Optimization of heat-sink limited thermoelectric generators," *Nanoscale and Microscale Thermophysical Engineering,* vol. 10, no. 2, pp. 143-155, May 2006.

Caroline A Ross

Professor
Department of Materials Science and Engineering

COLLABORATORS

H.I. Smith
C.V. Thompson
E.L. Thomas
R.C. O'Handley
Y. Shao-Horn
K.K. Berggren
G. Dionne, Lincoln Laboratory
G.J. Vancso, U. Twente, NL
J.A.C. Bland, Cambridge University
M. Pardavi-Horvath, G. Washington Univ.
R.D. McMichael, NIST
A. Adeyeye, Nat. Univ. Singapore
J.Y. Cheng, IBM
F.Y. Ogrin, Univ. Exeter, UK
M. Vazquez, Madrid
G. Gubbiotti, Perugia, Italy

VISITING PROFESSORS

Y. Oh
M. Ciria

POSTDOCTORAL ASSOCIATES

F. Castano
H.S. Kim
D. Navas
H. Miyagawa
C. Nam

GRADUATE STUDENTS

W. Jung
F. Ilievski
V. Sivakumar
V. Chuang
Y.S. Jung
A. Taussig
I. Colin
Bryan Ng
Lei Bi

SUPPORT STAFF

G. Joseph, Admin. Asst. II

PUBLICATIONS

L. Bi, H.-S. Kim, G.F. Dionne, S.A. Speakman, D. Bono, and C.A. Ross, "Structural, magnetic and magneto-optical properties of Co doped $CeO_{2-\delta}$ films," *Journal of Applied Physics*, 2008, to be published.

F. Ilievski, C.A. Ross, and G.J. Vancso, "Magnetic Reversal Phenomena of Perpendicular magnetic islands fabricated by block copolymer lithography," *Journal of Applied Physics*, 2008, to be published.

S. Tacchi, M. Madami, G. Gubbiotti, G. Carlotti, W. Jung, and C.A. Ross, "Spin waves in exchange-biased NiFe/IrMn circular nanorings," *Journal of Applied Physics*, 2008, to be published.

M. Pardavi-Horvath, P. E. Si, C.A. Ross, F. J. Castaño, B. Ng, and S. Moralejo, "Configurational stability of patterned magnetic nanosystems," *Journal of Applied Physics*, 2008, to be published.

R.D. McMichael, V.P. Chuang, and C.A. Ross, "Thickness dependence of magnetic film edge properties in Ni80Fe20 stripes," *Journal of Applied Physics*, 2008, to be published.

V.P. Chuang, W. Jung, C.A. Ross, J.Y. Cheng, O.-H. Park, and H.-C. Kim, "Multilayer magnetic antidot arrays from block copolymer templates," *Journal of Applied Physics*, 2008, to be published.

V. Sivakumar, Naoaki Yabuuchi, C.A. Ross, Y.Shao-Horn, "Partially reversible changes in magnetic properties of CrO_2 nanoparticles through electrochemical cycling," *Journal of Applied Physics*, 2008, to be published.

J.D. Suh and C.A. Ross, "Dependence of the giant magnetoresistance ratio on the nano-oxide layer position in NiFe/Cu/Co pseudo-spin valve films" *Physica B*, 2008, to be published.

D. Navas, K.R. Pirota, P. Mendoza Zelis, D. Velazquez, C.A. Ross and M. Vazquez, "Effects of the magnetoelastic anisotropy in Ni nanowire arrays," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07D523:1-3, Apr. 2008.

F.Y. Ogrin, E. Sirotkin, G. van der Laan, G. Beutier, C.A. Ross, W. Jung, and R. Menon, "Soft x-ray resonant magnetic scattering investigation of stable magnetic configurations in patterned rings," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07E909:1-3, Apr. 2008.

X.S. Gao, A.O. Adeyeye, and C.A.Ross, "Magnetization reversal process in elongated Co rings with engineered defects," *Journal of Applied Physics*, vol. 103, no. 6, pp. 063906:1-6, Mar. 2008.

A. Taussig, G.F. Dionne and C.A. Ross, "Dependence of Faraday rotation and magnetooptical figure of merit on dielectric tensor elements in materials with uniaxial symmetry," to be published, *Phyiscal Review B*, vol. 77, no. 1, pp. 012407:1-4, Jan. 2008.

J. Llandro, T.J. Hayward, D. Morecroft, J.A.C. Bland, F.J. Castaño, I.A. Colin, and C.A. Ross, "Quantitative digital detection of magnetic beads using pseudo-spin-valve rings for multiplexed bioassays," *Applied Physics Letters*, vol. 91, no. 20, pp. 203904:1-3, Nov. 2007.

A. Adeyeye, X. Gao, C.A. Ross, "Magnetostatic coupling in arrays of elongated $Ni_{80}Fe_{20}$ rings," *Journal of Physics D: Applied Physics*, vol. 40, no. 21, pp. 6479-6483, Nov. 2007.

W. Jung, F.J. Castaño, and C.A. Ross, "Current-in-plane magnetoresistance of spin valve elliptical rings," *Applied Physics Letters*, vol. 91, no. 15, pp. 152508:1-3, Oct. 2007.

D. Morecroft, I.A. Colin, F.J. Castaño, J.A.C. Bland, and C.A. Ross, "Current-induced magnetization reversal in NiFe/Cu/Co/Au notched mesoscopic bars," *Physical Review B*, vol. 76, no. 5, pp. 054449:1-8, Aug. 2007.

Y.S. Jung and C.A. Ross, "Orientation-controlled self-assembled nanolithography using a polystyrene-polydimethylsiloxane block copolymer, *Nano Letters*, vol. 7, no. 7, pp. 2046-2050, July 2007.

V. Sivakumar, S. Kumar, Y. Shao-Horn, and C.A. Ross, "Magnetic and structural investigation of electrochemically lithiated magnetite nanoparticles," *IEEE Transactions on Magnetics*, vol. 43, no. 6, pp. 3121-3123, June 2007.

F.Y. Ogrin, S.M. Weekes, B. Cubitt, A. Wildes, A. Drew, C.A. Ross, W. Jung, R. Menon, and B. Toperverg, "Polarized neutron reflectivity investigation of periodic magnetic rings," *IEEE Transactions on Magnetics*, vol. 43, no. 6, pp. 2731-2733, June 2007.

F. Ilievski, J.C. Perkinson, and C.A. Ross, "Magnetic reversal phenomena in pseudo spin valve films with perpendicular anisotropy," *Journal of Applied Physics*, vol. 101, no. 9, pp. 09D116:1-3, May 2007.

G.F. Dionne, A.R. Taussig, M. Bolduc, and C.A. Ross, "Mixed-cation designs of magnetic perovskites for Faraday rotation at IR wavelengths," *Journal of Applied Physics*, vol. 101, no. 9, pp. 09C524:1-3, May 2007.

Rahul Sarpeshkar
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

M. Fee, MIT
J. Wyatt, MIT

POSTDOCTORAL ASSOCIATE

L. Turicchia, EECS

GRADUATE STUDENTS

S. Arfin, Res. Asst., EECS
S. Mandal, Res. Asst., EECS
B. Rapoport, Grad. Student, EECS
J.J. Sit, Res. Asst., EECS
W. Wattanapanitch, Res. Asst., EECS
K.H. Wee, Res. Asst., EECS
S. Zhak, Res. Asst., EECS

SUPPORT STAFF

S. Davco, Admin. Asst.

PUBLICATIONS

K.H. Wee and R. Sarpeshkar, "An electronically tunable linear or nonlinear MOS resistor," *IEEE Transactions on Circuits and Systems I*, 2008, to be published.

J.J. Sit and R. Sarpeshkar, "A cochlear-implant processor for encoding music and lowering stimulation power," *IEEE Pervasive Computing,* vol. 7, no. 1, pp. 40-48, Jan. 2008.

S. Mandal and R. Sarpeshkar, "A bidirectional wireless link for neural prostheses that minimizes implanted power consumption," presented at the *IEEE Biological Circuits and Systems Conference,* Montreal, Canada, 2007.

J.J. Si and R. Sarpeshkar, "A low-power, blocking-capacitor-free, charge-balanced electrode-stimulator chip with less than 6nA DC error for 1mA full-scale stimulation," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 1, no. 3, pp. 172-183, Sept. 2007.

W. Wattanapanitch, M. Fee, and R. Sarpeshkar, "An energy-efficient micropower neural recording amplifier," *IEEE Transaction on Biomedical Circuits and Systems*, vol. 1, no. 2, pp. 136-147, June 2007.

B. Raj, L. Turicchia, B. Schmidt-Nielsen, and R. Sarpeshkar, "An FFT-based companding front end for noise-robust automatic speech recognition," *EURASIP Journal on Audio, Speech, and Music Processing,"* vol. 2007, pp. 65420:1-13, Apr. 2007.

Mark L. Schattenburg
Senior Research Scientst
MIT Kavli Institute

COLLABORATORS

H.I. Smith, MIT
D. Smith, PGL
D. Trumper, MIT
R. Hocken, UNCC

GRADUATE STUDENTS

M. Ahn, Res. Asst., ME
M. Akilian, Res. Asst., ME
C.-H. Chang, Res. Asst., ME
S. Slater, Res. Asst., Physics (Harvard)
Y. Zhao, Res. Asst., ME

SUPPORT STAFF

R. Fleming, Lab Manager
R. Heilmann, Lab Assoc. Director

PUBLICATIONS

C.-H. Chang, R.K. Heilmann, M.L. Schattenburg, and P. Glenn,"Design of a double-pass shear mode acousto-optical modulator," *Review of Scientific Instruments,* vol. 79, no. 3, pp. 033104:1-5, Mar. 2008.

M. Ahn, R.K. Heilmann and M. L. Schattenburg, "Fabrication of ultra-high aspect ratio freestanding gratings on silicon-on-insulator wafers," *Journal of Vacuum Science Technology B,* vol. 25, no. 6, 2593-2597, Nov. 2007.

Y. Zhao, C.-H. Chang, R.K. Heilmann, and M.L. Schattenburg, "Phase control in multiexposure spatial frequency multiplication," *Journal of Vacuum Science Technology B,* vol. 25, no. 6, pp. 2439-2443, Nov. 2007.

K. Flanagan, M. Ahn, J. Davis, R. Heilmann, D. Huenemoerder, A. Levine, H. Marshall, G. Prigozhin, A. Rasmussen, G. Ricker, M. Schattenburg, N. Schulz, and Y. Zhao, "Spectrometer concept and design for x-ray astronomy using a blazed transmission grating," in *Proc. SPIE Optics for EUV, X-Ray, and Gamma-Ray Astronomy III,* vol. 6688, pp. 66880Y:1-12, Sept. 2007.

M. Akilian, C.R. Forest, D.L. Trumper, A.H. Slocum, and M.L. Schattenburg, "Thin optic constraint," *Journal of Precision Engineering,* vol. 31, no. 2, pp. 130-138, Apr. 2007.

M. Akilian, R.K. Heilmann and M.L. Schattenburg, "Precision assembly of thin gratings for x-ray telescopes," in *Proc. 21st Annual Meeting of the American Society for Precision Engineering,* Monterey, CA, Oct. 2006, pp. 439-442.

Y. Zhao, D. Trumper R.K. Heilmann, and M.L. Schattenburg, "Sub-millidegree stability air thermal control for a large-volume lithography enclosure," in *Proc. 21st Annual Meeting of the American Society for Precision Engineering,* Monterey, CA, Oct. 2006, pp. 51-54.

J. Cottam, W. Cash, K.A. Flanagan, R.K. Heilmann, G.Y. Prigozhin, A.P. Rasmussen, G.R. Ricker, and M.L. Schattenburg, "The Constellation-X reflection grating spectrometer," *Proc. SPIE 6266, Space Telescopes and Instrumentation II: UV to Gamma Ray*, vol. 6266, June 2006, pp. 62661X:1-8.

M. Akilian, R.K. Heilmann, and M.L. Schattenburg, "Assembly of thin gratings for soft x-ray telescopes," *Proc. SPIE 6266, Space Telescopes and Instrumentation II: UV to Gamma Ray*, vol. 6266, June 2006, pp. 62663O:1-8.

J.F. Seely, L.I. Goray, B. Kjornrattanawanich, J.M. Laming, G.E. Holland, K.A. Flanagan, R.K. Heilmann, C.-H. Chang, M.L. Schattenburg, and A.P. Rasmussen, "Efficiency of a grazing-incidence off-plane grating in the soft x-ray region," *Applied Optics*, vol. 45, no. 8, pp. 1680-1687, Mar. 2006.

M.P. Kowalski, R.K. Heilmann, M.L. Schattenburg, C.-H. Chang, F.B. Berendse, and W.R. Hunter, "Near-normal-incidence extreme-ultraviolet efficiency of a flat crystalline anisotropically etched blazed grating," *Applied Optics*, vol. 45, no. 8, pp. 1676-1679, Mar. 2006.

C.R. Forest, M. Spenko, Y. Sun, A.H. Slocum, R.K. Heilmann, and M.L. Schattenburg, "Repeatable and accurate assembly of x-ray foil optics," *Journal of Precision Engineering,* vol. 30, no. 1, pp. 63-70, Jan. 2006.

C.-H. Chang, M. Akilian, and M.L. Schattenburg, "Describing isotropic and anisotropic out-of-plane deformations in thin cubic materials using Zernike polynomials," *Applied Optics*, vol. 45, no. 3, pp. 432-437, Jan. 2006.

J. Montoya, C.-H. Chang, R.K. Heilmann, and M.L. Schattenburg, "Doppler writing and linewidth control for scanning beam interference lithography," *Journal of Vacuum Science and Technology B,* vol. 23, no. 6, pp. 2640-2645, Nov. 2005.

C.-H. Chang, J.C. Montoya, M. Akilian, A. Lapsa, R.K. Heilmann, M.L. Schattenburg, M. Li, K.A. Flanagan, A.P. Rasmussen, J.F. Seely, J.M. Laming, B. Kjornrattanawanich, and L.I. Goray, "High fidelity blazed grating replication using nanoimprint lithography," *Journal of Vacuum Science-and Technology B*, vol. 22, no. 6, pp. 3260-3264, Nov. 2004.

R.K. Heilmann, C.G. Chen, P.T. Konkola, and M.L. Schattenburg, "Dimensional metrology for nanometer-scale science and engineering: towards sub-nanometer accurate encoders," *Nanotechnology,* vol. 15, no. 10, pp. S504-S511, Oct. 2004.

J. Montoya, R.K. Heilmann and M.L. Schattenburg, "Measuring two-axis stage mirror non-flatness using linear/angular interferometers," in *Proc. 19th Annual Meeting of the American Society for Precision Engineering*, Orlando, FL, Oct. 2004, vol. **34**, pp. 382-385.

Martin A. Schmidt

Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

A. Akinwande, MIT
V. Bulović, MIT
K.F. Jensen, MIT
S.G. Kim, MIT
C.G. Sodini, MIT
M. Chaparala, HP
J. Sims, Harvard-MGH
M. Toner, Harvard-MGH
D. Keszler, Oregon State University

RESEARCH STAFF

H. Li, Research Scientist
J. Chen, Post-Doctoral Associate
V. Leblanc, Post-Doctoral Associate

GRADUATE STUDENTS

K. Cheung, Res. Asst., EECS
E. Lam, Res. Asst., EECS
V. Sharma, Res. Asst., EECS
H. Zhou, Res. Asst., DMSE

ADMINISTRATIVE STAFF

A. Wasserman, Senior Administrative Staff

PUBLICATIONS

J. Chen, V. Leblanc, S.H. Kang, P.J. Benning, D. Shut, M.A. Baldo, M.A. Schmidt, and V. Bulović, "High definition digital fabrication of organic devices by molecular jet printing," *Advanced Functional Materials*, vol. 17, no. 15, pp. 2722-2727, Oct. 2007.

V. Leblanc, J. Chen, S.H. Kang, V. Bulović, and M.A. Schmidt, "Micromachined printheads for the evaporative patterning of organic materials and metals," *IEEE/ASME Journal of Microelectromechanical Systems,* vol. 16, no. 2, pp. 394-400, Apr. 2007.

L.R. Arana, N. deMas, R. Schmidt, A.J. Franz, M.A. Schmidt, and K.F. Jensen, "Isotropic etching of silicon in fluorine gas for MEMS micromachining," *Journal of Micromechanics and Microengineering,* vol. 17, no. 2, pp. 384-392, Feb. 2007.

Y. Wada, M.A. Schmidt, and K.F. Jensen, "Flow distribution and ozonolysis in gas-liquid multichannel microreactors," *Industrial & Engineering Chemistry Research,* vol. 45, no. 24, pp. 8036-8042, Nov. 2006.

B.A. Wilhite, S.E. Weiss, J.Y. Ying, M.A. Schmidt, and K.F. Jensen, "High-purity hydrogen generation in a microfabricated 23 wt % Ag-Pd membrane device integrated with 8:1 $LaNi_{0.95}Co_{0.0503}/Al_2O_3$ catalyst," *Advanced Materials,* vol. 18, no. 13, pp. 1701-1710, July 2006.

J.G. Kralj, M.T.W., Lis, M.A. Schmidt, and K.F. Jensen, "Continuous dielectrophoretic size-based particle sorting," *Analytical Chemistry,* vol. 78, no. 14, pp. 5019-5025, July 2006.

Alexander Slocum
Professor
Department of Mechanical Engineering

COLLABORATORS

J. Lang, MIT

POSTDOCTORAL ASSOCIATES

H. Ma

GRADUATE STUDENTS

A. Weber, ME
M. Reed, ME

SUPPORT STAFF

M. Lynch, Admin. Asst. II

PUBLICATIONS

H. Ma, J. Lang, and A.H. Slocum, "Permittivity measurements using adjustable microscale electrode gaps between millimeter-sized spherical electrodes," *Review of Science Instruments,* vol. 79, no. 3, pp. 035105:1-4, Mar. 2008.

L. van Laake, A.J. Hart, and A.H. Slocum, "A suspended heated silicon platform for rapid thermal control of surface reactions with application to carbon nanotube synthesis," *Review of Science Instruments*, vol, 78, no. 8, pp. 083901:1-9, Aug. 2007.

M. Akilian, C.R. Forest, A.H. Slocum, D.L. Trumper, and M.L. Schattenburg, "Thin optic constraint," *Precision Engineering,* vol. 31, no. 2, pp. 130-138, Apr. 2007.

O. Yaglioglu, A.J. Hart, R. Martens, and A.H. Slocum, "Method of characterizing electrical contact properties of carbon nanotube coated surfaces," *Review of Science Instruments,* vol. 77, no. 9, pp. 095105:1-3, Sept. 2006.

A.J. Hart and A.H. Slocum, "Force output, control of film structure, and microscale shape transfer by carbon nanotube growth under mechanical pressure," *NanoLetters,* vol. 6, no. 6, pp. 1254-1260, May 2006.

A.J. Hart and A.H. Slocum, "Rapid growth and flow-mediated nucleation of millimeter-scale aligned carbon nanotube structures from a thin-film catalyst," *Journal of Physical Chemistry B,* vol. 110, no. 16, pp. 8250-8257, Apr. 2006.

A.J. Hart, B.O. Boskovic, A.T.H. Chuang, V.B. Golovko, J. Robertson, B.F.G. Johnson, and A.H. Slocum, "Uniform and selective CVD growth of carbon nanotubes and nanofibres on arbitrarily microstructured silicon surfaces," *Nanotechnology*, vol. 17, no. 5, pp. 1397-1403, Mar. 2006.

A.J. Hart and A.H. Slocum, "Rapid growth and flow-mediated nucleation of millimeter-scale aligned carbon nanotube structures from a thin-film catalyst," *Journal of Physical Chemistry B,* vol. 110, no. 16, pp. 8250-8257, Mar. 2006.

A.J. Hart, A.H. Slocum, and L. Royer, "Growth of high-quality single-walled carbon nanotube films from Mo/Fe/Al_2O_3 deposited by electron beam evaporation," *Carbon*, vol. 44, no. 2, pp. 348–359, Feb. 2006.

E. Bamberg, C.P. Grippo, P. Wanakamol, A.H. Slocum, M.C. Boyce, and E.L. Thomas, "A tensile test device for in situ atomic force microscope mechanical testing," *Precision Engineering*, vol. 30, no. 1, pp. 71-84, Jan. 2006.

J. Li, M.P. Brenner, T. Christen, M.S. Kotilainen, J.H. Lang, and A.H. Slocum, "Deep reactive ion-etched compliant starting zone electrostatic zipping actuators," *Journal of Microelctromechanical Systems,* vol. 14, no. 6, pp. 1283-1297, Dec. 2005.

J.R. White, C.J. White, and A.H. Slocum, "Octave-tunable miniature rf resonators," *IEEE Microwave and Wireless Components Letters*, vol. 15, no. 11, pp. 793-795, Nov. 2005.

J. Qiu, J. Lang, A.H. Slocum, and A. Weber, "A bulk-micromachined bistable relay with u-shaped thermal actuators," *Journal of Microelctromechanical Systems*, vol. 14, no. 5, pp. 1099-1109, Oct. 2005.

Henry I. Smith
Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

J.T. Hastings, Univ. Kentucky
C.A. Ross, MIT
C.V. Thompson, MIT
F.R. Stellacci, MIT
E. Ippen, MIT
F. Kaertner, MIT
M. Schattenburg, MIT
E.L. Thomas, MIT

GRADUATE STUDENTS

W. Arora, Res. Asst., EECS
C. Fuceltola, Res. Asst., EECS
C. Holzwarth, Res. Asst., MSE
T.B. O'Reilly, Res. Asst., ME
A. Patel, Res. Asst., EECS
S. Tsai, Res. Asst., EECS

SUPPORT STAFF

T. Kuhn, Admin. Asst. I
J. Daley, Project Technician
M. Mondol, Facility Manager, SEBL
L. LaForce, Shop Helper, NSL
R.Menon, Research Scientist
T. Savas, Visiting Scientist
E.E. Moon, Research Scientist
F. Zhang, Research Affiliate

PUBLICATIONS

F.Y. Ogrin, E. Sirotkin, G. van der Laan, G. Beutier, C.A. Ross, W. Jung, and R. Menon, "Soft x-ray resonant magnetic scattering investigation of stable magnetic configurations in patterned rings," *Journal of Applied Physics*, vol. 103, no. 7, pp. 07E909:1-3, Apr. 2008.

T.B. O'Reilly and H.I. Smith, "Characterization of photoresist using double-exposure with interference lithography," *Journal of Vacuum Science and Technology B*, vol. 26, no. 1, pp. 128-131, Jan. 2008.

A.A. Patel and H.I. Smith, "Membrane stacking: A new approach for three-dimensional nanostructure fabrication," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2662-2664 Nov. 2007.

C. Holzwarth, T. Barwicz and H.I. Smith, "Optimization of hydrogen silsesquioxane films for photonic applications," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2658-2661, Nov. 2007.

W.J. Arora, S. Sijbrandij, L. Stern, J. Notte, H.I. Smith, and G. Barbastathis, "Membrane folding by He+ ion implantation for three-dimensional device fabrication," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2184-2187, Nov. 2007.

E.E. Moon, J. Kupec, M.K. Mondol, H.I. Smith, and K.K. Berggren, "Atomic-force lithography with interferometric tip-to-substrate position metrology," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2284-2287, Nov. 2007.

H-Y. Tsai, H.I. Smith, and R. Menon, "Fabrication of spiral-phase diffractive elements using scanning-electron beam-lithography," *Journal of Vacuum Science and Technology B*, vol. 25, no. 6, pp. 2068-2071, Nov. 2007.

W.J. Arora, H.I. Smith, and G. Barbastathis, "Membrane folding by ion implantation-induced stress to fabricate three-dimensional nanostructures," *Microelectronic Engineering*, vol. 84, no. 5-8, pp. 1454-1458, May-Aug. 2007.

I. Bita, T. Choi, M.E. Walsh, H.I. Smith and E.L. Thomas, "Large-area 3D nanostructures with octagonal quasicrystalline symmetry via phase mask lithography," *Advanced Materials*, vol. 19, no. 10, pp. 1403-1407, May 2007.

R. Menon, H.-Y. Tsai, and S.W. Thomas III, "Far-field generation of localized light fields using absorbance modulation," *Physical Review Letters*, vol. 98, no. 4, 043905:1-4, Jan. 2007.

T. Barwicz, M.R. Watts, M.A. Popović, P.T. Rakich, L. Socci, F.X. Kärtner, E.P. Ippen, and H.I. Smith "Polarization-transparent microphotonic devices in the strong confinement limit," *Nature Photonics*, vol. 1, no. 1, pp. 57-60, Jan. 2007.

T. Barwicz, H. Byun, F. Gan, C.W. Holzwarth, M.A. Popović, P.T. Rakich, M.R. Watts, E.P. Ippen, F.X. Kärtner, H.I. Smith, J.S. Orcutt, R.J. Ram, V. Stojanović, O.O. Olubuyide, J.L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J.U. Yoon, "Silicon photonics for compact, energy-efficient interconnects" (Inv.), *Journal of Optical Networking*, vol. 6, no. 1, pp. 63-73 Jan. 2007.

Charles G. Sodini

Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

P. Holloway, National Semiconductor

GRADUATE STUDENTS

F. Edalat, Texas Instruments Graduate Women's Fellow for Leadership in Microelectronics, EECS
D. He, Res. Asst., EECS
K. Lu, Res. Asst., EECS
I. Nausieda, Martin Family Society of Fellows for Sustainability, EECS
K. Nguyen, Res. Asst., EECS
J. Powell, Res. Asst., EECS
K. Ryu, Res. Asst., EECS

SUPPORT STAFF

S. Piccarini, Admin. Asst. II

PUBLICATIONS

H.-S. Lee and C.G. Sodini, "Analog-to-digital converters: Digitizing the analog world," *Proceedings of the IEEE*, vol. 96, no. 2, pp. 323-334, Feb. 2008.

I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C.G. Sodini, "An organic active-matrix imager *IEEE Transactions on Electron Devices*, vol. 55, no. 2, pp. 527-532, Feb. 2008.

A. Jerng and C.G. Sodini, "A wideband delta-sigma digital-RF modulator for high data rate transmitters," *IEEE Journal of Solid-State Circuits*, vol. 42, no- 8, August, 2007.

K. Ryu, I. Nausieda, I. Kymissis, V. Bulović, and C.G. Sodini, "Influence of source-drain contact resistance on accurate extraction of gate-bias-dependent charge carrier mobilities in organic FETs," presented at *Organic Microelectronics Workshop*, July, 2007.

J. Powell, H. Kim, and C.G Sodini, "A 77 GHz receiver front-end for passive imaging," presented at the *IEEE RFIC Symposium*, June 2007.

I. Nausieda, K. Ryu, I. Kymissis, A.I. Akinwande, V. Bulović, and C.G. Sodini, "An organic imager for flexible large area electronics," presented at the *IEEE International Solid-State Circuits Conference*, Feb. 2007.

J.K. Fiorenza, T. Sepke, P. Holloway, C.G. Sodini, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, pp. 2658-2668, Dec. 2006.

A. Jerng and C.G. Sodini, "A wideband delta-sigma digital-RF modulator with self-tuned RF bandpass reconstruction filter," in *Proc. IEEE Custom Integrated Circuits Conference*, San Jose, CA, Sept. 2006, pp. 125-128.

F. Edalat, J.K. Tan, K.M. Nguyen, N. Matalon, and C.G. Sodini, "Measured data rate from adaptive modulation in wideband OFDM systems," presented at *IEEE International Conference on Ultra Wide Band*, Sept. 2006.

A.Y. Wang and C.G. Sodini, "On the energy efficiency of wireless transceivers," in *Proc. IEEE International Conference on Communications*, Istanbul, Turkey, June 2006, pp. 3783-3788.

L. Khuon and C.G. Sodini, "An area-efficient 5-GHz multiple receiver RFIC for MIMO WLAN applications, presented at *IEEE Radio Frequency Integrated Circuits Symposium*, June 2006.

A. Pham and C.G. Sodini, "A 5.8-GHz, 47% efficiency, linear outphase power amplifier with fully integrated power combiner," *IEEE Radio Frequency Integrated Circuits Symposium*, June 2006.

A. Pham, G.W. Wornell, and C.G. Sodini, "A digital amplitude-to-phase conversion for high efficiency linear outphase power amplifiers," in *Proc. IEEE International Conference on Acoustics, Speech, and Signal Processing*, Toulouse, France, May 2006, pp. IV-97 - IV-100.

T. Sepke, J.K. Fiorenza, C.G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched-capacitor circuits for scaled CMOS technologies," in *Proc. IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2006, pp. 220-221, 649. (Recipient of the ISSCC 2006 Jack Kilby Outstanding Student Paper Award.)

D.B. Fuller, A.I. Akinwande, A.I., and C.G. Sodini, "Leading, following, or cooked goose? Explaining innovation, successes and failures in Taiwan's electronics industry," in *Global Taiwan: Building Competitive Strengths in a New International Economy*, S. Berger and R. Lester, Eds. Armonk: M.E. Sharpe, 2005.

K. Ryu, I. Kymissis, V. Bulović, and C.G. Sodini, "Direct extraction of mobility in pentacene OFETs using capacitance-voltage and current-voltage measurements," *IEEE Electron Device Letters*, vol. 26, no. 10, pp. 716-718, Oct. 2005.

R. Reif and C.G. Sodini, "Hong Kong electronics industry," in *Made by Hong Kong*, S. Berger and R. Lester, Eds. New York: Oxford University Press, 1997.

R.T. Howe and and C.G. Sodini, *Microelectronics: An Integrated Approach.* Upper Saddle River, NJ: Prentice Hall, 1997.

Vladimir Stojanović
Assistant Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

E. Alon, UC Berkeley
K. Asanovic, UC Berkeley
A. Kavcic, U. Hawaii
M. Horowitz, Stanford University
D. Markovic, UC Los Angeles
C-K. K. Yang, UC Los Angeles

GRADUATE STUDENTS

N. Blitvić, Res. Asst., EECS
F. Chen, Res. Asst., EECS
M. Georgas, Res. Asst., EECS
B. Kim, Res. Asst., EECS
J. Leu, Res. Asst., EECS
Y. Li, Res. Asst., EECS
B. Moss, Res. Asst., EECS
S. Song, Res. Asst., EESC
R. Sredojević, Res. Asst., EECS

PUBLICATIONS

N. Blitvic, L. Zheng, and V. Stojanović, "Low-complexity pattern-eliminating codes for ISI-limited channels," to appear in *IEEE International Communications Conference*, May 2008.

C.W. Holzwarth, J.S. Orcutt, H. Li, M.A. Popović, V. Stojanović, J.L. Hoyt, R.J. Ram, and H.I. Smith, "Localized substrate removal technique enabling strong-confinement microphotonics in bulk si CMOS processes," to appear in *Optical Society of America - CLEO/QELS Conference*, May 2008.

J.S. Orcutt, A. Khilo, M.A. Popović, C.W. Holzwarth, B. Moss, H. Li, M.S. Dahlem, T.D. Bonifield, F.X. Kärtner, E.P. Ippen, J.L. Hoyt, R.J. Ram and V. Stojanović, "Demonstration of an electronic photonic integrated circuit in a commercial scaled bulk CMOS process,"presented at the *Optical Society of America - CLEO/QELS Conference*, May 2008.

A. Amirkhany, A. Abbasfar, J. Savoj, M. Jeeradit, B. Garlepp, V. Stojanović, and M. A. Horowitz, "A 24Gb/s software programmable analog multi-tone transmitter," *IEEE Journal of Solid-State Circuits,* vol. 43, no. 4, pp. 999-1009, Apr. 2008.

B. Kim and V. Stojanović, "Equalized interconnects for on-chip networks: modeling and optimization framework," in *Proc. IEEE/ACM International Conference on Computer-Aided Design*, San Jose, CA, Nov. 2007, pp. 552-559.

F. Chen, A. Joshi, V.Stojanović, and A.P. Chandrakasan, "Scaling and evaluation of carbon nanotube interconnects for VLSI applications," in *Proc. ACM International Conference on Nano-Networks*, Catania, Italy, Sept. 2007.

A. Amirkhany, A. Abbasfar, V. Stojanović and M.A. Horowitz, "Practical limits of multi-tone signaling over high-speed backplane electrical links," in *Proc. IEEE International Conference on Communications*, Glasgow, Scotland, June 2007., pp. 2693-2698,

N. Blitvic and V. Stojanović, "Statistical simulator for block coded channels with long residual interference," in *Proc. IEEE International Conference on Communications*, Glasgow, Scotland, June, 2007, pp. 6287-6294.

A. Amirkhany, A. Abbasfar, J. Savoj, M. Jeeradit, B. Garlepp, V. Stojanović, and M. Horowitz, "24 Gbps, software programmable multi-channel transmitter," in *Proc. IEEE Symposium on VLSI Circuits*, Kyotom, Japan, June 2007, pp. 38-39.

E.-H. Chen, J. Ren, J. Zerbe, B. Leibowitz, H. Lee, V. Stojanović, and C.-K. K. Yang, "BER-based adaptation of I/O link equalizers," *IEEE Symposium on VLSI Circuits*, pp. 36-37, June 2007.

J. Ren, H. Lee, Q. Lin, B. Leibowitz, E..-H. Chen, D. Oh, F. Lambrecht, V. Stojanović, C.-K.K. Yang, and J. Zerbe, "Precursor ISI reduction in high-speed I/O," *IEEE Symposium on VLSI Circuits*, pp. 134-135, June 2007.

S. Vamvakos, V. Stojanović, J. Zerbe, C. Werner, D. Draper and B. Nikolic, "PLL on-chip jitter measurement: analysis and design," *Symposium on VLSI Circuits Digest of Technical Papers*, pp. 73-74, Feb. 2007..

B.S. Leibowitz, J. Kizer, H. Lee, F. Chen, A. Ho, M. Jeeradit, A. Bansal, T. Greer, S. Li, R. Farjad-Rad, W. Stonecypher, Y. Frans, B. Daly, F. Heaton, B.W. Gariepp, C.W. Werner, N. Nguyen, V. Stojanović and J.L. Zerbe, "A 7.5Gb/s 10-Tap DFE receiver with first tap partial response, spectrally gated adaptation, and 2nd-order data-filtered CDR," *IEEE International Solid-State Circuits Conference*, San Francisco, CA, Feb. 2007, pp. 228-599.

T. Barwicz, H. Byun, F. Gan, C. W. Holzwarth, M.A. Popovic, P.T. Rakich, M.R. Watts, E.P. Ippen, F.X. Kärtner, H.I. Smith, J.S. Orcutt, R.J. Ram, V. Stojanović, O.O. Olubuyide, J.L. Hoyt, S. Spector, M. Geis, M. Grein, T. Lyszczarz, and J. U. Yoon, "Silicon photonics for compact, energy-efficient interconnects [Invited]," *Journal of Optical Networking*, vol. 6, no. 1, pp.63-73, Jan. 2007.

A. Amirkhany, A. Abbasfar, V. Stojanović, and M.A. Horowitz, "Analog multi-tone signaling for high-speed backplane electrical links," in *Proc. IEEE Global Communications Conference,* San Francisco , CA, Nov. 2006.

H. Hatamkhani, F. Lambrecht, V. Stojanović and C.K. Yang, "Power-centric design of high-speed I/Os," in *Proc. 43rd ACM/IEEE Design Automation Conference*, San Francisco, CA, July, 2006, pp. 867-872.

Carl V. Thompson

Stavros Salapatas Professor of Materials Science and Engineering
Department of Material Science & Engineering

COLLABORATORS

W.K. Choi, National University of Singapore (NUS)
S.J. Chua, NUS
C.L. Gan, Nanyang Technical University
E.A. Fitzgerald, MIT
C. Hau-Riege, Advanced Micro Devices
Y. Li, NUS
Y.J. Park, Texas Instruments
H.I. Smith, MIT

POSTDOCTORAL ASSOCIATES

J. Kalb
D. Kim
R. Monig
Y. Wang

GRADUATE STUDENTS

N. Abate, Visiting Student., MSE
S. Boles, Res. Asst., MSE
S.-W. Chang, Res. Asst., MSE
Z. Choi, Res. Asst., MSE
T. Chookajorn, Res. Asst., MSE
P. Delcroix, Visting Student, MSE
A. Giermann, Intel Fellow, MSE
J. Leib, NSF Fellow, MSE
H.L. Leong, SMA Fellow, MSE
R. Mitchell, Xerox Fellow, MSE
R. Nagarajan, SMS Fellow, MSE
G.D. Nessim, Intel Fellow, MSE
J. Oh, Res. Asst., MSE
T.J. Park, Res. Asst., MSE
G. Qiang, SMA Fellow, NUS
M. Seita, Res. Asst., MSE
W. Sasangka, SMA Fellow, MSE
F.L. Wei, Res. Asst., MSE
P. Yang, Visiting student, MSE
J. Ye, Res. Asst., MSE
L. You, Visiting Student, MSE
H. Yu, Res. Asst., MSE
J. Yun, SMA Fellow, NUS

SUPPORT STAFF

K.A. Fitzgerald, Admin. Asst. II

PUBLICATIONS

J. Oh and C.V. Thompson, "Selective barrier perforation in porous alumina anodized on substrates," *Advanced Materials*, vol. 20, no. 7, pp. 1368-1372, Apr. 2008.

W.K. Choi, T.H. Liew, H.G. Chew, F. Zheng, C.V. Thompson. Y. Wang, M.H. Hong, X.D. Wang , L. Li and J. Yun, "A combined top-down and bottom-up approach for precise placement of metal nanoparticles on silicon," *Small*, vol. 4, no. 3, pp. 330-333, Mar. 2008.

R. Tadepalli, K.T. Turner, and C.V. Thompson, "Mixed-mode interface toughness of wafer-level Cu–Cu bonds using asymmetric chevron test," *Journal of the Mechanics and Physics of Solids*, vol. 56, no. 3, pp. 707-718, Mar. 2008.

R. Tadepalli, K.T. Turner and C.V. Thompson, "Effects of patterning on the interface toughness of wafer-level Cu-Cu bonds," *Acta Materialia*, vol. 56, no. 3, pp. 438-447, Feb. 2008.

Z.-S. Choi, R. Mönig, and C.V. Thompson, "Effects of microstructure on the formation, shape, and motion of voids during electromigration in passivated copper interconnects," *Journal of Materials Research*, vol. 23, no. 2, pp. 383-391, Feb. 2008.

H.L. Leong, C.L Gan, C.V. Thompson, K.L Pey, and H.Y. Li, "Application of contact theory to metal-metal bonding of silicon wafers," *Journal of Applied Physics*, vol. 102, no, 10, pp. 103510:1-9, Nov. 2007.

Z.-S. Choi, R. Mönig, and C.V. Thompson, "Activation energy and pre-factor for surface electromigration and void drift in Cu interconnects," *Journal of Applied Physics*, vol. 102, no. 8, pp. 083509:1-4, Oct. 2007.

Z.-S. Choi, R. Mönig, and C.V. Thompson, "Dependence of the electromigration flux on the crystallographic orientations of different grains in polycrystalline copper interconnects," *Applied Physics Letters*, vol. 90, no. 24, pp. 241913:1-3, June 2007.

C.W. Chang, C.V. Thompson, C.L. Gan, K.L. Pey, W.K. Choi, and Y. K. Lim, "Effects of micro-voids on the line-width dependence of electromigration failure of dual-damascene copper interconnects," *Applied Physics Letters*, vol. 90, no. 19, pp. 193505:1-3, May 2007.

R. Tadepalli and C.V. Thompson, "Formation of Cu–Cu interfaces with ideal adhesive strengths via room temperature pressure bonding in ultrahigh vacuum," *Applied Physics Letters*, vol. 90, no. 15, pp. 151919:1-3, Apr. 2007.

R. Krishnan and C.V. Thompson, "Monodomain high aspect ratio 2-D and 3-D ordered porous alumina structures with independently controlled pore spacing and diameter," *Advanced Materials*, vol. 19, no. 7, pp. 988-992, Apr. 2007.

S.M. Alam, C.L. Gan, C.V. Thompson, and D.E. Troxel, "Reliability computer-aided design tool for full-chip electromigration analysis and comparison with different interconnect metallizations," *Microelectronics Journal*, vol. 38, no. 4-5, pp. 463-473, Apr. 2007.

K.Y. Zang, Y.D.Wang, L.S. Wang, S. Tripathy, S.J. Chua, and C.V. Thompson, "Nanoheteroepitaxy of GaN on a nanopore array of Si(111) surface," *Thin Solid Film*s, vol. 515, no. 10, pp. 4505-4508, Mar. 2007.

H. Li, Q. Zhang, N. Peng, N. Liu, Y.C. Lee, O.K. Tan, N. Marzari, and C.V. Thompson, "Charge-trapping effects caused by ammonia in carbon nanotubes," *Journal of Nanoscience and Nanotechnology*, vol. 7, no. 1, pp. 335-338, Jan. 2007.

Harry L. Tuller
Professor
Department of Materials Science and Engineering

COLLABORATORS

I. D. Kim, KIST, Korea
E. Ivers-Tiffee & D. Gerthsen, University of Karlsruhe, Germany
M. Martin & R. DeSouza, Aachen University, Germany
J. Lewis, Univ. of Illinios
A. Rothschild, Technion, Israel

GRADUATE STUDENTS

W. Jung, Res. Asst., MSE
Y. Jin, Res. Asst., MSE
S. Litzelman, Res. Asst., MSE
G. Whitfield, Res. Asst., MSE
V. Sonn, Res. Asst., MSE (visiting student from Germany)

SUPPORT STAFF

T. Chung, Admin. Asst. II

PUBLICATIONS

A. Bieberle-Hütter, J.L. Hertz, and H.L. Tuller, "Fabrication and wlectrochemical characterization of planar Pt-CGO microstructures," *Acta Materialia,* vol. 56, no. 2, pp. 177-187, Jan. 2008.

J.L. Hertz and H.L. Tuller, "Measurement and finite element modeling of triple phase boundary-related current constriction in YSZ," *Solid State Ionics*, vol. 178, nos. 13-14, pp. 915-923, May 2007.

H. Seh, H. Fritze, and H.L. Tuller, "Defect chemistry of langasite III: Predictions of electrical and gravimetric properties and application to operation of high temperature crystal microbalance," *Journal of Electroceramics,* vol. 18, no. 1-2, pp. 139-147, Apr. 2007.

J.L. Hertz and H.L. Tuller, "Nanocomposite platinum-yttria stabilized zirconia electrode and implications for micro solid oxide fuel cell operation," *Journal of the Electrochemical Society*, vol. 154, no. 4, pp. B413-B418, Feb. 2007.

J. Hiltunen, D. Seneviratne, R. Sun, M. Stolfi, H.L. Tuller, J. Lappalainen, and V. Lantto, "$BaTiO_3$-$SrTiO_3$ multilayer thin-film electro-optic waveguide modulator," *Applied Physics Letters*, vol. 89, no. 24, pp. 242904-242906, Dec. 2006.

H.-S. Kim, I.-D. Kim, K.-B. Kim, T.-S. Yun, J.-C. Lee, H.L. Tuller, W.-Y. Choi, and H.-G. Kim, "Low frequency and microwave performances of Ba0.6Sr0.4TiO3 films on atomic layer deposited TiO2/High resistivity si substrates," *Journal of Electroceramics*, vol. 17, no. 2-4, pp. 421-425, Dec. 2006.

T. Hyodo, A. Bieberle-Hütter, J.L. Hertz, and H.L. Tuller, "Three dimensional arrays of hollow gadolinia-doped ceria microspheres prepared by R.F. magnetron sputtering employing PMMA microsphere templates," *Journal of Electroceramics*, vol. 17, nos. 2-4, pp. 695-699, Dec. 2006.

A. Rothschild and H.L. Tuller, "Gas sensors: new materials and processing approaches," *Journal of Electroceramics*, vol. 17, nos. 2-4, pp. 1005-1012, Dec. 2006.

P. Hofmann, K. Jacobs, H. Federmann, M. Schulz, H. Fritze, and H.L. Tuller, "Growth and high-temperature properties of gallium orthophosphate," *Solid State Ionics*, vol. 177, no. 35-36, pp. 3175-3178, Nov. 2006.

H. Fritze, M. Schulz, H. Seh, H.L. Tuller, S. Ganschow, and K. Jacobs, "High-temperature electromechanical properties of strontium-doped langasite," *Solid State Ionics*, vol. 177, no. 35-36, pp. 3171–3174, Nov. 2006.

M.-H. Lim, K.T. Kang, and H.-G. Kim, I.-D. Kim , Y.W. Choi, and H.L. Tuller, "Low leakage current - stacked MgO/Bi1.5Zn1.0Nb1.5O7 gate insulator - for low voltage ZnO thin film transistors," *Applied Physics Letters*, vol. 89, no. 20, pp. 202908:1-3, Nov. 2006.

H. Fritze, M. Schulz, H. Seh, and H.L. Tuller, "Sensor application-related defect chemistry and electromechanical properties of langasite," *Solid State Ionics*, vol. 177, nos. 26-32, pp. 2313–2316, Oct. 2006.

H.L. Tuller, "Ionic conduction and applications," in *Springer Handbook of Electronic and Photonic Materials,* S. Kasap and P. Capper, Eds. New York, NY: Springer Verlag, 2006,

A. Bieberle-Hütter, M. Søgaard, and H.L. Tuller, "Electrical and electrochemical characterization of microstructured thin film La1-xSrxCoO3 electrodes," *Solid State Ionics*, vol. 177, no. 19-25, pp. 1969-1975, Oct. 2006.

I-D. Kim, A. Rothschild, B.H. Lee, D.Y. Kim, S.M. Jo, and H.L. Tuller, "Ultrasensitive chemiresistors based on electrospun TiO2 nanofibers," *Nano Letters*, vol. 6, no. 9, pp. 2009-2013, Sept. 2006.

A. Rothschild, W. Menesklou, H.L. Tuller, and E. Ivers-Tiffée, "Electronic structure, defect chemistry, and transport properties of SrTi1-xFexO3-y solid solutions," *Chemistry of Materials*, vol. 18,no. 16, pp. 3651-3659, Aug. 2006.

A. Bieberle-Hütter and H.L. Tuller, "Fabrication and structural characterization of interdigitated thin film La1–xSrxCoO3 (LSCO) electrodes," *Journal of Electroceramics*, vol. 16, no. 2, pp. 151-157, Mar. 2006.

H. Seh and H.L. Tuller, "Defects and transport in langasite I: Acceptor-doped La3Ga5SiO14," *Journal of Electroceramics*, vol. 16, no. 2, pp. 115–125, Mar. 2006.

Joel Voldman
Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

G. Daley, Children's Hospital
R. Jaenish, MIT
K.M. Lim, NUS, Singapore
F. McKeon, Harvard Med. School
P. Sorger, Harvard Med. School
J. White, MIT

POSTDOCTORAL ASSOCIATES

A.M. Skelley
W.-M. Tsang
K. Blagović

GRADUATE STUDENTS

S. Desai, Res. Asst., EECS
L.Y. Kim, Res. Asst., HST
J.R. Kovac, Res. Asst., EECS
N. Mittal, Res. Asst., Physics
L. Pryzbyla, Res. Asst., Biology
P. Sampattavanich, Res. Asst., HST
B. Taff, Res. Asst., EECS
M. Vahey, Res. Asst., EECS

SUPPORT STAFF

C. Collins, Admin. Asst. II

PUBLICATIONS

M.D. Vahey and J. Voldman, "A new equilibrium method for continuous-flow cell sorting using dielectrophoresis," *Analytical Chemistry*, vol. 80, no. 9, pp. 3135-3143, Mar. 2008.

H.-H. Cui, K.-M. Lim, S.-P. Lim, B.-C. Khoo, and J. Voldman, "Microparticle separation using dynamic pulsed dielectrophoresis," presented at the *22nd International Symposium on MicroScale Bioseparations & Methods for Systems Biology,* 2008.

S.P. Desai, B.M. Taff, and J. Voldman, "A photopatternable silicone for biological microsystems," *Langmuir,* vol. 24, no. 2, pp. 575-581, Jan. 2008.

J.R. Kovac. and J. Voldman, "Intuitive, image-based cell sorting using opto-fluidic cell sorting," *Analytical Chemistry,* vol. 79, no. 24, pp. 9321-9330, Dec. 2007.

S.P. Desai, M.D. Vahey, and J. Voldman, "Vesicle libraries - tools for dielectrophoresis metrology," in *Proc. 11th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Paris, France, Oct. 2007, pp. 1104-1106.

M.D. Vahey, R.J. Barsotti, R. Wartena, Y.-M. Chiang, F. Stellacci, and J. Voldman, "Modeling the electrokinetics of nanoparticles for controlled assembly," in *Proc. 11th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Paris, France, Oct. 2007, pp. 991-999.

A.M. Skelley, O. Kirak, R. Jaenisch, and J. Voldman, "Studying reprogramming of somatic cells via fusion with embryonic s tem cells: a massively parallel device for cell fusion," in *Proc. 11th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Paris, France, Oct. 2007, pp. 581-583.

S.P. Desai, B.M. Taff, and J. Voldman, "A photopatternable silicone for BioMEMS applications," in *Proc. 11th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Paris, France, Oct. 2007, pp. 448-450.

B.M. Taff, S.P. Desai, and J. Voldman, "Dielectrophoretically switchable microfluidic weir structures for exclusion-based single-cell manipulation," in *Proc. 11th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Paris, France, Oct. 2007, pp. 8-10.

N. Mittal, A. Rosenthal, and J. Voldman, "nDEP microwells for single-cell patterning in physiological media," *Lab on a Chip*, vol. 7, no. 9, pp. 1146-53, Sept. 2007.

A. Rosenthal, A. Macdonald, and J. Voldman, "Cell patterning chip for controlling the stem cell microenvironment," *Biomaterials,* vol. 28, no. 21, pp. 3208-3216, July 2007.

L. Kim, Y.C. Toh, J. Voldman, and H. Yu, "A practical guide to microfluidic perfusion culture of adherent mammalian cells," *Lab on a Chip*, vol. 7, no. 6, pp. 681-694, June 2007.

H.-Y. Lee and J. Voldman, "Optimizing micromixer design for enhancing dielectrophoretic microconcentrator performance," *Analytical Chemistry,* vol. 79, no. 5, pp. 1833-1839, Mar. 2007.

R.J. Barsotti, M.D. Vahey, R. Wartena, Y.-M. Chiang, J. Voldman, and F. Stellacci, "Assembly of metal nanoparticles into nanogaps," *Small*, vol. 3, no. 3, pp. 488-499, Mar. 2007.

E. Kim, M.J. Mescher, H.Y. Lee, J. Voldman, and J. Fiering, "Microfluidic continuous bacteria concentrator with integrated microvalves," presented at the *20th International Symposium on Microscale Bioseparations,* 2007.

N. Gadish and J. Voldman, "High-throughput positive-dielectrophoretic bioparticle microconcentrator," *Analytical Chemistry,* vol. 78, no. 22, pp. 7870-7876, Nov. 2006.

J. Voldman, "Engineered systems for the physical manipulation of single cells," *Current Opinion in Biotechnology*, vol. 17 no. 5, pp. 532-537, Aug. 2006.

J. Voldman, "Electrical forces for microscale cell manipulation," *Annual Review of Biomedical Engineering,* vol. 8, pp. 425-454, Aug. 2006.

J. Voldman, "Dielectrophoretic traps for cell manipulation," in *BioMEMS and Biomedical Nanotechnology Volume IV: Biomolecular Sensing, Processing and Analysis,* M. Ferrari, R. Bashir and S. Wereley, Eds. New York, NY: Springer US, 2006.

J.R. Kovac and J. Voldman, "Facile image-based cell sorting using OPTO-FluCS (Opto-fluidic cell sorting)," in *Proc. 10th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Tokyo, Japan, Nov. 2006, pp. 1483-1485.

M.D. Vahey and J. Voldman, "Iso-dielectric Separation: A new method for the continuous-flow screening of cells," in *Proc. 10th International Conference on Miniaturized Systems for Chemistry and Life Sciences,* Tokyo, Japan, Nov. 2006, pp. 1058-1060.

Evelyn N. Wang
Assistant Professor
Department of Mechanical Engineering

COLLABORATORS

D. Streit, Northrop-Grumman
J. Karp, HST

GRADUATE STUDENTS

B. Alexander, Res. Asst., ME
K. Chu, Res. Asst., ME
R. Xiao, Res. Asst., ME

SUPPORT STAFF

D. Hanna, Admin. Asst. II

PUBLICATIONS

T.N. Krupenkin, J.A. Taylor, E.N. Wang, P. Kolodner, M. Hodes, and T.R. Salamon,"Reversible wetting-dewetting transitions on electrically tunable superhydrophobic nanostructured surfaces," *Langmuir*, vol. 23, no. 18, pp. 9128-9133, Aug. 2007.

C.H. Hidrovo, T.A. Kramer, E.N. Wang, S. Vigneron, J.E. Steinbrenner, J.-M. Koo, F.-M. Wang, D.W. Fogg, R.D. Flynn, E.S. Lee, C.-H. Cheng, T.W. Kenny, J.K. Eaton, and K.E. Goodson, "Two-phase microfluidics for semiconductor circuits and fuel cells," *Heat Transfer Engineering*, vol. 27, no. 4, pp. 53-63, May 2006.

E.N. Wang, S. Devasenathipathy, H. Lin, C.H. Hidrovo, J.G. Santiago, K.E. Goodson, and T.W. Kenny, "A hybrid method for bubble reconstruction in two-phase microchannels," *Experiments in Fluids* , vol. 40, no. 5, pp. 847-858, May 2006.

T.W. Kenny, K.E. Goodson, J.G. Santiago, E. Wang, J.-M. Koo, L. Jiang, L. Zhang, D. Fogg, S. Yao, K. Yao, R. Flynn, C.-H. Cheng, and C. Hidrovo, "Advanced cooling technologies for microprocessors," *International Journal of High Speed Electronics and Systems,* vol. 16, no. 1, pp. 301-313, Mar. 2006.

L. Zhang, E.N. Wang, K.E. Goodson, and T.W. Kenny, **"**Phase change phenomena in silicon microchannels," *International Journal of Heat and Mass Transfer,* vol. 48, no. 8, pp. 1572-1582, Apr. 2005.

E.N. Wang, S. Devasenathipathy, J.G. Santiago, K.E. Goodson, and T.W. Kenny, "Nucleation and growth of vapor bubbles in a heated silicon microchannel," *Journal of Heat Transfer*, vol. 126, no. 4, p. 497, Aug. 2004.

E.N. Wang, L. Zhang, L. Jiang, J.-M. Koo, J.G. Maveety, E.A. Sanchez, K.E. Goodson, and T.W. Kenny, "Micromachined jets for liquid impingement cooling of VLSI chips," *IEEE Journal of MicroElectroMechanical Systems,* vol. 13, no, 5, pp. 833-842, Oct. 2004.

A. Balandin, K.L. Wang, S. Cai, R. Li, C.R. Viswanathan, E.N. Wang, and M. Wojtowicz, "Investigation of flicker noise level and deep levels in AlGaN/GaN heterostructure field effect transistors," *Journal of Electronic Materials*, vol. 29, no. 3, pp. 297-301, Mar. 2000.

Brian L. Wardle
Assistant Professor
Department of Aeronautics and Astronautics

COLLABORATORS

H.-M. Duong, MIT XVI Postdoc
E.J. Garcia, Gamesa
R. Guzman deVilloria, MIT XVI Postdoc
A J. Hart, Univ. of Michigan
K.F. Jensen, MIT Chem. E.
W.-S. Kim, MIT XVI Postdoc
S.-G. Kim, MIT ME
S.-H. Kim, Inostek
S. Maruyama, Univ. of Tokyo
A. Miravete, Univ. Zaragoza
D. Papavassiliou, Univ. Oklahoma
D.-S. Park, KIMS
M.A. Schmidt, MIT EECS
A.H. Slocum, MIT ME
S.M. Spearing, Univ. Southampton
C. Thompson, MIT DMSE
H. Tuller, MIT DMSE
N. Wicks, Schlumberger

GRADUATE STUDENTS

H. Cebeci, Visiting Student, AA
F. Fachin, Res. Asst., AA
S. Figueredo, Res. Asst., ME
K. Ishiguro, Visiting Student, AA
M. Kim, Res. Asst., DMSE
S. Steiner, Res. Asst., AA
S. Wicks, Res. Asst., AA
N. Yamamoto, Res. Asst., AA

UNDERGRADUATE STUDENTS

T. Blackman, ME
H. Jeffrey, AA
L. Megalini, Politecnico di Torino (visiting)
D.S. Saito, ITA (visiting)
M. Tsai, AA
M. Zunino, AA

SUPPORT STAFF

J. Kane, Research Specialist
P. Lee, Financial Officer
M. Prendergast, Admin. Assist. II

PUBLICATIONS

E.J. Garcia, B.L. Wardle, A.J. Hart, and N. Yamamoto, "Fabrication and multifunctional properties of a hybrid laminate with aligned carbon nanotubes grown in situ," *Composites Science and Technology*, vol. 68, no. 9, pp. 2034-2041, July 2008.

D. Saito, B.L. Wardle, E.J. Garcia, L. Megalini, A.J. Hart, and R. Guzman deVilloria, "Fabrication and multifunctional properties of high volume fraction aligned carbon nanotube polymeric composites," AIAA-2008-1769, presented at the *49th AIAA Structures, Dynamics, and Materials Conference*, Schaumburg, IL, Apr. 2008.

L. Megalini, D. Saito, E.J. Garcia, B.L. Wardle, A.J. Hart, and O. Yaglioglu, "DC and AC properties of aligned carbon nanotube forests and polymeric nanocomposites," AIAA-2008-1854, presented at the *49th AIAA Structures, Dynamics, and Materials Conference*, Schaumburg, IL, Apr. 2008.

N. Yamamoto, and B.L. Wardle, "Thermal and electrical properties of hybrid woven composites reinforced with aligned carbon nantoubes," AIAA-2008-1857, presented at the *49th AIAA Structures, Dynamics, and Materials Conference*, Schaumburg, IL, Apr. 2008.

D. Quinn, B.L. Wardle, and S.M. Spearing, "Residual stress and microstructure of as-deposited and annealed sputtered yttria stabilized zirconia thin films," to appear in *Journal of Materials Research*, vol. 23, no. 3, pp.609-618, Mar. 2008.

E.J. Garcia, J. Hart, and B.L. Wardle, "Long carbon nanotubes grown on the surface of fibers for hybrid composites," *AIAA Journal*, vol. 6, no. 6, pp. 1405-1412, Mar. 2008.

B.L. Wardle, D.S.,Saito, E.J. Garcia, A.J. Hart, and R. Guzman deVilloria, "Fabrication and characterization of ultra-high volume fraction aligned carbon-nanotube-polymer composites," *Advanced Materials*, 2008, to be published.

E.J. Garcia, B.L. Wardle, and A.J. Hart, "Joining prepreg composite interfaces with aligned carbon nanotubes," *Composites Part A*, vol. 39, pp. 1065-1070, Mar. 2008.

D. Bello, A.J. Hart, K. Ahn, M. Hallock, N. Yamamoto, E. Garcia, E.J. Ellenbecker, and B.L. Wardle, "Particle exposure levels during CVD growth and subsequent handling of vertically-aligned carbon nanotube films," *Carbon*, vol. 46, pp. 974-978, Feb. 2008.

E.J. Garcia, J. Hart, B.L. Wardle, and A. Slocum, "Fabrication and nanocompression testing of aligned CNT/Polymer nanocomposites," *Advanced Materials*, vol. 19 pp.2151-2156, Aug. 2007.

N.E. duToit and B. L. Wardle, "Experimental verification of models for microfabricated piezoelectric vibration energy harvesters," *AIAA Journal*, vol. 45, no. 5, pp. 1126-1137, May 2007.

E.J. Garcia, J. Hart, B.L. Wardle, and A. Slocum, "Fabrication of composite microstructures by capillarity-driven wetting of aligned carbon nanotubes with polymers," *Nanotechnology*, vol. 18, no. 16, pp. 165602:11, Apr. 2007.

N.E. duToit, and B.L. Wardle, "Performance of microfabricated piezoelectric vibration energy harvesters," *Integrated Ferroelectrics,* vol. 83, no. 1, pp.13-23, Nov. 2006 .

N.E. duToit, B.L. Wardle, and S.-G. Kim, "Design considerations for MEMS-scale piezoelectric vibration energy harvesters," *Integrated Ferroelectrics*, vol. 71, no.1, pp. 121-160, July 2005.

8 Theses Awarded, 2007-2008

Bachelor of Science

Ashiabor, A. (J. Tilly, D.J. Perreault)	**Multiple LED Driver with Independent PWM Dimming and Fast Settling Time**
Berberian, S.J. (S.-G. Kim)	**Development of an In-Line Putter for Handicap Friendly Tabletop Golf Games**
Coleman, C. (S.-G. Kim)	**Design of a height adjustable wheelchair**
DiGenova, K. (S.-G. Kim)	**Design of a height adjustable wheelchair**
Gardner, J. (L. Shtargot, D.J. Perreault)	**Low-Ripple Micropower Buck Regulator**
Jeon, J. (S.-G. Kim)	**Printing PZT**
Kang, H. (S.-G. Kim)	**An analysis of Hybrid-Electric Vehicles as the Car of the Future**
Lah, M. (S.-G. Kim)	**Modeling of vortex-induced flow vibration along the trans Alaskan pipeline**
Lin, D. (R. Kapusta, D.J. Perreault)	**An Exploratory Design of a 65 nm CMOS Buck Converter for Maximum Efficiency**
Maher, P. (A. Hoefel, D.J. Perreault)	**Voltage Control for Permanent Magnet Downhole Alternators**
Mesa, A. (D.J. Perreault, T.A. Keim)	**Improved Performance Alternator with Switched-Mode Rectifier**
Pilawa, R. (D.J. Perreault)	**Investigation of a Very High Frequency dc-dc Power Converter**
Ranson, J. (D.J. Perreault)	**An Induction Teapot Warmer**
Saito, D.(ITA Brazil) (B. Wardle)	**Fabrication and Characterization of Aligned Carbon Nanotube Epoxy Composites**
Schrock, K. (J.C. Mayes, D.J. Perreault)	**A High-Voltage Low-Loss Three-Level Multi-Stage Inverter**
Stonely, A. (D.J. Perreault)	**Synchronous Buck Converter and Filter Demo**
Whitaker, M. (M. Vitunic, D.J. Perreault)	**Improving the Control Strategy for a Four-Switch Buck-Boost Converter**
Zhou, S. (S. Martin, D.J. Perreault)	**New Architecture for USB Powered Battery Charger**

Master of Science

Alexander, B. (E. Wang)	**Design of a Microbreather for Two-Phase Microchannel Devices**
Amataya, R. (R.J. Ram)	**Optimization of Tunable Silicon Compatible Microring Filters**
Bathurst, S. (S.-G. Kim)	**Thermal Ink Jetting of PZT Sol Gel Films using TIPS**
Ben-Simon, Y. (C.G. Sodini)	**Where India Fits Within Flextronics Global Supply Chain**
Blitvic, N. (V. Stojanovic)	**Channel Coding for High Speed Links**

Master of Science *continued*

Chandrasekhar, V. (A.P. Chandrakasan)	**CAD for a 3-Dimensional FPGA**
Cho, T.S. (A.P. Chandrakasan)	**An Energy Efficient CMOS Interface to Carbon Nanotube Sensor Arrays**
Chu, Y.J. (H.-S. Lee)	**A High Performance Zero-Crossing Based Pipelined Analog-to-Digital Converter**
Chung, J. (T. Palacios)	**Advanced Technologies for Improving High Frequency Performance of AlGaN/GaN High Electron Mobility Transistors**
Colin, I. (C.A. Ross)	**Field and current induced magnetization reversal in patterned Pseudo Spin Valve devices**
Communal, C. (D.S. Boning)	**Challenges Faced by a Global Team: the Case of the Tool Reuse Program at Intel**
DiLello, N.A. (J.L. Hoyt)	**Fabrication and Simulation of CMOS-Compatible Photodiodes**
Dunlop, C. (D.J. Perreault)	**Modeling Magnetic Core Loss for Sinusoidal Waveforms**
Godoy, P. (J.L. Dawson)	**Nested-Chopper Stabilization for Analog Multipliers and RF Mixers**
Gomez, L. (J.L. Hoyt)	**Electron Transport in Ultrathin-body Fully Depleted n-MOSFETs Fabricated on Strained Silicon Directly on Insulator with Body Thickness Rnaging from 2 to 25 nm**
Hoegen, M. (German Technical University of Braunschweig) (B. Wardle)	**Modeling and Experimental Verification of MEMS and micro Energy Harvesters**
Hu, J. (D.J. Perreault)	**Design of a Low-Voltage, Low-Power dc-dc HF Converter**
Hu, X. (K.K. Berggren)	**Couplinig Light to Superconductive Photon Counters**
Joh, J. (J.A. del Alamo)	**Degradation Mechanisms of GaN High Electron Mobility Transistors**
Kalanithi, J.J. (V.M. Bove, Jr.)	**Connectibles: Tangible Social Networking**
Khanna, T. (J.L. Dawson)	**System-Level Optimization for Large, Mixed-Signal Circuits in Aggressively Scaled CMOS**
Lee, S. (H.-S. Lee)	**Zero-Crossing Based Switched-Capacitor Filters**
Leitermann, O. (D.J. Perreault)	**Radio Frequency dc-dc Converters: Device Characterization, Topology Evaluation, and Design**
Leu, J.C. (K.K. Berggren)	**Templated Self-Assembly of Sub-10nm Quantum Dots**
Megalini, L. (Politecnico di Torino, Italy) (B. Wardle)	**Synthesis, Modeling, and Testing of Aligned CNTs for Advanced Composite Structures**
Mercier, P.P. (A.P. Chandrakasan)	**An All-Digital Transmitter for Pulsed Ultra-Wideband Communication**

8 Theses Awarded, 2007-2008

Master of Science *continued*

Mui, A. (J.L. Dawson)	**A 20 dBm 5-14 GHz Power Amplifier with Integrated Planar Transformers in SiGe**
Orcutt, J. (R.J. Ram)	**Flaw-Limited Transport in Germanium-on-Silicon Photodiodes**
Pan, T. (A.P. Chandrakasan)	**Carbon Nanotube Field Effect Transistors for Power Application**
Pulitzer, S. (D.S. Boning)	**Transitioning Technology from R&D to Production**
Reticker-Flynn, N.E. (S.-G. Kim)	**Nanoparticle filled polymeric switch for nanoscale fluidic control**
Sagneri, A. (D.J. Perreault)	**Design of a Very High Frequency dc-dc Boost Converter**
Sinangil, M.E. (A.P. Chandrakasan)	**Ultra-Dynamic Voltage Scalable (U-DVS) SRAM Design Considerations**
Taussig, A.R. (C.A. Ross)	**Growth and characterization of bismuth perovskite thin films for integrated magneto-optical isolator applications**
Traina, Z. (S.-G. Kim)	**Thin-film Piezoelectric Artificial Sarcomere for Muscle-like Large Strain Actuation**
Zhao, X. (T.A. Palacios)	**GaN HEMTs for Millimeter Wave Applications**

Master of Engineering (MEng)

Abdu, H. (V. Bulovic)	**Molecular and Quantum Dot Floating Gate Non-Volatile Memorie**
Blitvic, N. (V. Stojanovic)	**Channel Coding for High-Speed Links**
Clough, A. (V. Stojanovic)	**Increasing Adder Efficiency by Exploiting Input Statistics**
Cooper, R. (J.L. Dawson)	**Hardware and Software for Hand-held Electrical Impedance Myography Measurement Prototype System**
Farahanchi, A. (D.S. Boning)	**Characterization and Modeling of Pattern Dependencies and Time Evolution in Plasma Etching**
Feng, M.Y. (C.G. Sodini)	**Frequency Translation Method for Low Frequency Variable Gain Amplification and Filtering**
Friend, D. (V. Bulovic)	**Theory and Fabrication of Evanescently-Coupled Photoluminescent Devices**
Fu, J. (J. Han)	**Microfabricated Nanofilter Array Based Devices for Advanced Biomolecule Separation**
Ha, M. (J.L. Dawson)	**A Low Power, High Bandwidth LDO Voltage Regulator with no External Capacitor**
Palakodety, R. (C.G. Sodini)	**Investigating Packaging Effects on Bandgap References**
Perez, C.E. (C.G. Sodini)	**Variation-Aware Placement Tools for Field Programmable Gate Array Devices**
Puchala, K. (J. Voldman)	**Selective Micro-organism concentration using a dielectrophoresis-based microfabricated device**

Master of Engineering *continued*

Qazi, M. (A.P. Chandrakasan)	**A 4kb Memory Array for MRAM Development**
Sampattavanich, S. (J. Voldman)	**System to study Colony-Colony Interactions in Embryonic Stem Cells**
Sanchez, W. (J.L. Dawson)	**System-level Optimization for Discrete-Component Syste**
Scharfstein, M. (J.L. Dawson)	**An Impedance Measurement Head for a Clinical EIM System**
Shirasaki, Y. (V. Bulovic)	**Efficient Förster Energy Transfer From Phosphorescent Organic Molecules to J-aggregate Thin Fi**
Sredojevic, R. (V. Stojanovic)	**Bridging the Gap: An Optimization-based Framework for Fast, Simultaneous Circuit and System Design Space Exploration**
Tang, H. (V. Bulovic)	**Near Room Temperature Lithographically Processed Metal-Oxide Transistors**
Vitavasiri, S. (A.P. Chandrakasan)	**A Non-Coherent Ultra-Wideband Receiver: Algorithms and Digital Implementation**
Wang, Y.C. (J. Han)	**Electrokinetic Trapping of Biomolecules: Novel Nanofluidic Devices for Proteomic Applications**
Wu, Y. (C.G. Sodini)	**Null Power Reallocation for Data Rate Improvement in a Wireless Multicarrier System**

Doctor of Philosophy (PhD)

Amataya, R. R.J. Ram	**Optimization of Tunable Silicon Compatible Microring Filters**
Åberg, I. (J.L. Hoyt)	**Transport in Thin-Body MOSFETs Fabricated in Strained Si and Strained Si/SiGe Heterostructures on Insulator**
Albrecht, J. (K.F. Jensen)	**Micro Free-Flow Isoelectric Focusing**
Anant, V. (K.K. Berggren)	**Engineering the optical properties of subwavelength devices and materials**
Arora, W.J. (H.I. Smith, G. Barbastathis)	**Nanostructured Origami™: Stress-Engineering of Nanopatterned Membranes to Produce Three-Dimensional Structures**
Blackwell, B. (K.F. Jensen)	**Design, Fabrication, and Characterization of a Micro Fuel Processor**
Brooks, L. (H.-S. Lee)	**Circuits and Algorithms for Scaled CMOS Technologies Applied to Pipelined ADCs**
Chang, C.-H. (M.L. Schattenburg)	**Multilevel Interference Lithography–Fabricating Sub-wavelength Periodic Nanostructures**
Chen, J. (V. Bulovic)	**Novel Patterning Techniques for Manufacturing Organic and Nanostructured Electronics**
Choi, Z.S. (C.V. Thompson)	**Reliability of Copper Interconnects in Integrated Circuits**
Edalat, F. (C.G. Sodini)	**Real-time Sub-carrier Adaptive Modulation and Coding in Wideband Orthogonal Frequency Division Multiplexing Wireless Systems**

8 Theses Awarded, 2007-2008

Doctor of Philosophy (PhD) *continued*

Garcia, E.J. (Univ. of Zaragoza, Spain) (B. Wardle)	**Characterization of Composites with Aligned Carbon Nanotubes as Reinforcement**
Ginsburg, B.P. (A.P. Chandrakasan)	**Energy-Efficient Analog-to-Digital Conversion for Ultra-Wideband Radio**
Hart, A.J (A.H. Slocum)	**Chemical, Mechanical, and Thermal Control of Substrate-Bound Carbon Nanotube Growth**
Helal, B.M. (M.H. Perrott)	**Techniques for Low Jitter Clock Multiplication**
Jovanovic, N.Z. (L.A. Kolodziejski, J.G. Balakrishnan)	**Microstructured Tungsten Thermophotovoltaic Selective Emmiters**
Kern, A.M. (A.P. Chandrakasan)	**CMOS Circuits for VCSEL-Based Optical IO**
Khakifirooz, A. (D.A. Antoniadis)	**Transport Enhancement Techniques for Nanoscale MOSFETs**
Kim, S. (S.-G. Kim)	**CNT tip-enhanced Raman Spectroscopy for Protein Identification**
Kumar, S. (Q. Hu)	**Development of Terahertz Quantum-Cascade Lasers**
Lee, F.S. (A.P. Chandrakasan)	**Energy Efficient Ultra-Wideband Radio Transceiver Architectures and Receiver Circuits**
Limketkai, B.N (M.A. Baldo)	**Charge injection and transport in amorphous organic semiconductors**
Ma, H. (A.H. Slocum)	**Electrochemical Impedance Spectroscopy using adjustable nanometer-gap electrodes**
Mapel, J.K. (M.A. Baldo)	**High efficiency organic solar cells**
Ni Chleirigh, C. (J.L. Hoyt)	**Strained SiGe-channel p-MOSFETs: Impact of Heterostructure Design and Process Technology/**
O'Halloran, M.G. (R. Sarpeshkar)	**A Wide-Dynamic-Range Time-Based CMOS Imager**
Perkins, J. (C.G. Fonstad, Jr.)	**Low Threshold Vertical Cavity Surface Emitting Lasers Integrated onto Si-CMOS ICs Using a Novel Hybrid Assembly Technique**
Popovic, M. (E.P. Ippen, F.X. Kaertner)	**Theory and Design of High-Index Contrast Microphotonic Circuits**
Rosenthal, A. (J. Voldman)	**Cell Patterning Technology for Controlling the Stem Cell Microenvironment**
Rumpler, J.J. (C.G. Fonstad, Jr.)	**Micro-Cleaved Ridge Lasers for Optoelectronic Intergration on Silicon**
Segal, M. (M.A. Baldo)	**Spin engineering in organic light emitting devices**
Seneviratne, D. (H.L. Tuller)	**Materials and Devices for Optical Switching and Modulation of Photonic Integrated Circuits**

Doctor of Philosophy (PhD) *continued*

Son, S. (J. Kong, M.S. Dresselhaus)	**Raman Spectroscopy of Single-walled Carbon Nanotubes**
Straayer, M.A. (M.H. Perrott)	**Noise Shaping Techniques for Analog and Time to Digital Converters Using Voltage Controlled Oscillators**
Tischler, J. (V. Bulovic)	**Solid State Cavity QED: Practical Applications of the Strong Coupling Limit**
Villanueva, A. (J.A. del Alamo)	**Electrical Degradation Mechanisms of RF Power GaAs PHEMTs**
Waldron, N.S. (J.A. del Alamo)	**Self-Aligned InGaAs HEMT for Logic Applications**
Weber, A. (A.H. Slocum, J.H. Lang)	**MEMS Relays for Make-Break Power Switching Applications: {111} Si Etched Electrical Contacts**
Wei, F.L. (C.V. Thompson)	**Effects of Mechanical Properties on the Reliability of Cu/low-k Metallization Systems**
Wentzloff, D.D. (A.P. Chandrakasan)	**Pulse-Based Ultra-Wideband Transmitters for Digital Communication**
Wu, T.M. (F.R. Stellacci)	**Carbon Nanotube Processing and Chemistry for Electronic Interconnect Applications**
Yen, B. (J.H. Lang, Z. Spakovsky)	**A Fully-Integrated Multi-Watt Permanent-Magnet Synchronous Generator**

9 VLSI Memo Series

MTL maintains a comprehensive Memo Series covering the activities of MTL and related microsystems research at MIT. A chronological list of memos issued from 2007 appears below Copies of MTL Memos are available online exclusively to members of the Microsystems Industrial Group (MIG) at MTL. MIG members are invited to sign up for an account that will grant them access to these materials in a password-protected directory. Visit our website at ***http://mtlweb.mit.ed***u for more information and current memos.

2007	07-2015	L.Y. Chen	**Double-gated Isolated Vertically Aligned Carbon Nanofiber Field Emission and Field Ionization Arrays**
	07-2016	X. Xie	**Physical Understanding and Modeling of Chemical Mechanical Planarization in Dielectric Materials**
	07-2017	V. Anant	**Engineering the optical properties of subwavelength devices and materials**
	07-2018	B. Adeoti	**Field Ionization from Carbon NanoFibers**
	07-2019	F. Edalat	**Real-time Sub-carrier Adaptive Modulation and Coding in Wideband Orthogonal Frequency Division Multiplexing Wireless Systems**
2008	08-2020	R.E. Barreto	**Fabrication of Optical-Mode Converters for Efficient Fiber-to-Silicon-Waveguide Couplers**
	08-2021	C.R Forest, A.M. Rosenbaum, G.M. Church	**DNA Sequencing by Ligation on Surface-Bound Beads in a Microchannel Environment**
	08-2022	H. Miller, J. Collins	**High Resolution DRIE Resist for High Density Through Silicon Vias**
	08-2023	J.M. Perkins	**Low Threshold Vertical Cavity Surface Emitting Lasers Integrated onto Si-CMOS ICs Using Novel Hybrid Assembly Techniques**
	08-2024	M.G. O'Halloran	**A Wide-Dynamic-Range Time-Based CMOS Imager**
	08-2025	A. Khakifirooz	**Transport Enhancement Techniques for Nanoscale MOSFETs**
	08-2026	S. Jongthammanurak	**Germanium-rich Silicon-Germanium Materials for Field-Effect Modulator Applications**
	08-2027	R. Amatya	**Optimization of Tunable Silicon Compatible Microring Filters**
	08-2028	Y. Wu	**Null Power Reallocation for Data Rate Improvement in a Wireless Multicarrier System**
2008 *cont'd*	08-2029	H.S. Tsai	**Absorbance Modulation Optical Lithography**
	08-2030	N.A. DiLello	**Fabrication and Simulation of CMOS-compatible Photodiodes**
	08-2031	L. Zeng	**High Efficiency Thin Film Silicon Solar Cells with Novel Light Trapping: Principle, Design and Processing**
	08-2032	R. Sredojević	**Bridging the gap: An Optimization-based Framework for Fast, Simultaneous Circuit & System Design Space Exploration**
	08-2033	M. Straayer	**Noise Shaping Techniques for Analog and Time to Digital Converters Using Voltage Controlled Oscillators**
	08-2034	N. Jovanović	**Microstructured Tungsten Thermophotovoltaic Selective Emitters**
	08-2035	H. Zhou	**Micromechanical Actuators for Insect Flight Mechanics**
	08-2036	R.C. Cooper	**Hardware and Software for Hand-held Electrical Impedance Myography Measurement Prototype System**
	08-2037	W. Arora	**Nanostructured Origami™: Stress-Engineering of Nanopatterned Membranes to Produce Three-Dimensional Structures**
	08-2038	H. Ma	**Electrochemical Impedance Spectroscopy using Adjustable Nanometer-Gap Electrodes**
	08-2039	Y.J. Chu	**A High Performance Zero-Crossing Based Pipelined Analog-to-Digital Converters**
	08-2040	F. Hurley	**Advanced Nanofabrication of Thermal Emission Devices**
	08-2041	Y. Gu	**Femtosecond Laser Fabrication of Directional Couplers and Mach-Zehnder Interferometers**
	08-2042	B.M. Taff	**Microsystems Platforms for Array-based Single-cell Biological Assays**

10 MTL Seminar Series

MTL hosts a series of talks each semester known as the MTL Seminar Series. Speakers for the series are selected on the basis of their knowledge and competence in the areas of microelectronics research, manufacturing, or policy. The series is held on the MIT Campus during the academic year on Tuesdays at 4:00 pm. The seminar series is open to the public. A listing of recent seminars is also provided at ***http://mtlweb.mit.edu***. Streaming videos of the series are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group at MTL. For more information regarding the MTL Seminar Series, send e-mail to ***valeried@mit.edu***.

Fall 2007	September 18	Michael Geis, MIT Lincoln Laboratory **Responsivity and Transient Response of 1.5-µm Infrared Si Photodiodes Fabricated in a CMOS Line**
	September 25	Ted Vucurevich, Cadence Design Systems **Engineering Challenges in the Late-CMOSEra**
	October 2	Mike Hutton, Altera Corporation **FPGA Architecture**
	October 16	Jesus del Alamo, MTL **III-V CMOS: A 'Beyond-the-Roadmap' Semiconductor Logic Technology?**
	October 23	Kerry Bernstein, IBM **Technology Circuit Co-Design for High Performance Logic**
	October 30	Raj Amirtharajah, University of California-Davis **Micropower Integrated Circuits for Energy Harvesting Wireless Sensors**
	November 6	Ian Young, Intel Corporation **3-D Design Opportunities and Challenges for Microprocessors**
	November 27	Robert Langer, MIT **Advances in Drug Delivery and Tissue Engineering**
	December 4	Michael Perrott, MTL **Making Better Use of Time in Mixed-Signal Circuits**
	December 11	Doctoral Dissertation Seminar: Hong Ma, Department of Mechanical Engineering **Electrochemical Impedance Spectroscopy using Adjustable Nanometer-Gap Electrodes**
Spring 2008	March 4	Bob Metcalfe, Polaris Ventures **The Enernet**
	March 11	Emilio Bizzi, MIT **Combining Molecules for Movement**
	March 18	Larry Hornbeck, Texas Instruments **Digital Light Processors: The Synergism of Combining Digital Optical MEMS, CMOS, and Algorithms**
	April 1	Donhee Ham, Harvard University **The Making of the Smallest NMR System for Human Healthcare - Silicon Trigger & Monitor for Nuclear Spins**
	April 8	Ali Hajimiri, Caltech **Holistic Design in mm-Wave Silicon ICs**
	April 15	Carl Hansen, University of British Columbia **Microfluidic Technology Development for Single Cell Analysis**
	April 29	Kelin Kuhn, Intel Corporation **4 5nm High-k + Metal Gate Logic Technology**
	May 13	Doctoral Dissertation Seminar: Bernard Yen, Department of Electrical Engineering and Computer Science **µTurbogenerator: A Case Study on Resolving Cross-Domain Incompatibilities**

11 Abbreviations

AFOSR . . . . . Air Force Office of Scientific Research
AFRL . . . . . Air Force Research Laboratory
ARL . . . . . Army Research Lab
ARO . . . . . Army Research Office
DARPA . . . . . Defense Advanced Research Projects Agency
DOE . . . . . Department of Energy
DTRA . . . . . Defense Threat Reduction Agency
IARPA . . . . . Intelligence Advanced Research Projects Activity
MDA . . . . . Missile Defense Agency
NASA . . . . . National Aeronautics and Space Adminsitration
NDSEG . . . . . National Defense Science and Engineering Graduate fellowship
NIH . . . . . National Institutes of Health
NIH NIBIB . . . . . National Institute of Biomedical Imaging and BioEngineering
NOAA . . . . . National Oceanic and Atmospheric Administration
NRI . . . . . National Research Initiative
NSF . . . . . National Science Foundation
NSF NECST . . . . . Nano-Engineered Composite aerospace STructures Consortium
NSF NIRT . . . . . NSF Nanoscale Interdisciplinary Research Team
NSF PECASE . . . . . NSF Career Award
ONR . . . . . Office of Naval Research
CICS . . . . . Center for Integrated Circuits and Systems, MIT
CIMIT . . . . . Center for Integration of Medicine and Innovative Technology, MIT
CMSE . . . . . Center for Materials Science and Engineering, MIT
CSBi . . . . . Center for Systems Biology, MIT
EECS . . . . . Department of Electrical Engineering and Computer Science, MIT
ISN . . . . . Institute for Soldier Nanotechnologies
ITRC . . . . . Intelligent Transporation Research Center
KIST . . . . . Korea Institute of Science and Technology
MIT . . . . . Massachusetts Institute of Technology
MIT CEHS . . . . . MIT Center for Environmental Health Sciences
MITEI . . . . . MIT Energy Initiative
RLE . . . . . Research Labaoratory of Electronics, MIT
SMA . . . . . Singapore-MIT Alliance
IMC-KIST . . . . . Intelligent Microsystems Center, Korea Institute of Science and Technology
KAUST . . . . . King Abdullah University of Science and Technology
KIST IMC . . . . . Intelligent Microsystems Center, Korea Institute of Science and Technology
KIMM . . . . . Korea Institute of Metallurgy and Manufacturing
NSERC . . . . . Natural Sciences and Engineering Research Council of Canada
SNSF . . . . . Swiss National Science Foundation
SRC . . . . . Semiconductor Research Corporation
SRC/FCRP C2S2 . . . . . Semiconductor Research Corporation/Focus Center Research Program,Center for Circuits and Systems Solutions
SRC/FCRP IFC . . . . . Semiconductor Research Corporation/Focus Center Research Program. Interconnect Focus Center
SRC/FCRP MSD . . . . . Semiconductor Research Corporation/Focus Center Research Program Materials, Structures and Devices
AMD . . . . . Advanced Micro Devices
TSMC . . . . . Taiwan Semiconductor Manufacuring Corp.

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