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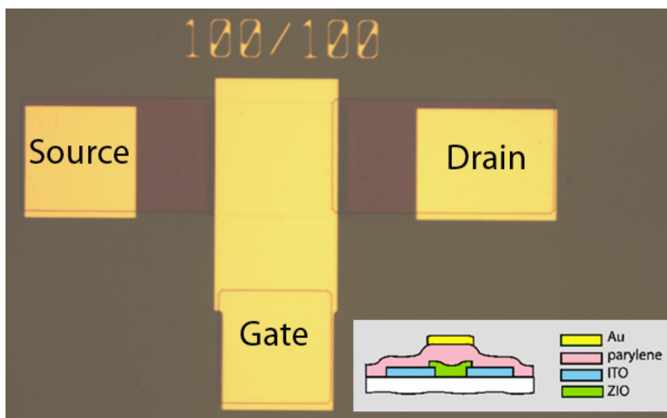
Near-room-temperature Processed Metal Oxide Field Effect Transistors for Large-area Electronics

A. Wang, K. Ryu, J.M. Perkins, I. Nausieda, B. Yaglioglu, C.G. Sodini, V. Bulović, A.I. Akinwande
Sponsorship: Hewlett-Packard

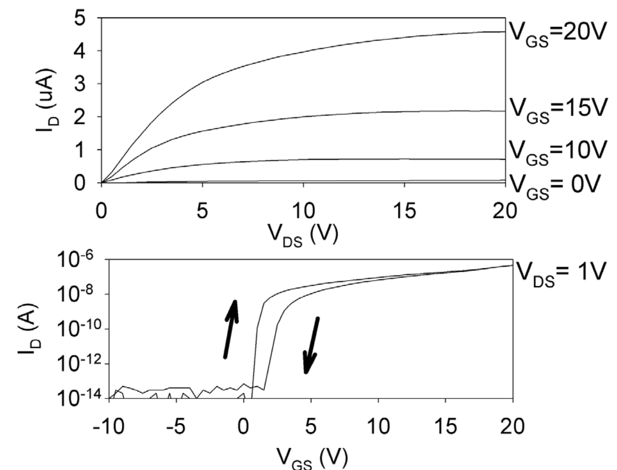
Recently, sputtered metal-oxide-based field effect transistors (FETs) have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1-2]. Furthermore, the optically transparent semiconducting oxide films can be deposited in a near-room-temperature process, making the materials compatible with future generations of large-area electronics technologies that require use of flexible substrates. [3]. It is possible to process FETs by shadow-mask patterning, but this method limits the range of feature sizes, accuracy of pattern alignment, and scalability of the process to large substrates. Consequently, our project aims to develop a low-temperature, lithographic process for metal oxide-based FETs, similar to one developed for organic FETs [4], that can be integrated into large-area electronic circuits.

Using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts, top-gate, lithographically processed FETs have been fabricated on glass substrates using $ZnO{:}In_2O_3$ channel layers. Figure 1 shows a micrograph of a completed FET, with current-voltage characteristics shown in Figure 2.

A reproducible FET process requires consistent control of material properties of the metal oxide semiconductor film. We examine the effect of varying deposition conditions (e.g., target composition, O_2 partial pressure, film thickness) and post-deposition treatment on DC- and RF-sputtered amorphous oxide thin films in the In_2O_3-ZnO system. The electrical properties of thin films are determined through resistivity and Hall measurements. These measurements are used as a guide to determine processing conditions for the fabrication of oxide-based field effect transistors and circuits.



▲ Figure 1: Top-view photomicrograph of lithographically patterned field effect transistor (W/L = 100µm/100µm). A schematic cross-section is also shown (inset).



▲ Figure 2: Current-voltage output characteristics (top) and transfer characteristics (bottom) for lithographically patterned zinc-indium-oxide field effect transistor. The transfer curve shown is a double sweep taken in the triode region (W/L = 100µm/100µm).

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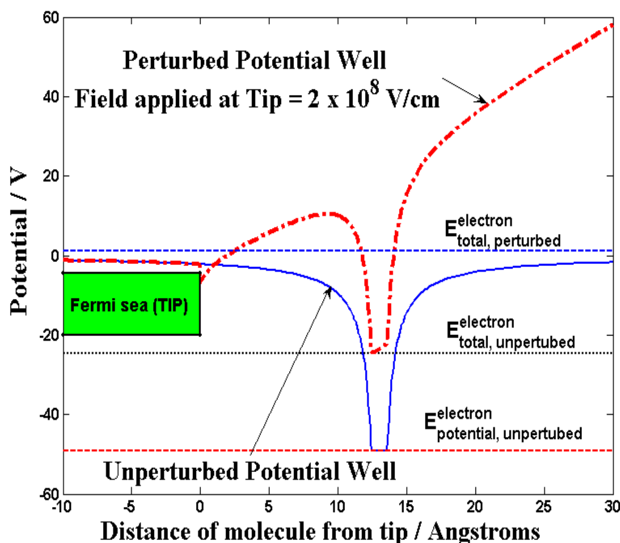
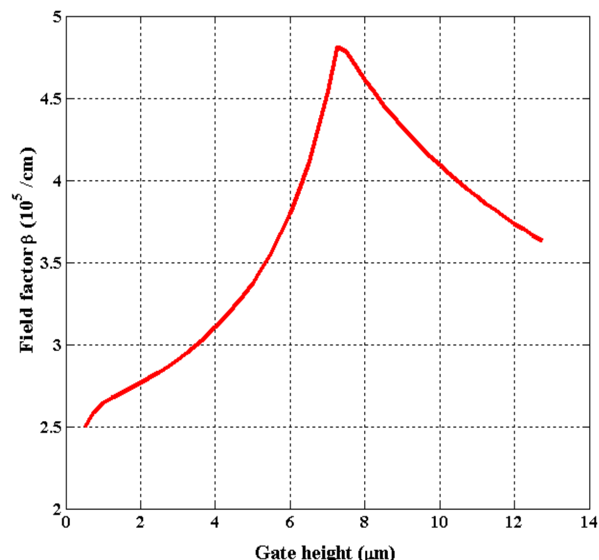
Characterization of Field-ionization from PECVD-grown CNT Tips

B. Adeoti, A.I. Akinwande, L. Velasquez-Garcia, L. Chen
Sponsorship: DARPA

The Micro Gas Analyzer project aims to develop the technology for portable, real-time sensors intended for chemical warfare and civilian air-purity control. For the analyzer, we are developing a field-ionizer array based on gated CNTs. We plan to use arrays of CNTs because their small tip radii and high aspect ratio yield high fields at low voltage. One possible configuration for the device is to bias the CNTs to the highest potential and the collecting anode to the lowest potential. The electrons in the outer shell of the molecules tunnel out due to the ambient high electric fields, which serve to lower the unperturbed potential barrier seen by the electrons (Figure 1). The tunneling effect is a purely quantum-mechanical process whose probability of occurrence is strongly dependent on the applied electric fields [1]. We optimize the electron current by varying structural parameters in our device. The most relevant parameters include the radius of curvature, height, base radius, and base angle of the grown tip; height and thickness of the tip; and the gate aperture. Varying the gate (or oxide) height without updating the height of the CNT yields the derivable result that the electric field is maximized with the tip peaks at about the same height as the gate. When the tip height is varied in sync with the height of the gate (or oxide), it is seen that an independent optimum height exists (Figure 2). The value of this height will depend, among other variables, on the electrostatic properties of the insulating material and the actual dimensions of the rest of the structure. These simulation results are being verified by experiment. Because it is not possible at this time to precisely control any of the CNT structural parameters, we focus on controlling the electrical properties of our device using the structural parameters of the gate.



▲ Figure 1: Representative picture of potential barrier faced by electron in a single molecule when the molecule is close to a tip biased at a high potential.



▲ Figure 2: The FI Field factor β for various heights of gate. Tip height was varied in sync with gate height so that the tip remained within the range of the gate width.
CNT : roc = 5.01nm | Base:- angle=85 , radius=101nm
GATE : Aperture=1.01μm Thickness=0.301μm
V_{CNT} = 10 V, V_{GATE} = 0 V, V_{ANODE} = -150 V

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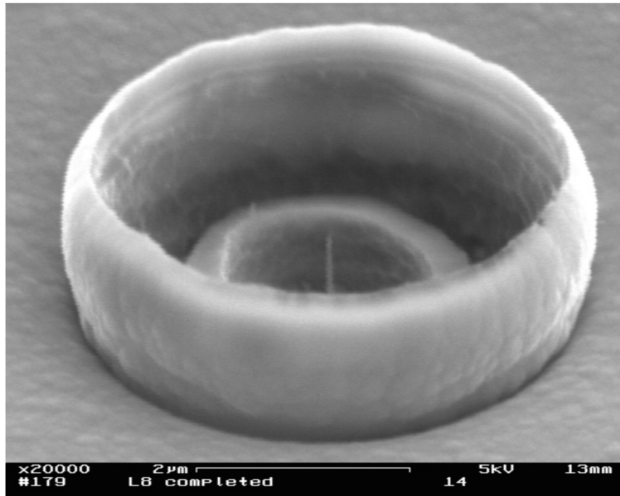
Field Emission from Double-gated, Isolated, Vertically Aligned Carbon Nanofiber Arrays

L.Y. Chen, L.F.V. Garcia, K. Cheung, X.Z Wang, K. Teo, A.I. Akinwande
Sponsorship: DARPA

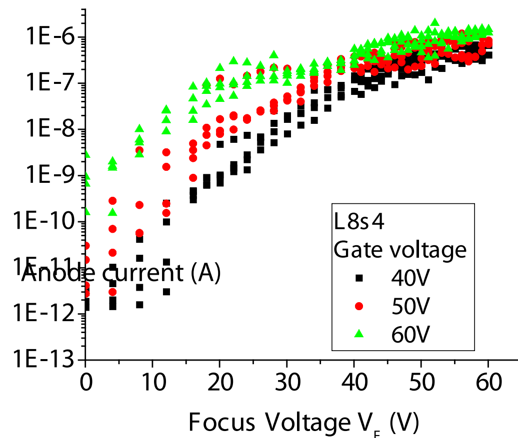
A collimated electron beam is often desired to achieve high performance for practical applications such as field emission display and ebeam lithography. We designed and fabricated a double-gated, isolated, vertically aligned carbon nanofiber field emission array (VACNF FEA) to produce a collimated electron beam. The first gate is used to extract electrons out of the tip and the second gate (focus gate) is biased at a lower voltage than the first gate to focus the emitted electrons.

In this work, we designed a device that maximizes the electric field generated at the tip and minimizes the shield effect from the neighbor while it is capable of handling a large breakdown voltage during the field emission operation. To accomplish this, an isolated VACNF with 4-µm-tall per emission site is needed with each site 10µm apart. The e-beam lithography and lift-off were used to define a 250-nm-diameter and 4-nm-thick Ni catalyst on an n-type Si substrate to guarantee nucleation of Ni dots and subsequent growth of CNFs. The 4-µm-tall VACNF was grown using plasma-enhanced chemical vapor deposition at 725ºC. Once the CNF was synthesized, the extraction gate and the out-of-plane focus gate were fabricated with a novel photoresist planarization technique. This technique offers a very fast, fairly uniform, and well-controlled planarization method of making the self-aligned gate, which can replace the CMP technique that has been reported and used by L. Dvorson *et al.*, M.A. Guillorn *et al.*, and L.-Y. Chen *et al.* [1-3]. This abstract is perhaps the first report of double-gated, self-aligned, field emitter arrays with isolated VACNF.

With this fabrication process, two types of devices were fabricated: (1) with tip in-plane with the extraction gate and (2) CNF with tip 900nm below the extraction gate. They were characterized as three-terminal devices (focus and extraction gate at same bias) and as four-terminal devices (focus and extraction gates at different biases). Figure 1 shows a scanning electron microscope (SEM) picture of a complete device. Using this device, a four-terminal current-voltage (I-V) measurement was performed. As the focus voltage increases, the anode current increases, which is shown in Figure 2.



▲ Figure 1: An SEM picture of a complete double-gated, isolated VACNF FEA device.



▲ Figure 2: The four-terminal I-V characteristic of the double-gated, isolated VACNF array.

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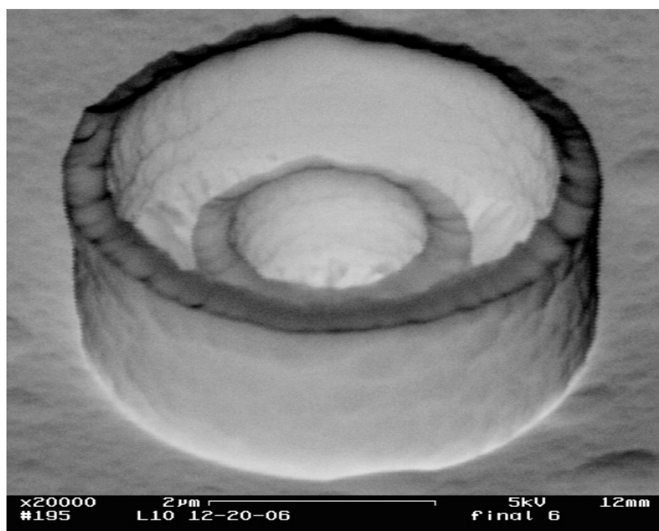
[3] L.-Y. Chen and A.I. Akinwande, “Aperture-focused double-gated silicon field emission arrays,” *IEEE Transactions on Electron Devices*, vol. 54, no. 3, pp. 601-608, 2007.

Electron Impact Ionization and Field Ionization of Gas through Double-gated, Isolated, Vertically Aligned Carbon Nanofiber Arrays

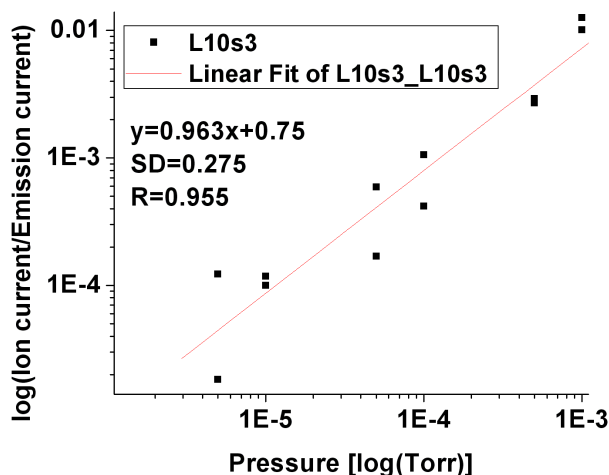
L.Y. Chen, L.F.V. Garcia, K. Cheung, X.Z. Wang, K. Teo, A.I. Akinwande
Sponsorship: DARPA

The goal of this project is to fabricate double-gated carbon nanofiber field emission and field ionization arrays, which can be utilized as an ionizer in a micro gas sensor. This device can help reduce the power consumption and the size of the conventional gas sensor. To achieve this goal, the double-gated isolated VACNF device is designed so that the electric field is maximized at the tip and the shielding effect from the neighbor is minimized while it is capable of handling a large breakdown voltage during the field emission and field ionization operations. Using a photoresist-based fabrication process, two types of devices were fabricated: (1) CNF with tip in-plane with the gate and (2) CNF with tip 0.9µm below the gate. Both devices have the following physical characteristics: (a) The tip height is about 4µm, (b) the gate diameter is 1.7µm, and (c) the focus diameter is 4.2µm. Figure 1 shows a scanning electron microscope (SEM) picture of a complete double-gated isolated vertically aligned carbon nanofiber (VACNF) array with tip 0.9µm below the gate.

Using the device shown in Figure 1, electron impact ionization and field ionization methods of ionizing gas molecules were performed. The electron impact ionization uses a strong electric field to emit electrons followed by collisions between the energetic electrons and neutral gas molecules, resulting in ionization. A linear relationship was obtained between the chamber pressure and the ratio of the ion current and the electron current, as shown in Figure 2. The field ionization is a gentler process in comparison to electron impact ionization. Instead of electrons tunneling from the tip to the vacuum under a high field (as in field emission), in field ionization, electrons tunnel from the gas molecules into the tip, thereby ionizing the gas molecules. It results in molecular ionization and a simpler mass spectrum due to less fragmentation of molecules.



▲ Figure 1: An SEM picture of a complete isolated VACNF array with tip 0.9µm below the gate.



▲ Figure 2: The linear relationship between the pressure and the ratio of the ion current and the emission current in electron impact ionization.

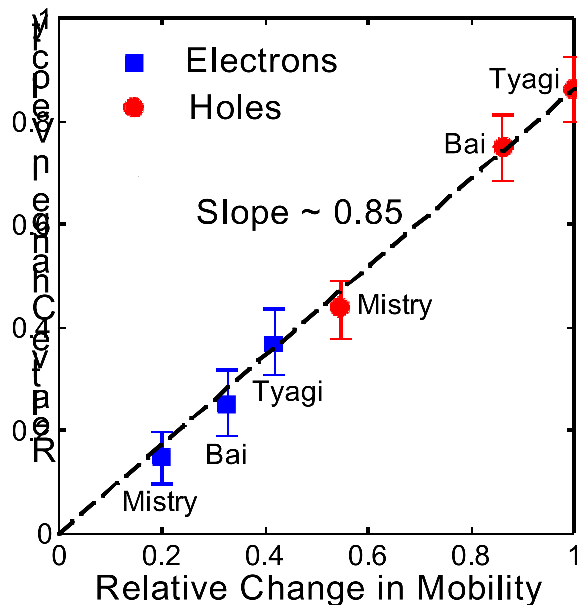
Correlation of Strain-modified Carrier Mobility and Velocity in Modern CMOS

A. Khakifirooz, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

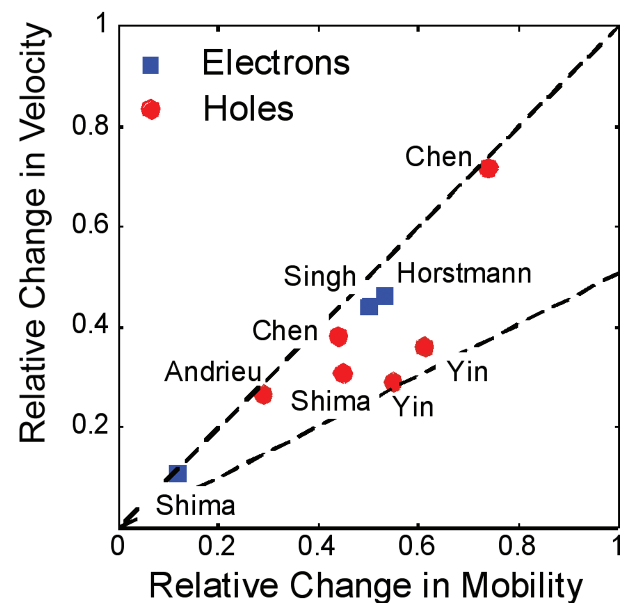
The introduction of strain into the Si channel at the 90-nm node [1] has been critical to increasing carrier mobility and velocity in the channel and maintaining historical CMOS performance trends. Recent experimental data on strain-engineered MOSFETs [2] show strong correlation between the low field mobility and the saturation drain current, both measured in short channel devices. To study this dependence, it is more instructive to explore the correlation between the actual (average) velocity of carriers at the potential barrier at the source side of the channel (virtual source) and the mobility. We have proposed a simple methodology for extracting the virtual source velocity from literature data [3]. Figure 1 shows the correlation between the virtual source velocity and mobility in strain-engineered MOSFETs reported by Intel [2]. As seen, the ratio between the change in the velocity to that of mobility is much higher than the commonly accepted value of 0.5 [4-5]. A similar observation is made on short channel devices reported by other groups as shown in Figure 2. This strong correlation between velocity and mobility can be explained based on the dependence of both mobility and velocity on the effective mass of carrier being modulated by applying mechanical stress. In addition, with less scattering in the channel, carriers gain velocity much faster when traveling across the channel. The steeper velocity profile requires a steeper drop in the inversion charge density and hence a steeper change in the potential. As a result, the distance over which the potential drops by kT/q (the critical length of backscattering) will be smaller. With these two effects combined together, the relative change in the velocity and mobility are related as follows:

$$\partial v_{x0}/v_{x0} = [\alpha+(1-B)(1-\alpha+\beta)]\,\frac{\partial\mu}{\mu}$$

where α models the dependence through the change in the effective mass of carriers, close to 0.5 for uniaxially strained transistors; β models the change in the critical backscattering length, roughly -0.45 according to self-consistent simulations; and B is the ballistic efficiency.



▲ Figure 1: Correlation between the relative change in the low field mobility and relative change in the virtual source velocity in state-of-the-art CMOS devices [2].



▲ Figure 2: Same as Figure 1, for short channel devices reported by other groups. The relative change in the mobility is usually taken from the change in the slope of R_{tot}-L_G curves.

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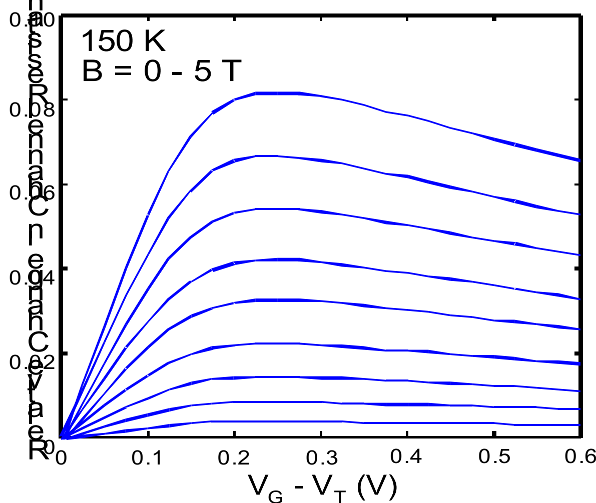
Carrier Mobility Characterization in Germanium MOSFETs

A. Khakifirooz, A. Ritenour, J. Hennessy, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

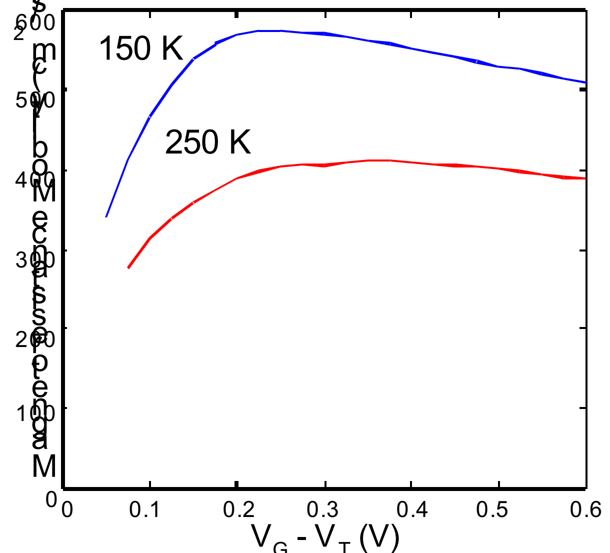
Germanium has attracted much attention in recent years as an alternative channel material for increasing the transistor performance because of its superior electron and hole mobility [1-3]. However, mobility values achieved so far have been considerably lower than what is expected in Ge. This points to the fact that high-k processes adapted for Ge devices are far from having optimum conditions. In addition to higher phonon scattering and surface roughness scattering associated with the presence of high-k dielectrics, due to the presence of a high number surface states (usually more than 10^{12} $cm^{-2}eV^{-1}$), carrier mobility is severely degraded. On one hand, charged surface states act as a source of Coulombic scattering, and on the other hand, their presence contaminates the estimation of inversion charge and hence the mobility calculation. Pulsed I-V and Q-V methods provide a path to D_{it}-free measurement of the mobility [4-5]. Alternatively, Hall and magnetoresistance measurements can be used to extract the intrinsic mobility of the carriers in the channel. Although the mobility probed with these two methods is different from the effective mobility measured by the split-CV method, they provide complementary information to estimate the inversion charge and gain insights into various scattering mechanisms involved. Measuring the device characteristics under relatively high magnetic fields is an integral part of both methods. Figure 1 shows the relative change in the channel resistance in a wide PMOS Ge transistor upon application of a magnetic field. As expected, the data show a quadratic dependence of resistance, R, according to

$$R(B)/R(0) = 1 + \mu_m^2 B^2$$

where μ_m is the magnetoresistance mobility. Figure 2 shows the magnetoresistance mobility in PMOS Ge devices as a function of the gate voltage and at two different temperatures. Combined with Hall measurements, these data provide valuable information about the scattering mechanisms that limit the mobility in Ge transistors.



▲ Figure 1: Relative change in the channel resistance in PMOS Ge transistors upon applying a magnetic field normal to the channel. The channel resistance shows a quadratic dependence on the magnetic field according to $R(B)/R(0) = 1 + \mu_m^2 B^2$, where μ_m is the magnetoresistance mobility.



▲ Figure 2: Magnetoresistance mobility measured in PMOS Ge transistors as a function of the gate voltage. Combined with Hall measurements, these data provide valuable information about the scattering mechanisms that limit the mobility in Ge transistors.

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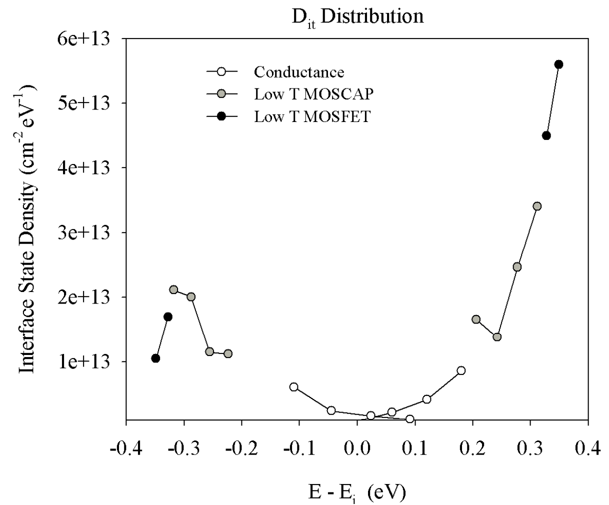
Investigation of Germanium MOSFETs with High-k Dielectric Stacks Based on Nitride Interfacial Layers

A. Ritenour, J. Hennessy, A. Khakifirooz, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

To improve source injection velocity and consequently MOSFET performance, high mobility semiconductors are being explored as possible replacements for silicon. Germanium offers enhanced electron mobility and superior hole mobility at high inversion charge density; however, the formation of a high-quality germanium-dielectric interface remains a serious challenge. High-k dielectrics deposited directly on germanium exhibit poor physical and electrical properties, so an interfacial layer is required. Proposed interlayers include GeON [1], Si [2], and metal nitrides such as AlN [3] and Hf_3N_4 [4].

This work focuses on metal nitride interlayers deposited by atomic layer deposition (ALD). The ALD $WN/Al_2O_3/AlN$ gate stacks were developed for use in Ge MOSFETs. An AlN thickness of approximately 2 nm and post-metal anneal at 450ºC in forming gas produced optimal electrical characteristics. Ge n- and p-MOSFETs were fabricated with this gate stack, and peak electron and hole mobilities of 50 and 150 cm^2/Vs, respectively, were observed. Investigation of these devices revealed an asymmetric distribution of interface states within the bandgap. Figure 1 shows the interface state distribution. Conductance measurements on capacitors and low-temperature measurements on both capacitors and MOSFETs were used to determine the interface state density in different regions of the bandgap. The poor mobility of Ge n-MOSFETs is due to carrier trapping and coulomb scattering resulting from a large density of interface states ($5x10^{13}$ cm^{-2} eV^{-1}) near the conduction band edge.



▲ Figure 1: Distribution of interface states for $WN/Al_2O_3/AlN$ gate stacks on germanium. Interface state density in different regions of the bandgap was determined from conductance measurements on capacitors and low-temperature characterization of both capacitors and MOSFETs.

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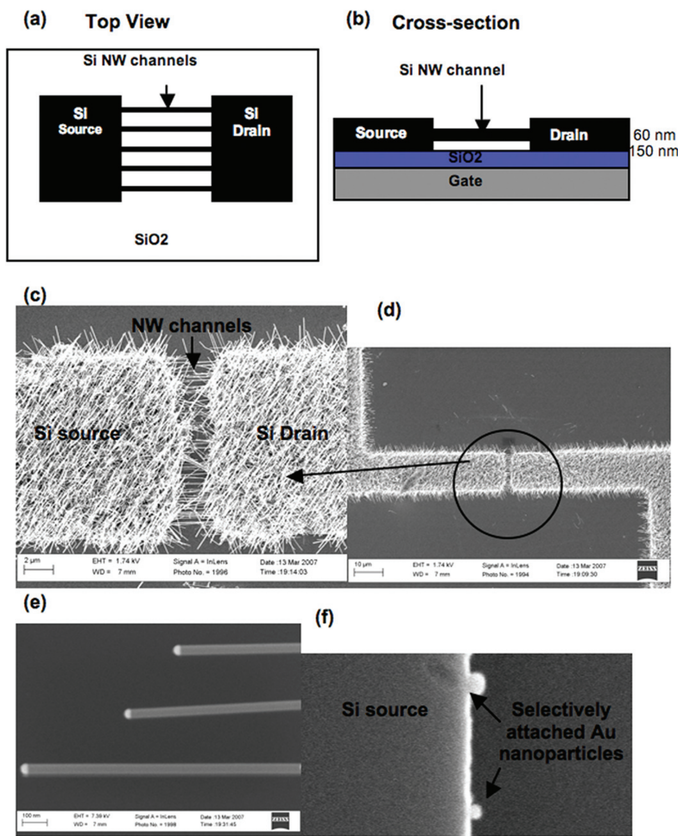
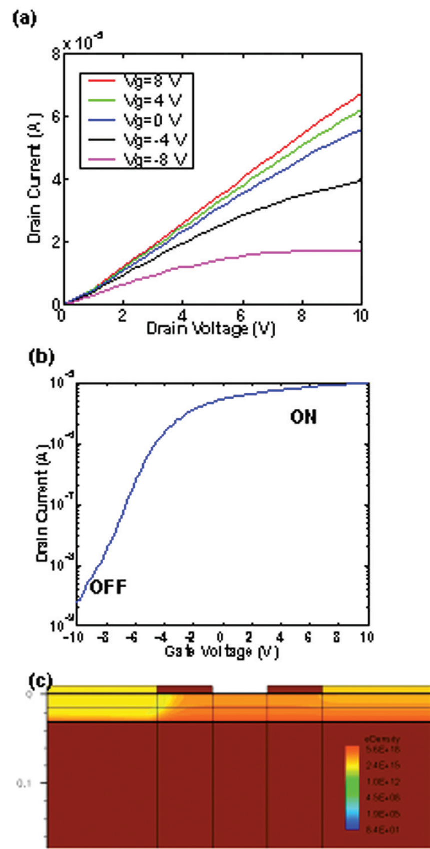
Si Nanowires: Fabrication, FETs, and Modeling

O.M. Nayfeh, D.A. Antoniadis
Sponsorship: Singapore-MIT Alliance

Silicon nanowires are attractive components in 22-nm-node and beyond high-performance technology. In this work, we fabricated silicon nanowire field effect transistors that incorporate single-layers of nanowire channels. The channels were laterally grown via the Vapor-Liquid-Solid (VLS) technique directly in the device structure to "bridge" the gap between adjacent short (~60 nm) Silicon-on-insulator (SOI) entrenched side-walls via a combined bottom-up/top-down method as shown in the schematics and SEM's of Figure 1. The utilization of short SOI sidewalls allowed for the selective attachment of single layers of catalyst particles on the sidewalls and hence the growth of single layers of entrenched channel bridges. Moreover, we were able to modulate the charge density of the wires immediately after growth without post-processing by biasing the planar back-gate. The measured 3 terminal current-voltage data shown in Figure 2 are characteristic of field-effect transistor behavior where the bridging nanowires act as the FET channel material and agree with simulation analysis of the structure.



▲ Figure 1: Top view(a) and cross-section (b) schematic of silicon nanowire FETs. An SEM micrograph of fabricated NWFET(c&d) showing a single layer of laterally grown parallel silicon nanowires bridging the gap between source-drain. An SEM closeup of as-grown nanowires ~30 nm in diameter (e) and an SEM of selectively attached Au catalyst nanoparticles on the short SOI sidewall (f).



▲ Figure 2: Transfer curves (a), Id. vs. Vds varying Vgs for the silicon nanowire FET shown in Figure 1, and (b) the Id. vs. Vgs showing clear transistor behavior, i.e., gate modulation of the current switching the device between on (Vgs=10 V) and off (Vgs=-10 V). Simulated electron density of the device in the on-state, Vgs=10 V, Vds=1V (c) showing the creation of a conduction pathway from source-drain consistent with the measurements of the device.

Scanning Helium Ion Beam Lithography

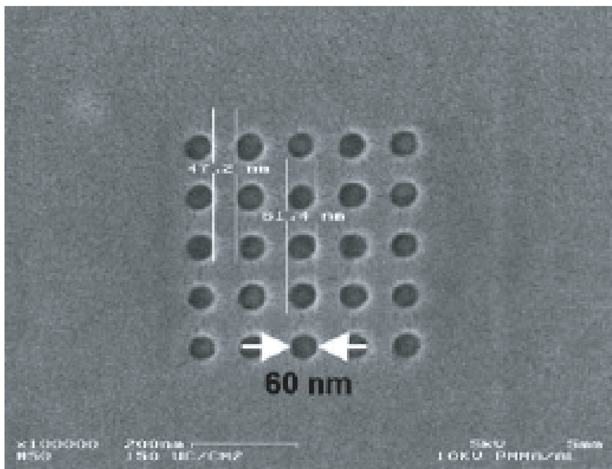
B. Cord, M.K. Mondol, K.K. Berggren, L.A. Stern (Karl Zeiss SMT)

Scanning electron beam lithography (SEBL) has been the leading technology in low-volume, high-resolution nanofabrication for over three decades. Unfortunately inherent limitations of the technology, such as electron beam scattering, have made improvement in SEBL resolution past the 10-nanometer limit problematic. Recent advances in resist contrast enhancement have mitigated this somewhat, but reliable patterning of dense, sub-10-nm features remains nontrivial on even the most high-end SEBL tools.

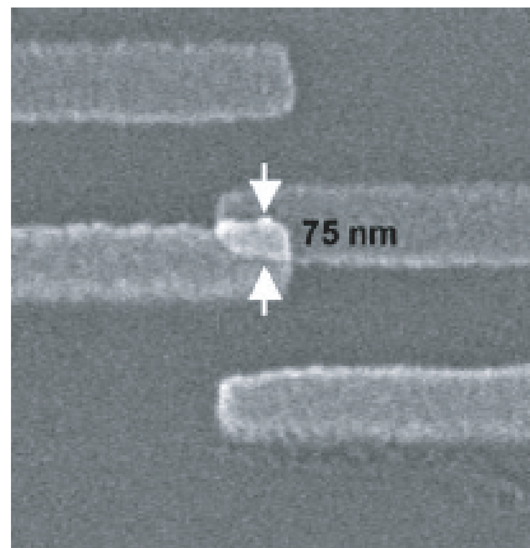
One of the key advantages of patterning using a helium ion, rather than an electron beam, is the substantial reduction in beam scattering as it travels through the resist. Helium ions, with a comparatively higher mass, are affected much less by atomic collisions when traveling through a material and exhibit only minimal scattering in normal resist materials. Figure 1 shows the results of a Monte Carlo simulation of a 50-KeV helium ion beam traveling through a PMMA layer; at a depth of 50 nm (a typical resist thickness for many applications), the point-spread function of the beam is only 2 nm wide, narrower than even 100-KeV electron beams under similar conditions. This reduction in beam scattering should help reduce the proximity effect that makes patterning dense, high-resolution features difficult with SEBL.

Experimentation with helium ion beam lithography has recently been made possible by the development of a scanning helium ion beam microscope by Alis Corporation [1]. Their commercial-grade microscope has achieved imaging resolutions on the order of 1 nm, making it a promising candidate as a lithography tool. Basic experimentation with their lower-resolution "proof-of-concept" system has demonstrated that patterning and successful transfer of features are possible using standard SEBL processes. Figure 2 shows a field of Ti-Au dots patterned with the system using a film of PMMA on silicon and standard metallization and liftoff.

While issues such as vibration, pattern generation, and process control remain to be addressed, further experimentation with helium ion beam lithography may lead to a tool that meets or exceeds the performance of modern SEBL systems.



▲ Figure 1: Simulation of He ion scattering in resist. (a) Result of SRIM-based Monte Carlo simulation of ion-scattering for 50-keV He ions traveling through 100 nm of PMMA into a Si substrate (b) Analysis of the data from (a) showing how the distribution of deposited energy widens as a function of resist depth. After 50 nm of resist (a practical thickness to work with), the beam width is only 2 nm. Note that this model does not take secondary electrons generated by the ion beam into account, as the details of the ion-secondary electron interactions are not yet fully understood.



▲ Figure 2: Scanning electron micrographs of a field of Ti-Au dots at two magnifications, fabricated by exposing 90-nm PMMA on a Si substrate to a single raster-scan of a helium ion beam and performing metal evaporation and liftoff on the resulting pattern. The consistently irregular dot shape in (b) is thought to be the result of vibrations in the system. The large square in (a) is a previously-fabricated fiducial mark.

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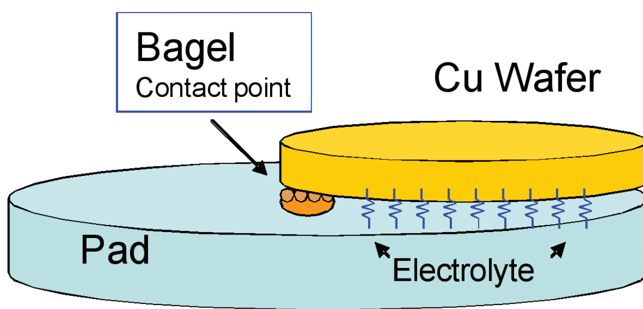
Wafer Level Modeling of Electrochemical-mechanical Polishing (ECMP)

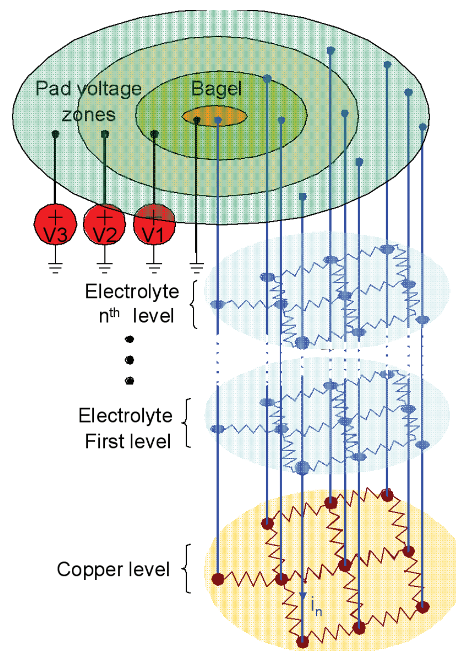
D. Truque, X. Xie, Z. Li, D.S. Boning
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, IBM, Albany Nanotech

In this work, we propose a wafer-level dynamic eCMP model based on time-evolving current density distributions across the wafer. The wafer is discretized, and the potential and current density distributions are calculated based on the applied voltage zones and metal film thicknesses across the wafer. The copper removal rate is proportional to the current density, and thus the copper thickness (and conductance) can be calculated as a function of position on the wafer and polish time. Using a time-stepping simulation, the model is able to capture the wafer level non-uniformity and time-dependence of eCMP removal. The model is also able to capture the time-varying voltage zones used in eCMP, and can be used to find optimal voltage zone control schemes to achieve improved wafer-level uniformity.

The configuration of the eCMP equipment is shown in Figure 1, where a voltage is applied in each of three zones on the platen, and electrical contact is made to the edge of the wafer. The modeling approach is pictured in Figure 2, in which the electrical current distributions on the wafer surface and in the electrolyte are accounted for, giving the removal rate at each location on the wafer.



▲ Figure 1: Schematic of wafer and tool configuration in electrochemical-mechanical polishing (eCMP).



▲ Figure 2: Wafer-level modeling approach for eCMP, accounting for the distribution of current through the wafer surface and electrolyte.

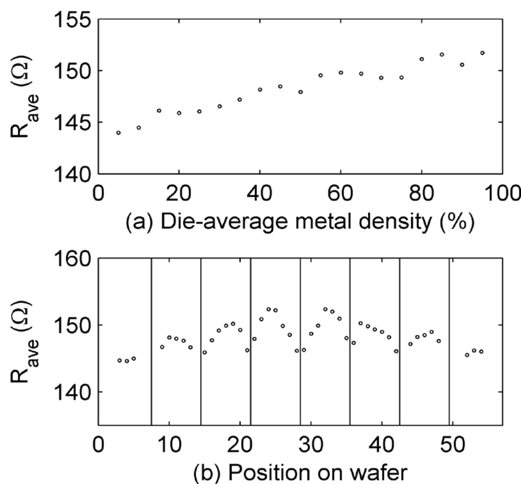
Models for Spatial Non-uniformity in Plasma Etching

A. Farahanchi, H.K. Taylor, D.S. Boning

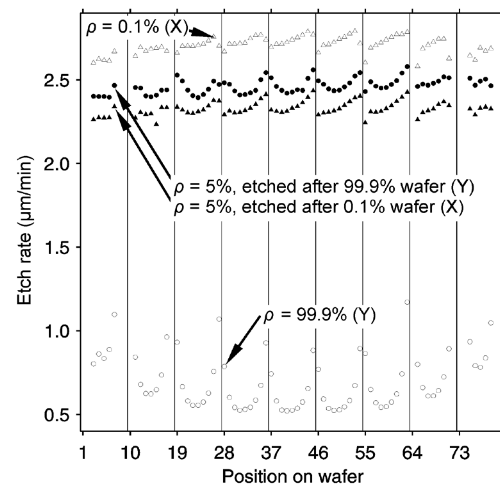
Sponsorship: National Semiconductor, SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

We are studying the plasma etching of aluminum films for IC metallization. Using electrical resistance measurements from a dedicated metal test pattern, we have identified, in a commercially-used etching process, resistance variations of 5% cross-wafer and additionally of about 5% according to the locally averaged metal pattern density (Figure 1). The etching rate also depends appreciably upon the size of the etched feature.

The deep reactive ion etching (DRIE) of silicon for MEMS also experiences spatial non-uniformity, which can be detrimental to its applications. We hope to use our model to predict the uniformity of proposed new operating "recipes." We continue to investigate an observed "memory" effect in DRIE chambers (Figure 2), whereby the average pattern density of one etched wafer influences the rate and uniformity of the subsequent wafer's etching.



▲ Figure 1: Spatial variation of the electrical resistances of aluminum snake patterns etched from a film on a 200 mm-diameter wafer. (a) shows how the average resistance of a snake (R_{ave}) increases by ~5% as the areal density of unetched metal near the feature increases from 5% to 95%. In areas of higher unetched metal density, local competition for reactants is less acute during etching, so that lateral etching of snake features can progress more quickly, increasing the features' resistances. (b) shows a cross-wafer variation of ~5% among the resistances of features with identical local surroundings.



▲ Figure 2: Vertical silicon etch rate as a function of location on each of four etched 150 mm-diameter wafers in a deep reactive ion etch (DRIE) process. A monitor wafer with 5% mask-opening density etched immediately after wafer Y (with 99.9% pattern density) etched consistently faster and less uniformly than a 5%-density monitor wafer etched after wafer X (with 0.1% pattern density). Here and in Figure 1b, the position axis corresponds to locations on a square grid, with each row of locations plotted consecutively and separated by vertical bars on the graph.

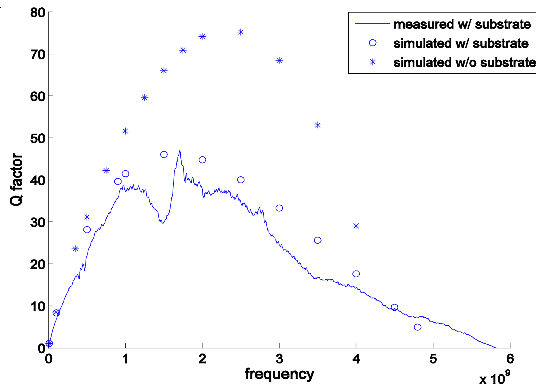
Development of Specialized Basis Functions and Efficient Substrate Integration Techniques for Electromagnetic Analysis of Interconnect and RF Inductors

X. Hu, T.A.E. Moselhy, J. White, L. Daniel
Sponsorship: SRC/FCRP GSRC, NSF

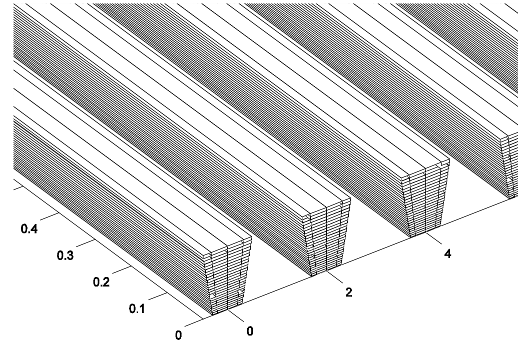
The performance of several mixed-signal and RF-analog platforms depends on substrate effects that need to be represented in the library model with critical field solver accuracy. For instance, substrate-induced currents in RF inductors can severely affect quality and hence RF filter selectivity. We have developed an efficient approach to full-wave impedance extraction that accounts for substrate effects through the use of two-layer media Green's functions in a mixed-potential-integral-equation (MPIE) solver. In particular, we have developed accelerated techniques for both volume and surface integrations in the solver.

In this work, we have also introduced a technique for the numerical generation of high-order basis functions that can parameterize the frequency-variant nature of cross-sectional conductor current distributions. Hence skin and proximity effects can be captured utilizing fewer high-order basis functions in comparison to the prevalently used piecewise-constant basis functions. One important characteristic of these basis functions is that they need to be pre-computed only once per unique conductor cross-sectional geometry, and then stored off-line with a minimal associated cost. In addition, the robustness of these frequency-independent basis functions is enforced using an optimization routine.

We have shown in [2] that the cost of solving a complex interconnect system using our new basis functions can be reduced by a factor of 170 when compared to the use of piecewise-constant basis functions over a wide range of operating frequencies. Furthermore our volume and surface integration routines improve efficiency by an additional factor of 9.8 [1]. Our solver accuracy is validated against measurements taken on fabricated devices.



▲ Figure 1: Measured and simulated Q-factors for a square RF inductor with an area of 15mm x 15mm and surrounded by a ground ring.



▲ Figure 2: Our basis functions avoid the expensive cross-sectional discretization shown in the figure necessary to account for trapezoidal cross-sections or skin and proximity effects.

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[2] X. Hu, T.A.E. Moselhy, J. White, and L. Daniel, "Optimization-based wideband basis functions for efficient interconnect extraction," *Design Automation and Test in Europe (DATE'07)*, April 2007.

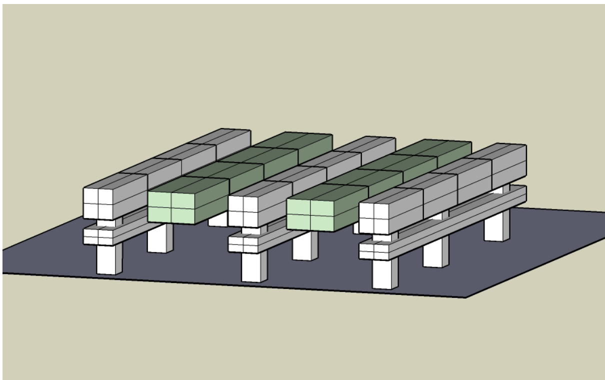
pFFT in FastMaxwell: A Fast Impedance Extraction Solver for 3D Conductor Structures over Substrate

T. Moselhy, X. Hu, L. Daniel
Sponsorship: SRC/FCRP IFC

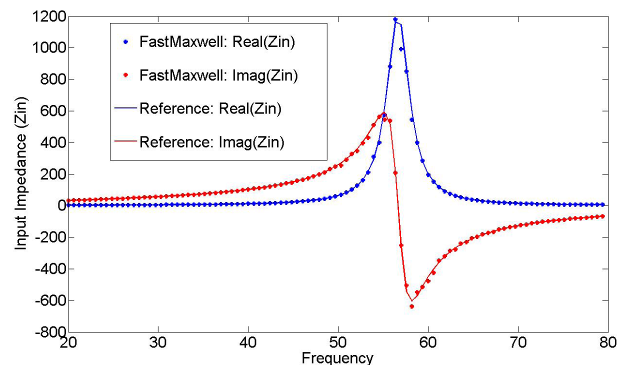
Interconnect-aware timing analysis and mixed-signal simulation rely on tools for extracting accurate low-order models for interconnect electrical behavior. Models should be physics-based to enable efficient modeling of 2D and 3D effects on interconnects with their statistics and variations. As a first step toward our goal, we have been focusing on the development of a very efficient 3D parasitic extractor for the deterministic analysis of a large collection of interconnects. FastMaxwell [1], is a program for wideband electromagnetic extraction of complicated 3D conductor structures over substrate. It is based on the volume mixed potential integral equation (MPIE) formulation, with a 3D full-wave substrate dyadic Green's function kernel. Two dyadic Green's functions are implemented [2]: a traditional Green's function and an alternative Green's function that can lead to computational cost reduction in most practical applications. Most importantly, the alternative Green's function allows the use of dipoles (i.e., filaments) in arbitrary orientations, and it helps providing symmetric positive semidefinite matrices, hence facilitating the passive model order reduction of distributed systems. The pre-corrected Fast Fourier Transform (pFFT) [3] algorithm has been extended and optimized to accelerate the iterative solver within FastMaxwell.

The accuracy and efficiency of FastMaxwell and the implemented acceleration algorithms have been verified against measurements of fabricated devices by a variety of examples, some as large as 100,000 unknowns, using less than 400MB of memory and a few hours of computation time. The pFFT computational complexity of O(N log N) in overall solver time and O(N) in memory usage has been observed from our results, leading to a scalable software for very large collection of interconnects.

FastMaxwell is public domain and can be downloaded at: www.rle.mit.edu/cpg/fastmaxwell.htm.



▲ Figure 1: FastMaxwell discretization of a two-wire transmission line on top of a substrate and shielded by a 3D cage structure. The cage is connected to ground through vertical vias. (Figure is rescaled and edited for clarity.)



▲ Figure 2: Real and imaginary components of the input impedance of a two-wire transmission line. Results obtained by FastMaxwell are within 2% of those obtained by reference simulator IE3D [4].

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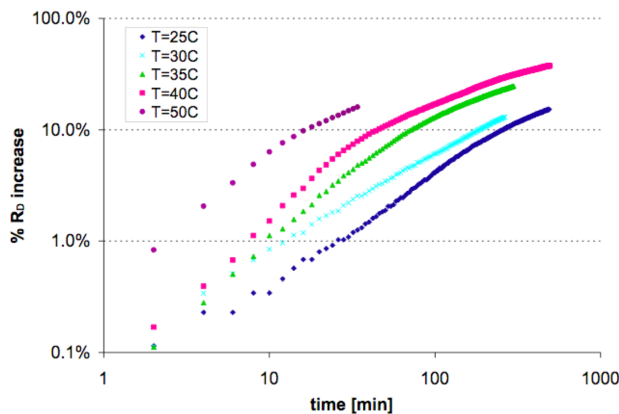
Modeling Drain Degradation of RF Power GaAs Pseudomorphic HEMTs under High Bias Conditions

A.A. Villanueva, J.A. del Alamo
Sponsorship: Mitsubishi Electric

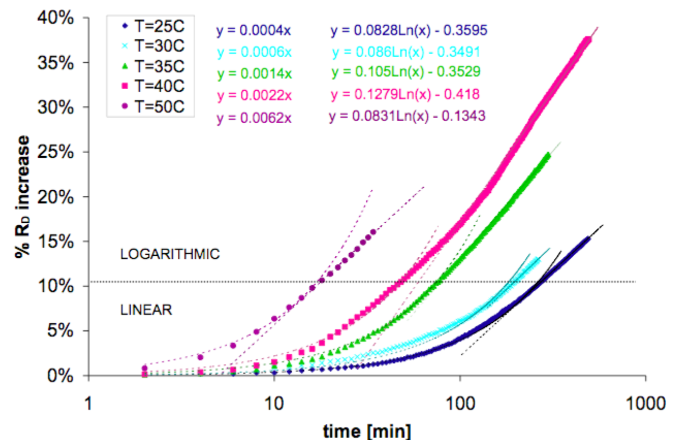
GaAs Pseudomorphic High-electron Mobility Transistors (PHEMTs) are widely used in RF power applications. A major concern with these devices is their gradual degradation under prolonged high-voltage biasing. This effect is mainly observed via an increase of the drain resistance (R_D) and a decrease of the maximum drain current (I_{max}). Previous studies have linked this degradation to various mechanisms, including impact ionization (II) and hot-electron effects, and surface corrosion [1]. However, further investigation is required to determine which of these mechanisms are actually behind the observed degradation. Understanding the time evolution of the degradation can provide some insight into this.

In our study, experimental (non-commercial) GaAs PHEMTs were electrically stressed. A stressing scheme that keeps II constant was employed. Specifically, this scheme consisted of keeping the drain current I_D constant and the intrinsic drain-to-gate voltage V_{DGo} constant (relative to the threshold voltage) [2]. During stressing, the devices were characterized at frequent intervals.

Figure 1 illustrates the time evolution of the increase of R_D in a set of experiments performed at various ambient temperatures. One can clearly see that the ΔR_D is dramatically accelerated with increasing temperature, which alone suggests a corrosion mechanism instead of an II mechanism. Also, there seem to be two "regimes" of degradation. For initial stages (less than ~10% increase in R_D), the degradation is roughly linear in time. In a later stage, the degradation slows down, becoming closer to a logarithmic dependence in time. This phenomenon is better seen in Figure 2, which shows a semi-log plot of the same data with both the linear and log fits superimposed. This behavior thus suggests that ΔR_D is directly related to the growth of an oxide layer on the GaAs surface on the drain side, which is accelerated with temperature and typically follows a time-dependence similar to what we observe. Initially, as a GaAs surface is oxidized, the oxide layer is thin enough so oxide growth at the GaAs/oxide interface is limited by the reaction rate, thus giving a linear dependence in time. However, as the oxide layer thickens, the oxide formation then becomes limited by the transport of the oxidizing agent through the oxide to the GaAs/oxide interface. In GaAs systems this transport process has been observed to have a logarithmic dependence on time.



▲ Figure 1: Log-log plot of percent increase of R_D versus stressing time for series of constant $V_{DGo}+V_T$ and constant I_D experiments performed on standard-parameter PHEMTs in nitrogen environment at T_{amb} =25, 30, 35, 40, and 50°C.



▲ Figure 2: Semi-log plot of percent increase of R_D versus stressing time for series of constant $V_{DGo}+V_T$ and constant I_D experiments performed on standard-parameter PHEMTs in nitrogen environment at T_{amb} =25, 30, 35, 40, and 50°C. Linear and logarithmic fits are shown for each data set.

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Electrical Reliability of GaN High Electron Mobility Transistors

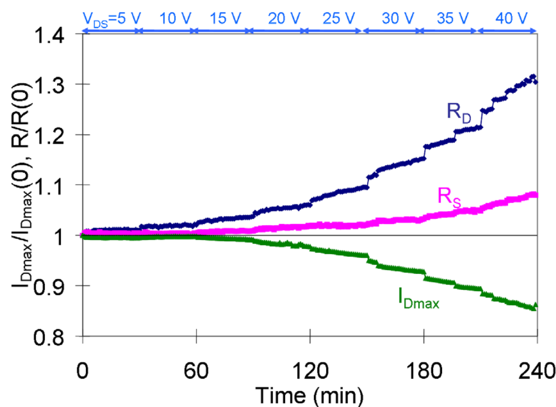
J. Joh, J.A. del Alamo (in coll. with TriQuint Semiconductor, BAE Systems)
Sponsorship: ARL

As a result of their large band gap (~3.4 eV) and high breakdown electric field (>3x10^6 V/cm), GaN-based devices can operate at voltages higher than 100 V. Also, due to the strong piezoelectric effect and spontaneous polarization of both GaN and AlN, a high sheet carrier density (~10^{13} cm^{-2}) can be achieved at the AlGaN/GaN heterointerface without any doping. In addition, high electron mobility (~1500 cm^2/V-s) and high saturation velocity (~2x10^7 cm/s) make GaN-based devices, especially GaN high electron mobility transistors (HEMT), suitable for high power amplification at high frequencies, such as WiMAX or WLAN base stations and radars.

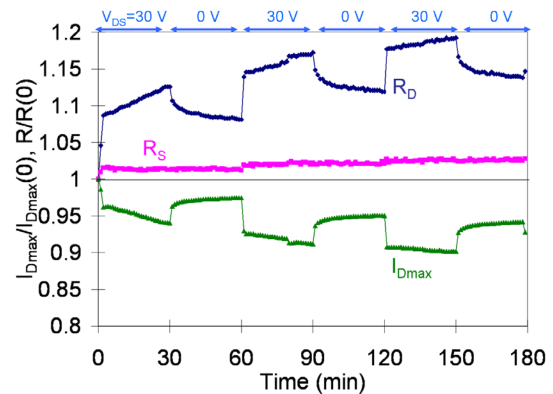
In spite of their extraordinary performance, GaN HEMTs still have limited reliability. In RF power applications, GaN HEMTs must operate at high voltage, where good reliability is hard to obtain. Physical understanding of the fundamental reliability mechanisms of GaN HEMTs is still lacking today. In this research, we carry out systematic reliability experiments on industrial GaN HEMTs provided by our collaborators, TriQuint Semiconductor and BAE Systems. In our study, GaN HEMTs have been electrically stressed at various bias conditions while they are being characterized by a benign characterization suite that we have developed for this study.

In our experiments, we have observed that electrical stress on GaN HEMTs results in an increase in drain resistance R_D and a decrease in maximum drain current I_{Dmax}, as shown in Figure 1. The source resistance R_S shows relatively less degradation. We have found that the electrical stress generates traps. Figure 2 shows a stress-recovery experiment in OFF state. Partial recovery in the recovery phase suggests electron detrapping, and immediate retrapping in the following stress phase suggests permanent trap formation. We have also seen that this degradation is driven mostly by the electric field, with the current being less relevant. We hypothesize that the main mechanism behind device degradation is defect formation through the inverse piezoelectric effect and subsequent electron trapping. Departing from current conventional wisdom, hot electrons are less likely to be the direct cause of electrical degradation in the devices that we have studied. Our studies suggest a number of possibilities to improve the electrical reliability of GaN HEMTs. As our hypothesis suggests that it is important to keep the elastic energy in the AlGaN barrier below a critical value, minimizing the initial elastic energy and peak vertical electric field in AlGaN can improve reliability.

Our research addresses the fundamental degradation physics of GaN HEMTs. This study will help us to understand failure mechanisms in detail and to develop processes and device designs that minimize these deleterious effects.



▲ Figure 1: Change in normalized I_{Dmax}, R_D, and R_S in a step-stress experiment in the OFF state (I_D=25 mA/mm,V_{DS}=5~40 V in 5 V steps, 30 minutes per step).



▲ Figure 2: Change in I_{Dmax}, R_D, and R_S in a stress-recovery experiment in the OFF state (V_{DS}=30 V, I_D=20 mA/mm) for 30 minutes of stress followed by 30 minutes at rest. This cycle is repeated three times.

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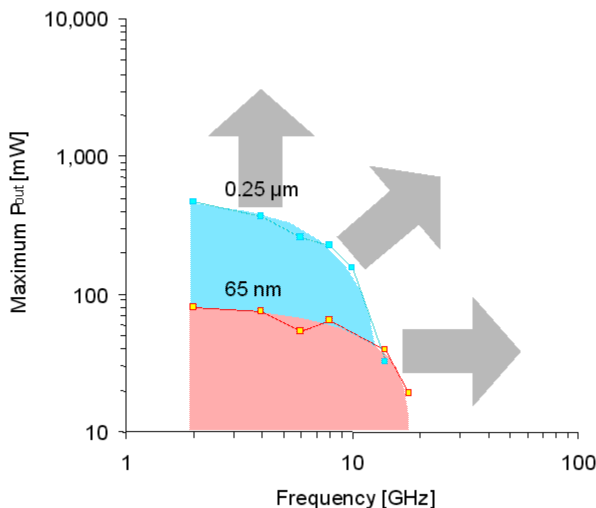
RF Power CMOS for Millimeter-wave Applications

U. Gogineni, J.A. del Alamo (in coll. with D.R. Greenberg, IBM)
Sponsorship: MIT Presidential Fellowship, IBM

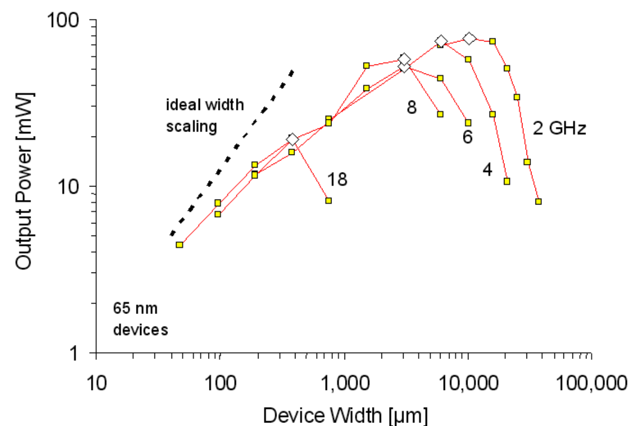
Radio frequency (RF) power amplifiers are core components of almost all wireless systems. Traditionally III-V devices, SiC devices or SiGe heterojunction bipolar transistors have been used in power amplifiers because of their ability to deliver high power and operate at high frequencies. Recently there has been an increased interest in using Si CMOS for designing single-chip integrated systems for operation in the millimeter-wave regime. Specific applications in this regime include wireless LAN and collision avoidance radar.

Previous research in our group at MIT into the RF power performance of 65-nm and 90-nm Si CMOS devices [1-2] has shown that it is not possible for currently available Si CMOS to operate significantly beyond 20 GHz (Figure 1). The effective cut-off frequency for power (frequency at which the output power drops below 10 mW) is around 20 GHz for 0.25-um, 90-nm and 65-nm CMOS. This suggests that further scaling is unlikely to improve the situation despite improvements in f_T and f_{max}. The reason for this saturation in the effective power cut-off frequency is that the optimum device width that delivers the maximum power at any frequency scales down as the frequency goes up (Figure 2). This effect indicates that the bottleneck for power is the device layout, especially the back-end wiring. An optimized device layout would enable us to operate Si CMOS in the millimeter wave regime.

In this research, we are investigating options for device optimization with the goal of pushing the power operation of Si CMOS into the millimeter-wave regime. In particular, we are studying designs that minimize interconnect resistance through optimization of source and drain routing. Some of the ideas to reduce interconnect resistance include use of multiple levels and thicker levels of metal and use of multiple source and drain pads. We are also exploring designs that separate DC and RF paths through on-chip bias networks.



▲ Figure 1: Maximum power (at peak PAE) vs. frequency of operation obtained in nominal 0.25-um devices (V_{dd}=2.5 V) and 65-nm devices (V_{dd} =1 V) fabricated in a 65-nm process [1].



▲ Figure 2: Maximum Power (at peak PAE) vs. device width for different frequencies for 65-nm devices (V_{dd} =1 V) [1].

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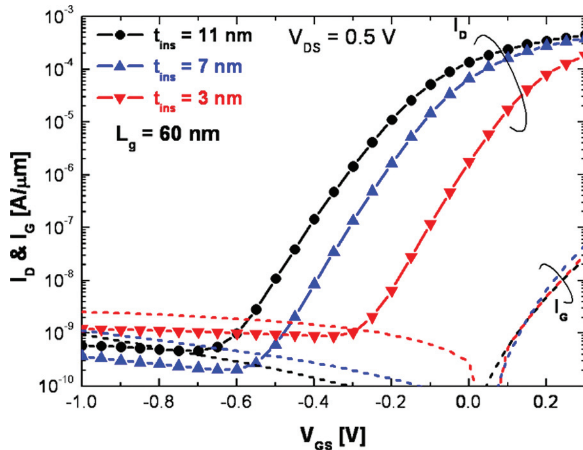
Scaling Potential of InGaAs HFETs for Beyond-the-roadmap CMOS

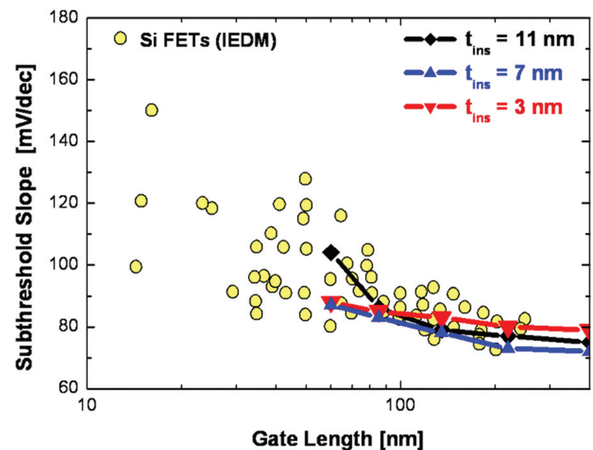
D.-H. Kim, J.A. del Alamo
Sponsorship: Intel Corporation, SRC/FCRP MSD

While a matter of considerable debate, the semiconductor device technology that has been responsible for the microelectronics revolution of the last 30 years appears to be reaching the end of the roadmap. There are severe doubts that it will make economic sense for Si CMOS to scale beyond the 22-nm node. In the landscape of alternatives to Si CMOS for beyond-the-roadmap logic applications, III-V compound semiconductors really stand out. For example, InGaAs looks particularly promising. Since room temperature bulk electron mobility of InGaAs is easily in excess of 10,000 cm^2/V-s, it is imperative to consider this material as a channel for next-generation "low-power" and "high-speed" logic technology.

In our work, we are investigating the scaling potential of InGaAs heterostructure-FETs (HFETs) as a model system to study the challenges and opportunities of III-V based FETs for logic. We have fabricated InGaAs HFETs with a 70% InAs composition in the channel and with varying gate lengths (L_g, from 400 nm to 60 nm) and InAlAs insulator thickness (t_{ins}, from 11 nm to 3 nm). Figure 1 shows subthreshold and gate leakage (I_G) characteristics of representative 60-nm InGaAs HFETs with three different t_{ins}, at V_{DS} = 0.5 V. As t_{ins} decreases, V_T shifts positively and the subthreshold slope improves considerably. The value of S = 88 mV/dec is obtained for the t_{ins} = 3 nm device, and this sharp subthreshold characteristic yields an I_{ON}/I_{OFF} ratio in excess of 10^4. Figure 2 compares S as a function of L_g between InGaAs HFETs with three different t_{ins} and Si CMOS. Our devices exhibit almost the same electrostatic integrity and, especially, InGaAs HFETs with t_{ins} = 3 nm exhibit values of S, that are on the low range of the reported state-of-the-art Si CMOS. Our research strongly confirms that InGaAs HFETs are an excellent test vehicle to explore issues of great relevance to future III-V FETs, such as self-aligned architectures, scaling limit of planar devices, band-to-band tunneling in a narrow band-gap (E_g) material, impact of strain on transport physics and the consequences of a low density of states on the current deeply scaled devices.



▲ Figure 1: Subthreshold and gate leakage characteristics of 60-nm InGaAs HFETs with three different t_{ins} at V_{DS} = 0.5 V. The t_{ins} = 3 nm devices exhibit almost enhancement mode operation (V_T = - 0.02 V), subthreshold slope (S) = 88 mV/dec and $I_{ON}/I_{OFF} > 10^4$.



▲ Figure 2: Subthreshold slope as a function of gate length for InGaAs HFETs with various insulator thickness, as well as Si CMOS. Well designed InGaAs HFETs exhibit values of the subthreshold slope that are on the low range of state-of-the-art Si CMOS.

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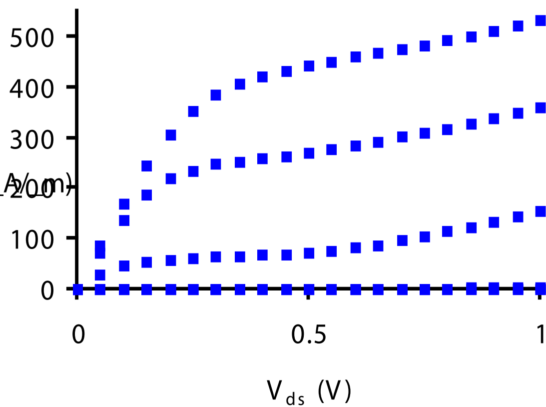
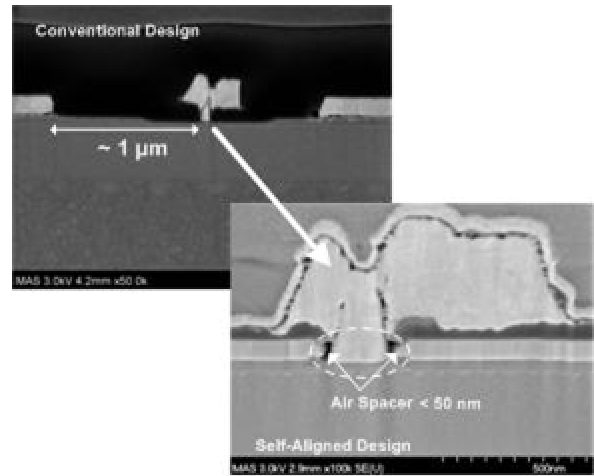
Self-aligned InGaAs HEMT for Logic Applications

N. Waldron, J.A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel Foundation Ph.D. Fellowship Program

As conventional CMOS scaling approaches the end of the roadmap, identifying a new logic device technology is becoming a matter of great urgency. With room-temperature electron mobility easily in excess of 10,000 $cm^2/V.s$, InGaAs represents a very attractive proposition as a channel material. Previously it has been shown that InGaAs-based high electron mobility transistors (HEMTs) show great promise for logic applications. The 60-nm devices fabricated with a triple recess process showed a significant improvement in drive current compared to 65-nm CMOS for the same level of leakage current [1]. However, the conventional design of HEMTs is not well suited for VLSI applications. The gate is not self-aligned and is typically separated from the source/drain by a distance of around 1µm, which results in a large device footprint and associated parasitics. Also the exposed surface area and alloyed contacts represent reliability concerns.

To address these issues we have developed a self-aligned process that reduces the gate to source/drain distance to less than 50 nm. This is more than a 20x improvement over the conventional design. The new device relies on the use of W for non-alloyed ohmic contacts. A two-step e-beam lithography process is used to define the gate. The first step defines both the W source/drain contacts and the gate foot, resulting in a final structure that is self-aligned. An SEM of the completed device is shown in Figure 1. The output characteristics of a 0.3-µm device are shown in Figure 2. The self-aligned devices show excellent DC characteristics. The device has a maximum transconductance of 988 µS/um, SS of 77 mV/dec, DIBL of 44 mV/V and an I_{on}/I_{off} ratio of 6 x 10^3. Currently we are working on fabricating devices of varying gate lengths to determine the scaling potential of the self-aligned scheme. We are also exploring various approaches to achieve enhancement-mode devices.





▲ Figure 1: An SEM comparing a conventional HEMT to a self-aligned HEMT device. The source/drain is separated from the gate by a distance of 1 um in the conventional design. Using the self-aligned architecture use of an air-spacer reduces this distance to less than 50 nm.

▲ Figure 2: Output characteristics of a 0.3-µm device fabricated using the self-aligned process. The device threshold voltage is -0.2 V.

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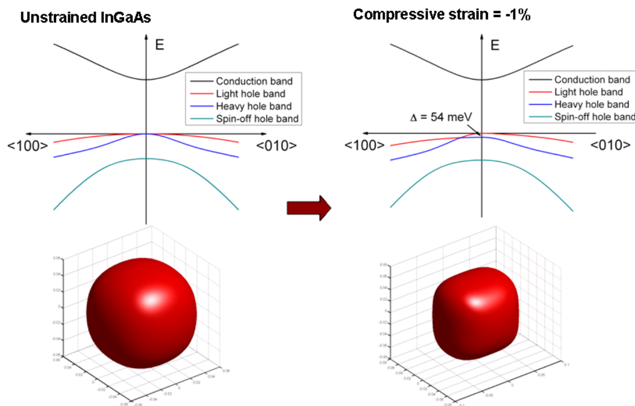
P-channel InGaAs HEMTs for beyond-Si Complementary Logic

L. Xia, J.A. del Alamo
Sponsorship: SRC/FCRP MSD

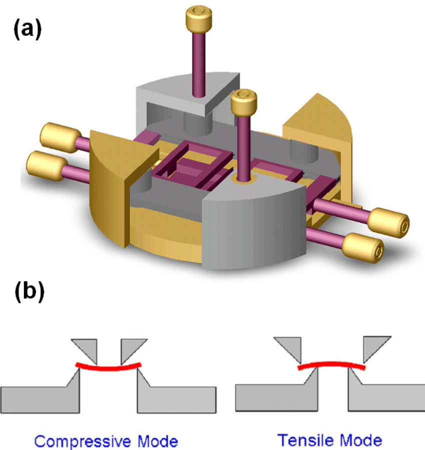
As the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches the end of the roadmap, its performance improvement brought by size scaling will reach a limit. Among the beyond-Si logic alternatives, InGaAs shows superior potential for n-channel FET-type devices [1]. However, the hole mobility in InGaAs is currently not much higher than that in silicon. In fact, the large disparity between n- and p-channel InGaAs FET performance raises concerns about the possibility of implementing InGaAs CMOS-type logic.

In order to boost the speed of p-channel InGaAs FETs, we are studying the enhancement of the hole mobility by mechanically straining the channel. This has been demonstrated in Si and Ge devices. Compared with their unstrained counterparts, strained Ge and Si showed 6× and 2× higher hole mobilities respectively. [2, 3] We are carrying out simulations that indicate that strain will also show positive effects on hole mobility in InGaAs. As shown in Figure 1, in unstrained InGaAs, the heavy-hole and light-hole valence bands are degenerate at the Γ point. When strain is applied, the two bands split. This splitting leads to preferential occupation of holes into the lighter band, so that the effective mass of the holes decreases. In this way, the hole mobility should be enhanced.

To experimentally probe the potential enhancement brought by strain, a chip-bending apparatus (Figure 2a) has been fabricated. This apparatus has four ridges whose vertical and horizontal positions are controlled by micrometers. By positioning the ridges as shown in Figure 2b, we can apply either tensile or compressive strain on the upper surface of the chip. By fitting the apparatus into a probe station, we can conduct electrical measurements on strained samples. These measurements are expected to provide understanding of the speed-enhancing effects of strain in InGaAs FET's.



▲ Figure 1: Simulation results of strain-induced band structure change in InGaAs. The bandstructures and light-hole iso-energy surfaces of unstrained and strained InGaAs are shown. Under 1% compressive strain, the heavy-hole band and light-hole band split apart by the amount of 54 meV. The shapes of light-hole iso-energy surface indicate that strain also breaks the symmetry of the light-hole band. This anisotropy would allow us to better tailor both in-plane and out-plane effective masses.



▲ Figure 2: (a) Schematic figure of the chip-bending apparatus. (b) Methods to apply compressive and tensile strain to the chip surface.

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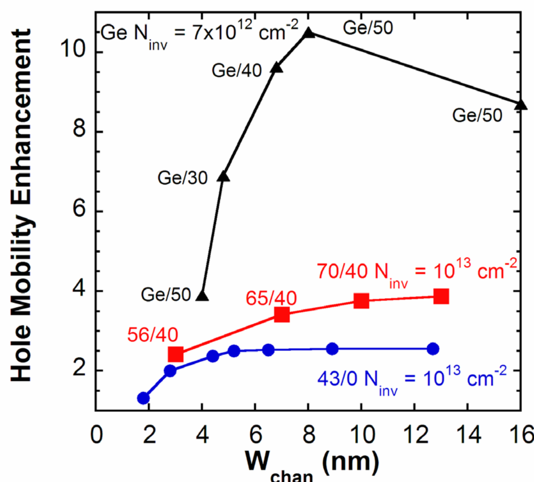
Strained SiGe-channel p-MOSFETs: Impact of Heterostructure Design and Process Technology

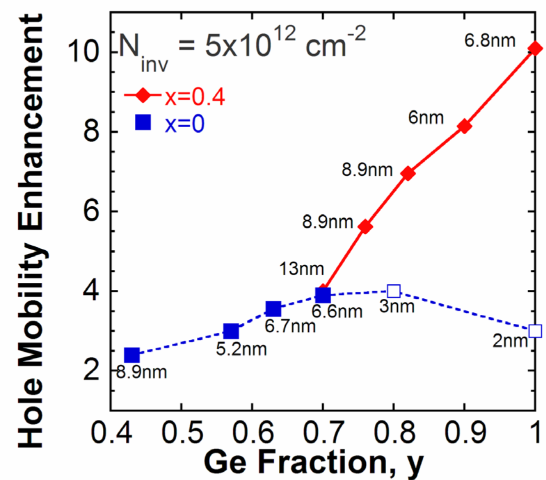
C. Ní Chléirigh, J.L. Hoyt
Sponsorship: SRC, SRC/FCRP MSD, Texas Instruments Fellowship, Applied Materials Fellowship

Superior hole mobility (up to 10X enhancement over bulk Si channels) and compatibility with mainstream Si processing technology make compressively strained SiGe an attractive channel material for sub-45-nm p-MOSFETs. This research investigates strained SiGe as a suitable channel material for p-MOSFETs using SiGe grown pseudomorphically on both relaxed SiGe and bulk Si substrates. Strained SiGe channels directly on bulk Si are appealing due to the relative ease of integration with mainstream CMOS processing. However, there are severe critical thickness constraints on the strained SiGe channel for Ge compositions above 40 at. %. Reducing the lattice mismatch by growing the strained SiGe channel on a relaxed SiGe virtual substrate allows investigation of high Ge composition channels independent of critical thickness constraints. To understand the performance possibilities for these structures, it is essential to understand the impact of channel thickness, W_{chan}, on hole mobility.

Hole mobility for 43% Ge pseudormophic SiGe channels drops for W_{chan} below 4 nm due to increased phonon and Si/SiGe interface scattering (Figure 1). The 70/40 structure follows a similar trend; however, there is a large drop in Ge concentration for the 3-nm channel. The thermal budget will reduce final Ge % (and mobility), especially for thinner films, higher Ge fraction and increased strain [1]. For the strained Ge channel there is a dramatic drop in mobility for W_{chan} below 6 nm due to increased interface roughness and some drop in the Ge concentration. Mobility enhancements for SiGe heterostructres are plotted in Figure 2 as a function of Ge fraction in the strained layer for bulk Si and relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate. Use of a virtual substrate can produce peak mobility enhancements of up to 10X. Peak enhancements are limited to 4X for strained SiGe channels on bulk Si due to the mobility degradation for thinner channels required at high Ge compositions.



▲ Figure 1: Hole mobility enhancement as a function of strained SiGe channel thickness, W_{chan} for strained Ge on a relaxed SiGe virtual substrate (triangles), strained $Si_{0.3}Ge_{0.7}$ on relaxed $S_{i0.6}Ge_{0.4}$ (squares) and strained $Si_{0.57}Ge_{0.43}$ on bulk Si (circles). Drop in mobility for strained SiGe channels for W_{chan} below 4 nm. Drop in mobility below 6 nm for Ge channels due to interface roughness. Ge composition in strained SiGe (Y %) and relaxed virtual substrate (X%) are denoted Y/X for each point.



▲ Figure 2: Mobility enhancement as a function of Ge fraction for strained SiGe channels grown on bulk Si (squares) and relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate (diamonds). Solid symbols: results from this work. Open symbols: [2]. Strained SiGe channel thickness noted for each point. Critical thickness constraints limit channel thickness for strained SiGe channels on bulk Si, restricting mobility enhancements for high Ge compositions.

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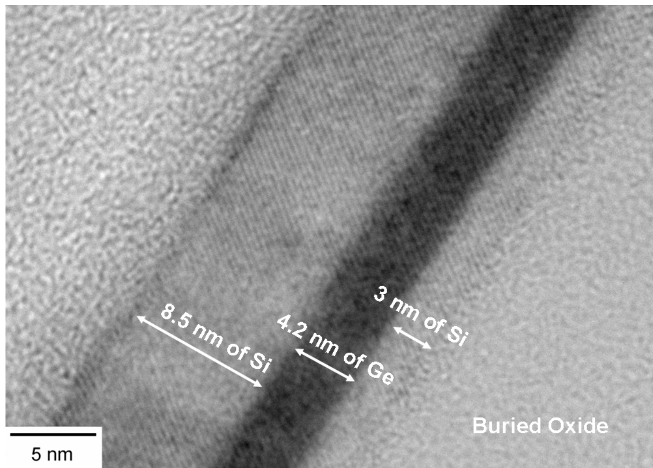
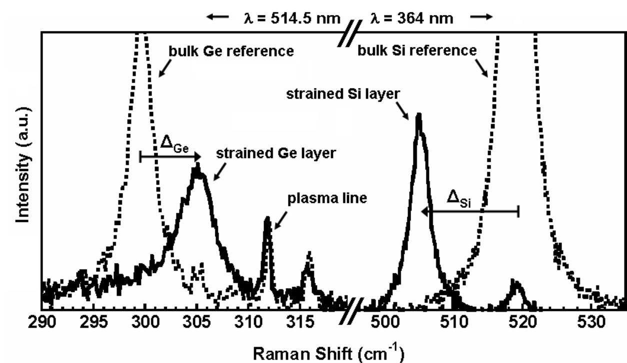
Strained-Si/strained-Ge Heterostructure-on-insulator for Improved CMOS Performance

L. Gomez, M.K. Kim, J.L. Hoyt
Sponsorship: SRC/FCRP MSD

Geometric scaling of device dimensions can no longer provide the necessary current drive enhancements to continue historic performance gains. Novel channel materials as well as strain can provide enhanced transport characteristics that help to maintain this historic trend. Thin-body devices can also offer the benefit of improved electrostatic control in deeply scaled MOSFETs. In previous work, fully depleted MOSFETs were fabricated on Si/SiGe heterostructures (55% Ge) to realize both enhanced transport for electrons and holes and improved subthreshold characteristics [1]. Subthreshold swing was improved over heterostrucutre-on-bulk devices and was observed to be 66-70 mV/dec. Mobility enhancements of 1.9x and 2.8x were observed for electrons and holes, respectively, at an inversion charge density of $1.5x10^{13}$ cm^{-2}. Heterostructure-on-bulk MOSFETs with pure Ge buried channels have exhibited mobility enhancement factors of 10x for holes [2-3], motivating the fabrication of strained-Ge heterostructures on insulator. The Ge-HOI substrate combines the excellent electrostatic characteristics observed in UTB SOI with the high mobility benefits of a strained-Si/strained-Ge heterostructure. In this work, Ge HOI is fabricated by epitaxial growth and layer transfer by bond and etch-back. A process was developed to grow thin Ge films on strained Si using an intermittent SiGe passivating layer (strained Si layers were pseudomorphic to 50% Ge relaxed SiGe layers). Figure 1 presents a cross-sectional transmission electron microscopy image of a Ge-HOI substrate. Figure 2 presents Raman analysis that was conducted to verify strain retention in the buried Ge layer. Further development is being conducted to fabricate short channel devices on these substrates.



▲ Figure 1: Crosssectional transmission electron microscopy image of the final Ge-HOI substrate. The layers in this structure were grown to be pseudomorphic to relaxed $Si_{0.5}Ge_{0.5}$.



▲ Figure 2: Raman spectra from the Ge-HOI substrate using 364- and 514.5-nm excitation to obtain a signal from the Si cap and Ge buried layer, respectively. The UV and visible Raman spectra are shown for the Ge-Ge and Si-Si LO phonons from bulk crystals (dotted black curves) and the Ge-HOI substrate (black solid curve). Raman analysis courtesy M. Canonico, Freescale Semiconductor.

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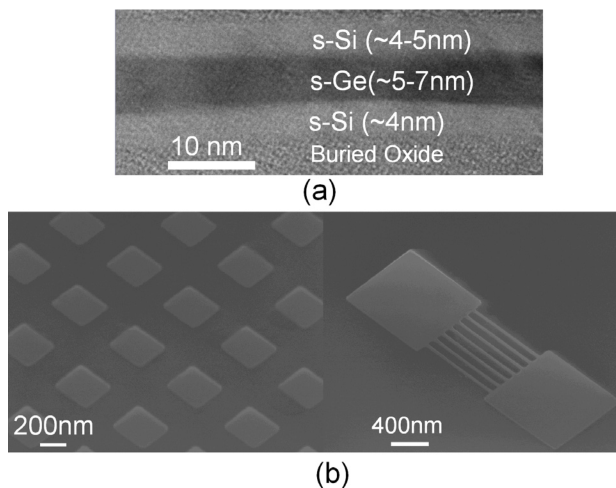
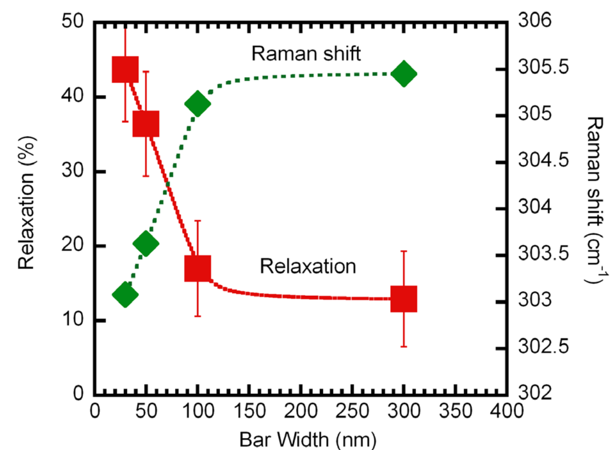
Strain in Nano-scale Patterned Strained Si/strained Ge Heterostructures on Insulator

P. Hashemi, L. Gomez, J.L. Hoyt
Sponsorship: SRC/FCRP MSD

Possessing superior electron and hole transport characteristics, thin-body strained Si/ strained-SiGe (Ge)/strained Si heterostructures on insulator (HOI) MOSFETs are possible candidates for future low-power CMOS [1]. However, when these substrates are patterned into nano-scale mesas and fins, some changes in the stress profile are expected that may either degrade or enhance the mobility of the devices. Here, we report the variation of the stress profile in the strained-Si and strained-Ge layers as a function of the patterning geometry and thickness of strained layers. Finite element simulations in TAURUS TSUPREM IV™ were also performed to support experimental results. Strained heterostructure substrates used in this work were fabricated by a bond-and-etch-back method followed by thinning the cap layer by wet oxidation and removal. Figure 1(a) shows a typical TEM image of such a substrate. Scanning electron beam lithography with HSQ as a negative tone resist was used to create nano-scale long bars and mesas with sub-300-nm geometries. The density of these features is a key to achieving a measurable Raman signal to analyze the stress profile. The pattern transfer was performed in an RIE system stopping at the buried oxide interface. Figure 1(b) shows sample SEM images of patterned mesas and long bars. UV Micro-Raman spectroscopy with 325-nm He-Cd and 364-nm Ar-Ion laser lines was used to explore the stress profile in the patterned ultra-thin strained Ge and strained Si layers, respectively. Figure 2 shows the relaxation percentage and position of the Raman peak in the strained Ge layer as a function of bar width for patterned long bars. As can be seen from this figure, the relaxation in strained Ge is increased when the pattern width is reduced. For 30-nm-wide patterns, a relaxation of around 43% is measured. Finite element stress simulations demonstrate that the longitudinal stress component along the bars is almost maintained while the in-plane component tends to relax in the narrow direction of the bars. As a result, the biaxial stress profile of the unpatterned structure tends to move towards uniaxial strain for ultra-narrow structures, which can further enhance hole transport properties. On the other hand, the results on relaxation in nano-scale pattern mesas indicate a general trend of relaxation with decreasing aspect ratio. As an example, the 100-nm, square-shape mesas show nearly 33% relaxation (assuming isotropic biaxial strain) indicating that a large amount of strain can still be preserved in patterned regions suitable for fabrication of planar HOI MOSFETs.



▲ Figure 1: (a) A TEM image of the HOI structure before patterning. (b) Tilted SEM images of the 300-nm-wide patterned square mesas (left) and 24-nm-wide patterned multi-fin mesas (right).



▲ Figure 2: Relaxation and Raman peak position as a function of the bar width in the strained-Ge layer. Raman measurements and analysis courtesy of M. Canonico, Freescale Semiconductor, Inc.

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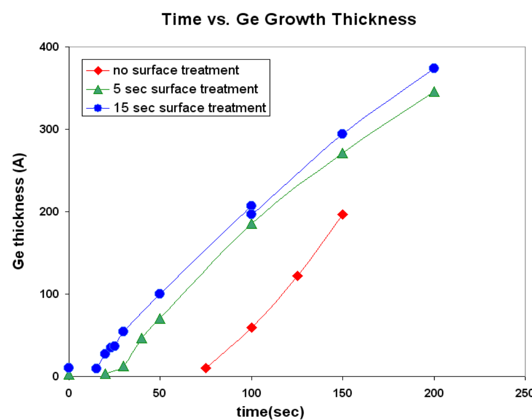
Epitaxial Growth of Ultrathin Ge on Si Substrates

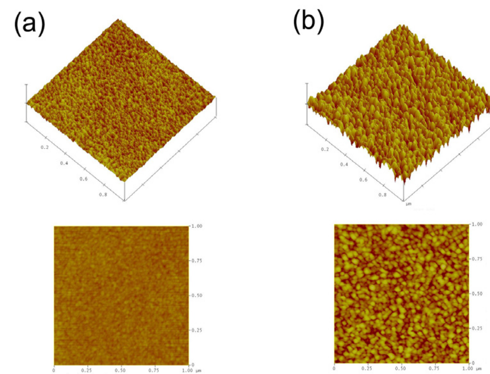
M. Kim, L. Gomez, J.L. Hoyt
Sponsorship: DARPA, NSF Graduate Research Fellowship

Growing ultrathin, uniform germanium epitaxial films with minimal crystal defect density is desirable for several applications to emerging technologies. For example, multilayer structures of Ge and SiGe on Si wafers are used for enhanced-mobility heterostructure-on-insulator (HOI) MOSFETS, and thin Ge films are used as seed layers in CMOS-compatible photodetectors. However, due to the 4% mismatch in lattice size, the initial stages of Ge growth on Si substrates show a 3-D growth mode, in which Ge initially forms islands and then coalesces to form a more uniform surface [1-2]. To improve the morphology of Ge films with thickness in the range of 20A to 50A, several growth parameters and surface treatment methods were studied using an Applied Materials Epi Centura Reactor. Varying growth temperature and pressure, the optimal condition for ultrathin Ge films on Si substrates was determined to be 365ºC and 60T, with 5slpm of Hydrogen flow to the slit.

A surface treatment consisting of a SiGe pulse before Ge growth improves the surface smoothness greatly, as well as enhancing the growth rate. Before Ge growth, a short "pulse" of 5-15 seconds of 50% SiGe was used to treat Silicon surface, and this treatment was shown to enhance Ge growth on Si substrates, as shown in Figure 1. Figure 2 shows improved film uniformity for SiGe-pulse treated samples. With this new technique, the RMS values as well as average peak-to-valley heights are improved by a factor of ~3.



▲ Figure 1: The germanium thickness as a function of growth time. The graph shows a reduced incubation period for SiGe-pulse treated samples. Epitaxial Ge was grown at 365ºC, 60T on P- CZO Si wafers in Applied Materials's "Epi Centura" System.



▲ Figure 2: The 1um x 1um AFM scans of 35A-thick Ge films grown on Si substrates, (a) with 15-sec SiGe pulse surface treatment and (b) without SiGe pulse. For (a), RMS is 0.251 nm, with average peak heights of 1.4 nm. Without the surface treatment, the Ge film is much rougher, with RMS value of 0.686 nm and peak heights of 5 nm, as shown in (b).

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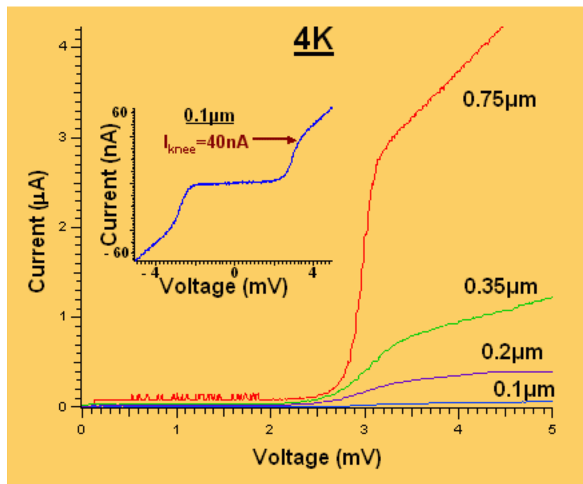
Niobium Superconducting Persistent-current Qubits with Deep Submicron Josephson Junctions

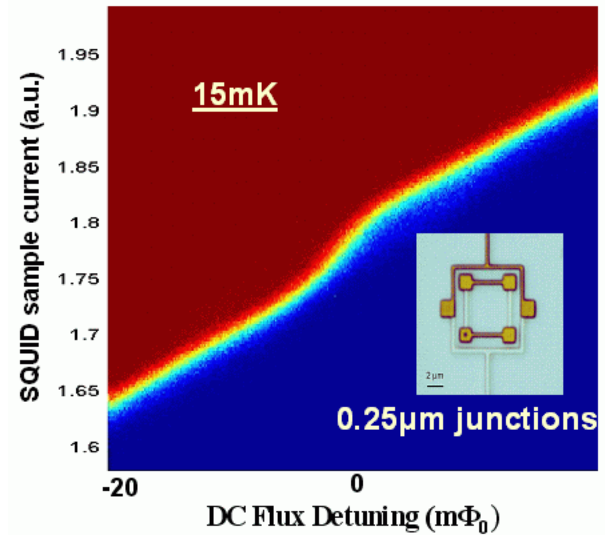
D.M. Berns, W.D. Oliver, S.O. Valenzuela, T.P. Orlando, V. Bolkhovsky, E. Macedo

Quantum computation holds the potential to solve problems currently intractable with current computers. The basic component of a quantum computer is the "qubit," the quantum analog to today's bits. Although any two-level quantum system could serve as a qubit; however, the qubit must satisfy two major criteria for practical quantum computing: long coherence times and the ability to scale to thousands of qubits. Persistent-current (PC) qubits are promising candidates for realizing such a large-scale quantum computer. The PC qubit is a superconducting circuit with Josephson junction (JJ) elements that can be effectively operated as a two-level quantum system [1].

With a tri-layer process using optical lithography, we can create the deep-submicron JJs required to realize large qubit tunnel-couplings, which allow improved immunity to dielectric-induced decoherence, and there is no foreseeable barrier to large-scale integration. We have recently begun measuring and characterizing the PC qubits designed with these deep-submicron JJs fabricated with the Nb-Al/AlOx-Nb trilayers. Initital testing of the JJs shows excellent performance down to sizes necessary for long decoherence times (Figure 1), and first studies of how the ground state of the new qubits changes as the applied DC flux is swept show the large tunnel-couplings we were aiming for (Figure 2).



▲ Figure 1: IV traces taken at 4K for a few different test junctions, from 0.75 um down to 0.1um. Blown up in the inset is the 0.1-um junction IV and we see a knee current of 40 nA and a very large subgap resistance.



▲ Figure 2: Qubit step taken at dilution refrigerator temperatures with the device seen in the inset, where the larger junctions are 250 nm on a side. One can clearly see that as the applied DCmagnetic flux is changed, the ground state changes from one circulating current state to the other.

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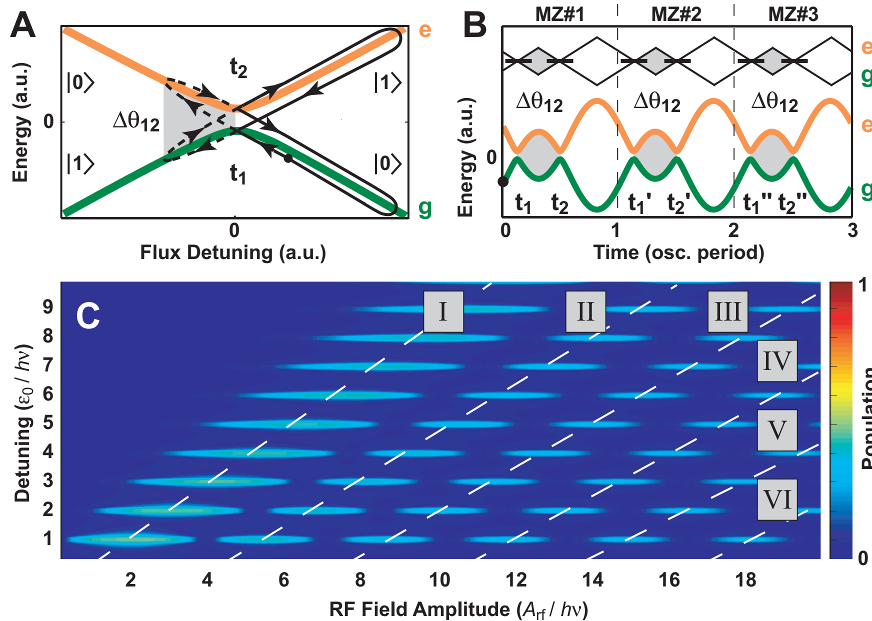
Mach-Zehnder Interferometry in a Persistent-current Qubit

W.D. Oliver, Y. Yu, J.C. Lee, K.K. Berggren, L.S. Levitov, T.P. Orlando

We have demonstrated Mach-Zehnder (MZ)-type interferometry with a niobium superconducting persistent-current qubit. These experiments exhibit remarkable agreement with theory, and they will find application to non-adiabatic qubit control methods. The qubit is an artificial atom, the ground and first-excited states of which exhibit an avoided crossing. Driving the qubit with a large-amplitude harmonic excitation sweeps it through this avoided crossing two times per period. The induced Landau-Zener (LZ) transitions at the avoided crossing cause coherent population transfer between the eigenstates, and the accumulated phase between LZ transitions varies with the driving amplitude. This is analogous to a Mach-Zehnder interferometer, in which the LZ transition is the beamsplitter and the relative phase accumulated between LZ transitions is the optical path-length difference between the arms of the interferometer. Over the entire length of the microwave driving pulse, we have a sequence of Mach-Zehnder interferometers. We have observed MZ quantum interference fringes as a function of the driving amplitude for single- and multi-photon excitations.



▲ Figure 1 : (a) Energy of the two-level system. Starting at the marker, the qubit state is swept through the avoided crossing twice, accumulating a phase between the LZ transitions that occur. (b) The corresponding energy variation over a few pulse periods. The sequence of LZ transitions and phase accumulation are analogous to a sequence of Mach-Zehnder interferometers. (c) Qubit population as a function of driving amplitude. We see the Bessel dependence to the Mach-Zehnder-like quantum interference for n-photon transitions.

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Coherent Quasiclassical Dynamics of a Niobium Persistent-current Qubit

D.M. Berns, W.D. Oliver, S.O. Valenzuela, A.V. Shytov, K.K. Berggren, L.S. Levitov, T.P. Orlando

We have recently demonstrated Mach-Zehnder (MZ)-type interferometry in the persistent-current (PC) qubit, in the strong driving limit [1]. We have now extended this work to much lower driving frequencies [2]. By driving our system at frequencies smaller than our linewidth, we have observed a new regime of quasiclassical dynamics within the strong driving limit. Now a transition at a DC flux detuning resonant with n photons is assisted by neighboring resonances. In this regime we find remarkable agreement with theory by assuming the population transfer rate for the nth photon resonance is the sum of rates from all other resonances.

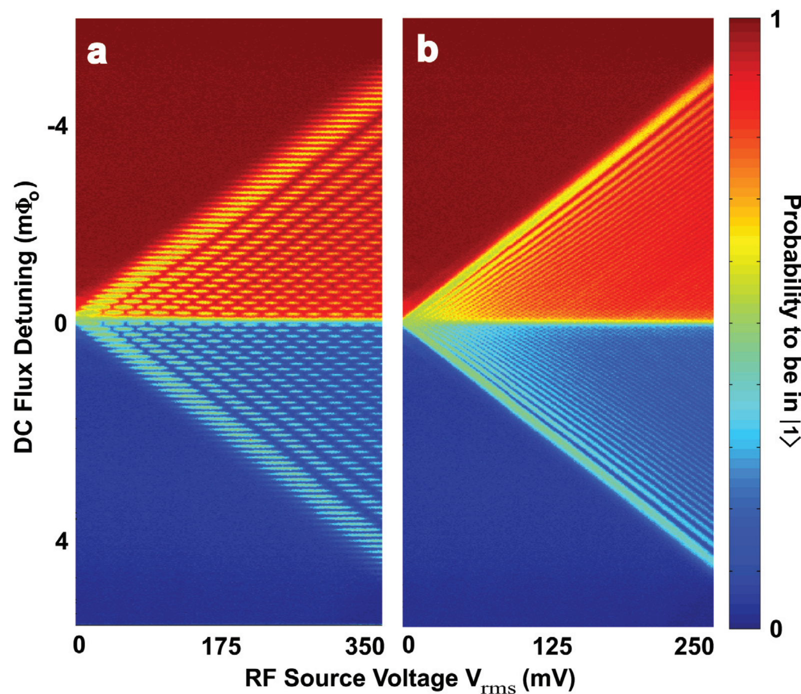

Figure 1 : Qubit population as a function of driving amplitude. (a) Driving frequency = 270 MHz. We see the Bessel dependence to the Mach-Zehnder-like quantum interference for n-photon transitions. (b) Driving frequency = 90 MHz. Individual resonances are no longer distinguishable but we still see coherent quantum interference.

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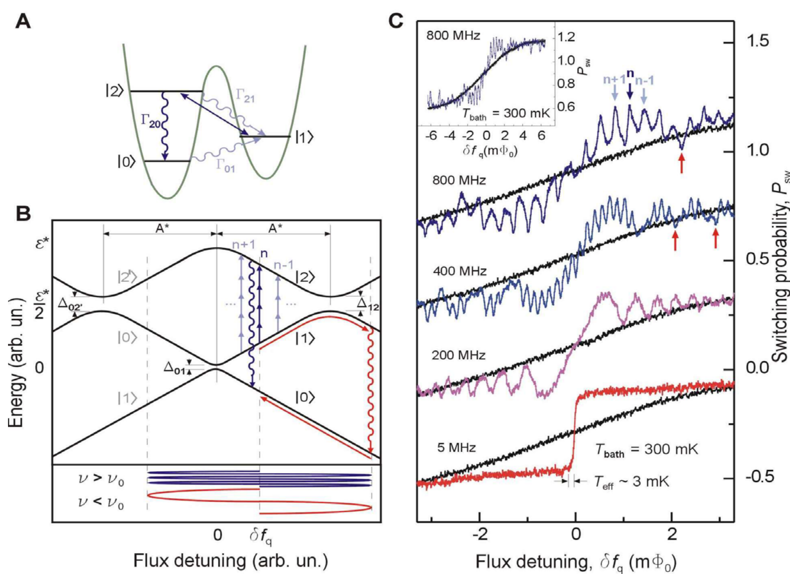
Microwave-induced Cooling of a Superconducting Qubit

S.O. Valenzuela, W.D. Oliver, D.M. Berns, K.K.Berggren, L.S. Levitov, T.P. Orlando

We have recently demonstrated microwave-induced cooling in a superconducting flux qubit [1]. The thermal population in the first-excited state of the qubit is driven to a higher-excited state by way of a sideband transition. Subsequent relaxation into the ground state results in cooling. Effective temperatures as low as 3 millikelvin are achieved for bath temperatures from 30 - 400 millikelvin, a cooling factor between 10 and 100. This demonstration provides an analog to optical cooling of trapped ions and atoms and is generalizable to other solid-state quantum systems. Active cooling of qubits, applied to quantum information science, provides a means for qubit-state preparation with improved fidelity and for suppressing decoherence in multi-qubit systems.



▲ Figure 1 : Sideband cooling in a flux qubit. (a) Double-well illustration of cooling. External excitation transfers thermal population from state 1 to state 2, from which it decays to the ground state 0. (b) Band diagram illustration of cooling. One to two transitions are driven resonantly at high driving frequencies and occur adiabatically at low driving frequency. (c) Thermal population cooled at different frequencies. Cooling from 300mK to as low as 3mK is shown.

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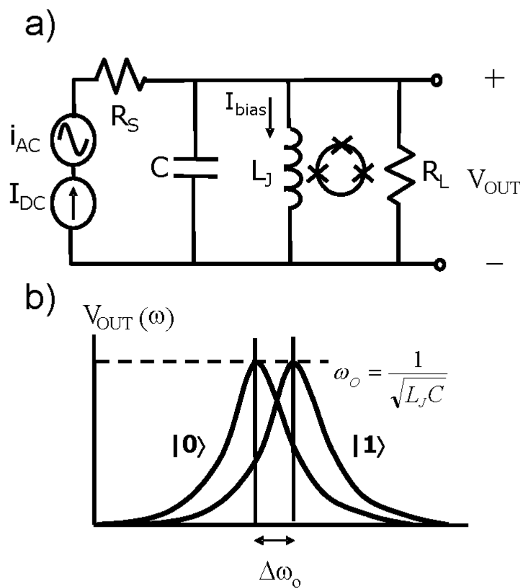
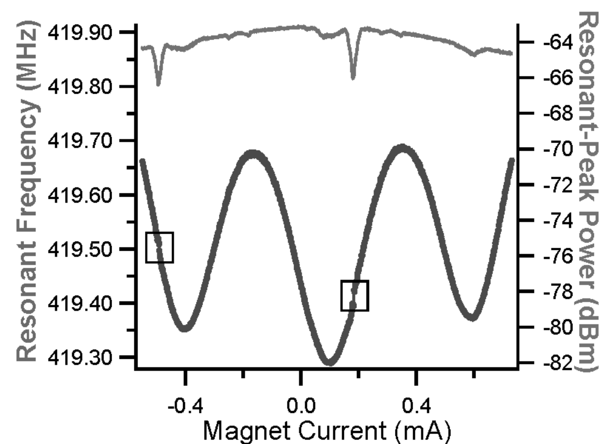
Resonant Readout of a Persistent-current Qubit

J.C. Lee, W.D. Oliver, T.P. Orlando
Sponsorship: DURINT, DTO, NSF

The two logical states of a persistent-current (PC) qubit correspond to oppositely circulating currents in the qubit loop. The induced magnetic flux associated with the current either adds to or subtracts from the background flux. The state of the qubit can thus be detected by a DC SQUID magnetometer inductively coupled to the qubit. We have implemented a resonant technique that uses a SQUID as a flux-sensitive Josephson inductor for qubit readout. This approach keeps the readout SQUID biased at low currents along the supercurrent branch and is more desired for quantum computing applications in reducing the level of decoherence on the qubit. By incorporating the SQUID inductor in a high-Q on-chip resonant circuit, we can distinguish the two flux states of a niobium PC qubit by observing a shift in the resonant frequency of the readout circuit. The nonlinear nature of the SQUID Josephson inductance, as well as its effect on the resonant spectra of the readout circuit, was also characterized.



▲ Figure 1: a) The SQUID inductor is incorporated in a resonant readout circuit. It is inductively coupled to a PC qubit to detect its state. b) A transition of the qubit state changes the Josephson inductance of the SQUID and can be sensed as a shift in the resonant frequency of the readout circuit.



▲ Figure 2: Experimental results at 300 mK: the lower plot (left axis) shows the modulation of the resonant frequency with external magnetic field. Qubit steps corresponding to transitions between opposite flux states were observed at every 1.3 periods of the SQUID lobe. The upper plot (right axis) shows the corresponding peak amplitude of the resonant spectrum. The dip in peak power coincides with the qubit step.

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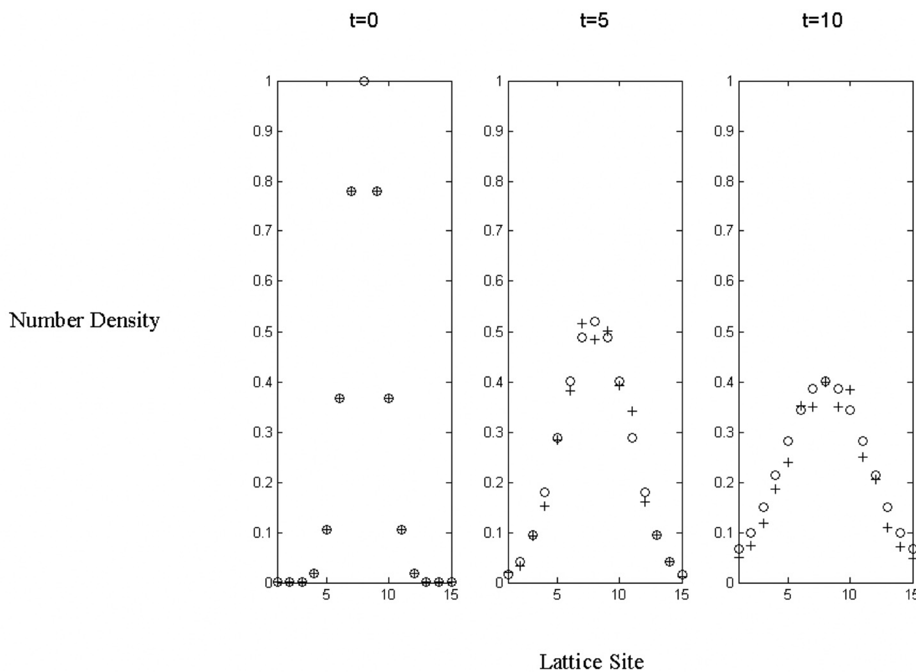
Type-II Quantum Computing Using Superconducting Qubits

D. Berns, W.M. Kaminsky, B. Cord, K. Berggren, W. Oliver, T.P. Orlando (in coll. with J. Yepez (Air Force Laboratories)
Sponsorship: AFOSR, Fannie and John Hertz Foundation

The Factorized Quantum Lattice-Gas Algorithm (FQLGA) [1] is a quantum version of classical lattice-gases (CLG) [2]. The CLGs are an extension of classical cellular automata with the goal of simulating fluid dynamics without reference to specific microscopic interactions. The binary nature of the CLG lattice variables is replaced for the FQLGA by the Hilbert space of a two-level quantum system. The results of this replacement are similar to that of the lattice-Boltzmann model, but with a few significant differences [3]. The first is the exponential decrease in required memory. The second is the ability to simulate arbitrarily small viscosities.

We have recently developed two implementations of the algorithm for the 1D diffusion equation using the PC Qubit [4]. The first consists of initializing the qubits while keeping them in their ground state and then performing the collision by quickly changing their flux bias points and then performing a single /2 pulse (Figure 1). This initialization technique could prove quite useful, since relaxation effects are avoided, but the way we have implemented the collision is not easily generalized to other collisions. A more general collision implementation was then developed by decomposing the unitary collision matrix into a sequence of single qubit rotations and coupled free evolution. The single qubit rotations then also serve to initialize the fluid's mass density.



▲ Figure 1: Simulation of the FQLGA for 1D diffusion is pictured (o) alongside simulation of the first proposed implementation (+). The expected diffusion of a Gaussian is observed.

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Scalable Superconducting Architecture for Adiabatic Quantum Computation

W.M. Kaminsky, S. Lloyd, T.P. Orlando
Sponsorship: Fannie and John Hertz Foundation

Adiabatic quantum computation (AQC) is an approach to universal quantum computation in which the entire computation is performed in the ground state of a suitably chosen Hamiltonian [1]. As such, AQC offers intrinsic protection against dephasing and dissipation [2-3]. Moreover, AQC naturally suggests a novel quantum approach to the classically intractable constrained minimization problems of the complexity class NP. Namely, by exploiting the ability of coherent quantum systems to follow adiabatically the ground state of a slowly changing Hamiltonian, AQC promises to bypass automatically the many separated local minima occurring in difficult constrained minimization problems that are responsible for the inefficiency of classical minimization algorithms. To date, most research on AQC [4-8] has focused on determining the precise extent to which it could outperform classical minimization algorithms. The tantalizing possibility remains that---at least for all practical purposes---AQC offers at least a large polynomial, and often an exponential, speedup over classical algorithms. However, it may be the case that in the same way the efficiency of many practical classical algorithms for NP problems can be established only empirically, the efficiency of AQC on large instances of classically intractable problems can be established only by building a large-scale AQC experiment.

To make feasible such a large-scale AQC experiment, we have proposed a scalable architecture for AQC based on the superconducting persistent-current (PC) qubits [9-10] already under development here at MIT. As first proposed in [11], the architecture naturally incorporates the terms present in the PC qubit Hamiltonian by exploiting the isomorphism [12] between antiferromagnetic Ising models in applied magnetic fields and the canonical NP-complete graph theory problem Max Independent Set. Such a design notably removes any need for the interqubit couplings to be varied during the computation. Moreover, since the Max Independent Set remains NP-complete even when restricted to planar graphs where each vertex is connected to no more than 3 others by edges, a scalable programmable architecture capable of posing any problem in the class NP may simply take the form of a 2D, hexagonal, square, or triangular lattice of qubits. Finally, the latest version of the architecture [13] permits interqubit couplings to be limited to nearest-neighbors and qubit measurements to be inefficient.

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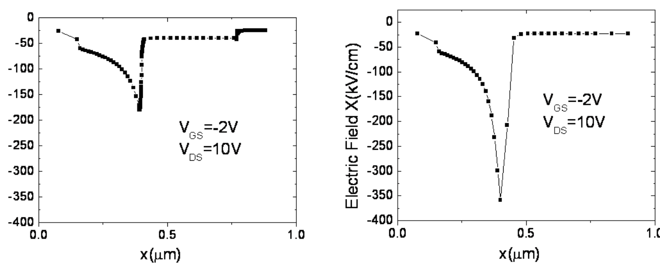
Improvement of Electron Velocity in GaN HEMTs by Electric Field Engineering

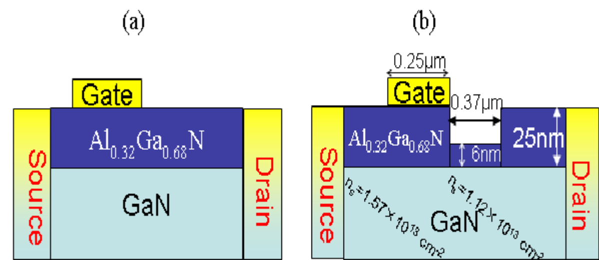
X. Zhao, J.W. Chung, T. Palacios
Sponsorship: ONR, MIT, MTL

Electron velocity influences both the intrinsic delay and drain delay of gallium nitride (GaN) High Electron Mobility Transistors (HEMTs). Although the peak electron velocity in AlGaN/GaN structures is 2.5×10^7cm/s, the electron velocity decreases very fast due to polar optical phonon scattering for electric fields in excess of 150kV/cm [1]. As seen in Figure 1a, in standard GaN HEMT devices, the average electric field under the gate along the channel direction far exceeds the optimal value for peak electron velocity. This high electric field results in an average electron velocity of 1.5×10^7cm/s, significantly lower than the peak velocity. In this project, we propose a new GaN HEMT structure with a recessed drain access region to reduce the electric field in the drain of these transistors. We have used Silvaco/Atlas to simulate these new devices. Figure 2 shows the structure of a conventional AlGaN/GaN HEMT and the novel HEMT device proposed in this work.

In the recessed devices, the carrier concentration underneath the recess region is lower than elsewhere, which redistributes the electric field in the channel. Figure 1 shows the electric field along the channel in two structures of Figure 2. Due to the lower electric field peak in the novel structure, the average electron velocity is boosted by 50%. On the other hand, in our simulations we have not observed any increase in the effective gate length due to the drain recess. This fact in combination with the enhanced electron velocity makes this new structure extremely promising for millimeter- and submillimeter-wave applications.



▲ Figure 1: Electric field along the channel direction in conventional AlGaN/GaN HEMT (a) and along a novel structure with recessed drain access region (b). The average electron velocities are 1.53×10^7cm/s and 2.41×10^7cm/s, respectively.



▲ Figure 2: Diagram of a conventional AlGaN/GaN HEMT structure (a) and the novel HEMT structure with a recess in the drain access region (b). The width of the recess region is 0.37μm.

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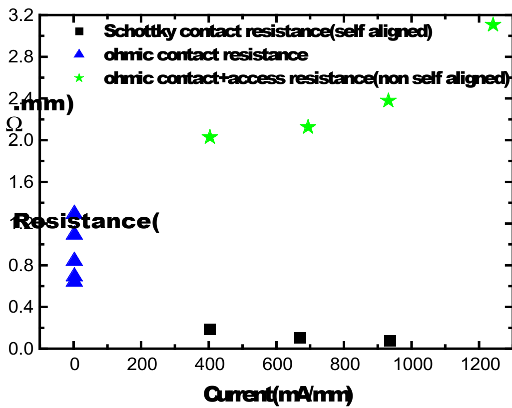
Schottky Drain AlGaN/GaN HEMTs for Millimeter-wave Applications

X. Zhao, J.W. Chung, T. Palacios
Sponsorship: ONR, MIT, MTL

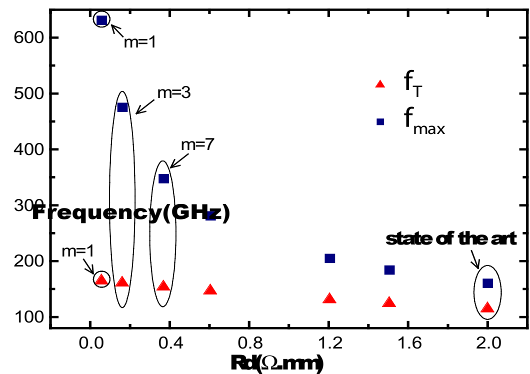
The drain parasitic resistance is one of the main factors limiting the current gain cut-off frequency (f_T) and the power gain cut-off frequency (f_{max}) in high performance AlGaN/GaN HEMTs [1]. The drain parasitic resistance consists of two components: the contact resistance between the metal and the channel and the access resistance due to the distance between the gate edge and drain contact. In this project, we demonstrate a new drain contact technology based on the use of a Schottky metallization.

The use of a Schottky contact in the drain of a HEMT has two major advantages. First, for moderate current levels, the differential resistance of a Schottky contact is much lower than what is achievable with conventional ohmic technology. Second, due to the low thermal budget required in Schottky contact, these contacts can be easily self-aligned to the gate to eliminate the access resistance. Therefore, Schottky drain contact has the potential to outperform the ohmic contact both in contact resistance and access resistance.

Using an Agilent 4155 parameter analyzer, we have measured the ohmic contact and the Schottky contact resistances as a function of the drain current (Figure1). We have also measured the total drain parasitic resistance in devices with conventional ohmic drain contacts. In conventional AlGaN/GaN HEMTs, the total drain parasitic resistance is above 2 Ω·mm and increases with the drain current. In contrast, with use of a Schottky drain contact, the contact resistance is ~0.2 Ω·mm at 500-mA/mm-current level. We have also used the commercial software ADS to simulate the high-frequency performance of Schottky drain AlGaN/GaN HEMTs. As shown in Figure 2, reducing the drain parasitic resistance from 2 Ω·mm to 0.2 Ω·mm increases the f_T from 116 GHz to 162 GHz and increases f_{max} from 162 GHz to 477 GHz.



▲ Figure 1: Measurement of the ohmic contact resistance, Schottky contact resistance and the total parasitic resistance in ohmic contact devices.



▲ Figure 2: Small signal simulations of f_T and f_{max} as a function of R_d. Reducing the drain parasitic resistance from 2Ω·mm to 0.2 Ω·mm increases f_T from 116 GHz to 162 GHz and increases f_{max} from 162 GHz to 477 GHz.

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Estimation of Trap Density in AlGaN/GaN HEMTs from Subthreshold Study

J.W. Chung, X. Zhao, T. Palacios
Sponsorship: ONR, MIT, MTL, KFAS

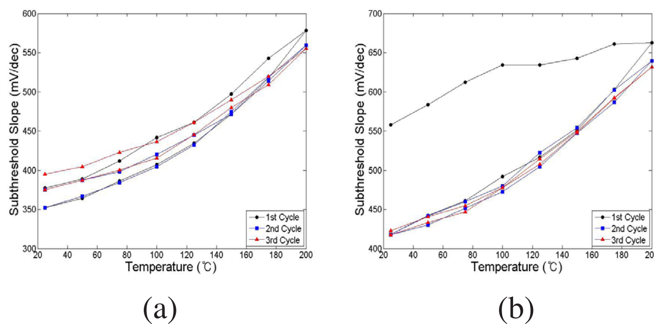
The AlGaN/GaN high electron mobility transistors (HEMTs) have shown outstanding performance on high power and high frequency applications. However, AlGaN/GaN HEMTs suffer from a much higher subthreshold slope than the theoretical limit of 60 mV/decade, an issue that has been only barely addressed. Subthreshold slope (S) is very important not only to assure excellent pinch-off and low dissipated power in digital applications but also for achieving good power-added efficiency in analog applications. Most crucially, the subthreshold slope can be used to quantify the trap density in the gate-modulated region of AlGaN/GaN HEMTs. The presence of traps in this region degrades gate modulation efficiency, which is closely related to the subthreshold slope and ultimately to high-frequency performance. In this paper, we first demonstrate effects of thermal annealing on the subthreshold slope in AlGaN/GaN HEMTs. Then, based on the temperature dependence of the subthreshold slope, we introduce a new method to estimate interface trap density in these devices.

Figure 1 shows the temperature dependence of S in two different transistors with different initial values of S. Notably, when the initial subthreshold slope is very high (typically in excess of 500 mV/dec, Figure 1b), reproducible results are achieved only after the first heating sequence. From the change of S with temperature (T), the interface trap density in these devices can be extracted. By analogy with MOSFETs, the equation for the subthreshold slope in HEMTs is given by the equation,

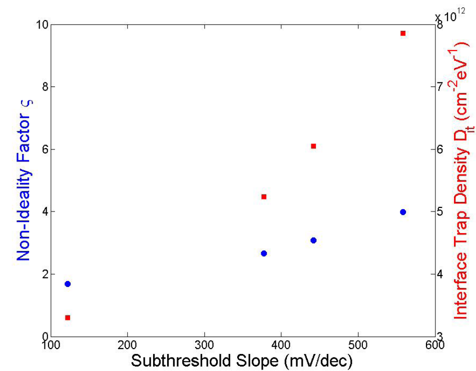
$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_Q + C_{it}}{C_i}\right) = \frac{kT}{q}\ln(10)(1+\varsigma) \rightarrow \frac{k}{q}\ln(10)(1+\varsigma) \quad (1)$$

where C_i is AlGaN layer capacitance, C_Q is quantum capacitance, and C_{it} is associated with the interface trap density. Here, ς is a non-ideality factor related to the interface trap density. The variable ς can be calculated from the equation (1) after measuring the slope from the S vs. T curve. As shown in Figure 2, ς varies between 2 and 4. From the value of ς, we estimated an interface trap density of $3\times10^{12}\sim 8\times10^{12}$ $cm^{-2}eV^{-1}$, assuming C_Q is negligible. This value is similar to previously reported data obtained from low-frequency noise data [1] or from gate-drain conductance and capacitance-dispersion studies [2].

In conclusion, we have studied the change in the subthreshold slope in AlGaN/GaN HEMTs with temperature. Using this experiment, we propose for the first time a relatively simple way to estimate interface trap density. The understanding of this interface trap is critical to optimize the gate-modulation efficiency of these transistors and maximize their high-frequency performance.



▲ Figure 1: Dependence of subthreshold slope on temperature for two different transistors. (a) Transistors with an initial subthreshold slope below 500 mV/dec typically show a very reproducible linear dependence with temperature. (b) However, transistors with higher initial subthreshold slope reach stable operation only after the first heating sequence.



▲ Figure 2: Calculated non-ideality factor and interface trap density. Slight variations of ς might be caused by differences in gate leakage current and its behavior with temperature.

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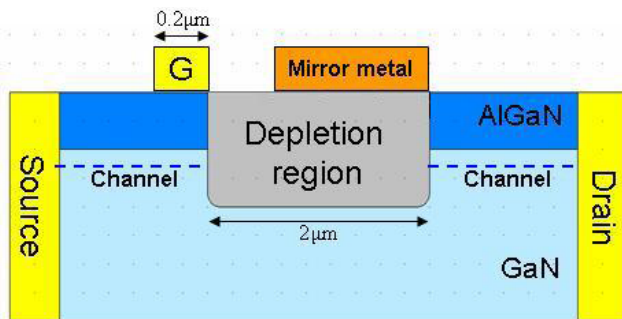
Effect of Image Charges in the Drain Delay of AlGaN/GaN HEMTs

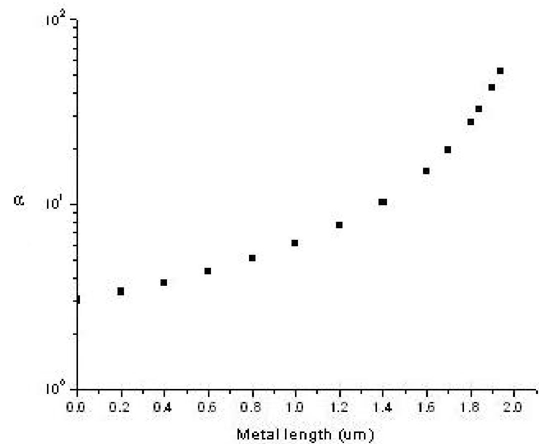
J.W. Chung, X. Zhao, T. Palacios
Sponsorship: ONR, MIT, MTL, KFAS

The electron delay in high electron mobility transistor (HEMT) can be divided into three different components: intrinsic delay, channel delay, and drain delay [1]. Both the intrinsic and channel delays decrease when one scales down the device. However, the drain delay remains constant and ultimately limits the maximum frequency performance of these transistors. From a physical point of view, the drain delay is the time taken by the electrons to cross the depletion region at the drain side of the gate. Mathematically, the drain delay can be expressed as $\tau_{drain} = w_d / (\alpha v_e)$, where w_d is the width of the depletion region, v_e is the electron velocity and α is a constant given by the effect of image charges. The value of α has been extensively studied in heterojunction bipolar transistors. In these devices, α is equal to 2 [2]. However, to the best of our knowledge the value of α has not been studied in field effect transistors. In this paper, we have calculated the value of α in AlGaN/GaN HEMTs. Through simulations, we have found that α represents the ratio of injected charges in the depletion region to image charges in the source side of the channel. In standard HEMTs, α equals 3. We have also found that α can be engineered through the introduction of additional "mirror" metal to the original AlGaN/GaN HEMT structure.

Depending on the location and length of the "mirror" metal, α can vary significantly due to a portion of image charges "imaging" onto the metal. Figure 1 shows the standard AlGaN/GaN HEMT structure with the "mirror" metal. As the length of the "mirror" metal increases, α increases and the drain delay decreases. Figure 2 illustrates α as a function of the length of the "mirror" metal from the right edge of the depletion region. By using these simulations, the transistor can be engineered to have a value of α at least three times higher than in standard devices. This improvement in α significantly reduces the drain delay and increases linearity with drain voltage of these transistors, which make it extremely attractive for future generations of high-speed devices.



▲ Figure 1: Standard AlGaN/GaN HEMT with "mirror" metal. The size of depletion region is exaggerated to emphasize the location where the drain delay occurs. The "mirror" metal is connected to the drain.



▲ Figure 2: The α increases as the length of "mirror" metal on the depletion region increases toward the gate.

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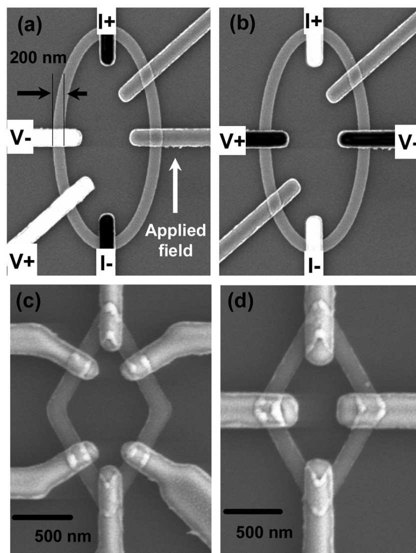
Magnetic Rings for Memory and Logic Devices

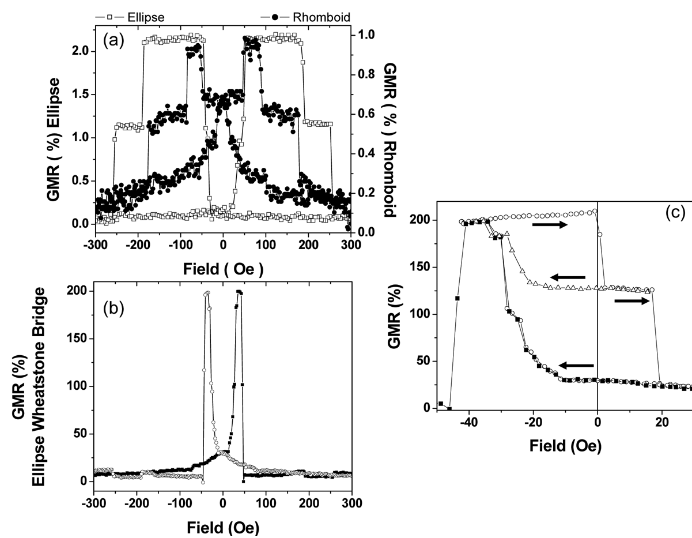
F.J. Castaño, W Jung, I.A. Colin, B. Ng, C.A. Ross
Sponsorship: Cambridge-MIT Institute, Singapore-MIT Alliance, NSF

We are using fabrication processes combining electron-beam lithography and photo-lithography to create magneto-electronic devices based on small ring-shaped multilayered magnetic elements with widths in the deep-sub-micron regime. These small structures have potential uses in magnetic-random-access memories (MRAM), magnetic logic devices, and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multilayered magnets containing two magnetic layers separated by a thin layer of either a non-magnetic metal (spin-valves) or an insulator (magnetic tunneling junctions). The resistance of such elements depends on the relative orientation (parallel or anti-parallel) between the magnetization in the read-out (free) and storage (pinned) layers. When the direction of magnetization of the free layer is switched, two different resistance levels can be detected, allowing storage of a non-volatile bit of data ("0" or "1") in each element. As an alternative bit shape, MRAMs based on ring-shaped multilayered magnets have been recently proposed [1], due to their robust magnetization reversal and the existence of flux-closure or "vortex" states.

We have fabricated devices based on elliptical, circular and rhomboidal rings made from NiFe/Cu/Co/Au pseudo-spin-valves (PSVs) [2-3], Ta/NiFe/Cu/Co/IrMn/Au spin-valves (SVs) and Co/IrMn exchanged-biased structures [4]. The magneto-transport response of PSV and SV rings is dominated by giant-magnetoresistance (GMR) and the ring-shape allows for intermediate resistance levels [2] (see also Figure 2 (a)), resulting from vortex-like magnetic configuration in both the free (NiFe) and hard (Co) or pinned (Co/IrMn) rings. Such intermediate resistance levels are not present in bar-shaped multilayered magnets and can allow storage of more than one bit of data in each cell, as well as increased functionality of logic devices. Most recently, we have found that Wheatstone-bridge contact configurations (Figure 1 (b)&(d)) can result in GMR ratios in excess of 200% (Figure 2 (b)&(c)) for modest applied fields, even though the GMR of the rings in a standard contact configuration (Figure 1 (a)&(c)) is just 1-2% (Figure 2(a)). As the soft rings reverse from both ends, two reverse walls traverse each side of the rings and the bridge becomes unbalanced. We are currently exploring operating these devices using current pulses instead of an external applied field.



▲ Figure 1: Scanning electron micrographs corresponding to elliptical (a)&(b) and rhomboidal (c)&(d) rings devices made from NiFe/Cu/Co/Au PSVs and Ta/Cu non-magnetic contact wires. The long axis of the rings ranged from 930 nm to 4 µm and the widths ranged from 80 nm to 200 nm.



▲ Figure 2: (a) Resistance versus applied field measurements using a standard contact configuration in elliptical and rhomboidal NiFe (6 nm) /Cu (4 nm) /Co (Co 4 or 5 nm) /Au (4 nm) rings, on switching both the free (NiFe) and hard (Co) layers. (b) Resistance versus applied field corresponding to a Wheatstone-bridge contact configuration on a NiFe (6 nm) /Cu (4 nm) /Co (Co 4 nm) /Au (4 nm) elliptical ring (Figure 1(b)), on switching both magnetic layers and (c) on switching back and forth only the soft NiFe ring.

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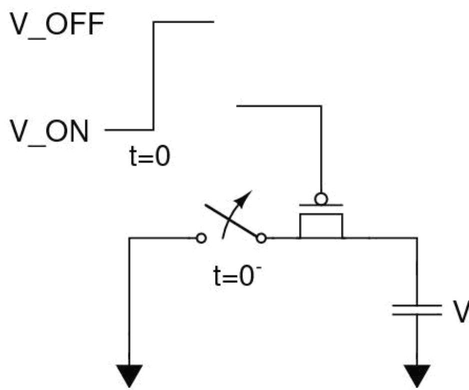
Characterization of Organic Field-effect Transistors for Circuit Applications

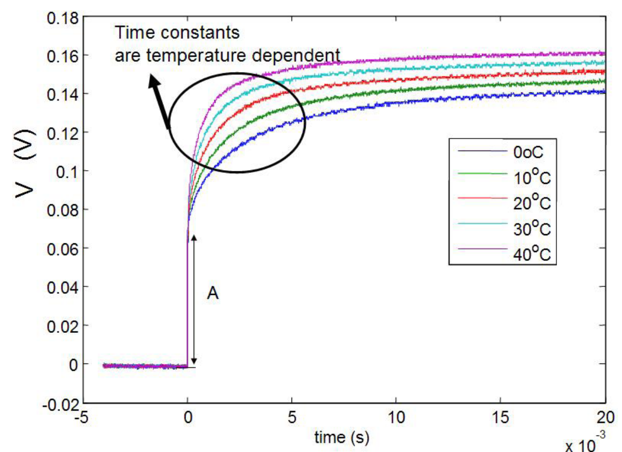
K. Ryu, D. He, I. Nausieda, V. Bulović, A.I Akinwande, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

It has been demonstrated that organic materials have semiconducting properties with mobility comparable to that of amorphous silicon (a-Si), the dominant material used in display applications. Organic field-effect transistors (OFETs) provide an exciting possibility of flexible large-area plastic electronics. Organic materials can also be deposited using a solution-based method enabling "printing" circuits. A roll-to-roll method can be used for mass production, and inkjet can be used for customized small-volume applications. One crucial area that needs to be researched is how the different charge transport mechanisms and material sets in organic transistors change the design considerations in circuit applications compared to the traditional silicon MOSFETs.

This project aims to characterize and model OFET behavior for various circuit applications. Thus far, the nonlinear contact resistance, threshold voltage, and mobility are extracted from top-contact and bottom-contact transistors with current-voltage (I-V), and capacitance-voltage (C-V) measurements. Extraction of contact resistance is found to be important in characterization of bottom-contact transistors as it obscures mobility extraction. The mobility extracted after removing the effect of contact-resistance is shown to increase with the gate field, unlike that in crystalline silicon MOSFETs [1]. The mobility dependence on gate voltage leads to an interesting study of how the channel charge comes out of the channel as an OFET turns off. When a transistor is turned off, the charge that forms the channel returns to the source and drain. This effect is called charge injection and changes the final voltage on a capacitance load. When the transistor is off, the low mobility in the OFET slows charge injection significantly. To study how mobility and trapping affects charge injection, the transient response of an OFET switch is measured as a function of temperature. Figure 1 shows the setup used to make charge injections measurements. The source and drain are grounded with the transistor on until steady-state. The mechanical switch is opened and the voltage on the load capacitor is measured as the transistor is switched off. The measurement in Figure 2 shows the transient voltage measurements on the capacitor with varying temperature. The capacitor voltage rises as the positive charge in the accumulation layer exits to the capacitive load. From the measurement, we hope to fully understand the transport mechanism in the organic semiconductor used.



▲ Figure 1: Schematic of a charge-injection measurement.



▲ Figure 2: A typical charge injection measurement from a 1000/25 µm OFET.

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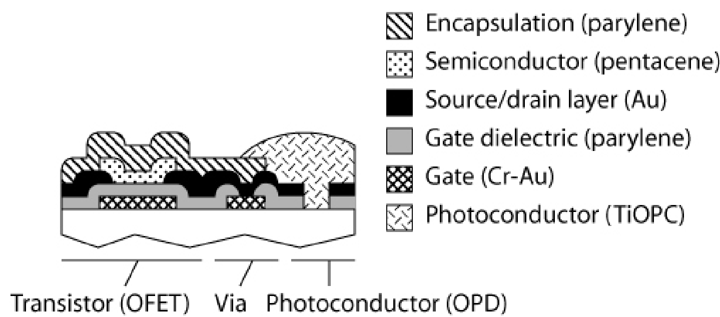
Integrated Organic Circuits and Technology for Large Area Optoelectronic Applications

I. Nausieda, K. Ryu, D. He, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

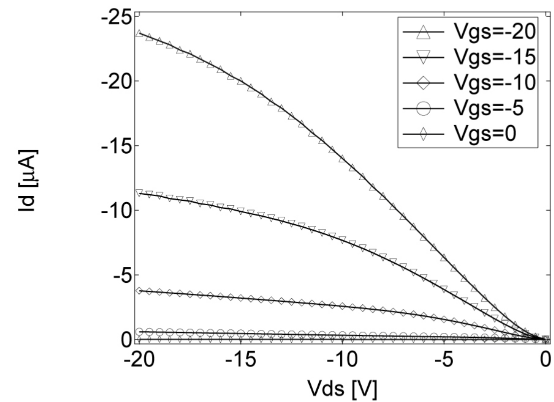
Organic semiconductors can be deposited at near-room temperatures, enabling the creation of electronic and optoelectronic devices on virtually any substrate. This unique technology makes possible the fabrication of large-area, mechanically flexible optoelectronics, such as conformable displays or image sensors. To realize these systems, an integrated approach to fabrication of organic optoelectronics is necessary.

A near-room temperature (<95°C), scalable process has been developed, using conventional photolithography and inkjet printing [1]. This process produces integrated organic field effect transistors (OFETs) and organic photoconductors (OPDs) on a single substrate. A cross section of the finished substrate is shown in Figure 1.

Typical device characteristics for an integrated OFET are shown in Figure 2. As a proof of concept, a 4x4 active-matrix imager was created using the process and was demonstrated to correctly image patterns [2].



▲ Figure 1: Schematic cross section of finished substrate illustrating OFET, OPD, and two interconnect layers.



▲ Figure 2: Typical output characteristics for a 1000µm / 4µm OFET.

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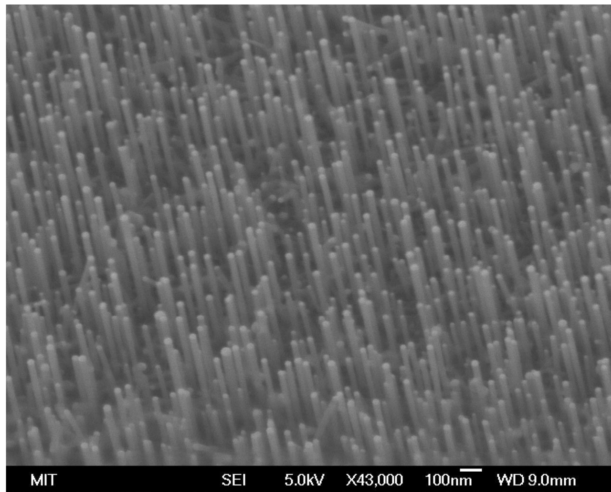
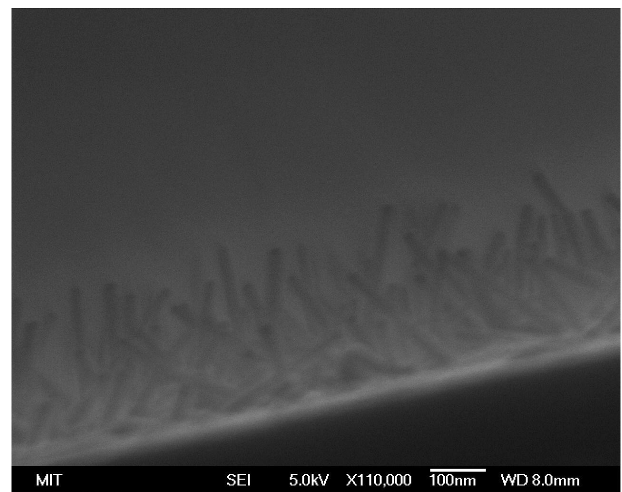
Catalyst Engineering and Growth Mechanisms of Si and III-V Nanowires

S.T. Boles, O.M. Nayfeh, D.A. Antoniadis, E.A. Fitzgerald, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

The vapor-liquid-solid mechanism for growth of single crystal whiskers and wires was originally discovered in the 1960s, but it has only recently been rediscovered as a way to fabricate high performance nanoscale electronic devices below the limits of photolithography. Although a great deal of attention has been focused on the electronic properties of Si and III-V nanowires, many of the physical mechanisms involved in growing these single crystal wires remain unclear. We have been investigating the importance of catalyst size and shape in growth morphology by using evaporated island catalysts, catalysts derived from dewetted thin films, and commercially available nanoparticles. Also in this study, the role of growth conditions has been examined by controlling temperature, partial pressures of reactants and pre-growth annealing. These parameters have been determined to be critical to stable and repeatable growth of Si and III-V nanowires.



▲ Figure 1: Si nanowires grown on Si <111> substrates.



▲ Figure 2: GaP nanowires grown on Si <111> substrates.

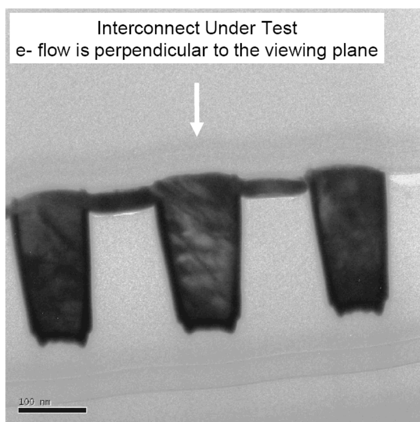
Effects of the Mechanical Properties on the Reliability of Cu/low-*k* Metallization Systems

F.L. Wei, Z.S. Choi, T. Chookajorn, C.L. Gan, C. Hau-Riege, C.V. Thompson
Sponsorship: SRC

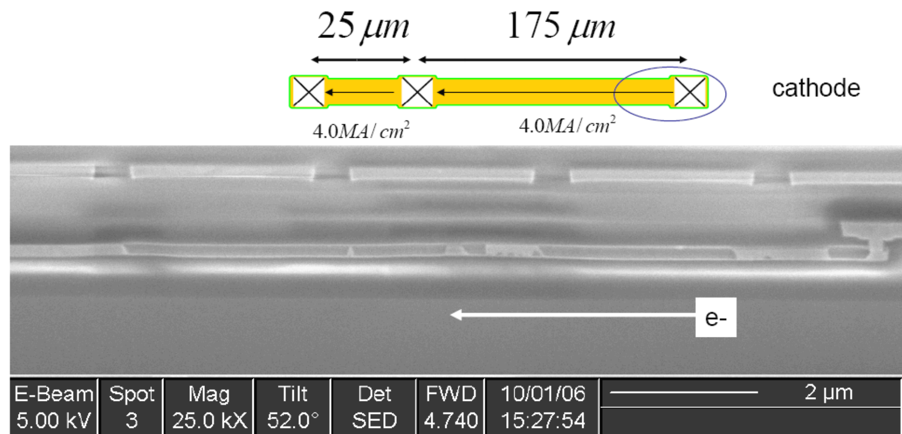
Electromigration, current-induced atomic diffusion due to momentum transfer from conducting electrons, is and will remain a major reliability concern for interconnects in integrated circuits (ICs), as future technologies demand increasing packing efficiencies and current densities. The Cu and low dielectric constant (*k*) inter-level dielectric (ILD) metallization scheme is the preferred choice for high-performance ICs. However, low elastic moduli, a characteristic of the low-*k* ILDs, and decreasing diffusion barrier thicknesses, lead to significant degradation of reliability. In order to analyze the mechanical responses and assess the failure criteria for electromigration in Cu/low-*k* interconnects, we have carried out a comprehensive investigation involving both thin-film characterizations on the constituent materials and electromigration experiments on fully processed interconnect structures manufactured by AMD Inc. and International Sematech Inc.

As Cu atoms electromigrate from the cathode to the anode inside nodes of interconnect segments, an atomic concentration change is related to a change in stress through the effective bulk modulus of the materials system, *B*. This property is central in considerations of electromigration-induced failures by void nucleation and growth, as well as Cu extrusions. The value of *B* is computed using finite element modeling (FEM) analyses using experimentally determined mechanical properties of the individual constituents. Such characterization techniques include nanoindentation, cantilever deflection, pressured membrane deflection for film elastic properties measurements, and Chevron-notched double-cantilever pull structures for adhesion measurements.

We have also carried out electromigration experiments on fully processed interconnect tree structures. We found that, under most test conditions, the conventional "10% initial resistance increase" failures are due to void growth. Such growth rates, i.e., the rate of failure for a structure, highly depend on two factors: (1) the stress conditions of neighboring interconnect segments that function as atomic sinks or reservoirs (if any is present) and (2) *B*. The higher the *B* value, the more back-stress force would be generated to counteract void growth. We also observed, over a long duration of experiments, extremely long voids and Cu extrusion formations (see Figures 1a and 1b). Studies on the threshold for Cu extrusions are being conducted.



(a)



(b)

▲ Figure 1: (a) Observation of Cu extrusions near the anode end: decohesion between the side-wall diffusion barrier and the capping layer leads to a thin layer of Cu being extruded out along the capping layer/ILD interface; (b) observation of an extremely long void near the cathode end of a Cu/low-k test segment: a void >10mm long in a 200mm-long interconnect is shown.

Bonded Copper Interconnects and Integrated Microchannels for 3D Integrated Circuits

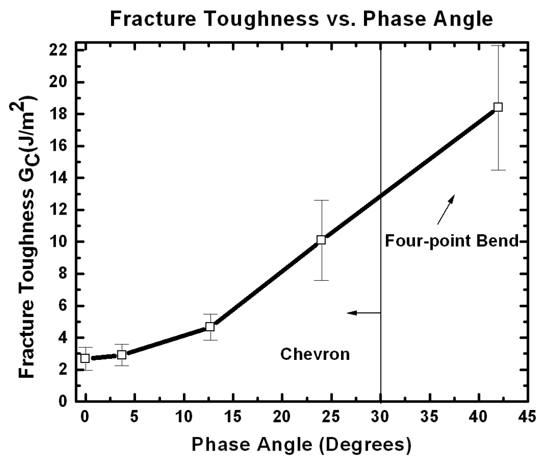
R. Tadepalli, H.L. Leong, C.L. Gan, K.L. Pey, D.E. Troxel, K. Turner, C.V. Thompson
Sponsorship: DARPA (3D Integrated Circuits), Singapore-MIT Alliance, IME

Performance of thermocompression Cu-Cu bonds is critical to reliability of devices created by stacking of individual wafers. Thermal effects in such 3D circuits are expected to be severe compared to conventional devices, owing to multiple heat-generation locations and limited heat-dissipation pathways. Bond quality and thermal performance issues in Cu wafer-bonding technology are investigated using both experiments and modeling.

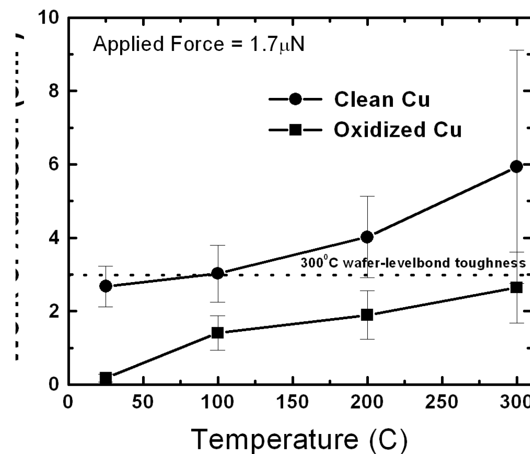
A novel test method (the Chevron test) has been developed to complement the conventional four-point bend test for bond toughness measurements. The Chevron test is used to measure Mode I (Tensile) toughness of Cu bonds (Figure 1). Nominal toughness values for Cu bonds created at 300˚C as measured by Chevron and Four-point bend tests are 2.5 J/m^2 and 17J/m^2, respectively, the difference attributed to plastic deformation of the Cu stack [1]. Therefore, the Chevron test gives a measure of the true interface strength, minus external contributions. We have also used the Chevron test technique to measure bond toughness under a variety of load conditions (mode mixities with phase angles from 0 to about 35^0), by varying the ratios of the thickness of the two substrates (Figure 1).

Effects of process and film parameters on ultimate bond quality are being analyzed using bonded ECP damascene-patterned Cu interconnects (NTU, Singapore). Results indicate a strong dependence of bonded die yield on Cu film roughness and applied bonding load. An analytical model is being developed to explain these findings.

The fundamental limit of Cu adhesion is probed using a UHV-AFM/deposition system. Force of adhesion between pristine oxide-free Cu surfaces deposited on a cantilever tip and a substrate is measured under UHV conditions. The room-temperature bond strength measured in the AFM set-up is comparable to the 300^0 C wafer-level bond strength, thereby showing a significant dependence of bond quality on Cu surface cleanliness. We find that exposure to 1 x 10^{-6} Torr oxygen is sufficient to prevent formation of strong bonds at or near room temperature.



▲ Figure 1: Use of asymmetric chevron test structures allows bond toughness measurements in a range of loading conditions



▲ Figure 2: The Cu-Cu bonds made under UHV conditions at room temperature have the same strength as bonds that require 300^{0}C in conventional bonding systems. Exposure to 1 x 10^{-6} Torr leads to behavior seen in conventional bonding.

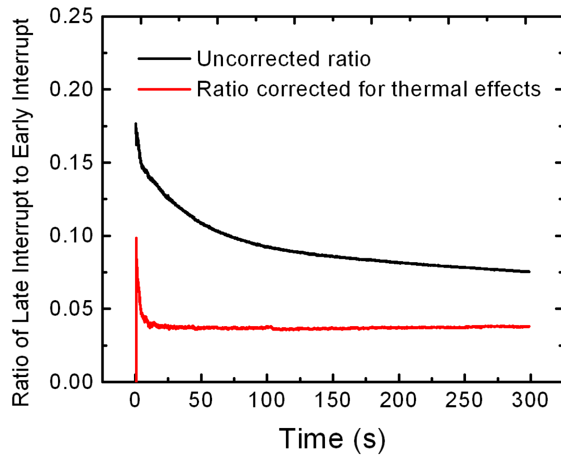
Co-evolution of Stress and Structure During Volmer-Weber Growth of Thin Films

J. Leib, A.R. Takahashi, C.V.Thompson
Sponsorship: NSF

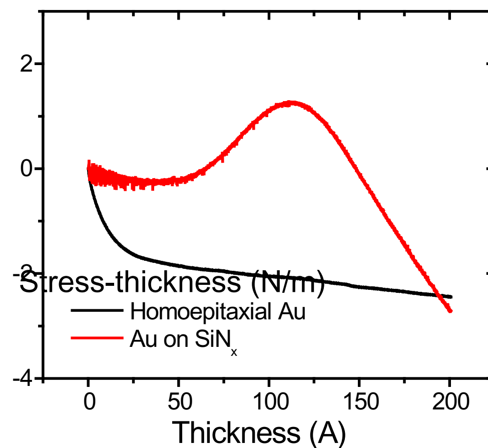
Most metallic films used in electronic and microelectromechanical devices and systems are polycrystalline and therefore form through the Volmer-Weber mechanism, in which each grain nucleates as an isolated single crystal island that coalesces with other islands to form a film. This process of film formation can lead to compressive or tensile residual stresses as well as to stress gradients that can affect both performance and reliability in microsystems.

We are using cantilever devices to measure evolution of the thin film stress-thickness product during Volmer-Weber formation and growth of polycrystalline and epitaxial films. The island coalescence process leads to tensile stresses that may or may not be retained as the coalesced film thickens. In high atomic mobility materials (such as Cu, Au, Ag, and Al) deposited at room temperature, not only does the tensile stress reduce as the film thickens, but the film can evolve into a net compressive state. During interruptions of growth, some of the compressive stress relaxes. However, this happens reversibly in that the stress returns to its previous value when deposition is resumed. This phenomenon has been particularly difficult to understand, especially given an apparent film-thickness dependence. Our recent experiments have identified two components of this reversible stress change, one of which is associated with thermal effects. These components can be separated as illustrated in Figure 1, showing that the remaining component is not dependent on the film thickness.

To further understand the origins of both the non-thermal component of the reversible compressive stress and the residual compressive stress, we are comparing evolution of polycrystalline and homoepitaxial films. Stress-thickness curves for gold grown at 1 Å/s on both silicon nitride and homoepitaxially on Au are shown in Figure 2. Both systems have strong <111> texture out of the film plane, but while the grains in the polycrystalline have random in-plane orientations, heteroepitaxial films grown on <111>Au substrates have only two in-plane variants (corresponding to fcc and hcp stacking relative to an fcc underlayer). The stress associated with coalescence is not seen in the homoepitaxial film, but a compressive stress is observed in both types of films. We are currently investigating the origins of both the similarities and differences in this compressive behavior in these two types of films.



▲ Figure 1: Ratio of the stress vs. time for a growth interruption performed at 2000 Å thickness to one performed at 400 Å thickness. When reversible thermal stresses are removed, all interrupts become similar.

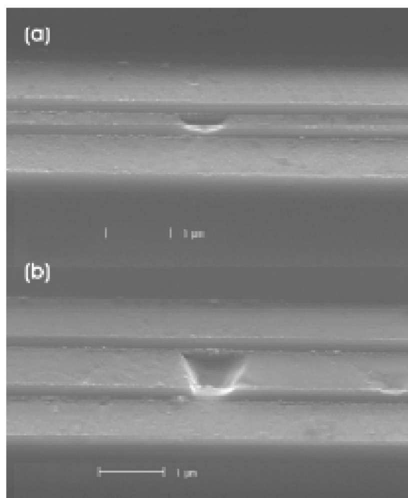


▲ Figure 2: Comparison of stress-thickness curves for gold films grown at 1 Å/s on epitaxial (111) Au layers and on silicon nitride.

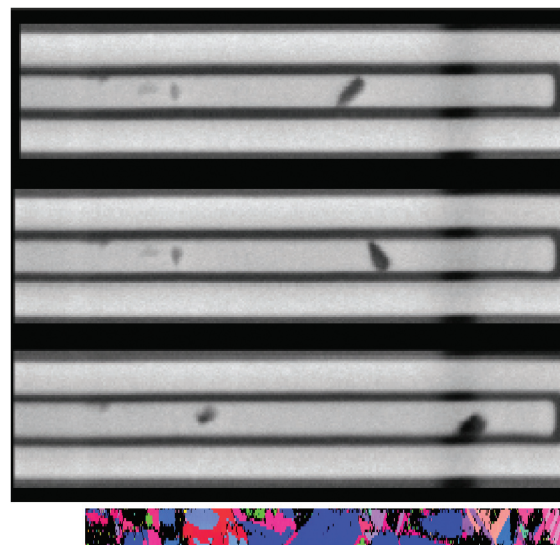
Surface Electromigration and Void Dynamics in Copper Interconnects

Z.S. Choi, T. Chookajorn, C.V. Thompson
Sponsorship: Intel Corporation, AMD, SRC

Electromigration is one of the main causes of failures in interconnects. It has been shown that the dominant diffusion path in copper interconnect technology is the interface between the dielectric passivation layer and the copper line. This interface is also the most prone to void nucleation and growth. We have carried out two types of experiments to investigate the details of void dynamics during electromigration. The first type of experiment is performed on interconnects without passivation layers to determine the dependence of copper surface diffusion and electromigration on different grain orientations. The samples are heated in reducing gas to remove copper oxide and then tested in a vacuum (<10^{-7}torr). The voids in these samples nucleate and grow at flux divergence sites (Figure 1). The flux divergences occur due to the differences in diffusivity for different grain orientations. After the electromigration tests, we obtain the crystallographic orientations of the grains surrounding the voids using electron backscattered diffraction (EBSD) in an SEM and correlate the results with differences in diffusivities between different grains. In a second type of experiment, we take a fully fabricated sample and thin the passivation layer using a focused ion beam microscope (FIB), in order to observe the underlying metal line in an SEM while still retaining sufficient passivation layer to constrain electromigration in the same way that it is constrained in service. We then test the samples at elevated temperatures in the SEM and observe the voids in the interconnects through the thinned passivation layer in real time, as Figure 2 shows. Voids are seen to originate at locations other than just the cathode end of the interconnect. These voids can grow in place or grow until they de-pin from their growth site and drift toward the cathode. The dependence of atomic diffusivity on crystallographic directions and textures causes changes in size, shape, and drift velocity of voids as they pass through different grains. After the test, we remove the passivation layer and use EBSD analysis to determine the effects of grain orientation on void kinetics. We are correlating these experimental observations with simulations of electromigration both to better understand this complex behavior and to better account for it in reliability assessment methods.



▲ Figure 1: Voids in interconnects with no dielectric passivation layer, interconnects with length of1000 µm, depth of 0.45 µm, widths of a) 0.3 µm and b) 1.0 µm.



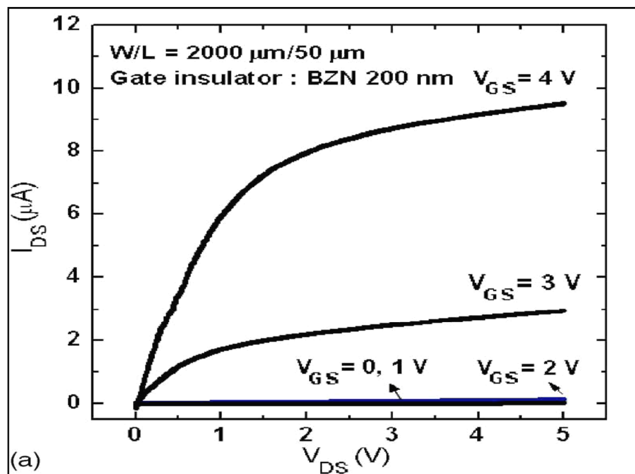
▲ Figure 2: *In situ* SEM images of the cathode of a test structure, showing void drift toward cathode end. The test line is surrounded by a Cu-extrusion monitor. Bottom image is a texture mapping by EBSD obtained after EM test. National Science Foundation.

Thin Film Transistors for Flexible Electronics and Displays

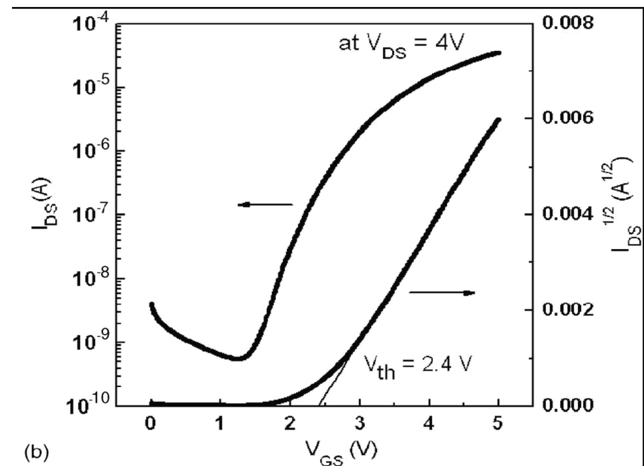
I.D. Kim, Y.S. Jin, H.L. Tuller (in coll. with Y.W. Choi, A.I. Akinwande)
Sponsorship: NSF

Organic thin film transistors (OTFT) are receiving much attention, given their potential for structural flexibility, large-area coverage, low temperature processing and low cost compared to current technology. A key limitation has been the low K of the dielectric layer and thereby high operating voltages. For example, we demonstrated the ability to RT sputter-deposit $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN) onto polymers with a K value as high as ~50, thereby enabling operation at voltages as low as 4V [1].

Transistors based on ZnO are being investigated as a possible alternative for the hydrogenated amorphous silicon or poly-silicon TFT that are employed as the backplane of liquid crystal and related displays. In addition to its transparency, ZnO has an uncommonly high mobility (up to 100 cm^2/Vs) for an oxide semiconductor. By complementing ZnO channels with high K dielectric layers, we have obtained TFTs with low operating voltage (Figure 1) and high on/off current ratios and mobilities (Figure 2) [2-3].



▲ Figure 1: Drain Current I_{DS} as a function of Drain Voltage V_{DS} depending on gate voltage V_{GS}. Note that operating voltage for the ZnO transistor is lower than 4V.



▲ Figure 2: Drain Current I_{DS} as a function of gate voltage V_{GS}. Note that threshold voltage from saturation region is 2.4 V. On/Off current ratio is ~ 10^4. Mobility of the ZnO transistor is 1.13cm^2/Vs.

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