MTL

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massachusetts institute of technology

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September 2007

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INTRODUCTION

Anantha P. Chandrakasan
Director, MTL

Welcome to the 2007 MTL Annual Report. This report summarizes the research from faculty and senior research staff associated with the MTL. The report covers diverse research areas related to electronic device fabrication, integrated circuits and systems, photonics, micro-electromechanical systems (MEMS), as well as molecular and nano-technologies. These investigators come from more than 38 different departments, labs, and centers across the Institute.

The MIT Microsystems Technology Laboratories (MTL) is an interdepartmental laboratory with a mission to foster research and education in semiconductor process and device technology, and integrated circuits and systems design. MTL provides micro- and nano-fabrication and computer aided design (CAD) infrastructure to the entire campus. Last year, more than 500 researchers, primarily graduate students, conducted research using the MTL infrastructure.

MTL's fabrication environment includes three clean rooms: the Class 10 Integrated Circuits Laboratory, the Class 100 Technology Research Laboratory, and the flexible Exploratory Materials Laboratory. The computational environment provides access to advanced electronic design automation (EDA) for device, circuit and system design. The fabrication and computation facilities of MTL are maintained and operated by approximately 20 full-time technical staff members.

MTL partners with industry through the Microsystems Industrial Group (MIG). MTL research and operation is significantly subsidized by the MIG consortium. This year, two new members, NEC and Cadence, have joined the MIG. The members of the Industrial Advisory Board (one member from each of our MIG companies) provide significant guidance in shaping the vision of MTL.

There are significant changes in MTL over the past year. Several new committees have been established for setting strategic directions as well as dealing with operations issues. A new website with significant new content was launched in January of 2007 (www-mtl.mit.edu). The newly formed MTL Seminar Committee has put together an outstanding seminar series open to the public.

The flagship technical event of MTL is our annual research conference (MARC) held annually in Waterville Valley, New Hampshire. The conference is run by MTL graduate students in collaboration with a steering committee. The conference has grown significantly over the past few years and is widely attended by industry, faculty, students and staff. MARC 2007 had more than 200 attendees. We have also initiated an MTL visit day to companies where MTL graduate students present leading-edge results to our MIG companies.

Research conducted at MTL (as organized in the Annual Report) can be broadly classified into five categories: Circuits and Systems, Electronic Devices, MEMS and BioMEMS, Molecular and Nanotechnology and Photonics. MTL has four affiliated industrial research centers with more focused interests: the Center for Integrated Circuits and Systems (CICS), Intelligent Transportation Research Center (ITRC), MEMS@MIT, and the Center for Integrated Photonic Systems (CIPS).

ACKNOWLEDGEMENTS

We are grateful to the following organizations for their generosity and participation in the Microsystems Industrial Group (MIG). Their membership makes possible the continuing operations of the Microsystems Technology Laboratories:

- Analog Devices
- Applied Materials
- Cadence, Inc.
- Hewlett-Packard
- IBM Corporation
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- National Semiconductor
- NEC Corporation
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We would also like to acknowledge past support of the Microsystems Technology Laboratories by the following organizations:

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We also wish to acknowledge the support of those organizations who have generously contributed equipment for use at the Microsystems Technology Laboratories:

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Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
A.I. Akinwande	Display devices: flexible large area electronics, organic and inorganic thin film transistors, field emission displays; high aspect ratio gated microstructure arrays: field emission devices, electrospray thrusters and gas analyzers.	39-553b	617-258-7974	akinwand@mtl.mit.edu
D.A. Antoniadis	Fabrication, measurements and modeling of silicon- and germanium-based devices for high-speed and low-power integrated circuits.	39-427b	617-253-4693	daa@mtl.mit.edu
M.A. Baldo	Molecular electronics, integration of biological materials and conventional electronics, electrical and exciton transport in organic materials, energy transfer, metal-organic contacts, nanomechanical transistors.	13-3053	617-452-5132	baldo@mit.edu
K.K. Berggren	Superconductive nanodevice physics and applications; nanofabrication methods, processes, and tool-development for application to superconductive quantum computing and single-photon detection.	36-219	617-324-0272	berggren@mit.edu
S.N. Bhatia	Micro- and nano-technologies for tissue repair and regeneration. Applications in liver tissue engineering, cell-based BioMEMS, and nanobiotechnology.	E19-502d	617-324-0221	sbhatia@mit.edu
D.S. Boning	Characterization and modeling of variation in semiconductor and MEMS manufacturing with emphasis on chemical mechanical polishing (CMP), electroplating, plasma etch, and advanced interconnect processes. Understanding the impact of process and device variation on circuit performance, and design for manufacturability.	38-435	617-253-0931	boning@mtl.mit.edu
V.M. Bove, Jr.	Sensing, display, user interface, and computation for consumer electronics applications, particularly self-organizing ecosystems of devices. Advanced data representations for multimedia.	E15-368B	617-253-0334	vmb@media.mit.edu
V. Bulović	Physical properties of organic and organic/inorganic nanocrystal composite thin films and structures; development of nanostructured electronic and optoelectronic devices.	13-3138	617-253-7012	bulovic@mit.edu
A.P. Chandrakasan	Design of digital integrated circuits and systems. Energy efficient implementation of signal processing and communication systems. Circuit design with emerging technologies.	38-107	617-258-7619	anantha@mtl.mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
G. Chen	Heat transfer and energy conversion at micro- and nanometer scales, such as thermoelectrics, and thermophotovoltaics and photovoltaics; hydrogen storage; development of thermally conductive polymers and liquids; nanoscale fluid flow.	3-260	617-253-0006	gchen2@mit.edu
M.J. Cima	Forming methods for complex macro and micro devices, using three dimensional printing. Development of chemically-derived epitaxial oxide films for HTSC coated conductors. Implantable devices for drug delivery and biomedical applications. Devices and processes for high throughput combinatorial screening of complex materials formulations.	12-011	617-253-6877	mjcima@mit.edu
M.L. Culpepper	Macro, micro and nano-scale machines for precision positioning, assembly and manipulation. Basic and applied research on physical principles, modeling approaches, synthesis/simulation tools, design methods and manufacturing practices. Design and manufacture of multi-scale, multi-physics mechanical systems. Hands-on education applied to the mechanical design of micro and nano-scale devices.	35-209	617-452-2395	culpepper@mit.edu
L. Daniel	Parameterized model order reduction of linear and nonlinear dynamical systems; mixed-signal, RF and mm-wave circuit design and robust optimization; power electronics, MEMs design and fabrication; parasitic extraction and accelerated integral equation solvers.	36-849	617-253-2631	luca@mit.edu
J.L. Dawson	Analog system theory and its applications. RF transceivers, power amplifier linearization, high-speed data conversion, problems in nonlinear control.	39-527a	617-324-5281	jldawson@mtl.mit.edu
J.A. del Alamo	Microelectronics device technologies for gigahertz and gigabit-per-second communication systems: physics, modeling, technology and design. InGaAs as a post-CMOS semiconductor logic technology. Technology and pedagogy of online laboratories for engineering education.	39-567a	617-253-4764	alamo@mit.edu
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C.G. Fonstad, Jr.	Compound semiconductor heterostructure devices and physics. Optoelectronics: laser diodes, photodiodes, quantum effect devices, and OEICs. Monolithic heterogeneous integration. Microscale thermophotovoltaics.	13-3050	617-253-4634	fonstad@mit.edu
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Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
J.L. Hoyt	Epitaxial growth, fabrication and device physics of silicon-based heterostructures and nanostructures. High mobility Si and Ge-channel MOSFETs, and silicon-germanium photodetectors for electronic/photonic integrated circuits.	39-427A	617-452-2873	jlhoyt@mtl.mit.edu
Q. Hu	Physics and applications of millimeter-wave, terahertz, and infrared devices.	36-465	617-253-1573	qhu@mit.edu
K.F. Jensen	Design, fabrication, testing, and integration of microsystems for chemical and biological discovery, synthesis and processing. Microsystems for energy applications, including micro-combustors,-reformers, and thermophotovoltaicsystems. Chemical kinetics and transport phenomena related to processing of materials for biomedical, electronic and optical applications.	66-350	617-253-4589	kfjensen@mit.edu
R.D. Kamm	Fluid mechanics, biomedical fluid mechanics, molecular, cell and tissue biomechanics, respiratory physiology, transport phenomena	NE47-321	617-253-5330	rdkamm@mit.edu
S.-G. Kim	Nanomanufacturing, MEMS assembly en masse, carbon nanotube transplanting assembly. self-cleaning RF MEMS switch, piezoelectric energy harvesting, printable PZT MEMS.	1-310	617-452-2472	sangkim@mit.edu
L.A. Kolodziejski	Research in integrated photonic devices and optoelectronic components. Design and fabrication of photonic crystals and III-V semiconductor devices. Electronic materials growth and characterization.	36-287	617-253-6868	leskolo@mit.edu
J. Kong	Synthesis, characterization and applications of carbon-based nanomaterials (nanotubes and graphene) and inorganic nanowires.	13-3065	617-324-4068	jingkong@mit.edu
J.H. Lang	Analysis, design and control of electromechanical systems with application to traditional electromagnetic actuators, micron-scale actuators and sensors (MEMS), and flexible structures.	10-176	617-253-4687	lang@mit.edu
H.-S. Lee	Analog and mixed-signal integrated circuits with a particular emphasis in data conversion circuits in scaled CMOS.	39-553	617-253-5174	hslee@mtl.mit.edu
C. Livermore	Microelectromechanical systems (MEMS). Design and fabrication of high power microsystems, including electrical generators and MEMS components for lasers. Self-assembly techniques for nano- and micro-scale manufacturing.	3-449C	617-253-6761	livermor@mit.edu
S.R. Manalis	Microdevices for biomolecular and single-cell detection.	E15-422	617-253-5039	scottm@media.mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
I. Masaki	VLSI architecture. Emphasis on interrelationship among applications, systems, algorithms, and chip architectures. Major application fields include intelligent transportation systems, video, and multimedia.	38-107	617-253-8532	imasaki@aol.com
T.P. Orlando	Our focus is on the implementation of the major components of a quantum computer using superconducting circuits. This includes the study of single and coupled qubit behavior, qubit measurement, algorithm implementation, and scalability.	13-3006	617-253-5888	orlando@mit.edu
T. Palacios	Design, fabrication and characterization of novel electronic devices in wide bandgap semiconductors; polarization and bandgap engineering; transistors for sub-mm wave power and digital applications; new ideas for power conversion and generation; interaction of biological systems with semiconductor materials and devices; nanowires and carbon nanotube –based transistors.	39-567B	617-324-2395	tpalacios@mit.edu
J.A. Paradiso	Sensor networks, ubiquitous computing, energy harvesting, power management for sensor networks, passive sensors, human-computer interfaces, localization.	E15-327	617-253-8998	joep@media.mit.edu
D.J. Perreault	Design, manufacturing, and control of power electronics and energy conversion systems,; power generation; rf and analog circuit design. Applications to industrial, commercial, scientific, transportation, and biomedical systems.	10-039	617-258-6038	djperrea@mit.edu
M.H. Perrott	Circuit and architecture design for high speed mixed-signal circuits such as phase-locked loops and A/D converters: circuit topologies, architectural approaches, design methodologies, modeling, simulation techniques. Communication system simulation software and tutorials for engineering education.	38-344b	617-452-2889	perrott@mit.edu
R.J. Ram	Photonic devices for applications in communications, computing, and biological sensing with special emphasis on fiber-to-the-home, InP photonic integration, Silicon photonics and high speed interconnects, microscale bioreactors, and biomanufacturing.	36-491	617-253-4182	rajeev@mit.edu
C.A. Ross	Fabrication, properties and applications of magnetic and magnetooptical films and nanostructures; self assembly, block copolymer lithography.	13-4005	617-258-0223	caross@mit.edu
R. Sarpeshkar	Biomedical systems, circuit modeling of biology, bio-inspired systems.	38-294	617-258-6599	rahuls@mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
M.L. Schattenburg	Advanced lithography, including x-ray, electron-beam, ion-beam, and optical. Nanotechnology and nanofabrication. Precision engineering and nano-accuracy dimensional metrology. Advanced interference lithography technology for high-accuracy patterning of general grating and grid patterns. Micro and nanometer fabrication technology applied to advanced astronomical and laboratory instrumentation. Silicon micromachined structures applied to high-precision optical assembly. X-ray optics and instrumentation.	37-487	617-253-3180	marks@space.mit.edu
M.A. Schmidt	Micromechanical systems (MEMS). Microfabrication technologies for integrated circuits, sensors, and actuators; design of micromechanical sensor and actuator systems; mechanical properties of microelectronic materials with emphasis on silicon wafer bonding technology; integrated microsensors, and microfluidic devices. Novel applications of MEMS and nanotechnologies to a variety of fields, including miniature gas turbines, miniature chemical reactors, miniature gas analyzers, microswitches, biological applications, and sensors monolithically integrated with electronics.	39-521	617-253-7817	schmidt@mtl.mit.edu
Y. Shao-Horn	Fundamental science and engineering of materials used in electrochemical conversion and storage systems such as fuel cells and batteries to provide high efficiency and low environmental impact energy sources. Characterizing and design of electronic, crystal and surface structures of materials for lithium storage and electrocatalysis of small molecules of energy consequence.	3-158	617-253-2259	shaohorn@mit.edu
A.H. Slocum	Precision machines and mechanisms from macro to nanoscale.	3-445	617-253-0012	slocum@mit.edu
H.I. Smith	Co-director, NanoStructures Lab. Development of nanofabrication tools and techniques aimed at reaching molecular dimensions and sub-1nm positional accuracy; nanophotonics; templated self assembly.	36-225	617-253-6865	hismith@mit.edu
C.G. Sodini	Design of technology-intensive Microsystems, emphasizing integrated circuit design at the device level, including organic integrated circuits, high data rate wireless LANs, and mm-wave imaging systems.	39-527b	617-253-4938	sodini@mit.edu
F.R. Stellacci	Study and use of large supramolecular assemblies of molecules, with particular interest in situations where these assemblies can develop collective properties that are uniquely determined by their structure and molecular functions.	13-4053	617-324-2500	frstella@mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
V. Stojanović	On-chip interconnects and high-speed off-chip interfaces (electrical, photonic). Modeling and analysis of noise and dynamics in circuits and systems. Application of optimization techniques to digital communications, analog and digital circuits. Digital communications and signal-processing architectures, clock generation and distribution, high-speed digital circuit design, VLSI and mixed-signal IC design.	38-260	617-324-4913	vlada@mit.edu
C.V Thompson	Processing and property optimization for thin films and nanostructures for applications in electronic and electromechanical integrated device systems. Advanced, reliable integrated circuit interconnects.	13-5069	617-253-7652	cthomp@mit.edu
H.L. Tuller	Resonant and chemoresistive sensors, micro-fuel cells, high K dielectrics, electro-optic and piezoelectric thin films, solid state ionics, thin film transistors, MEMS structures and devices.	13-3126	617-253-6890	tuller@mit.edu
J. Voldman	Microtechnology for basic and applied cell biology; Microfluidic perfusion culture, patterning, and manipulation of stem cells. Electrostatics at the microscale, especially dielectrophoresis.	36-824	617-253-2094	voldman@mit.edu
B.L. Wardle	Nano-engineered composites, MEMS Power devices and energy harvesting, advanced composite materials and systems, structural health monitoring (SHM), fracture, fatigue and damage mechanics, durability modeling/ testing, finite-element modeling, structural response and testing, buckling mechanics, project design and management, business strategy and growth, cost modeling.	33-314	617-252-1539	wardle@mit.edu

Section 1

CIRCUITS & SYSTEMS

Test Structures and Optimization Methodologies for Electrical Variation in IC Manufacturing

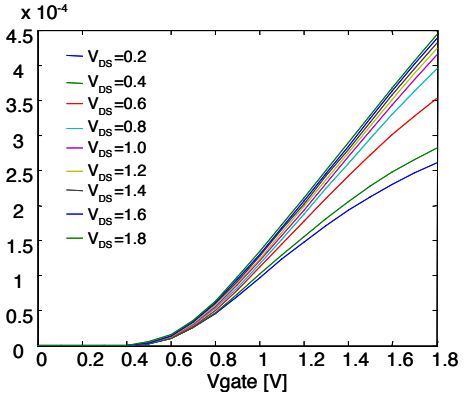
K. Balakrishnan, N. Drego, K. Gettings, D. Lim, D.S. Boning
Sponsorship: SRC/FCRP C2S2, SRC/FCRP IFC, Samsung Electronics, IBM Faculty Fellowship

Modern circuit design needs efficient methods to characterize and model circuit variation in order to obtain high-yielding chips. Circuit and mask designers need accurate guidelines to prevent failures due to layout-induced variations. We address this need by contributing methodologies and new test structures to characterize the variations at device, interconnect, and system levels. Our recent work examines the sources of variation that affect the contact and via resistances associated with integrated MOSFET devices. Due to slight variations in the placement of these metal contacts due to lithographic uncertainties as well as the impacts of strain-induced regions, the uniformity of nominally identical contacts on a die may be lessened. Early results of simulations performed in MEDICI demonstrate the effects of geometric perturbations on the current flow through the contact.

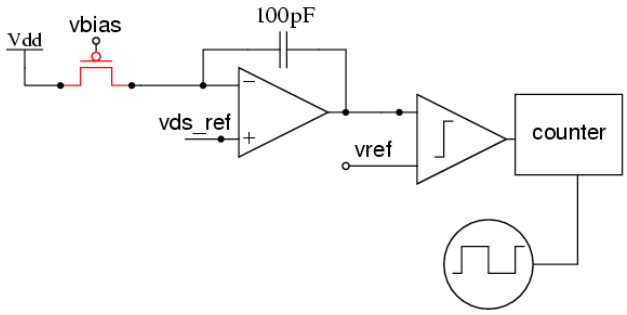
In order to address both device and interconnect variations, we introduce another methodology that uses a large number of test structures, such as MOSFETs and Charge-Based Capacitance Measurement (CBCM), to model variations in threshold voltage and leakage current, among others, based on the architecture proposed by Lefferts [1]. We designed, implemented and measured test circuits that include a large number of high-performance devices (devices under test or DUTs) controlled by low leakage switches and sensors to ensure a nominal value at the DUT terminals, as shown in Figure 1. With this methodology we gather the statistics necessary to identify and model these variations and prevent them from contributing to performance failure.

In addition, we also study an efficient method to characterize the variation in circuit parameters and optimize a circuit based on the variation model. While a direct measurement of physical circuit parameters, e.g., threshold voltage and parasitic capacitance, is costly, the measurement of electrical outputs such as drain currents and oscillation frequencies can be conducted in efficient ways. Combined with a response sensitivity model (RSM) evaluated from a circuit simulator such as SPICE, the statistical properties of the circuit parameter variation with correlation can be estimated from the measured electrical observables. This scheme has been tested using a frequency divider that generates self-oscillation frequencies at multiple bias conditions. The knowledge about the uncertainty of process and circuit parameters can be applied to a robust circuit-optimization framework developed based on convex optimization theory [2].

Lastly, a test-structure consisting of a DUT array containing ~140K DUTs to study threshold voltage (V_T) variation has been designed and submitted for fabrication. Due to the exponential dependence of drain current on V_T in the sub-threshold regime of operation, V_T variation can be effectively isolated from other variation sources (Figure 2). A hierarchical, memory-like access scheme and analog-to-digital converter enable efficient data collection with minimal post-processing required to compute the actual DUT V_T. The large number of DUTs in a dense array allows determination of spatial correlation with high statistical significance. Additionally, a design consisting of completely digital logic paths is currently being formulated to study spatial correlation at the digital circuit level rather than solely at the device parameter level. These measurements will then be used to study architectural ideas to mitigate the impact of variation.



▲ Figure 1: Full I_{DS} vs. V_{GS} curves for a transistor that is part of a large array, and with dynamically controlled and monitored terminals.



▲ Figure 2: Test structure to extract V_T variation by measuring drain current in the sub-threshold regime.

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[2] Y. Xu, L. Pileggi, and S. Boyd, "ORACLE: Optimization with recourse of analog circuits including layout extraction," in *Proc. of IEEE Design Automation Conference*, San Diego, CA, June 2004, pp. 151-154.

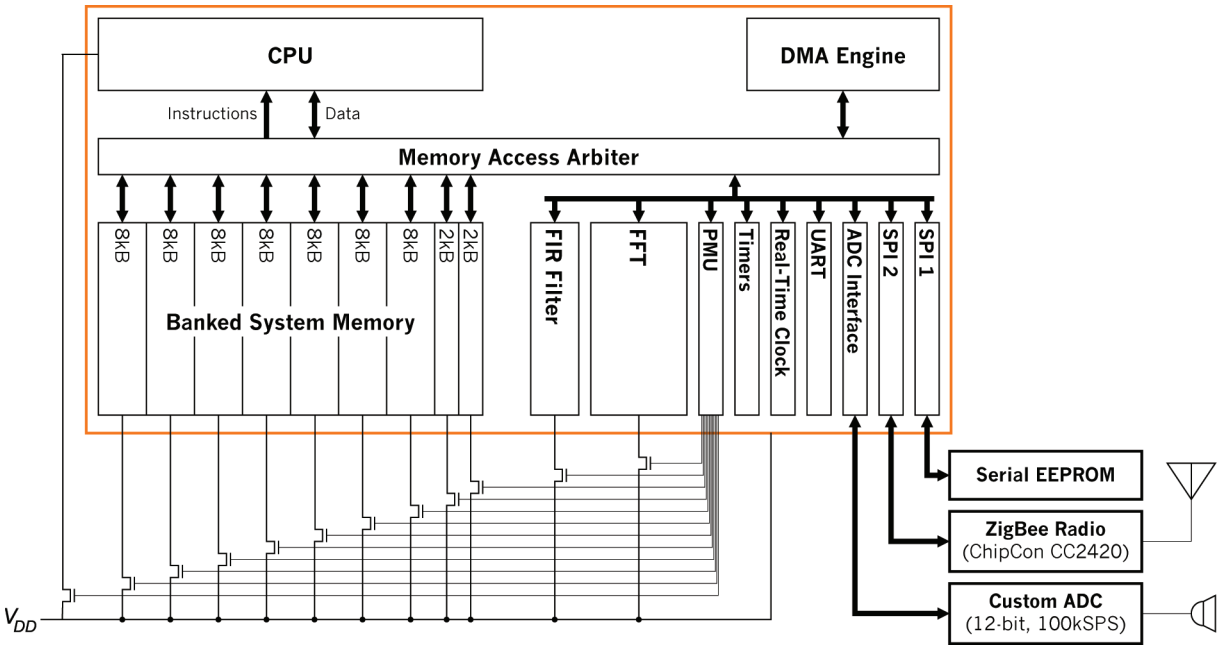
A Micropower DSP Architecture for Self-powered Microsensor Applications

N. Ickes, A.P. Chandrakasan
Sponsorship: DARPA, Texas Instruments

Distributed microsensor networks consist of hundreds or thousands of miniature sensor nodes. Each node individually monitors the environment and collects data as directed by the user, and the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. However, the small size and highly distributed arrangement of the individual sensor nodes make aggressive power management a necessity.

The aim of our project is to develop a micropower DSP platform optimized for medium bandwidth microsensor applications, such as acoustic sensing and tracking. These applications require significant signal processing capability at each node within a sensor network, while maintaining a roughly 100μW average power consumption to enable self-powered (energy scavenging) operation. As illustrated in Figure 1, our DSP includes a general-purpose processor core with an energy efficient instruction set, as well as coprocessors for accelerating Fourier transforms and FIR filtering. Power consumption in the large (62kB) on-chip memory is reduced by dividing the memory into banks (to reduce access energy) and by power-gating inactive banks (to reduce leakage energy). The CPU, FIR, and FFT cores are also power-gated. The DSP was fabricated in 90-nm CMOS by ST Microelectronics.

As part of ongoing work to develop a lightweight, power-aware operating system, the power-gating mechanisms have been characterized with respect to wakeup and energy break-even times. This information is being used to develop scheduling and memory management mechanisms that efficiently utilize power gating. The goal is to automate the details of power management behind standard programming interfaces, exposing only clear and easy-to-use controls.



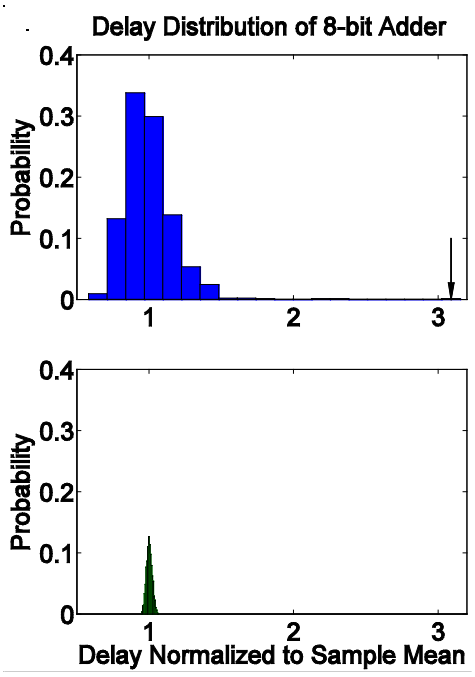
▲ Figure 1: DSP architecture, illustrating the twelve independent power domains, controlled by off-chip power switches. When combined with an external nonvolatile memory (for program storage), radio, and ADC, the DSP becomes a complete microsensor node.

A Sub-threshold Cell Library and Methodology

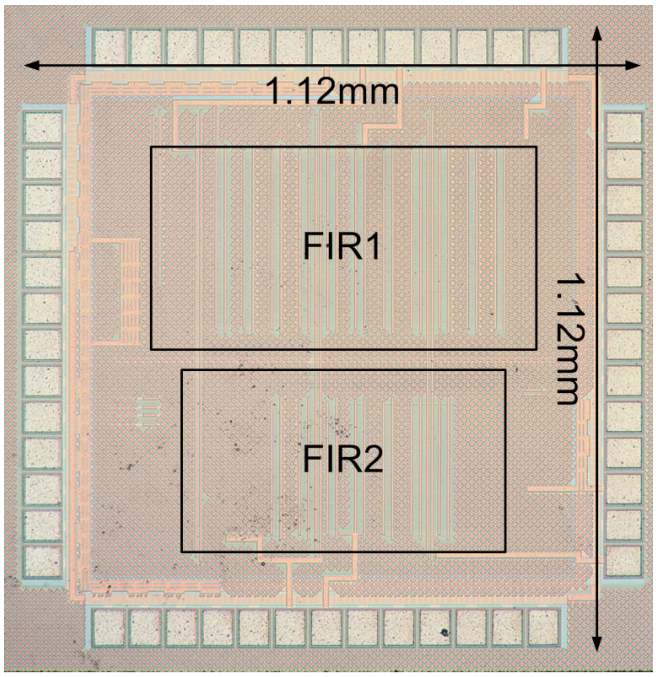
J. Kwong, A.P. Chandrakasan
Sponsorship: Texas Instruments, DARPA

In this work, we develop a sub-threshold library and design methodology that addresses the unique challenges and trade-offs in ultra-low voltage operation. Drive currents become comparable in magnitude to idle leakage currents, causing reduced output swings and possible functional errors. Due to the exponential dependence of sub-threshold currents on threshold voltage, sub-threshold circuits are particularly sensitive to environmental and process variations. Figure 1 compares the delay distributions of an 8-bit adder in the sub-threshold and above-threshold regimes under transistor threshold voltage variation. Circuit performance exhibits much larger variability in sub-threshold, which can be mitigated through device sizing and choice of logic styles.

The sub-threshold library employs a device-sizing methodology with functionality as the primary consideration, while implementing appropriate trade-offs between energy, delay, and variability. The theoretical sizing approach is detailed in [1] and validated in a 65-nm CMOS test chip fabricated by Texas Instruments. The test chip, shown in Figure 2, consists of two 16-bit FIR filters synthesized from the custom library using a standard CAD flow. By voltage scaling the power supply from 1.2V to 300mV, the test chip achieves 8 times energy reduction per filtering operation.



▲ Figure 1: Delay distribution of 8-bit adder in sub-threshold (top) and nominal V_{DD} (bottom), under threshold voltage variation. Arrow points to outliers.



▲ Figure 2: Die photograph of sub-threshold library test chip in 65-nm CMOS. Total die area is 1.12 x 1.12mm^2.

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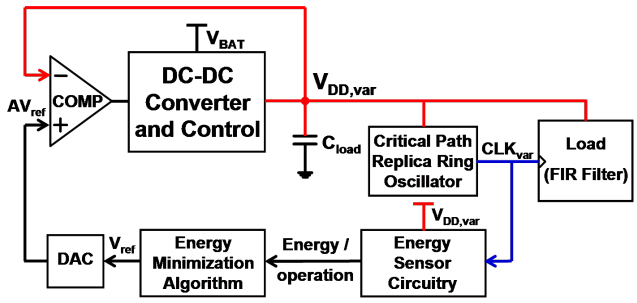
Minimum Energy Tracking Loop with Embedded DC-DC Converter in 65-nm CMOS

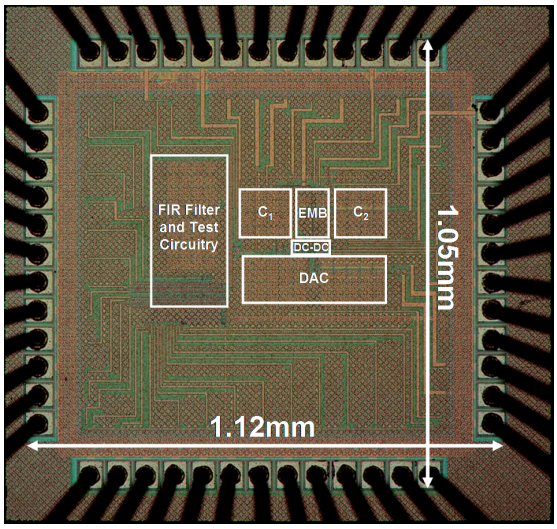
Y.K. Ramadass, A.P. Chandrakasan
Sponsorship: DARPA, Texas Instruments

Minimizing the energy consumption of battery-powered systems is a key focus in integrated circuit design. Switching energy of digital circuits reduces quadratically as V_{DD} is decreased below V_T, i.e., sub-threshold operation, while the leakage energy increases exponentially. These opposing trends result in a minimum energy point (MEP), defined as the operating voltage at which the total energy consumed per operation (E_{op}) is minimized [1]. The MEP can vary widely for a given circuit depending on its workload and environmental conditions, e.g., temperature. Energy savings of 50 - 100% are demonstrated by tracking the MEP as it varies, and even greater savings can be achieved in circuits dominated by leakage.

The energy-minimization circuitry shown in Figure 1 consists of a buck converter [2] that operates in the Pulse Frequency Modulation (PFM) mode. The digital circuit (FIR filter), which operates at the V_{DD} set by the converter, is clocked by a critical path replica ring oscillator. The energy-sensor circuitry determines the energy consumed per operation at different operating voltages. Based on the energy per operation at a given operating voltage obtained from the energy-sensing circuit, an energy minimization algorithm changes the reference voltage to the buck converter suitably and the system approaches the minimum-energy operating voltage of the digital circuit using a slope-detection strategy. A test chip containing the minimum-energy tracking loop and the embedded DC-DC converter was fabricated in Texas Instruments' 65nm CMOS process (Figure 2). The area overhead of the minimum energy tracking loop which comprises the energy-minimizing block and the energy sense capacitors C_1 and C_2 is just 0.05mm^2. The digital test circuitry operates at voltages as low as 0.25V. Energy savings of the order of 50 – 100% were measured while tracking the MEP as it varies with workload and temperature. The DC-DC converter was able to deliver load voltages between 0.25V and 0.7V with an efficiency > 80% at load power levels of the order of 1μW and above.



▲ Figure 1: Block diagram of the minimum-energy tracking loop and embedded DC-DC converter.



▲ Figure 2: Die Photo of the test chip in 65nm CMOS. The EMB is the energy-minimizing block, which comprises the energy-sensor circuitry and the energy-minimization algorithm.

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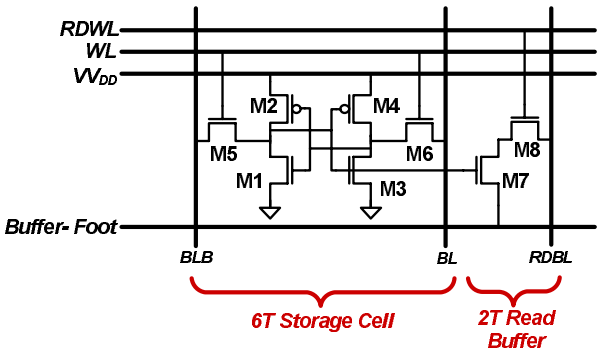
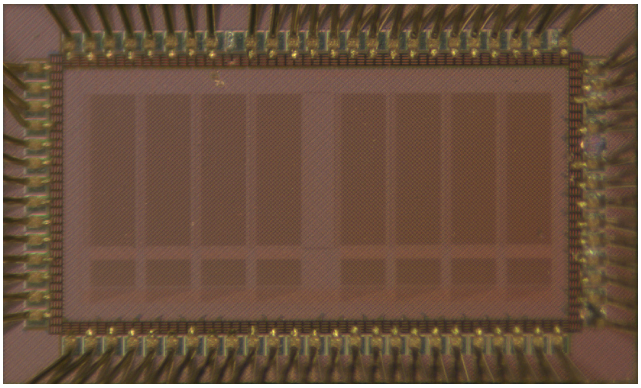
A 65-nm 8T Sub-threshold SRAM Employing Sense-amplifier Redundancy

N. Verma, A.P. Chandrakasan
Sponsorship: DARPA, Intel Foundation Ph.D. Fellowship Program, NSERC

Deeply scaled technologies promise greater efficiency for digital circuits. Unfortunately, random device variations compromise the functionality of large SRAM arrays, which traditionally rely on ratioed bit-cell topologies to achieve the highest density. By virtue of greatly reduced leakage and access energy, sub-threshold SRAMs tremendously lower the total system power but require new bit-cell topologies and peripheral assists to manage variation and read-current degradation [1]. This work demonstrates a 256kb SRAM in 65-nm CMOS that uses the bit-cell shown in Figure 1 [2]. The buffered read eliminates the read static noise margin limitation [3]; peripheral footer circuitry eliminates read data signal degradation due to bit-line leakage; peripheral supply drivers weaken the accessed storage cells to enforce the relative device strengths required for write-ability; and sense-amplifier redundancy provides a favorable trade-off between the offset and the area of the sensing network. These techniques are applied in the prototype test-chip shown in Figure 2. The test-chip integrates 256kb-in-8, 256-row-by-128-column blocks. Test results show that the design achieves full read and write functionality to 350mV, where the leakage power savings are over 20x compared to a 6T SRAM at 1V and over 3x compared to a 6T SRAM operating at its projected lowest voltage. Additionally, sense-amplifier redundancy reduces the probability of error from offsets by a factor of 5 for a given area constraint.



▲ Figure 1: An 8T bit-cell with 2T read-buffer for read stability and peripheral control of buffer-foot and VV_{DD} to manage bit-line leakage and write-ability in the presence of variation.



▲ Figure 2: Prototype 256kb SRAM in 65-nm CMOS organized as 8 blocks with 256 rows and 128 columns. Test-chip achieves full read and write functionality to 350mV.

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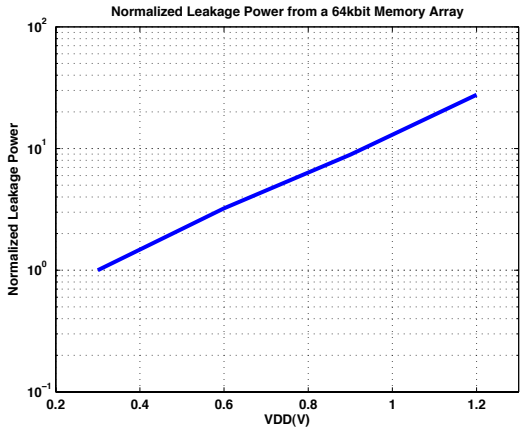
A 65-nm, Ultra-dynamic Voltage, Scalable SRAM with Operating Range from 300mV to 1.2V for Optimal Performance and Energy

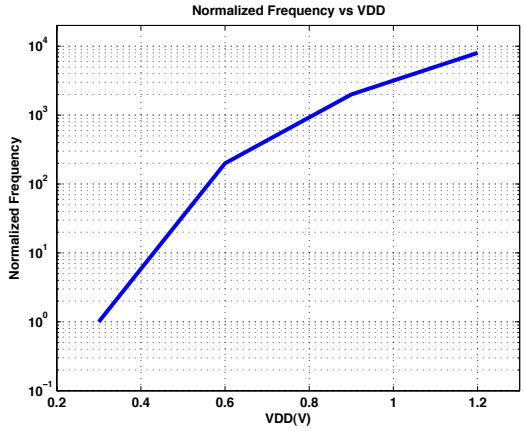
M.E. Sinangil, N. Verma, A.P. Chandrakasan
Sponsorship: DARPA

Memory blocks account for a large fraction of the total chip area and total power consumption, so making a low power memory is very important for applications where power consumption is crucial. Dynamic Voltage Scaling is a very well-known method for reducing the power consumption of a system when the performance requirements change [1]. If the performance requirement for a system is varying, the voltage level and hence the speed of the system can also be changed instead of running the whole circuit at the highest speed and voltage all the time. Since energy consumption depends on the voltage level, significant savings can be achieved. Figure 1 shows the normalized leakage power of a 64kbit-SRAM memory array over different voltages. Operating the memory at 0.3V provides nearly 30X leakage power reduction. Figure 2 shows the normalized frequency of operation for the same memory over 0.3V to 1.2V range.

Designing a memory for operation in both sub-threshold and above threshold is challenging because of the totally different characteristics of these regions. It is shown that a classical 6Tcell cannot operate in sub-threshold because of the degraded Read and Write Static Noise Margins (SNM). An 8T design is shown to be fully operational in the sub-threshold region [2]. In this design, the addition of a read-buffer to the bit-cell and the peripheral assists ensures the correct read operation. Correct write operation requires the header of the bit-cell to be driven to ground. However, for the high voltage operation, some of the peripheral assists may not be needed and, even more importantly, they might severely degrade the performance of the circuit. Because of that, the bit-cell transistor sizing and peripheral circuitry design should be made by considering their effects on circuit operation for both ends of the voltage range.



▲ Figure 1: Normalized leakage power of a 64kbit-SRAM memory array over the range 0.3V to 1.2V.



▲ Figure 2: Normalized frequency of operation of the memory over the range 0.3V to 1.2V.

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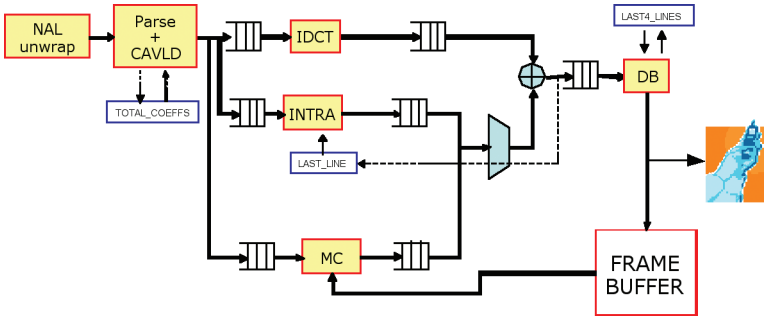
Algorithms and Architectures for Ultra-low-power Video Compression

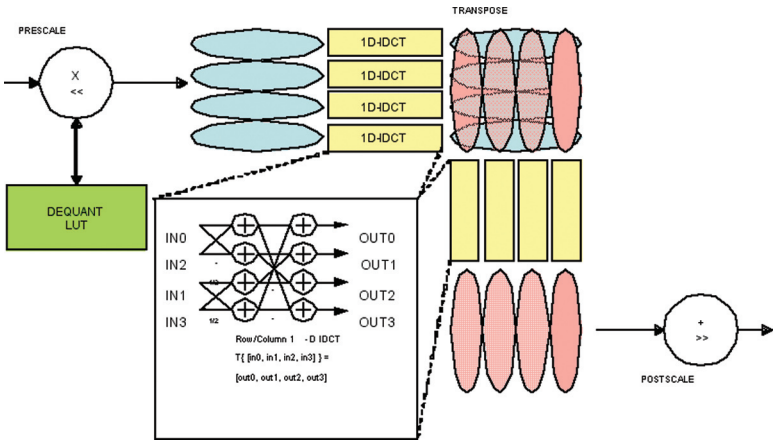
D. Finchelstein, V. Sze, A.P. Chandrakasan
Sponsorship: Nokia, Texas Instruments

Multimedia applications, such as video playback, are becoming increasingly pervasive. Since the platforms are often energy-constrained devices (cell phones, IPODs), the user experience is enhanced by extending the battery life during video decoding. The latest video coding standard is H.264 [1], and it is used in DVB-H and HDTV. While it provides a 50% improvement in compression efficiency over previous standards, this coding efficiency comes at the cost of increased decoder complexity of 4X over MPEG-2 and 2X over MPEG-4 Visual Simple Profile. This increased complexity translates to increased energy consumption, which is a critical concern for mobile and handheld devices.

This project aims to build an ASIC decoder that exploits techniques such as pipelining, parallelism, ultra-low voltage operation, and ultra-dynamic voltage scaling [2]. For instance, the IDCT computation can be parallelized as shown in Figure 2. In video decoders, memory consumes a large portion of overall system power. As a result, the number of redundant memory transfers must be minimized and caching data in on-chip SRAMs/registers should be explored. Using these techniques, the goal is to minimize system power, as compared to previously published decoders [3-4]. In addition to optimizing the hardware architecture of the H.264 decoder (Figure 1), we will also focus on the design of future video coding standards, e.g., "H.265". We envision that future algorithms will account for the energy and complexity costs of their hardware implementations. By incorporating the energy-awareness into the algorithm, future video coders can provide an explicit energy/PSNR trade-off, along with the existing bitrate/PSNR trade-off curves.



▲ Figure 1: H.264 video decoder architecture.



▲ Figure 2: Parallel IDCT architecture.

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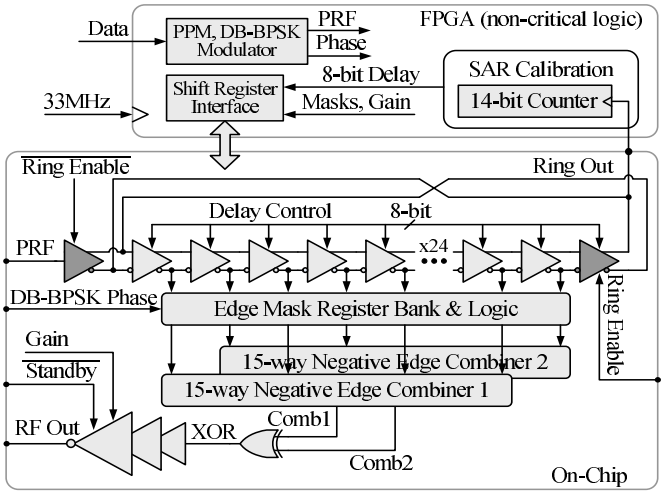
An All-digital UWB Transmitter in 90-nm CMOS

D. Wentzloff, A.P. Chandrakasan
Sponsorship: SRC/FCRP C2S2, NSF

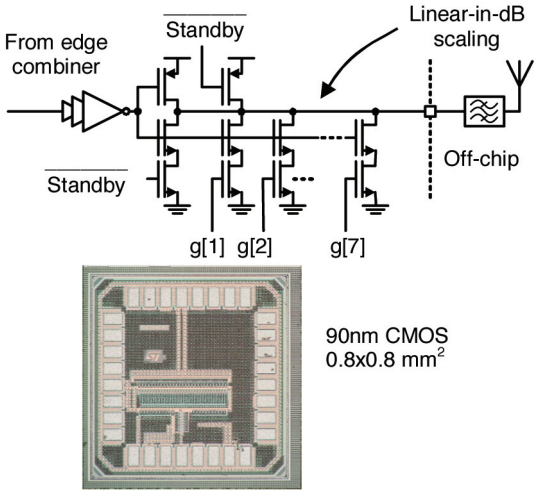
Pulsed ultra-wideband (UWB) transceivers offer the potential for ultra-low-energy/bit operation because the signals are inherently duty-cycled. By eliminating components with long startup times, such as a phase-locked loop, all components in a pulsed-UWB transceiver can be disabled during the interval between pulses. This work focuses on an all-digital, pulsed-UWB transmitter that requires no analog bias currents, in which the energy is dissipated only in switching events, i.e., CV^2, and by sub-threshold leakage currents.

This transmitter supports three channels with center frequencies of 3.45GHz, 4.05GHz, and 4.65GHz, and each channel carries 550-MHz-wide pulses. It communicates with a separate receiver IC [1] that performs energy detection in the desired channel. Pulse position modulation (PPM) is used to encode the data with a pulse repetition frequency (PRF) range of 10kHz-16.7MHz and a fixed PPM delay of 30ns. A block diagram of the transmitter is shown in Figure 1. Pulses are formed by combining a programmable number of equally-delayed edges, similar in operation to a frequency multiplier. During pulsed operation, the last stage of the delay line feeding back to the input is disabled, and the input to the delay line is a clock signal operating at the PRF. Depending on the data, the rising edge of this clock is externally delayed by the PPM interval of 30ns. This clock propagates through a 32-stage differential delay line with a delay controlled by an 8-bit code, which generates a series of edges. The output of each stage is independently masked, and thus only the selected edges are combined to form an RF pulse. The 30 masked edges are combined using interleaved 15-edge combiners that toggle their outputs on falling edges on any of their inputs [2]. Thus, pulses are generated only on the rising edge of the PRF signal. The two combiners' outputs are XOR'ed. The resulting pulse has a center frequency determined by the delay per stage and a pulse width determined by the number of edges selected. The RF pad driver is essentially a CMOS inverter, with some added features for reducing leakage current and digitally controlling the output power (see Figure 2). The pulsed output of the inverter chain has spectral content at DC; therefore an off-chip band-select filter has been used to eliminate the DC content.

The chip was fabricated in a 90-nm CMOS process; a die photo is shown in Figure 2. The transmitter consumes a fixed 96μW due to leakage currents. The active energy added only while pulsing is 37pJ/pulse, independent of the data rate. Pulse generation has been demonstrated in the three desired channels and the transmitter operation was verified in a wireless link using an energy-detection receiver [1]. At 16.7Mb/s, the total energy consumption (active and leakage power) is 43pJ/bit.



▲ Figure 1: Block diagram of the all-digital transmitter. All blocks are full-swing static CMOS circuits.



▲ Figure 2: Digital RF pad driver (top) and die photo of the transmitter (bottom).

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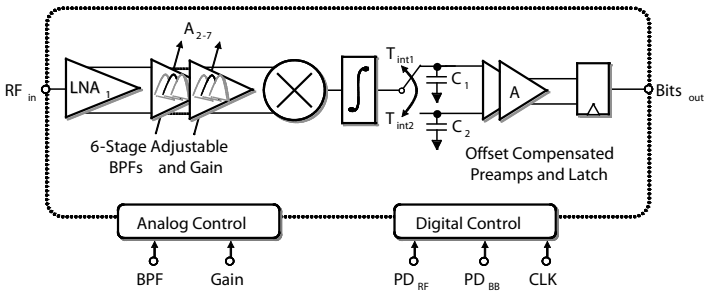
A 3- to 5-GHz Sub-banded UWB Receiver in 90-nm CMOS

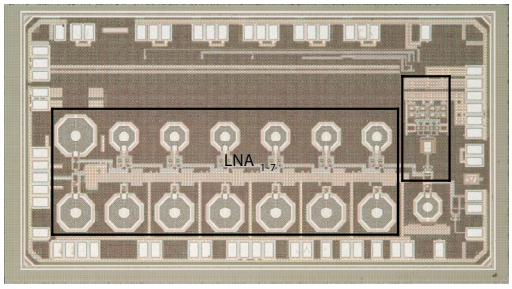
F.S. Lee, A.P. Chandrakasan
Sponsorship: SRC/FCRP C2S2, NSF

With the proliferation of portable electronics and wireless sensor networks, energy-efficient radios have become an active area of research [1-3]. Though sub-nJ/b data reception is achievable for data rates >100Mbps using optimized coherent architectures [4], there is a need for simple, low-cost, low-power, and scalable radios as specified in the IEEE 802.15.4a task group [5]. This work explores the unique properties of FCC-compliant pulsed UWB signals and scaled CMOS devices to improve energy/b of existing low data-rate GHz-range integrated radios for use in wireless sensor network applications.

A non-coherent 0–16Mbps UWB receiver (Figure 1) using 3–5GHz sub-banded PPM signaling is implemented in a 90-nm CMOS process (Figure 2) [6]. The RF and mixed-signal baseband circuits operate at 0.65V and 0.5V. Using duty-cycling, adjustable bandpass filters, and a relative-compare baseband, the receiver achieves 2.5nJ/b at 10^{-3} BER with -99dBm sensitivity at 100~kbps. The energy efficiency is maintained across three orders of magnitude in data rate. A basic acquisition algorithm is developed on an FPGA platform and a transceiver system demo is assembled using this chip.



▲ Figure 1: Receiver block diagram.



▲ Figure 2: Chip die photo.

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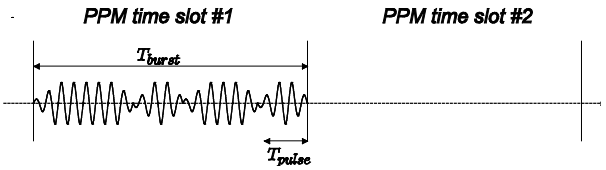
Pulsed UWB Transceiver for Small Lightweight Flying Vehicles

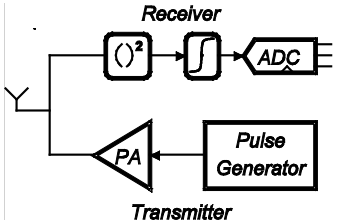
D.C. Daly, M. Bhardwaj, P. Mercier, A.P. Chandrakasan
Sponsorship: DARPA, NSERC

Ultra-wideband (UWB) technology has recently gained popularity for low-power, low-data rate wireless links [1-2]. In January 2007, an amendment to the low-power IEEE 802.15.4 standard was approved that adds support for an alternate, UWB physical layer. The UWB physical layer supports scalable data rates from kbps to Mbps, distances up to 100m, and both non-coherent and coherent signaling. The signaling scheme includes pulse-position modulation (PPM) combined with BPSK pulse bursting. Figure 1 presents a time-domain waveform of the 802.15.4a signaling scheme, in which multiple pulses are BPSK- modulated in a short burst during a single PPM time slot.

Our target wireless application is a small, lightweight flying vehicle. The flying vehicle must be able to communicate wirelessly up to 100 meters at a data rate of tens to hundreds of kbps. As the vehicle is miniature, power consumption, volume, and weight must all be minimized. In such systems, the transceiver must be highly integrated with few if any off-chip components. Non-coherent UWB signaling is used to relax the frequency accuracy requirements of RF circuit blocks, thereby allowing for a highly integrated, low-power implementation. Figure 2 presents the proposed UWB transceiver architecture. The receiver consists of a windowed energy detector and the transmitter consists of an all-digital pulse generator followed by a power amplifier. The lack of phase information associated with non-coherent signaling makes synchronization more challenging, leading to longer preambles. We are designing codes and algorithms to minimize this penalty.



▲ Figure 1: Time-domain representation of UWB pulse bursting combined with pulse-position modulation.



▲ Figure 2: Proposed 802.15.4a transceiver consisting of a burst-mode UWB transmitter and a non-coherent, energy-detection receiver.

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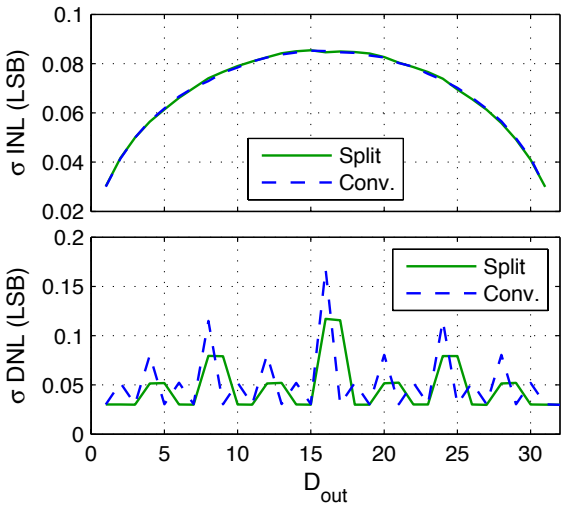
Reaching the Optimal Mixed-signal Energy Point

B.P. Ginsburg, A.P. Chandrakasan
Sponsorship: NDSEG Fellowship, DARPA

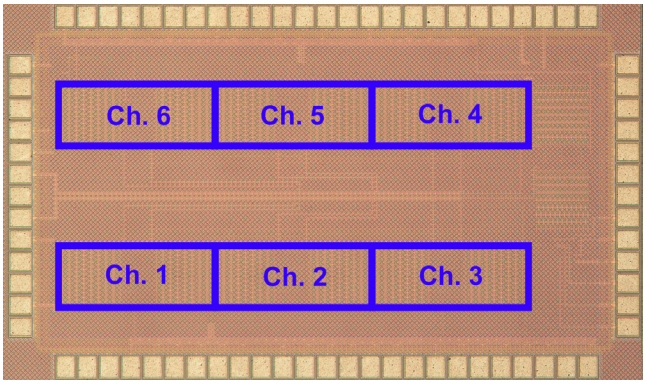
Ultra-wideband radio can be used for very high data rate (≥480 Mb/s) communication over short distances. For proper reception, the receiver requires a 500 MS/s analog-to-digital converter (ADC) with 4 bits of resolution. While flash is the typical architecture chosen, successive approximation register (SAR) ADCs feature superior complexity characteristics with similar amenability to deep submicron CMOS. Time-interleaving multiple SAR ADCs allows this long latency architecture to equal the throughputs necessary for UWB reception [1]. A comparative energy model concludes that SAR should outperform flash above 5 bits of resolution in 0.18μm CMOS, with its energy advantage improving in more advanced technologies [2]. The SAR architecture is particularly well suited to meet the challenges of design in deep submicron CMOS, including reduced voltage supplies, increased variability, and lower transistor output impedances. It uses only open loop amplification in a comparator, as opposed to the operational amplifier for the pipelined architecture. There is significant digital complexity on the critical path in a SAR converter, but digital power and speed directly benefit from the reduced feature sizes.

A prototype 500-MS/s, 5-b, 6-way time-interleaved SAR ADC [3] has been designed and fabricated in Texas Instruments' 65-nm CMOS process. The prototype includes the split capacitor array that conserves charge between bit-cycles to lower the overall switching energy, and it settles faster because fewer capacitors switch during each period. The array also exhibits improved differential nonlinearity, as seen in Figure 1, with the same integral nonlinearity, which decreases the capacitor matching required to avoid missing codes. The ADC achieves Nyquist performance and consumes 6 mW from a 1.2 V supply. Its die photo is shown in Figure 2.

An understated trend in ADC design is the significant impact of digital circuitry on performance and power, particularly at medium to low resolutions. Even in this advanced technology, half of the total ADC power is consumed by the digital circuitry. A genuine mixed-signal energy optimization that explicitly includes all of the analog and digital blocks, and their interactions, is being developed to minimize the power consumption of this ADC. The optimization uses coupled energy and behavioral models to explicitly define the analog/digital interactions and tradeoffs.



▲ Figure 1: Behavioral simulations comparing the static linearity of the conventional and split capacitor arrays.



▲ Figure 2: Die photograph of 65-nm CMOS ADC. Total die area is 1.2 x 1.8 mm^2.

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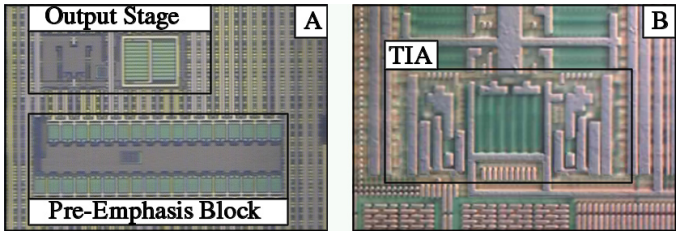
18Gb/s Optical IO: VCSEL Driver and TIA in 90-nm CMOS

A. Kern, I. Young, A.P. Chandrakasan
Sponsorship: SRC/FCRP IFC, Intel Corporation, NSF

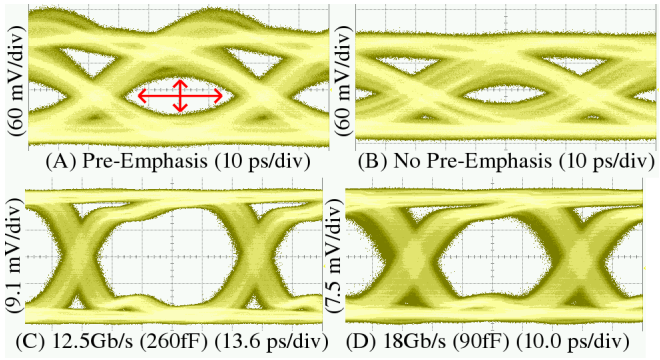
Electrical IO is becoming limited by copper interconnect channel losses that depend on frequency and distance. Package-to-package optical interconnect sees negligible frequency-dependent channel losses, but data rates are limited by the intrinsic optical dynamics and electrical parasitics of the optical devices. This abstract summarizes the results of [1] and [2], including a pre-emphasis VCSEL driver and a cross-coupled cascode transimpedance amplifier (TIA) that apply circuit techniques to operate optical components beyond the intrinsic data rates imposed by these bandwidth limits. Die photographs of the fabricated VCSEL driver and TIA are shown in Figure 1A and Figure 1B, respectively.

The presented VCSEL driver operates a standard commercial GaAs VCSEL at 18Gb/s by using pre-emphasis to compensate for the large capacitance and intrinsic optical dynamics of the VCSEL. The driver derives timing information directly from the full-rate input data and generates pre-emphasis pulses with width resolution less than one bit period in a manner that is compatible with full-rate IO architectures. The VCSEL is modulated with the summed output of two current-mode drivers, where the output of the second driver is delayed, inverted, and attenuated with respect to the first. DACs and a digital delay line provide digital control of the pre-emphasis pulse height and pulse width. Optical measurements shown in Figure 2A and Figure 2B demonstrate that pre-emphasis improves the vertical eye opening by 122% and the horizontal eye opening by 76% for modulation from 2mA to 10mA.

The differential TIA is based on a proposed core amplifier that uses cross-coupled NMOS cascodes to increase gain and bandwidth. A proposed symmetric feedback method provides near-constant gain from DC to 9GHz in the differential TIA when used in conjunction with a DAC to perform DC offset cancellation. Measurements and simulations demonstrate that the TIA has the required gain and bandwidth to operate at 12.5Gb/s with 260fF input capacitance (Figure 2C) and 18Gb/s with 90fF input capacitance (Figure 2D) for an input current of 200uA.



▲ Figure 1: Die photographs of the fabricated pre-emphasis VCSEL driver (A) and cross-coupled cascode transimpedance amplifier (B).



▲ Figure 2: Measured eye diagrams of the VCSEL driver and transimpedance amplifier. For the VCSEL driver, pre-emphasis (A) improves the original eye (B). The TIA operates at 12.5Gb/s with 260fF (C) and 18Gb/s with 90fF (D) of input capacitance.

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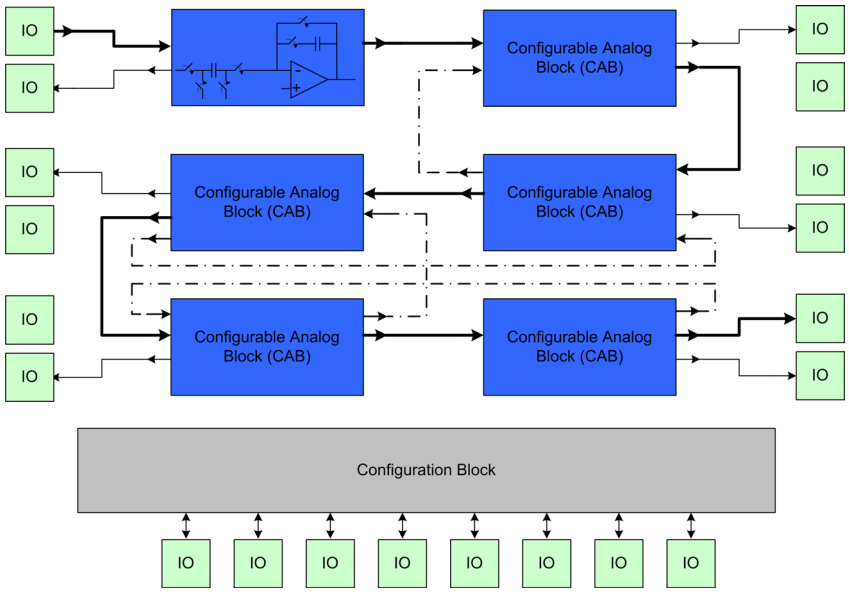
Reconfigurable Zero-crossing-based Analog Circuits

P. Lajevardi, A.P. Chandrakasan, H.-S. Lee
Sponsorship: CICS, DARPA

Switched-capacitor circuits can be used to implement many analog systems such as ADCs, DACs, filters, amplifiers, and integrators. In this research, a reconfigurable switched-capacitor system is proposed to implement different analog systems. Using the same building blocks, Figure 1 shows the block diagram of the system. Each switched-capacitor block can implement an integrator or a multiplier with a reconfigurable coefficient. Such a system will be useful for software defined radios and fast prototyping of analog circuits.

The design of such systems has not been practical since switched-capacitor circuits are op-amp-based. The design of reconfigurable switched-capacitor blocks with op-amp is very challenging if widely ranging speed, accuracy, signal-to-noise ratio (SNR), and power consumption space are to be covered. Many different op-amp topologies may be required to cover a large performance and configuration space. While new technology nodes provide transistors with higher f_t, the design of op-amp is becoming more challenging as the supply voltage and intrinsic gain of transistors are decreasing. Recently, [1] and [2] proposed zero-crossing circuits to design ADCs. Zero-crossing circuits can replace the op-amp in traditional switched-capacitor design with a combination of a current source and a zero-crossing detector. The power consumption of zero-crossing-based analog circuits scales according to the operating frequency and required SNR. Zero-crossing circuits are used to implement the reconfigurable analog blocks needed for this research. The system can operate at different speeds and SNR requirements while the power consumption is kept at the optimum level.



▲ Figure 1: Block diagram of reconfigurable zero-crossing-based analog circuits. Each configurable analog block can be programmed to perform an integration or multiplication.

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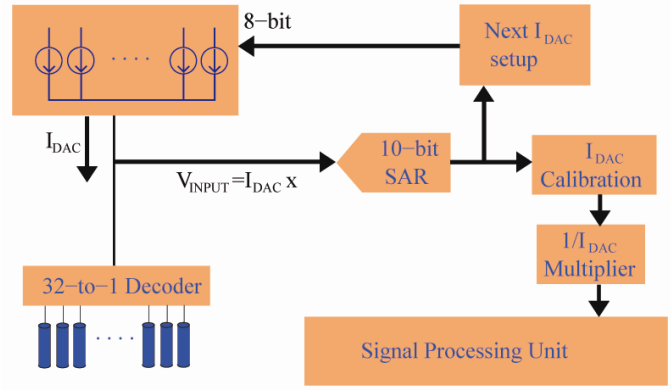
Design and Characterization of CNT-CMOS Hybrid Systems

T.S. Cho, K.-J. Lee, T. Pan, J. Kong, A.P. Chandrakasan
Sponsorship: SRC/FCRP IFC, Intel

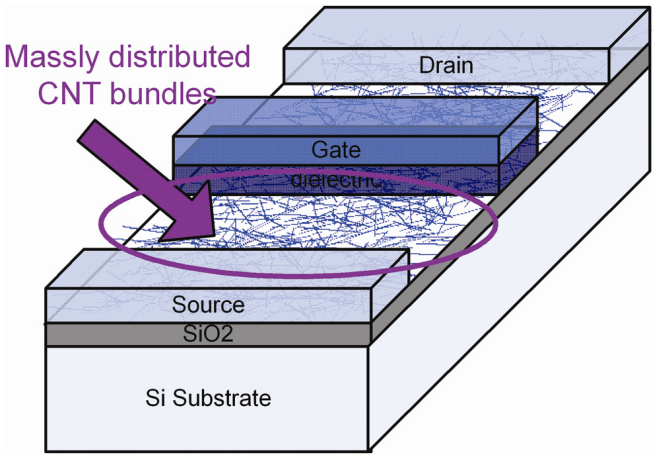
Carbon nanotubes (CNTs) are nanometer-diameter cylinders formed from rolled-up graphene sheets [1]. CNTs have found widespread interest due to many of its excellent electrical properties. In particular, the low density and high electron mobility of CNTs make them attractive for electronic applications. Our investigation of hybrid CMOS-CNT systems attempts to take advantage of the superior properties of CNTs while building on top of existing CMOS technology.

We propose an integrated chemical sensor system to verify the concept of a CNT-CMOS hybrid system design. The CNT changes its conductance when exposed to certain chemicals, and thus we can effectively use CNTs as resistive chemical sensors [2]. Room-temperature operation of the CNT sensors makes them an appealing candidate for low-power chemical sensor application. However, poor control over the local and global variation of CNT devices, the resolution requirements in resistance measurements, and the changes in resistance due to specific chemicals implies a large dynamic range in the front-end circuitry. We investigate energy efficient architectures to accommodate the specification (Figure 1). Chip fabrication is done by National Semiconductor.

Another system of interest is a DC-DC power converter circuit. Near ballistic transport behavior [3] of CNTFET makes it a potential energy-efficient candidate in power applications. In addition, the power transistor size could be greatly reduced if CNTFETs can replace the CMOS power transistors and the CNTs are aligned. Currently, we are looking into ways to model CNTFET behavior and fabricating CNT devices that can support large currents (Figure 2).



▲ Figure 1: Diagram of CMOS interface. The interface architecture includes on-chip calibration functionality. This interface chip and CNT sensors are integrated at the PCB level.



▲ Figure 2: Device schematic of a massively distributed CNTFET. Bundles of CNTs are fabricated to support large currents. Additional chemical or electrical treatment may be required to eliminate metallic CNTs.

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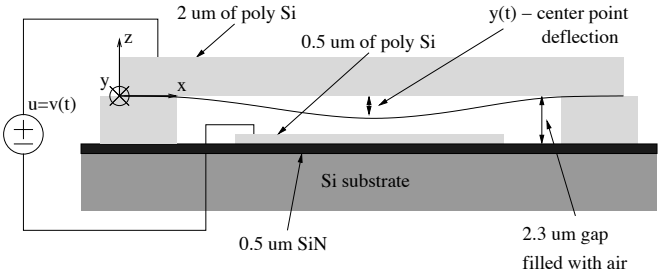
A Piecewise-linear Moment-matching Approach to Parameterized Model Order Reduction for Highly Nonlinear Systems

B. Bond, L. Daniel
Sponsorship: SRC/FCRP GSRC, NSF, DARPA

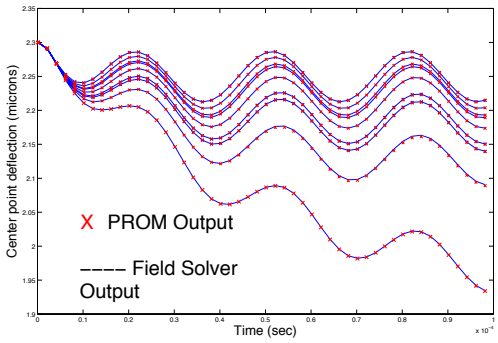
The automatic extraction of parameterized macromodels for modern mixed signal System-on-Chips is an extremely challenging task due to the presence of several nonlinear analog circuits and Micro-Electro-Mechanical (MEM) components. The ability to generate Parameterized Reduced Order Models (PROM) of nonlinear dynamical systems could serve as a first step toward the automatic and accurate characterization of geometrically complex components and sub-circuits, eventually enabling their synthesis and optimization.

Our approach to this problem combines elements of a non-parameterized trajectory piecewise linear method [1] for nonlinear systems with a moment matching parameterized technique [2] for linear systems. By building on these two existing methods, we have created an algorithm for generating PROMs for nonlinear systems. The algorithms were tested on three different systems: a MEM switch, shown in Figure 1, and two nonlinear analog circuits. All of the examples contain distributed strong nonlinearities and possess some dependence on several geometric parameters.

In addition, we have proposed a model-construction procedure in which we approximate the system sensitivity to parameters of interest for the purpose of efficiently sampling important regions of the parameter space. Figure 2 shows the output of one PROM created for the example in Figure 1 and compared to the field solver output of the full nonlinear system at several parameter values. Typical PROMs constructed in this manner can be accurately reduced in size by a factor of 10, yielding a speedup of a factor of 10 in general. For further details on parameter-space accuracy and cost of the algorithms, see [3].



▲ Figure 1: Application example: MEM switch realized by a polysilicon beam fixed at both ends and suspended over a semiconducting pad and substrate expansion



▲ Figure 2: Center point deflection predicted by our parameterized reduced model (crosses) at a series of parameter values, compared to a finite difference detailed simulation (solid lines).

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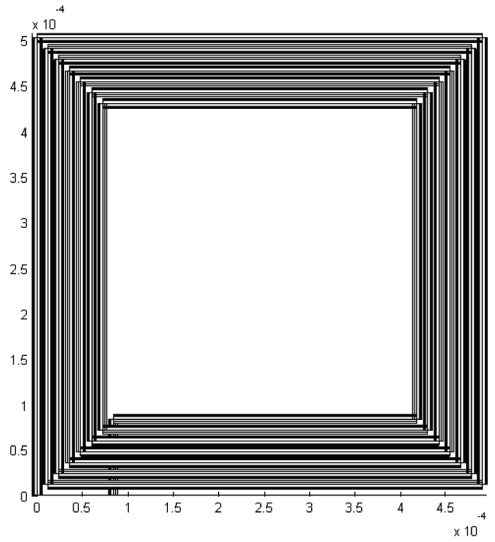
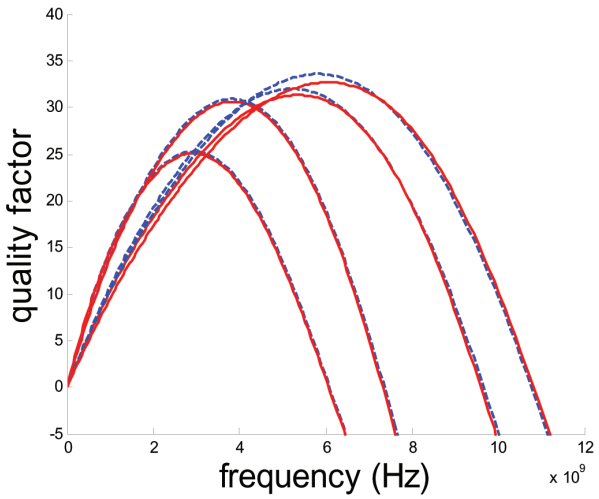
A Quasi-convex Optimization Approach to Parameterized Model-order Reduction

K.C. Sou, L. Daniel, A. Megretski
Sponsorship: SRC/FCRP GSRC, Semiconductor Research Corporation, NSF

This work proposes an optimization-based model order reduction (MOR) framework [1]. The method involves setting up a quasi-convex program that explicitly minimizes a relaxation of the optimal H-infinity norm MOR problem. The method generates guaranteed stable and passive reduced models and it is very flexible in imposing additional constraints. The proposed optimization approach is also extended to a parameterized model reduction problem (PMOR). The proposed method is compared to existing moment matching and optimization based MOR methods in several examples. For example, a 32nd order parameterized reduced model has been constructed for a 7- turn RF inductor with substrate (infinite order) and the error of quality factor matching was less than 5% for all design parameter values of interest.



▲ Figure 1: A 7-turn RF inductor for which a parameterized (with respect to wire width and wire separation) reduced model has been constructed.



▲ Figure 2: Matching of quality factor of 7-turn RF inductor when wire width = 16.5 μm, wire separation = 1,5,18,20 μm. Blue dash line: Full model. Red solid line: ROM.

REFERENCES

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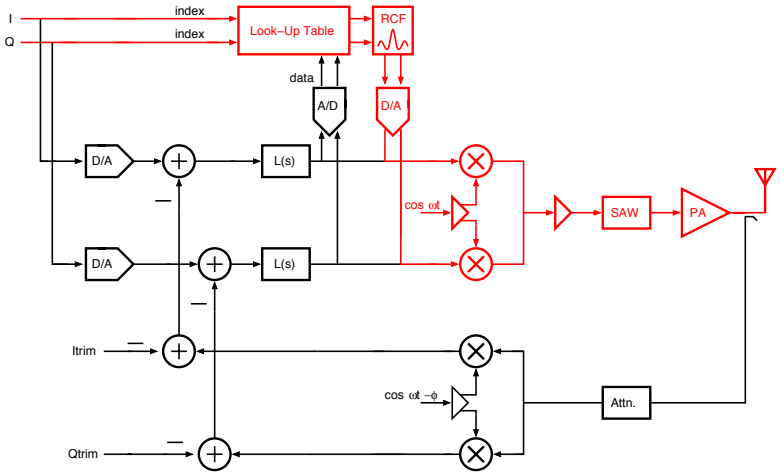
Open-loop Digital Predistortion Using Cartesian Feedback for Adaptive RF Power Amplifier Linearization

S. Chung, J.W. Holloway, J.L. Dawson
Sponsorship: SRC/FCRP C2S2, KOSEF

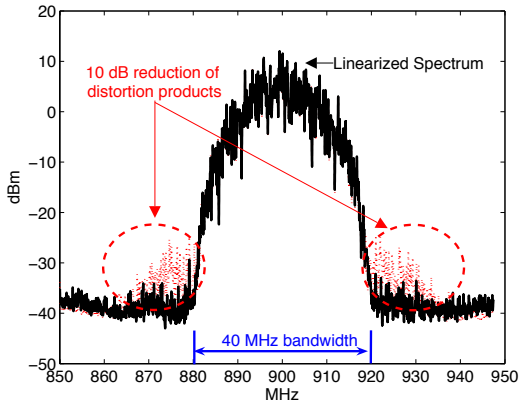
This work focuses on implementing a new wideband linearization technique for RF power amplifiers (PAs). Linearization is necessary for PAs because they consume the bulk of the power in most transmitter chains. The efficiency improvement offered by linearization translates into significant overall power savings in mobile broadband streaming video systems. Our technique combines the best of two established RF PA linearization techniques: digital predistortion and Cartesian feedback. We get the modeling simplicity of Cartesian feedback, combined with the wideband capability of digital predistortion. Substantial improvement in the PA output spectrum and adjacent channel power ratio can be achieved with little increase in power and die area.

Cartesian feedback is an analog technique, giving the ability to continuously linearize a PA without the extensive knowledge of PA characteristics [1], but the bandwidth of classical Cartesian feedback systems is severely limited by the need for a surface-acoustic wave filter. Digital predistortion is an inherently open-loop technique and thus does not suffer from the bandwidth limitation. Nevertheless, digital predistortion requires detailed modeling of a PA and cannot cope with the drift of the PA characteristics [2]. Our technique uses a slow Cartesian feedback loop to train a Cartesian look-up table predistorter to be used for digital predistortion [3], characterizing a PA over the input symbol constellation.

We designed and implemented a 900-MHz RF transmitter with a class-A PA using discrete modules (Figure 1). A measured spectrum of QAM-16 signals having 40 MHz bandwidth (Figure 2) shows approximately 10 dB linearity enhancement and good noise floor. The measured channel power is 27 dBm. The 1-dB compression point of the PA is 26.5 dBm. The implemented transmitter achieved a 2.3-W reduction in power consumption. Our prototype provides linearization at symbol rates over two orders of magnitude higher than is possible with conventional analog feedback.



▲ Figure 1: Cartesian feedback for predistortion.



▲ Figure 2: Power amplifier output spectrum for 40-MHz bandwidth 16-QAM signals.

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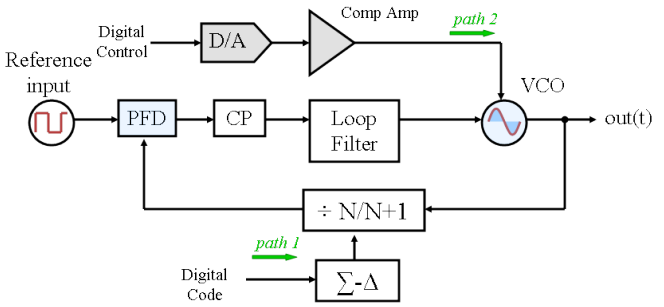
Wideband Two-point Modulators for Multi-standard Transceivers

S. Rayanakorn, J.L. Dawson
Sponsorship: SRC/FCRP C2S2

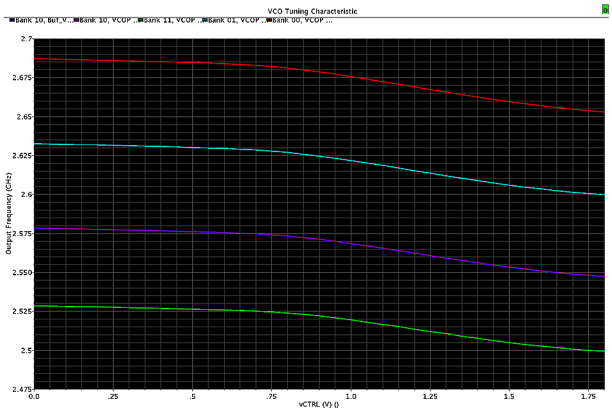
Two-point modulators are a fundamental building block in polar transmitters, which have the potential to accommodate multiple wireless standards. A primary challenge for polar transmitters, however, is that they demand large baseband bandwidths compared to their Cartesian counterparts. To put polar transmitters into use, the separate amplitude and phase paths have to be extremely broadband. This project addresses the need on the phase path.

The two-point modulator, used to perform phase modulation, is a phase-locked loop (PLL) with two inputs (Figure 1). The input data through the first path is low-pass filtered to the output by the closed-loop transfer function of the PLL. If this terminal were the only input, the speed of the PLL would therefore limit the achievable data rate. However, in a two-point modulator, data injected into the second path is high-pass filtered to the output. The corner frequency of this high-pass filter is exactly equal to the low-pass corner of the PLL's closed-loop transfer function. In theory, the bandwidth of a two-point modulator is therefore unbounded. However, nonlinearity in the voltage-controlled oscillator (VCO) (Figure 2) is a barrier to realizing this potential of two-point modulators. The high-pass second path does not benefit from the linearized VCO tuning characteristic that the PLL provides for the first path. If this linearity goes uncorrected, a wideband two-point modulator can introduce significant phase error.

Adaptive digital predistortion, a linearization technique commonly applied to RF power amplifiers, is a promising solution. Recent work using analog feedback to train a predistorter has been shown to enable dramatic bandwidth extensions for Cartesian feedback power amplifiers [1]. With this same principle and the observation that the PLL continuously performs VCO linearization, a predistortion block is added in the second data path. The introduction of this predistortion circuit will eliminate the phase error, and it therefore enables the two-point modulator to function as a truly broadband phase path in polar transmitters.



▲ Figure 1: Classical two-point modulator.



▲ Figure 2: Voltage-controlled oscillator nonlinear tuning characteristic (frequency vs. control voltage).

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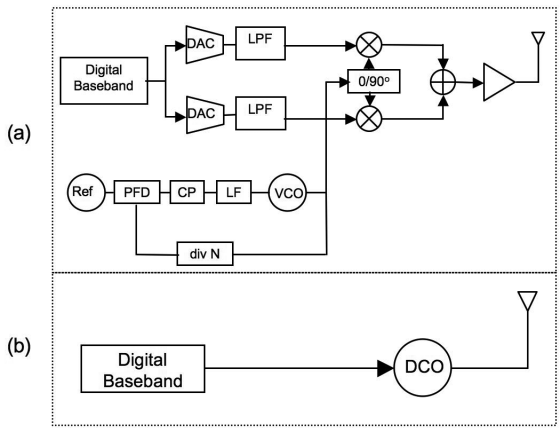
An Ultra-low Power CMOS RF Transceiver for Medical Implants

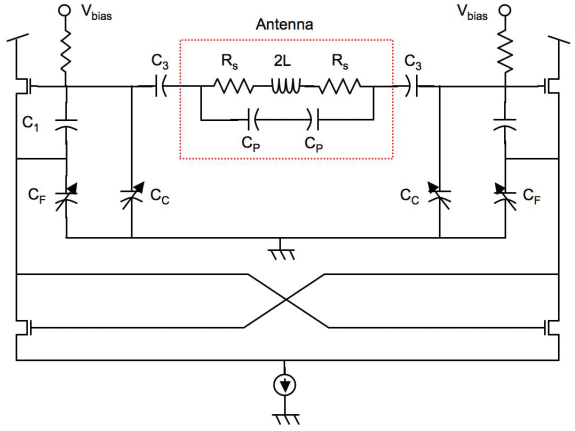
J. Bohorquez, J.L. Dawson, A.P. Chandrakasan
Sponsorship: The Lemelson Foundation Presidential Fellowship

Until recently, few medical implantable devices existed and fewer still provided the capability for wireless transmission of information. Most devices capable of data transmission did so through inductive coupling, which requires physical contact with the base-station and allows for only low data rates. In 1999, the FCC created the Medical Implant Communications Service (MICS) band in the range of 402–405 MHz specifically for medical telemetry [1]. The MICS band plan allows for RF communication between a medical implant and a base-station that is up to two meters away. This research seeks to design a transceiver specifically optimized for low-power, short-distance data transmission in a temperature-regulated environment, i.e., the human body. We do this by pushing as much complexity as possible out of the implant and into the base-station, taking advantage of the attributes of the environment, such as temperature control and slow transients, and incorporating the antenna into the oscillator for reduced power and improved performance. By optimizing the transceiver for reduced volume and power, we hope to extend the battery lifetime and functionality of medical implants for greater comfort and benefits to patients.

Figure 1a shows a conventional direct up-conversion transmitter that comprises a digital baseband, digital-to-analog converters (DAC), low-pass filters, up-conversion mixers, an I/Q phase generator, a power amplifier (PA), a frequency synthesizer, and an antenna. We propose a much simpler, almost all-digital implementation (see Figure 1b, composed of a digital baseband and a digitally controlled oscillator (DCO)). Instead of direct I/Q up-conversion, we propose using minimum frequency-shift keying to directly modulate the DCO with baseband information. We exploit the inherent temperature regulation of the human body and the lax frequency stability requirements of the MICS standard to replace the frequency synthesizer with a much slower frequency-control loop, which incorporates the base-station. Furthermore, we create a linear digital-to-frequency converter by using predistorted capacitor banks for coarse and fine frequency tuning. Instead of driving the antenna with a matched PA, we exploit the low radiation power requirement to incorporate a loop antenna into the DCO. The inherently high Q of the antenna leads to improved noise performance for a given amount of power. Figure 2 shows the differential Clapp DCO including coarse- and fine-tuning capacitor banks, a circuit model for the loop antenna, and a cross-coupled pair of transistors for power reduction [2].



▲ Figure 1: (a) Conventional direct up-conversion transmitter. (b) Proposed transmitter comprised of a digital baseband, a digitally controlled oscillator, and a loop antenna.



▲ Figure 2: Differential digitally controlled Clapp oscillator topology including a simple antenna model, coarse- and fine-tuning capacitor banks, and a cross-coupled transistor pair for current switching.

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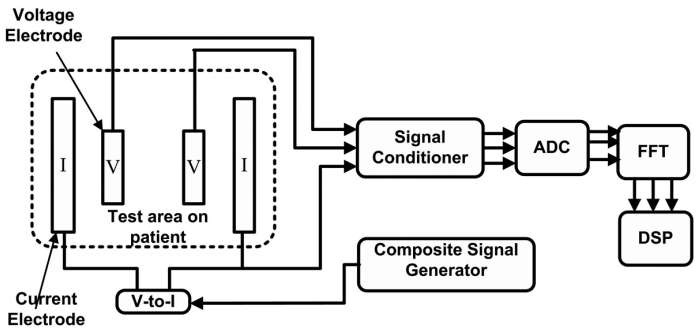
An Integrated Circuit Capable of Rapid Multi-frequency Measurements and a Reconfigurable Electrode Array for Use in Anisotropic Electrical Impedance Myography

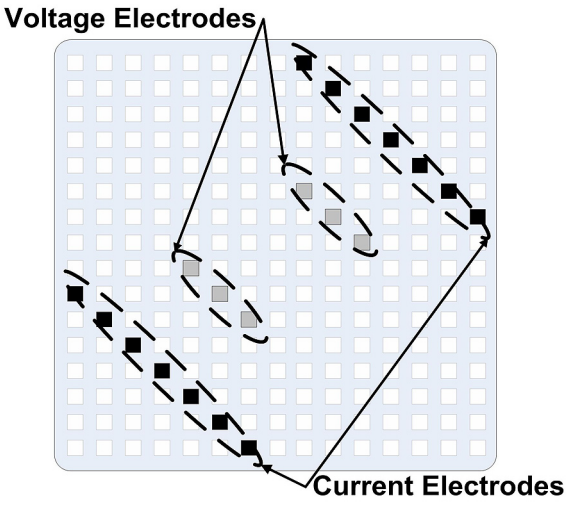
O.T. Ogunnika, M. Scharfstein, J.L. Dawson
Sponsorship: CIMIT, NIH

Electrical impedance myography (EIM) is a noninvasive technique for neuromuscular assessment originally developed by Dr. Seward Rutkove [1] of Beth Israel Deaconess Medical Center and Drs. Ronald Aaron and Carl Shiffman of Northeastern University. The technique is capable of detecting degenerative neuromuscular diseases such as amyotrophic lateral sclerosis (Lou Gehrig's disease) and inclusion body myositis. In this technique, a low-intensity alternating current is applied to a muscle and the consequent surface voltage patterns are evaluated [2,4-5]. Although the current system is sufficient to prove the value of EIM, it is too slow and cumbersome, being made up of large discrete components, to achieve its full potential as a diagnostic medical tool.

This project consists of two main parts. For the first part, we will develop an IC that combines a spectrum analyzer and signal generator (Figure 1) capable of making rapid measurements between 100Hz and 10MHz. This will significantly miniaturize the system and reduce its power consumption, allowing us to build a handheld, battery-operated instrument. Our focus will be on greatly increasing measurement speed, which will enable the clinician to do dynamic muscle characterization that is impossible with current technology. For the second part, we will develop a new, reconfigurable electrode array to make measurements at different orientations on a patient (Figure 2). The electrode array, consisting of many small electrodes combinable into larger virtual electrodes, needs to inject current into a patient's muscle, going through layers of skin and fat, as well as measure voltage precisely and be reusable in a single patient [3]. Through the development of a new electrode array and a new integrated circuit, our goal is to move EIM from a clinically proven concept to a widely applicable, inexpensive, and sophisticated diagnostic tool.



▲ Figure 1: System diagram of integrated circuit.



▲ Figure 2: Concept of reconfigurable electrode array.

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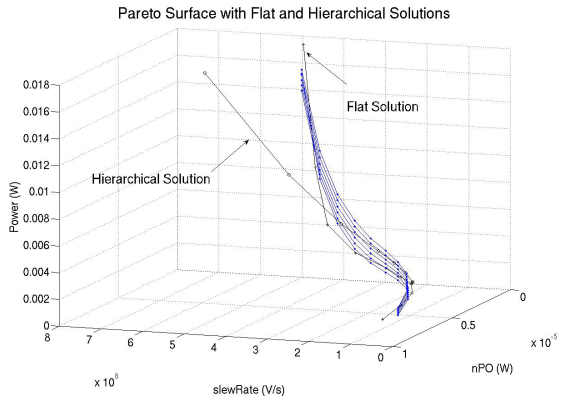
Equation-based Hierarchical Optimization of a Pipelined ADC

T. Khanna, R. Sredojević, W. Sanchez, V. Stojanović, J.L. Dawson
Sponsorship: SRC/FCRP C2S2, CICS

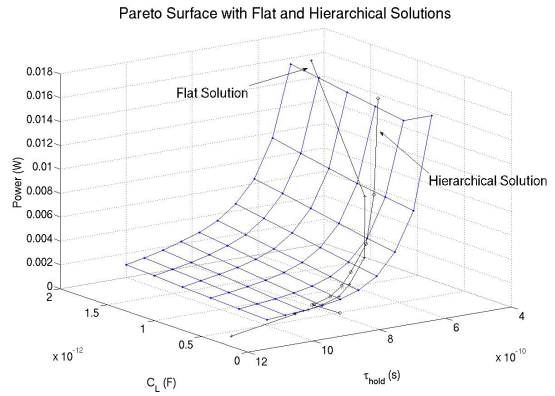
Much work has been done within the optimization and circuit communities related to the optimization of individual circuit blocks [1-2]. Both equation-based and simulation-based optimization methods have enjoyed recent success for certain problems [3-4]. However, the best of these newest methods are still painfully overwhelmed by the sheer size of the design space typical of even modest-sized mixed-signal systems. Employing hierarchy is a natural way to cope with a large number of design variables, and many hierarchical approaches have been explored to simplify system level optimization [5-7]. Still, an efficient technique that brings value to the designer remains elusive.

We propose decomposing a large system into manageable circuit blocks and adopting a hierarchical, bottom-up (H-BU) approach. After efficient exploration of the design space, we generate Pareto optimal curves for the smaller, less complex blocks. The tradeoffs between system design variables are quantitatively modeled as simple monomial functions. Unlike past works, we use simple models to take advantage of the gentle nature of the tradeoffs, thereby making the system formulation less complex and more solver-friendly. This work applies the H-BU method on a 10-stage pipeline ADC in a 0.18-um CMOS process as proof of concept.

The pipeline was optimized to achieve a sampling frequency of 100 MHz with an SNR greater than 60 dB. Figures 1 and 2 plot the operating point of each stage in the pipeline against the Pareto surfaces. Both figures are plotted in the dimensions of the system design variables: Figure 1 plots the power against the slew rate, slewRate, and noise power, nPO, of each pipeline stage and Figure 2 plots power against the load capacitance, C_L, and settling time constant, τ_{hold}, of each pipeline stage.



▲ Figure 1: Pareto surface and power of each pipeline stage in flat and hierarchical solutions against slewRate and nPO.



▲ Figure 2: Pareto surface and power of each pipeline stage in flat and hierarchical solutions against C_L and τ_{hold}.

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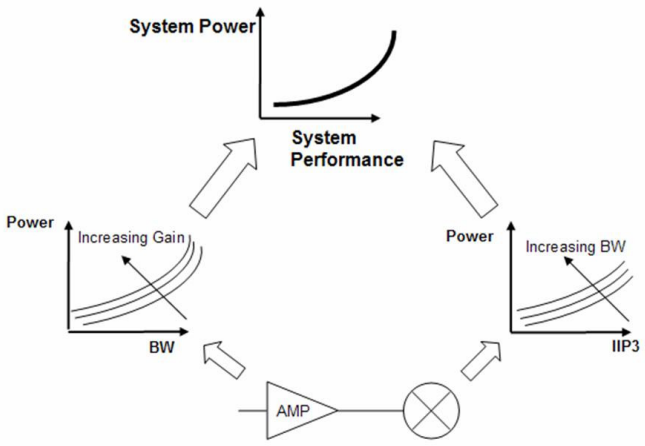
A Hierarchical Bottom-up, Equation-based Optimization Design Methodology for RF Transceivers

W. Sanchez, J.L. Dawson
Sponsorship: Gates Millennium Scholars Graduate Fellowship

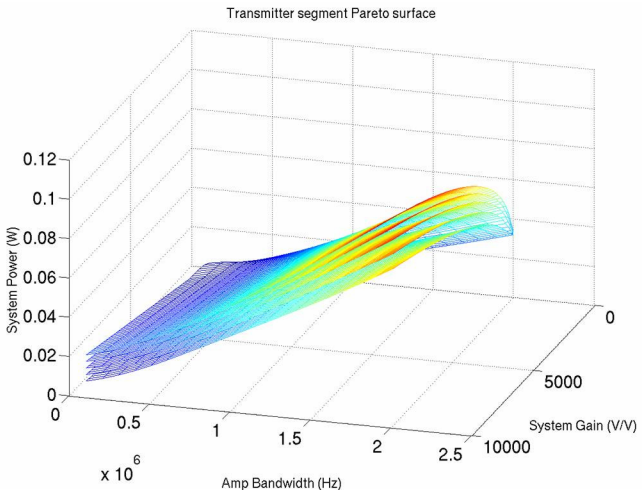
Over the last decade, the use of mixed-signal circuits on system-on-chip integrated circuits (IC) has increased at a steady rate. The challenges associated with large-scale analog system-level exploration, including early-stage tradeoff analysis, create the bottleneck for mixed-signal system design. Equation-based and simulation-based optimization techniques have been predominant in the exploration of a circuit's design space. However, these tools are practical only for small electronic systems. We show that this need not be a limitation by establishing a general design methodology for large systems. By decomposing a system into smaller, less complex building blocks, thereby adopting a Hierarchical, Bottom-up (H-BU) approach, we keep the problem tractable, and the tradeoff space can be constructed in a piecewise manner up to the system level. This idea is illustrated via a transmitter segment in Figure 1.

The H-BU methodology and a suitably chosen optimization framework (i.e., geometric programming) [1-2] coupled with an equation-based design philosophy and intended to provide an alternative analog IC system design process. Once the initial system decomposition is settled at the system level, each circuit designer produces a set of Pareto-optimal (PO) surfaces, to send to the system level designer for system level allocation. Whether a simulation- or equation-based approach is used in the generation of the surfaces, an equation-based approach should prevail at the system level. The reasons for using this approach are several: to eliminate the common convoluted use of spreadsheets and systematize a straightforward formulation strategy, as well as take advantage of the gentle surfaces, which are amenable to equation fitting. These surfaces fully describe the block-level space in an optimal sense. At the system level, the system designer can select the operating points for each block so as to optimally distribute the allocated resources. Moreover, fitting the PO surfaces into functions amenable to an MP allows the system designer to formulate a system level MP and to produce the PO surface characterizing the system over any range of interest. Figure 2 show a PO curve for the transmitter segment.

For large systems composed of many blocks, tradeoff information between the various blocks is of enormous value. The value of this information lies in readily exposed relations hidden underneath strong non-inearities, indirect parameter correlations, subsystem trans-coupling, and otherwise non-intuitive interactions between blocks. This information will allow designers to make the best decisions on how to choose optimal allocation of the available resources. Moreover, if each block is kept within a geometric programming framework, then each can be optimized efficiently. Regardless of adherence to a GP framework at the bottom-level, the system-level formulation is always amenable to GP.



▲ Figure 1: Hierarchical, bottom-up design methodology. By generating Pareto-optimal curves for each block, the system-level PO space can be created.



▲ Figure 2: A Pareto-optimal surface for transmitter segment.

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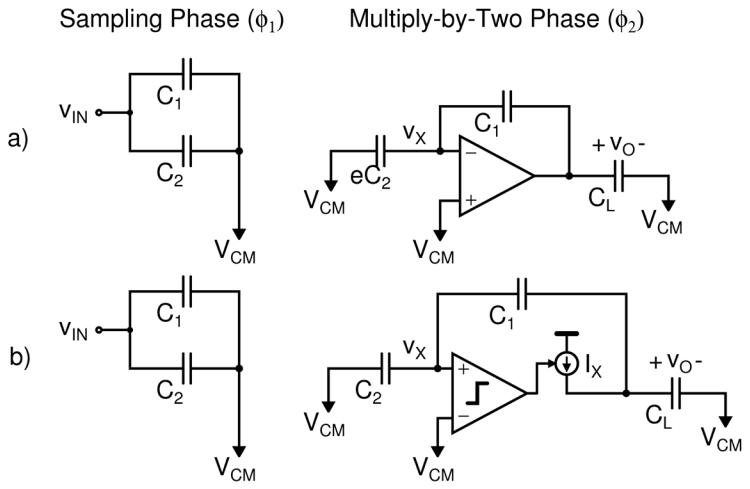
Comparator-based Switched Capacitor Circuits (CBSC)

J.K. Fiorenza, T. Sepke, P. Holloway, H.-S. Lee, C.G. Sodini
Sponsorship: SRC/FCRP C2S2, CICS

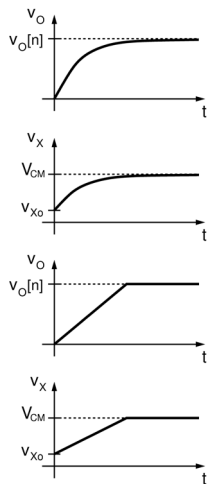
Two side effects of technology scaling that have a significant impact on analog circuit design are the reduced signal swing and the decrease in intrinsic device gain. Gain is important in feedback-based, analog signal processing systems because it determines the accuracy of the output value. Cascded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swings of scaled technologies. An alternative method for achieving high gain in an operational amplifier without reducing signal swing is to cascade several lower gain amplifiers. Nested-Miller compensation approaches [1] can be used to stabilize the cascaded feedback system, but the frequency response of the closed loop system is significantly sacrificed to ensure stability. In this project [2-3], a new comparator-based switched capacitor (CBSC) circuit design methodology has been explored that eliminates the use of op-amps in sampled data systems.

A sampled-data system typically operates in two phases, a sampling phase (ϕ_1) and a charge transfer phase (ϕ_2). An important property of these systems is that the output voltage needs to be accurate only at the moment the output is sampled. No constraint is placed on how the stage gets to the final output value. Feedback systems use a high-gain operational amplifier to force a virtual ground condition at the op-amp input. The top circuit in Figure 1a shows the conventional op-amp-based switched-capacitor gain stage. The circuit in Figure 1b shows the proposed CBSC approach, in which a comparator and a current source have replaced the op-amp. Assuming the comparator input V_x starts below the common-mode voltage at V_{xo}, the current source charges the output circuit until the comparator detects the virtual ground condition and turns the current source off. At this instant, the output is sampled on C_L. Because the CBSC design ensures the same virtual ground condition as the op-amp based design, both circuits produce the same output value at the sampling instant. This is demonstrated by waveforms for the two circuits shown in Figure 2.

The CBSC concept is general and can be applied to any sampled-data analog circuit. For example, the CBSC design approach can be applied to a pipelined ADC. A prototype 1.5b/stage CBSC pipeline ADC was constructed and operates similar to the op-amp version of the ADC. The prototype CBSC ADC was implemented in a 0.18μm CMOS technology. The active die area of the ADC is 1.2mm^2. At a 7.9MHz sampling frequency, the DNL is +0.33/-0.28LSB, and the INL is +1.59/-1.13LSB. It achieves an SFDR of 62dB, an SNDR of 53dB and an ENOB of 8.7b for input frequencies up to the Nyquist rate. The core ADC power consumption of all 10 stages of the pipeline converter is 2.5mW at a 1.8V power supply, resulting in a 0.8pJ/b figure of merit.



▲ Figure 1: (a) Traditional op-amp based multiply-by-two amplifier versus (b) proposed comparator-based multiply-by-two amplifier.



▲ Figure 2: Multiply-by-two waveforms.

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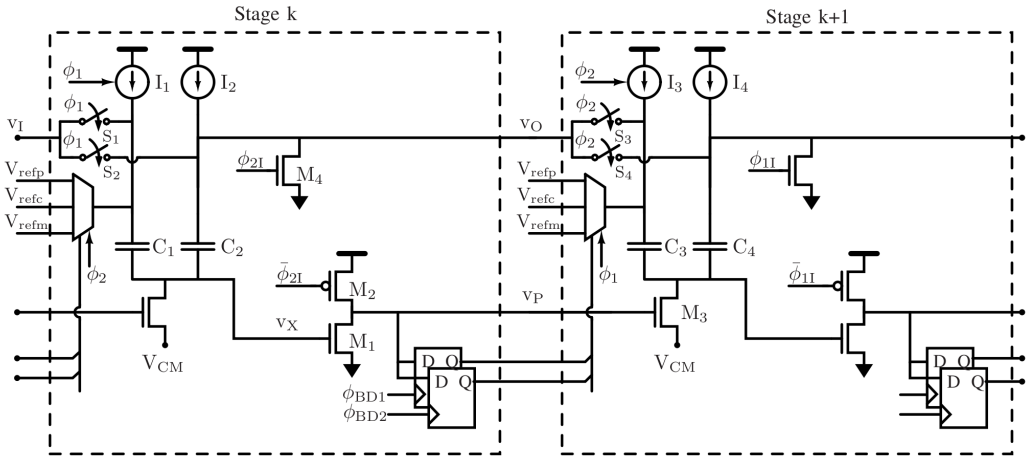
A Zero-crossing Based, 8b, 200MS/s Pipelined ADC

L. Brooks, H.-S. Lee
Sponsorship: NDSEG Fellowship, CICS

Technology scaling is creating significant issues for switched capacitor circuit design. Decreasing device gain and voltage supplies make traditional implementations of high-gain, high-speed operational amplifiers (op-amps) increasingly difficult and less power-efficient. A comparator-based switched capacitor (CBSC) circuit technique was introduced in [2] that replaces the functionality of an op-amp with a comparator and current source to help with these issues. The current source sweeps the output node with a voltage ramp until the comparator detects that the virtual ground condition has been realized. Whereas an op-amp-based implementation *forces* the virtual ground condition, CBSC circuits *detect* the virtual ground condition to realize the same precision charge transfer.

The comparator input in a CBSC implementation is a constant slope voltage ramp, and so the comparator performs a zero-crossing detection. This work generalizes CBSC by replacing the general-purpose comparator of CBSC circuits with a zero-crossing detector to realize new architecture called zero-crossing based circuits (ZCBC) [1]. Two stages of the implementation of the 1.5 bit/stage ZCBC pipelined analog-to-digital converter (ADC) are shown in Figure 1. Devices M_1 and M_2 make a dynamic zero-crossing detector that is fast, simple, and amenable to scaling. It draws no static current and thus realizes a power-efficient threshold detector. To improve linearity and output swing, the single current source of the previous design was split to create current sources I_1, I_2, I_3, and I_4. In this topology the capacitors are no longer charged through a series switch, so the associated nonlinear voltage drop is eliminated. Furthermore, the traditional bit decision comparators in a pipelined ADC have been replaced with bit decision flip-flops for improved speed.

To demonstrate these techniques, an 8b, 200MS/s ZCBC pipelined ADC was implemented in a 0.18-um CMOS technology in an active die area of $0.05mm^2$. The differential non-linearity (DNL) and integral non-linearity (INL) are $0.75LSB_8$ and $1.0LSB_8$. The measured effective number of bits (ENOB) is 6.4b. It consumes 8.5mW (2.9/5.6mW analog/digital) from a 1.8V power supply. It draws only dynamic CV^2f power as there are no statically biased circuits in the complete ADC. The corresponding figure of merit ($FOM=P/2f_{in}/2^{ENOB}$) is 510 fJ/step at 200MS/s. This demonstrates best-in-class performance in terms of power-efficiency among other published ADCs in its class.



▲ Figure 1: Two stages of the 1.5 bit/stage zero-crossing based pipelined ADC.

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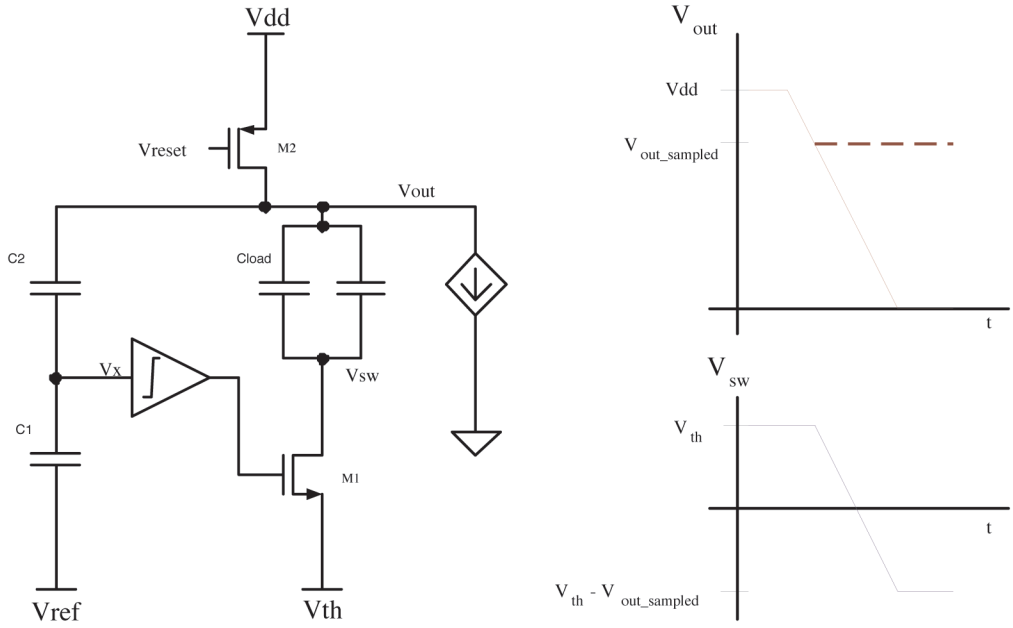
Ultra-high Speed A/D Converters Using Zero-crossing-based Circuits

A. Chow, H.-S. Lee
Sponsorship: SRC/FCRP C2S2

With an increasing need for higher data rates, both wireless applications and data links are demanding higher speed analog-to-digital converters (ADC) with medium resolution. In particular, this work will investigate ADC's with sampling rate up to 10 Gs/s with 6-8 bits of resolution. Time-interleaved converters achieve their high sampling rate by placing several converters in parallel. Each individual converter, or channel, has a delayed sampling clock and operates at a reduced sampling rate. Therefore each channel is responsible for digitizing a different time slice. This method requires that the individual converters, which make up the parallel combination, be matched. Mismatches and non-idealities, such as gain error, timing error, and voltage offset, degrade the performance. Therefore channel matching is an important design consideration for time-interleaved ADCs.

Although digital calibration can mitigate many of these non-idealities, timing mismatches are non-linear errors, which are more difficult to remove. At sampling rates up to 10Gs/s, digital calibration would consume a large amount of power. An alternative solution uses a global switch running at the full speed of the converter. This technique works well for medium-high speed ADC's [1-2]. At higher speeds the ability to turn the switch on and off at the full sampling rate becomes a major challenge. We will investigate the applicability of the global switch technique in 90- or 65-nm CMOS technologies for 10Gs/s operation.

Power optimization is a major design consideration when implementing a time-interleaved ADC. We will lower total power consumption by exploring innovative technologies for implementing the individual ADCs in the channel, such as the zero-crossing based circuits (ZCBCs) [3]. The ADC topology was previously presented. In particular, this work investigates a fast, single-slope architecture (Figure 1). The faster each channel operates, the fewer channels are needed, hence lowering power in clock and buffer circuits. The primary emphasis falls on the development of highly power-efficient single-slope ZCBC architecture. Since the single slope architecture is more sensitive to non-idealities such as ramp nonlinearity, we are carefully studying the sources of non-idealities and develop clever techniques to address the accuracy issues.



▲ Figure 1: One stage of a single-slope ZCBC-based pipelined ADC.

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High-accuracy Pipelined A/D Converter Based on Zero-crossing Switched Capacitor Circuits

M. Markova, P. Holloway, H.-S. Lee
Sponsorship: EECS Fellowship, CICS

Technology scaling poses challenges in designing analog circuits because of the decrease in intrinsic gain and reduced swing. An alternative to using high- gain amplifiers in the implementation of switched- capacitor circuits has been proposed [1] that replaces the amplifier with a current source and a comparator. The new comparator- based switched- capacitor (CBSC) technique has been implemented in two pipelined ADC architectures at 10MHz and 200MHz and 10bit and 8bit accuracy, respectively [1-2].

The purpose of this project is to explore the use of the CBSC technique for very high-precision AD converters. The goal of the project is a 100MHz 16 bit pipelined ADC. First, we are investigating multiphase CBSC operation to improve the power-linearity trade off of the A/D conversion [3]. We are also developing linearization techniques for the ramp waveforms. Linear ramp waveforms require fewer phases, thus allowing faster operation. Techniques for improving linearity beyond using a cascoded current source are explored. A linear ramp generator, which decouples the current source from the output ramp through a Miller capacitor is proposed to improve the linearity of the ramp waveform in all phases. This ramp generator improves the range by improving linearity through compensation of the gate-to-source voltage of the current source without the use of a cascode. In addition it lends itself to a symmetric differential implementation for the final phase to ensure adequate noise rejection. At the target resolution of 16 bits, power supply and substrate noise coupling can limit the performance. We are studying their effects in CBSC circuits. For reduced sensitivity to power supply and substrate noise, we are developing a differential CBSC architecture. Other techniques that we are presently developing include power-efficient offset cancellation in comparators and exploiting *a priori* information from previous stages in the pipeline structure to increase linearity and speed.

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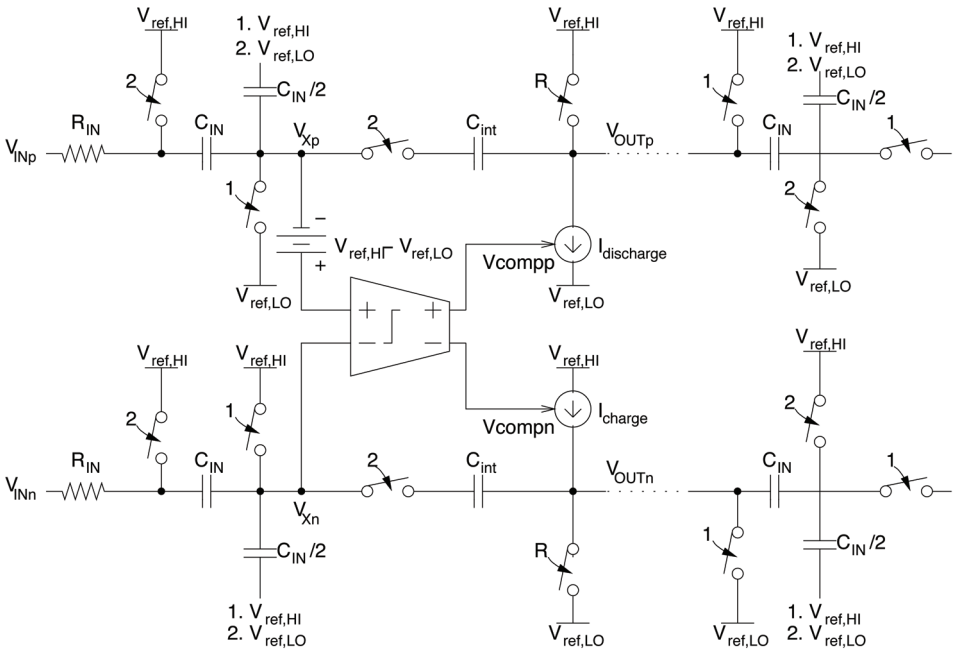
Low-voltage Comparator-based Switched-capacitor Sigma-delta ADC

M. Guyton, H.-S. Lee
Sponsorship: CICS, DARPA

Many analog signal-processing circuits use operational amplifiers (op-amps) in a negative feedback topology. The amount of error in these feedback systems is inversely proportional to the gain of the op-amp. Because scaled CMOS technologies use shorter channel lengths and require lower power supply voltages, it becomes more difficult to implement high gain op-amps. Recently, a comparator-based switched-capacitor (CBSC) technique was proposed [1] that uses a comparator rather than an op-amp to implement switched-capacitor topologies.

In this project, we investigate very-low-voltage delta-sigma converters. One of the biggest challenges of low-voltage circuits is the transmission gates that must pass the signal. If the signal is near the middle of the power supply range, neither the NMOS nor the PMOS transistor has sufficient gate drive to pass the signal properly. The switched-op-amp technique [2] was proposed to mitigate this problem. In this technique, the output of the op-amp is directly connected to the next sampling capacitor without a transmission gate to perform charge transfer. During the charge transfer phase, the op-amp is switched off, and the output is grounded.

Similar to the standard switched-capacitor technique, CBSC circuits use two-phase clocking, having both sampling and charge-transfer clock phases. Unlike a standard switched-capacitor circuit, in a CBSC circuit all current sources connected to the output node are off at the end of the charge-transfer phase. Therefore, there is no op-amp or current source to turn off to accommodate the charge transfer without a transmission gate. Thus, the CBSC technique is inherently better suited to low-voltage applications than switched-op-amp circuit topologies. Although the previous CBSC implementation was a single-ended version, many high-resolution systems require fully differential implementation for better power supply and substrate noise rejection properties. Since the CBSC is a new technique without an op-amp, existing fully differential circuitry cannot be applied. In this program, we are developing fully-differential CBSC topologies for applications in high resolution data conversion. Figure 1 shows a fully-differential low-voltage CBSC integrator stage using the combined techniques. We are designing a fourth-order sigma-delta ADC for operation at 1V power supply using this integrator stage.



▲ Figure 1: Fully-differential comparator-based switched-capacitor integrator. The input of the next integrator stage is also shown. Common-mode feedback circuits are not shown.

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Zero-crossing-based ADC for mm-Wave Applications

J. Chu, H.-S. Lee
Sponsorship: SRC/FCRP C2S2

In an mm-wave imaging system, the resolution depends on the phase accuracy of the signal. Our system design uses digital beam forming with extensive digital processing to reduce the phase variance and extract accurate phase information from an array of receivers. This design choice demands a high-speed, medium-resolution ADC to digitize the signal. Since there are up to 1000 receivers in the imaging system, each requiring 2 ADC's for in-phase and quadrature signals, the power consumption of each ADC is also a major constraint. We are investigating a time-interleaved ADC operating at 4 Gs/s with 8-10 bits of resolution with less than 50mW of power consumption. This work is also useful in many other applications including wireless and wireline communications.

Each individual channel will be implemented using a zero-crossing-based circuit (ZCBC) [1], which is an extension of the comparator-based switch-capacitor circuit (CBSC) design methodology [2]. The focus of the project is to explore novel circuit structures based on ZCBC to improve the FOM and power consumption of A/D converters. In particular, we are investigating the use of a dynamically biased zero-crossing detector. The idea is to use the most power when the signal is crossing the threshold; this extra power decreases the delay and reduces the noise. During the other times, power can be reduced without degrading the ADC performance.

Time interleaving will be used to achieve the speed requirement. In a time-interleaved structure, matching between the different channels will be very important to maintain the desired performance. Any mismatch in non-idealities such as gain error, offset, and timing errors can greatly degrade the performance. We plan to use a global sampling technique, which mitigates the timing errors [3-4]. Careful design and layout will be needed to reduce the other mismatches.

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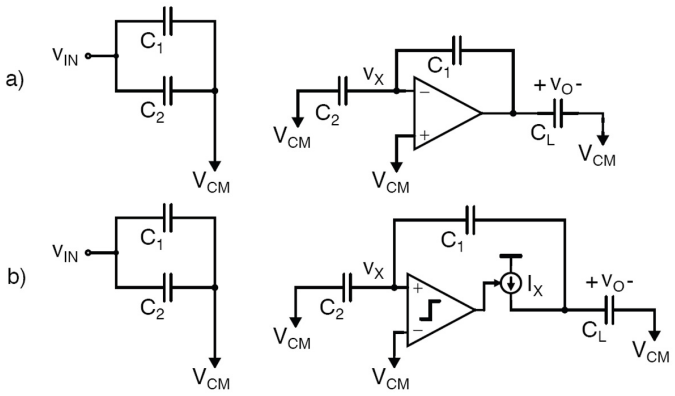
Comparator-based Circuits for HBTs

J. Feng, H.-S. Lee
Sponsorship: BAE Systems

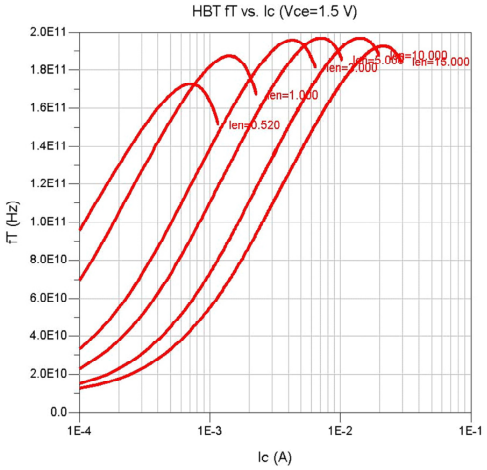
Recently, comparator-based switched-capacitor (CBSC) circuits and zero-crossing-based circuits (ZCBC) were introduced [1,2] as a viable alternative to op-amp-based circuits. The use of op-amps in analog signal processing circuits is becoming more difficult due to the decreased intrinsic device gains and reduced signal swings obtained in scaled CMOS technologies. Op-amps rely upon high gain in the negative feedback mode in sampled data systems because the gain determines the accuracy of the output value. CBSC and ZCBC-based circuits replace the op-amp using a comparator and a current source (see Figure 1), and therefore do not require high gain and stability simultaneously as in op-amp-based circuits. Since comparators can be designed without the use of complementary devices, these techniques can be applied to a variety of transistor technologies. In this work, we explore the use of heterojunction bipolar transistors (HBTs) in comparator-based circuits for sampled data systems.

HBTs offer much higher device speeds than CMOS devices and have demonstrated the fastest transistor speeds to date with cutoff frequencies as high as f_T=710 GHz using a pseudomorphic InGaAs/InP HBT [3]. Commercially, silicon germanium (SiGe) based HBTs have been developed with a cutoff frequency of f_T=200 GHz as shown in Figure 2. The faster device speeds that HBTs offer can help meet the demand for very high speed, high-resolution analog-to-digital converters (ADC) for various applications including wireless and wireline communications and radar systems. HBTs also have a more constant g_m/I ratio over the normal operating range, lower 1/f noise, and better device-matching of differential pairs than CMOS devices.

This project focuses on the development of innovative circuits and architectures to design a 12-bit pipelined ADC operating at 2 GHz using either an HBT-only or SiGe BiCMOS process. The first goal of the project is focused on adapting switched emitter-follower sample-and-hold circuits for switched-capacitor applications. Ultimately, the project will culminate in the design of a prototype ADC chip.



▲ Figure 1: (a) Traditional op-amp based multiply-by-two amplifier versus (b) comparator-based multiply-by-two amplifier.



▲ Figure 2: Unity cutoff frequency f_T vs. collector current at V_{CE}=1.5 V for 0.12 µm width SiGe HBT at different device lengths.

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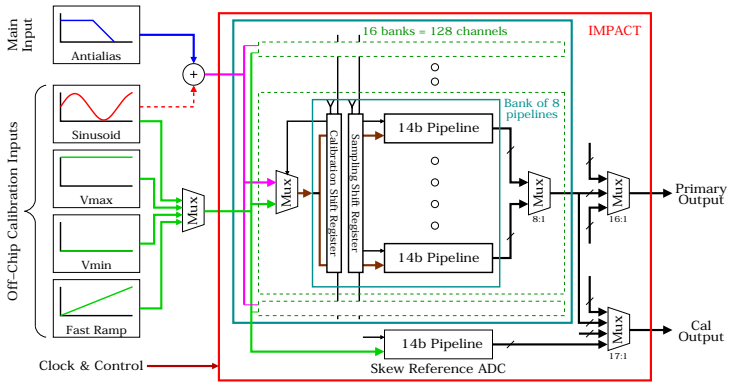
Massively Parallel ADC with Self-calibration

M. Spaeth, H.-S. Lee
Sponsorship: CICS

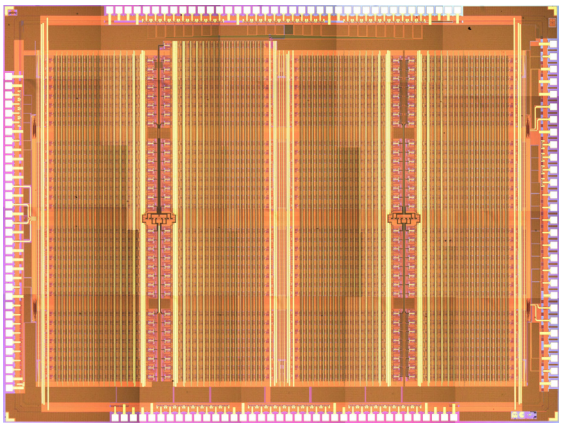
In this program we are developing an analog-to-digital converter (ADC)that can quantize a wideband 150-MHz signal at 600 mega-samples per second, with signal-to-noise ratio and linearity in excess of 75dB (12-bits). Use of a massively parallel, time-interleaved architecture with 128 active ADC channels reduces the requisite speed for each channel and enables the devices to be biased in the sub-threshold region for an extremely low-power (<50mW, core) solution. In a parallel time-interleaved system, any mismatches between channels result in undesired spurious tones. Most existing time-interleaved ADCs either employ a low degree of parallelism, such that the tones appear outside the signal band, or are low enough in resolution that the tones are below the quantization noise floor. In this design, however, all inherent gain, offset, and timing skew mismatches must be calibrated away to achieve the stated high-performance goals.

The 128 14-bit pipeline ADCs are arranged into 16 blocks of 8 channels each, as shown in Figure 1. The hierarchal organization of the design allows individual blocks to be pulled out for background calibration, while the remaining blocks continue to quantize the input signal. Due to the large number of channels to be calibrated, the calibration algorithm must be simple but effective. The sub-radix-2 calibration algorithm [1-2] is very effective in removing offset and linearity errors but poses a challenge due to the complexity when applied to the massively parallel converter. We have modified the algorithm to allow nominal radix-2 operations to be employed, for similar calibration efficiency with reduced complexity. We are also exploring several innovative techniques to calculate and remove systematic timing skew between channels. An additional channel is included in the design to act as a timing reference for some of the timing skew measurement algorithms. A novel token-passing control scheme is used to generate local clock phases for the individual blocks and channels, minimizing the number of clock lines that must be routed across the chip.

The design was fabricated in a 0.18-µm digital CMOS process by National Semiconductor and is currently under test. A micrograph of the finished chip is shown in Figure 2.



▲ Figure 1: Top-level block diagram of the IMPACT ADC architecture.



▲ Figure 2: Micrograph of the fabricated chip.

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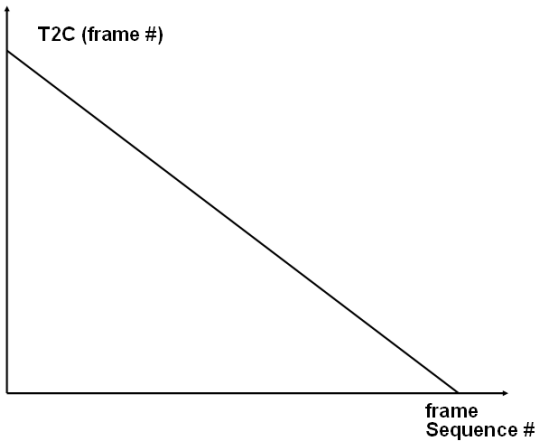
Prediction of Time-to-contact for Intelligent Vehicles

Y. Fang, B.K.P. Horn, I. Masaki
Sponsorship: Intelligent Transportation Research Center

The time-to-contact (TTC) is the time it takes two objects to touch if they continue in their current trajectory. The TTC estimation based on video sequences from single camera provides a simple and convenient way to detect approaching objects, andpotential danger and to analyze surrounding environment for automotive and robotic applications. Most current TTC estimation methods depend on the computation of the optical flow as an intermediate result by tracking "interesting feature points" over multiple images [4-6]. However, the optical flow estimation itself is very noisy [1-2], especially when motion between two continuous frames is large. The TTC estimation based on optical flow takes advantage only of information about moving object boundaries. Thus the estimation accuracy and robustness are very noisy. We propose a new direct "gradient-based" method [3,7-9] to determine TTC that operates directly on the spatial and temporal derivatives of brightness. The proposed method does not depend on "feature detection" and thus does not require careful calibration of the optical system. The new method enhances robustness and is computationally efficient, which is especially important to provide fast response for vehicle applications. The results of TTC estimation present an expected trend as in Figure 1 and show the robustness to parameter choices. Figure 2 shows the intermediate results of TTC calculation process for one video sequence.



▲ Figure 1: Typical time to contact for most applications. The vertical axis shows the number of frames before contact will happen for different frames in a frame sequence.

▲ Figure 2: The TTC calculation process for one video sequence. The circle represents the focus of expansion with coordinate at the bottom right corner. The three bars represent the relative speed between camera and object. The TTC value is at the upper left corner of each image.

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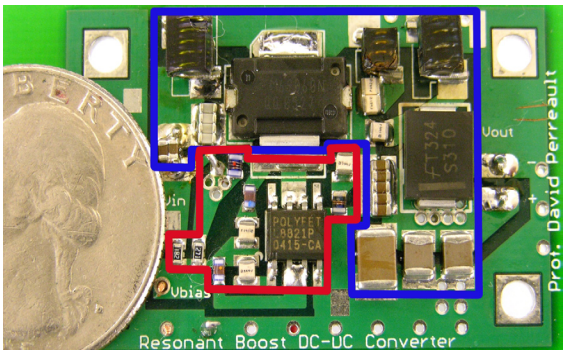
Very High-frequency DC-DC Boost Conversion

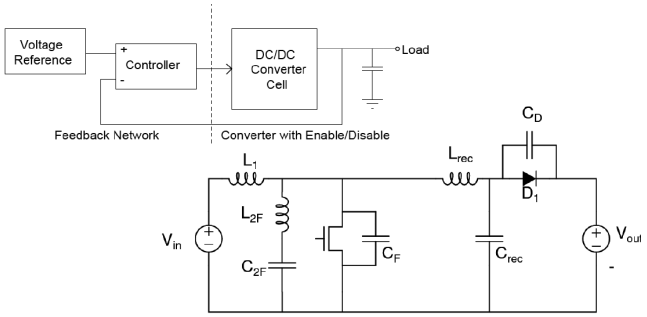
A. Sagneri, R. Pilawa, D. Perreault
Sponsorship: MIT/Industry Consortium on Advanced Automotive Electrical/Electronic Components and Systems, NSF, National Semiconductor, CICS

At current switching frequencies (about 1-10 MHz), the required energy storage in a typical dc-dc converter yields passive component dimensions that are large with respect to integrated processes. Shrinking these components at constant energy storage results in an unacceptable efficiency penalty. Larger size accompanies greater cost, both because more material is required and because batch processing is more complicated. This is especially true of magnetic materials, where deposited materials exhibit relatively poor characteristics and add significant cost. On the other hand, continually improving semiconductor devices is a key enabler in the focus of this research—to explore converter operation in the very high frequency (VHF, 30-300 MHz) regime. At VHF, reduced energy storage translates directly to smaller passive components. Significantly, air-core inductors can be implemented in a small volume. These components are simple, small, and ready for batch fabrication. Further, without the frequency dependent loss of a magnetic core, passive components no longer limit switching frequency. The other loss mechanisms—switching and gating loss—are dealt with through resonant circuit techniques. The resulting dc-dc boost converters shown here are capable of nominal power levels above 20 watts and efficiency in excess of 87% while switching at 110 MHz (Figure 1).

The circuit topology in Figure 2 consists of a resonant Φ_2 inverter coupled to a resonant rectifier [1,3-5]. The result is a resonant dc-dc boost converter operating at VHF (Figure 1). The inverter uses wave-shaping to minimize peak voltage stress (about 2.3 V_{IN}) [1], in this case staying within typical integrated power process breakdown voltage limits (50 V) for input voltage over the automotive range (8-18 V). A 110-MHz converter using a commercial MOSFET achieved greater than 87% efficiency. The converter nominally supplies 23 W output power, over an 8-18 V input range and a 22-33 V output range. A 50-MHz converter using a MOSFET fabricated in an integrated power process achieved 75% efficiency over the same voltage ranges with a 19 W nominal output power. The largest inductors in each design are 33 nH and 56 nH, respectively. Both converters use resonant gate drives for high efficiency and operate in bang-bang modulation under hysteretic voltage mode control [3-4,6]. This control scheme takes advantage of exceptional transient performance to achieve wide load range at high efficiency [2]. Greater load range can be achieved by adding more cells. Current work focuses on designing optimal devices for a given power process and co-packaging of passive components.



▲ Figure 1: Picture of a 110 MHz dc-dc boost converter. Vin: 8-18V, Vout: 22-33V, Pnom: 23W, efficiency: 87%.



▲ Figure 2: A VHF dc-dc boost power stage and control scheme. The dc-dc converter cell is modulated by a hysteretic controller ~ 200 kHz while the cell switches ~100 MHz. Ripple is set by the hysteresis band. Power and ripple requirements size the bulk output capacitor.

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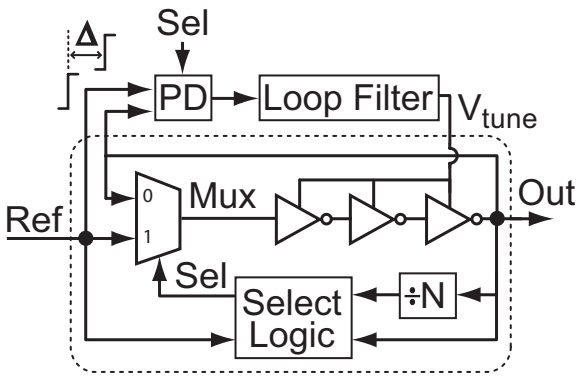
Techniques for Low-jitter Clock Multiplication

B.M. Helal, M.H. Perrott

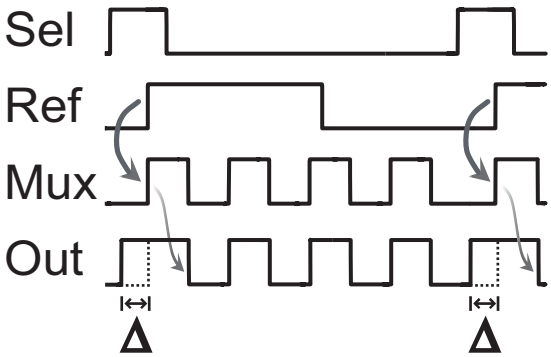
High-frequency clocks are essential to high-speed digital and wireless applications. The performance of such clocks is measured by the amount of jitter, or phase noise, their outputs exhibit. Phase-Locked Loops (PLLs) are typically used to generate high-frequency clocks. However, a major disadvantage of PLLs is the accumulation of jitter within their Voltage Controlled Oscillators (VCOs) [1]. Multiplying Delay-Locked Loops (MDLLs) have been introduced recently to significantly reduce the problem of jitter accumulation in PLLs and reject VCO phase noise at a higher bandwidth than possible with PLLs [2-3].

Jitter accumulation is reduced in an MDLL by resetting the circulating edge in its ring oscillator using a clean edge from the reference signal. The Select-logic circuitry commands the multiplexer, using the Sel signal, to pass the reference edge instead of the output edge at the proper time, as shown in Figure 1. The major disadvantage of a typical MDLL is static delay offset, which causes its output to exhibit deterministic jitter and reference spurs. Static delay offset is caused mostly by path and current mismatches in the phase detector and charge pump, respectively [2-3]. When the VCO is not perfectly tuned, the last output edge and the reference edge that replaces it occur at a time offset, causing an inconsistent transition time. Figure 2 illustrates the problem of static delay offset in a locked MDLL, showing a deterministic jitter of Δ seconds peak-to-peak.

A digital correlation technique was developed to eliminate sources of analog mismatches and drastically reduce static delay offset in MDLLs, thereby allowing their use in applications that require low-jitter, high-frequency clocks. A test chip was fabricated using a CMOS 0.13μm process. A highly-digital MDLL prototype, which used a scrambling time-to-digital converter, generated a 1.6GHz output from a 50MHz reference input. Measured results demonstrated reference spurs below -59 dBc and estimated random and deterministic jitter below 1 ps [4].



▲ Figure 1: Classical MDLL block diagram.



▲ Figure 2: Timing diagram illustrating the effect of static delay offset.

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A Digitally-enhanced Delta-sigma Fractional-N Synthesizer

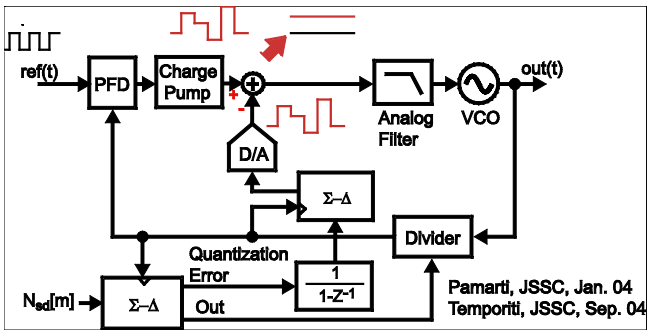
C.-M. Hsu, M.H. Perrott
Sponsorship: SRC/FCRP C2S2

Recent advances in frequency synthesizer architectures have formed the groundwork for a very exciting and active area of research. On the one hand, the need for a wider-bandwidth fractional-N synthesizer has inspired researchers to develop phase noise cancellation techniques to avoid tradeoffs between noise performance and synthesizer bandwidth [1], as shown in Figure 1. On the other hand, the continuing development of the deep submicron CMOS process has initiated people's interest in all-digital phase locked loop (PLL) [2], which not only leverages the high-speed digital capability available in a deep submicron process but also avoids the problems those a conventional charge-pump PLL may encounter, such as high variation and leakage current. The work in [2] demonstrated that an all-digital synthesizer can meet GSM specifications, but the need of a strong DSP capability and a complicated VCO structure prevents it from being a simple solution for many applications. In addition, the bandwidth of [2] is ten times lower than that achievable by analog techniques [1]. Therefore, the goal of this research is to find a digital synthesizer solution that not only is simpler than [2] but also can achieve a high bandwidth comparable to the analog approach [1].

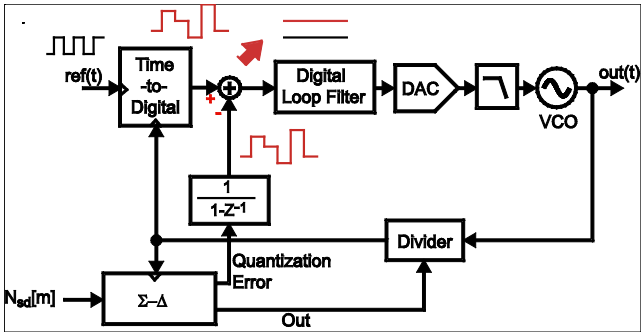
The high in-band phase noise due to the quantization noise of the time-to-digital converter (TDC) in [2] limits the PLL bandwidth to roughly 40 kHz. Recently, a new TDC architecture introduced in [3] demonstrated the possibility of first-order noise shaping the TDC quantization noise. This technique shows the potential to achieve <-110 dBc/Hz in-band phase noise, according to simulation results. With such a low in-band noise floor, we are able to extend the PLL loop bandwidth to roughly 400 kHz without violating the GSM mask.

The digital controlled oscillator proposed in [2] requires a large, fine-resolution switched capacitor bank, which is a challenging design. An alternative in [4] combines a digital-to-analog converter (DAC) and a conventional analog LC voltage-controlled oscillator into a DAC-controlled oscillator. However, the resistor-string DAC used in [4], which offers an easy implementation, will not support dynamic element matching techniques (DEM). Applying DEM to remove the resistor mismatching is critical, since the DAC nonlinearity will fold MASH quantization noise to low-frequencies and thereby overwhelm the benefit of our low-phase-noise TDC. Therefore, we modified the resistor-string DAC into another form that enables us to apply DEM technique easily. Just as with the design in [4], this DAC does not require an analog buffer or an op-amp.

By combining the techniques stated above, we expect to achieve a 400-kHz bandwidth digitally-enhanced fractional-N synthesizer with a carrier frequency of 3.6 GHz, which is an order of magnitude higher than offered by [2]. Figure 2 illustrates the block diagram of our architecture. Behavior simulation verifies that the proposed architecture can still meet GSM mask even with the high bandwidth.



▲ Figure 1: Conventional phase cancellation fractional-N synthesizer.



▲ Figure 2: Proposed digital enhanced phase cancellation fractional-N synthesizer.

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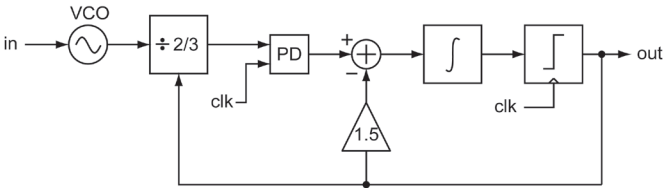
Voltage-controlled Oscillator-based A/D Conversion

M. Park, M.H. Perrott
Sponsorship: NSF

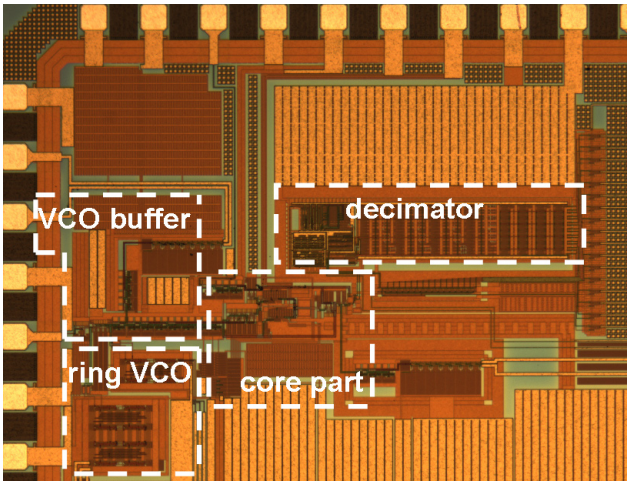
There has recently been increasing interest in developing highly digital analog-to-digital converter (ADC) structures for on-chip testing and ease of integration in future CMOS processes. An intriguing circuit to utilize in such cases is a ring oscillator voltage-controlled oscillator (VCO), which outputs a clock waveform whose frequency is a function of an input tuning voltage. By comparing the clock frequency to that of a separate clock reference using digital counters, one can create an all-digital A/D converter that can be readily utilized for on-chip monitoring of supply voltage variations and other on-chip waveforms [1-2]. A shortcoming of the approach in [1] is that the effective conversion rate must be quite low to achieve high resolution, and the shortcoming of the approach in [2] is that the overall A/D implementation ends up being primarily analog in nature.

In this project, we propose a VCO-based A/D converter structure, which allows second-order Σ– noise shaping to be achieved with a highly digital structure. We suggest the use of a primarily digital structure that is augmented by a small amount of low-performance analog circuitry to achieve the higher-order noise shaping. Figure 1 shows the proposed second-order ∑-Δ ADC architecture using a VCO as a first-stage integrator. The VCO and the dual-modulus divider form a feedback path. A second-stage integrator consists of the charge pump and the capacitor.

The prototype chip was fabricated in a 0.18-μm CMOS process. Figure 2 shows the die photograph. The fabricated ADC achieves 60 dB SNR over 1 MHz bandwidth with a sampling rate of 800 MHz, and the quantization noise is second-order noise-shaped. The highly digital architecture makes it possible to realize ADCs with only a small number of analog circuits, and it could potentially be useful for on-chip signal monitoring for ASIC chips, especially in the future CMOS technology.



▲ Figure 1: Proposed second-order Σ–Δ ADC employing a VCO.



▲ Figure 2: Die photograph of prototype IC.

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A ΣΔ ADC with Noise-shaping VCO Quantizer and DEM Circuit

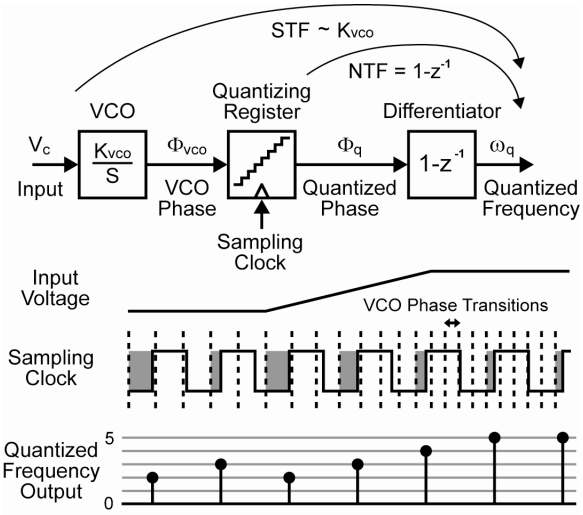
M. Straayer, M.H. Perrott
Sponsorship: Lincoln Laboratory

A combined 5-bit, 1st order noise-shaped quantizer and dynamic element matching (DEM) circuit running at 950 MHz based on a multi-phase voltage controlled oscillator (VCO) is presented. This quantizer structure is the key element in a 3rd-order noise-shaped analog-to-digital converter (ADC) with 2nd order loop dynamics and a single op-amp.

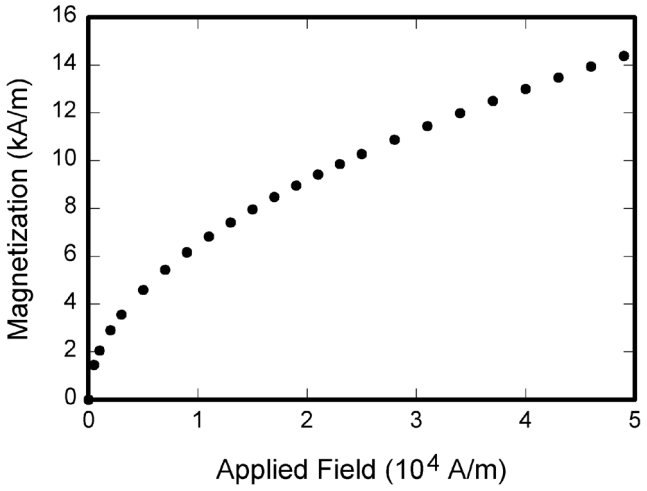
Figure 1 shows the basic operation of the multi-phase VCO-based quantizer. In this circuit, the VCO integrates an input voltage into a phase, and a digital quantizing register captures the phase state of the VCO. The quantization is particularly efficient due to the digital form of the ring oscillator. When the quantized phase is differentiated, a digital output proportional to the input voltage results. However, because the quantization error is also differentiated, the VCO-quantizer achieves first-order noise-shaping.

To improve the linearity and quantization noise performance of the converter, a sigma-delta feedback loop is formed with second-order loop dynamics. Figure 2 shows a simplified block diagram of this architecture. Interestingly, the rotation of the VCO phase can be utilized to perform dynamic element matching on the feedback DAC elements.

The authors wish to acknowledge MIT Lincoln Laboratory for research support through the Lincoln Scholars Program.



▲ Figure 1: Magnetization as a function of applied field.



▲ Figure 2: Magnetization as a function of applied field.

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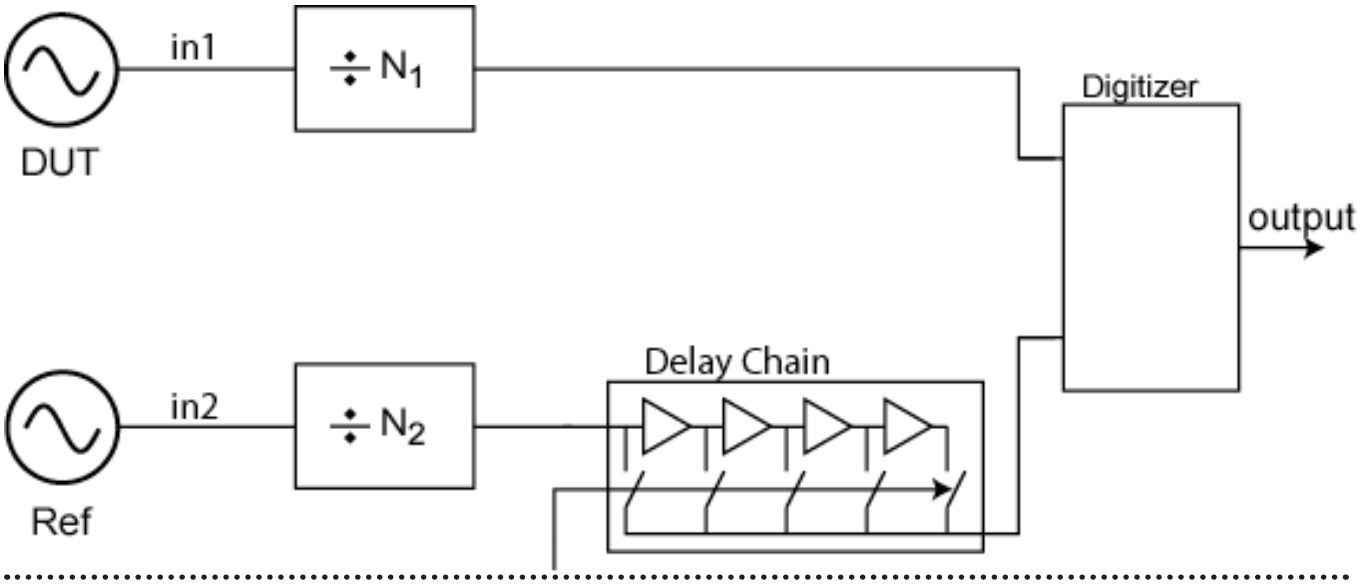
A Sub Picosecond Time-to-digital Converter for On-chip Jitter Measurement

K. Johnson, M.H. Perrott
Sponsorship: SRC/FCRP C2S2

Digital chip clock distribution consumes a major portion of the chip power budget. On-chip jitter and phase noise measurement promises the ability to control the jitter and power consumption in real-time. Current on-chip jitter measurement systems measure either a histogram with fine resolution [1] or transient jitter using a time to digital converter (TDC) with coarser resolution [2]. A finer resolution TDC would result in a single circuit that satisfies both purposes.

In a related application space, recent innovations in frequency synthesizers [3] make increased use of digital components including a TDC as a phase detector. The resolution of the TDC sets an upper limit on the bandwidth of the frequency synthesizer. A finer resolution TDC would result in lower in-band phase noise, wider bandwidth, and greater frequency agility.

Our architecture uses dividers and delay stages to present the delay to the digitizer (Figure 1). The remainder of the system is discrete time. Our work has a time resolution below the minimum inverter delay. All signals are full-swing digital signals with no information stored as low-frequency analog voltages to increase immunity to supply noise. The architecture is suitable for digital standard cells, which allows for simple migration as technology scales.



▲ Figure 1: A TDC converter architecture. The dividers and the delay chain present edges to the digitizer.

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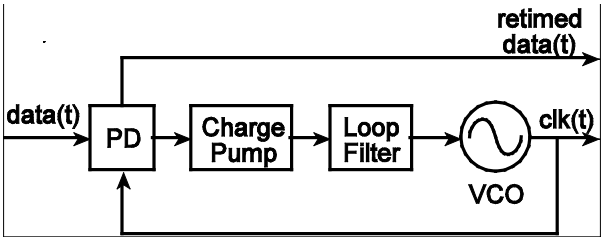
Techniques for Highly-digital Implementation of Clock and Data Recovery Circuits

C. Lau, M.H. Perrott
Sponsorship: SRC/FCRP C2S2

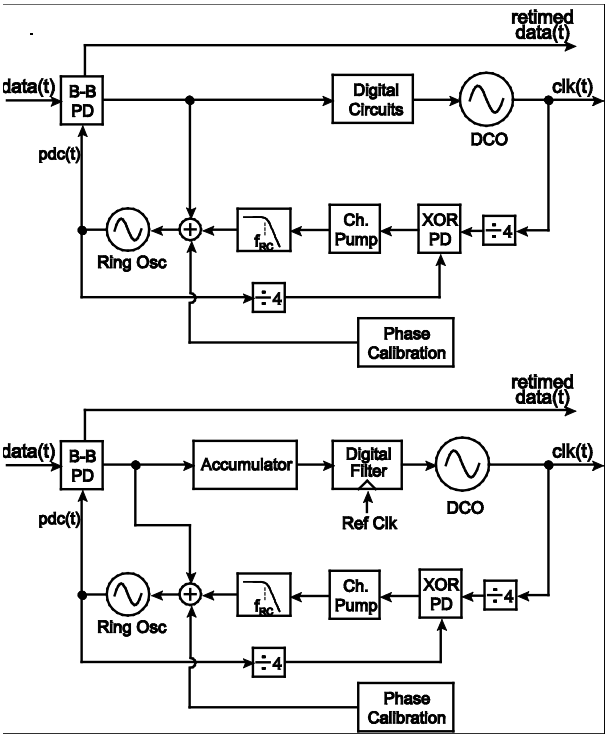
A clock and data recovery (CDR) circuit is an essential building block in a chip-to-chip communication system. Its key functions are to extract the clock signal and retime the data from an incoming non-return to zero (NRZ) data stream. As shown in Figure 1, conventional designs of CDR circuits typically employ a phase-locked loop (PLL), which consists of analog components such as a phase detector (PD), charge pump, loop filter, and voltage controlled oscillator (VCO). Although this analog implementation works well in most modern applications, we have started to see its limitations as we migrate to deep-submicron CMOS IC processes. For example, this analog system relies on low-leakage capacitors to hold values when the phased-locked loop is locked. The input of the VCO must be held stable in order to minimize frequency drift and jitter in the recovered clock. However, as the leakage current problem worsens in new generations of CMOS process, it demands a great deal of power and chip area to maintain not only the CDR's performance but also its functionality.

In view of the above challenge, it would be useful to pursue a new mixed-signal CDR architecture that minimizes its analog content and takes advantage of digital circuits. In line with this goal, recent research on digitally-controlled oscillators (DCOs) has demonstrated the feasibility of achieving fine resolution in frequency synthesis through digital control [1]. Therefore, we propose a highly-digital CDR circuit that leverages digital circuits, as shown in Figure 2. We use a bang-bang phase detector to generate error pulses of fixed width, which are then directly treated as digital signals in the subsequent digital blocks in the major loop. In this way, we can preserve the digital nature in the control path to the DCO, thus alleviating the need for high-performance, low-leakage analog components. We also utilize a simple analog feedback loop to linearize the bang-bang phase detector's nonlinear dynamics. Simulation results show that the achievable recovered clock jitter is around 2ps RMS and verify that this architecture meets the OC-48 SONET specification. This design has been implemented in the 0.18-um CMOS process and is being tested.

We acknowledge National Semiconductor for providing the fabrication services.



▲ Figure 1: A conventional CDR architecture.



▲ Figure 2: The proposed digital CDR architecture.

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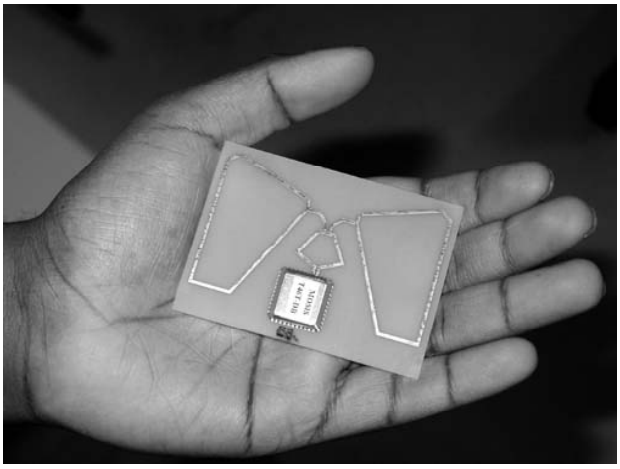
Low-power CMOS Rectifier Design for RFID Applications

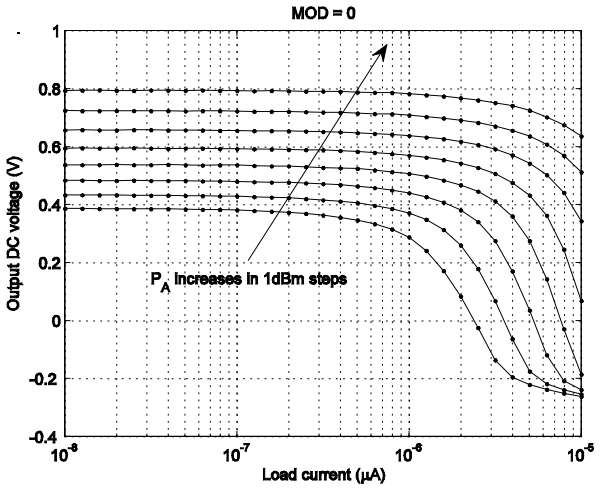
S. Mandal, R. Sarpeshkar
Sponsorship: Symbol Technologies

We have developed a general theory for far-field RF power extraction (or harvesting) systems. Such systems consist of an antenna and impedance-matching network that capture and efficiently transfer radiated RF power to a rectifier that converts it to DC for powering other circuits [1]. We have studied how fundamental physical relationships that link the operating bandwidth and range of such systems are related to technology-dependent quantities like transistor threshold voltage and parasitic capacitances. An important conclusion is that major improvements in rectifier efficiency are possible when advanced CMOS processes are used to fabricate them. The availability of high-Q capacitors and transistors with lower gate resistance, threshold voltage and parasitic capacitances, i.e., higher fT, in such processes proves to be crucial.

We have used our theory to accurately model far-field power extraction systems for passive RFID tags operating at UHF (850-950MHz). Efficient planar antennas, coupled resonator impedance matching networks and low power all-MOS rectifiers fabricated in standard CMOS technologies (0.5μm and 0.18μm) have been individually designed and later combined to form complete power extraction systems. One of our systems was found to have power-up thresholds of 6μW±10% (at 1μW load) and 8.5μW±10% (at 2μW load) while operating around 950MHz, closely matching values predicted by theory (5.2μW and 8μW, respectively). These low values of the power-up threshold allow the operating range of passive RFID tags to be extended without increasing the transmitted power. As far as we know, our experimental results constitute the best performance reported from a far-field power extraction system built in standard CMOS to date.



▲ Figure 1: Photograph of completed power extraction system. The planar antenna and impedance-matching network occupies most of the area. The packaged chip containing the MOS rectifier is also visible.



▲ Figure 2: Measured load curves of the power extraction system. The load current was varied from 10nA to 10μA for available power levels PA ranging from -24.7±0.5dBm (3.4μW±10%) to -17.7±0.5dBm (17.2μW±10%).

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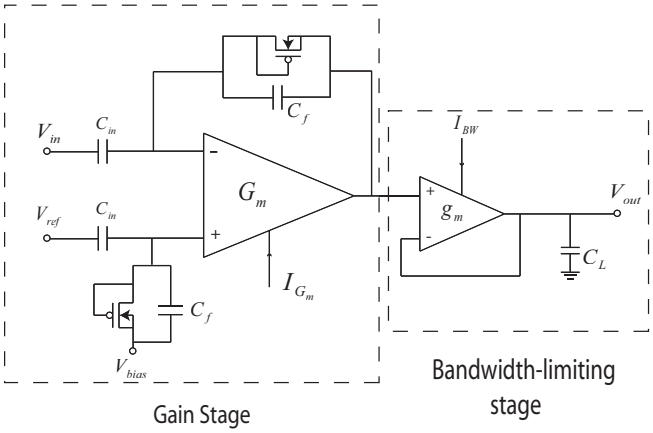
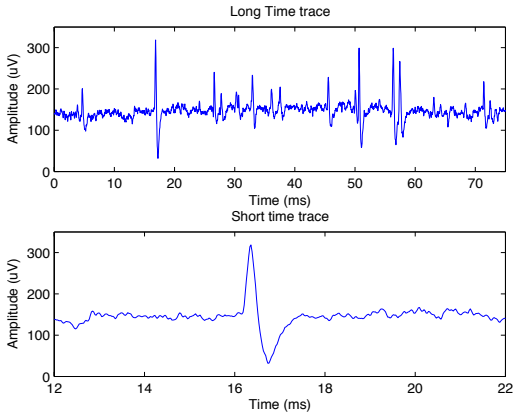
Low-power Circuits for Brain-machine Interfaces

R. Sarpeshkar, W. Wattanapanitch, B.I. Rapoport, S.K. Arfin, M.W. Baker, S. Mandal, M. Fee, R.A. Andersen, S. Musallam

This work involves the development of ultra-low-power circuits for brain-machine interfaces with applications for paralysis prosthetics, prosthetics for the blind, and experimental neuroscience systems. The circuits developed include a micropower neural amplifier with adaptive power biasing for use in multi-electrode arrays (Figure 1); an analog linear decoding and learning architecture for data compression; radio-frequency (RF) impedance modulation for low-power data telemetry; a wireless link for efficient power transfer; mixed-signal system integration for efficiency, robustness, and programmability; and circuits for wireless stimulation of neurons. Experimental results have been obtained from chips that have recorded from and stimulated neurons in the zebra-finch brain (Figure 2) and from RF power-link systems. Circuit simulations have also successfully processed prerecorded data from a monkey brain and from an RF data telemetry system.



▲ Figure 1: The adaptive micropower neural amplifier circuit.



▲ Figure 2: Recordings obtained from the RA region of a zebra-finch brain using the amplifier circuit shown in Figure 1.

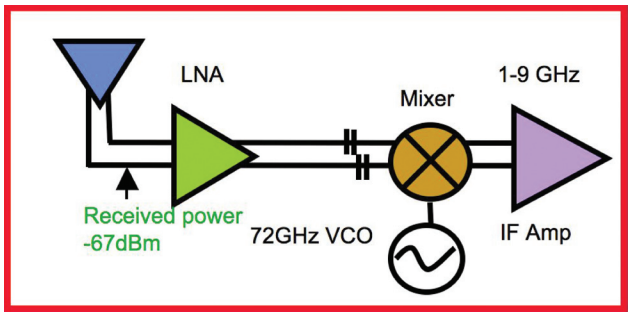
A 77-GHz Receiver Front-end for Passive Imaging

J.D. Powell, H. Kim (Lincoln Laboratory), C.G. Sodini
Sponsorship: SRC/FCRP C2S2, Lincoln Laboratory

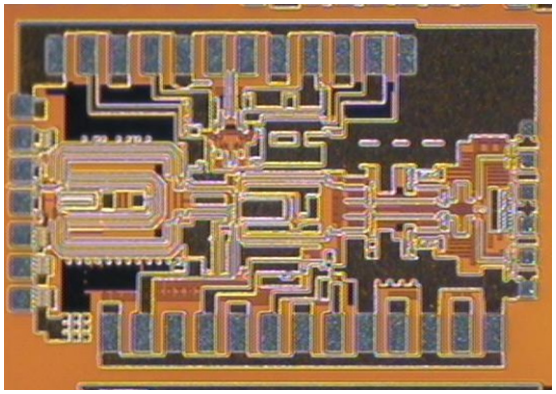
The area of Millimeter-Wave (MMW) system research and design has become increasingly popular in recent years, as advanced silicon processes have enabled integrated circuit operation in the MMW regime. The SiGe process features 200+ GHz f_T, including fully modeled passive elements. Several applications exist for MMW design, including wireless communications at 60-GHz, collision-avoidance radar imaging at 77-GHz, and concealed weapons detection imaging at 77-GHz and higher. Significant advances have been made in these areas using SiGe technology [1]. This research will focus on a passive imager front-end that has been developed and tested for the application of concealed weapons detection.

The Passive Imager enables detection of concealed weapons, given that they are composed of materials that possess emissive properties that contrast with those of the human body. The integrated Passive Imager operates from 73-81 GHz. Compared with current mm-wave research, this system is a wideband receiver that is fully differential, which allows many receivers to be tightly packaged in an array for the passive imager. The Passive Imager RF Front-End is composed of a low noise amplifier (LNA) tuned to the RF frequency band of 73-81 GHz; a double-balanced mixer, which down-converts the RF frequency to the intermediate frequency (IF) range of 1-9 GHz; and an on-chip cross-coupled voltage controlled oscillator (VCO), which provides a local oscillator frequency of 72 GHz. The LNA is a two-stage independently biased cascode design, which achieves 4-6 dB NF, 20-26 dB gain, and excellent impedance matching. The mixer design is a double-balanced Gilbert cell with IF amplifier. The stand-alone mixer has a broadband 180° hybrid at LO and RF input ports for testing purposes. The mixer achieves 12-14 dB NF, 20-26 dB conversion gain and P1dB of -26 dBm. The VCO core is a cross-coupled pair incorporating capacitive coupling and independent base biasing. The capacitors in feedback act as capacitive dividers and enable higher output power from the VCO core, as well as a substantially higher output frequency. The VCO achieves output power of -2 to 0 dBm, center frequency of 72-GHz and phase noise of approximately -93 dBc/Hz.

The Passive Imager RF Front-End block diagram is shown in Figure 1. The integrated chip, implemented in 0.13-um SiGe, is shown in Figure 2. It achieves particularly impressive conversion gain for wide-bandwidth applications, with approximately 46-36 dB conversion gain and 7-10 dB NF from 1-9 GHz. The P1dB is approximately -38 dBm at 76 GHz RF.



▲ Figure 1: Block diagram of RF front-end.



▲ Figure 2: Die photo of front-end receiver composed of the LNA, VCO and mixer.

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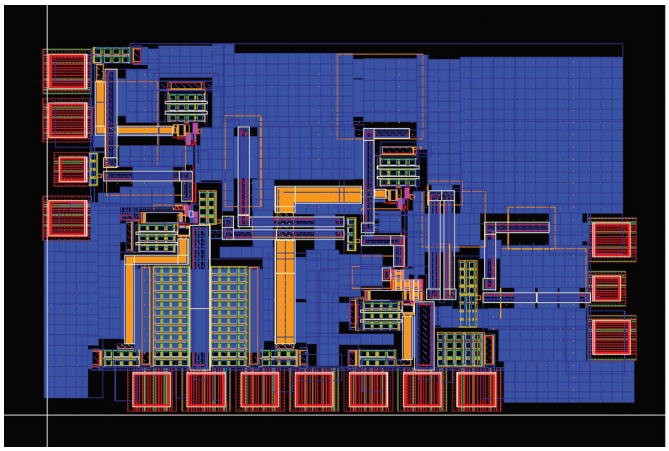
Power Amplifier Design for Millimeter-wave Imaging

K.M. Nguyen, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

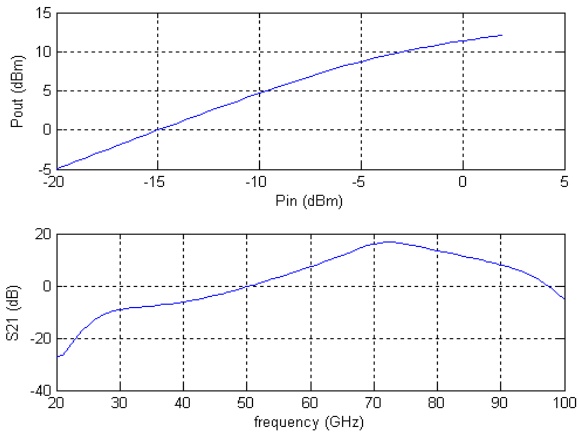
This research investigates the challenges of designing a power amplifier (PA) that could be used in a millimeter-wave (MMW) imaging system. A 130-nm SiGe BiCMOS process was used to develop an understanding of the specification limits. At MMW frequencies, the operating frequencies are pushing towards the f_T (200 GHz) of the devices. Furthermore, the low breakdown voltage of the bipolar devices limits the voltage swing and output power of the PA. To overcome this, a cascode topology was used in which the DC base resistance of the cascode transistor was reduced to increase the breakdown voltage of the transistor and allow more voltage swing. The reduced Miller effect from the cascode gave an increase in power gain.

A simulation study was conducted to determine the device parameters that limited the performance of MMW PAs. The operating frequency was pushed to 120 GHz, and a nominal PA was designed and simulated. Parameters within the model file were systematically changed, and the nominal PA was redesigned to compensate for the adjusted parameters. The change in performance could be attributed to the specific parameter. We found that the most significant parameters were the intrinsic and extrinsic base-collector capacitances rather than the base transit time. This showed that reducing the line widths of the bipolar devices provides greater gains in PA performance than reducing the base widths.

A test chip was submitted for fabrication in December 2006. Due to limitations of available test equipment, the operating frequency was reduced to 110 GHz. Using a 2-stage cascode design, the PA achieves a simulated maximum output power of 10.7 dBm and 6.7 dBm 1-dB compression point. The maximum power added efficiency is 5.1%, and it has a 13.6 dB power gain. Figure 1 shows a 77 GHz PA that was submitted for fabrication in January 2007 using a topology similar to the 110 GHz design. Simulation results of this PA are shown in Figure 2. It shows a maximum output power of 12 dBm and an 8.1 dBm 1-dB compression point. The maximum power added efficiency is 6.0%, and it has a 15-dB power gain at 77 GHz.



▲ Figure 1: Layout of the 2-stage 77 GHz PA that was submitted in January 2007 in a 120-nm BiCMOS process. The die dimension is 1.1mm x 0.75mm.



▲ Figure 2: Simulated results of the 77 GHz PA. The top graph shows the input power versus output power, and the bottom graph shows the S21 power gain.

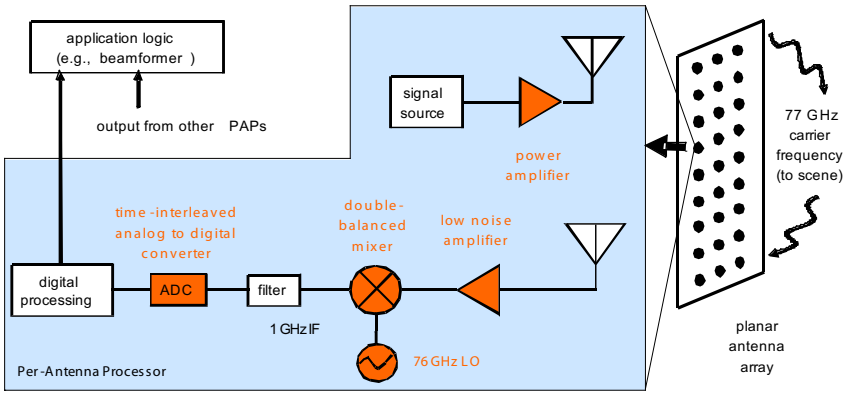
A 77-GHz System for Millimeter-wave Active Imaging

A. Accardi, J. Chu, K. Nguyen, J. Powell, H. Kim (Lincoln Laboratory), G. Wornell, H.-S. Lee, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

Due to advances in silicon and digital processing technology, low-cost millimeter-wave (MMW) imaging solutions with high antenna array density are now viable. While millimeter resolution or better is desirable for many applications, this wavelength is large enough to avoid scattering by tiny interfering particles. Furthermore, a large bandwidth can be supported at this high carrier frequency. The MMW technology is therefore well suited for applications such as automotive collision avoidance and concealed weapons detection.

By superimposing the signals recorded at antennas configured in an array, the imaging receiver can be focused on a portion of the scene corresponding to a particular pixel. This process, called beam forming, makes use of constructive interference at the carrier frequency and allows the receiver to be "electronically steered" without any moving parts. However, very low phase noise is required for fine resolution at long range.

Traditionally, beam-formers at such high frequencies are fabricated using custom analog technology to ensure precise phase control. Our system performs digital beam forming, allowing for low-cost, large-scale production and low power consumption. We address the phase noise by over-sampling, averaging, and employing feedback. That is, we correct for phase noise introduced in the analog and data conversion circuitry in the digital domain, thereby driving research with high data rate, low phase noise, and low power consumption requirements. Figure 1 illustrates the system and indicates the components we plan to fabricate. Our goal is to justify the system architecture and establish a proof of concept by implementing the most challenging components.



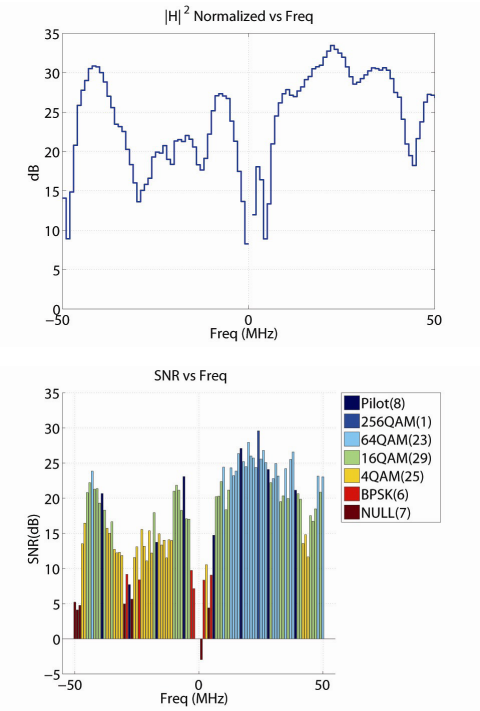
▲ Figure 1: A functional block diagram indicating the key components in the active imaging system. These components are part of the per-antenna processor (PAP), which is replicated for each node in the array.

Coding in Wideband OFDM Wireless Communications with Adaptive Modulation

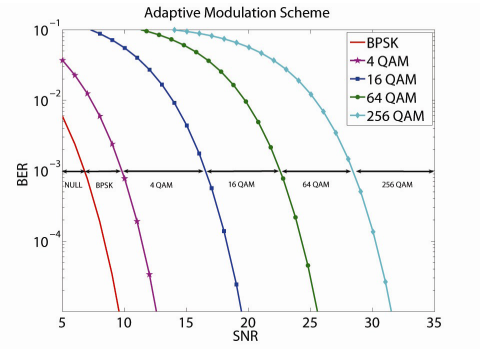
F. Edalat, C.G. Sodini
Sponsorship: CICS, NSF, Texas Instruments Fellowship

To achieve high-speed wireless communications, such as streaming of next-generation Gigabit Internet or HDTV, orthogonal frequency division multiplexing (OFDM) has been proven as the enabling technology. In an indoor environment where reflections from the surrounding objects result in multiple copies of the transmitted signal arriving at the receiver, the channel is highly frequency-selective over a wide bandwidth. An OFDM system decomposes such a channel into multiple flat fading sub-bands by transmitting the high data-rate signal in multiple parallel lower data-rate blocks. Furthermore, an OFDM system can exploit this channel characteristic to maximize the data rate by adapting the modulation per bin based on the estimated Signal-to-Noise Ratio (SNR), as shown in Figure 1 [1]. In addition, channel coding is necessary to achieve the required system performance with a limited transmit power. In this work, we determine suitable codes in an adaptive modulation OFDM system to achieve highest throughput with a constrained latency. In particular, we analyze the benefits and tradeoffs of such codes as convolutional coding, trellis-coded modulation, and capacity-approaching low-density parity-check codes used in current OFDM systems.

To measure the performance gain from coding with adaptive modulation in an indoor wireless environment, we have implemented a transceiver prototype. In this prototype, the adaptive modulation takes place in three steps. In step 1, the transmitter sends a training sequence, and the receiver measures the SNR on each bin. If the true SNR is known for each sub-band, the most efficient sub-band modulation that yields an uncoded bit error rate (BER) smaller than 10^{-3} is selected, as shown in Figure 2. However, the errors in the estimation of channel and time and frequency synchronizations result in a loss in SNR that increases the SNR thresholds in Figure 2. Next, in step 2, the receiver feeds back to the transmitter the assigned modulation scheme, which the transmitter uses to sends the data packet in step 3.



▲ Figure 1: Top: Channel attenuation vs. frequency. Bottom: SNR vs. frequency with the number of bins assigned for each modulation in the parenthesis [1].



▲ Figure 2: Sub-band modulation assignment at target uncoded BER of 10^{-3}.

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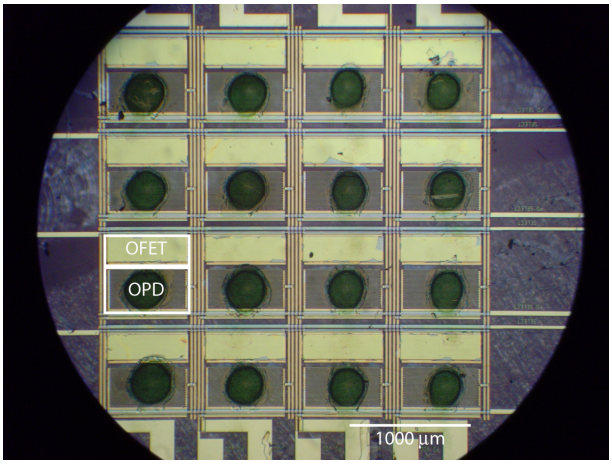
An Organic Imager for Flexible Large-area Electronics

I. Nausieda, K. Ryu, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

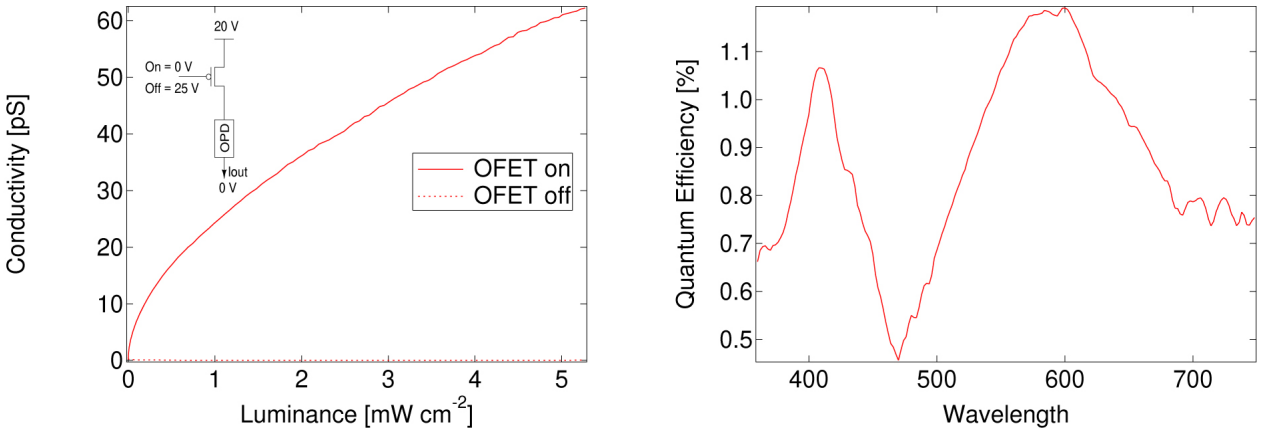
Interest in organic semiconductors is sustained in part by the promise of large-area and flexible electronics. Early work in this field has focused on the fabrication and testing of discrete devices, such as an organic field effect transistor (OFET), or organic photoconductor (OPD). Creating electronic systems, however, requires an integrated approach, for both fabrication and testing.

In this work, a 4x4 addressable imager consisting of OFET switches with OPDs was fabricated and tested, using a near-room temperature (<95°C) process [1]. The individual pixel circuit is shown in the top left of Figure 1. The OFET and lateral OPD were sized in order for the OPD to determine the pixel conductance while the OFET was on and for the pixel conductance to be dominated by the OFET while it was biased off. Since the OFET acts only as a switch, the circuit is robust to process variation and degradation over time. Measurements indicate a pixel responsivity of $6x10^{-5}$ A/W and an on/off ratio of 880 at a luminance of $5mWcm^{-2}$. The conductivity versus luminance is pictured in Figure 1.

The fabricated active matrix imager is seen in Figure 2. It occupies an area of $10.24mm^2$ and uses a 25-V power supply. The imager was demonstrated to correctly image a "T" pattern after a first-order calibration.



▲ Figure 2: Optical micrograph of the 4x4 active matrix imager.



▲ Figure 1: Pixel conductivity versus luminance, for the cases of the OFET switch biased on and off.

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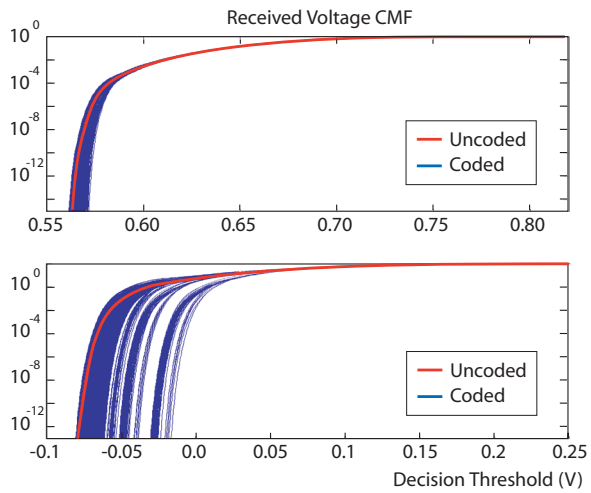
Channel- and Circuits-aware, Energy-efficient Coding for High-speed Links

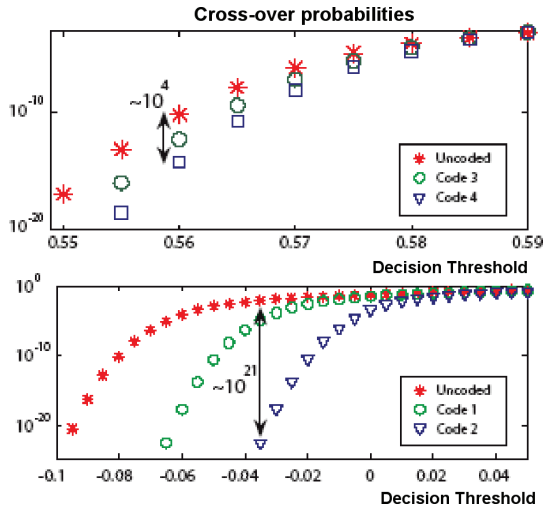
N. Blitvic, L. Zheng, V. Stojanović
Sponsorship: SRC/FCRP C2S2

In order to achieve high throughput while satisfying energy and density constraints, both the data rates and the energy efficiency of high-speed chip-to-chip interconnects need to increase. This project aims to extend the link system design to incorporate energy-efficient channel coding techniques. To enable the systematic characterization of different codes, we have developed a new statistical simulator [1]. The simulator employs a divide-and-conquer approach to fully account for the effect of long residual interference on the received voltage for systematic binary-linear-block-coded transmissions. It is therefore the first link simulator to accurately account for dependencies in transmitted data instead of approximating the transmissions as independent (uncoded). This method is of most use for high-rate codes, but it remains valid for both arbitrarily long channel lengths and block lengths. The resulting probability distributions are computed analytically and are therefore accurate at the low bit-error-rates (BER) required in high-speed links.

Integrating the voltage probability distributions computed through the previously described technique yields individual cross-over probabilities for different bit locations in a codeword. The resulting difference in the cross-over probabilities of individual bits compared to the cross-over probability of an uncoded system indicates the extent to which coupling residual interference with the data correlation due to binary linear block coding affects the performance of the system. Figures 1 and 2 illustrate this effect for two different link channels. Although the present focus is on developing simple codes tailored for interference-dominated environments, the current framework also allows for the characterization of classical error-detecting codes. For links with relatively well-compensated interference and low noise correlation, the channel can be approximated as binary-symmetric. The individual crossover probabilities are therefore sufficient to compute the error probabilities *after* error correction. This property was verified in [1] for some typical link channels and down to BERs achievable by Monte Carlo simulation.



▲ Figure 1: Voltage distributions for the set of all (10,8) linear block codes. Shown are the cumulative mass functions (CMF) for two different channels: Peters B3 operating at 5 Gbps [top] and Peters B32 operating at 10 Gbps [bottom]. The plots also show the voltage CMF computed under the assumption that the data is uncoded.



▲ Figure 2: Bit crossover probabilities for the uncoded case and two different (10,8) linear block codes on a B3 channel [top] and B32 channel [bottom]. Code 2 was chosen to yield the maximum deviation from the uncoded CMF, while Code 1 was chosen roughly in between the two extremes. The results are computed under the common assumption that the link noise is additive, white and Gaussian with $\sigma \approx 3$mV.

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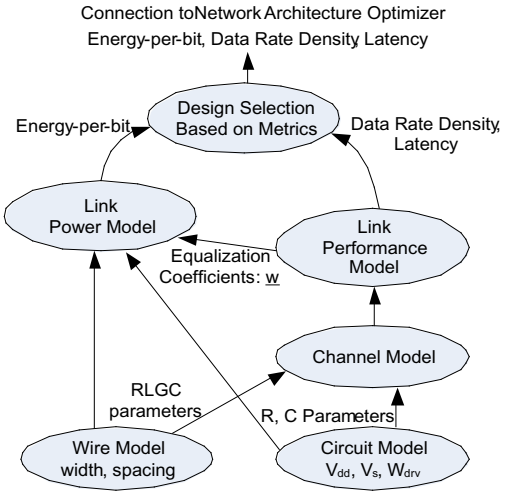
Design and Optimization of Equalized Interconnects for Energy-efficient On-chip Networks

B. Kim, V. Stojanović
Sponsorship: NEC Fund, IBM Faculty Award

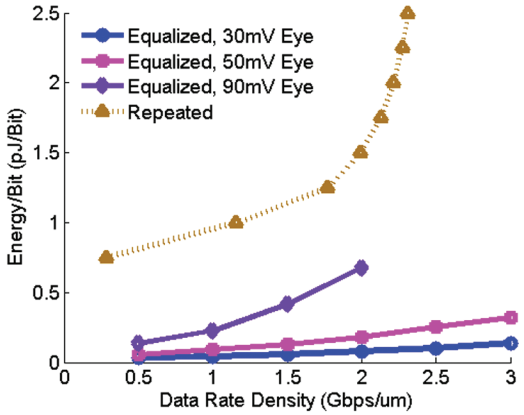
In recent high-performance processor design, multi-hierarchical co-optimization of on-chip network and overall chip architecture improves the performance-power efficiency significantly [1]. Though equalized on-chip interconnects have been proposed to improve the network efficiency [2-3], the multi-hierarchical co-optimization of equalized interconnect has been a difficult problem due to its design complexity.

This work presents a modeling and tool framework for fast design space exploration of equalized on-chip interconnects by exporting abstracted low-level design parameters to a link model. Using this tool technique, we can explore how the transistor and wire parameters affect link performance; equalization coefficients; and architecture-friendly metrics like delay, power, and area throughput density. With this approach, we are able to find the best link design for target throughput power and area constraints, thus enabling the architectural optimization of energy-efficient on-chip networks.

Figure 1 shows the hierarchical simulation framework. The lower level models are abstracted into the higher-level models. For example, RLGC matrices of the wire's transmission line are used to derive the through- and cross-talk closed-form transfer functions of the channel. At the top level, the behavioral model simulator uses the transfer functions to compute the link metrics and provides interconnect metrics for a low common mode (LCM) type equalized interconnect [4]. Figure 2 shows optimization results comparing interconnect metrics between the LCM and the repeated interconnects. Our simulation shows that the equalized LCM interconnect is much more power-efficient than the repeated interconnect for given target throughput density.



▲ Figure 1: Hierarchical simulation framework.



▲ Figure 2: Interconnects throughput density and power density trade-off.

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System-to-circuit Framework for High-speed Link Design-space Exploration

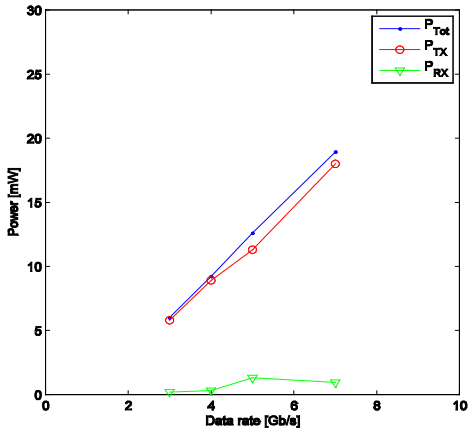
R. Sredojević, T. Khanna, V. Stojanović, J.L. Dawson

Currently, we aim to bridge the gap between analog/mixed-signal circuit and system design by providing a framework for fast design space exploration at the system-to-circuit level, based on the bottom-up information from the underlying circuits and process technology. This gap is particularly severe in high-speed link I/O circuits, which are rapidly growing into mini-communication systems due to the bandwidth limitations of packages and board traces [1]. Finding the best methods to compensate inter-symbol interference and minimize timing noise while running circuits at lowest possible power end maximum possible data rate is a difficult balancing act that requires extremely tight connection between circuit and system levels.

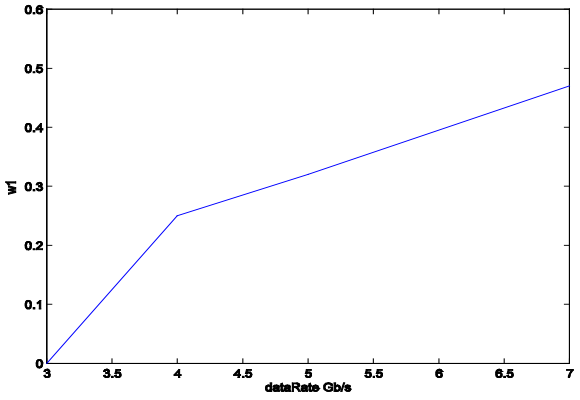
We try to provide a missing link between the system and circuit levels by formulating the system-to-circuit high-speed link description. This framework intimately connects circuit level parameters with block and system-level link specification, providing a direct vertical link from transistor sizes and parasitic to top-level link metrics: data rate, power, and bit-error-rate. We want this framework to provide answers to questions that link designers often ask: Which equalization method should be used (transmit pre-emphasis, linear analog receiver equalizer, decision-feedback equalizer)? What is the power/data-rate trade-off?

One of the most interesting descriptions of a high-speed link design space is a power vs. data rate trade-off for a given BER. Different link architectures, driver styles, and equalization methods can be plugged into our system-to-circuit framework to enable design space exploration. In Figure 1 we show the trade-off for a high-speed link with one-tap of transmit pre-emphasis and with receiver pre-amplifier equalization. When coupled with transmit pre-emphasis, receiver amplification improves the power-data rate trade-off since receiver pre-amplifier can drive larger on-chip impedance.

Next, in Figure 2 we show transmitter tap coefficients w for data rates in Figure 1. At lower data rates, where channel attenuation is not too strong, receive equalizer is very efficient, taking on most of the equalization and amplification roles. At higher loss conditions, the residual ISI in the channel saturates the input range of the receiver equalizer (the non-linearity limit) and transmit pre-emphasis has to increase to narrow down the dynamic range of the signal at the input to the receiver (transmit pre-emphasis attenuates the DC value of the received signal).



▲ Figure 1: Power vs. data rate trade-off for a given topology.



▲ Figure 2: Transmit side tap coefficient.

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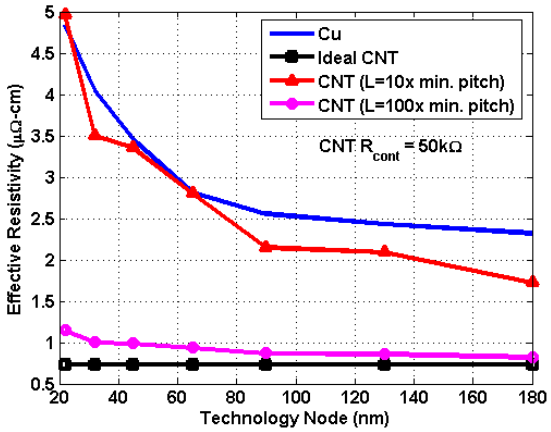
System Architecture Implications of CNT Interconnects

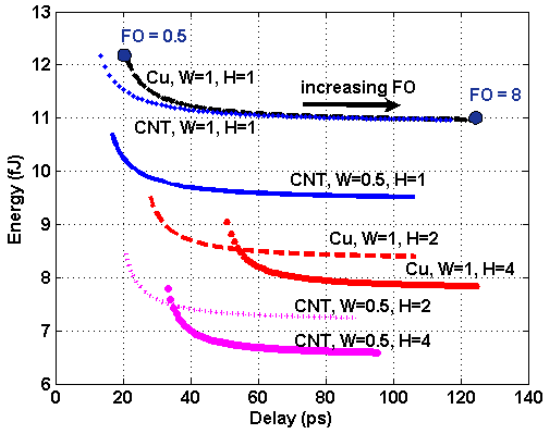
F. Chen, V. Stojanović, A.P. Chandrakasan
Sponsorship: SRC/FCRP IFC

As CMOS processes scale into the nanometer regime, lithography limitations, electromigration problems that increase resistivity, and relative delay of copper interconnects have driven the need to find alternative interconnect solutions. Carbon Nanotube (CNT) interconnects have emerged as a potential candidate to supplant copper interconnects because of their purported ballistic transport and ability to carry large current densities in the absence of electromigration. There have been several investigations [1-2] that assess the potential use of CNTs as interconnects in scaled VLSI applications. However, these works primarily focus on the relative interconnect delay of CNTs to copper for forthcoming technology nodes and do not address any higher-level issues.

In this work, we intend to investigate the relative system impact of using CNTs in order to gain insight as to how CNTs should be integrated into future processes. The CNTs are in effect a material similar to copper but with superior conducting properties as shown in Figure 1. The use of CNTs presents an opportunity to rescale the cross-sectional dimensions of the interlayer dielectric (ILD) stack up to take advantage of CNT properties. Figure 2 shows the energy delay tradeoff curves for several ILD and wire cross-sections for hybrid CNT and copper interconnects. The W and H values shown represent the wire width and dielectric height values normalized to the minimum copper wire width for the process and the nominal dielectric height, respectively. The CNT interconnects are assumed to have a resistivity close to that of bulk copper, which is roughly 2X better at sub-45-nm technology nodes. Results of the study indicate there is potential for improvements in both delay and energy by introducing a combination of CNT wires and CNT vias. Initial studies investigating the impact of using CNT interconnects on dense, buffered, on-chip routing networks show nearly a 2X increase in aggregate routing bandwidth and 3X longer routing distance before aggregate bandwidth saturates as compared to copper at the same technology node.



▲ Figure 1: Effective resistivity as a function of technology node. Figure 1 shows the effective resistivity of copper (Cu) interconnects and carbon nanotubes (CNTs) as the technology process scales. The Cu values are taken from the ITRS roadmap and include grain boundary scattering effects. The three CNT curves show the effective resistivity for ideally contacted CNTs and CNTs with 50kΩ of contact resistance at lengths of 10 times and 100 times the minimum metal pitch for the process node.



▲ Figure 2: Figure 2 shows energy vs. delay curves for various inverter driven copper and CNT wiring cross-section configurations at the 45 nm node. The load being driven is an 8X minimum-sized buffer load, and the length of the wires is 1000 times the minimum wire pitch. Variable H is the dielectric height normalized to the nominal ILD height, and W is the minimum wire width normalized to the minimum wire width for the process. Curves marked as "CNT" are assumed to have 1/2 the resistivity of copper wires.

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Section 2

ELECTRONIC DEVICES & EMERGING TECHNOLOGIES

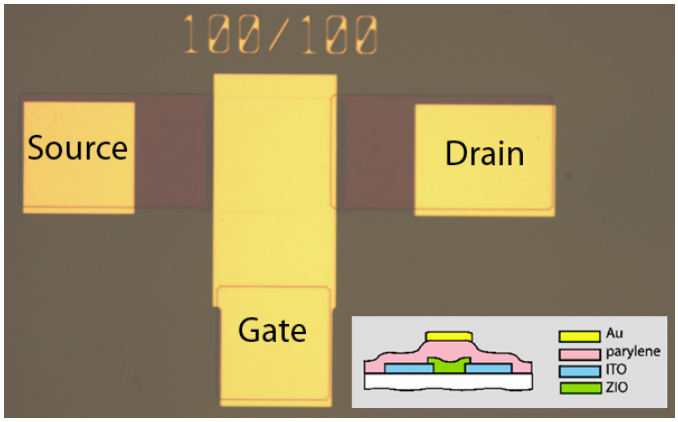
Near-room-temperature Processed Metal Oxide Field Effect Transistors for Large-area Electronics

A. Wang, K. Ryu, J.M. Perkins, I. Nausieda, B. Yaglioglu, C.G. Sodini, V. Bulović, A.I. Akinwande
Sponsorship: Hewlett-Packard

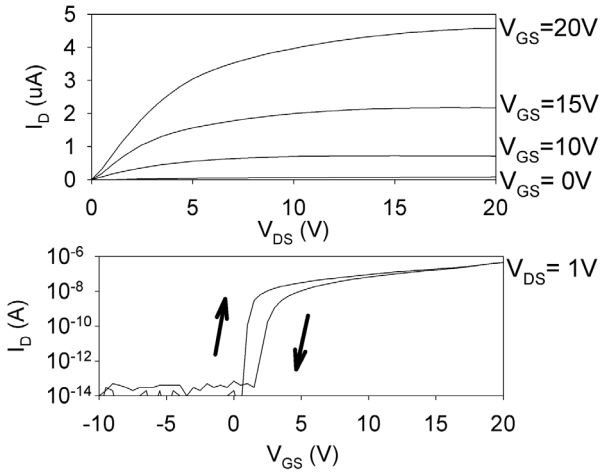
Recently, sputtered metal-oxide-based field effect transistors (FETs) have been demonstrated with higher charge carrier mobilities, higher current densities, and faster response performance than amorphous silicon FETs, which are the dominant technology used in display backplanes [1-2]. Furthermore, the optically transparent semiconducting oxide films can be deposited in a near-room-temperature process, making the materials compatible with future generations of large-area electronics technologies that require use of flexible substrates. [3]. It is possible to process FETs by shadow-mask patterning, but this method limits the range of feature sizes, accuracy of pattern alignment, and scalability of the process to large substrates. Consequently, our project aims to develop a low-temperature, lithographic process for metal oxide-based FETs, similar to one developed for organic FETs [4], that can be integrated into large-area electronic circuits.

Using an organic polymer, parylene, as the gate dielectric and indium-tin-oxide (ITO) for source/drain contacts, top-gate, lithographically processed FETs have been fabricated on glass substrates using ZnO:In_2O_3 channel layers. Figure 1 shows a micrograph of a completed FET, with current-voltage characteristics shown in Figure 2.

A reproducible FET process requires consistent control of material properties of the metal oxide semiconductor film. We examine the effect of varying deposition conditions (e.g., target composition, O_2 partial pressure, film thickness) and post-deposition treatment on DC- and RF-sputtered amorphous oxide thin films in the In_2O_3-ZnO system. The electrical properties of thin films are determined through resistivity and Hall measurements. These measurements are used as a guide to determine processing conditions for the fabrication of oxide-based field effect transistors and circuits.



▲ Figure 1: Top-view photomicrograph of lithographically patterned field effect transistor (W/L = 100μm/100μm). A schematic cross-section is also shown (inset).



▲ Figure 2: Current-voltage output characteristics (top) and transfer characteristics (bottom) for lithographically patterned zinc-indium-oxide field effect transistor. The transfer curve shown is a double sweep taken in the triode region (W/L = 100μm/100μm).

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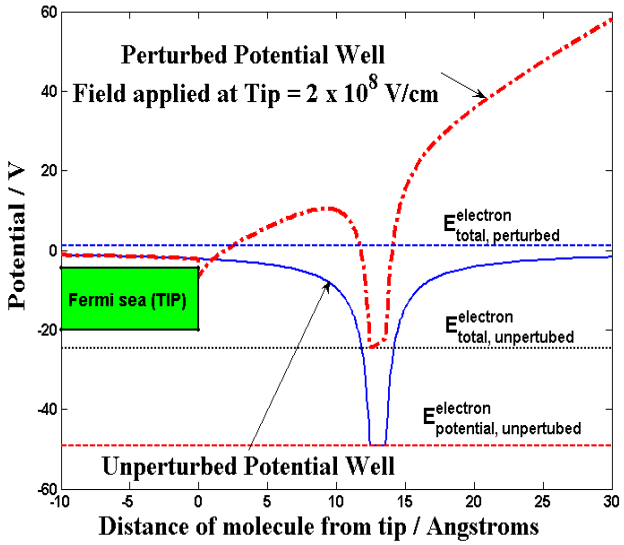
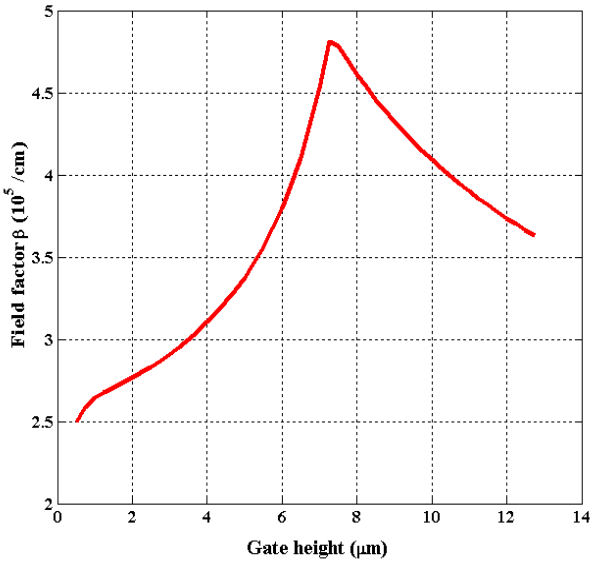
Characterization of Field-ionization from PECVD-grown CNT Tips

B. Adeoti, A.I. Akinwande, L. Velasquez-Garcia, L. Chen
Sponsorship: DARPA

The Micro Gas Analyzer project aims to develop the technology for portable, real-time sensors intended for chemical warfare and civilian air-purity control. For the analyzer, we are developing a field-ionizer array based on gated CNTs. We plan to use arrays of CNTs because their small tip radii and high aspect ratio yield high fields at low voltage. One possible configuration for the device is to bias the CNTs to the highest potential and the collecting anode to the lowest potential. The electrons in the outer shell of the molecules tunnel out due to the ambient high electric fields, which serve to lower the unperturbed potential barrier seen by the electrons (Figure 1). The tunneling effect is a purely quantum-mechanical process whose probability of occurrence is strongly dependent on the applied electric fields [1]. We optimize the electron current by varying structural parameters in our device. The most relevant parameters include the radius of curvature, height, base radius, and base angle of the grown tip; height and thickness of the tip; and the gate aperture. Varying the gate (or oxide) height without updating the height of the CNT yields the derivable result that the electric field is maximized with the tip peaks at about the same height as the gate. When the tip height is varied in sync with the height of the gate (or oxide), it is seen that an independent optimum height exists (Figure 2). The value of this height will depend, among other variables, on the electrostatic properties of the insulating material and the actual dimensions of the rest of the structure. These simulation results are being verified by experiment. Because it is not possible at this time to precisely control any of the CNT structural parameters, we focus on controlling the electrical properties of our device using the structural parameters of the gate.



▲ Figure 1: Representative picture of potential barrier faced by electron in a single molecule when the molecule is close to a tip biased at a high potential.



▲ Figure 2: The FI Field factor β for various heights of gate. Tip height was varied in sync with gate height so that the tip remained within the range of the gate width.
CNT : roc = 5.01nm | Base:- angle=85 , radius=101nm
GATE : Aperture=1.01μm Thickness=0.301μm
V_{CNT} = 10 V, V_{GATE} = 0 V, V_{ANODE} = -150 V

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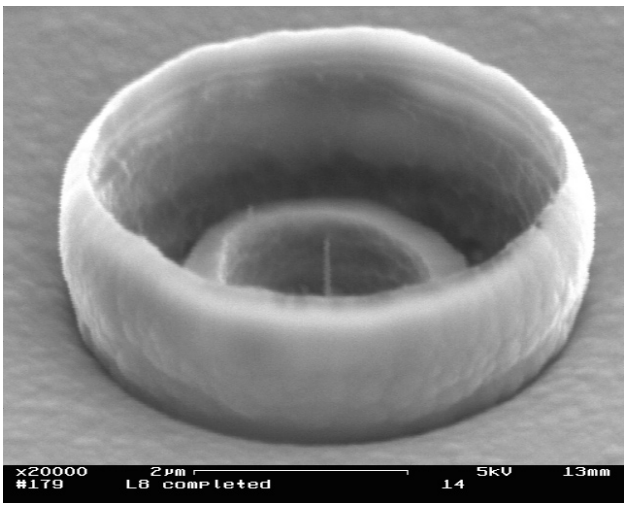
Field Emission from Double-gated, Isolated, Vertically Aligned Carbon Nanofiber Arrays

L.Y. Chen, L.F.V. Garcia, K. Cheung, X.Z Wang, K. Teo, A.I. Akinwande
Sponsorship: DARPA

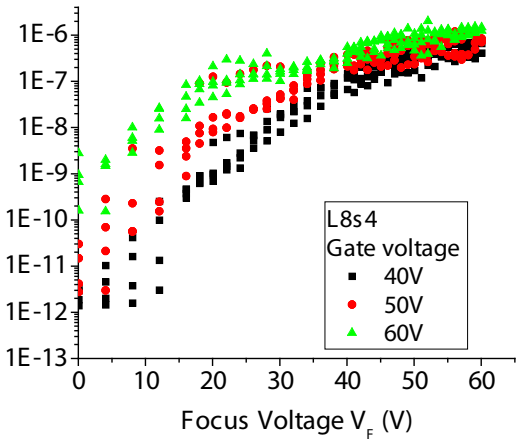
A collimated electron beam is often desired to achieve high performance for practical applications such as field emission display and ebeam lithography. We designed and fabricated a double-gated, isolated, vertically aligned carbon nanofiber field emission array (VACNF FEA) to produce a collimated electron beam. The first gate is used to extract electrons out of the tip and the second gate (focus gate) is biased at a lower voltage than the first gate to focus the emitted electrons.

In this work, we designed a device that maximizes the electric field generated at the tip and minimizes the shield effect from the neighbor while it is capable of handling a large breakdown voltage during the field emission operation. To accomplish this, an isolated VACNF with 4-μm-tall per emission site is needed with each site 10μm apart. The e-beam lithography and lift-off were used to define a 250-nm-diameter and 4-nm-thick Ni catalyst on an n-type Si substrate to guarantee nucleation of Ni dots and subsequent growth of CNFs. The 4-μm-tall VACNF was grown using plasma-enhanced chemical vapor deposition at 725°C. Once the CNF was synthesized, the extraction gate and the out-of-plane focus gate were fabricated with a novel photoresist planarization technique. This technique offers a very fast, fairly uniform, and well-controlled planarization method of making the self-aligned gate, which can replace the CMP technique that has been reported and used by L. Dvorson *et al.*, M.A. Guillorn *et al.*, and L.-Y. Chen *et al.* [1-3]. This abstract is perhaps the first report of double-gated, self-aligned, field emitter arrays with isolated VACNF.

With this fabrication process, two types of devices were fabricated: (1) with tip in-plane with the extraction gate and (2) CNF with tip 900nm below the extraction gate. They were characterized as three-terminal devices (focus and extraction gate at same bias) and as four-terminal devices (focus and extraction gates at different biases). Figure 1 shows a scanning electron microscope (SEM) picture of a complete device. Using this device, a four-terminal current-voltage (I-V) measurement was performed. As the focus voltage increases, the anode current increases, which is shown in Figure 2.



▲ Figure 1: An SEM picture of a complete double-gated, isolated VACNF FEA device.



▲ Figure 2: The four-terminal I-V characteristic of the double-gated, isolated VACNF array.

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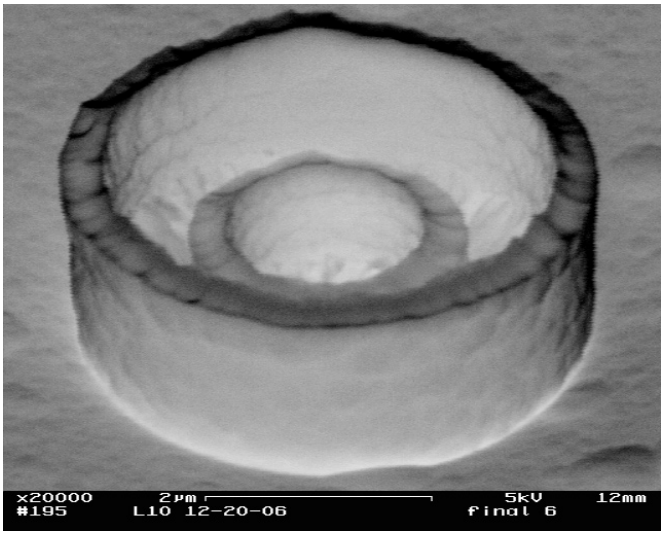
Electron Impact Ionization and Field Ionization of Gas through Double-gated, Isolated, Vertically Aligned Carbon Nanofiber Arrays

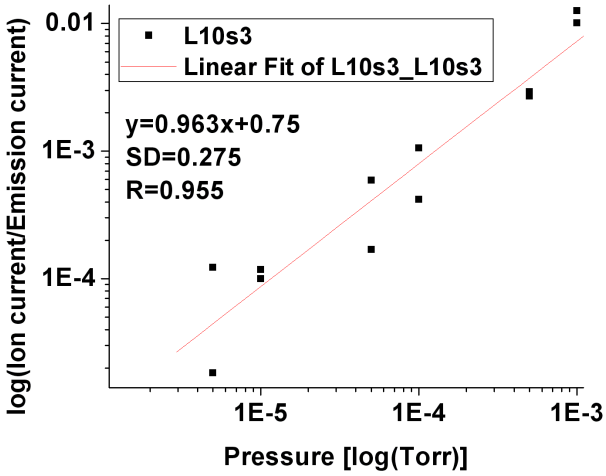
L.Y. Chen, L.F.V. Garcia, K. Cheung, X.Z. Wang, K. Teo, A.I. Akinwande
Sponsorship: DARPA

The goal of this project is to fabricate double-gated carbon nanofiber field emission and field ionization arrays, which can be utilized as an ionizer in a micro gas sensor. This device can help reduce the power consumption and the size of the conventional gas sensor. To achieve this goal, the double-gated isolated VACNF device is designed so that the electric field is maximized at the tip and the shielding effect from the neighbor is minimized while it is capable of handling a large breakdown voltage during the field emission and field ionization operations. Using a photoresist-based fabrication process, two types of devices were fabricated: (1) CNF with tip in-plane with the gate and (2) CNF with tip 0.9μm below the gate. Both devices have the following physical characteristics: (a) The tip height is about 4μm, (b) the gate diameter is 1.7μm, and (c) the focus diameter is 4.2μm. Figure 1 shows a scanning electron microscope (SEM) picture of a complete double-gated isolated vertically aligned carbon nanofiber (VACNF) array with tip 0.9μm below the gate.

Using the device shown in Figure 1, electron impact ionization and field ionization methods of ionizing gas molecules were performed. The electron impact ionization uses a strong electric field to emit electrons followed by collisions between the energetic electrons and neutral gas molecules, resulting in ionization. A linear relationship was obtained between the chamber pressure and the ratio of the ion current and the electron current, as shown in Figure 2. The field ionization is a gentler process in comparison to electron impact ionization. Instead of electrons tunneling from the tip to the vacuum under a high field (as in field emission), in field ionization, electrons tunnel from the gas molecules into the tip, thereby ionizing the gas molecules. It results in molecular ionization and a simpler mass spectrum due to less fragmentation of molecules.



▲ Figure 1: An SEM picture of a complete isolated VACNF array with tip 0.9μm below the gate.



▲ Figure 2: The linear relationship between the pressure and the ratio of the ion current and the emission current in electron impact ionization.

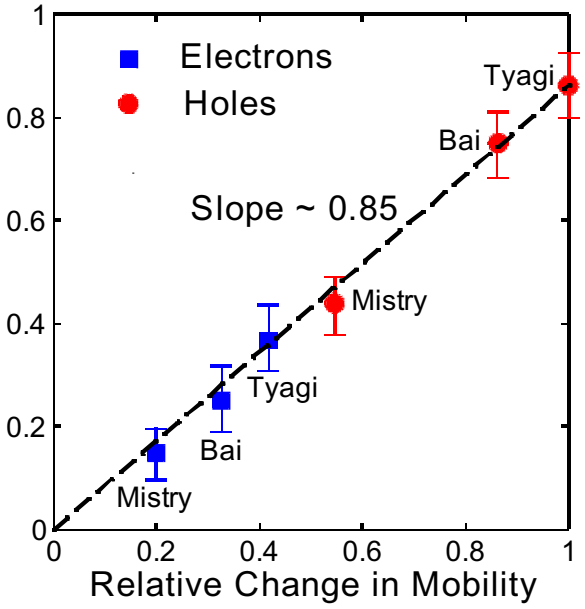
Correlation of Strain-modified Carrier Mobility and Velocity in Modern CMOS

A. Khakifirooz, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

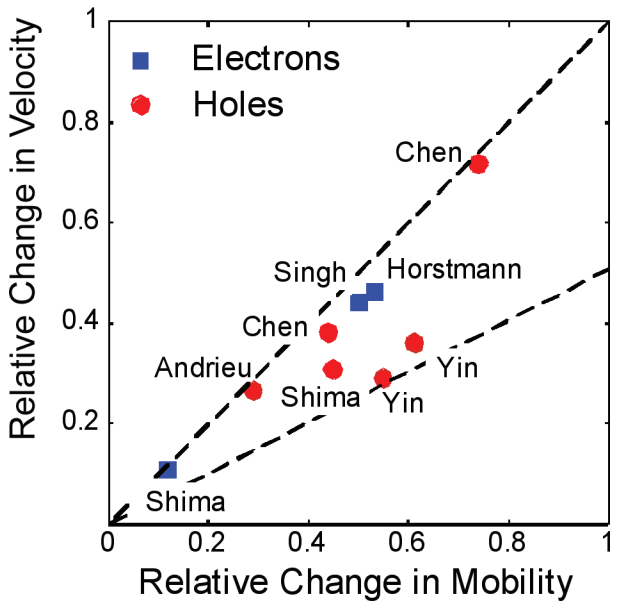
The introduction of strain into the Si channel at the 90-nm node [1] has been critical to increasing carrier mobility and velocity in the channel and maintaining historical CMOS performance trends. Recent experimental data on strain-engineered MOSFETs [2] show strong correlation between the low field mobility and the saturation drain current, both measured in short channel devices. To study this dependence, it is more instructive to explore the correlation between the actual (average) velocity of carriers at the potential barrier at the source side of the channel (virtual source) and the mobility. We have proposed a simple methodology for extracting the virtual source velocity from literature data [3]. Figure 1 shows the correlation between the virtual source velocity and mobility in strain-engineered MOSFETs reported by Intel [2]. As seen, the ratio between the change in the velocity to that of mobility is much higher than the commonly accepted value of 0.5 [4-5]. A similar observation is made on short channel devices reported by other groups as shown in Figure 2. This strong correlation between velocity and mobility can be explained based on the dependence of both mobility and velocity on the effective mass of carrier being modulated by applying mechanical stress. In addition, with less scattering in the channel, carriers gain velocity much faster when traveling across the channel. The steeper velocity profile requires a steeper drop in the inversion charge density and hence a steeper change in the potential. As a result, the distance over which the potential drops by kT/q (the critical length of backscattering) will be smaller. With these two effects combined together, the relative change in the velocity and mobility are related as follows:

$$\partial v_{x0}/v_{x0} = [\alpha+(1-B)(1-\alpha+\beta)]\frac{\partial\mu}{\mu}$$

where α models the dependence through the change in the effective mass of carriers, close to 0.5 for uniaxially strained transistors; β models the change in the critical backscattering length, roughly -0.45 according to self-consistent simulations; and B is the ballistic efficiency.



▲ Figure 1: Correlation between the relative change in the low field mobility and relative change in the virtual source velocity in state-of-the-art CMOS devices [2].



▲ Figure 2: Same as Figure 1, for short channel devices reported by other groups. The relative change in the mobility is usually taken from the change in the slope of R_{tot}-L_G curves.

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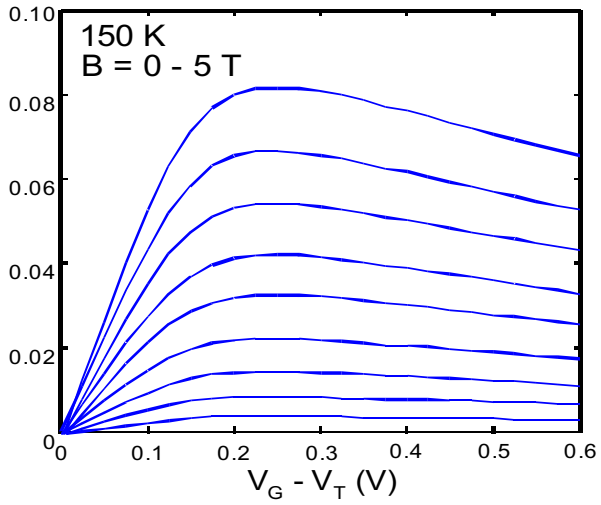
Carrier Mobility Characterization in Germanium MOSFETs

A. Khakifirooz, A. Ritenour, J. Hennessy, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

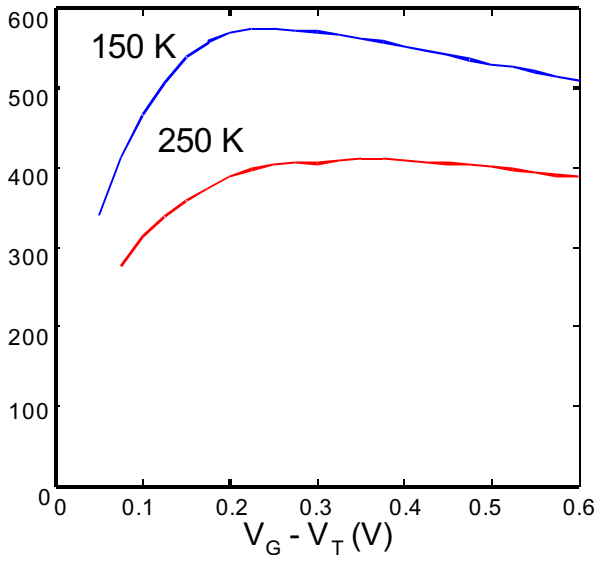
Germanium has attracted much attention in recent years as an alternative channel material for increasing the transistor performance because of its superior electron and hole mobility [1-3]. However, mobility values achieved so far have been considerably lower than what is expected in Ge. This points to the fact that high-k processes adapted for Ge devices are far from having optimum conditions. In addition to higher phonon scattering and surface roughness scattering associated with the presence of high-k dielectrics, due to the presence of a high number surface states (usually more than 10^{12} $cm^{-2}eV^{-1}$), carrier mobility is severely degraded. On one hand, charged surface states act as a source of Coulombic scattering, and on the other hand, their presence contaminates the estimation of inversion charge and hence the mobility calculation. Pulsed I-V and Q-V methods provide a path to D_{it}-free measurement of the mobility [4-5]. Alternatively, Hall and magnetoresistance measurements can be used to extract the intrinsic mobility of the carriers in the channel. Although the mobility probed with these two methods is different from the effective mobility measured by the split-CV method, they provide complementary information to estimate the inversion charge and gain insights into various scattering mechanisms involved. Measuring the device characteristics under relatively high magnetic fields is an integral part of both methods. Figure 1 shows the relative change in the channel resistance in a wide PMOS Ge transistor upon application of a magnetic field. As expected, the data show a quadratic dependence of resistance, R, according to

$$R(B)/R(0) = 1 + \mu_m^2 B^2$$

where μ_m is the magnetoresistance mobility. Figure 2 shows the magnetoresistance mobility in PMOS Ge devices as a function of the gate voltage and at two different temperatures. Combined with Hall measurements, these data provide valuable information about the scattering mechanisms that limit the mobility in Ge transistors.



▲ Figure 1: Relative change in the channel resistance in PMOS Ge transistors upon applying a magnetic field normal to the channel. The channel resistance shows a quadratic dependence on the magnetic field according to $R(B)/R(0) = 1 + \mu_m^2 B^2$, where μ_m is the magnetoresistance mobility.



▲ Figure 2: Magnetoresistance mobility measured in PMOS Ge transistors as a function of the gate voltage. Combined with Hall measurements, these data provide valuable information about the scattering mechanisms that limit the mobility in Ge transistors.

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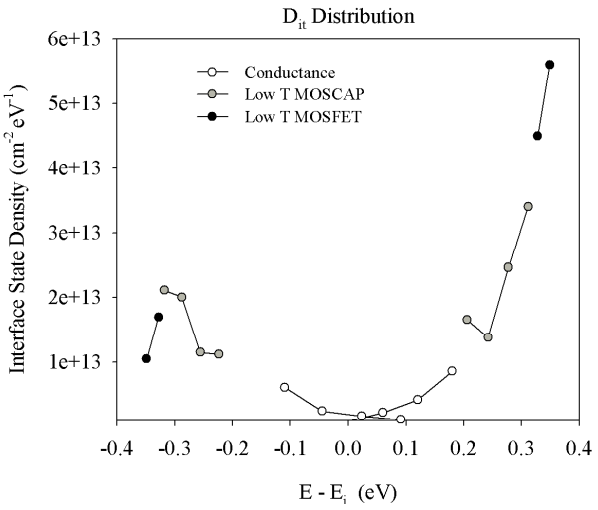
Investigation of Germanium MOSFETs with High-k Dielectric Stacks Based on Nitride Interfacial Layers

A. Ritenour, J. Hennessy, A. Khakifirooz, D.A. Antoniadis
Sponsorship: SRC/FCRP MSD

To improve source injection velocity and consequently MOSFET performance, high mobility semiconductors are being explored as possible replacements for silicon. Germanium offers enhanced electron mobility and superior hole mobility at high inversion charge density; however, the formation of a high-quality germanium-dielectric interface remains a serious challenge. High-k dielectrics deposited directly on germanium exhibit poor physical and electrical properties, so an interfacial layer is required. Proposed interlayers include GeON [1], Si [2], and metal nitrides such as AlN [3] and Hf_3N_4 [4].

This work focuses on metal nitride interlayers deposited by atomic layer deposition (ALD). The ALD $WN/Al_2O_3/AlN$ gate stacks were developed for use in Ge MOSFETs. An AlN thickness of approximately 2 nm and post-metal anneal at 450°C in forming gas produced optimal electrical characteristics. Ge n- and p-MOSFETs were fabricated with this gate stack, and peak electron and hole mobilities of 50 and 150 cm^2/Vs, respectively, were observed. Investigation of these devices revealed an asymmetric distribution of interface states within the bandgap. Figure 1 shows the interface state distribution. Conductance measurements on capacitors and low-temperature measurements on both capacitors and MOSFETs were used to determine the interface state density in different regions of the bandgap. The poor mobility of Ge n-MOSFETs is due to carrier trapping and coulomb scattering resulting from a large density of interface states ($5x10^{13}$ cm^{-2} eV^{-1}) near the conduction band edge.



▲ Figure 1: Distribution of interface states for $WN/Al_2O_3/AlN$ gate stacks on germanium. Interface state density in different regions of the bandgap was determined from conductance measurements on capacitors and low-temperature characterization of both capacitors and MOSFETs.

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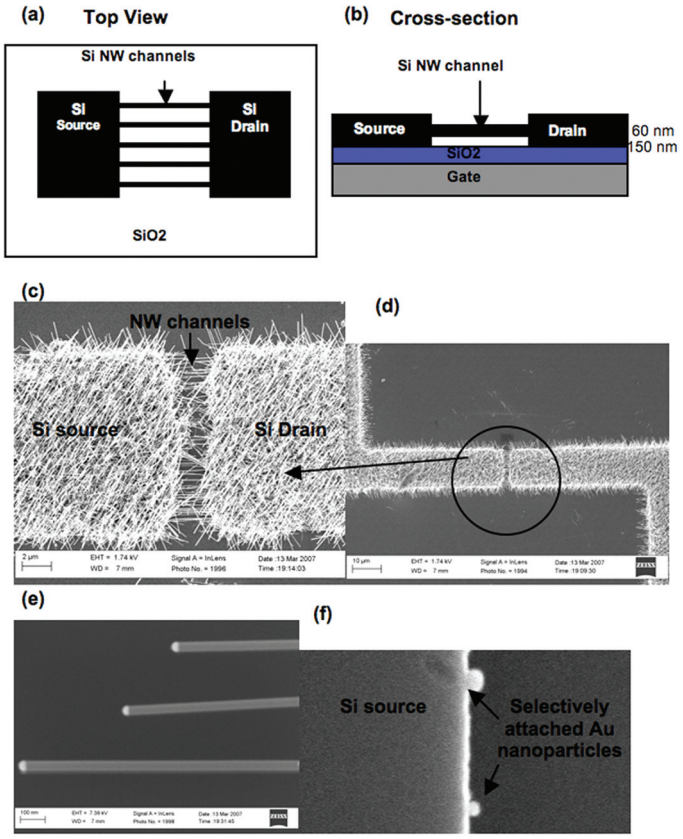
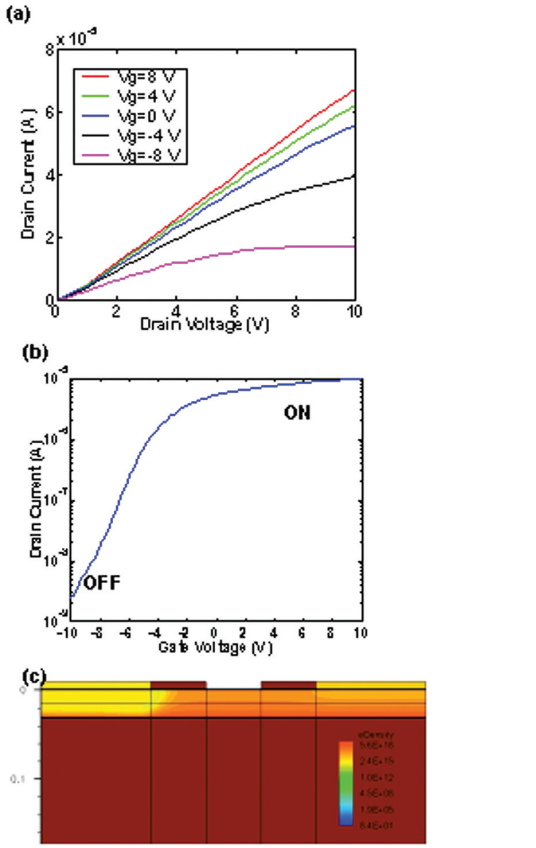
Si Nanowires: Fabrication, FETs, and Modeling

O.M. Nayfeh, D.A. Antoniadis
Sponsorship: Singapore-MIT Alliance

Silicon nanowires are attractive components in 22-nm-node and beyond high-performance technology. In this work, we fabricated silicon nanowire field effect transistors that incorporate single-layers of nanowire channels. The channels were laterally grown via the Vapor-Liquid-Solid (VLS) technique directly in the device structure to "bridge" the gap between adjacent short (~60 nm) Silicon-on-insulator (SOI) entrenched side-walls via a combined bottom-up/top-down method as shown in the schematics and SEM's of Figure 1. The utilization of short SOI sidewalls allowed for the selective attachment of single layers of catalyst particles on the sidewalls and hence the growth of single layers of entrenched channel bridges. Moreover, we were able to modulate the charge density of the wires immediately after growth without post-processing by biasing the planar back-gate. The measured 3 terminal current-voltage data shown in Figure 2 are characteristic of field-effect transistor behavior where the bridging nanowires act as the FET channel material and agree with simulation analysis of the structure.



▲ Figure 1: Top view(a) and cross-section (b) schematic of silicon nanowire FETs. An SEM micrograph of fabricated NWFET(c&d) showing a single layer of laterally grown parallel silicon nanowires bridging the gap between source-drain. An SEM closeup of as-grown nanowires ~30 nm in diameter (e) and an SEM of selectively attached Au catalyst nanoparticles on the short SOI sidewall (f).



▲ Figure 2: Transfer curves (a), Id. vs. Vds varying Vgs for the silicon nanowire FET shown in Figure 1, and (b) the Id. vs. Vgs showing clear transistor behavior, i.e., gate modulation of the current switching the device between on (Vgs=10 V) and off (Vgs=-10 V). Simulated electron density of the device in the on-state, Vgs=10 V, Vds=1V (c) showing the creation of a conduction pathway from source-drain consistent with the measurements of the device.

Scanning Helium Ion Beam Lithography

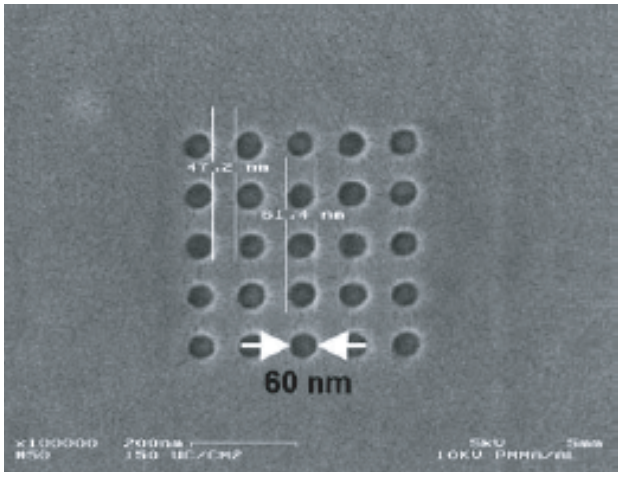
B. Cord, M.K. Mondol, K.K. Berggren, L.A. Stern (Karl Zeiss SMT)

Scanning electron beam lithography (SEBL) has been the leading technology in low-volume, high-resolution nanofabrication for over three decades. Unfortunately inherent limitations of the technology, such as electron beam scattering, have made improvement in SEBL resolution past the 10-nanometer limit problematic. Recent advances in resist contrast enhancement have mitigated this somewhat, but reliable patterning of dense, sub-10-nm features remains nontrivial on even the most high-end SEBL tools.

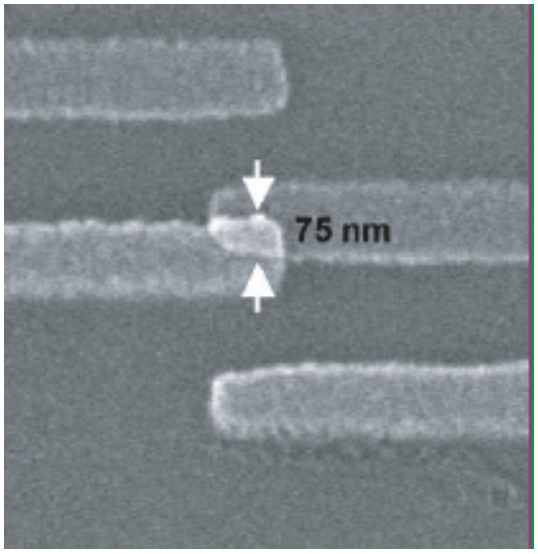
One of the key advantages of patterning using a helium ion, rather than an electron beam, is the substantial reduction in beam scattering as it travels through the resist. Helium ions, with a comparatively higher mass, are affected much less by atomic collisions when traveling through a material and exhibit only minimal scattering in normal resist materials. Figure 1 shows the results of a Monte Carlo simulation of a 50-KeV helium ion beam traveling through a PMMA layer; at a depth of 50 nm (a typical resist thickness for many applications), the point-spread function of the beam is only 2 nm wide, narrower than even 100-KeV electron beams under similar conditions. This reduction in beam scattering should help reduce the proximity effect that makes patterning dense, high-resolution features difficult with SEBL.

Experimentation with helium ion beam lithography has recently been made possible by the development of a scanning helium ion beam microscope by Alis Corporation [1]. Their commercial-grade microscope has achieved imaging resolutions on the order of 1 nm, making it a promising candidate as a lithography tool. Basic experimentation with their lower-resolution "proof-of-concept" system has demonstrated that patterning and successful transfer of features are possible using standard SEBL processes. Figure 2 shows a field of Ti-Au dots patterned with the system using a film of PMMA on silicon and standard metallization and liftoff.

While issues such as vibration, pattern generation, and process control remain to be addressed, further experimentation with helium ion beam lithography may lead to a tool that meets or exceeds the performance of modern SEBL systems.



▲ Figure 1: Simulation of He ion scattering in resist. (a) Result of SRIM-based Monte Carlo simulation of ion-scattering for 50-keV He ions traveling through 100 nm of PMMA into a Si substrate (b) Analysis of the data from (a) showing how the distribution of deposited energy widens as a function of resist depth. After 50 nm of resist (a practical thickness to work with), the beam width is only 2 nm. Note that this model does not take secondary electrons generated by the ion beam into account, as the details of the ion-secondary electron interactions are not yet fully understood.



▲ Figure 2: Scanning electron micrographs of a field of Ti-Au dots at two magnifications, fabricated by exposing 90-nm PMMA on a Si substrate to a single raster-scan of a helium ion beam and performing metal evaporation and liftoff on the resulting pattern. The consistently irregular dot shape in (b) is thought to be the result of vibrations in the system. The large square in (a) is a previously-fabricated fiducial mark.

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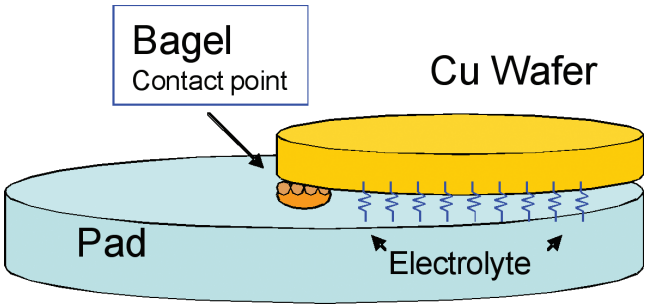
Wafer Level Modeling of Electrochemical-mechanical Polishing (ECMP)

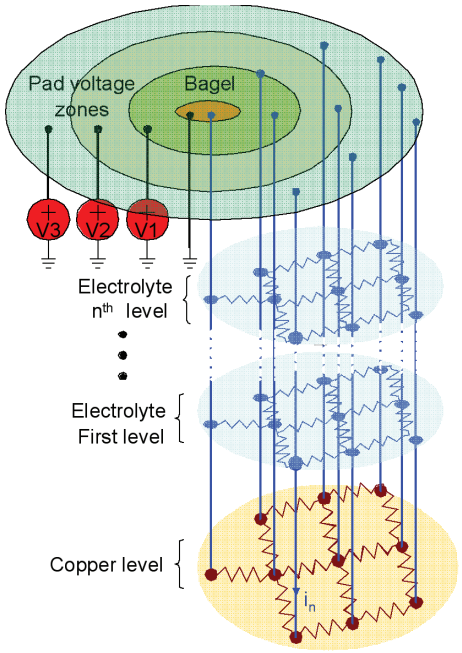
D. Truque, X. Xie, Z. Li, D.S. Boning
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, IBM, Albany Nanotech

In this work, we propose a wafer-level dynamic eCMP model based on time-evolving current density distributions across the wafer. The wafer is discretized, and the potential and current density distributions are calculated based on the applied voltage zones and metal film thicknesses across the wafer. The copper removal rate is proportional to the current density, and thus the copper thickness (and conductance) can be calculated as a function of position on the wafer and polish time. Using a time-stepping simulation, the model is able to capture the wafer level non-uniformity and time-dependence of eCMP removal. The model is also able to capture the time-varying voltage zones used in eCMP, and can be used to find optimal voltage zone control schemes to achieve improved wafer-level uniformity.

The configuration of the eCMP equipment is shown in Figure 1, where a voltage is applied in each of three zones on the platen, and electrical contact is made to the edge of the wafer. The modeling approach is pictured in Figure 2, in which the electrical current distributions on the wafer surface and in the electrolyte are accounted for, giving the removal rate at each location on the wafer.



▲ Figure 1: Schematic of wafer and tool configuration in electrochemical-mechanical polishing (eCMP).



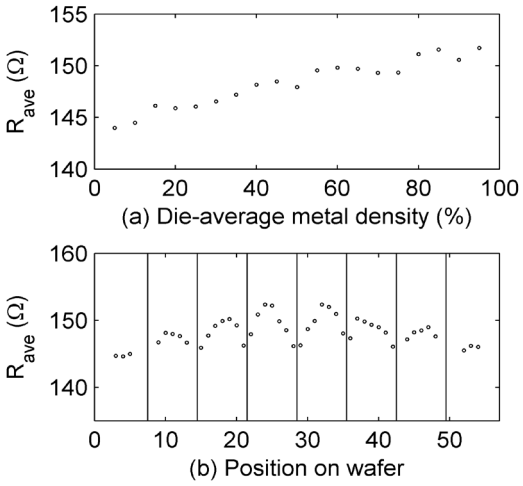
▲ Figure 2: Wafer-level modeling approach for eCMP, accounting for the distribution of current through the wafer surface and electrolyte.

Models for Spatial Non-uniformity in Plasma Etching

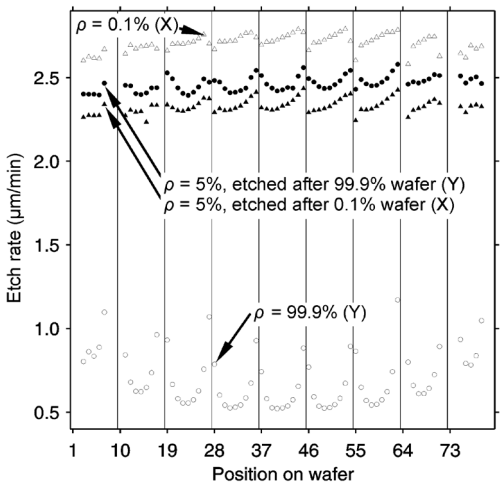
A. Farahanchi, H.K. Taylor, D.S. Boning
Sponsorship: National Semiconductor, SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

We are studying the plasma etching of aluminum films for IC metallization. Using electrical resistance measurements from a dedicated metal test pattern, we have identified, in a commercially-used etching process, resistance variations of 5% cross-wafer and additionally of about 5% according to the locally averaged metal pattern density (Figure 1). The etching rate also depends appreciably upon the size of the etched feature.

The deep reactive ion etching (DRIE) of silicon for MEMS also experiences spatial non-uniformity, which can be detrimental to its applications. We hope to use our model to predict the uniformity of proposed new operating "recipes." We continue to investigate an observed "memory" effect in DRIE chambers (Figure 2), whereby the average pattern density of one etched wafer influences the rate and uniformity of the subsequent wafer's etching.



▲ Figure 1: Spatial variation of the electrical resistances of aluminum snake patterns etched from a film on a 200 mm-diameter wafer. (a) shows how the average resistance of a snake (R_{ave}) increases by ~5% as the areal density of unetched metal near the feature increases from 5% to 95%. In areas of higher unetched metal density, local competition for reactants is less acute during etching, so that lateral etching of snake features can progress more quickly, increasing the features' resistances. (b) shows a cross-wafer variation of ~5% among the resistances of features with identical local surroundings.



▲ Figure 2: Vertical silicon etch rate as a function of location on each of four etched 150 mm-diameter wafers in a deep reactive ion etch (DRIE) process. A monitor wafer with 5% mask-opening density etched immediately after wafer Y (with 99.9% pattern density) etched consistently faster and less uniformly than a 5%-density monitor wafer etched after wafer X (with 0.1% pattern density). Here and in Figure 1b, the position axis corresponds to locations on a square grid, with each row of locations plotted consecutively and separated by vertical bars on the graph.

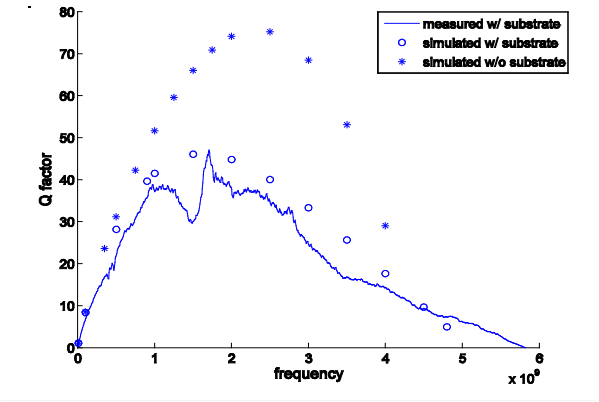
Development of Specialized Basis Functions and Efficient Substrate Integration Techniques for Electromagnetic Analysis of Interconnect and RF Inductors

X. Hu, T.A.E. Moselhy, J. White, L. Daniel
Sponsorship: SRC/FCRP GSRC, NSF

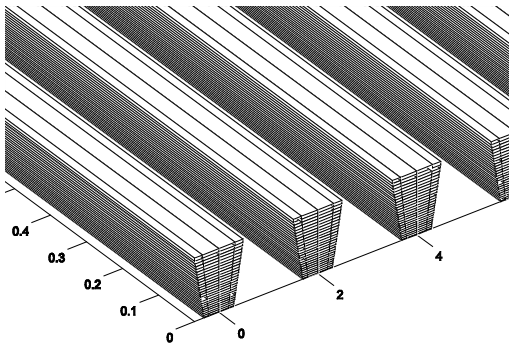
The performance of several mixed-signal and RF-analog platforms depends on substrate effects that need to be represented in the library model with critical field solver accuracy. For instance, substrate-induced currents in RF inductors can severely affect quality and hence RF filter selectivity. We have developed an efficient approach to full-wave impedance extraction that accounts for substrate effects through the use of two-layer media Green's functions in a mixed-potential-integral-equation (MPIE) solver. In particular, we have developed accelerated techniques for both volume and surface integrations in the solver.

In this work, we have also introduced a technique for the numerical generation of high-order basis functions that can parameterize the frequency-variant nature of cross-sectional conductor current distributions. Hence skin and proximity effects can be captured utilizing fewer high-order basis functions in comparison to the prevalently used piecewise-constant basis functions. One important characteristic of these basis functions is that they need to be pre-computed only once per unique conductor cross-sectional geometry, and then stored off-line with a minimal associated cost. In addition, the robustness of these frequency-independent basis functions is enforced using an optimization routine.

We have shown in [2] that the cost of solving a complex interconnect system using our new basis functions can be reduced by a factor of 170 when compared to the use of piecewise-constant basis functions over a wide range of operating frequencies. Furthermore our volume and surface integration routines improve efficiency by an additional factor of 9.8 [1]. Our solver accuracy is validated against measurements taken on fabricated devices.



▲ Figure 1: Measured and simulated Q-factors for a square RF inductor with an area of 15mm x 15mm and surrounded by a ground ring.



▲ Figure 2: Our basis functions avoid the expensive cross-sectional discretization shown in the figure necessary to account for trapezoidal cross-sections or skin and proximity effects.

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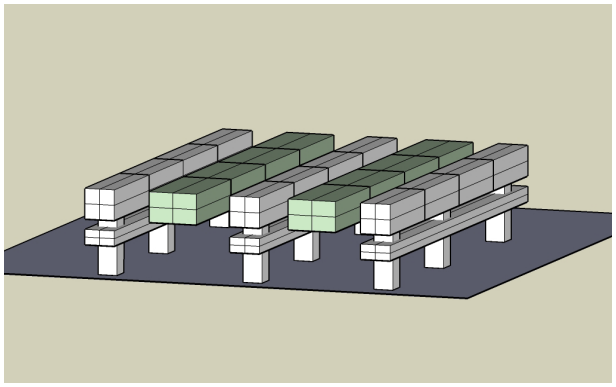
pFFT in FastMaxwell: A Fast Impedance Extraction Solver for 3D Conductor Structures over Substrate

T. Moselhy, X. Hu, L. Daniel
Sponsorship: SRC/FCRP IFC

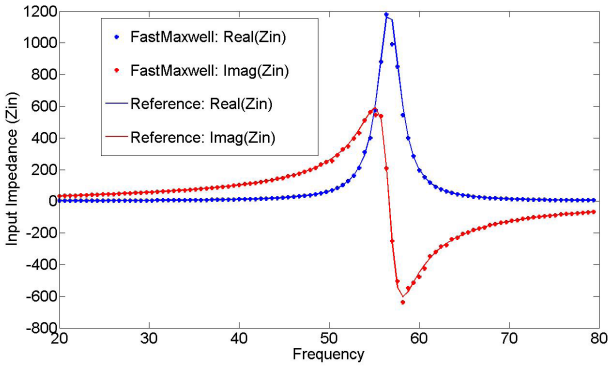
Interconnect-aware timing analysis and mixed-signal simulation rely on tools for extracting accurate low-order models for interconnect electrical behavior. Models should be physics-based to enable efficient modeling of 2D and 3D effects on interconnects with their statistics and variations. As a first step toward our goal, we have been focusing on the development of a very efficient 3D parasitic extractor for the deterministic analysis of a large collection of interconnects. FastMaxwell [1], is a program for wideband electromagnetic extraction of complicated 3D conductor structures over substrate. It is based on the volume mixed potential integral equation (MPIE) formulation, with a 3D full-wave substrate dyadic Green's function kernel. Two dyadic Green's functions are implemented [2]: a traditional Green's function and an alternative Green's function that can lead to computational cost reduction in most practical applications. Most importantly, the alternative Green's function allows the use of dipoles (i.e., filaments) in arbitrary orientations, and it helps providing symmetric positive semidefinite matrices, hence facilitating the passive model order reduction of distributed systems. The pre-corrected Fast Fourier Transform (pFFT) [3] algorithm has been extended and optimized to accelerate the iterative solver within FastMaxwell.

The accuracy and efficiency of FastMaxwell and the implemented acceleration algorithms have been verified against measurements of fabricated devices by a variety of examples, some as large as 100,000 unknowns, using less than 400MB of memory and a few hours of computation time. The pFFT computational complexity of O(N log N) in overall solver time and O(N) in memory usage has been observed from our results, leading to a scalable software for very large collection of interconnects.

FastMaxwell is public domain and can be downloaded at: www.rle.mit.edu/cpg/fastmaxwell.htm.



▲ Figure 1: FastMaxwell discretization of a two-wire transmission line on top of a substrate and shielded by a 3D cage structure. The cage is connected to ground through vertical vias. (Figure is rescaled and edited for clarity.)



▲ Figure 2: Real and imaginary components of the input impedance of a two-wire transmission line. Results obtained by FastMaxwell are within 2% of those obtained by reference simulator IE3D [4].

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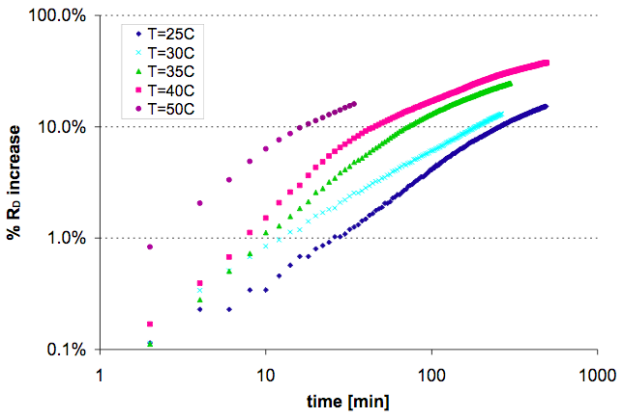
Modeling Drain Degradation of RF Power GaAs Pseudomorphic HEMTs under High Bias Conditions

A.A. Villanueva, J.A. del Alamo
Sponsorship: Mitsubishi Electric

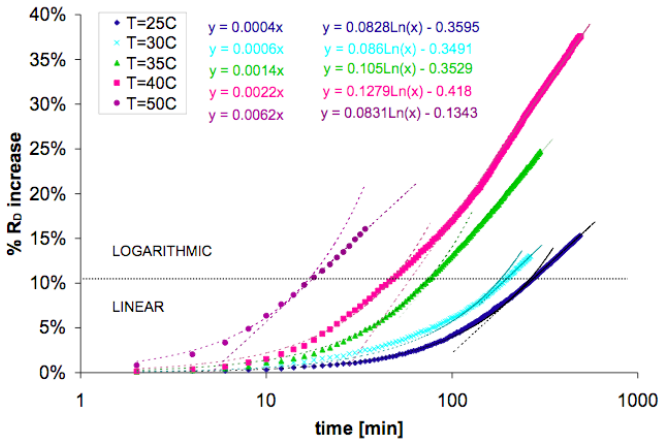
GaAs Pseudomorphic High-electron Mobility Transistors (PHEMTs) are widely used in RF power applications. A major concern with these devices is their gradual degradation under prolonged high-voltage biasing. This effect is mainly observed via an increase of the drain resistance (R_D) and a decrease of the maximum drain current (I_{max}). Previous studies have linked this degradation to various mechanisms, including impact ionization (II) and hot-electron effects, and surface corrosion [1]. However, further investigation is required to determine which of these mechanisms are actually behind the observed degradation. Understanding the time evolution of the degradation can provide some insight into this.

In our study, experimental (non-commercial) GaAs PHEMTs were electrically stressed. A stressing scheme that keeps II constant was employed. Specifically, this scheme consisted of keeping the drain current I_D constant and the intrinsic drain-to-gate voltage V_{DGo} constant (relative to the threshold voltage) [2]. During stressing, the devices were characterized at frequent intervals.

Figure 1 illustrates the time evolution of the increase of R_D in a set of experiments performed at various ambient temperatures. One can clearly see that the ΔR_D is dramatically accelerated with increasing temperature, which alone suggests a corrosion mechanism instead of an II mechanism. Also, there seem to be two "regimes" of degradation. For initial stages (less than ~10% increase in R_D), the degradation is roughly linear in time. In a later stage, the degradation slows down, becoming closer to a logarithmic dependence in time. This phenomenon is better seen in Figure 2, which shows a semi-log plot of the same data with both the linear and log fits superimposed. This behavior thus suggests that ΔR_D is directly related to the growth of an oxide layer on the GaAs surface on the drain side, which is accelerated with temperature and typically follows a time-dependence similar to what we observe. Initially, as a GaAs surface is oxidized, the oxide layer is thin enough so oxide growth at the GaAs/oxide interface is limited by the reaction rate, thus giving a linear dependence in time. However, as the oxide layer thickens, the oxide formation then becomes limited by the transport of the oxidizing agent through the oxide to the GaAs/oxide interface. In GaAs systems this transport process has been observed to have a logarithmic dependence on time.



▲ Figure 1: Log-log plot of percent increase of R_D versus stressing time for series of constant $V_{DGo}+V_T$ and constant I_D experiments performed on standard-parameter PHEMTs in nitrogen environment at T_{amb} =25, 30, 35, 40, and 50°C.



▲ Figure 2: Semi-log plot of percent increase of R_D versus stressing time for series of constant $V_{DGo}+V_T$ and constant I_D experiments performed on standard-parameter PHEMTs in nitrogen environment at T_{amb} =25, 30, 35, 40, and 50°C. Linear and logarithmic fits are shown for each data set.

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Electrical Reliability of GaN High Electron Mobility Transistors

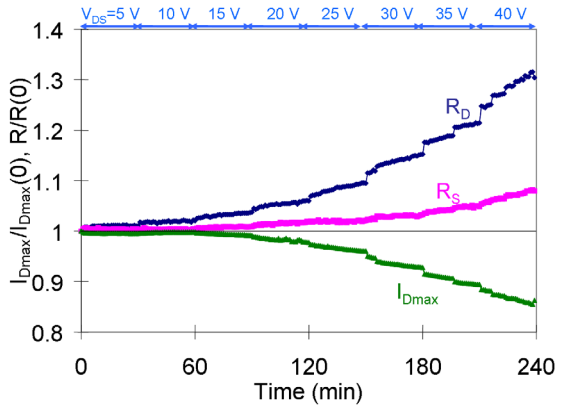
J. Joh, J.A. del Alamo (in coll. with TriQuint Semiconductor, BAE Systems)
Sponsorship: ARL

As a result of their large band gap (~3.4 eV) and high breakdown electric field (>3x10^6 V/cm), GaN-based devices can operate at voltages higher than 100 V. Also, due to the strong piezoelectric effect and spontaneous polarization of both GaN and AlN, a high sheet carrier density (~10^{13} cm^{-2}) can be achieved at the AlGaN/GaN heterointerface without any doping. In addition, high electron mobility (~1500 cm^2/V-s) and high saturation velocity (~2x10^7 cm/s) make GaN-based devices, especially GaN high electron mobility transistors (HEMT), suitable for high power amplification at high frequencies, such as WiMAX or WLAN base stations and radars.

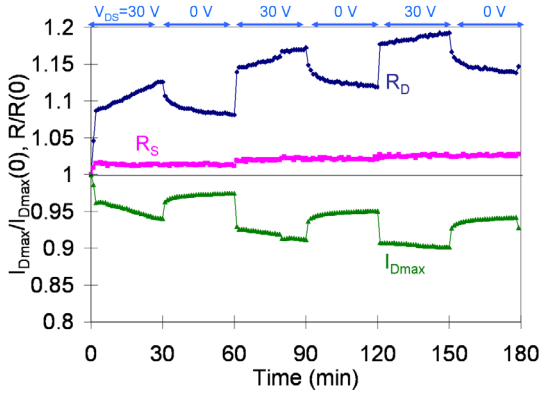
In spite of their extraordinary performance, GaN HEMTs still have limited reliability. In RF power applications, GaN HEMTs must operate at high voltage, where good reliability is hard to obtain. Physical understanding of the fundamental reliability mechanisms of GaN HEMTs is still lacking today. In this research, we carry out systematic reliability experiments on industrial GaN HEMTs provided by our collaborators, TriQuint Semiconductor and BAE Systems. In our study, GaN HEMTs have been electrically stressed at various bias conditions while they are being characterized by a benign characterization suite that we have developed for this study.

In our experiments, we have observed that electrical stress on GaN HEMTs results in an increase in drain resistance R_D and a decrease in maximum drain current I_{Dmax}, as shown in Figure 1. The source resistance R_S shows relatively less degradation. We have found that the electrical stress generates traps. Figure 2 shows a stress-recovery experiment in OFF state. Partial recovery in the recovery phase suggests electron detrapping, and immediate retrapping in the following stress phase suggests permanent trap formation. We have also seen that this degradation is driven mostly by the electric field, with the current being less relevant. We hypothesize that the main mechanism behind device degradation is defect formation through the inverse piezoelectric effect and subsequent electron trapping. Departing from current conventional wisdom, hot electrons are less likely to be the direct cause of electrical degradation in the devices that we have studied. Our studies suggest a number of possibilities to improve the electrical reliability of GaN HEMTs. As our hypothesis suggests that it is important to keep the elastic energy in the AlGaN barrier below a critical value, minimizing the initial elastic energy and peak vertical electric field in AlGaN can improve reliability.

Our research addresses the fundamental degradation physics of GaN HEMTs. This study will help us to understand failure mechanisms in detail and to develop processes and device designs that minimize these deleterious effects.



▲ Figure 1: Change in normalized I_{Dmax}, R_D, and R_S in a step-stress experiment in the OFF state (I_D=25 mA/mm,V_{DS}=5~40 V in 5 V steps, 30 minutes per step).



▲ Figure 2: Change in I_{Dmax}, R_D, and R_S in a stress-recovery experiment in the OFF state (V_{DS}=30 V, I_D=20 mA/mm) for 30 minutes of stress followed by 30 minutes at rest. This cycle is repeated three times.

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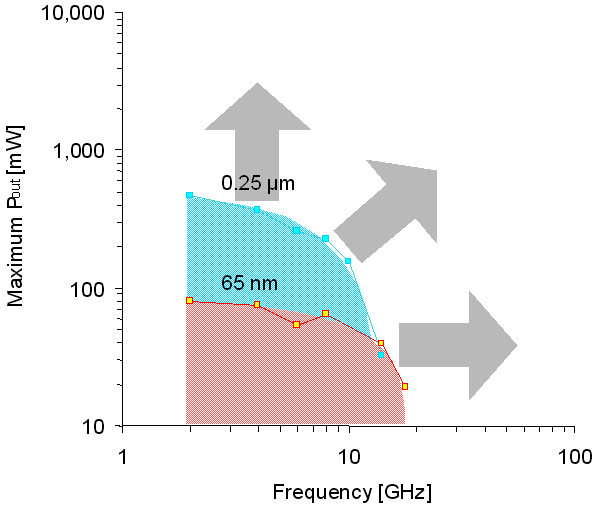
RF Power CMOS for Millimeter-wave Applications

U. Gogineni, J.A. del Alamo (in coll. with D.R. Greenberg, IBM)
Sponsorship: MIT Presidential Fellowship, IBM

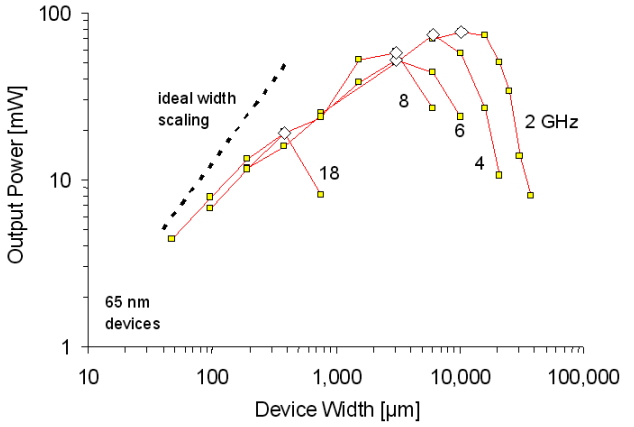
Radio frequency (RF) power amplifiers are core components of almost all wireless systems. Traditionally III-V devices, SiC devices or SiGe heterojunction bipolar transistors have been used in power amplifiers because of their ability to deliver high power and operate at high frequencies. Recently there has been an increased interest in using Si CMOS for designing single-chip integrated systems for operation in the millimeter-wave regime. Specific applications in this regime include wireless LAN and collision avoidance radar.

Previous research in our group at MIT into the RF power performance of 65-nm and 90-nm Si CMOS devices [1-2] has shown that it is not possible for currently available Si CMOS to operate significantly beyond 20 GHz (Figure 1). The effective cut-off frequency for power (frequency at which the output power drops below 10 mW) is around 20 GHz for 0.25-um, 90-nm and 65-nm CMOS. This suggests that further scaling is unlikely to improve the situation despite improvements in f_T and f_{max}. The reason for this saturation in the effective power cut-off frequency is that the optimum device width that delivers the maximum power at any frequency scales down as the frequency goes up (Figure 2). This effect indicates that the bottleneck for power is the device layout, especially the back-end wiring. An optimized device layout would enable us to operate Si CMOS in the millimeter wave regime.

In this research, we are investigating options for device optimization with the goal of pushing the power operation of Si CMOS into the millimeter-wave regime. In particular, we are studying designs that minimize interconnect resistance through optimization of source and drain routing. Some of the ideas to reduce interconnect resistance include use of multiple levels and thicker levels of metal and use of multiple source and drain pads. We are also exploring designs that separate DC and RF paths through on-chip bias networks.



▲ Figure 1: Maximum power (at peak PAE) vs. frequency of operation obtained in nominal 0.25-um devices (V_{dd}=2.5 V) and 65-nm devices (V_{dd} =1 V) fabricated in a 65-nm process [1].



▲ Figure 2: Maximum Power (at peak PAE) vs. device width for different frequencies for 65-nm devices (V_{dd} =1 V) [1].

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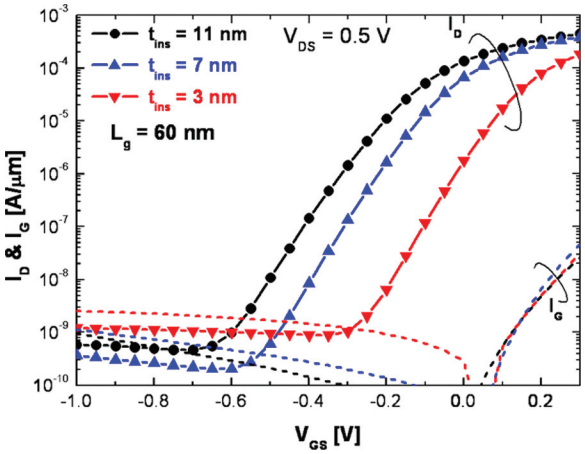
Scaling Potential of InGaAs HFETs for Beyond-the-roadmap CMOS

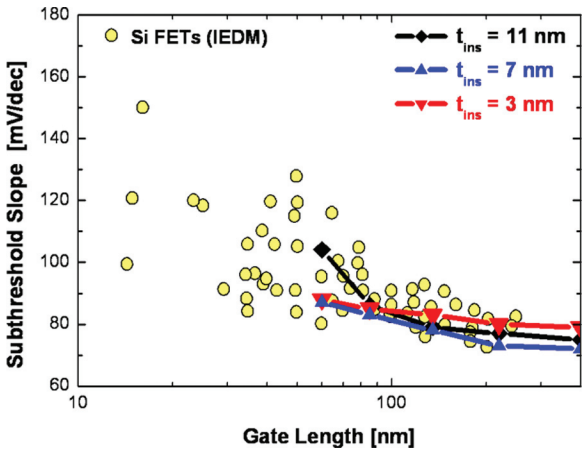
D.-H. Kim, J.A. del Alamo
Sponsorship: Intel Corporation, SRC/FCRP MSD

While a matter of considerable debate, the semiconductor device technology that has been responsible for the microelectronics revolution of the last 30 years appears to be reaching the end of the roadmap. There are severe doubts that it will make economic sense for Si CMOS to scale beyond the 22-nm node. In the landscape of alternatives to Si CMOS for beyond-the-roadmap logic applications, III-V compound semiconductors really stand out. For example, InGaAs looks particularly promising. Since room temperature bulk electron mobility of InGaAs is easily in excess of 10,000 cm^2/V-s, it is imperative to consider this material as a channel for next-generation "low-power" and "high-speed" logic technology.

In our work, we are investigating the scaling potential of InGaAs heterostructure-FETs (HFETs) as a model system to study the challenges and opportunities of III-V based FETs for logic. We have fabricated InGaAs HFETs with a 70% InAs composition in the channel and with varying gate lengths (L_g, from 400 nm to 60 nm) and InAlAs insulator thickness (t_{ins}, from 11 nm to 3 nm). Figure 1 shows subthreshold and gate leakage (I_G) characteristics of representative 60-nm InGaAs HFETs with three different t_{ins}, at V_{DS} = 0.5 V. As t_{ins} decreases, V_T shifts positively and the subthreshold slope improves considerably. The value of S = 88 mV/dec is obtained for the t_{ins} = 3 nm device, and this sharp subthreshold characteristic yields an I_{ON}/I_{OFF} ratio in excess of 10^4. Figure 2 compares S as a function of L_g between InGaAs HFETs with three different t_{ins} and Si CMOS. Our devices exhibit almost the same electrostatic integrity and, especially, InGaAs HFETs with t_{ins} = 3 nm exhibit values of S, that are on the low range of the reported state-of-the-art Si CMOS. Our research strongly confirms that InGaAs HFETs are an excellent test vehicle to explore issues of great relevance to future III-V FETs, such as self-aligned architectures, scaling limit of planar devices, band-to-band tunneling in a narrow band-gap (E_g) material, impact of strain on transport physics and the consequences of a low density of states on the current deeply scaled devices.



▲ Figure 1: Subthreshold and gate leakage characteristics of 60-nm InGaAs HFETs with three different t_{ins} at V_{DS} = 0.5 V. The t_{ins} = 3 nm devices exhibit almost enhancement mode operation (V_T = - 0.02 V), subthreshold slope (S) = 88 mV/dec and $I_{ON}/I_{OFF} > 10^4$.



▲ Figure 2: Subthreshold slope as a function of gate length for InGaAs HFETs with various insulator thickness, as well as Si CMOS. Well designed InGaAs HFETs exhibit values of the subthreshold slope that are on the low range of state-of-the-art Si CMOS.

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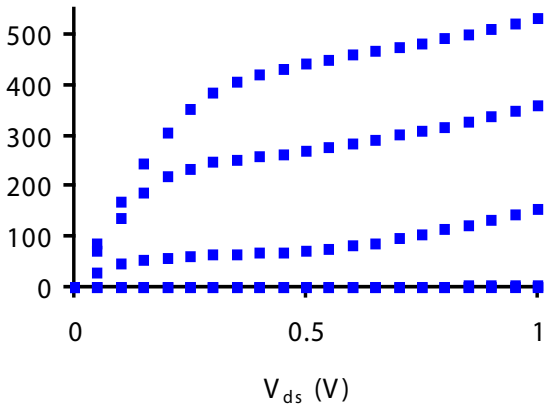
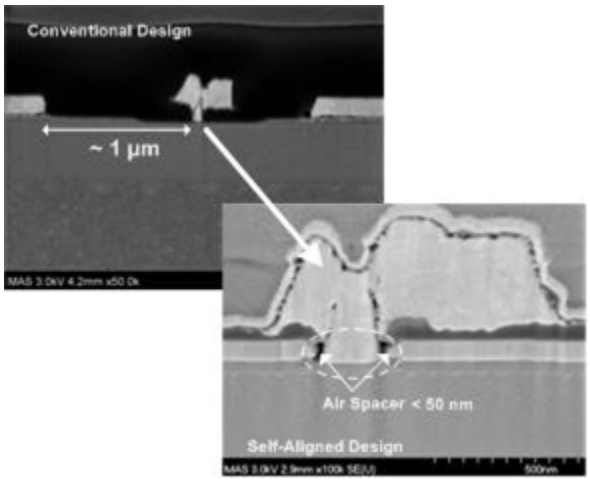
Self-aligned InGaAs HEMT for Logic Applications

N. Waldron, J.A. del Alamo
Sponsorship: SRC/FCRP MSD, Intel Foundation Ph.D. Fellowship Program

As conventional CMOS scaling approaches the end of the roadmap, identifying a new logic device technology is becoming a matter of great urgency. With room-temperature electron mobility easily in excess of 10,000 cm^2/V.s, InGaAs represents a very attractive proposition as a channel material. Previously it has been shown that InGaAs-based high electron mobility transistors (HEMTs) show great promise for logic applications. The 60-nm devices fabricated with a triple recess process showed a significant improvement in drive current compared to 65-nm CMOS for the same level of leakage current [1]. However, the conventional design of HEMTs is not well suited for VLSI applications. The gate is not self-aligned and is typically separated from the source/drain by a distance of around 1μm, which results in a large device footprint and associated parasitics. Also the exposed surface area and alloyed contacts represent reliability concerns.

To address these issues we have developed a self-aligned process that reduces the gate to source/drain distance to less than 50 nm. This is more than a 20x improvement over the conventional design. The new device relies on the use of W for non-alloyed ohmic contacts. A two-step e-beam lithography process is used to define the gate. The first step defines both the W source/drain contacts and the gate foot, resulting in a final structure that is self-aligned. An SEM of the completed device is shown in Figure 1. The output characteristics of a 0.3-μm device are shown in Figure 2. The self-aligned devices show excellent DC characteristics. The device has a maximum transconductance of 988 μS/um, SS of 77 mV/dec, DIBL of 44 mV/V and an I_{on}/I_{off} ratio of 6 x 10^3. Currently we are working on fabricating devices of varying gate lengths to determine the scaling potential of the self-aligned scheme. We are also exploring various approaches to achieve enhancement-mode devices.





▲ Figure 1: An SEM comparing a conventional HEMT to a self-aligned HEMT device. The source/drain is separated from the gate by a distance of 1 um in the conventional design. Using the self-aligned architecture use of an air-spacer reduces this distance to less than 50 nm.

▲ Figure 2: Output characteristics of a 0.3-μm device fabricated using the self-aligned process. The device threshold voltage is -0.2 V.

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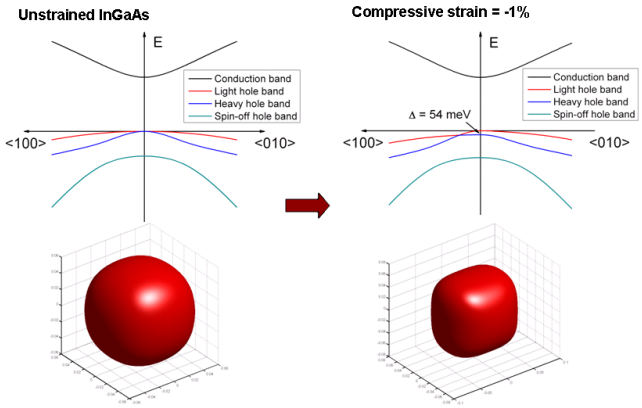
P-channel InGaAs HEMTs for beyond-Si Complementary Logic

L. Xia, J.A. del Alamo
Sponsorship: SRC/FCRP MSD

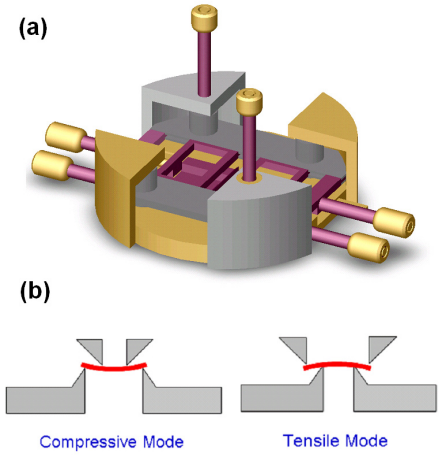
As the silicon metal-oxide-semiconductor field-effect transistor (MOSFET) approaches the end of the roadmap, its performance improvement brought by size scaling will reach a limit. Among the beyond-Si logic alternatives, InGaAs shows superior potential for n-channel FET-type devices [1]. However, the hole mobility in InGaAs is currently not much higher than that in silicon. In fact, the large disparity between n- and p-channel InGaAs FET performance raises concerns about the possibility of implementing InGaAs CMOS-type logic.

In order to boost the speed of p-channel InGaAs FETs, we are studying the enhancement of the hole mobility by mechanically straining the channel. This has been demonstrated in Si and Ge devices. Compared with their unstrained counterparts, strained Ge and Si showed 6× and 2× higher hole mobilities respectively. [2, 3] We are carrying out simulations that indicate that strain will also show positive effects on hole mobility in InGaAs. As shown in Figure 1, in unstrained InGaAs, the heavy-hole and light-hole valence bands are degenerate at the Γ point. When strain is applied, the two bands split. This splitting leads to preferential occupation of holes into the lighter band, so that the effective mass of the holes decreases. In this way, the hole mobility should be enhanced.

To experimentally probe the potential enhancement brought by strain, a chip-bending apparatus (Figure 2a) has been fabricated. This apparatus has four ridges whose vertical and horizontal positions are controlled by micrometers. By positioning the ridges as shown in Figure 2b, we can apply either tensile or compressive strain on the upper surface of the chip. By fitting the apparatus into a probe station, we can conduct electrical measurements on strained samples. These measurements are expected to provide understanding of the speed-enhancing effects of strain in InGaAs FET's.



▲ Figure 1: Simulation results of strain-induced band structure change in InGaAs. The bandstructures and light-hole iso-energy surfaces of unstrained and strained InGaAs are shown. Under 1% compressive strain, the heavy-hole band and light-hole band split apart by the amount of 54 meV. The shapes of light-hole iso-energy surface indicate that strain also breaks the symmetry of the light-hole band. This anisotropy would allow us to better tailor both in-plane and out-plane effective masses.



▲ Figure 2: (a) Schematic figure of the chip-bending apparatus. (b) Methods to apply compressive and tensile strain to the chip surface.

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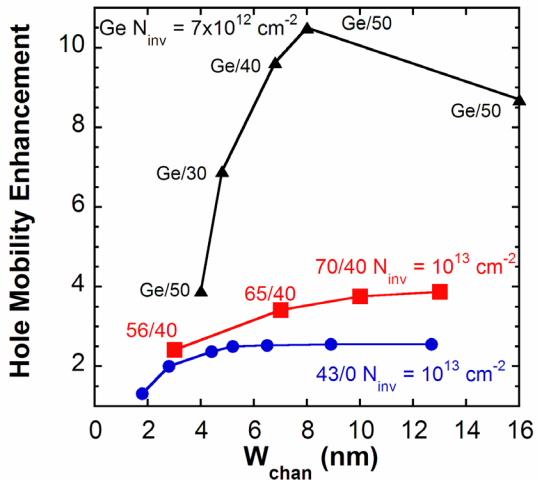
Strained SiGe-channel p-MOSFETs: Impact of Heterostructure Design and Process Technology

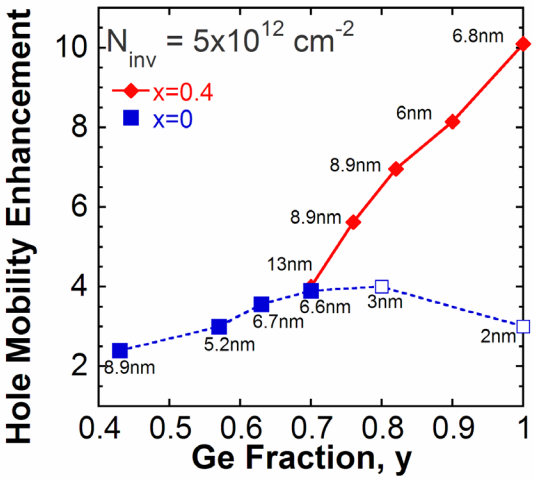
C. Ní Chléirigh, J.L. Hoyt
Sponsorship: SRC, SRC/FCRP MSD, Texas Instruments Fellowship, Applied Materials Fellowship

Superior hole mobility (up to 10X enhancement over bulk Si channels) and compatibility with mainstream Si processing technology make compressively strained SiGe an attractive channel material for sub-45-nm p-MOSFETs. This research investigates strained SiGe as a suitable channel material for p-MOSFETs using SiGe grown pseudomorphically on both relaxed SiGe and bulk Si substrates. Strained SiGe channels directly on bulk Si are appealing due to the relative ease of integration with mainstream CMOS processing. However, there are severe critical thickness constraints on the strained SiGe channel for Ge compositions above 40 at. %. Reducing the lattice mismatch by growing the strained SiGe channel on a relaxed SiGe virtual substrate allows investigation of high Ge composition channels independent of critical thickness constraints. To understand the performance possibilities for these structures, it is essential to understand the impact of channel thickness, W_{chan}, on hole mobility.

Hole mobility for 43% Ge pseudormophic SiGe channels drops for W_{chan} below 4 nm due to increased phonon and Si/SiGe interface scattering (Figure 1). The 70/40 structure follows a similar trend; however, there is a large drop in Ge concentration for the 3-nm channel. The thermal budget will reduce final Ge % (and mobility), especially for thinner films, higher Ge fraction and increased strain [1]. For the strained Ge channel there is a dramatic drop in mobility for W_{chan} below 6 nm due to increased interface roughness and some drop in the Ge concentration. Mobility enhancements for SiGe heterostructres are plotted in Figure 2 as a function of Ge fraction in the strained layer for bulk Si and relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate. Use of a virtual substrate can produce peak mobility enhancements of up to 10X. Peak enhancements are limited to 4X for strained SiGe channels on bulk Si due to the mobility degradation for thinner channels required at high Ge compositions.



▲ Figure 1: Hole mobility enhancement as a function of strained SiGe channel thickness, W_{chan} for strained Ge on a relaxed SiGe virtual substrate (triangles), strained $Si_{0.3}Ge_{0.7}$ on relaxed $S_{i0.6}Ge_{0.4}$ (squares) and strained $Si_{0.57}Ge_{0.43}$ on bulk Si (circles). Drop in mobility for strained SiGe channels for W_{chan} below 4 nm. Drop in mobility below 6 nm for Ge channels due to interface roughness. Ge composition in strained SiGe (Y %) and relaxed virtual substrate (X%) are denoted Y/X for each point.



▲ Figure 2: Mobility enhancement as a function of Ge fraction for strained SiGe channels grown on bulk Si (squares) and relaxed $Si_{0.6}Ge_{0.4}$ virtual substrate (diamonds). Solid symbols: results from this work. Open symbols: [2]. Strained SiGe channel thickness noted for each point. Critical thickness constraints limit channel thickness for strained SiGe channels on bulk Si, restricting mobility enhancements for high Ge compositions.

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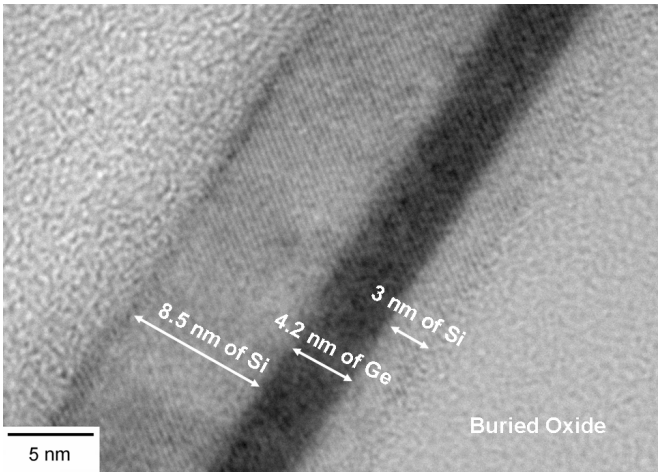
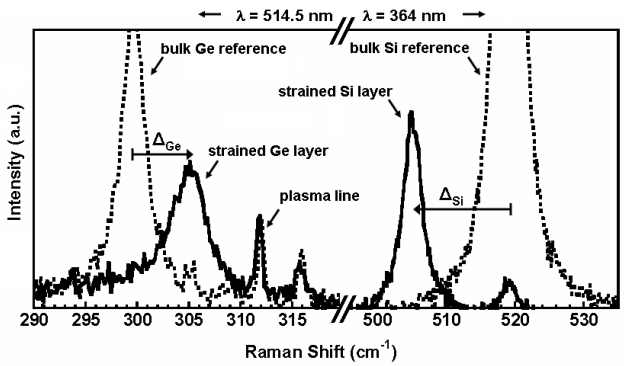
Strained-Si/strained-Ge Heterostructure-on-insulator for Improved CMOS Performance

L. Gomez, M.K. Kim, J.L. Hoyt
Sponsorship: SRC/FCRP MSD

Geometric scaling of device dimensions can no longer provide the necessary current drive enhancements to continue historic performance gains. Novel channel materials as well as strain can provide enhanced transport characteristics that help to maintain this historic trend. Thin-body devices can also offer the benefit of improved electrostatic control in deeply scaled MOSFETs. In previous work, fully depleted MOSFETs were fabricated on Si/SiGe heterostructures (55% Ge) to realize both enhanced transport for electrons and holes and improved subthreshold characteristics [1]. Subthreshold swing was improved over heterostrucutre-on-bulk devices and was observed to be 66-70 mV/dec. Mobility enhancements of 1.9x and 2.8x were observed for electrons and holes, respectively, at an inversion charge density of $1.5x10^{13}$ cm^{-2}. Heterostructure-on-bulk MOSFETs with pure Ge buried channels have exhibited mobility enhancement factors of 10x for holes [2-3], motivating the fabrication of strained-Ge heterostructures on insulator. The Ge-HOI substrate combines the excellent electrostatic characteristics observed in UTB SOI with the high mobility benefits of a strained-Si/strained-Ge heterostructure. In this work, Ge HOI is fabricated by epitaxial growth and layer transfer by bond and etch-back. A process was developed to grow thin Ge films on strained Si using an intermittent SiGe passivating layer (strained Si layers were pseudomorphic to 50% Ge relaxed SiGe layers). Figure 1 presents a cross-sectional transmission electron microscopy image of a Ge-HOI substrate. Figure 2 presents Raman analysis that was conducted to verify strain retention in the buried Ge layer. Further development is being conducted to fabricate short channel devices on these substrates.



▲ Figure 1: Crosssectional transmission electron microscopy image of the final Ge-HOI substrate. The layers in this structure were grown to be pseudomorphic to relaxed $Si_{0.5}Ge_{0.5}$.



▲ Figure 2: Raman spectra from the Ge-HOI substrate using 364- and 514.5-nm excitation to obtain a signal from the Si cap and Ge buried layer, respectively. The UV and visible Raman spectra are shown for the Ge-Ge and Si-Si LO phonons from bulk crystals (dotted black curves) and the Ge-HOI substrate (black solid curve). Raman analysis courtesy M. Canonico, Freescale Semiconductor.

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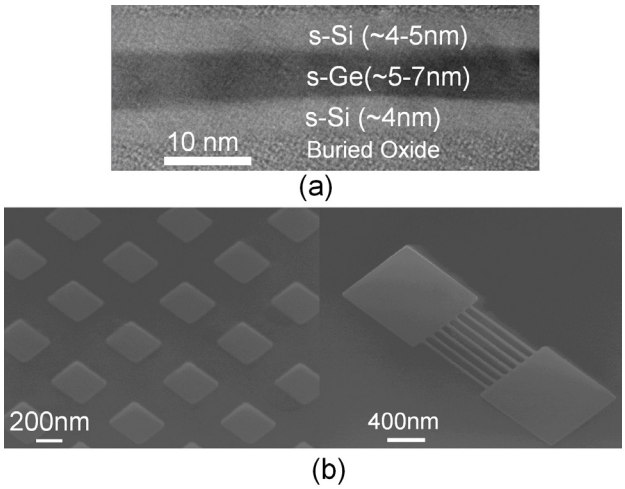
Strain in Nano-scale Patterned Strained Si/strained Ge Heterostructures on Insulator

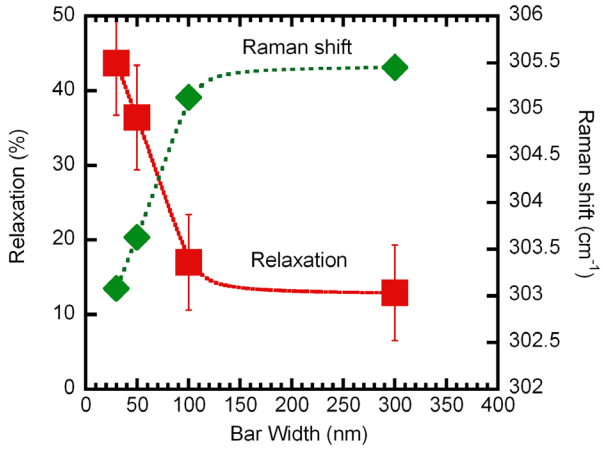
P. Hashemi, L. Gomez, J.L. Hoyt
Sponsorship: SRC/FCRP MSD

Possessing superior electron and hole transport characteristics, thin-body strained Si/ strained-SiGe (Ge)/strained Si heterostructures on insulator (HOI) MOSFETs are possible candidates for future low-power CMOS [1]. However, when these substrates are patterned into nano-scale mesas and fins, some changes in the stress profile are expected that may either degrade or enhance the mobility of the devices. Here, we report the variation of the stress profile in the strained-Si and strained-Ge layers as a function of the patterning geometry and thickness of strained layers. Finite element simulations in TAURUS TSUPREM IV™ were also performed to support experimental results. Strained heterostructure substrates used in this work were fabricated by a bond-and-etch-back method followed by thinning the cap layer by wet oxidation and removal. Figure 1(a) shows a typical TEM image of such a substrate. Scanning electron beam lithography with HSQ as a negative tone resist was used to create nano-scale long bars and mesas with sub-300-nm geometries. The density of these features is a key to achieving a measurable Raman signal to analyze the stress profile. The pattern transfer was performed in an RIE system stopping at the buried oxide interface. Figure 1(b) shows sample SEM images of patterned mesas and long bars.

UV Micro-Raman spectroscopy with 325-nm He-Cd and 364-nm Ar-Ion laser lines was used to explore the stress profile in the patterned ultra-thin strained Ge and strained Si layers, respectively. Figure 2 shows the relaxation percentage and position of the Raman peak in the strained Ge layer as a function of bar width for patterned long bars. As can be seen from this figure, the relaxation in strained Ge is increased when the pattern width is reduced. For 30-nm-wide patterns, a relaxation of around 43% is measured. Finite element stress simulations demonstrate that the longitudinal stress component along the bars is almost maintained while the in-plane component tends to relax in the narrow direction of the bars. As a result, the biaxial stress profile of the unpatterned structure tends to move towards uniaxial strain for ultra-narrow structures, which can further enhance hole transport properties. On the other hand, the results on relaxation in nano-scale pattern mesas indicate a general trend of relaxation with decreasing aspect ratio. As an example, the 100-nm, square-shape mesas show nearly 33% relaxation (assuming isotropic biaxial strain) indicating that a large amount of strain can still be preserved in patterned regions suitable for fabrication of planar HOI MOSFETs.



▲ Figure 1: (a) A TEM image of the HOI structure before patterning. (b) Tilted SEM images of the 300-nm-wide patterned square mesas (left) and 24-nm-wide patterned multi-fin mesas (right).



▲ Figure 2: Relaxation and Raman peak position as a function of the bar width in the strained-Ge layer. Raman measurements and analysis courtesy of M. Canonico, Freescale Semiconductor, Inc.

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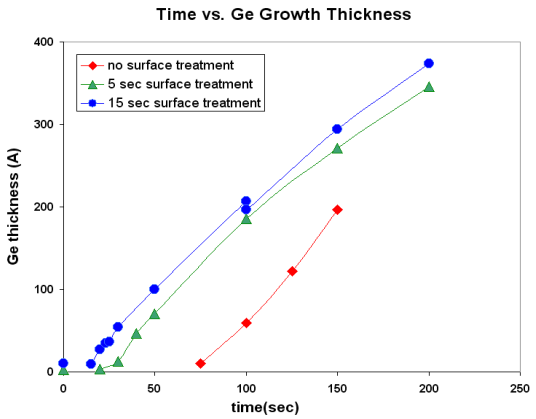
Epitaxial Growth of Ultrathin Ge on Si Substrates

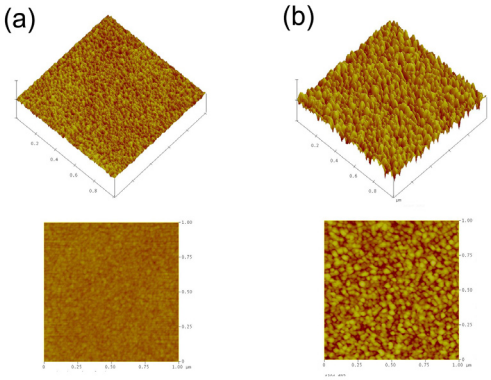
M. Kim, L. Gomez, J.L. Hoyt
Sponsorship: DARPA, NSF Graduate Research Fellowship

Growing ultrathin, uniform germanium epitaxial films with minimal crystal defect density is desirable for several applications to emerging technologies. For example, multilayer structures of Ge and SiGe on Si wafers are used for enhanced-mobility heterostructure-on-insulator (HOI) MOSFETS, and thin Ge films are used as seed layers in CMOS-compatible photodetectors. However, due to the 4% mismatch in lattice size, the initial stages of Ge growth on Si substrates show a 3-D growth mode, in which Ge initially forms islands and then coalesces to form a more uniform surface [1-2]. To improve the morphology of Ge films with thickness in the range of 20A to 50A, several growth parameters and surface treatment methods were studied using an Applied Materials Epi Centura Reactor. Varying growth temperature and pressure, the optimal condition for ultrathin Ge films on Si substrates was determined to be 365ºC and 60T, with 5slpm of Hydrogen flow to the slit.

A surface treatment consisting of a SiGe pulse before Ge growth improves the surface smoothness greatly, as well as enhancing the growth rate. Before Ge growth, a short "pulse" of 5-15 seconds of 50% SiGe was used to treat Silicon surface, and this treatment was shown to enhance Ge growth on Si substrates, as shown in Figure 1. Figure 2 shows improved film uniformity for SiGe-pulse treated samples. With this new technique, the RMS values as well as average peak-to-valley heights are improved by a factor of ~3.



▲ Figure 1: The germanium thickness as a function of growth time. The graph shows a reduced incubation period for SiGe-pulse treated samples. Epitaxial Ge was grown at 365ºC, 60T on P- CZO Si wafers in Applied Materials's "Epi Centura" System.



▲ Figure 2: The 1um x 1um AFM scans of 35A-thick Ge films grown on Si substrates, (a) with 15-sec SiGe pulse surface treatment and (b) without SiGe pulse. For (a), RMS is 0.251 nm, with average peak heights of 1.4 nm. Without the surface treatment, the Ge film is much rougher, with RMS value of 0.686 nm and peak heights of 5 nm, as shown in (b).

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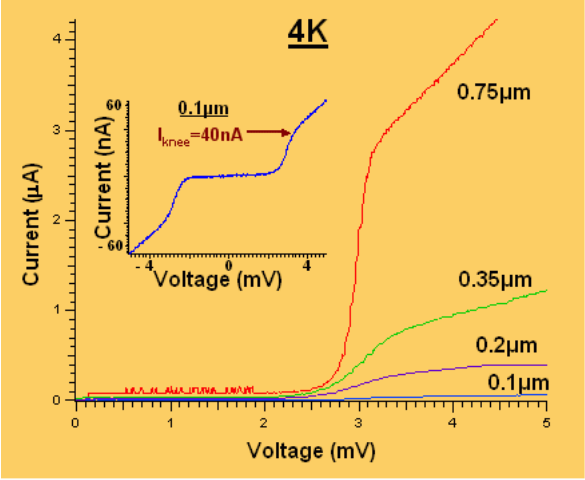
Niobium Superconducting Persistent-current Qubits with Deep Submicron Josephson Junctions

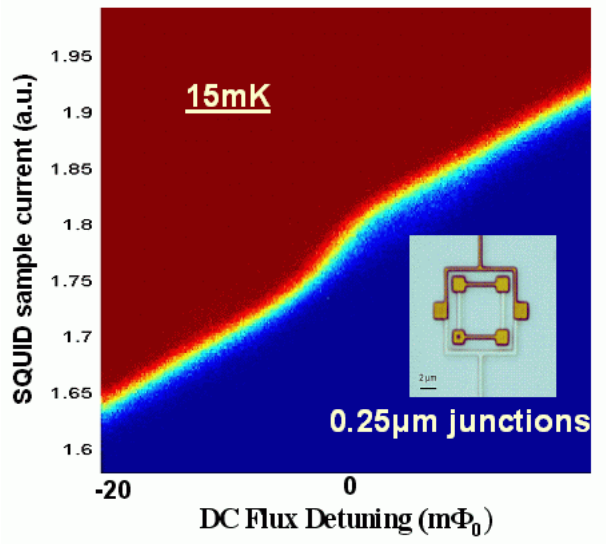
D.M. Berns, W.D. Oliver, S.O. Valenzuela, T.P. Orlando, V. Bolkhovsky, E. Macedo

Quantum computation holds the potential to solve problems currently intractable with current computers. The basic component of a quantum computer is the "qubit," the quantum analog to today's bits. Although any two-level quantum system could serve as a qubit; however, the qubit must satisfy two major criteria for practical quantum computing: long coherence times and the ability to scale to thousands of qubits. Persistent-current (PC) qubits are promising candidates for realizing such a large-scale quantum computer. The PC qubit is a superconducting circuit with Josephson junction (JJ) elements that can be effectively operated as a two-level quantum system [1].

With a tri-layer process using optical lithography, we can create the deep-submicron JJs required to realize large qubit tunnel-couplings, which allow improved immunity to dielectric-induced decoherence, and there is no foreseeable barrier to large-scale integration. We have recently begun measuring and characterizing the PC qubits designed with these deep-submicron JJs fabricated with the Nb-Al/AlOx-Nb trilayers. Initital testing of the JJs shows excellent performance down to sizes necessary for long decoherence times (Figure 1), and first studies of how the ground state of the new qubits changes as the applied DC flux is swept show the large tunnel-couplings we were aiming for (Figure 2).



▲ Figure 1: IV traces taken at 4K for a few different test junctions, from 0.75 um down to 0.1um. Blown up in the inset is the 0.1-um junction IV and we see a knee current of 40 nA and a very large subgap resistance.



▲ Figure 2: Qubit step taken at dilution refrigerator temperatures with the device seen in the inset, where the larger junctions are 250 nm on a side. One can clearly see that as the applied DCmagnetic flux is changed, the ground state changes from one circulating current state to the other.

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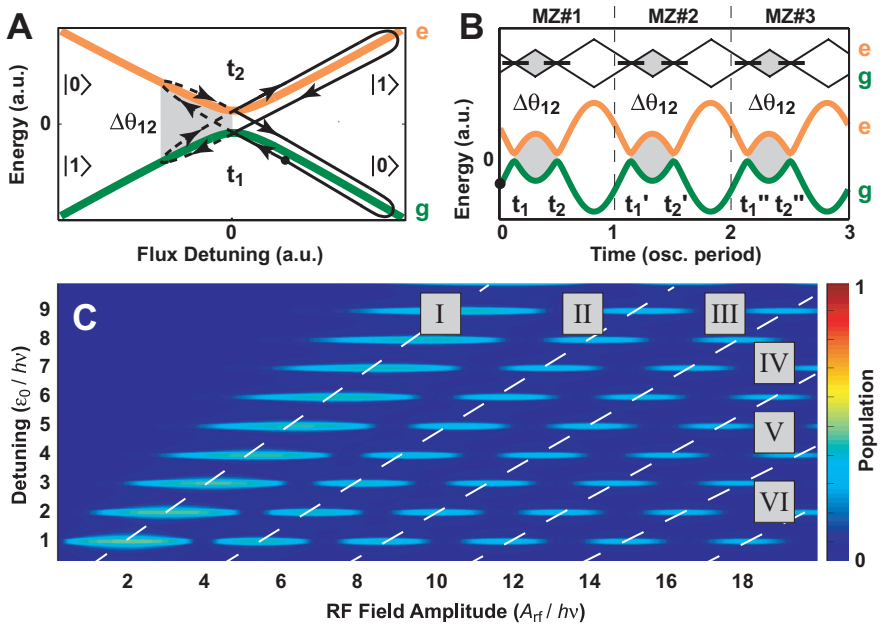
Mach-Zehnder Interferometry in a Persistent-current Qubit

W.D. Oliver, Y. Yu, J.C. Lee, K.K. Berggren, L.S. Levitov, T.P. Orlando

We have demonstrated Mach-Zehnder (MZ)-type interferometry with a niobium superconducting persistent-current qubit. These experiments exhibit remarkable agreement with theory, and they will find application to non-adiabatic qubit control methods. The qubit is an artificial atom, the ground and first-excited states of which exhibit an avoided crossing. Driving the qubit with a large-amplitude harmonic excitation sweeps it through this avoided crossing two times per period. The induced Landau-Zener (LZ) transitions at the avoided crossing cause coherent population transfer between the eigenstates, and the accumulated phase between LZ transitions varies with the driving amplitude. This is analogous to a Mach-Zehnder interferometer, in which the LZ transition is the beamsplitter and the relative phase accumulated between LZ transitions is the optical path-length difference between the arms of the interferometer. Over the entire length of the microwave driving pulse, we have a sequence of Mach-Zehnder interferometers. We have observed MZ quantum interference fringes as a function of the driving amplitude for single- and multi-photon excitations.



▲ Figure 1 : (a) Energy of the two-level system. Starting at the marker, the qubit state is swept through the avoided crossing twice, accumulating a phase between the LZ transitions that occur. (b) The corresponding energy variation over a few pulse periods. The sequence of LZ transitions and phase accumulation are analogous to a sequence of Mach-Zehnder interferometers. (c) Qubit population as a function of driving amplitude. We see the Bessel dependence to the Mach-Zehnder-like quantum interference for n-photon transitions.

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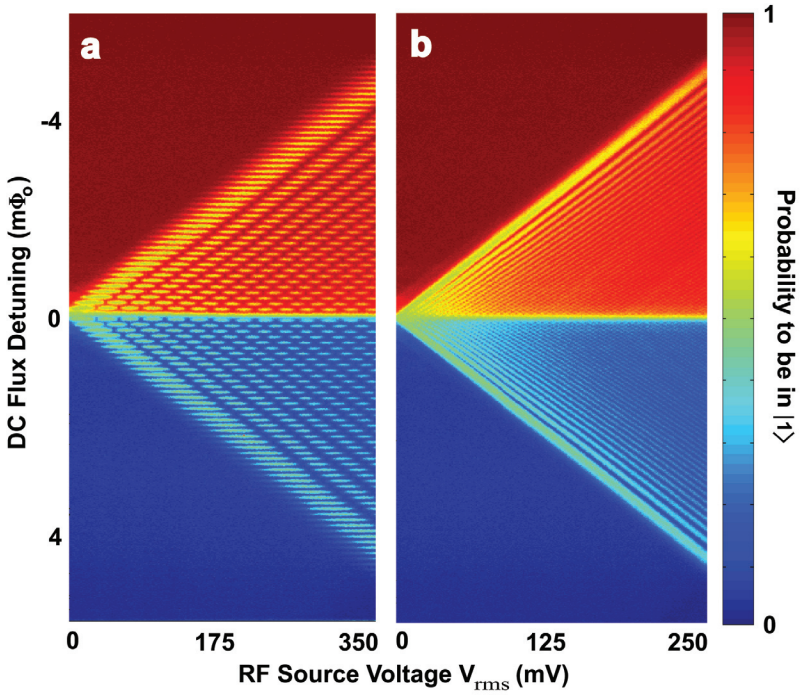
Coherent Quasiclassical Dynamics of a Niobium Persistent-current Qubit

D.M. Berns, W.D. Oliver, S.O. Valenzuela, A.V. Shytov, K.K. Berggren, L.S. Levitov, T.P. Orlando

We have recently demonstrated Mach-Zehnder (MZ)-type interferometry in the persistent-current (PC) qubit, in the strong driving limit [1]. We have now extended this work to much lower driving frequencies [2]. By driving our system at frequencies smaller than our linewidth, we have observed a new regime of quasiclassical dynamics within the strong driving limit. Now a transition at a DC flux detuning resonant with n photons is assisted by neighboring resonances. In this regime we find remarkable agreement with theory by assuming the population transfer rate for the nth photon resonance is the sum of rates from all other resonances.



▲ Figure 1 : Qubit population as a function of driving amplitude. (a) Driving frequency = 270 MHz. We see the Bessel dependence to the Mach-Zehnder-like quantum interference for n-photon transitions. (b) Driving frequency = 90 MHz. Individual resonances are no longer distinguishable but we still see coherent quantum interference.

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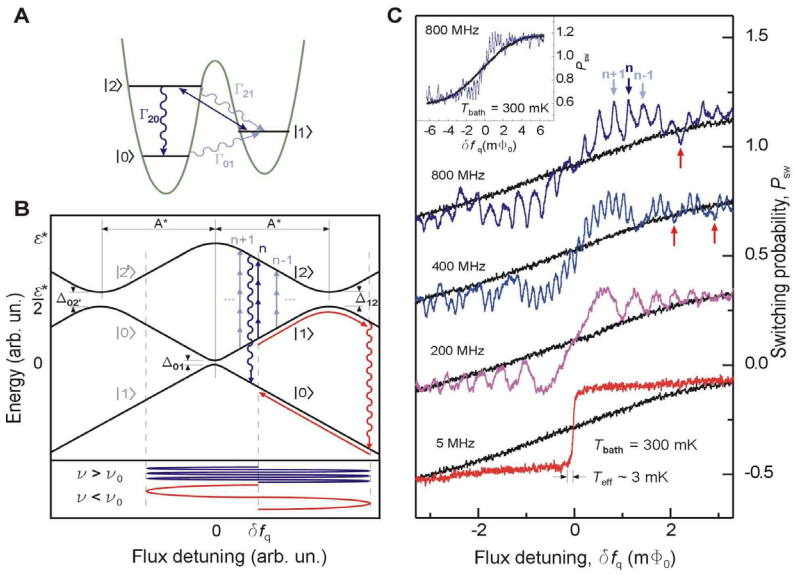
Microwave-induced Cooling of a Superconducting Qubit

S.O. Valenzuela, W.D. Oliver, D.M. Berns, K.K.Berggren, L.S. Levitov, T.P. Orlando

We have recently demonstrated microwave-induced cooling in a superconducting flux qubit [1]. The thermal population in the first-excited state of the qubit is driven to a higher-excited state by way of a sideband transition. Subsequent relaxation into the ground state results in cooling. Effective temperatures as low as 3 millikelvin are achieved for bath temperatures from 30 - 400 millikelvin, a cooling factor between 10 and 100. This demonstration provides an analog to optical cooling of trapped ions and atoms and is generalizable to other solid-state quantum systems. Active cooling of qubits, applied to quantum information science, provides a means for qubit-state preparation with improved fidelity and for suppressing decoherence in multi-qubit systems.



▲ Figure 1 : Sideband cooling in a flux qubit. (a) Double-well illustration of cooling. External excitation transfers thermal population from state 1 to state 2, from which it decays to the ground state 0. (b) Band diagram illustration of cooling. One to two transitions are driven resonantly at high driving frequencies and occur adiabatically at low driving frequency. (c) Thermal population cooled at different frequencies. Cooling from 300mK to as low as 3mK is shown.

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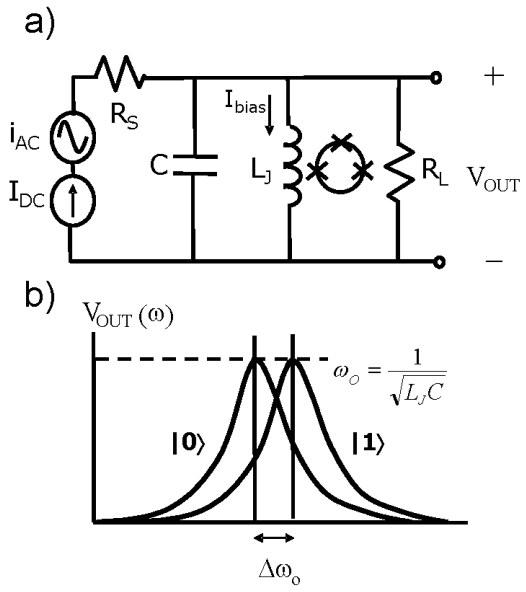
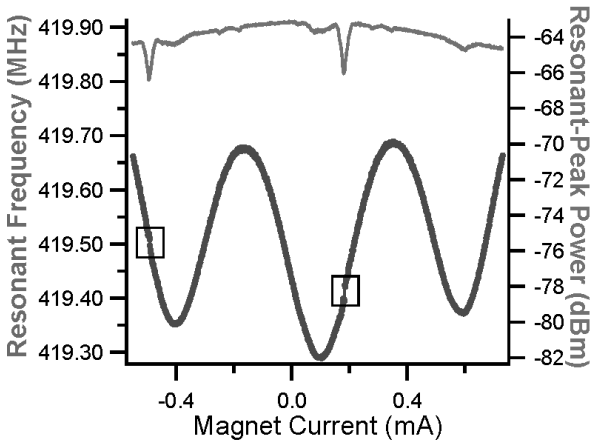
Resonant Readout of a Persistent-current Qubit

J.C. Lee, W.D. Oliver, T.P. Orlando
Sponsorship: DURINT, DTO, NSF

The two logical states of a persistent-current (PC) qubit correspond to oppositely circulating currents in the qubit loop. The induced magnetic flux associated with the current either adds to or subtracts from the background flux. The state of the qubit can thus be detected by a DC SQUID magnetometer inductively coupled to the qubit. We have implemented a resonant technique that uses a SQUID as a flux-sensitive Josephson inductor for qubit readout. This approach keeps the readout SQUID biased at low currents along the supercurrent branch and is more desired for quantum computing applications in reducing the level of decoherence on the qubit. By incorporating the SQUID inductor in a high-Q on-chip resonant circuit, we can distinguish the two flux states of a niobium PC qubit by observing a shift in the resonant frequency of the readout circuit. The nonlinear nature of the SQUID Josephson inductance, as well as its effect on the resonant spectra of the readout circuit, was also characterized.



▲ Figure 1: a) The SQUID inductor is incorporated in a resonant readout circuit. It is inductively coupled to a PC qubit to detect its state. b) A transition of the qubit state changes the Josephson inductance of the SQUID and can be sensed as a shift in the resonant frequency of the readout circuit.



▲ Figure 2: Experimental results at 300 mK: the lower plot (left axis) shows the modulation of the resonant frequency with external magnetic field. Qubit steps corresponding to transitions between opposite flux states were observed at every 1.3 periods of the SQUID lobe. The upper plot (right axis) shows the corresponding peak amplitude of the resonant spectrum. The dip in peak power coincides with the qubit step.

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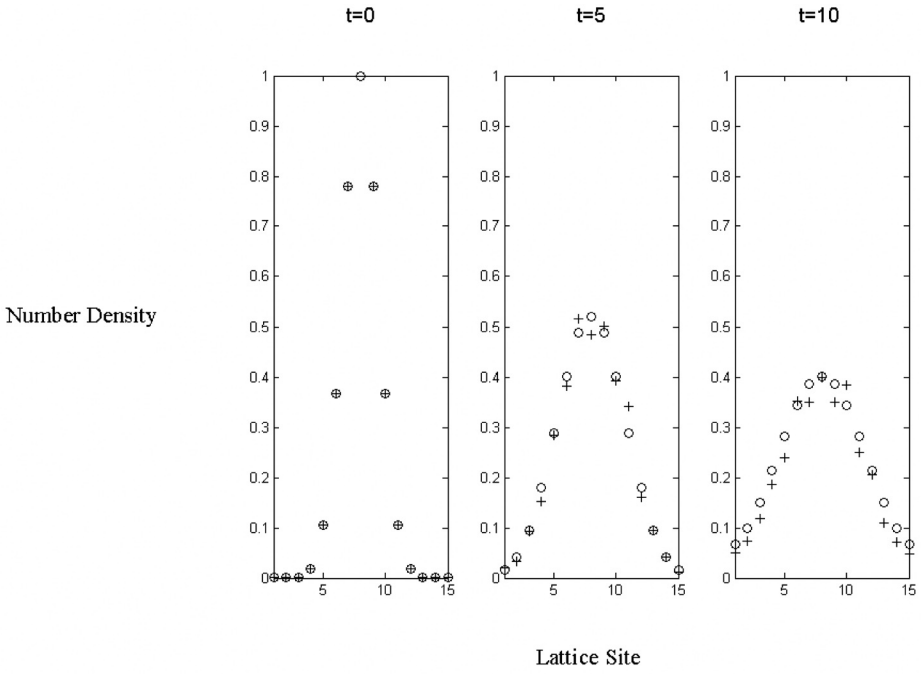
Type-II Quantum Computing Using Superconducting Qubits

D. Berns, W.M. Kaminsky, B. Cord, K. Berggren, W. Oliver, T.P. Orlando (in coll. with J. Yepez (Air Force Laboratories)
Sponsorship: AFOSR, Fannie and John Hertz Foundation

The Factorized Quantum Lattice-Gas Algorithm (FQLGA) [1] is a quantum version of classical lattice-gases (CLG) [2]. The CLGs are an extension of classical cellular automata with the goal of simulating fluid dynamics without reference to specific microscopic interactions. The binary nature of the CLG lattice variables is replaced for the FQLGA by the Hilbert space of a two-level quantum system. The results of this replacement are similar to that of the lattice-Boltzmann model, but with a few significant differences [3]. The first is the exponential decrease in required memory. The second is the ability to simulate arbitrarily small viscosities.

We have recently developed two implementations of the algorithm for the 1D diffusion equation using the PC Qubit [4]. The first consists of initializing the qubits while keeping them in their ground state and then performing the collision by quickly changing their flux bias points and then performing a single /2 pulse (Figure 1). This initialization technique could prove quite useful, since relaxation effects are avoided, but the way we have implemented the collision is not easily generalized to other collisions. A more general collision implementation was then developed by decomposing the unitary collision matrix into a sequence of single qubit rotations and coupled free evolution. The single qubit rotations then also serve to initialize the fluid's mass density.



▲ Figure 1: Simulation of the FQLGA for 1D diffusion is pictured (o) alongside simulation of the first proposed implementation (+). The expected diffusion of a Gaussian is observed.

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Scalable Superconducting Architecture for Adiabatic Quantum Computation

W.M. Kaminsky, S. Lloyd, T.P. Orlando
Sponsorship: Fannie and John Hertz Foundation

Adiabatic quantum computation (AQC) is an approach to universal quantum computation in which the entire computation is performed in the ground state of a suitably chosen Hamiltonian [1]. As such, AQC offers intrinsic protection against dephasing and dissipation [2-3]. Moreover, AQC naturally suggests a novel quantum approach to the classically intractable constrained minimization problems of the complexity class NP. Namely, by exploiting the ability of coherent quantum systems to follow adiabatically the ground state of a slowly changing Hamiltonian, AQC promises to bypass automatically the many separated local minima occurring in difficult constrained minimization problems that are responsible for the inefficiency of classical minimization algorithms. To date, most research on AQC [4-8] has focused on determining the precise extent to which it could outperform classical minimization algorithms. The tantalizing possibility remains that---at least for all practical purposes---AQC offers at least a large polynomial, and often an exponential, speedup over classical algorithms. However, it may be the case that in the same way the efficiency of many practical classical algorithms for NP problems can be established only empirically, the efficiency of AQC on large instances of classically intractable problems can be established only by building a large-scale AQC experiment.

To make feasible such a large-scale AQC experiment, we have proposed a scalable architecture for AQC based on the superconducting persistent-current (PC) qubits [9-10] already under development here at MIT. As first proposed in [11], the architecture naturally incorporates the terms present in the PC qubit Hamiltonian by exploiting the isomorphism [12] between antiferromagnetic Ising models in applied magnetic fields and the canonical NP-complete graph theory problem Max Independent Set. Such a design notably removes any need for the interqubit couplings to be varied during the computation. Moreover, since the Max Independent Set remains NP-complete even when restricted to planar graphs where each vertex is connected to no more than 3 others by edges, a scalable programmable architecture capable of posing any problem in the class NP may simply take the form of a 2D, hexagonal, square, or triangular lattice of qubits. Finally, the latest version of the architecture [13] permits interqubit couplings to be limited to nearest-neighbors and qubit measurements to be inefficient.

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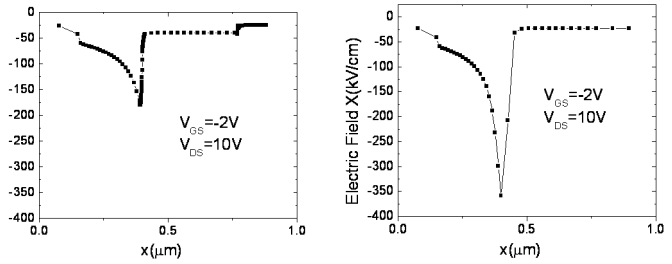
Improvement of Electron Velocity in GaN HEMTs by Electric Field Engineering

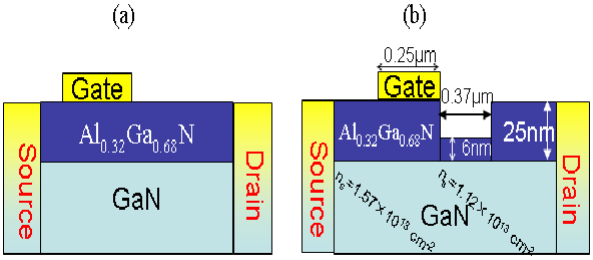
X. Zhao, J.W. Chung, T. Palacios
Sponsorship: ONR, MIT, MTL

Electron velocity influences both the intrinsic delay and drain delay of gallium nitride (GaN) High Electron Mobility Transistors (HEMTs). Although the peak electron velocity in AlGaN/GaN structures is 2.5×10^7cm/s, the electron velocity decreases very fast due to polar optical phonon scattering for electric fields in excess of 150kV/cm [1]. As seen in Figure 1a, in standard GaN HEMT devices, the average electric field under the gate along the channel direction far exceeds the optimal value for peak electron velocity. This high electric field results in an average electron velocity of 1.5×10^7cm/s, significantly lower than the peak velocity. In this project, we propose a new GaN HEMT structure with a recessed drain access region to reduce the electric field in the drain of these transistors. We have used Silvaco/Atlas to simulate these new devices. Figure 2 shows the structure of a conventional AlGaN/GaN HEMT and the novel HEMT device proposed in this work.

In the recessed devices, the carrier concentration underneath the recess region is lower than elsewhere, which redistributes the electric field in the channel. Figure 1 shows the electric field along the channel in two structures of Figure 2. Due to the lower electric field peak in the novel structure, the average electron velocity is boosted by 50%. On the other hand, in our simulations we have not observed any increase in the effective gate length due to the drain recess. This fact in combination with the enhanced electron velocity makes this new structure extremely promising for millimeter- and submillimeter-wave applications.



▲ Figure 1: Electric field along the channel direction in conventional AlGaN/GaN HEMT (a) and along a novel structure with recessed drain access region (b). The average electron velocities are 1.53×10^7cm/s and 2.41×10^7cm/s, respectively.



▲ Figure 2: Diagram of a conventional AlGaN/GaN HEMT structure (a) and the novel HEMT structure with a recess in the drain access region (b). The width of the recess region is 0.37μm.

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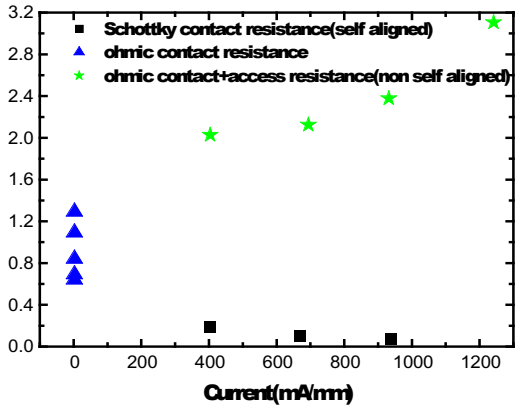
Schottky Drain AlGaN/GaN HEMTs for Millimeter-wave Applications

X. Zhao, J.W. Chung, T. Palacios
Sponsorship: ONR, MIT, MTL

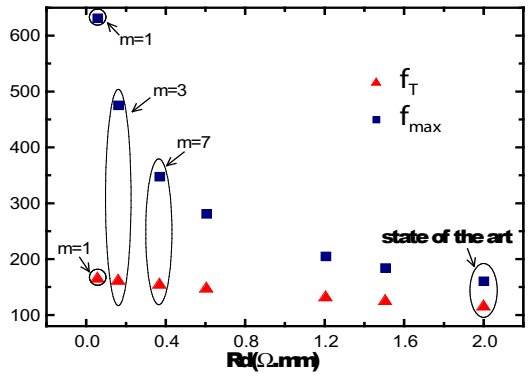
The drain parasitic resistance is one of the main factors limiting the current gain cut-off frequency (f_T) and the power gain cut-off frequency (f_{max}) in high performance AlGaN/GaN HEMTs [1]. The drain parasitic resistance consists of two components: the contact resistance between the metal and the channel and the access resistance due to the distance between the gate edge and drain contact. In this project, we demonstrate a new drain contact technology based on the use of a Schottky metallization.

The use of a Schottky contact in the drain of a HEMT has two major advantages. First, for moderate current levels, the differential resistance of a Schottky contact is much lower than what is achievable with conventional ohmic technology. Second, due to the low thermal budget required in Schottky contact, these contacts can be easily self-aligned to the gate to eliminate the access resistance. Therefore, Schottky drain contact has the potential to outperform the ohmic contact both in contact resistance and access resistance.

Using an Agilent 4155 parameter analyzer, we have measured the ohmic contact and the Schottky contact resistances as a function of the drain current (Figure1). We have also measured the total drain parasitic resistance in devices with conventional ohmic drain contacts. In conventional AlGaN/GaN HEMTs, the total drain parasitic resistance is above 2 Ω·mm and increases with the drain current. In contrast, with use of a Schottky drain contact, the contact resistance is ~0.2 Ω·mm at 500-mA/mm-current level. We have also used the commercial software ADS to simulate the high-frequency performance of Schottky drain AlGaN/GaN HEMTs. As shown in Figure 2, reducing the drain parasitic resistance from 2 Ω·mm to 0.2 Ω·mm increases the f_T from 116 GHz to 162 GHz and increases f_{max} from 162 GHz to 477 GHz.



▲ Figure 1: Measurement of the ohmic contact resistance, Schottky contact resistance and the total parasitic resistance in ohmic contact devices.



▲ Figure 2: Small signal simulations of f_T and f_{max} as a function of R_d. Reducing the drain parasitic resistance from 2Ω·mm to 0.2 Ω·mm increases f_T from 116 GHz to 162 GHz and increases f_{max} from 162 GHz to 477 GHz.

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Estimation of Trap Density in AlGaN/GaN HEMTs from Subthreshold Study

J.W. Chung, X. Zhao, T. Palacios
Sponsorship: ONR, MIT, MTL, KFAS

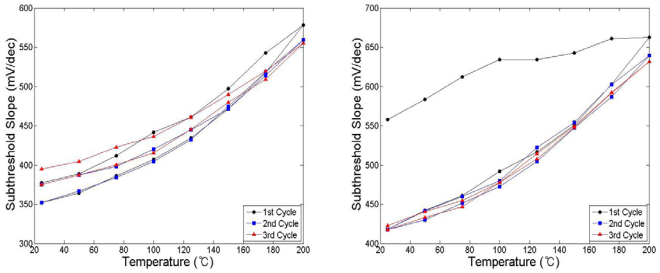
The AlGaN/GaN high electron mobility transistors (HEMTs) have shown outstanding performance on high power and high frequency applications. However, AlGaN/GaN HEMTs suffer from a much higher subthreshold slope than the theoretical limit of 60 mV/decade, an issue that has been only barely addressed. Subthreshold slope (S) is very important not only to assure excellent pinch-off and low dissipated power in digital applications but also for achieving good power-added efficiency in analog applications. Most crucially, the subthreshold slope can be used to quantify the trap density in the gate-modulated region of AlGaN/GaN HEMTs. The presence of traps in this region degrades gate modulation efficiency, which is closely related to the subthreshold slope and ultimately to high-frequency performance. In this paper, we first demonstrate effects of thermal annealing on the subthreshold slope in AlGaN/GaN HEMTs. Then, based on the temperature dependence of the subthreshold slope, we introduce a new method to estimate interface trap density in these devices.

Figure 1 shows the temperature dependence of S in two different transistors with different initial values of S. Notably, when the initial subthreshold slope is very high (typically in excess of 500 mV/dec, Figure 1b), reproducible results are achieved only after the first heating sequence. From the change of S with temperature (T), the interface trap density in these devices can be extracted. By analogy with MOSFETs, the equation for the subthreshold slope in HEMTs is given by the equation,

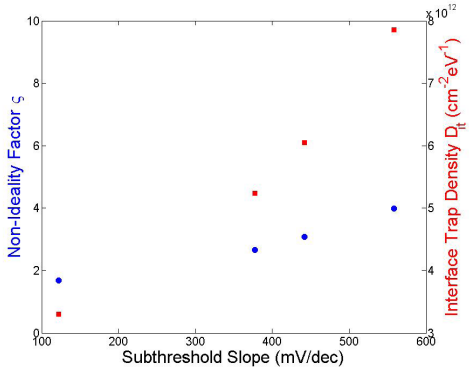
$$S = \frac{kT}{q}\ln(10)\left(1+\frac{C_Q + C_{it}}{C_i}\right) = \frac{kT}{q}\ln(10)(1+\varsigma) \rightarrow \frac{k}{q}\ln(10)(1+\varsigma) \quad (1)$$

where C_i is AlGaN layer capacitance, C_Q is quantum capacitance, and C_{it} is associated with the interface trap density. Here, ς is a non-ideality factor related to the interface trap density. The variable ς can be calculated from the equation (1) after measuring the slope from the S vs. T curve. As shown in Figure 2, ς varies between 2 and 4. From the value of ς, we estimated an interface trap density of $3\times10^{12}\sim 8\times10^{12}$ $cm^{-2}eV^{-1}$, assuming C_Q is negligible. This value is similar to previously reported data obtained from low-frequency noise data [1] or from gate-drain conductance and capacitance-dispersion studies [2].

In conclusion, we have studied the change in the subthreshold slope in AlGaN/GaN HEMTs with temperature. Using this experiment, we propose for the first time a relatively simple way to estimate interface trap density. The understanding of this interface trap is critical to optimize the gate-modulation efficiency of these transistors and maximize their high-frequency performance.



▲ Figure 1: Dependence of subthreshold slope on temperature for two different transistors. (a) Transistors with an initial subthreshold slope below 500 mV/dec typically show a very reproducible linear dependence with temperature. (b) However, transistors with higher initial subthreshold slope reach stable operation only after the first heating sequence.



▲ Figure 2: Calculated non-ideality factor and interface trap density. Slight variations of ς might be caused by differences in gate leakage current and its behavior with temperature.

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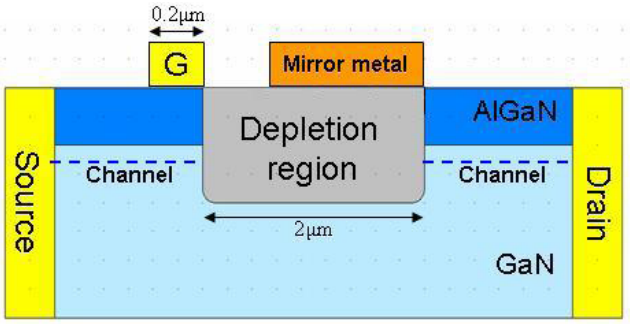
Effect of Image Charges in the Drain Delay of AlGaN/GaN HEMTs

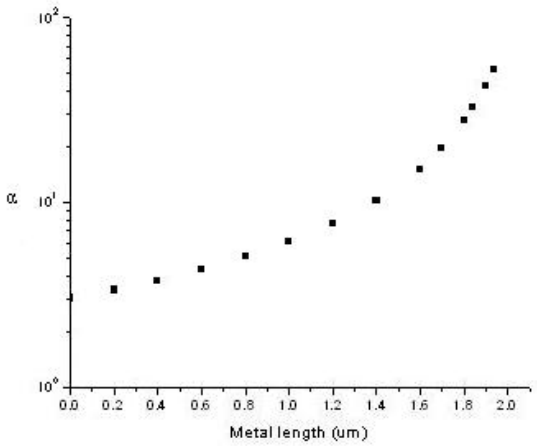
J.W. Chung, X. Zhao, T. Palacios
Sponsorship: ONR, MIT, MTL, KFAS

The electron delay in high electron mobility transistor (HEMT) can be divided into three different components: intrinsic delay, channel delay, and drain delay [1]. Both the intrinsic and channel delays decrease when one scales down the device. However, the drain delay remains constant and ultimately limits the maximum frequency performance of these transistors. From a physical point of view, the drain delay is the time taken by the electrons to cross the depletion region at the drain side of the gate. Mathematically, the drain delay can be expressed as $\tau_{drain} = w_d / (\alpha v_e)$, where w_d is the width of the depletion region, v_e is the electron velocity and α is a constant given by the effect of image charges. The value of α has been extensively studied in heterojunction bipolar transistors. In these devices, α is equal to 2 [2]. However, to the best of our knowledge the value of α has not been studied in field effect transistors. In this paper, we have calculated the value of α in AlGaN/GaN HEMTs. Through simulations, we have found that α represents the ratio of injected charges in the depletion region to image charges in the source side of the channel. In standard HEMTs, α equals 3. We have also found that α can be engineered through the introduction of additional "mirror" metal to the original AlGaN/GaN HEMT structure.

Depending on the location and length of the "mirror" metal, α can vary significantly due to a portion of image charges "imaging" onto the metal. Figure 1 shows the standard AlGaN/GaN HEMT structure with the "mirror" metal. As the length of the "mirror" metal increases, α increases and the drain delay decreases. Figure 2 illustrates α as a function of the length of the "mirror" metal from the right edge of the depletion region. By using these simulations, the transistor can be engineered to have a value of α at least three times higher than in standard devices. This improvement in α significantly reduces the drain delay and increases linearity with drain voltage of these transistors, which make it extremely attractive for future generations of high-speed devices.



▲ Figure 1: Standard AlGaN/GaN HEMT with "mirror" metal. The size of depletion region is exaggerated to emphasize the location where the drain delay occurs. The "mirror" metal is connected to the drain.



▲ Figure 2: The α increases as the length of "mirror" metal on the depletion region increases toward the gate.

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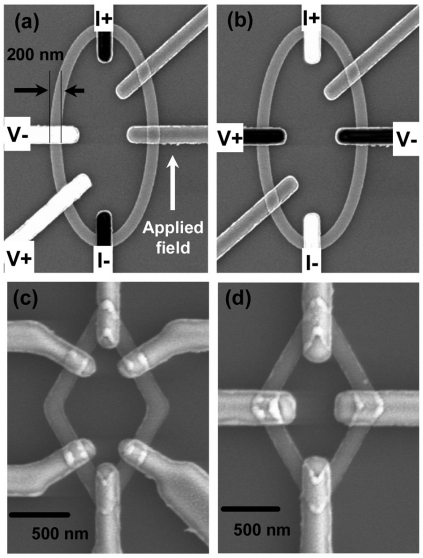
Magnetic Rings for Memory and Logic Devices

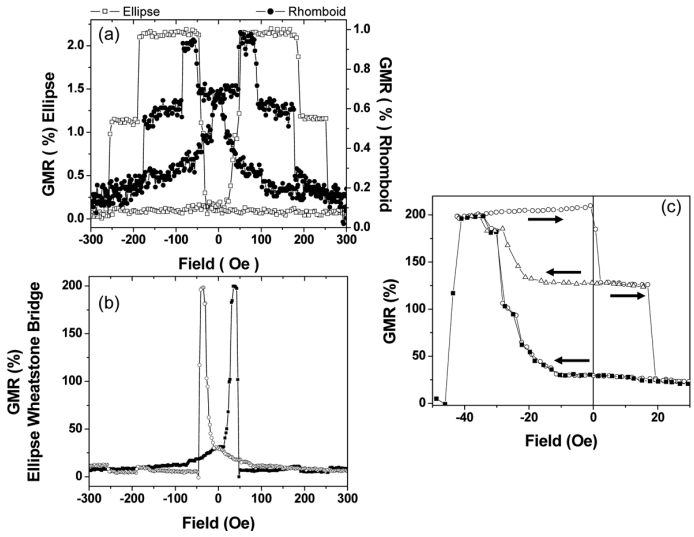
F.J. Castaño, W Jung, I.A. Colin, B. Ng, C.A. Ross
Sponsorship: Cambridge-MIT Institute, Singapore-MIT Alliance, NSF

We are using fabrication processes combining electron-beam lithography and photo-lithography to create magneto-electronic devices based on small ring-shaped multilayered magnetic elements with widths in the deep-sub-micron regime. These small structures have potential uses in magnetic-random-access memories (MRAM), magnetic logic devices, and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multilayered magnets containing two magnetic layers separated by a thin layer of either a non-magnetic metal (spin-valves) or an insulator (magnetic tunneling junctions). The resistance of such elements depends on the relative orientation (parallel or anti-parallel) between the magnetization in the read-out (free) and storage (pinned) layers. When the direction of magnetization of the free layer is switched, two different resistance levels can be detected, allowing storage of a non-volatile bit of data ("0" or "1") in each element. As an alternative bit shape, MRAMs based on ring-shaped multilayered magnets have been recently proposed [1], due to their robust magnetization reversal and the existence of flux-closure or "vortex" states.

We have fabricated devices based on elliptical, circular and rhomboidal rings made from NiFe/Cu/Co/Au pseudo-spin-valves (PSVs) [2-3], Ta/NiFe/Cu/Co/IrMn/Au spin-valves (SVs) and Co/IrMn exchanged-biased structures [4]. The magneto-transport response of PSV and SV rings is dominated by giant-magnetoresistance (GMR) and the ring-shape allows for intermediate resistance levels [2] (see also Figure 2 (a)), resulting from vortex-like magnetic configuration in both the free (NiFe) and hard (Co) or pinned (Co/IrMn) rings. Such intermediate resistance levels are not present in bar-shaped multilayered magnets and can allow storage of more than one bit of data in each cell, as well as increased functionality of logic devices. Most recently, we have found that Wheatstone-bridge contact configurations (Figure 1 (b)&(d)) can result in GMR ratios in excess of 200% (Figure 2 (b)&(c)) for modest applied fields, even though the GMR of the rings in a standard contact configuration (Figure 1 (a)&(c)) is just 1-2% (Figure 2(a)). As the soft rings reverse from both ends, two reverse walls traverse each side of the rings and the bridge becomes unbalanced. We are currently exploring operating these devices using current pulses instead of an external applied field.



▲ Figure 1: Scanning electron micrographs corresponding to elliptical (a)&(b) and rhomboidal (c)&(d) rings devices made from NiFe/Cu/Co/Au PSVs and Ta/Cu non-magnetic contact wires. The long axis of the rings ranged from 930 nm to 4 μm and the widths ranged from 80 nm to 200 nm.



▲ Figure 2: (a) Resistance versus applied field measurements using a standard contact configuration in elliptical and rhomboidal NiFe (6 nm) /Cu (4 nm) /Co (Co 4 or 5 nm) /Au (4 nm) rings, on switching both the free (NiFe) and hard (Co) layers. (b) Resistance versus applied field corresponding to a Wheatstone-bridge contact configuration on a NiFe (6 nm) /Cu (4 nm) /Co (Co 4 nm) /Au (4 nm) elliptical ring (Figure 1(b)), on switching both magnetic layers and (c) on switching back and forth only the soft NiFe ring.

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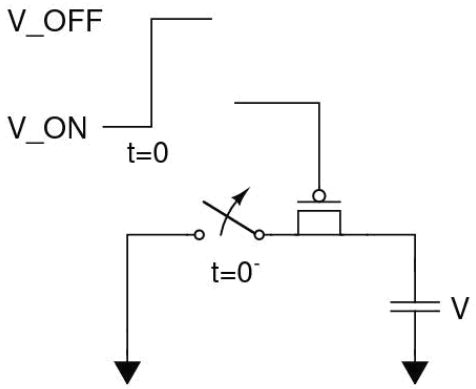
Characterization of Organic Field-effect Transistors for Circuit Applications

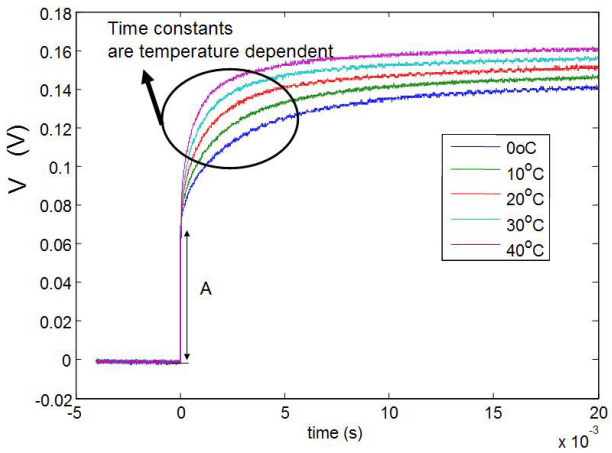
K. Ryu, D. He, I. Nausieda, V. Bulović, A.I Akinwande, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

It has been demonstrated that organic materials have semiconducting properties with mobility comparable to that of amorphous silicon (a-Si), the dominant material used in display applications. Organic field-effect transistors (OFETs) provide an exciting possibility of flexible large-area plastic electronics. Organic materials can also be deposited using a solution-based method enabling "printing" circuits. A roll-to-roll method can be used for mass production, and inkjet can be used for customized small-volume applications. One crucial area that needs to be researched is how the different charge transport mechanisms and material sets in organic transistors change the design considerations in circuit applications compared to the traditional silicon MOSFETs.

This project aims to characterize and model OFET behavior for various circuit applications. Thus far, the nonlinear contact resistance, threshold voltage, and mobility are extracted from top-contact and bottom-contact transistors with current-voltage (I-V), and capacitance-voltage (C-V) measurements. Extraction of contact resistance is found to be important in characterization of bottom-contact transistors as it obscures mobility extraction. The mobility extracted after removing the effect of contact-resistance is shown to increase with the gate field, unlike that in crystalline silicon MOSFETs [1]. The mobility dependence on gate voltage leads to an interesting study of how the channel charge comes out of the channel as an OFET turns off. When a transistor is turned off, the charge that forms the channel returns to the source and drain. This effect is called charge injection and changes the final voltage on a capacitance load. When the transistor is off, the low mobility in the OFET slows charge injection significantly. To study how mobility and trapping affects charge injection, the transient response of an OFET switch is measured as a function of temperature. Figure 1 shows the setup used to make charge injections measurements. The source and drain are grounded with the transistor on until steady-state. The mechanical switch is opened and the voltage on the load capacitor is measured as the transistor is switched off. The measurement in Figure 2 shows the transient voltage measurements on the capacitor with varying temperature. The capacitor voltage rises as the positive charge in the accumulation layer exits to the capacitive load. From the measurement, we hope to fully understand the transport mechanism in the organic semiconductor used.



▲ Figure 1: Schematic of a charge-injection measurement.



▲ Figure 2: A typical charge injection measurement from a 1000/25 μm OFET.

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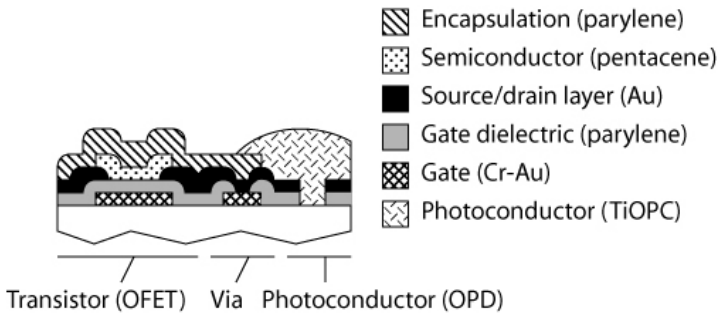
Integrated Organic Circuits and Technology for Large Area Optoelectronic Applications

I. Nausieda, K. Ryu, D. He, A.I. Akinwande, V. Bulović, C.G. Sodini
Sponsorship: SRC/FCRP C2S2

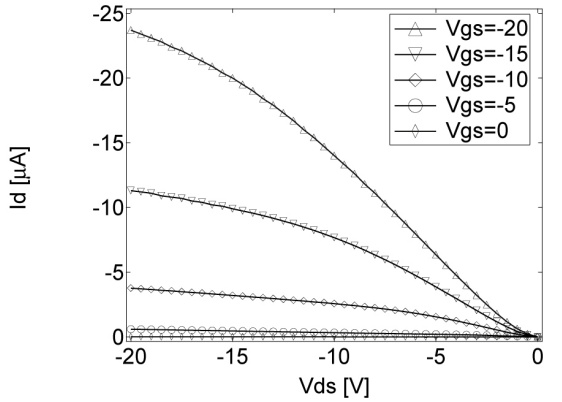
Organic semiconductors can be deposited at near-room temperatures, enabling the creation of electronic and optoelectronic devices on virtually any substrate. This unique technology makes possible the fabrication of large-area, mechanically flexible optoelectronics, such as conformable displays or image sensors. To realize these systems, an integrated approach to fabrication of organic optoelectronics is necessary.

A near-room temperature (<95°C), scalable process has been developed, using conventional photolithography and inkjet printing [1]. This process produces integrated organic field effect transistors (OFETs) and organic photoconductors (OPDs) on a single substrate. A cross section of the finished substrate is shown in Figure 1.

Typical device characteristics for an integrated OFET are shown in Figure 2. As a proof of concept, a 4x4 active-matrix imager was created using the process and was demonstrated to correctly image patterns [2].



▲ Figure 1: Schematic cross section of finished substrate illustrating OFET, OPD, and two interconnect layers.



▲ Figure 2: Typical output characteristics for a 1000µm / 4µm OFET.

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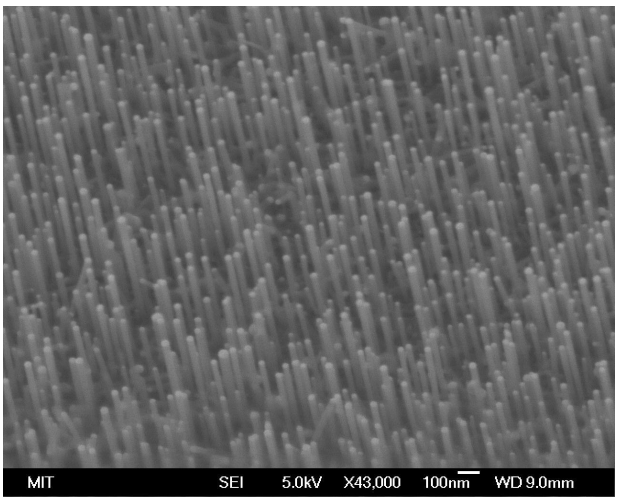
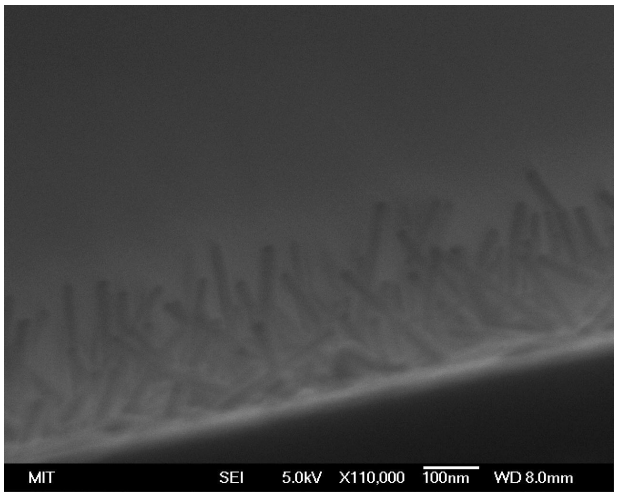
Catalyst Engineering and Growth Mechanisms of Si and III-V Nanowires

S.T. Boles, O.M. Nayfeh, D.A. Antoniadis, E.A. Fitzgerald, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

The vapor-liquid-solid mechanism for growth of single crystal whiskers and wires was originally discovered in the 1960s, but it has only recently been rediscovered as a way to fabricate high performance nanoscale electronic devices below the limits of photolithography. Although a great deal of attention has been focused on the electronic properties of Si and III-V nanowires, many of the physical mechanisms involved in growing these single crystal wires remain unclear. We have been investigating the importance of catalyst size and shape in growth morphology by using evaporated island catalysts, catalysts derived from dewetted thin films, and commercially available nanoparticles. Also in this study, the role of growth conditions has been examined by controlling temperature, partial pressures of reactants and pre-growth annealing. These parameters have been determined to be critical to stable and repeatable growth of Si and III-V nanowires.



▲ Figure 1: Si nanowires grown on Si <111> substrates.



▲ Figure 2: GaP nanowires grown on Si <111> substrates.

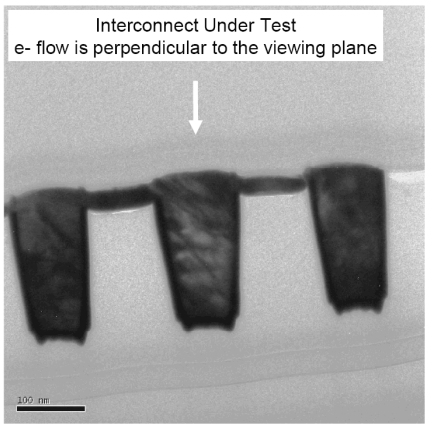
Effects of the Mechanical Properties on the Reliability of Cu/low-*k* Metallization Systems

F.L. Wei, Z.S. Choi, T. Chookajorn, C.L. Gan, C. Hau-Riege, C.V. Thompson
Sponsorship: SRC

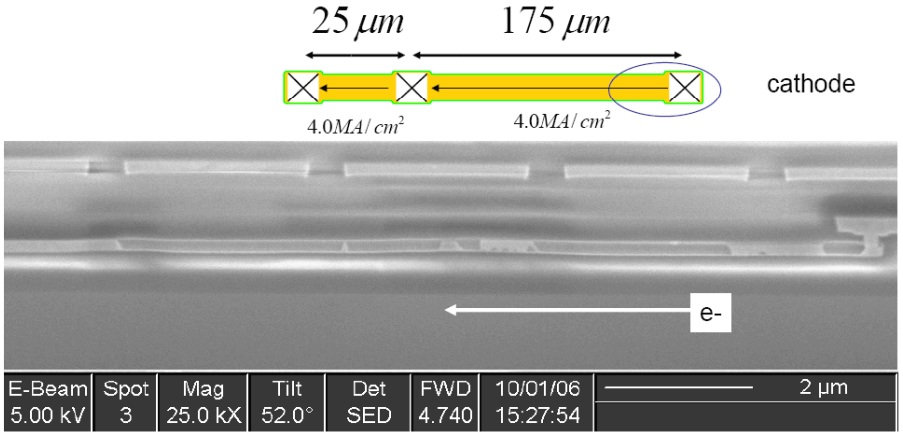
Electromigration, current-induced atomic diffusion due to momentum transfer from conducting electrons, is and will remain a major reliability concern for interconnects in integrated circuits (ICs), as future technologies demand increasing packing efficiencies and current densities. The Cu and low dielectric constant (*k*) inter-level dielectric (ILD) metallization scheme is the preferred choice for high-performance ICs. However, low elastic moduli, a characteristic of the low-*k* ILDs, and decreasing diffusion barrier thicknesses, lead to significant degradation of reliability. In order to analyze the mechanical responses and assess the failure criteria for electromigration in Cu/low-*k* interconnects, we have carried out a comprehensive investigation involving both thin-film characterizations on the constituent materials and electromigration experiments on fully processed interconnect structures manufactured by AMD Inc. and International Sematech Inc.

As Cu atoms electromigrate from the cathode to the anode inside nodes of interconnect segments, an atomic concentration change is related to a change in stress through the effective bulk modulus of the materials system, *B*. This property is central in considerations of electromigration-induced failures by void nucleation and growth, as well as Cu extrusions. The value of *B* is computed using finite element modeling (FEM) analyses using experimentally determined mechanical properties of the individual constituents. Such characterization techniques include nanoindentation, cantilever deflection, pressured membrane deflection for film elastic properties measurements, and Chevron-notched double-cantilever pull structures for adhesion measurements.

We have also carried out electromigration experiments on fully processed interconnect tree structures. We found that, under most test conditions, the conventional "10% initial resistance increase" failures are due to void growth. Such growth rates, i.e., the rate of failure for a structure, highly depend on two factors: (1) the stress conditions of neighboring interconnect segments that function as atomic sinks or reservoirs (if any is present) and (2) *B*. The higher the *B* value, the more back-stress force would be generated to counteract void growth. We also observed, over a long duration of experiments, extremely long voids and Cu extrusion formations (see Figures 1a and 1b). Studies on the threshold for Cu extrusions are being conducted.



(a)



(b)

▲ Figure 1: (a) Observation of Cu extrusions near the anode end: decohesion between the side-wall diffusion barrier and the capping layer leads to a thin layer of Cu being extruded out along the capping layer/ILD interface; (b) observation of an extremely long void near the cathode end of a Cu/low-k test segment: a void >10mm long in a 200mm-long interconnect is shown.

Bonded Copper Interconnects and Integrated Microchannels for 3D Integrated Circuits

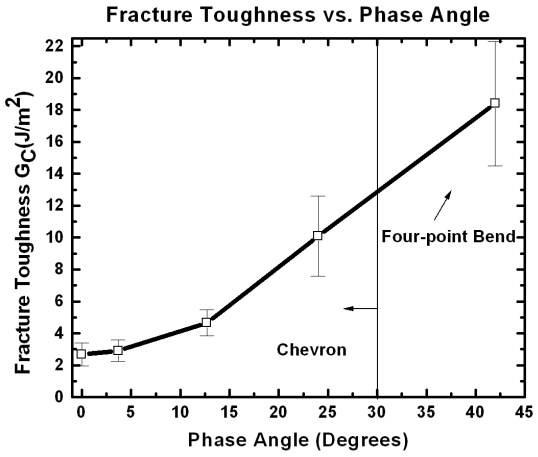
R. Tadepalli, H.L. Leong, C.L. Gan, K.L. Pey, D.E. Troxel, K. Turner, C.V. Thompson
Sponsorship: DARPA (3D Integrated Circuits), Singapore-MIT Alliance, IME

Performance of thermocompression Cu-Cu bonds is critical to reliability of devices created by stacking of individual wafers. Thermal effects in such 3D circuits are expected to be severe compared to conventional devices, owing to multiple heat-generation locations and limited heat-dissipation pathways. Bond quality and thermal performance issues in Cu wafer-bonding technology are investigated using both experiments and modeling.

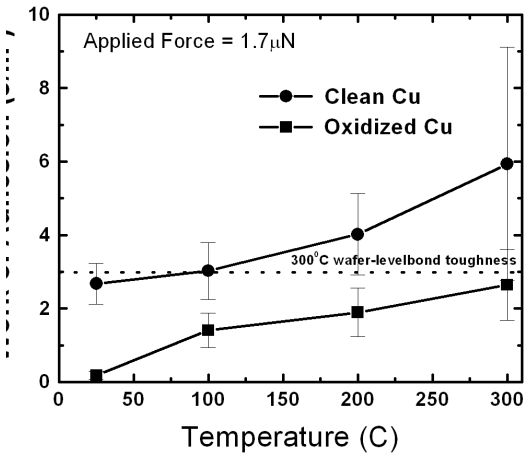
A novel test method (the Chevron test) has been developed to complement the conventional four-point bend test for bond toughness measurements. The Chevron test is used to measure Mode I (Tensile) toughness of Cu bonds (Figure 1). Nominal toughness values for Cu bonds created at 300˚C as measured by Chevron and Four-point bend tests are 2.5 J/m^2 and 17J/m^2, respectively, the difference attributed to plastic deformation of the Cu stack [1]. Therefore, the Chevron test gives a measure of the true interface strength, minus external contributions. We have also used the Chevron test technique to measure bond toughness under a variety of load conditions (mode mixities with phase angles from 0 to about 35^0), by varying the ratios of the thickness of the two substrates (Figure 1).

Effects of process and film parameters on ultimate bond quality are being analyzed using bonded ECP damascene-patterned Cu interconnects (NTU, Singapore). Results indicate a strong dependence of bonded die yield on Cu film roughness and applied bonding load. An analytical model is being developed to explain these findings.

The fundamental limit of Cu adhesion is probed using a UHV-AFM/deposition system. Force of adhesion between pristine oxide-free Cu surfaces deposited on a cantilever tip and a substrate is measured under UHV conditions. The room-temperature bond strength measured in the AFM set-up is comparable to the 300^0 C wafer-level bond strength, thereby showing a significant dependence of bond quality on Cu surface cleanliness. We find that exposure to 1 x 10^{-6} Torr oxygen is sufficient to prevent formation of strong bonds at or near room temperature.



▲ Figure 1: Use of asymmetric chevron test structures allows bond toughness measurements in a range of loading conditions



▲ Figure 2: The Cu-Cu bonds made under UHV conditions at room temperature have the same strength as bonds that require 300^{0}C in conventional bonding systems. Exposure to 1 x 10^{-6} Torr leads to behavior seen in conventional bonding.

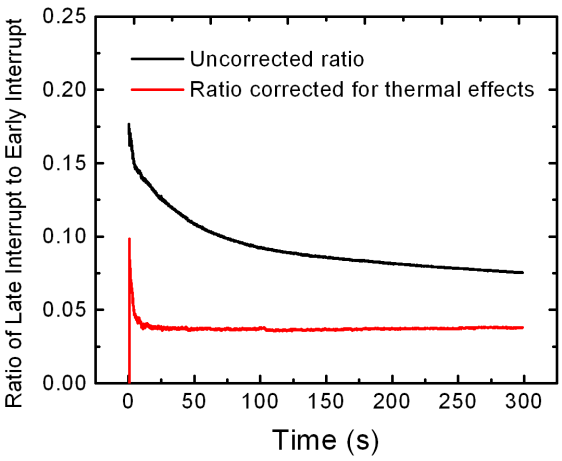
Co-evolution of Stress and Structure During Volmer-Weber Growth of Thin Films

J. Leib, A.R. Takahashi, C.V.Thompson
Sponsorship: NSF

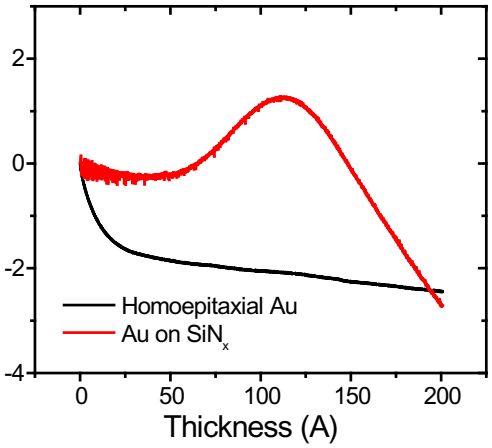
Most metallic films used in electronic and microelectromechanical devices and systems are polycrystalline and therefore form through the Volmer-Weber mechanism, in which each grain nucleates as an isolated single crystal island that coalesces with other islands to form a film. This process of film formation can lead to compressive or tensile residual stresses as well as to stress gradients that can affect both performance and reliability in microsystems.

We are using cantilever devices to measure evolution of the thin film stress-thickness product during Volmer-Weber formation and growth of polycrystalline and epitaxial films. The island coalescence process leads to tensile stresses that may or may not be retained as the coalesced film thickens. In high atomic mobility materials (such as Cu, Au, Ag, and Al) deposited at room temperature, not only does the tensile stress reduce as the film thickens, but the film can evolve into a net compressive state. During interruptions of growth, some of the compressive stress relaxes. However, this happens reversibly in that the stress returns to its previous value when deposition is resumed. This phenomenon has been particularly difficult to understand, especially given an apparent film-thickness dependence. Our recent experiments have identified two components of this reversible stress change, one of which is associated with thermal effects. These components can be separated as illustrated in Figure 1, showing that the remaining component is not dependent on the film thickness.

To further understand the origins of both the non-thermal component of the reversible compressive stress and the residual compressive stress, we are comparing evolution of polycrystalline and homoepitaxial films. Stress-thickness curves for gold grown at 1 Å/s on both silicon nitride and homoepitaxially on Au are shown in Figure 2. Both systems have strong <111> texture out of the film plane, but while the grains in the polycrystalline have random in-plane orientations, heteroepitaxial films grown on <111>Au substrates have only two in-plane variants (corresponding to fcc and hcp stacking relative to an fcc underlayer). The stress associated with coalescence is not seen in the homoepitaxial film, but a compressive stress is observed in both types of films. We are currently investigating the origins of both the similarities and differences in this compressive behavior in these two types of films.



▲ Figure 1: Ratio of the stress vs. time for a growth interruption performed at 2000 Å thickness to one performed at 400 Å thickness. When reversible thermal stresses are removed, all interrupts become similar.

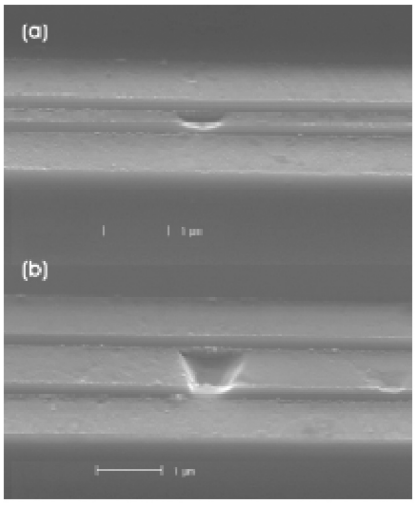


▲ Figure 2: Comparison of stress-thickness curves for gold films grown at 1 Å/s on epitaxial (111) Au layers and on silicon nitride.

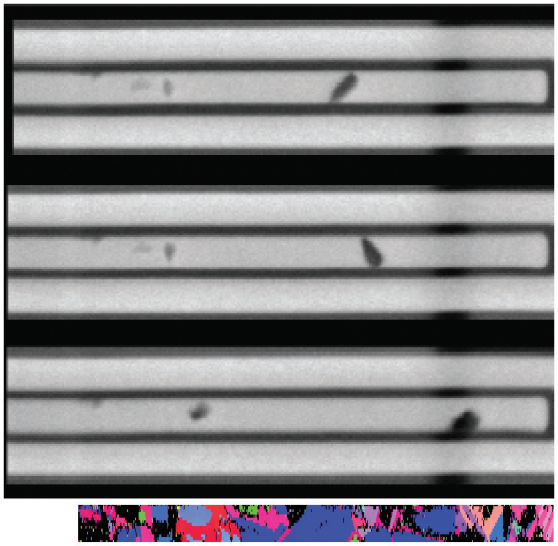
Surface Electromigration and Void Dynamics in Copper Interconnects

Z.S. Choi, T. Chookajorn, C.V. Thompson
Sponsorship: Intel Corporation, AMD, SRC

Electromigration is one of the main causes of failures in interconnects. It has been shown that the dominant diffusion path in copper interconnect technology is the interface between the dielectric passivation layer and the copper line. This interface is also the most prone to void nucleation and growth. We have carried out two types of experiments to investigate the details of void dynamics during electromigration. The first type of experiment is performed on interconnects without passivation layers to determine the dependence of copper surface diffusion and electromigration on different grain orientations. The samples are heated in reducing gas to remove copper oxide and then tested in a vacuum ($<10^{-7}$torr). The voids in these samples nucleate and grow at flux divergence sites (Figure 1). The flux divergences occur due to the differences in diffusivity for different grain orientations. After the electromigration tests, we obtain the crystallographic orientations of the grains surrounding the voids using electron backscattered diffraction (EBSD) in an SEM and correlate the results with differences in diffusivities between different grains. In a second type of experiment, we take a fully fabricated sample and thin the passivation layer using a focused ion beam microscope (FIB), in order to observe the underlying metal line in an SEM while still retaining sufficient passivation layer to constrain electromigration in the same way that it is constrained in service. We then test the samples at elevated temperatures in the SEM and observe the voids in the interconnects through the thinned passivation layer in real time, as Figure 2 shows. Voids are seen to originate at locations other than just the cathode end of the interconnect. These voids can grow in place or grow until they de-pin from their growth site and drift toward the cathode. The dependence of atomic diffusivity on crystallographic directions and textures causes changes in size, shape, and drift velocity of voids as they pass through different grains. After the test, we remove the passivation layer and use EBSD analysis to determine the effects of grain orientation on void kinetics. We are correlating these experimental observations with simulations of electromigration both to better understand this complex behavior and to better account for it in reliability assessment methods.



▲ Figure 1: Voids in interconnects with no dielectric passivation layer, interconnects with length of1000 μm, depth of 0.45 μm, widths of a) 0.3 μm and b) 1.0 μm.



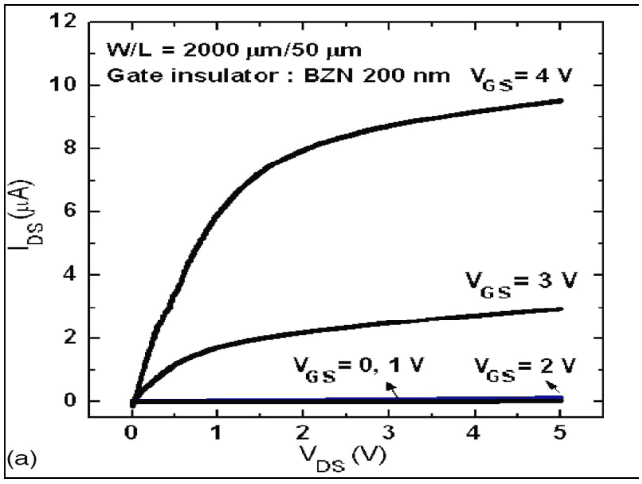
▲ Figure 2: *In situ* SEM images of the cathode of a test structure, showing void drift toward cathode end. The test line is surrounded by a Cu-extrusion monitor. Bottom image is a texture mapping by EBSD obtained after EM test. National Science Foundation.

Thin Film Transistors for Flexible Electronics and Displays

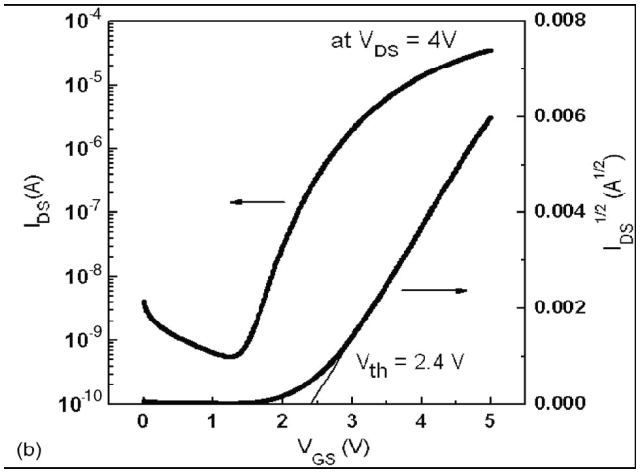
I.D. Kim, Y.S. Jin, H.L. Tuller (in coll. with Y.W. Choi, A.I. Akinwande)
Sponsorship: NSF

Organic thin film transistors (OTFT) are receiving much attention, given their potential for structural flexibility, large-area coverage, low temperature processing and low cost compared to current technology. A key limitation has been the low K of the dielectric layer and thereby high operating voltages. For example, we demonstrated the ability to RT sputter-deposit $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN) onto polymers with a K value as high as ~50, thereby enabling operation at voltages as low as 4V [1].

Transistors based on ZnO are being investigated as a possible alternative for the hydrogenated amorphous silicon or poly-silicon TFT that are employed as the backplane of liquid crystal and related displays. In addition to its transparency, ZnO has an uncommonly high mobility (up to 100 cm^2/Vs) for an oxide semiconductor. By complementing ZnO channels with high K dielectric layers, we have obtained TFTs with low operating voltage (Figure 1) and high on/off current ratios and mobilities (Figure 2) [2-3].



▲ Figure 1: Drain Current I_{DS} as a function of Drain Voltage V_{DS} depending on gate voltage V_{GS}. Note that operating voltage for the ZnO transistor is lower than 4V.



▲ Figure 2: Drain Current I_{DS} as a function of gate voltage V_{GS}. Note that threshold voltage from saturation region is 2.4 V. On/Off current ratio is ~ 10^4. Mobility of the ZnO transistor is 1.13cm^2/Vs.

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Section 3

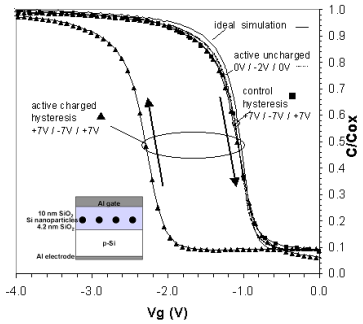
MOLECULAR & NANOTECHNOLOGY

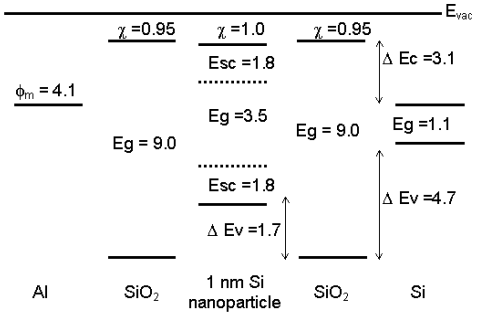
Charge-trapping in 1-nm Si Nanoparticles Embedded in a MOS Gate Stack

O.M. Nayfeh, D.A. Antoniadis, K. Mantey, M.H. Nayfeh
Sponsorship: Singapore-MIT Alliance, NSF

The MOS capacitors incorporating *ex-situ* produced, colloidal, highly mono-dispersed, spherical, 1-nm Si nanoparticles were fabricated and evaluated for potential use as charge storage elements in future non-volatile memory devices. The C-V characteristics are well behaved and agree with similarly fabricated zero-nanoparticle control samples and with an ideal simulation. Unlike larger particle systems, the demonstrated memory effect exhibits effectively pure hole storage. The nature of charging (i.e., hole-type vs. electron-type) may be understood in terms of the novel characteristics of ultra-small Si particles: large energy gap, large charging energy, and consequently a small electron affinity [1].

The left shift of the programmed C-V with respect to the uncharged curve of the active device in Figure 1 indicates charging of the particles with holes. With the application of an erase bias, the stored holes are removed. The effectively pure hole-charging characteristic may be understood in terms of properties of the 1-nm particles and their high degree of mono-dispersity. For instance, Quantum Monte Carlo (QMC) and time-dependent local density theory (TDLDT) calculations predict that the energy-gap and the charging energy for Si particles in the 1-3 nm regime rise due to the effects of quantum confinement, and consequently the electron affinity decreases, approaching that of the SiO_2 matrix [2-3]. The excitation and emission measurements of [4] for the 1-nm $Si_{29}H_{24}$ particles used in this study yielded 3.5 eV for the energy gap, the difference between the highest unoccupied molecular orbital (HOMO), and the lowest unoccupied molecular orbital (LUMO). In addition, [5] measured ~ 1.8 eV for the charging energy of individual 1-nm silicon particles by UHV-STM tunneling spectroscopy. Because of the increased band-gap and large charging energy, the electron affinity of 1-nm Si nanoparticles is greatly reduced from that of bulk Si and becomes comparable to that of SiO_2 ~ 1.0 eV. Consequently, there is no or very little conduction band-offset between the nanoparticles and SiO_2, thus inhibiting electron storage in the conduction band of the particle. However, the well-known asymmetry in the electron and hole barrier heights for the Si/SiO2 system (~ 3.1 eV for electrons, and ~ 4.7 eV for holes) maintains a valence band-offset on the order of 1.7 eV between the nanoparticles and SiO_2, suitable for hole-storage in the valence band of the particles. Figure 2 shows a proposed energy band diagram.





▲ Figure 1: The C-V hysteresis loops. Control and active devices have negligible hysteresis under uncharged conditions (sweeping forward and backward between Vg = 0 V, and Vg = -2.0 V (light-solid, and labeled). Under charging/discharging conditions (sweeping voltage between Vg=+/- 7.0 V, forward and backward), the control device (squares, labeled) has a hysteresis of only ~0.01 V; however, the active device (triangles, labeled) has a hysteresis of ~1.2 V.

▲ Figure 2: Proposed energy band diagram of an MOS system. Shown are adjustments to the band-gap of the 1-nm particles (~ 3.5 eV) and the charging energy (~1.8 eV). There still remains a valence band offset on the order of 1.7 eV for the storage of holes due to the asymmetry in barrier heights for electrons and holes in the Si/SiO2 system.

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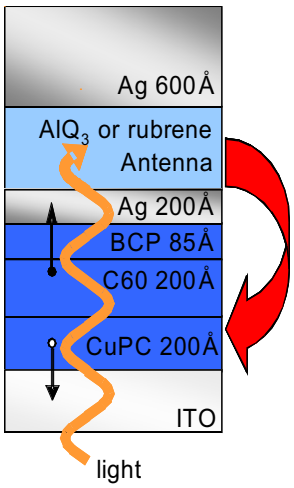
Surface Plasmon Polariton Mediated Energy Transfer in Organic Photovoltaic Devices

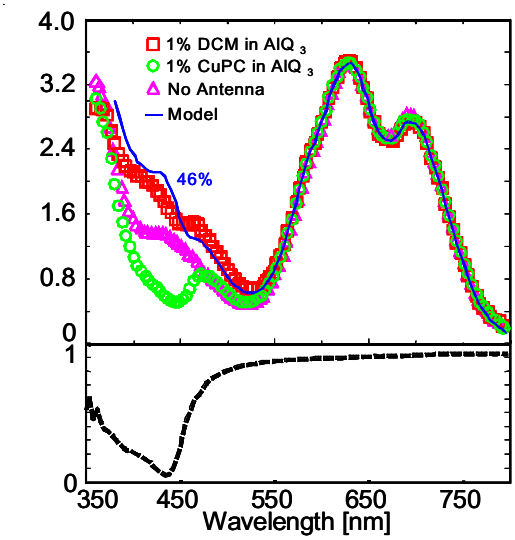
T.D. Heidel, J.K. Mapel, K. Celebi, M. Singh, M.A. Baldo
Sponsorship: DARPA/AFOSR, NSF NIRT

With a theoretical efficiency similar to conventional inorganic photovoltaics (PVs) [1] and the potential to be manufactured inexpensively, organic semiconductor technology offers a promising route to ubiquitous solar energy generation. Organic PVs, however, are constrained by a tradeoff between exciton diffusion and optical absorption. The short exciton diffusion length within organic semiconductors demands the use of extremely absorptive materials[2]. Unfortunately, the excitonic character of most organic materials yields highly structured absorption spectra, with regions of strong and weak absorption. We propose a device architecture that boosts the performance of a phthalocyanine-based PV in the absorption gap between the phthalocyanine Q and Soret bands. Light absorption is decoupled from exciton diffusion using a light-absorbing antenna layer external to the conventional charge generating layers (Figure 1). Radiation absorbed by the antenna is transferred into the charge generating layers via surface plasmon polaritons (SPP) in an interfacial thin silver contact. Off resonance, the antenna cavity operates as a reflector and all devices exhibit identical performance. However, in the region where the cavity is tuned to absorb light strongly, the devices with antennas have exhibited increased quantum efficiency of up to 200% compared to those with non-functioning antennas. Peak increases in external quantum efficiency of approximately 80% have been measured for devices with external light absorbing antennas compared to those without.

Energy coupling from external antenna layers into thin film organic PV provides a flexible route to higher efficiency devices. While the introduction of the antenna necessarily adds a step into the energy transduction process, it can be successfully employed in spectral regions where the absorption fraction of the PV cell drops below the SPP-mediated energy transfer efficiency. We measured this latter efficiency to be at least (51±10)%. It is possible to increase the quantum efficiency of an antenna to nearly 100% by optimizing the orientation and position of a luminescent dye with respect to a thin Ag film. Targeting resonant antennas to regions of poor absorption promises to solve a characteristic deficiency of organic PVs.



▲ Figure 1: Structure of organic photovoltaic devices with external resonant antenna cavities. We fabricate identical charge generation structures with antennas of varying PL efficiency consisting of isotropic mixtures of AlQ_3 and either 1% of the quenching material CuPC or 1% of the laser dye DCM. Comparing the performance of these devices allows us to isolate the photocurrent originating from light absorbed in the antenna while avoiding interference effects due to changing device structures.



▲ Figure 2: External quantum efficiency (EQE) for resonant antenna devices with functional external AlQ_3-based antenna layers exhibits an increase in EQE over the wavelength range where AlQ_3 absorption occurs and cavity reflectivity decreases. The functional antenna (□) shows a significant performance enhancement versus both the quenched antenna (□) and devices fabricated without any antenna (△). Comparison with modeling (—) indicates that the energy transfer efficiency is approximately 46%.

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Reduction of Self-absorption in Luminescent Solar Concentrators (LSC) Using Energy Transfer in Guest/Host Thin Films

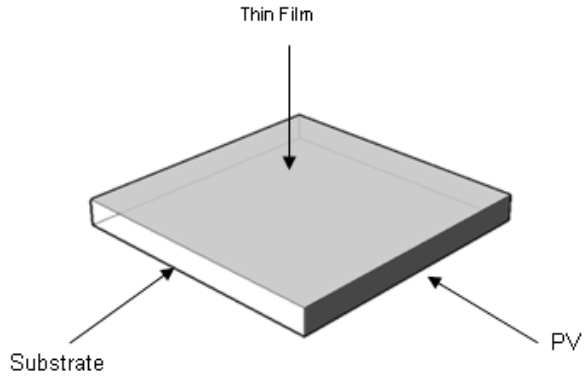
M.J. Currie, J.K. Mapel, M.A. Baldo
Sponsorship: DARPA/AFOSR, NSF NIRT

Rapidly rising global demand for silicon solar cells has exceeded the capacity of silicon suppliers, leading to escalating costs and material shortages. The development of high performance solar concentrators could dramatically reduce costs and are, we believe, the most promising solution to this problem. By concentrating the sun's light, energy conversion systems can be deployed that use just a fraction of the silicon required by typical solar cells. In particular, luminescent solar concentrators (LSCs) are an especially economical choice since they have the added benefit of having a large acceptance angle for sunlight, reducing the need for expensive tracking equipment. We show recent advances in the field of organic light emitting devices (OLEDs) can be applied to LSCs.

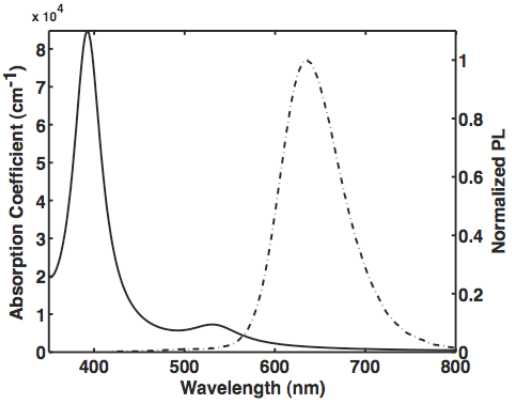
The operation of an LSC is as follows: (1) Light is absorbed by luminescent chromophores embedded within a waveguide. (2) The chromophores re-emit a photon of lower energy, and some portion of the emitted light is confined in the waveguide by total internal reflection. (3) The trapped light is guided to a photovoltaic cell.

Laser dyes are typical choices for LSC chromophores [1], and core-shell quantum dots have also been investigated [2]. Typically a combination of dyes or quantum dots is required to cover the entire solar spectrum, but both dyes and quantum dot suffer from a low quantum yield for emission in the infrared. The other significant limitation in a LSC is re-absorption of trapped light by neighboring chromophores in the waveguide.

OLED fabrication techniques allow us to precisely control the physical distance between chromophores [3], and we are able to achieve resonant energy transfer to a terminal chromophore optimized for quantum yield and self-absorption. This process is repeated with each additional chromophore with the goal of complete coverage of the solar spectrum from the visible to the near infrared.



▲ Figure 1: Schematic of a luminescent solar concentrator (LSC). Thin film absorber is applied over a transparent substrate. Photovoltaic is mounted to an edge.



▲ Figure 2: Absorption and photoluminescence spectra of a two-dye LSC.

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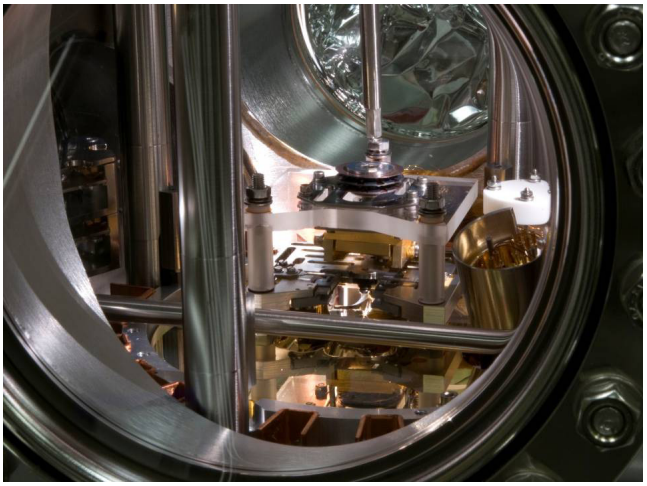
Kelvin Probe Microscopy of Organic Electronic Devices

K. Milaninia, K. Celebi, M.A. Baldo
Sponsorship: DuPont-MIT Alliance

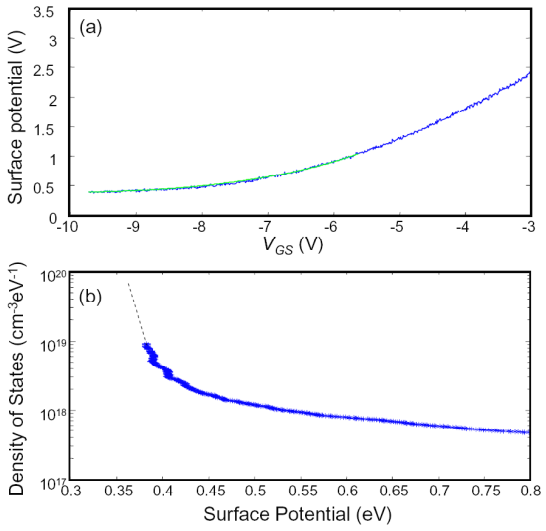
Kelvin Probe Microscopy (KPM) [1] may be used to determine the contact potential difference between different materials using scanning force microscopy. It has been employed previously in the study of organic semiconductor surfaces and interfaces [2]. We are applying KPM to the channel of an organic field effect transistor to determine the density of states [3]. The technique measures changes in the surface potential of the channel in response to changes in the gate potential relative to a grounded source and drain electrode. The measurement setup is shown in Figure 1. In an ordered semiconductor with energy bands and no states in the gap, the surface potential is expected to vary linearly with the gate before being pinned at threshold by the large density of states at the band edge. But in a disordered semiconductor with an energetic dispersion of localized states, the transition at the threshold voltage is expected to be blurred. Figure 2a shows the initial results for the hole transporting organic semiconductor copper phthalocyanine (CuPC). The CuPC is observed to have a broad density of states that stretch well into the gap between its highest occupied molecular orbital (HOMO) and its lowest unoccupied molecular orbital (LUMO). In Figure 2b we plot the density of states as calculated from the relation

$$DOS = C_G / q^2 (dV_{GS}/dU - 1)$$

where DOS is the density of states per unit energy, C_G is the gate-channel capacitance, V_{GS} is the gate-source potential, U is the surface potential and q is the electronic charge. Because the technique offers previously unattainable resolution, it promises to yield new insights into electronic transport and degradation processes in organic semiconductors.



▲ Figure 1: Image of the VT-SPM (Omicron GmbH) inside the UHV chamber (3x10^{-10} Torr). Surface potential measurements are recorded relative to a Pt-Ir coated Si tip. Measurement of the tail states requires equilibrium in the channel. However, the resistance of the channel is extremely large below the threshold. Further measurements are required to determine whether the measurement of the extreme tail states have indeed been made under equilibrium conditions.



▲ Figure 2(a): The OFET channel surface potential versus the gate bias. The blue dots represent the actual data and the green line is a cosh-fit of the data. The OFET consists of 50-nm-thick Au top-contacts with a 50-μm-wide, 20-nm-thick CuPC channel on Si-substrate with 300-nm thermal oxide. (b) The calculated density of states noting that the measured density of the extreme tail states remains subject to additional verification.

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Scanning Helium Ion Beam Lithography

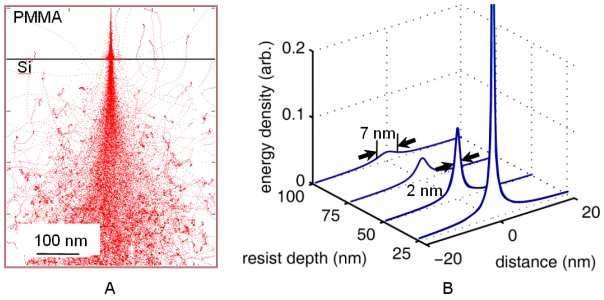
B. Cord, M.K. Mondol, K.K. Berggren, L.A. Stern (Karl Zeiss SMT, Peabody, MA)

Scanning electron beam lithography (SEBL) has been the leading technology in low-volume, high-resolution nanofabrication for over three decades. Unfortunately inherent limitations of the technology, such as electron beam scattering, have made improvement in SEBL resolution past the 10-nanometer limit problematic. Recent advances in resist contrast enhancement have mitigated this somewhat, but reliable patterning of dense, sub-10-nm features remains nontrivial on even the most high-end SEBL tools.

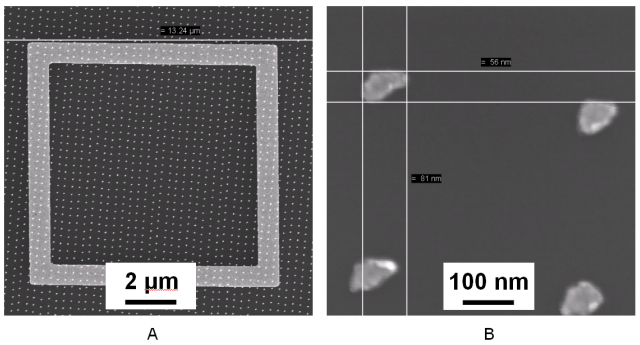
One of the key advantages of patterning using a helium ion, rather than an electron beam, is the substantial reduction in beam scattering as it travels through the resist. Helium ions, with a comparatively higher mass, are affected much less by atomic collisions when traveling through a material and exhibit only minimal scattering in normal resist materials. Figure 1 shows the results of a Monte Carlo simulation of a 50 KeV helium ion beam traveling through a PMMA layer; at a depth of 50 nm (a typical resist thickness for many applications), the point-spread function of the beam is only 2 nm wide, narrower than even 100 KeV electron beams under similar conditions. This reduction in beam scattering should help reduce the proximity effect that makes patterning dense, high-resolution features difficult with SEBL.

Experimentation with helium ion beam lithography has recently been made possible by the development of a scanning helium ion beam microscope by Alis Corporation [1]. Their commercial-grade microscope has achieved imaging resolutions on the order of 1 nm, making it a promising candidate as a lithography tool. Basic experimentation with their lower-resolution "proof-of-concept" system has demonstrated that patterning and successful transfer of features is possible using standard SEBL processes. Figure 2 shows a field of Ti-Au dots patterned with the system using a film of PMMA on silicon and standard metallization and liftoff.

While issues such as vibration, pattern generation, and process control remain to be addressed, further experimentation with helium ion beam lithography may lead to a tool that meets or exceeds the performance of modern SEBL systems.



▲ Figure 1: Simulation of He ion scattering in resist. (a) Result of SRIM-based Monte Carlo simulation of ion-scattering for 50 keV He ions traveling through 100 nm of PMMA into a Si substrate (b) Analysis of the data from (a) showing how the distribution of deposited energy widens as a function of resist depth. After 50 nm of resist (a practical thickness to work with), the beam width is only 2 nm. Note that this model does not take secondary electrons generated by the ion beam into account, as the details of the ion-secondary electron interactions are not yet fully understood.



▲ Figure 2: Scanning electron micrographs of a field of Ti-Au dots at two magnifications, fabricated by exposing 90 nm PMMA on a Si substrate to a single raster-scan of a helium ion beam and performing metal evaporation and liftoff on the resulting pattern. The consistently irregular dot shape in (b) is thought to be the result of vibrations in the system. The large square in (a) is a previously-fabricated fiducial mark.

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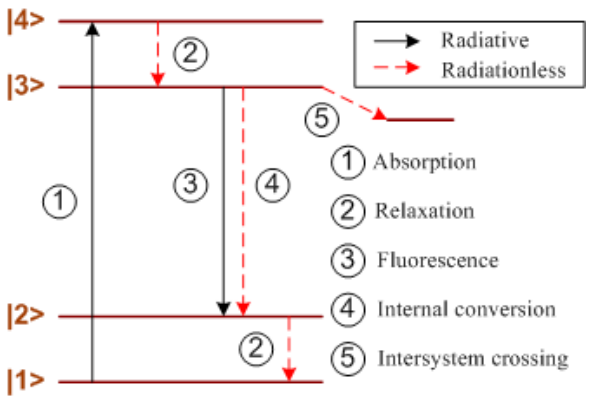
Nodal Optical Lithography: Breaking the Diffraction Limit

D. Winston, A. Chao, K. Rosfjord, S. Kooi, K. Berggren
Sponsorship: MIT, AFOSR

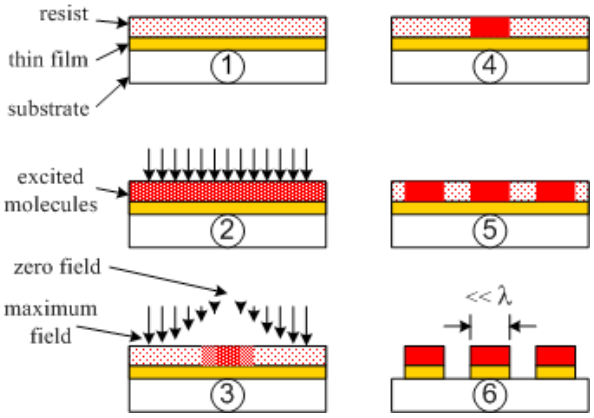
We propose to use the quantum-optical properties of materials to achieve super-resolution in optical lithography. By using beams of light instead of electrons, we can avoid substrate damage, use more intense fields that can write faster, and write with multiple beams simultaneously. By optically gating the photochemistry in the resist, we can squeeze the point-spread function of the resist exposure caused by the patterning pulse and thereby achieve sub-diffraction nanopatterning.

Resolution improvement in lithographic systems using the optical field nodes has already been demonstrated using nonlinear optical processes in neutral atoms [1]. The process used atoms in excited states and then de-excited the atoms before they were able to use their absorbed energy to stimulate a reaction. In the case of a photoresist, as was recently proposed [2], the goal is to de-excite the photo-initiating species before it can generate free radicals (Figure 1) and facilitate polymerization/crosslinking (in the case of negative-tone resist) or chain scission (in the case of positive-tone resist).

Arbitrary, dense patterning may be achieved using two synchronized laser pulses, the second of which is patterned so that it has at least one point of zero intensity, and a negative-tone resist with an appropriate photo-initiating species (Figure 2). Because the nodes – the points of zero intensity – in the second pulse determine the pattern transferred to the resist, we call this technique "nodal lithography." Increasing the intensity of the second pulse will "squeeze" the resulting pattern because even as pulse intensity rises, nodes remain nodes; herein lies the potential for diffraction-unlimited patterning.



▲ Figure 1: Energy-level diagram that models a few of the photophysical transitions, both radiative and radiationless, that a fluorescent molecule can undergo upon absorption of light. Following absorption, chemical reactions will occur after intersystem crossing. Optical de-excitation would induce fluorescence before intersystem crossing, thus deactivating the resist and enabling a tighter point spread function for higher-contrast features.



▲ Figure 2: Exposure sequence for nodal lithography with a single node: (1) a photolabile (resist) material is put on top of a film to be patterned; (2) the resist is excited uniformly, rendering it reactive; (3) the resist is selectively quenched by a patterned light; (4) the molecules near the node, which were not quenched in step (3), react; (5) the substrate is translated relative to the radiation and steps (2)-(4) are repeated to form an arbitrary pattern; (6) the resulting pattern is developed and then transferred to the underlying film using a chemical or physical etching process.

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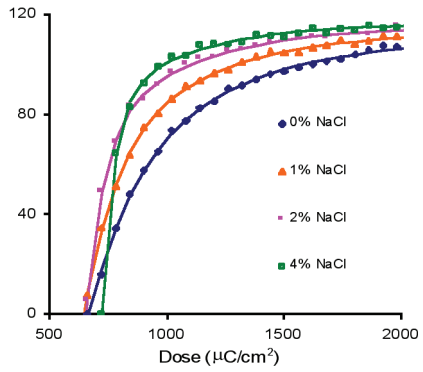
High-contrast Salty Development of Hydrogen Silsesquioxane

J.K.W. Yang, K.K. Berggren
Sponsorship: MIT

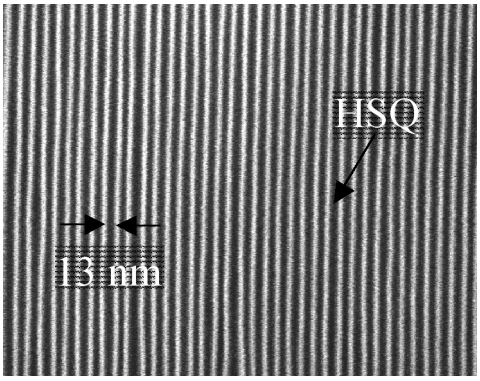
In electron-beam lithography (EBL), the highest resolution one can achieve depends primarily on the electron-beam spot size and the resist contrast. As the electron-beam spot size is constrained by the type of EBL system used, which is not easily modified, the only practical route to improved patterning resolution is to use resists with better contrast. Hydrogen silsesquioxane (HSQ) is a negative-tone electron resist that allows direct writing of etch-resistant silicon oxide nanostructures with low line-edge roughness. However, due to its low contrast, patterning high-resolution, densely packed nanostructures in HSQ has been a challenge. Recent efforts to increase the contrast of hydrogen silsesquioxane (HSQ) have focused on developing with more concentrated bases [1], and elevating development temperatures [2]. While these strong developers improve contrast, they also can cause material damage and are thus unsuitable in certain situations: for instance, hot or concentrated bases etch Si and hence are not compatible with Si processing.

In this work, we instead increased the contrast of HSQ by adding salt (NaCl) to an aqueous NaOH developer. Figure 1 shows contrast curves of HSQ using different amounts of salt in an aqueous solution of 1% wt NaOH. We noticed that the resist contrast increased with increasing amount of salt. For 4% wt NaCl in 1% wt NaOH, we demonstrated a contrast value of 10 with a 30 kV beam acceleration voltage exposure of a 120-nm-thick resist. This achieved contrast was more than triple those obtained from development in tetramethyl ammonium hydroxide (TMAH) [1,2]. We also notice that the addition of NaCl increased resist contrast without significant decrease in resist sensitivity. This effect allows one to achieve higher resolution without increasing electron-beam exposure times.

Finally, we studied the effect of development with salt on the fabrication of nanostructures. Figure 2 shows an SEM image of 13-nm-wide HSQ lines in a 30-nm-pitch grating. These gratings were formed by single-pass electron exposure of 50-nm-thick HSQ on Si at 30 kV acceleration voltage in a Raith 150 EBL system, followed by development in an aqueous solution of 1% wt NaOH with 4% wt NaCl for 4 mins. The addition of salt into the developer has enabled us to increase our resolution by roughly a factor of three. In addition to enhancing the contrast of HSQ, these experiments could provide an improved understanding of the developmental mechanism of HSQ.



▲ Figure 1: Plot of remaining HSQ thickness vs. area dose for varying amounts of NaCl to aqueous 1% wt NaOH developer. Filled markers are data points while solid lines are fitting curves of exponential functions.



▲ Figure 2: An SEM micrograph of 13-nm-wide HSQ lines in a 30-nm-pitch grating on Si. Lines were exposed at 30 kV acceleration voltage and developed in 4% wt NaCl in 1% wt NaOH.

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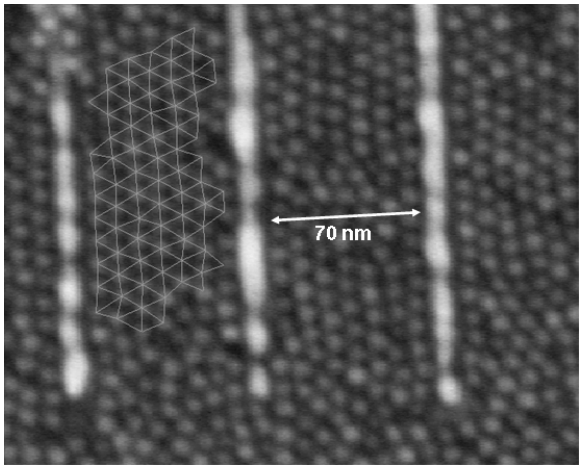
Templated Self-assembly of Sub-10-nm Quantum Dots

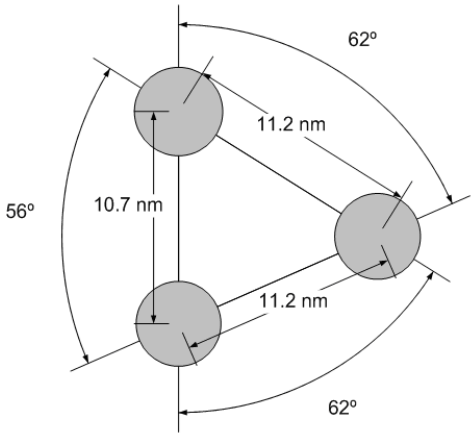
J. Leu, B. Cord, P. Anikeeva, M. Bawendi, V. Bulović, K.K. Berggren
Sponsorship: SRC/FCRP MSD

Patterned templates can guide the self-assembly of nanoparticles into ordered arrays [1]. Our motivation in pursuing templated self-assembly is to develop a robust method for the creation of ordered structures at length scales below ten nanometers. The basic process entails creating surface relief templates via electron-beam lithography and spin-coating a suspension of colloidal nanoparticles onto the template. The quantum dots self-assemble primarily through the capillary forces created by the dewetting of the template as the solvent evaporates [2].

We demonstrate this technique at sub-10-nm length scales by spin-coating a solution of organically capped semiconducting quantum dots onto nanopatterned grating structures on silicon substrates. We observe the geometric confinement of the quantum dots via physical templating and capillary forces into well-ordered monolayer aggregates with defined orientations. Additionally, we observe the presence of lattice strain in these aggregates, indicating the attractive interaction of the template with the quantum dots.



▲ Figure 1: Scanning electron micrograph of a self-assembled quantum dot monolayer on a templated silicon substrate. The vertical lines are part of a template grating, with 10-nm-wide, 80-nm-tall Au lines at a pitch of 80 nm. The spheres are organically capped 8-nm CdZnS semiconducting quantum dots. Shown superimposed on the image is a wire grid indicating the adjacency relations of a well-ordered aggregate.



▲ Figure 2: The averaged center-to-center distances and orientation of the quantum dot aggregate highlighted in Figure 1. The direction of tensile strain is perpendicular to the grating lines.

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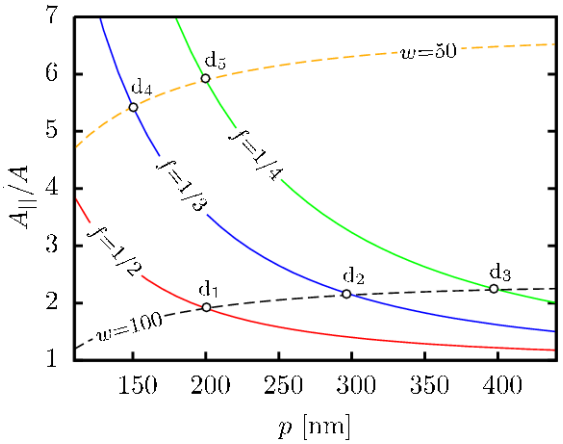
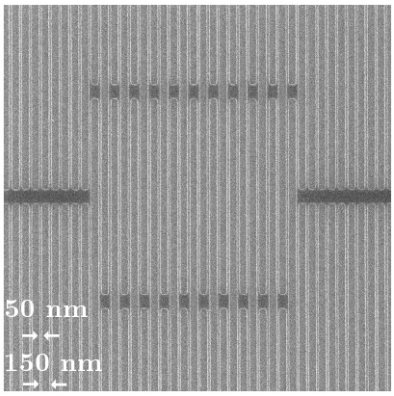
Optical Properties of Superconducting Nanowire Single-photon Detectors

V. Anant, A.J. Kerman, J.K.W. Yang, E.A. Dauler, K.M. Rosfjord, K.K. Berggren
Sponsorship: AFOSR, Lincoln Laboratory, MIT

High-efficiency single-photon detection requires careful design of the device optics. For superconducting-nanowire single-photon detectors (SNSPDs) [1-3], this challenge is amplified by the complexities of optical propagation in subwavelength structures. We have conducted an initial theoretical study of the optical design issues that must be addressed to achieve efficient absorption of infrared light by SNSPDs. We found that the absorption depends not only on geometrical parameters of the device, but also on the polarization of the incident photon. We are now testing our model by directly measuring the optical absorptance of SNSPDs fabricated at MIT. We will then feed back the testing results to the design process to realize high-efficiency SNSPDs that, by design, are either sensitive or insensitive to incident photon polarization. This work is sponsored by the United States Air Force under Air Force Contract #FA8721-05-C-0002. Opinions, interpretations, recommendations and conclusions are those of the authors and are not necessarily endorsed by the United States Government.



▲ Figure 1: Plot of the predicted ratio of parallel to perpendicular absorptance by the SNSPD as a function of pitch, *p*, wire width *w* (given in nm), and fill factor, *f=w/p*. A maximum sensitivity to polarization occurs when the fill factor and wire width are both small. We fabricated devices that correspond to points d_1-d_5 shown on this plot in order to test our model.



▲ Figure 2: Scanning electron micrograph of device d_4, where the wire width was 50 nm and pitch was 150 nm. This device was fabricated using processes described in [1] and tested using the apparatus described in [2] and [3].

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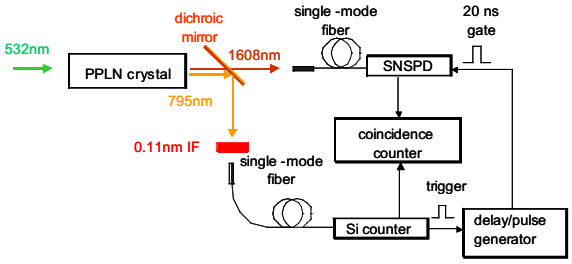
Characterization of Nondegenerate Spontaneous Parametric Downconversion Photon-pair Sources Using a Superconducting Nanowire Single-photon Detector

X. Hu, A.J. Kerman, E. Dauler, J.K.W. Yang, A. Vikas, F.N.C. Wong, K.K. Berggren
Sponsorship: DTO, DARPA, MIT, AFOSR

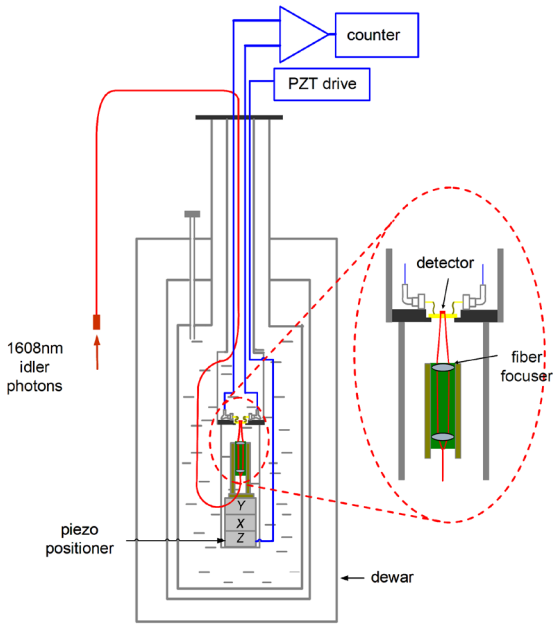
As a basis of many quantum information processing applications, photon pairs can be generated efficiently by spontaneous parametric downconversion (SPDC) in a periodically poled lithium niobate (PPLN) crystal. For instance, pumped by a 532-nm laser source, the PPLN downconverter can efficiently yield nondegenerate photon pairs, a signal photon at ~800 nm and an idler photon at ~1600 nm [1]. To measure the efficiency of this process, we perform signal-idler coincidence measurements (Figure 1), which require high-efficiency, low dark-count-rate photon counters at those two wavelengths. To detect the signal photon at ~800 nm, a Si photon counter with efficiency about 50% is commercially available; however, to detect the idler photon at ~1600 nm, a commercial InGaAs avalanche photodiode (APD) can only achieve 20% detection efficiency.

We have instead fabricated a superconducting nanowire single-photon detector (SNSPD) to count the idler photons. Compared with the InGaAs APD, we have demonstrated that our SNSPD can achieve device detection efficiency as high as over 50% at near-infrared wavelengths [2]. Furthermore, to minimize the possible optical coupling loss from fiber to the SNSPD, we have designed an experimental setup to do optical coupling and helium-immersion SNSPD testing inside a dewar (Figure 2). We use a fiber focuser to shrink the mode size of the light down to 5-6 μm and a nanopositioner to further maximize the overlap of the optical mode and the SNSPD. Our preliminary calculation shows that our SNSPD can achieve ~50% system detection efficiency.

This work is sponsored by the United States Air Force under Air Force Contract #FA8721-05-C-0002. Opinions, interpretations, recommendations and conclusions are those of the authors and are not necessarily endorsed by the United States Government.



▲ Figure 1: Schematic for photon-pair generation and the signal-idler coincidence measurements.



▲ Figure 2: Schematic for helium-immersion testing of superconducting nanowire single-photon detectors.

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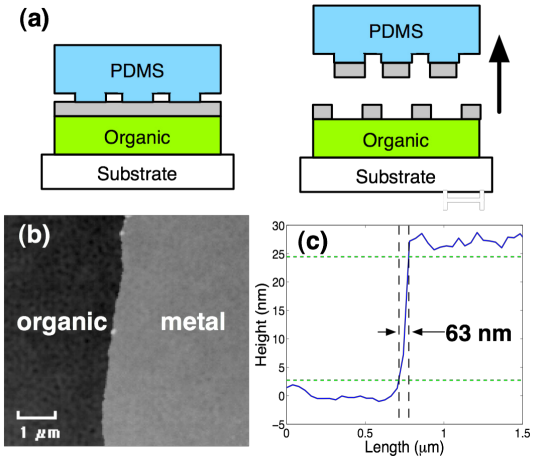
Micropatterning Organic Electronic Device Electrodes by PDMS Lift-off

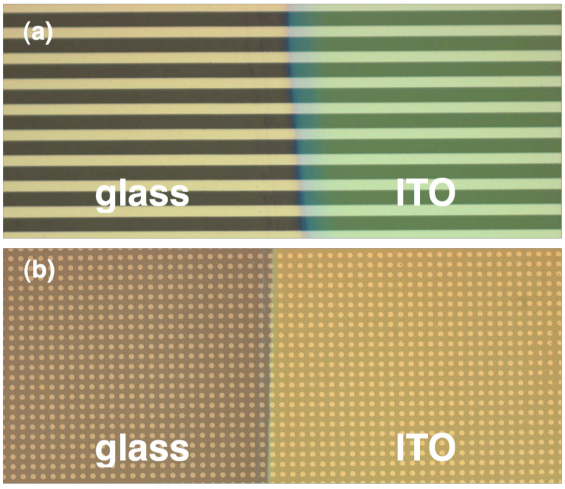
J. Yu, V. Bulović
Sponsorship: PECASE, NSF MRSEC

Patterning of electrodes in organic electronic devices is done primarily by techniques that are limited in resolution and scalability or are potentially damaging to the underlying organic material. We demonstrate a subtractive stamping technique for patterning the top metal electrode of organic electronic devices. Patterning is achieved by placing a relief-patterned polydimethylsiloxane (PDMS) stamp in contact with a metal electrode and quickly peeling off the stamp (Figure 1a). The fast peel rate increases the adhesion energy of the PDMS to the metal electrode, allowing the stamp to pick up the metal from the substrate.

The in-plane roughness of the patterned straight edge is less than 1 um (Figure 1b) while the transition region of the patterned abrupt step is less than 0.1 um in width (Figure 1c). We pattern micron-sized features on a glass substrate with an ITO step with good yield (Figure 2). We have shown that for organic light emitting devices, this technique is comparable to the traditional shadow masking technique [1]. This technique can also be applied to patterning gold electrodes for organic pentacene transistors.



▲ Figure 1: (a) Demonstration of the subtractive stamping technique. A quick release of the PDMS stamp to the substrate is required to lift off metal film from substrate surface. (b) Top view of in-plane roughness of patterned edge of organic to metal from AFM (c) AFM height data to view transition region of organic to metal edge.



▲ Figure 2: Optical microscope image of (a) 13-um-wide lines patterned from 17-nm-thick Mg:Ag film and (b) 25-um-diameter circles on 11-nm-thick Mg:Ag film on top of 50-nm Alq3, 50-nm TPD, 40-nm PEDOT, and 80-nm ITO or glass substrate. Both images show the technique can work even on a step of ITO on a glass substrate.

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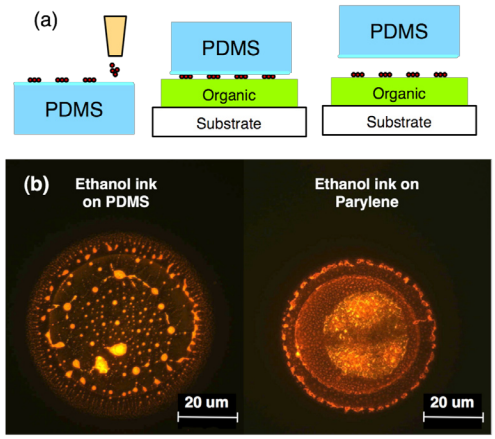
Microcontact Printing of Quantum-dot LEDs Using an Inkjet-assisted Patterning Method

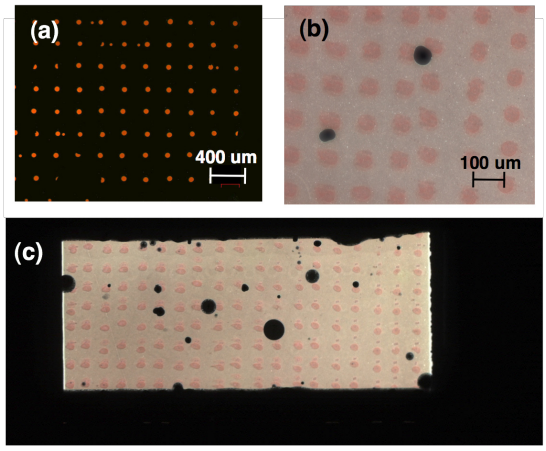
J. Yu, J. Chen, H. Huang, M. Bawendi, V. Bulović
Sponsorship: PECASE, NSF MRSEC, Hewlett-Packard

Colloidal quantum dots (QDs) with tunable emission wavelength, narrow emission band and efficient luminescence have been incorporated into OLEDs and used as lumophores in the QD-LED structure. In the past, the favored method of QD deposition has included a spin-coating step that does not utilize most of the QD material [1-2]. We propose an alternative method that directly patterns the QD layers on a stamp by inkjet printing and is subsequently transferred onto organic material via microcontact printing (Figure 1a). This technique allows patterning of the QD material and drastically improves material usage in fabrication of QD-LEDs and other optoelectronic devices that utilize QD thin films.

With a thermal inkjet printer from Hewlett Packard, we pattern QDs onto a polydimethylsiloxane (PDMS) stamp with a feature size of 50μm. Interaction between the QD solution and the stamp surface plays an important role in the formation of the inkjet printed QD patterns. Coating the stamp with a layer of parylene allows for better drying properties of the ink on the stamp (Figure 1b). The QD patterns have been transfer stamped onto organic hole transport layers (Figure 2a). The QD-LED structure is completed by subsequent deposition of a hole blocking layer, electron transport layer, and electrode, and electroluminescence images of QD-LEDs are shown in Figure 2b and c.



▲ Figure 1: (a) Inkjet printed quantum-dot technique (b) Photoluminescence of quantum-dot drop on different stamp surfaces.



▲ Figure 2: (a) Photoluminescence of inkjet printed red quantum dots transfer printed from parylene coated PDMS stamp to TPD. (b) and (c) Electroluminescence from an inkjet-assisted patterned QD-LED.

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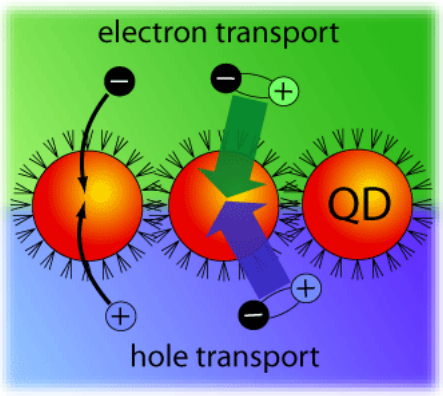
Electronic and Excitonic Processes in Quantum Dot LEDs

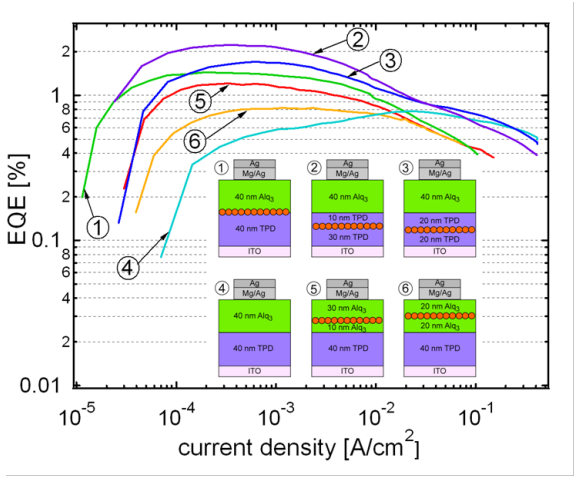
P.O. Anikeeva, C.F. Madigan, J.E. Halpert, M.G. Bawendi, V. Bulović
Sponsorship: ISN, NSF MRSEC, PECASE

Hybrid light emitting devices (LEDs) based on organic charge transporting materials and emissive colloidal quantum dot monolayers have demonstrated superior color purity and high external quantum efficiency close to that of organic LEDs (OLEDs) [1], making them a technology that can potentially replace OLEDs in flat panel displays. While fabrication methods for QD-LEDs have been extensively studied over the past several years, the mechanisms of QD-LED operation still present a significant scientific challenge. Understanding the excitonic and electronic processes in QD-LEDs is crucial to efficient device design.

We investigate the mechanism of operation of the hybrid organic/colloidal quantum dot (QD) light emitting devices (QD-LEDs). By varying the position of the emitting QD monolayer within the stacked organic structure, we find that the quantum efficiency of the device improves by >50% upon imbedding the emissive QD monolayer into the hole-transporting layer <10 nm below the interface between hole and electron transporting layers. We analyze these results in the context of two different mechanisms for QD light emission: the charge injection model and the exciton energy transfer model. We find that maximizing energy transfer contribution to QD luminescence improves QD-LED performance, primarily due to inefficiencies arising from charged QDs.



▲ Figure 1: Schematic diagram of the charge injection and energy transfer from organic charge transporting layers to a monolayer of colloidal CdSe/ZnS core-shell QDs.



▲ Figure 2: External quantum efficiency curves are shown for six devices displayed in the inset. The highest EQE of 2.3% corresponds to the device 2, in which a QD monolayer is imbedded 10 nm into TPD layer below the TPD/Alq$_3$ interface.

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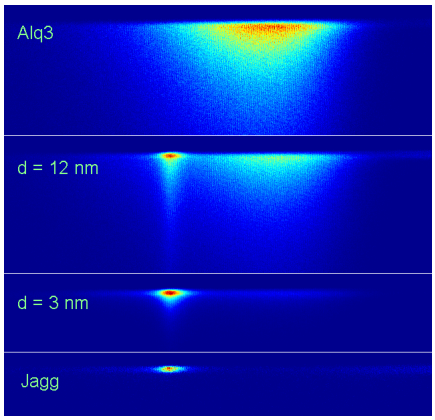
Förster Energy Transfer from Fluorescent and Phosphorescent Organic Small Molecules to J-aggregate Thin Films

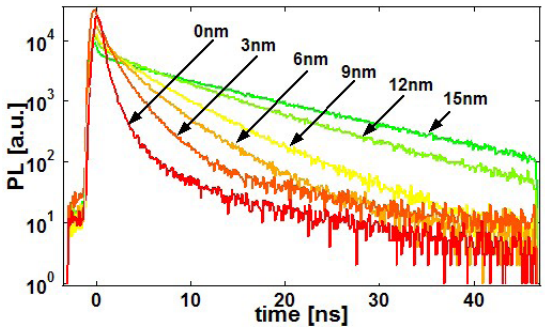
Y. Shirasaki, P.O. Anikeeva, J.R. Tischler, M.S. Bradley, V. Bulović
Sponsorship: ISN, NSF MRSEC, PECASE

Due to their extremely narrow absorption spectra and high peak absorption constant (α~1.0x10 cm), J-aggregated thin films composed of the anionic cyanine dye TDBC electrostatically adsorbed to the cationic polyelectrolyte PDAC (poly diallyldimethylammonium chloride) present an interesting material for thin film opto-electronic devices. For example, J-aggregated film was successfully incorporated into a microcavity light-emitting device (LED) to produce strongly coupled states of light and matter [1]. Its strong dipole also enables us to consider its application as an efficient light-harvesting material that can transfer energy to other materials of interest, such as quantum dots.

As an initial step in this research, we study Förster resonance energy transfer (FRET) from fluorescent (Alq_3) and phosphorescent ($Ir(ppy)_3$) donors to the J-aggregated films. The two donor materials were chosen for the large overlap between their emission spectra and J-aggregate absorption spectrum, allowing for efficient long range (~10nm) FRET. In order to find a Förster radius and potentially a magnitude of the J-aggregate transition dipole, an organic spacer layer of high bandgap material (TAZ) with varying thickness of 0-15 nm with 3 nm increments is deposited between the acceptor and donor films. The donor films are excited with a 400-nm pulsed laser and the total photon emission from the films is measured using a streak camera as shown in Figure 1. Figure 2 shows the J-aggregate photoluminescence decay times changing with respect to the distance to the donor film, indicating an efficient FRET.



▲ Figure 1: Streak camera pictures of photon emission from films with the J-aggregate (acceptor) and Alq_3 (donor) layers with varying spacer layer thickness d in between.



▲ Figure 2: Time-resolved PL measurements of J-aggregate emission from films with Alq_3 as the donor material. The spacer layer thicknesses between the donor and the acceptor layers vary from 0-15 nm with 3 nm increments.

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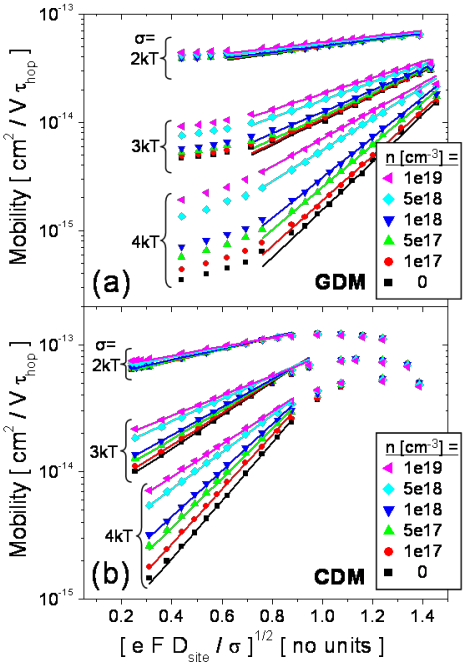
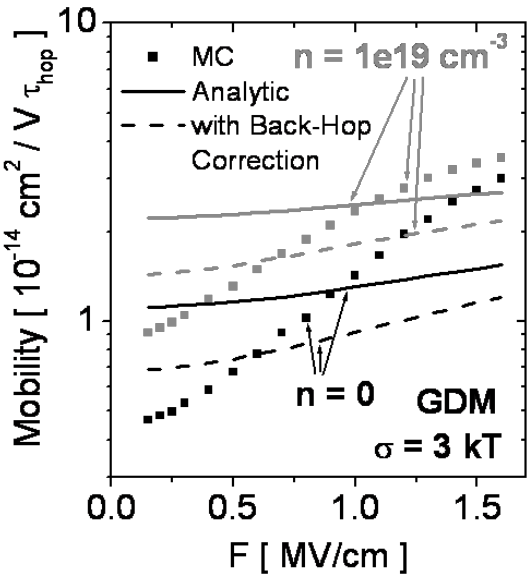
Combined Impact of Field and Carrier Concentration on Charge- carrier Mobilities in Amorphous Organic Thin Films

C. Madigan, V. Bulović

We report Monte Carlo (MC) simulations of charge-carrier transport in amorphous organic solids and provide the first calculations of the field-dependent charge-carrier mobility in the presence of elevated carrier concentrations in energetically disordered solids. We utilize the Miller-Abrahams field-assisted hopping rate [1] to perform mobility calculations over a range of carrier concentrations, electric fields and energy disorders typically encountered in organic electronic devices. We find that charge accumulation in energetically disordered solids increases the mobility, with the strongest effects at the lowest applied fields and the highest energy disorders. We show that the Poole-Frenkel regime [2-3] persists at elevated carrier concentrations. However, comparison of our MC calculations shows that existing analytic theory of charge transport in amorphous solids [4] inadequately accounts for impact of carrier concentration on charge transport as it neglects hopping cycles and improperly uses Fermi statistics under non-equilibrium conditions.



▲ Figure 1: Equilibrium mobility as a function of field and carrier concentration, n, subject to two Gaussian disorder models (GDM and CDM) for σ = [2-4] k_BT.



▲ Figure 2: Comparison of equilibrium mobility as computed by MC calculations and existing analytic theory [4] for the GDM with σ = 3 k_BT.

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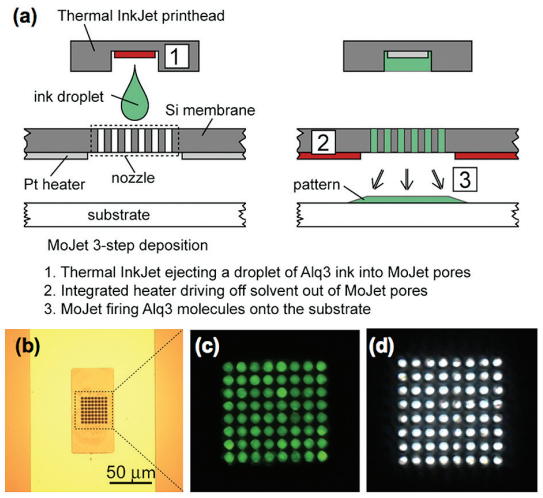
Ambient Environmental Patterning of Organic Thin Films by a Second-generation Molecular Jet (MoJet) Printer

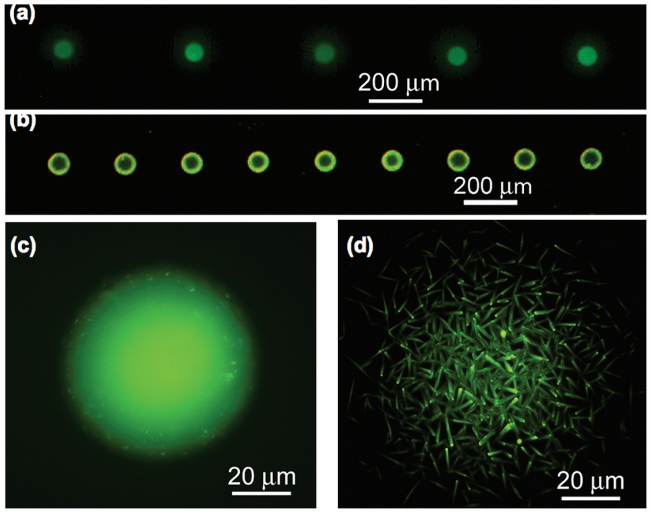
J. Chen, V. Leblanc, P. Mardilovich, M.A. Schmidt, V. Bulović
Sponsorship: Hewlett-Packard

Organic light emitting device (OLED) technology for use in flat panel display (FPD) applications would benefit greatly from the development of a reliable, repeatable, additive patterning technique of forming organic electroluminescent (EL) thin films. We previously demonstrated that the first-generation molecular jet (MoJet-I) printing technique is superior to the two industrial mainstream methods to pattern the EL layers, namely shadow-masking patterning for molecular organics and InkJet printing for polymeric materials [1-2]. We present here the concept and application of the second generation (MoJet-II) printing technique. Using an improved silicon MEMS printhead, we demonstrate the feasibility of ambient environmental patterning of molecular organic EL thin films directly by local evaporative deposition. Three stages are involved in the printing process. In the first stage, thermal InkJet printing technology is used to dispense ink drops into a micro-machined silicon membrane consisting of an array of 8 by 8 micro-pores and an integrated heater. Once the pores are filled, in the second stage, a small current is passed through the heater to completely drive off solvent from the micro-pores. In the final stage, a pulsed current of larger magnitude is applied to heat up the pores to a temperature sufficient to discharge the dry ink materials out of the pores and form molecular flux. The flux is then condensed onto a nearby substrate, forming designated thin-film EL patterns.

MoJet printing combines the advantages of the film purity of thermally evaporated films with the flexibility of direct patterning to enable "flux on demand" deposition of molecular organic thin films with scalability over arbitrary form/size substrates. Such ambient environmental patterning can enable high-quality, low-cost, on-demand digital fabrication of organic devices [3].



▲ Figure 1: (a) Schematic diagram of MoJet-II 3-step deposition; (b) MoJet-II printhead; (c) Photoluminescent (PL) image of printhead micro-pores filled with ink; (d) Empty pores after printing, ready for the next round of receiving ink.



▲ Figure 2: MoJet-II printing results (a) in comparison with the inkjet printing results (b) with identical ink composition; (c) Individual OLED pixel reveals improved thickness uniformity under PL excitation; (d) example of the final printed pattern annealed by excessive solvent.

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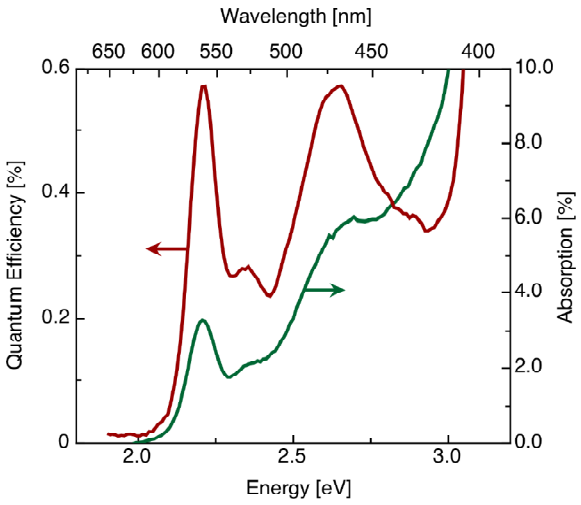
Heterojunction Photovoltaics Using Printed Colloidal Quantum Dots as a Photosensitive Layer

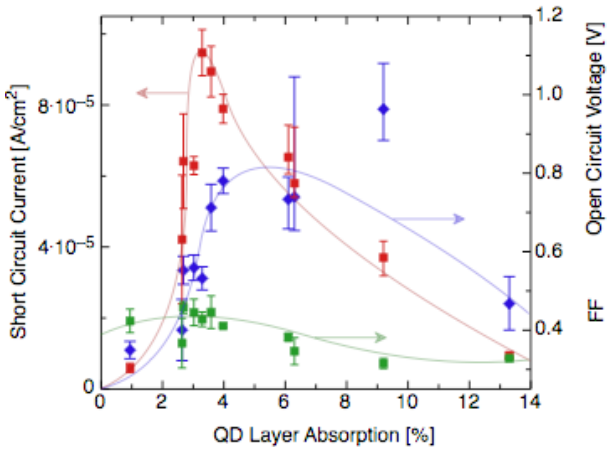
A.C. Arango, D.C. Oertel, M.G. Bawendi, V. Bulović
Sponsorship: ISN

Colloidal quantum dot (QD) systems offer distinct optical and electronic properties that are not easily attained by other nanostructured semiconductors, such as highly saturated emission in QD light-emitting-diodes, access to infrared radiation in QD photodetectors, and the prospect of optically optimized solar cell structures. The prevailing deposition method for colloidal QD systems is spin casting, which introduces limitations such as solvent incompatibility with underlying films and the inability to pattern side-by-side pixels for multispectral photodetector arrays. In the present work we employ a non-destructive microcontact printing method, which allows for deposition of a thin quantum dot films onto a wide-band-gap organic hole transport layer, N,N'-bis-(3-methylphenyl)-N,N'-bis-(phenyl)-benzidine (TPD), thus producing an inorganic/organic heterojunction that serves to enhance charge separation in the device. The top and bottom contacts are provided by ITO electrodes, allowing for near transparency.

We observe a photocurrent spectrum that follows the QD absorption profile. The magnitude of the quantum efficiency is low, due in part to minimal absorption and also to excess charge transport losses in the CdSe layer. We achieve a maximum short circuit current density at a QD film thickness corresponding to 3% absorption. By changing the size and material properties of the QDs, the response spectrum of the device can be tuned across visible and near infra-red. The present focus is on improving the device's performance and optimizing the photodetection response in the 1μm to 2μm wavelength region by utilizing different QD film chemistries.



▲ Figure 1: Plot of the quantum efficiency and absorption versus incident photon energy and wavelength. The absorption is determined by measuring the transmission and reflection of the entire device stack. The internal quantum efficiency at the first absorption peak is 16%..



▲ Figure 2: Plot of the short circuit current, open circuit voltage and fill factor (FF) for devices where the QD layer thickness is varied from greater than six monolayers (13% absorption) to less than complete surface coverage (1% absorption). Lines are guides to the eye.

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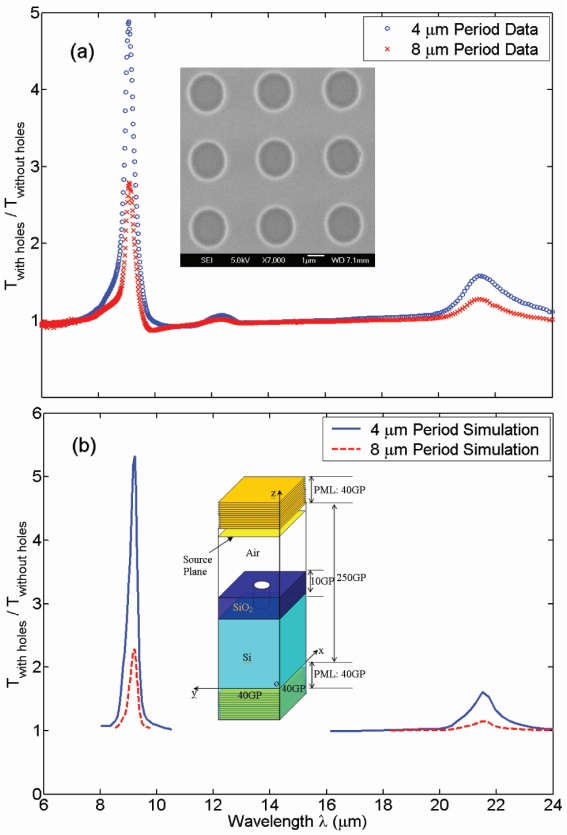
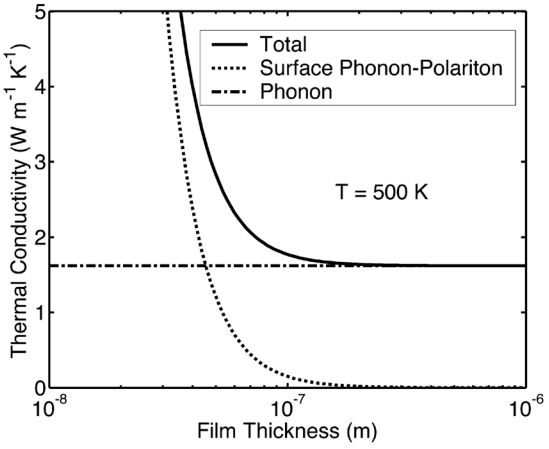
Transmission and Flux Due to Surface Phonon-Polaritons

D.-Z. A. Chen, A. Narayanaswamy, X. Chen, G. Chen (in coll. with R. Hamam, M. Soljačić, J.D. Joannopoulos)
Sponsorship: DOE, MURI (through UC Berkeley)

Surface phonon-polaritons are electromagnetic surface waves that are present in dielectrics with a negative permittivity. These near-field modes lead to interesting far-field phenomena such as extraordinary optical transmission through sub-wavelength holes. Although light propagation is classically cut-off by the holes, experimental Fourier transform infra-red measurements of the transmission through the perforated film show that significant transmission still occurs [1]. As shown in Figure 1, the enhanced transmission occurs only for certain frequency ranges. Furthermore, these frequencies correspond exactly with where surface phonon-polaritons are found and are also confirmed by finite-difference time-domain simulations.

The in-plane thermal conductivity due to surface phonon-polaritons has also been examined. The in-plane energy transfer due to these surface polaritons is modeled as a diffusive process in an absorbing medium. Due to the well-known very long propagation length of the anti-symmetric mode, it was found that the surface polaritons can make a significant contribution to the effective thermal conductivity along thin films. In particular, for a 50-nm-thick film of amorphous silicon dioxide, the total thermal conductivity was calculated to be 4 W m^{-1} K^{-1} at 500K, which is an increase of ~100% over the intrinsic phonon thermal conductivity [2], as shown in Figure 2.





▲ Figure 1: Transmission through silicon dioxide films perforated with 2-μm holes normalized to the transmission through a solid film. (a) The experimentally measured transmission spectra. The inset shows a scanning electron micrograph of the actual sample. (b) FDTD simulation results for the same structures. The inset shows a schematic of the computational cell for the structure with a 4-μm period.

▲ Figure 2: Amorphous silicon dioxide (glass) thermal conductivity due to phonons and surface phonon-polaritons as a function of film thickness at 500 K.

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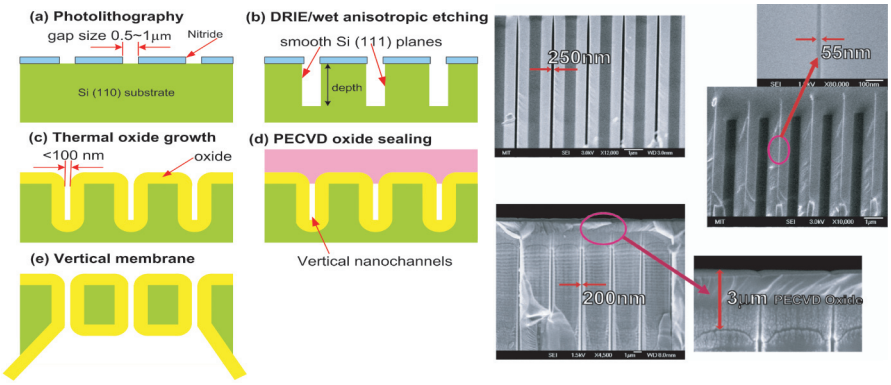
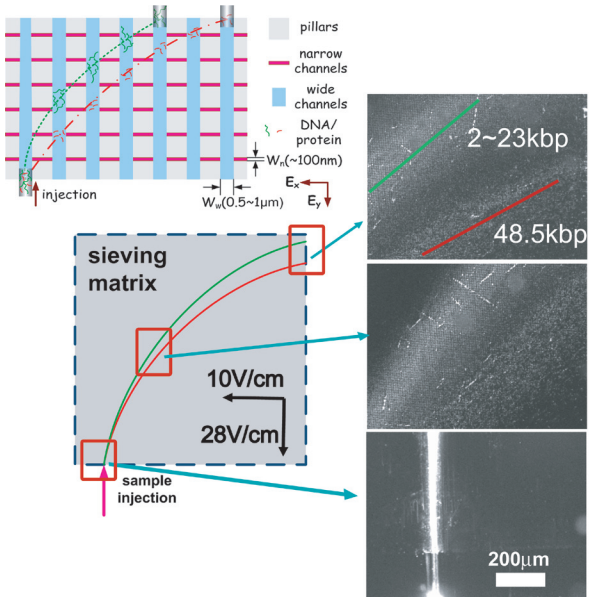
High-throughput, Continuous-flow Separation of Biomolecules in a High-aspect-ratio Nanofilter Array

P. Mao, J. Han
Sponsorship: KIST IMC, NSF

We have developed a novel fabrication approach to generate massively-parallel, high-aspect-ratio vertical nanofluidic channels with smooth, vertical sidewalls and precise control of uniform gap sizes (lateral trench width) down to 50 nm (Figure 1) [1]. The aspect ratio can be as high as 400 and the channel depths are more than 20 μm. This technique enables us to fabricate a large area of solid membrane structures with well-defined pore size and geometries, which can be very useful for membrane-based application such as filtration, separation and fuel cells. Also, using such systems as molecular sieving filters, we demonstrated efficient continuous-flow size-fractionation of large DNA molecules in a two-dimensional (2D) vertical nanofilter array device fabricated by this method (Figure 2). Our device allows much higher sample volume processing rate (1μL/hour), compared with the planar nanofilter array chip previously reported [2]. We believe that these devices could be a key to the efficient proteomic sample preparation microsystems as well as useful in purifying and separating various bioparticles and nanoparticles.



▲ Figure 1: (A) Schematic diagram of fabricating massively-parallel vertical nanofluidic membranes. (B) Cross-sectional SEM micrograph of vertical nanochannels with lateral gap sizes (widths) of 250 nm, 200 nm, and 30 nm.



▲ Figure 2: Bidirectional transport of molecules (top view) and fluorescence micrographs of continuous fractionation of the mixture of λ-DNA and λ-DNA Hind III digest in 2D vertical nanofilter array device. Electrical fields in both horizontal and longitudinal directions are applied over the sieving matrix. The gap sizes (widths) of horizontal and longitudinal channels are around 100 nm and 500 nm, respectively.

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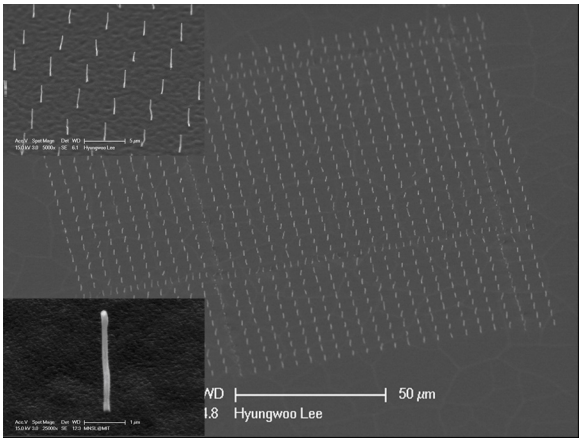
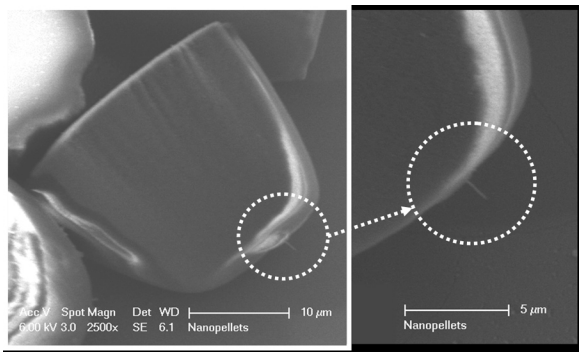
Transplanting Assembly of Single-strand Carbon Nanotubes

S. Kim, H.W. Lee, S.G. Kim
Sponsorship: Intelligent Microsystems Center

Most of the potential applications of carbon nanotubes (CNTs) such as field emitters, scanning probe microscopy (SPM) tips, and nanowire interconnection require deterministic assembly techniques with control of shape (diameter and length), orientation, location, and range. We are developing a new deterministic assembly method for single strand CNTs such that the individual CNTs can be integrated into micro-scale devices. For this purpose, we propose and demonstrate a concept of transplanting assembly of individual CNTs. An array of nickel catalytic dots is seeded at the predefined locations on a titanium deposited silicon wafer using electron beam lithography followed by a metal liftoff process. An array of vertically aligned CNTs is grown from the Ni catalysts (Figure 1) using plasma enhanced chemical vapor deposition (PECVD) machine developed by Micro & Nano Systems Laboratory of MIT [1-2]. Each single strand CNT is embedded into polymer blocks, which work as CNT carriers. A 1.5-μm-thick positive photoresist is coated on the silicon wafer before 20-μm-thick negative photoresist (SU8 of MicroChem Corp.) is coated on top of it. The SU8 layer is patterned into cylindrical blocks. Finally, each SU8 block encapsulating one single-strand CNT is released by removing the positive photoresist layer (Figure 2). Each released SU-8 block can be transplanted to the location of interest using the assembly methods readily available at the micro scales.



▲ Figure 1: An array of vertically aligned single strand CNTs. CNTs were grown straight on the seeded area, and the enlarged view shows that each CNT has a uniform diameter from the top to the bottom.



▲ Figure 2: An SU8 block with a single CNT on one side. The length of the extruded CNT is 1.5μm, and this is the same as the thickness of the positive photoresist layer.

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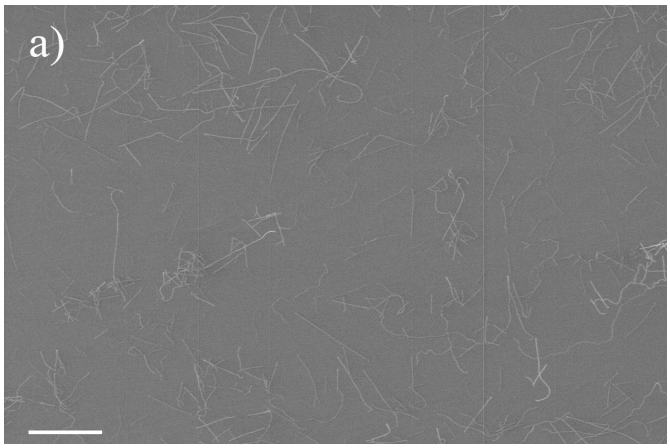
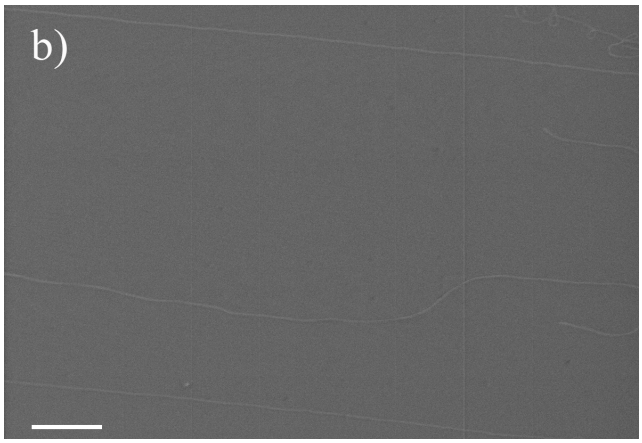
Growth Mechanisms of Horizontally Aligned Carbon Nanotubes by CVD

A. Reina, M. Hofmann, D. Zhu, J. Kong
Sponsorship: SRC/FCRP IFC, Intel Higher Education Program

The selective production of long, horizontally aligned carbon nanotubes (>1mm) or short, randomly oriented carbon nanotubes (<50μm) was achieved in a chemical vapor deposition process by influencing the catalyst pretreatment and reaction conditions. A detailed investigation was undertaken to elucidate the mechanism yielding the two different morphologies. It was found that the duration of the catalytic growth of a nanotube plays a vital role; i.e., the actual growth period of long nanotubes is significantly higher (up to 15 minutes or more) compared to short nanotubes (10 seconds or less). Alignment with the gas flow occurs only when a nanotube reaches a critical length, which suggests that short growth durations limit not only the length of CNTs but also their alignment with the gas flow. Furthermore, it is concluded that differences in the nanoparticle's catalytic lifetime is the most probable factor determining the extension of growth duration and lengths to obtain long, horizontally aligned CNTs. This work represents a step forward towards the integration of CNTs in electronic applications.



▲ Figure 1: An SEM micrograph of short, randomly aligned carbon nanotubes.



▲ Figure 2: An SEM micrograph of long, gas-flow-aligned carbon nanotubes.

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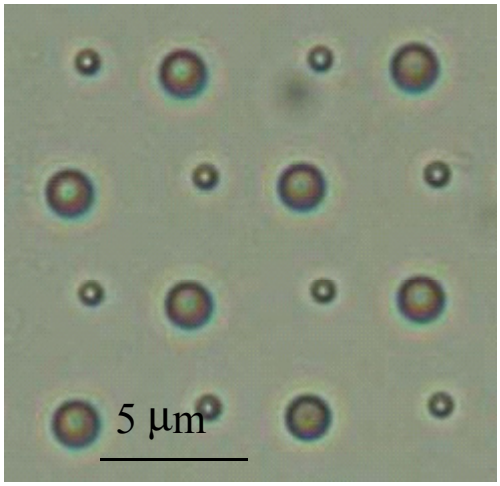
Templated Assembly by Selective Removal

M. Hyers, F. Eid, C. Livermore
Sponsorship: NSF Career Award, Pappalardo Fellowship, NSF Graduate Research Fellowship

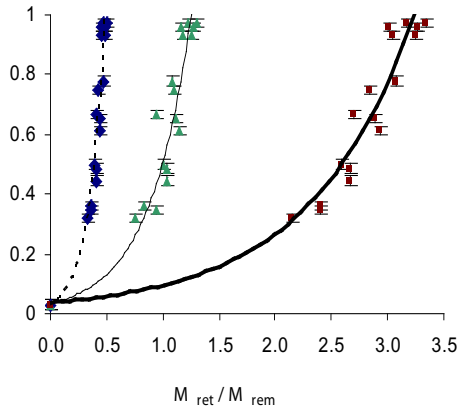
Templated assembly by selective removal (TASR) is an effective technique for site-selective multi-component assembly at the nano- and micro-scales. In this project, the TASR approach has been created and quantitatively modeled; work to expand the technology and demonstrate practical applications is now underway. The TASR approach offers great promise for assembling arbitrary (not necessarily periodic) systems of multiple different types of nanoscale components, such as electronics and biological or chemical sensing devices. It also offers a path to a new kind of shape and size selective chromatography.

The key elements of the approach follow. First, the topography of the substrate is modified to match the components' 3D shapes. Then the substrate and components are coated with an adhesion promoter, such as a hydrophobic SAM for adhesion in a water-based environment. The components and substrate are placed in a fluid environment for the assembly process, and megahertz frequency ultrasound is applied to the fluid bath. Components contact the substrate randomly and adhere wherever they land; however, components that are not in shape-matched sites are removed by fluid force, which is initiated by the high-frequency ultrasound. The fluid forces create a moment that rolls components from mismatched holes. Components in shape-matched sites are selectively retained because the adhesive forces create a stronger moment that retains components in matching holes. Figure 1 is an optical micrograph showing the successful assembly of 600-nm- and 2-mm-diameter silica microspheres into designated sites on the substrate. The TASR approach has been demonstrated for component sizes down to about 400 nm and with a variety of excitation and interaction strengths. Figure 2 shows how the assembly yield (the ratio of the number of filled sites to the total number of sites) varies with the ratio of the retention moment to the removal moment.

This approach to assembly is inherently selective; since each component will adhere only in a shape- and size-matched site, geometrically distinct components will assemble only into their designated assembly sites. The TASR method allows the organizing information to be stored in the template initially and permits components that may not be compatible with top-down manufacturing techniques to be added to the system later, with high positional precision. Present work is focused on the creation of improved models based on molecular dynamics simulations, extension of TASR to smaller size scales and a diverse set of component shapes and materials, and improved template fabrication techniques, with the goal of demonstrating practical applications enabled by the TASR approach.



▲ Figure 1: Optical micrograph of a template with assembled spheres of two different sizes.



▲ Figure 2: Plot of yield versus retention to removal moment ratio for the simultaneous assembly of 636-nm- and 2-µm-diameter spheres with various excitation and interaction strengths. The plot shows the actual data points and the fitted curves for the cases of minimum, nominal, and maximum moment ratios.

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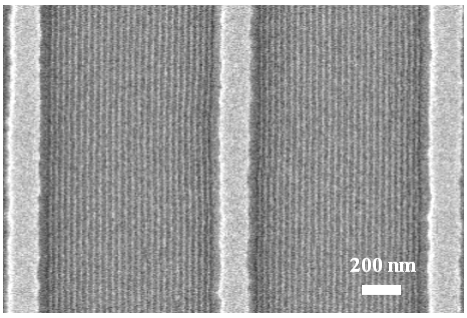
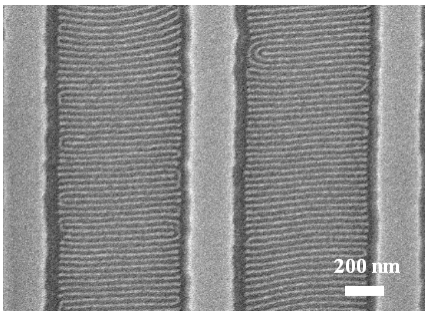
Templated Self-assembly of Block Copolymers for Nanolithography

C.A. Ross, H.I. Smith, F. Ilievski, V. Chuang, Y.S. Jung
Sponsorship: NSF, CMSE, Singapore-MIT Alliance, SRC

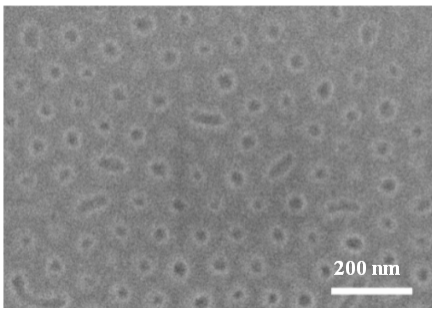
By combining "bottom-up" self-assembly with "top-down" patterned templates, templated self-assembly can provide many advantages in nanofabrication methods. Block copolymers consist of two covalently bound polymer chains of chemically distinct polymer materials. The chains can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction [1]. Previously, sphere-forming polystyrene-b-ferrocenyldimethylsilane (PS-PFS) diblock copolymers were successfully aligned in 2-D [2] or 3-D [3] templates. On the one hand, with the purpose of fabricating arrays of magnetic nanosized dots, we are working on templating the block copolymers in a removable template. These arrays are a potential candidate for magnetic hard-drive media, but the flexibility of the technique allows it to be extended to the fabrication of other devices such as plasmon waveguides or biomedical devices. On the other hand, cylindrical morphology of block copolymers can be used for defining nanoscale line patterns. Poly(styrene-b-dimethylsiloxane) (PS-PDMS) diblock copolymers have a large interaction parameter between two blocks, which is desirable for long-range ordering [4]. The high density of Si in the backbone of PDMS provides extremely high etch contrast between the two blocks when it is treated in an oxygen plasma, which is advantageous for pattern transfer into underlying materials. The cylinders can be oriented either parallel (Figure 1) or perpendicular (Figure 2) to the template by controlling mesa width and solvent vapor pressure. Beyond rather limited morphologies of diblock copolymers, an appropriate combination of block sequence, interaction parameter of the adjacent blocks, volume fraction, and molecular weights of ABC triblock polymer thin films provides a diversity of new structures. For example, a concentric cylinder forming triblock polymer thin films can be used as a lithographic mask for patterning a magnetic film into rings via an etching process. As shown in Figure 3, a concentric forming PB-PS-PMMA is vertically oriented after solvent annealing.



▲ Figure 1: Parallel cylinders from PS-PDMS diblock copolymers on trench substrates.



▲ Figure 2: Perpendicular cylinders from PS-PDMS diblock copolymers on trench substrates.



▲ Figure 3: Vertically oriented hollow cylinders of PS. The PMMA at the center of the cylinders and PB matrix are partly removed.

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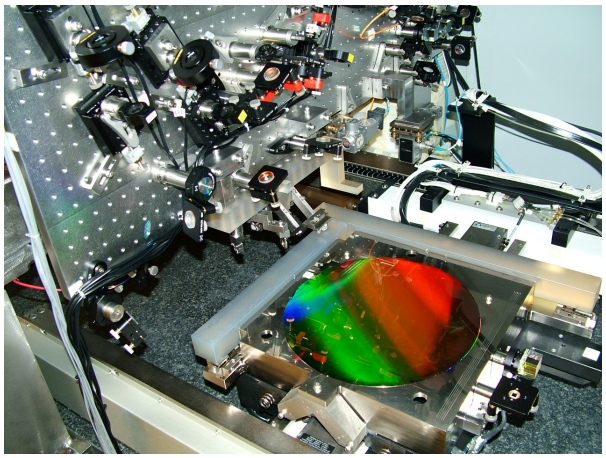
Scanning Beam Interference Lithography

M. Ahn, C.-H. Chang, R. Heilmann, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA, Plymouth Grating Laboratory

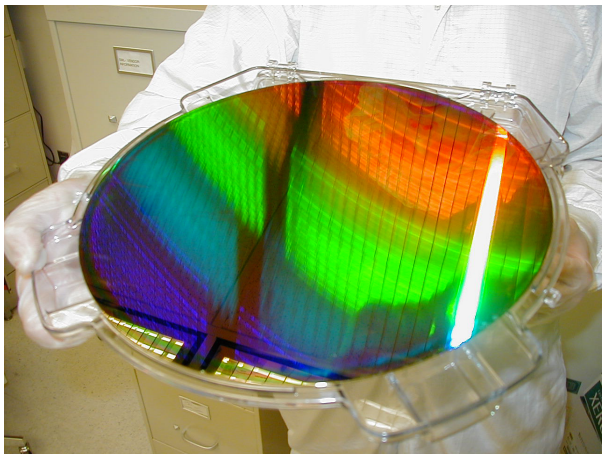
Traditional methods of fabricating gratings, such as diamond tip ruling, electron and laser beam scanning, or holography, are generally very slow and expensive and result in gratings with poor control of phase and period. More complex periodic patterns, such as gratings with chirped or curved lines or 2D and 3D photonic patterns, are even more difficult to pattern. This research program seeks to develop advanced interference lithography tools and techniques to enable the rapid patterning of general periodic patterns with much lower cost and higher fidelity than current technology.

Interference lithography (IL) is a maskless lithography technique based on the interference of coherent beams. Interfering beams from an ultra-violet laser generates interference fringes, which are captured in a photo-sensitive polymer resist. Much of the technology used in modern IL practice is borrowed from technology used to fabricate computer chips. Traditional IL methods result in gratings with large phase and period errors. We are developing new technology based on interference of phase-locked scanning beams, called scanning beam interference lithography (SBIL). The SBIL technique has been realized in a tool called the MIT Nanoruler, which recently won an R&D 100 award (Figure 1). Large gratings can be patterned in a matter of minutes with a grating phase precision of only a few nanometers and a period error in the ppb range (Figure 2).

Current research efforts seek to generalize the SBIL concept to pattern more complex periodic patterns, such as variable period (chirped) gratings, 2D metrology grids, and photonic patterns [1]. Important applications of large, high-fidelity gratings are for high-resolution x-ray spectroscopes on NASA x-ray astronomy missions, high-energy laser pulse-compression optics, and length metrology standards. We are in the process of a major upgrade of the Nanoruler optical and mechanical system that will allow rapid variation and control of grating pitch and fringe orientation, which will enable a new mode of operation of the Nanoruler that we call variable-period SBIL.



▲ Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.



▲ Figure 2: A 300-mm-diameter silicon wafer patterned with a 400-nm-period grating by the Nanoruler. The grating is diffracting light from the overhead fluorescent bulbs.

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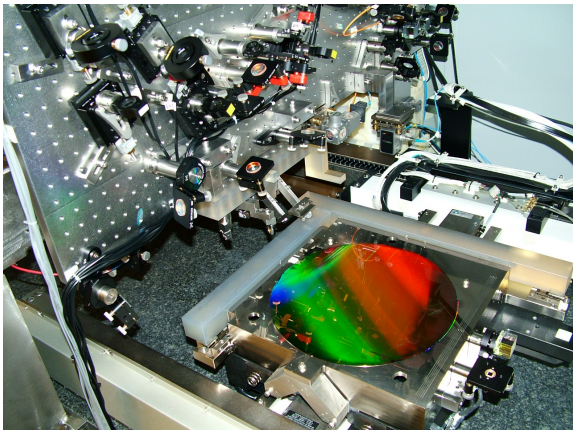
Nanometrology

R. Heilmann, Y. Zhao, D. Trumper, M.L. Schattenburg
Sponsorship: NSF

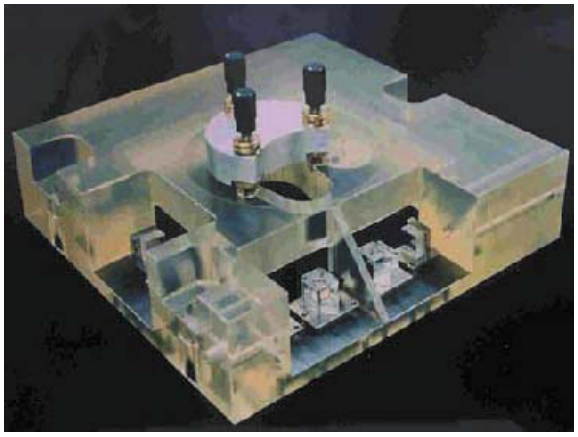
Manufacturing of future nanodevices and systems will require accurate means to pattern, assemble, image and measure nanostructures. Unfortunately, the current state-of-the-art of dimensional metrology, based on the laser interferometer, is grossly inadequate for these tasks. While interferometers can be very precise when used in carefully-controlled conditions, they typically have an accuracy measured in microns rather than nanometers. Achieving high accuracy requires extraordinarily tight control of the environment and thus high cost. Manufacturing at the nanoscale will require new technology for dimensional metrology that enables sub-1 nm precision and accuracy in realistic factory environments.

A recently formed MIT–UNC-Charlotte team is developing new metrology technology based on large-area grating patterns that have long-range spatial-phase coherence and ultra-high accuracy. Our goal is to reduce errors in gratings by 10-100 times over the best available today. These improved gratings can be used to replace interferometers with positional encoders to measure stage motion in new nanomanufacturing tools and to calibrate the dimensional scales of existing nanofabrication tools. This increased precision and accuracy will enable the manufacturing of nanodevices and systems that are impossible to produce today. Improved dimensional accuracy at the nano-to-picometer scale will have a large impact in many nanotechnology disciplines including semiconductor manufacturing, integrated optics, precision machine tools, and space research.

As part of this effort, we will utilize a unique and powerful tool recently developed at MIT called the Nanoruler that can rapidly pattern large gratings with a precision well beyond other methods. Another unique high-precision tool, the UNCC-MIT-built Sub-Atomic Measuring Machine (SAMM), is being brought to bear to research new ways to quantify and reduce errors in the gratings. Recent work at MIT is focused on improving the thermal controls in the Nanoruler lithography enclosure and developing an improved interferometer system to reduce errors in the stage metrology frame. At UNCC the SAMM is undergoing extensive refurbishment and improvements designed to boost interferometer accuracy.



▲ Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.



▲ Figure 2: Photograph of reference block/sample holder for the Sub-atomic Measuring Machine at the University of North Carolina at Charlotte.

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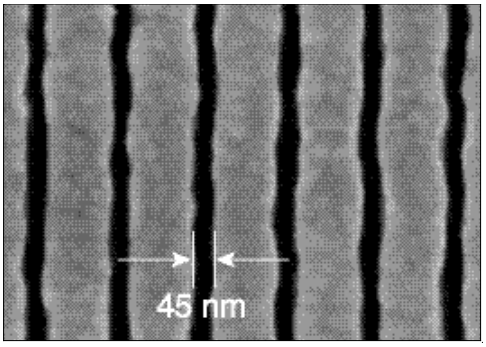
Nanofabricated Reflection and Transmission Gratings

M. Ahn, C.-H Chang, R.K. Heilmann, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA

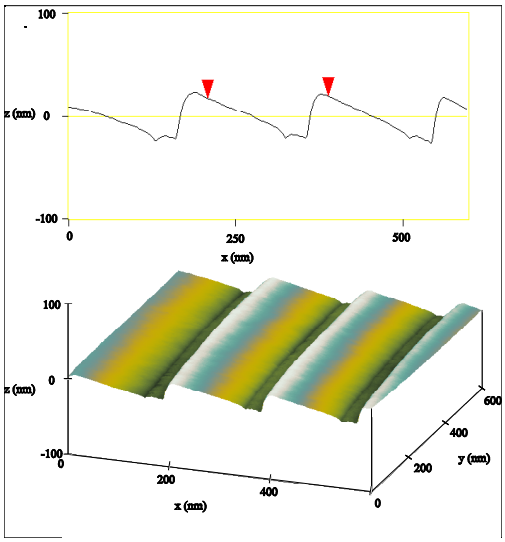
Diffraction gratings and other periodic patterns have long been important tools in research and manufacturing. Diffraction occurs due to the coherent superposition of waves—a phenomenon with many useful properties and applications. Waves of many types can be diffracted, including visible and ultraviolet light, x-rays, electrons and even atom beams. Periodic patterns have many useful applications in fields such as optics and spectroscopy, filtering of beams and media, metrology, high-power lasers, optical communications, semiconductor manufacturing, and nanotechnology research in nanophotonics, nanomagnetics and nanobiology.

The performance of a grating is critically dependant on the geometry of individual grating lines. Lines can have rectangular, triangular or other geometries, depending on the application. High efficiency requires control of the geometric parameters that define individual lines (e.g., width, height, smoothness, sidewall angle, etc.) in the nanometer or even sub-nanometer range. For some applications, control of grating period in the picometer to femtometer range is critical. Traditional methods of fabricating gratings, such as diamond tip ruling, electron and laser beam scanning, or holography, generally result in gratings that fall far below theoretical performance limits due to imperfections in the grating line geometry. The main goal of our research is to develop new technology for the rapid generation of general periodic patterns with control of geometry measured in the nanometer to sub-nanometer range in order to achieve near-theoretical performance and high yields.

Fabrication of gratings is generally accomplished in two main steps, (1) lithographic patterning into a photosensitive polymer resist, followed by (2) pattern transfer. A companion research program in this report entitled *Scanning Beam Interference Lithography* describes progress in advanced grating patterning. In this abstract we report on research in pattern transfer technology. Development of a variety of grating geometries and materials is ongoing. Advanced gratings have been fabricated for 10 NASA missions, and further advances are sought for future missions [1]. Figure 1 depicts a gold wire-grid transmission grating designed for filtering deep-UV radiation for atom telescopes, while Figure 2 depicts a nano-imprinted saw-tooth reflection grating for x-ray spectroscopy.



▲ Figure 1: Scanning-electron micrograph of a deep-UV blocking grating used in atom telescopes on the NASA *IMAGE* and *TWINS* missions. The grating blocks deep-UV radiation while passing energetic neutral atoms.



▲ Figure 2: An AFM image of 200-nm-period nano-imprint grating with 7° blaze angle developed for the NASA *Constellation-X* mission. The groove surfaces are extremely smooth, with an RMS surface roughness of <0.2 nm.

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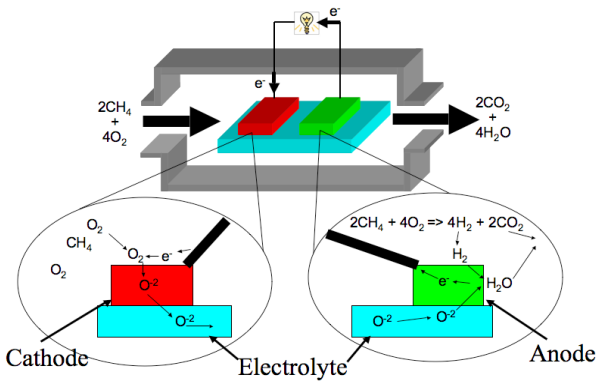
Microscale Single-Chamber Solid Oxide Fuel Cell Stacks

E.J. Crumlin, G.J. la O', Y. Shao-Horn
Sponsorship: GEM, MIT-Lemelson Fund, Ford-MIT Alliance, NSF MRSEC

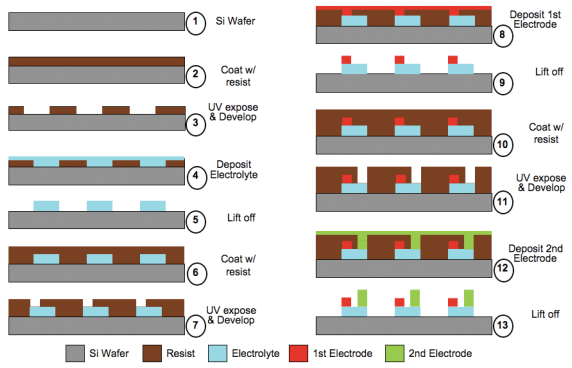
Solid oxide fuel cells (SOFCs) are electrochemical conversion devices that convert various fuel sources directly into electrical energy at temperatures ranging from 600 to 1000°C. These high temperatures could potentially allow the direct use of various hydrocarbon fuel sources and hydrogen, without the need for expensive noble metal catalyst. Conventional SOFCs are designed in a two-chamber system, separating the fuel and oxidant flow to the anode and cathode, respectively. However, fuel cell manufacturing cost and robustness has proven to be the main challenge to rapid commercialization. A promising alternate method to achieve these requirements and to open up new architecture designs for the SOFC is the single-chamber solid oxide fuel cell (SC-SOFC). The SC-SOFC avoids many of manufacturing challenges associated with conventional SOFCs and has shown optimal performance between 500 and 800°C. Figure 1 demonstrates how a SC-SOFC operates. This device reduces the need for high temperature sealing and a complicated manifold structure; however, it also reduces the partial pressure of the gases at the electrodes, which reduces the theoretical obtainable voltage.

The architecture of a SC-SOFCs allows for entire fuel cells to be manufactured with a micro-size scale. Figure 2 shows the manufacturing processes to create micro SC-SOFCs. After successfully fabricating these micro SC-SOFCs, the fuel cells are tested in a microprobe station with a custom gas chamber enclosure. Current micro SC-SOFCs using Au and Pt electrodes are among the smallest created and obtain an OCV of 0.4V and a power density of approximately 0.03mW/cm^2. The OCV is comparable to previous studies[1]; however, the power is much lower due to the non-porous electrodes and thin electrolyte layers.

Future research will involve characterizing micro SC-SOFCs to understand the fundamental reaction mechanisms, electrode materials, and architectures to obtain dense, high performing stacks of micro SC-SOFCs.



▲ Figure 1: The diagram depicts how a SC-SOFC works; the kinetic reactions are driven by the selective reactions that occur at each electrode. The cathode will selectively reduce oxygen to form an oxygen anion, which traverses the electrolyte to the anode. The anode selectively breaks down the fuel into hydrogen atoms, which lose an electron (to flow through the electrical circuit providing electrical power then to the cathode to create the oxygen anions) to form a proton that combines with the oxygen anion from the cathode, thus creating water molecules and completing the electrochemical reaction.



▲ Figure 2: This schematic depicts the fabrication steps used to produce micro-sized SC-SOFCs: (1) a silicon wafer is used as the SC-SOFC support; (2) a spin-coating of negative photoresist is applied; (3) photo-mask with electrolyte features; (4) 8YSZ is deposited by sputtering for 2 hours; (5) excess 8YSZ is lifted off by removing the resist with a photoresist stripper, leaving the desired electrolyte features; (6) photoresist is applied; (7) photo-mask with the first electrode features is exposed; (8) Au is deposited via sputtering; (9) excess Au is lifted off; (10) photoresist; is applied (11) photo-mask with the second electrode features is exposed; (12) Pt is deposited via sputtering; (13) excess Pt is lifted off, completing the micro SC-SOFC.

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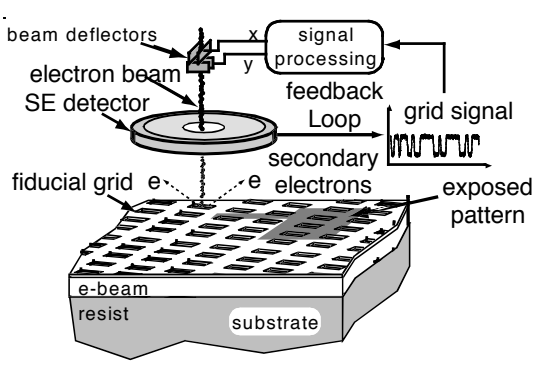
Spatial-phase-locked Electron-beam Lithography

E. Moon, H.I. Smith, J.T. Hastings (U. Kentucky)
Sponsorship: NSF

Our research in spatial-phase-locked electron-beam lithography (SPLEBL) is conducted in collaboration with the University of Kentucky. It is aimed at reducing pattern-placement errors in electron-beam-lithography systems to the sub-1 nm level. Such high precision is essential for certain applications in photonics and nanoscale science and engineering. The SPLEBL is currently the only approach capable of achieving such pattern-placement accuracy. As shown in Figure 1, SPLEBL uses a periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid placed directly on the substrate, to continuously track the position of the beam while patterns are being written. The SPLEBL senses any deviation of the beam from its intended location on the substrate and feeds corrections to the beam-control electronics to cancel beam-position errors. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate.

The research effort at MIT is now focused on developing the materials and processes for producing the fiducial grid, with the objectives of maximizing the signal-to-noise of the secondary-electron signal derived from the grid; minimizing electron scattering from the grid, which would be deleterious to precision lithography; maximizing the area and absolute accuracy of the grid; and minimizing the cost and inconvenience of producing the grid on substrates of interest. We have determined that signal levels are maximized when the grid is formed from nanoparticles. Substrates have been patterned with in-situ Faraday cups to make accurate measurements of signal to noise for a wide variety of nanoparticle types. To minimize electron scattering, the nanoparticles must be composed of low-atomic-number materials. Fullerenes may be the optimal nanoparticle, but achieving uniform thickness of layers and attaching the fullerenes along the grid lines represents a challenge of attachment chemistry. Scanning-beam interference lithography will be used to produce master grids. A special form of imprint lithography that maintains long-range spatial-phase coherence will be used to transfer attachment-chemistry grid patterns onto substrates of interest. The research effort at the University of Kentucky is focused on processing of the signal from the grid. Specifically, new approaches are being developed that enable spatial-phase locking while writing in a vector-scan mode. Previous approaches utilized only the raster-scan mode.



▲ Figure 1: Schematic of the global-fiducial-grid mode of spatial-phase-locked electron-beam lithography. The periodic signal detected from the fiducial grid, which includes both X and Y components, is used to measure placement error, and a correction signal is fed back to the beam deflection system.

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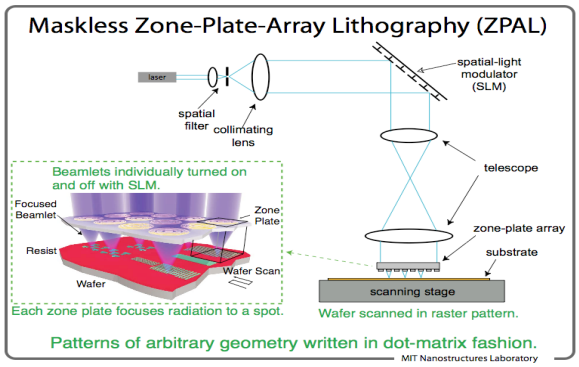
Zone-plate-array Lithography (ZPAL)

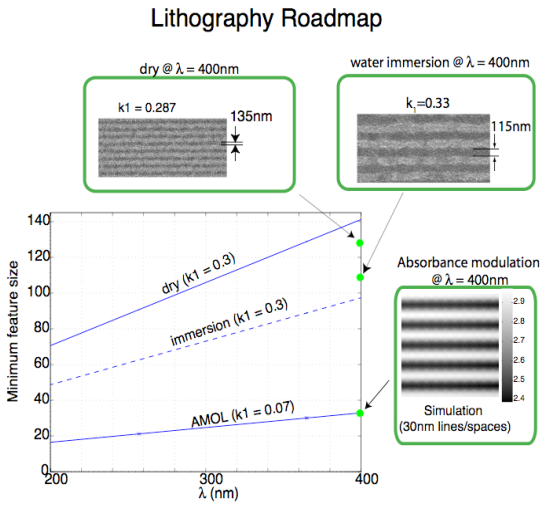
R. Menon, S.-Y. Tsai, H.I. Smith
Sponsorship: DARPA, NSF

Optical projection lithography (OPL) has been the key enabler of the continued improvements in performance of silicon integrated electronics. Modern OPL systems are designed for both high resolution and high-volume production, resulting in capital costs of tens of millions of dollars for OPL systems and putting them out of reach for applications other than high-volume production. Moreover, to achieve high resolution, various resolution-enhancement and proximity-effect-correction techniques must be employed. These, in turn, make the cost of masks prohibitive for low-volume production and for research. To address this dilemma, the NanoStructures Lab has for several years been developing an entirely new approach to OPL, depicted in Figure 1, called zone-plate-array lithography (ZPAL)[1]. No mask is required and writing is done in a dot-matrix fashion, which makes proximity-effect correction orders-of-magnitude simpler computationally.

In ZPAL the array of beamlets is created by an array of high-numerical aperture zone plates. The illumination of each zone plate is controlled by one pixel on an upstream spatial-light modulator. This technology is currently being commercialized by LumArray Inc. [2]. Figure 2 shows the roadmap for continued improvement in resolution.



▲ Figure 1: Schematic of zone-plate-array lithography (ZPAL). Light from a CW laser illuminates a spatial-light modulator (SLM), which redirects the light to an array of phase zone plates. These zone plates, in turn, focus the light to diffraction-limited spots on axis, with 40% efficiency. Each pixel of the SLM addresses one zone plate of the array and adjusts the intensity from zero to the maximum in a quasi-continuous manner. By moving the stage and adjusting the intensity of each focal spot under computer control patterns of arbitrary geometry are created in a dot-matrix fashion.



▲ Figure 2: Roadmap for extending ZPAL to the 22 nm node. The micrographs show experimental results for λ = 400 nm. The side plot is a simulation of result expected with Absorbance Modulation Optical Lithography (AMOL) using existing photochromic materials. AMOL is a recent invention at MIT[3][4].

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[1] H.I. Smith, R. Menon, A. Patel, D. Chao, M. Walsh, and G. Barbastathis, "Zone-plate-array lithography: a low-cost complement or competitor to scanning-electron-beam lithography," *Microelectronic Engineering*, vol. 83, pp. 956-961, Apr.-Sep. 2006.

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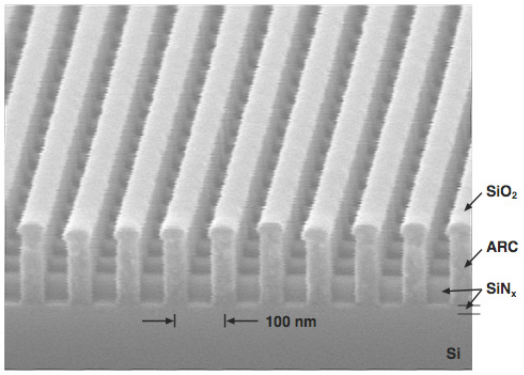
Interference Lithography

T.B. O'Reilly, H.I. Smith
Sponsorship: Internal Funds

Interference lithography (IL) uses the interference of 2 or more coherent light beams to produce periodic structures, such as gratings and grids. Typically, light from a laser is divided and recombined, forming a periodic intensity pattern that can be recorded in a photosensitive film (resist) on a substrate. The NanoStructures Lab (NSL) has been developing interference lithography systems since the mid 1970's, and it operates a range of tools for fabrication gratings, grids, and other periodic structures with periods as fine as 100 nm. These structures have a wide range of applications in nanoscale science and engineering. The most flexible and widely used of our IL systems is the Lloyd's mirror (LM). It can be easily configured to write patterns with periods from 170 nm to several microns. The LM system has recently been used to develop a simple and effective means of testing the response of photoresist to variations in image contrast and exposure dose. Other projects have used patterns from the LM to cut carbon nanotubes, guide the assembly of nanoparticles for templated self-assembly, study the behavior of strained-silicon, or fabricate templates for imprint lithography.

The NSL also operates a Mach-Zehnder interferometer. Although this system lacks the flexibility and ease of use of the Lloyd's mirror, it produces higher quality patterns. The Mach-Zehnder system has been used to study in-plane distortion of silicon nitride membranes and to create super-prisms and super-collimators based on 2D photonic crystals. The NSL also operates an achromatic interference lithography (AIL) system. The AIL uses phase gratings to split and recombine the light from a pulsed, 193-nm ArF excimer laser. It produces 100-nm-period patterns, as shown in Figure 1. This system can form high-contrast fringe patterns over a large area, despite the limited temporal coherence of the ArF laser. The AIL system has been used to create free-standing gratings used in atom-beam interference experiments and EUV spectroscopy.

In addition, the NSL collaborates with the Space Nanotechnology Laboratory, which also operates a Mach-Zehnder IL system and the Nanoruler, an IL system that can write high-quality gratings over areas larger than 300 mm in diameter.



▲ Figure 1: Scanning-electron micrograph of a stage in the fabrication of a 100-nm-period 2D grid, by means of two orthogonal exposures. Note that the underlying grating does not adversely affect the exposure control for the second, orthogonal grating on top.

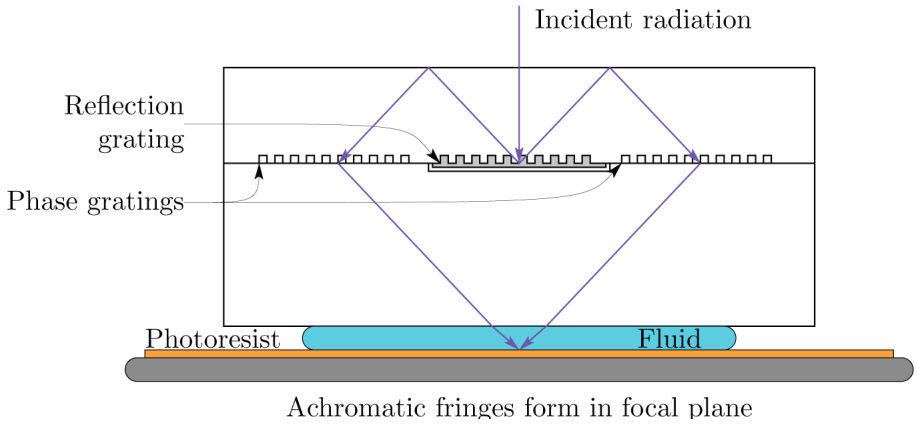
Immersion-achromatic-interference Lithography

T.B. O'Reilly, M. Walsh, T. Savas, H.I. Smith
Sponsorship: Singapore-MIT Alliance

Interference lithography is a means of using the coherent interference of light to create periodic structures such as gratings and grids. The period of the pattern written is determined by the interference angle, θ, and the wavelength, λ, according to the equation $P = \lambda/2n\sin(\theta)$. Since an upper limit exists for the interference angle (90°), to reduce the period below half the wavelength it is necessary to use an immersion fluid to reduce the effective wavelength of the light. The NanoStructures Lab is developing an immersion-interference-lithography system that will be capable of writing gratings with periods of 70 nm or even smaller.

The system under development, shown in Figure 1, is an achromatic grating interferometer similar to an existing system that is used to produce 100-nm-period gratings. Diffraction gratings are used to split and recombine light in such a way that the contrast of the fringe pattern formed is not dependent on the source's having high spatial or temporal coherence. Analysis of the proposed system has shown that it will be capable of writing gratings with periods as fine as 70 nm, over areas as large as the parent gratings, using water as the immersion fluid. Using immersion fluids of higher index, it should be possible to achieve grating periods as fine as 60 nm (i.e., lines and spaces of 30-nm width). Gratings produced by this system will find application in areas such as atom interferometry, short-wavelength spectroscopy, and templated self-assembly of macromolecules. In addition, the system will be used to study the performance of photoresists and immersion fluids at very high numerical apertures.

To produce a system with reasonable exposure times, the parent gratings must have high diffraction efficiency. Efficiency depends on the dimensions of the grooves that constitute the parent gratings. Diffraction from the gratings has been modeled using the rigorous-coupled-wave analysis method. The resulting designs present a fabrication challenge, requiring the etching of high-aspect-ratio slots in silica glass. New processing techniques have been developed to produce such parent gratings.



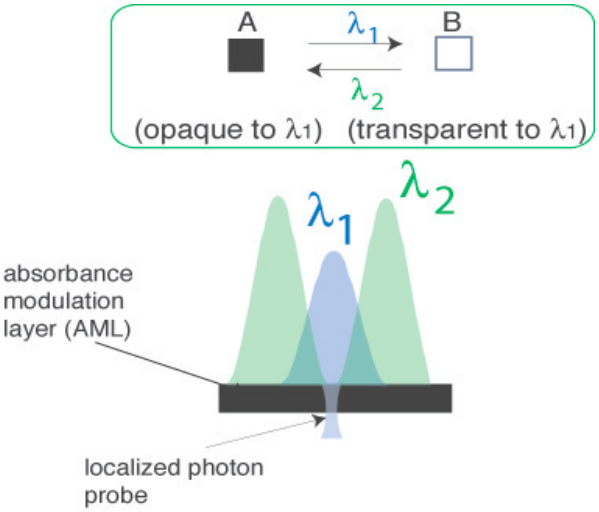
▲ Figure 1: Immersion-achromatic-interference lithography system.

Absorbance-modulation Optical Lithography (AMOL)

R. Menon, H-Y. Tsai, H.I. Smith
Sponsorship: DARPA

We are investigating absorbance modulation as a means to overcome the diffraction limit in far-field, optical-projection imaging. A substrate is coated with an absorbance-modulation layer (AML) in which illumination at one wavelength, λ_2, renders the AML opaque, while illumination at a shorter wavelength, λ_1, renders it transparent. When illuminated with a ring-shaped spot at λ_2 co-incident with a focused spot at λ_1, the dynamic competition between λ_1 and λ_2 results in a nanoscale aperture, through which λ_1 can penetrate to the substrate beneath (see Figure 1). The size of the aperture is limited only by the photokinetic parameters of the AML and the intensities of the illuminations [1].

If the AML is placed atop a photoresist that is sensitive to λ_1 but not to λ_2, patterns of arbitrary geometry can be written by scanning the substrate. The writing speed can be increased by using a large number of independently illuminated lenses operating in parallel and scanning the stage [2]. This technology, which we call Absorbance-Modulation Optical Lithography (AMOL), will be maskless, fast, nanoscale and low-cost. The resolution of AMOL is determined by the ratio of the intensities at the two wavelengths. By simply scaling this ratio, it is possible to scale the transmitted spot far beyond the diffraction limit, enabling AMOL to eventually replace scanning-electron-beam lithography.



▲ Figure 1: Absorbance modulation. The absorbance modulation layer can be made transparent or opaque, depending upon the wavelength of illumination. By illuminating with both wavelengths at appropriate intensities, a stable, transparent aperture of nanoscale dimensions can be generated as shown.

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[1] R. Menon and H. I. Smith, "Absorbance modulation optical lithography," *Journal of the Optical Society of America A*, vol. 23, p. 2290, Sep. 2006.

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[3] H. I. Smith, R. Menon, A. Patel, D. Chao, M. Walsh, and G. Barbastathis, "Zone-plate-array lithography: a low-cost complement or competitor to scanning-electron-beam lithography," *Microelectron. Eng.*, vol. 83, p. 956, Apr.-Sep. 2006.

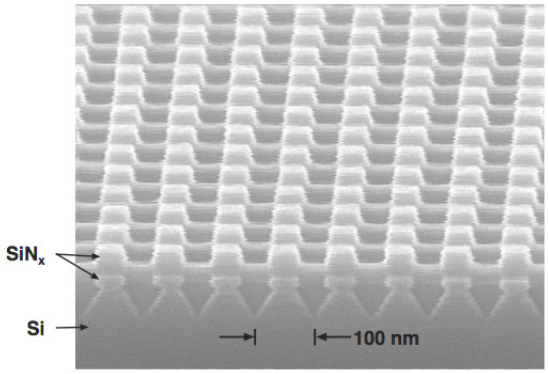
Fabrication of 100-nm Pitch Inverted Pyramid Arrays for Templated Self-assembly

T. Savas, H.I. Smith
Sponsorship: Singapore-MIT Alliance

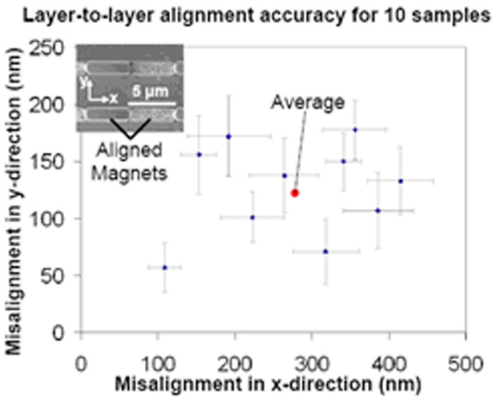
Arrays of inverted pyramids of 100-nm pitch are produced by anisotropically etching silicon through holes in a thin silicon nitride masking layer. The holes in the silicon nitride are patterned with Achromatic Interference Lithography (AIL). The AIL uses diffraction gratings to split and recombine an ArF laser beam of 193-nm wavelength [1]. The recombined beams produce a 100-nm-period grating (lines and spaces), which is recorded in PMMA resist. Grids (posts or holes) can be patterned by recording two orthogonal grating images.

It is well known that an array of holes is most easily obtained by recording the two orthogonal grating images in a negative resist. However, robust, high-resolution negative resists, for lithography at 193 nm, are not available. Therefore, we currently use a positive resist, PMMA, for AIL at 193 nm and pattern holes in the silicon nitride by etching two orthogonal gratings into the nitride.

The inverted pyramids represent artificial structures with facets that are nearly atomically smooth and apices that are close to atomically sharp. They are used in a variety of experiments on templated self-assembly and for producing arrays of crystallographically aligned metallic nanoparticles [2].



▲ Figure 1: Scanning-electron micrograph showing the pattern in SiN_x on top of (100) Si in which the inverted pyramids have been etched. The SiNx is produced by reactive ion etching following achromatic interference lithography.



▲ Figure 2: Scanning-electron micrograph of an array of inverted pyramids etched in Si. For templated self-assembly, the Si is lightly oxidized and material to be assembled is deposited on top and annealed.

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Building Three-dimensional Nanostructures via Membrane Folding

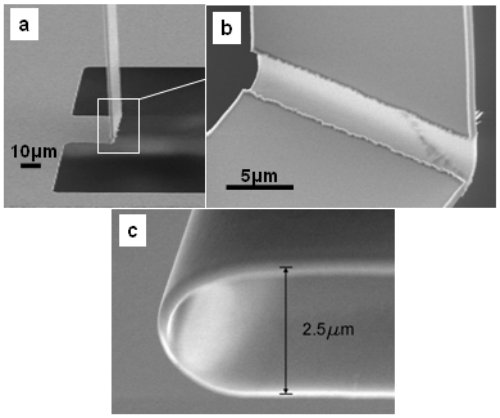
W.J. Arora, A.J. Nichol, G. Barbastathis, H.I. Smith
Sponsorship: ISN, NSF Graduate Research Fellowships

Nanostructured Origami [1] describes a method of fabricating three-dimensional (3D) nanostructures. Nanometer-scale structures are best fabricated with various two-dimensional (2D) lithography techniques. This project investigates the idea of patterning thin membranes in 2D and then folding them up into a 3D configuration. We have developed methods of both folding and aligning patterned silicon-nitride membranes.

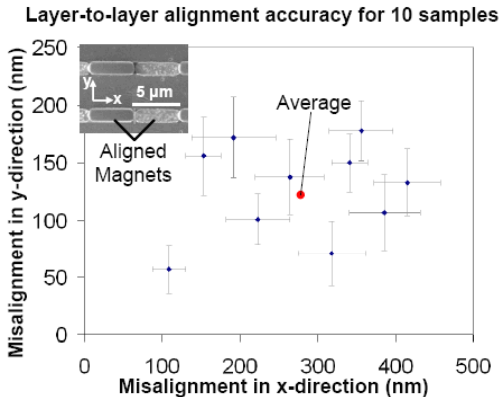
Ion implantation can be used to fold membranes. Membranes are implanted locally with a high dose to create a large stress. By varying the implanted ion energy, the implantation depth can be controlled and hence where the stress is generated. This depth control enables one to fold membranes either up or down. In our experiments, helium ions are used because they do almost no sputtering, do not damage the membrane and can be implanted to depths of 20 to 200 nm with low voltages (2-20 kV). Results are shown in Figure 1.

Magnetic forces can be used to both fold and align nanopatterned membranes [2]. Silicon nitride membranes of 1μm thickness and 100 μm×100 μm area were patterned with arrays of 75 nm thick cobalt nanomagnets. The membrane segments were then patterned and released from the substrate, making them free to rotate about compliant torsional hinges. Before folding, a 0.2 tesla external field magnetized the nanomagnets along their long axis. The field was then rotated 180° to create a magnetic torque to fold the membranes. This procedure resulted in the membranes completely folding over into a coarse layer-to-layer alignment of 2 μm.

After coarse alignment is achieved via folding, the nanomagnet arrays on the folded segments interact resulting in a very precise self-aligning force between arrays. Figure 2 shows the alignment results for folding ten samples. As shown in the plot, the magnet array interaction resulted in alignment error of roughly 200 nm. Therefore, the coarse alignment was reduced by a factor of ten. We modeled the dynamics and found that the alignment accuracy can actually be much better than the lithographic patterning accuracy. Therefore, this method may be useful for 3D nano-systems that need feature placement accuracy better than 20 nm, such as 3D nanophotonics, 3D integrated circuits, and 3D memory.



▲ Figure 1: a) A 600-nm SiN_x membrane folded to 90°. b) Magnified view of folded region, which was thinned to 150 nm by CF_4 RIE. The ion implantation was done at 16kV with a dose of 10^{18} ions/cm^2. c) View of a 180° fold illustrating typical fold radius of about 1μm.



▲ Figure 2: The layer-to-layer alignment error for 100μm ×100μm ×1 μm SiN_x membranes that were folded and aligned using arrays of nanomagnets and an external magnetic field.

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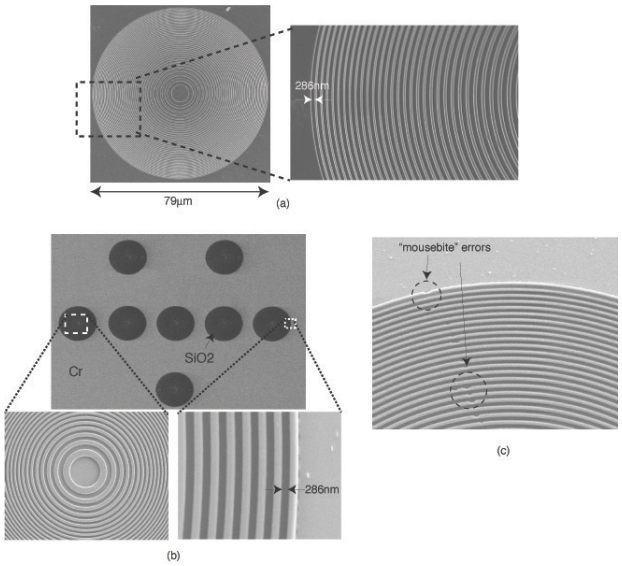
Replication of Diffractive-optical Arrays via Imprint Lithography

E.E. Moon, M.D. Galus, R. Menon, H.I. Smith
Sponsorship: Molecular Imprints, Inc.

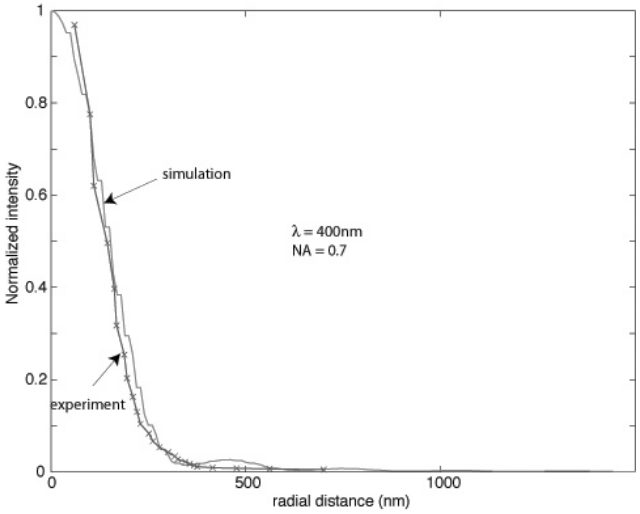
Diffractive-optical arrays serve important functions in a variety of applications, including zone-plate-array maskless lithography, in which they focus light to diffraction-limited spots and expose multiple features in parallel. Diffractive arrays are typically fabricated by e-beam lithography, but this approach is very time-consuming and prone to defects. We investigated the feasibility of replicating such arrays using a custom step-and-flash imprint lithography (S-FIL) tool [1].

Imprint template patterns were fabricated as relief structures in bulk fused silica, using nickel liftoff after e-beam exposure of PMMA. The nickel pattern was used as a hardmask to dry-etch the patterns into the underlying fused silica. After coating of the template with a release layer, droplets of a low-viscosity imprint fluid were applied to the substrate surface, and the template was leveled and brought to within ~100 nm of the substrate. At that point the imprint fluid filled the template features via capillary action. The imprint fluid was crosslinked under UV exposure, and the template removed. The imprint process was completed in under 5 min. A two-step dry etch transferred the patterns into a transparent substrate. Figure 1 shows micrographs of the resulting imprinted and etched features [2].

The focusing capability of the imprinted diffractive elements was characterized by exposing single-spot features and comparing the feature width, or the derived point-spread function, with a finite-difference time-domain (FDTD) model, as illustrated in Figure 2. We believe these experiments establish the efficacy of imprint lithography for reproduction of diffractive-optical arrays.



▲ Figure 1: Scanning-electron micrographs of a zone plate imprinted in a fused silica substrate. (a) Imprinted pattern. (b) Etched pattern in fused silica. (c) Close-up view of etched patterns, indicating few local defects ("mousebites"). Moiré artefacts in the micrographs are generated by beating between the scan period of the SEM beam and the spatial periods of the zone plate.



▲ Figure 2: Point-spread function (PSF) characterization of the etched zone plates via single-spot exposures at increasing doses. After scaling, inverse diameters were plotted as a function of the dose. The FDTD-simulated PSF is also plotted for comparison. The parameters were λ = 400 nm, NA = 0.7, f = 40 μm. The data indicate the ability to achieve sub-wavelength focusing using imprinted zone plates.

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Three-dimensional Photonic Crystals via Membrane Assembly.

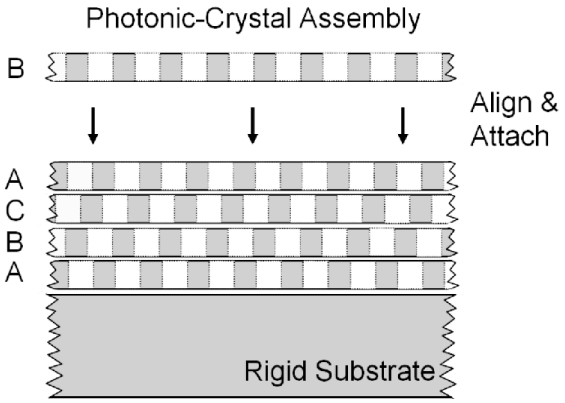
A. Patel, H.I. Smith
Sponsorship: NSF

The diffraction of light within periodic structures (so called "photonic crystals") offers a wide variety of opportunities for controlling and manipulating light. Most research to date has focused on 2-dimensional (2D) photonic crystals, because highly developed planar-fabrication techniques (i.e., lithography followed by pattern transfer) are directly applicable. However, the full potential of photonic crystals in futuristic sensing, communication and computation systems is best achieved with 3-dimensional (3D) structures. The problem is that new methods of 3D fabrication need to be developed to achieve desired complex structures over large areas with low cost and high yield.

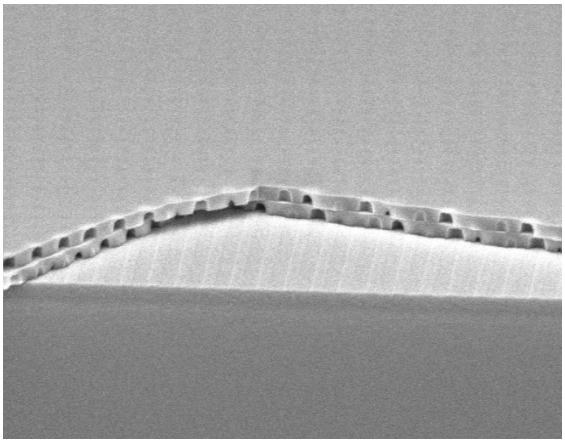
Interference lithography can produce periodic 3D structures in photosensitive polymers, but the introduction of deviations from perfect periodicity (i.e., waveguides and structures that constitute "devices" within the periodic matrix, so-called "defects") is highly problematic. Moreover, it is not clear that backfilling 3D polymeric structures is applicable to a suitable range of materials. Layer-by-layer methods enable the controlled introduction of defects, but to date fabrication is tedious, slow, low yield, and covers impractically small areas (e.g., <0.1mm on edge).

We describe a novel approach in which the 3D structure is fabricated by assembling membranes that are patterned in advance using conventional planar methods (Figure 1). This approach minimizes the yield problem because membranes can be inspected and selected before assembly, and the desired waveguides and devices can be introduced at any level. When brought into contact, membranes that are free of particulate and other contamination will bond spontaneously by Van der Waals or other mechanisms.

We report the progress to date using low-stress SiN_x membranes as the test vehicle. 2D periodic structures have been etched into-free standing membranes (Figure 2), and nonaligned stacking carried out (Figure 3). We do not consider precise alignment of layers a potential problem since light diffracted from the structures during assembly will provide a built-in, reliable alignment signal. We believe the major problem facing the membrane assembly approach will be ensuring freedom from particles and other contamination. The Si membranes, with their higher refractive index, are more desirable and will be used in the next stage of our research.



▲ Figure 1: Depiction of the layer-by-layer stacking paradigm we are developing. All the layers in the photonic crystal are fabricated in parallel reducing processing cycles, which will help improve yield and reduce lead times.



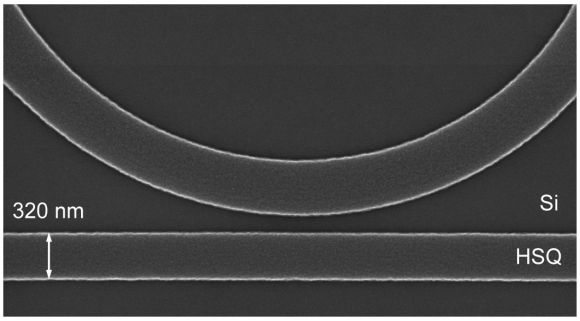
▲ Figure 2: Initial stacking experiment. A patterned SiN membrane is brought into contact with SiN substrate. The pitch of the array is 600 nm and the membrane is 350 nm thick. A second patterned membrane is brought into contact.

Nanofabrication of Hitless Reconfigurable Optical Add-drop Multiplexers in Silicon

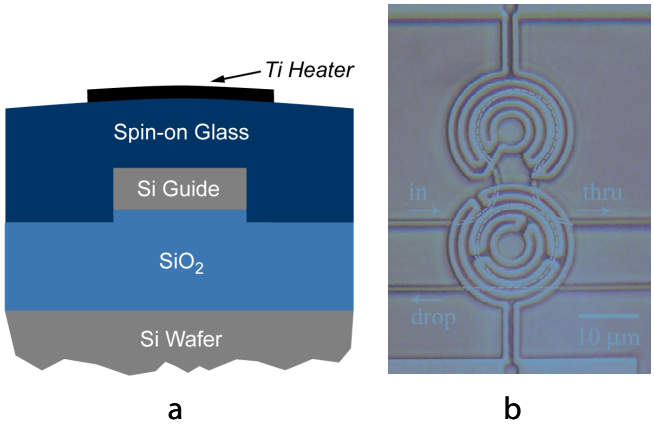
T. Barwicz, M.A. Popovic, F. Gan, M. Dahlem, C.W. Holzwarth, P.T. Rakich, E.P. Ippen, F.X. Kaertner, H.I. Smith
Sponsorship: Pirelli S.p.A (Milan, Italy)

Reconfigurable optical add-drop multiplexers (ROADMs) are key components of modern optical networks. Data in optical fibers is carried via numerous wavelengths, referred to as channels. ROADMs allow the rerouting (dropping) of a subset of the data channels traveling in an optical fiber and replacing these with new data streams (adding) that will be carried in the fiber at the previously rerouted wavelengths. The term "reconfigurable" indicates that the subset of dropped channels can be changed in real time while the ROADM is in operation.

Previously, we developed nanofabrication techniques of unprecedented accuracy that allowed us to demonstrate, in silicon-rich silicon nitride, the most advanced micro-ring filters reported to date [1]. In the present work, we employ silicon micro-rings to take advantage of the lower optical loss and high thermo-optical coefficient of silicon. The latter enables wide-range tuning of the wavelengths of operation of the ROADM by means of integrated heaters. Line-edge roughness is of critical concern in silicon waveguides as it translates into optical-propagation loss via scattering of the guided mode. We found that the smoothest waveguides are obtained using hydrogen silsesquioxane (HSQ) as an e-beam resist and etch-mask. Reactive ion etching was done in HBr. Figure 1 is an electron micrograph of the coupling region between a micro-ring and a bus waveguide defined in HSQ. The patterning was done by dose-controlled scanning electron-beam lithography. Figure 2 presents a cross-sectional diagram and top-view micrograph of our implementation of a silicon waveguide with an integrated heater.



▲ Figure 1: Top-view scanning-electron micrograph of a coupling region defined in HSQ. Line-edge smoothness is critical for Si waveguides. The patterning is based on scanning electron-beam lithography. The minimum feature size required is ~100 nm and must be controlled to ~ 5 nm.



▲ Figure 2: (a) Cross-sectional schematic of a silicon waveguide with an integrated titanium heater. Spin-on glass is used for the upper cladding of the waveguide to allow self-planarization and to avoid filling problems in narrow gaps. (b) Top-view optical micrograph of an overclad silicon-micro-ring filter below a Ti heater.

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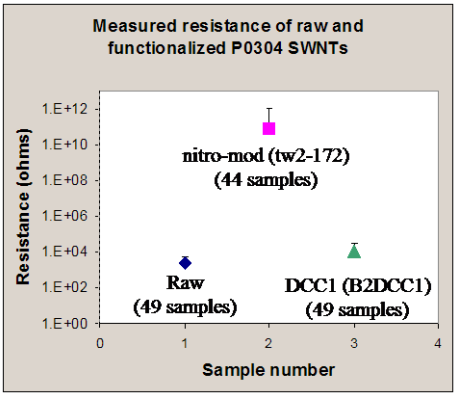
Carbene-modified Single-walled Carbon Nanotubes: Electronic Property Control via Chemical Modification

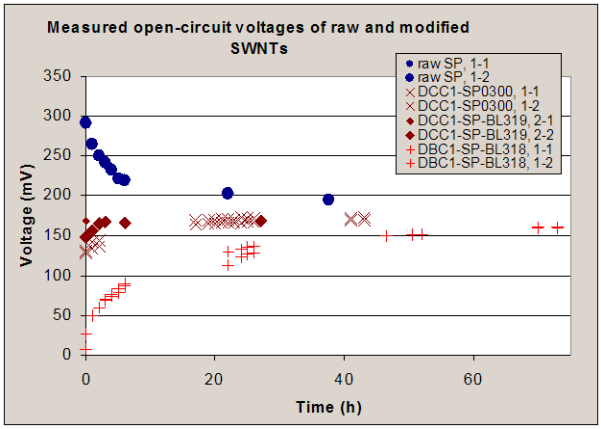
T.M. Wu, B. Long, B. Wunsch, F. Stellacci
Sponsorship: SRC/FCRP IFC

Carbon nanotubes (CNTs) are materials with excellent mechanical, thermal, and electronic properties that may be suitable for electronic devices and interconnects. A potential method for the fabrication of CNT structures on a substrate involves the deposition of CNTs from suspension coupled with chemically-driven alignment or subsequent lithographic processes. As-produced CNTs are notoriously difficult to disperse in solvents, often requiring high-powered sonication or chemical modification that can damage CNT physical and electronic structure. Recently, a covalent chemical functionalization scheme has been proposed [1] that may allow modification of CNTs to impart solubility without the corresponding loss in electronic conductivity observed in other covalent modification schemes. We have fabricated interdigitated electrodes with single-walled carbon nanotubes (SWNTs) to test this theory (see Figure 1), and results indicate that carbene-modified SWNTs are significantly less resistive than SWNTs modified with a standard covalent radical method while remaining more soluble than the as-produced material.

In addition to the conductance-preserving properties of the carbene-CNT chemistry, there is also evidence that the carbene chemistry may shift the Fermi levels of functionalized CNTs. Using an electrochemical open-circuit potential measurement technique, we have observed varying and reproducible steady-state potential values for SWNTs modified with different carbenes (see Figure 2). This approach may allow the development of a chemical doping technique for CNTs where the final Fermi level is determined by the type of substituent on the carbene group.



▲ Figure 1: Measured resistance for unmodified and modified SWNTs. The carbene-modified sample (green) show slightly higher resistance than the unmodified sample (blue) but significantly lower resistance than the sample modified with a standard covalent radical method (magenta). Error bars represent two standard deviations.



▲ Figure 2: Measured open-circuit potentials for unmodified and modified SWNTs. The unmodified samples are shown in blue. The SWNTs modified with a dichlorocarbene are shown in brown; SWNTs modified with a dibromocarbene are shown in red.

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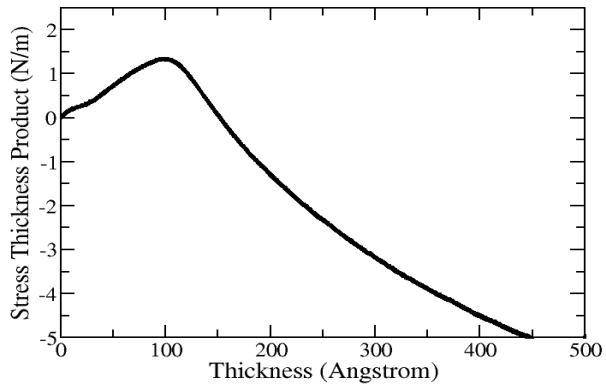
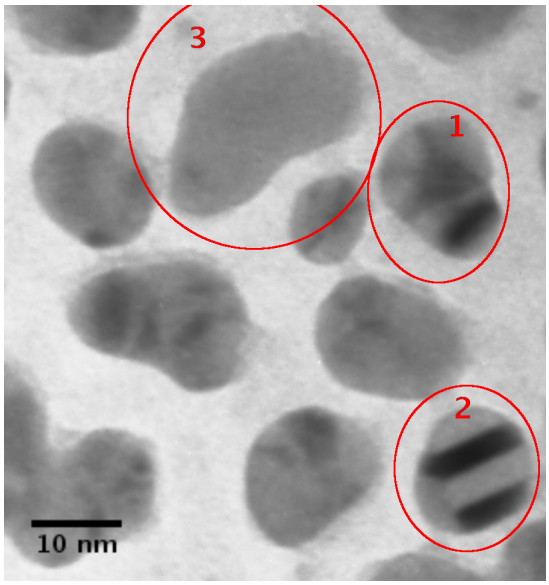
Stress Evolution and Defect Formation during Nanoparticle Coalescence

A.R. Takahashi, J. Leib, C.V. Thompson
Sponsorship: NSF, Singapore-MIT Alliance

Metal thin films are key components in a wide variety of micro- and nano-systems. The performance characteristics of thin films are strongly dependent on the intrinsic stress in the film. Figure 1 shows an example of the variation of film stress with film thickness. The tensile stress peak is a key feature in the stress evolution of the film and is associated with the process of particle coalescence [1]. Our computational modeling via molecular dynamics indicates that the magnitude of the stress incorporated during coalescence may be modified by the formation of planar defects [2]. These planar defects relieve strain energy at the expense of stacking fault interface energy. Our calculations also show that planar defects induced by particle coalescence occur only for a specific range of particle sizes. We rationalize the existence of the size window using an analytic energetic model consistent with existing continuum theories for particle coalescence [3]. The presence of stacking faults in coalesced nanoparticles has been confirmed by transmission electron microscopy (TEM); see Figure 2. The planar defects can further reduce the intrinsic stress by changing position within the particle. The TEM observations of partially coalesced structures suggest that the faults anneal out of the particles at high temperatures. Our observations and model show that the intrinsic stress in thin films can be tuned by controlling the particle size at coalescence and defect density.



▲ Figure 1: Stress thickness product as a function of Au film thickness on silicon nitride. The tensile peak in the curve is associated with the process of island coalescence.



▲ Figure 2: A TEM image of Au nanoparticle structures after 20 Angstroms of deposition. Regions 1 and 2 show particles clearly containing stacking faults. Region 3 shows a larger particle that appears to be defect-free.

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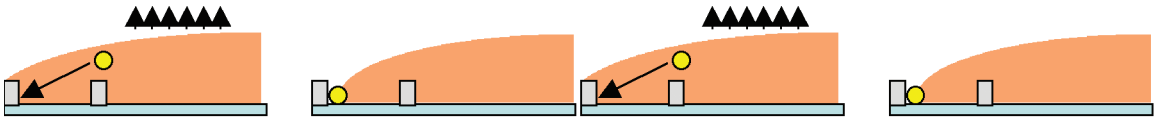
Templated Dewetting of Nanoparticle Solutions

S.-W. Chang, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

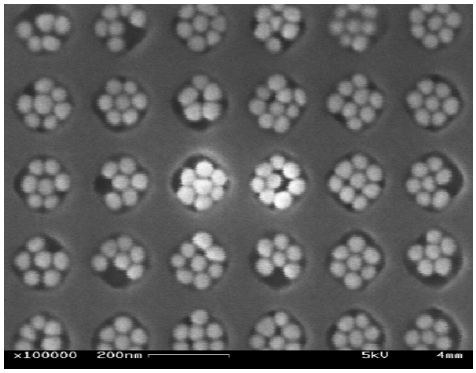
A major issue in nanotechnology is the need for versatile techniques for self-organization of nanometer-scale building blocks, such as nanoparticles, to form large-area periodic systems. Our goal is to combine physical templating and self-assembly to form nanoparticle arrays that can be used as catalysts for the growth of nanowire or nanotube arrays and other applications such as nanoelectronics or nanophotonics.

A combination of physical templating and capillary interaction has been employed to self-organize colloidal particles into lithographically patterned templates with well-controlled sizes and structures. The patterned features can act as pinning sites for the moving contact line, leading to high particle concentrations near the pinning sites. Particles in the physical templates then self-assemble into close-packed structures due to long-range immersion forces.

As an initial effort, patterned substrates with gratings and holes were fabricated using interference lithography. The substrates were then immersed in Au nanoparticle solutions for evaporation. The resulting capillary interaction due to solvent evaporation was found to be sufficiently strong to force the nanoparticles into the templated features without leaving particles on the surrounding areas. Figure 1 presents a schematic outline of the process. Current efforts include applying the templated dewetting approach to smaller nanostructures and on different topographies.



▲ Figure 1: Schematic of the templating process.



▲ Figure 2: Au particles that are 50 nm in diameter self-assemble into templated holes.

Templated Self-assembly for Nanoparticle Organization: Solid-state Dewetting

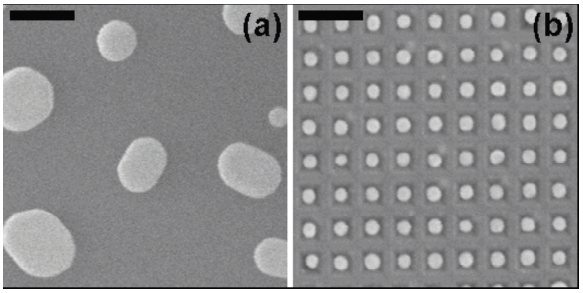
A.L. Giermann, J. Ye, Y. Wang, W.K. Choi, H.I. Smith, C.V. Thompson
Sponsorship: Singapore-MIT Alliance, NSF

We are investigating solid-state dewetting of thin films as a technique for producing ordered arrays of metal nanodots over large areas. Such arrays are used as catalysts for nanowire and nanotube growth and may also be of interest in memory or plasmon device applications. Our research comprises two main dewetting systems: 1) polycrystalline films on amorphous substrates and 2) epitaxial films on single crystal substrates.

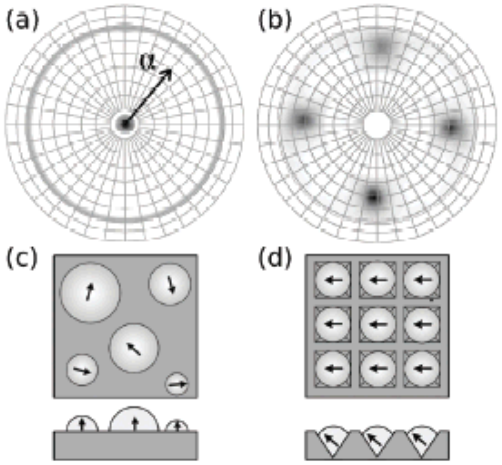
In our study of polycrystalline films, we influence dewetting behavior with topographically patterned oxidized silicon substrates that modulate the curvature of as-deposited films. Gold films deposited and annealed on di-periodic arrays of pyramidal pits result in one-to-one self-assembly of ordered arrays of gold particles over large areas. Average particles sizes of less than 50 nm can be achieved. Compared to dewetting on flat substrates, the templates impose a significant decrease in average particle size and ensure a narrow size and spatial distribution (Figure 1). This technique uniquely results in crystallographic ordering of the particles, imposing an in-plane texture and changing the out-of-plane texture (Figure 2).

Our current efforts include investigation of other topographic geometries and development of numeric models to predict topographies that lead to the formation of multiple particles per lithographic feature. We are also expanding the technique to nickel, which is known to catalyze carbon nanotube growth, with the goal of studying the impact of crystallographic texture and facet morphology on nanotube growth.

In our study of epitaxial films, we grow nickel thin films on single crystal magnesium oxide substrates and observe the dependence of the dewetting behavior on various experimental parameters, such as crystallographic orientation of the substrate, film thickness, annealing time, and annealing temperature. The crystallographic orientation of the substrate has a profound effect on the evolution and final form of the dewetted film. We believe these differences are associated with surface energy anisotropy of nickel. Dewetting of single crystal films also offers the potential for obtaining ordered arrays of crystallographically aligned catalyst particles.



▲ Figure 1: The effect of topography on particle morphology. The results of dewetting a 10-nm-thick Au film on (a) a flat substrate and (b) a topographic substrate. Micrographs are displayed at the same magnification to emphasize the effect of topography on particle size. Scale bars are 200 nm in length.



▲ Figure 2: The effect of topography on particle orientation. (a) and (b) show Au <111> X-ray pole figures (37.4° < 2θ < 38.6°), (a) for particles on a flat substrate and (b) for particles on a topographic substrate. (c) and (d) schematically illustrate the particle orientation on flat and topographic substrates, respectively. The arrows indicate the <111> projection.

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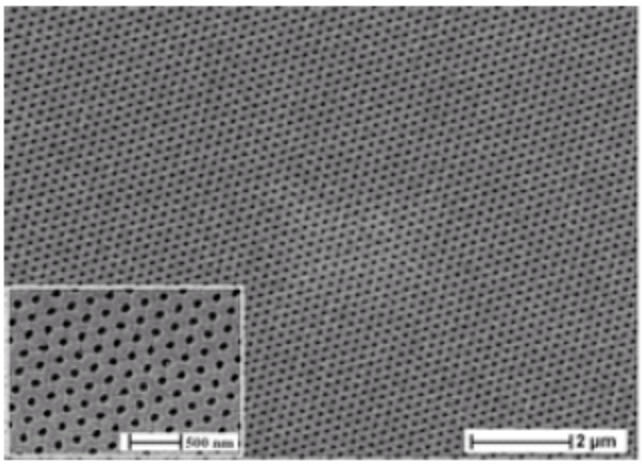
Anodic Aluminum Oxide Scaffolds for Realization of Integrated Self-assembled Devices

J. Oh, C.V. Thompson
Sponsorship: SRC/FCRP IFC, Singapore-MIT Alliance

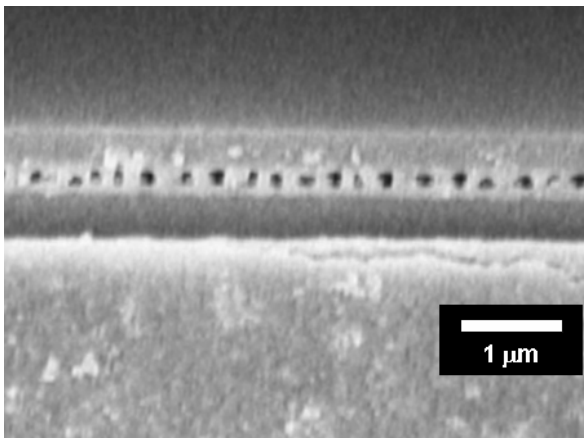
Nano-sized materials are core building blocks for advanced functional devices such as interconnects, logics, memories, sensors, and displays. To integrate synthesized nano-materials into the devices, it is desirable to fabricate them with controlled size and distribution on the device applicable substrates with precise location. As a strategy, we are developing templated self-assembly methods that combine top-down (lithography) and bottom-up (self-assembly) approaches for fabricating and assembling metallic and semiconducting nano-wires, rods, and dots, for new applications including nano-contacts for devices and interconnects for mixed-material and multifunctional micro- and nano-systems.

Anodic aluminum oxide (AAO) is a self-ordered nanostructured material that is well-suited as a scaffold to grow multi-functional nanowires and nanotubes for use in magnetic, electronic and opto-electronic devices. Perfectly ordered porous alumina scaffolds were developed by combining interference lithography with anodization of the evaporated Al thin films on silicon substrates. The regular array of electrically insulating holes obtained had diameters of less than 30 nm and aspect ratios >50:1, which is hardly achievable without the state-of-art Si technology. Topographic templating of long-range order in anodic aluminum oxide allows independent control of the pore size, spacing, and order symmetry in ranges not achievable without templating. Using the perfectly-ordered AAO scaffolds, we have fabricated ordered metallic nanodots, nanorods, and nanotubes as well as well-aligned multi-walled carbon nanotubes (CNTs) on silicon substrates. In addition to the vertically ordered AAO scaffolds, we are also developing the porous alumina scaffold, horizontally lying on the substrate to grow nano-materials on the plane of substrate.

We are currently pursuing the growth of uniform arrays of CNTs in templated AAO scaffolds to obtain statistical electrical and thermal characterization of CNTs as a function of nanotube diameter and length variations



▲ Figure 1: An SEM image of perfectly ordered porous alumina with hexagonal symmetry on silicon over wafer-scale areas with pore diameter of 80 nm and pore spacing of 180 nm [1]



▲ Figure 2. An SEM image of a monolayer of porous alumina lying horizontally on the substrate.

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Catalyst Engineering and Carbon Nanotube Growth Mechanisms

G.D. Nessim, Y. Wang, A.J. Hart, D. Acquaviva, J. Oh, J.S. Kim, C. Morgan, N. Abate, M. Seita, C.V. Thompson
Sponsorship: SRC/FCRP IFC, Intel Corporation

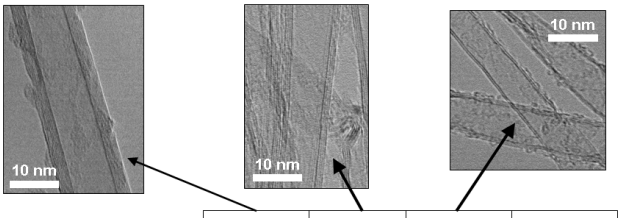
As integrated circuit technology is developed at dimensions below 45 nm, carbon nanotubes (CNTs) represent an ideal replacement for copper interconnects as they can carry higher current densities, do not need liners, and do not suffer from electromigration. However, fabrication issues such as growing the desired type of CNTs in a selected position and making electrical contacts and interconnections remain major technical challenges.

Consistent with our goal of making the use of carbon nanotubes a manufacturing reality for interconnect vias, we have achieved the following results:

We discovered that by introducing the reducing gas (hydrogen) at specific times during the thermal chemical vapor deposition process, we were able to control the diameter and the number of walls of vertically-aligned CNTs grown on insulating substrates, as shown by Transmission Electron Microscopy images. We also analyzed the substrate with Atomic Force Microscopy to correlate catalyst morphology with CNT density.

Using appropriate catalyst/substrate metallic thin films, we have grown carbon nanostructures at temperatures below 500 degrees Celsius. We analyzed properties such as the grain structure of the substrate to maximize CNT density and achieve vertical alignment. Electrical measurements show contact of the CNTs with the conductive substrate.

Finally, we have grown CNTs on conductive substrates in an insulating anodized alumina scaffold with perfectly periodic templated pores. This technique will allow us to emulate a nanometer-scale via system for measurement of electrical and thermal properties of CNTs, averaged over a large regular matrix. We plan to use this structure to develop CNT-based devices.



	H_2 @ -5	H_2 @ 0	H_2 @ +10	H_2 @ +13
Outer diameter [nm]	13.6 ±1.9	9.8 ±1.8	7.4 ±1.0	8.1 ±1.3
Number of walls	7.3 ±1.1	4.7 ±1.0	3.0 ±0.9	3.1 ±1.0
CNT areal density [/cm^2]	3.9×10^9	2.6×10^{10}	4.9×10^{10}	4.5×10^{10}
Growth rate [μm/min]	32	37	154	**440**

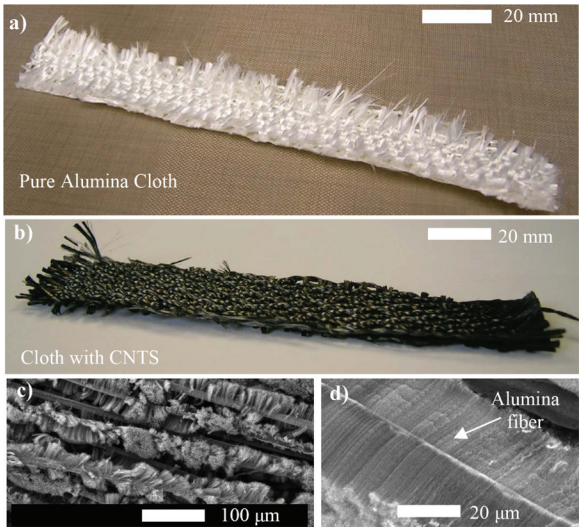
▲ Figure 1: Transmission electron microscope images of multi-wall carbon nanotubes grown using iron catalysts on alumina substrates using the same process but delaying the introduction of hydrogen. As the delay in hydrogen introduction is increased (up to a limit), the diameters and number of walls of the tubes reduces, and the length and number of tubes per area increases.

Fiber Composites Reinforced by Aligned CNTs

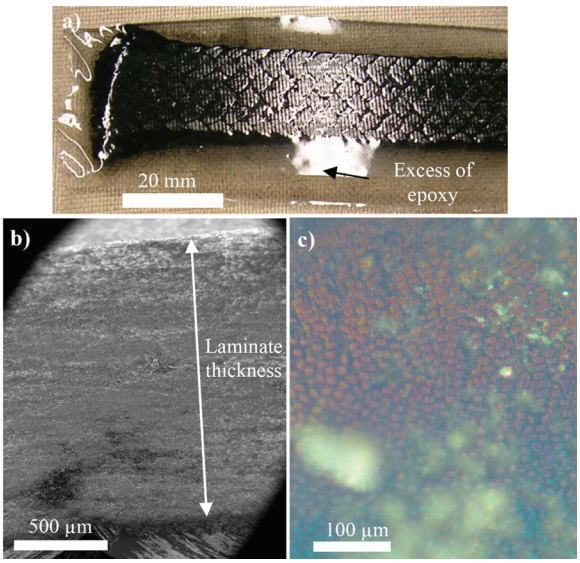
E.J. Garcia, A.J. Hart, B.L. Wardle (in coll. with A.H. Slocum)
Sponsorship: Airbus S.A.S., Karl Chang Innovation Fund, La Caixa Foundation

The interaction, or wetting, of long aligned carbon nanotube (CNT) forests with off-the-shelf (no solvent added) commercial thermoset polymers is investigated experimentally. A technique for creating vertically aligned CNT composite microstructures of various shapes is presented [1]. Direct characterization of the mechanical properties of the nanocomposites structures is also presented in this work. The mechanical reinforcement results (220% increase of the Young´s modulus at 2% volume loading [2]) support the feasibility of using these CNT forests in large-scale, hybrid, advanced composite architectures reinforced with aligned CNTs.

A hybrid composite architecture consisting of aligned carbon nanotubes (CNTs), woven ceramic fiber cloth, and a thermoset epoxy is described and fabricated. Interlaminar reinforcement improvement is also quantified experimentally [3]. The nano-engineered laminates are constructed using conventional hand lay-up techniques. Fabrication begins with growth of aligned CNTs on the surface of fibers in a ceramic fiber cloth using a thermal chemical vapor deposition process and liquid-based catalyst as shown in Figure 1. Effective wetting of the CNT/cloth by the polymer is shown via optical and scanning electron microscopy (see Figure 2). This intralaminar reinforcement by CNTs also extends to the interlaminar region between individual plies in the laminate. The strength of the interlaminar reinforcement is investigated experimentally, focusing on shear strength with an average improvement of 70% over the unreinforced laminate. Ongoing investigations focus on such nano-engineered laminates, including mechanical and multifunctional performance benefits derived from the aligned nature of the CNTs appearing everywhere in the laminate. Future work focuses on extending this model architecture to carbon- fiber-based advanced composites.



▲ Figure 1: a) As-received alumina cloth; b) Alumina cloth with CNTs grown on the surface of fibers; c) An SEM of the alumina fibers with CNTs grown on the surface; d) An SEM of one alumina fiber with well-aligned, 30-µm long CNTs grown on its surface.



▲ Figure 2: a) Nanoengineered composite laminate before cutting the specimen for inspection; b) An SEM picture of a cross section of CNT/alumina cloth/epoxy hybrid composite with no evidence of voids; c) Optical microscopy picture of the cross section, showing regular distribution (volume fraction) of the fibers inside the cloth.

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[2] E.J. García, A.J. Hart, B.L. Wardle, A.H. Slocum, "Fabrication and nanocompression testing of aligned CNT/polymer nanocomposites," *Advanced Materials*, 2007, to be published.

[3] E.J. García, A.J. Hart, B.L. Wardle, A.H. Slocum, "Aligned carbon nanotube reinforcement of ply interfaces in woven composites," presented at the *48th AIAA/ASME/ASCE/AHS/ASC Structures, Structural Dynamics, and Materials Conference*, Apr. 2007.

Section 4

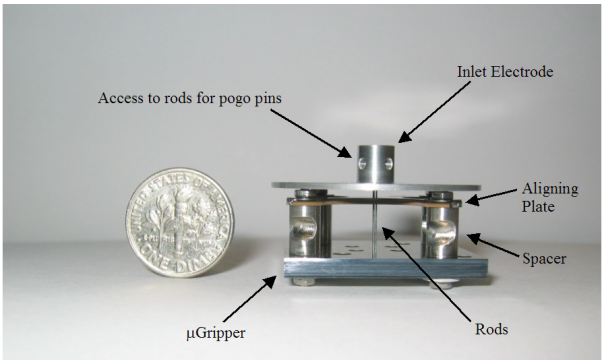
MEMS & BIOMEMS

A Versatile MEMS Quadrupole Platform for Portable Mass Spectrometry Using the First and Second Stability Regions

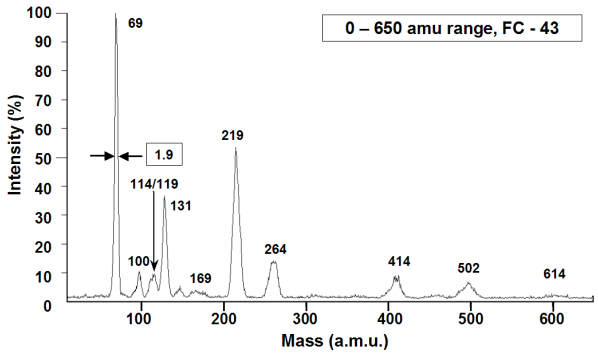
L.F. Velásquez-García, K. Cheung, A.I. Akinwande
Sponsorship: DARPA

The Micro Gas Analyzer Program aims to develop portable, low-power, fast and low-false-alarm-rate gas analyzer technology for a wide range of applications. One of the subsystems of the gas analyzer is a mass filter. An array of micro-fabricated quadrupole mass filters is being developed for this purpose. The quadrupoles will sort out the ions based on their specific charges. Both high sensitivity and high resolution are needed over a wide range of ion masses, from 15 to 650 amu. In order to achieve this performance, multiple micro-fabricated quadrupoles, each operating at a specific stability region and mass range, are operated in parallel.

The proof-of-concept device is a single, linear quadrupole that has a micro-fabricated mounting head with meso-scaled DRIE-patterned springs. The mounting head allows micron-precision hand assembly of the quadrupole rods [1] –critical for good resolution and ion transmission. The micro-fabricated mounting head can implement quadrupoles with a wide range of aspect ratios for a given electrode diameter. The springs can be individually actuated using spring tip handlers. The current version of the spring-head is able to interact with rods with diameters from 1588 µm down to 250 µm. The quadrupoles that have been implemented thus far span the aspect ratio range from 30 to 60. The choice of electrode diameter takes into account the dimensional uncertainties and alignment capabilities with respect to the expected resolution and transmission goals. Figure 1 shows an assembled MEMS quadrupole with 250-micrometer diameter rods. Figure 2 shows the experimental data of one of these quadrupoles using FC-43 as a calibration compound, where a mass resolution of 2 amu and a full mass range of 650 amu are demonstrated, while using a 1.44 MHz RF power supply to drive the quadrupole with a constant-width circuit made by the Extrel company (Pittsburgh, PA). To obtain better resolution, the MEMS quadrupoles have been driven with up to 4 MHz RF sources, resulting in 0.7 amu peak width. Also, the devices have been driven in the second stability regions to obtain 0.4 amu of peak width and smoother peaks. Current research efforts concentrate on developing RF power supplies of higher frequency and further exploration of the second stability region to obtain better performance.



▲ Figure 1: A micro-fabricated quadrupole with electrode diameter equal to 250 micrometers, near a dime for size comparison. The micro-fabricated part of the device is the square base, which contains a system of meso-scaled DRIE-patterned springs.



▲ Figure 2: Experimental characterization of a MEMS quadrupole, using the compound FC-43 to get peaks in the 1 – 650 amu mass range. The peak width is estimated at 2 amu, using a 1.44-MHz-RF-power supply. Peak widths as small as 0.4 amu have been obtained.

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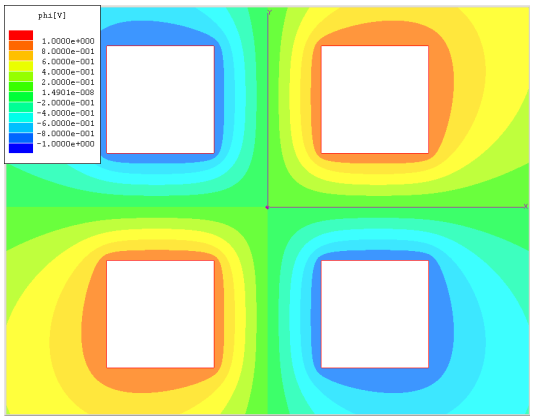
First Principles Optimization of Mass-producible Microscaled Linear Quadrupoles for Operation in Higher Stability Regions

K. Cheung, L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

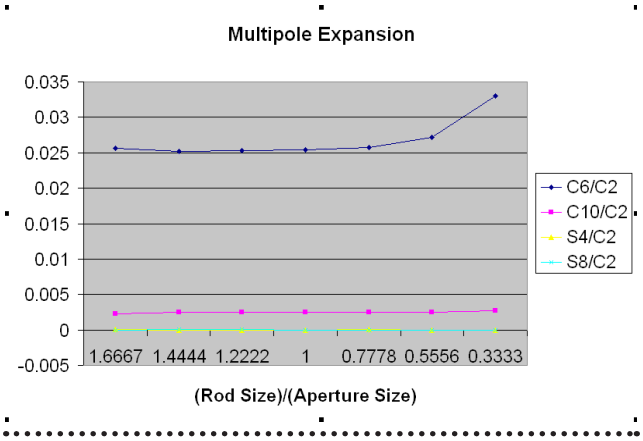
In recent years, there has been a desire to scale down linear quadrupoles. The key advantages of this miniaturization are the portability it enables and the reduction of pump-power needed due to the relaxation on operational pressure. Various attempts at making microscaled linear quadrupoles met with varying degrees of success [1-2]. Producing these devices involved some combination of precision machining or microfabrication and downstream assembly. For miniature quadrupole mass filters to be mass-produced cheaply and efficiently, manual assembly should be removed from the process.

A purely microfabricated quadrupole mass filter comprising a planar design and a rectangular electrode geometry is proposed. Quadrupole resolution is inversely-proportional to the square of the electrode length, thus favoring a planar design since electrodes can be made quite long. Rectangular rods are considered since that is the most amenable geometric shape for planar microfabrication. This deviation from the conventional round rod geometry calls for optimization and analysis. Electrode designs were parameterized, and the potential fields were solved using Maxwell 3D (Figure 1). The fields were decomposed using a multipole expansion to examine the higher-order coefficients (Figure 2). This process was used to minimize the significant high-order terms, thus optimizing the design and determining the ultimate limitations of the device.

Higher-order field contributions arising from geometric non-idealities lead to non-linear resonances. These resonances manifest as peak splitting that is typically observed in quadrupole mass spectra. Reported work involving linear quadrupoles operated in the second stability region show improved peak shape without these splits [3]. It is believed that operating the device in the second stability region will provide a means to overcome the non-linear resonances introduced by the square electrode geometry. This study was conducted to justify a fully microfabricated, mass-producible, MEMS linear quadrupole mass filter. Successful implementation of such devices will lead into arrayed configurations for parallel analysis and aligned quadrupoles operated in tandem for enhanced resolution.



▲ Figure 1: Potential field solution generated by Maxwell 3D using a rectangular electrode geometry. Geometries were parameterized and solved.



▲ Figure 2: Dependence of the coefficients derived from a multipole expansion on the ratio of rod size to aperture size. The C2 refers to an ideal quadrupole field.

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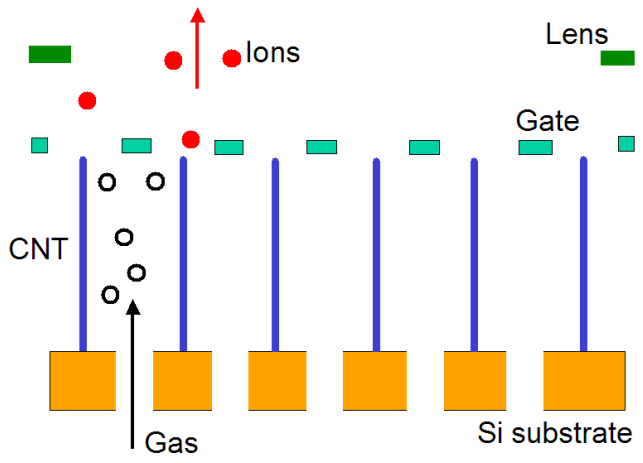
A Single-gated Open Architecture Carbon Nanotube Array for Efficient Field Ionization

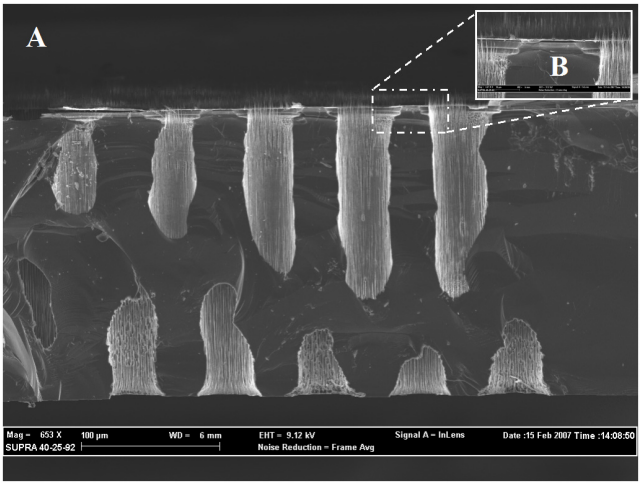
L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

Mass spectrometers require a suitable ionizer to be able to discern the chemical composition of the sample that they are analyzing. Traditional ionizers for gases use either chemical ionization (CI) or electron impact ionization (EI). In the latter case, electrons from thermionic sources produce ions by colliding with neutral molecules. More efficient carbon nanotube-based field emitted electron impact ionizers have been developed [1]. However, one of the drawbacks of electron impact ionization is that the sample is transformed into fragmentation products. Several samples could have similar fragmentation spectra but be quite different compounds, with radically different properties (for example, one substance can be a poisonous agent while another is a harmless material). Therefore, an approach to reduce the fragmentation products would improve the informational power of the mass spectrometer.

Field ionization soft-ionizes molecules, thus reducing the fragmentation products. In the field ionization scheme, ions are created by directly tunneling electrons from the outer shell of neutral molecules by virtue of a very high electric field [2]. The electric field is produced by high aspect ratio field enhancers and the application of a large (up to 1 kV) bias voltage. Carbon nanotubes are ideal field enhancers because of their high aspect ratio and their reduced tip radius. A good field ionizer should work in the field-limited regime instead of the molecular flux-limited regime, where all the molecules that approach the high field region are thus ionized. In the case of the electron impact ionizers, a closed architecture is implemented because it is intended to protect the field enhancers from back streaming ions [3]. Therefore, an open architecture, where the field enhancers surround a through-hole, is a more suitable approach to produce field ionization. We plan to implement a single-gated field ionizer array with an open architecture. Figure 1 shows a schematic of the open architecture concept. Figure 2 shows a cross section of the device. Current research effort focuses on device characterization.



▲ Figure 1: Schematic of a Field Ionizer array. The gas inlet provides neutral species to the field enhancers. If the molecules of the gas come close enough to the CNT tips, an electron from the outer shell of the molecule will tunnel to the CNT, thus ionizing the molecule.



▲ Figure 2: A single-gated CNT field ionizer array grown at MIT. Field view of an array cross-section (A), and detail of two adjacent field ionizers (B). The ionizer well has a film of silicon dioxide 5 µm thick below the gate that acts as electrical insulator between the gate and the CNTs. The CNT catalyst was Ni 7.5 nm thick.

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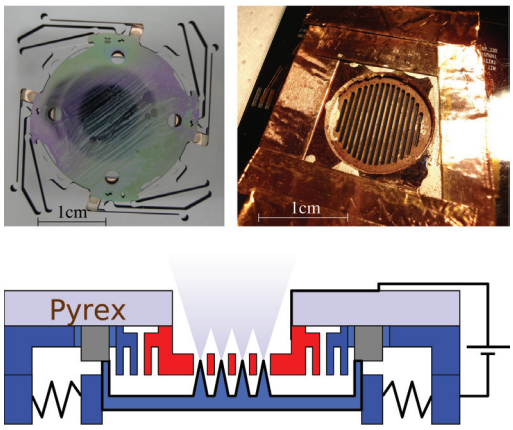
A Fully Micro-fabricated Planar Array of Electrospray Emitters for Space-propulsion Applications

B. Gassend, L.F. Velasquez-Garcia, A.I. Akinwande, M. Martinez-Sanchez
Sponsorship: AFOSR, DARPA

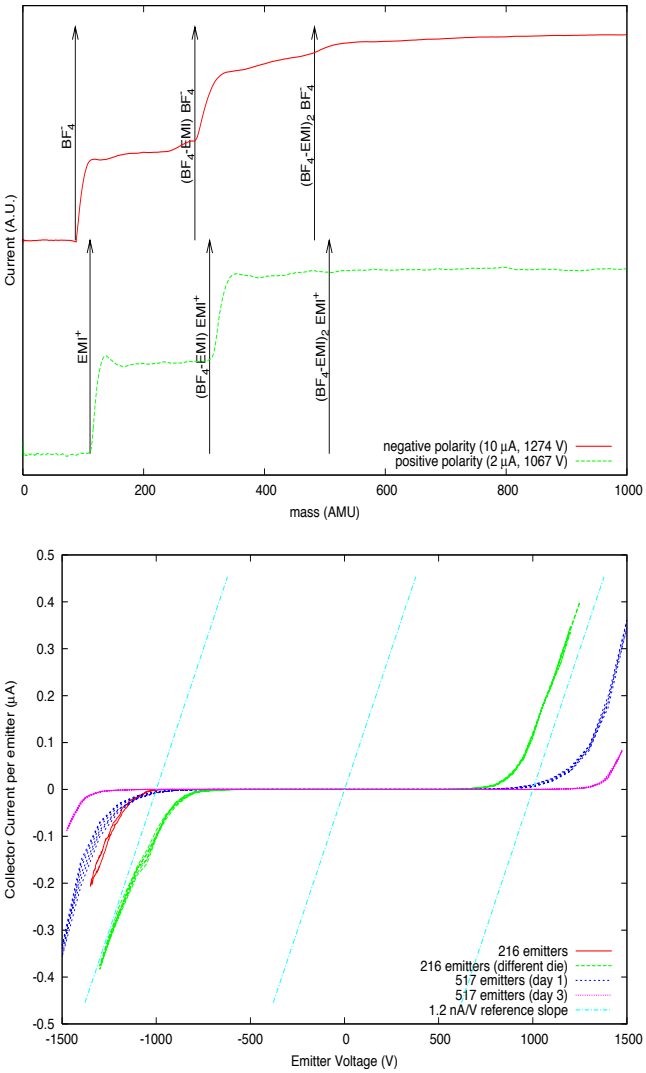
Electrospray thrusters work by extracting ions or charged droplets directly from a liquid surface using an electrostatic field and accelerating them in that field to produce thrust [1]. This method could lead to more efficient and precise thrusters for space propulsion applications. Emission occurs from sharp emitter tips, which enhance the electric field and constrain the emission location. The electrospray process limits the thrust from a single tip. To get into the millinewton range will require an array with tens of thousands of emitters. Batch microfabrication is well suited to making this array.

We have designed, built, and tested a thruster made in silicon using deep reactive ion etching (DRIE) and wafer-bonding technology (see Figure 1). This thruster comprises two components. The emitter die has up to 517 emitters in a 0.75 cm^2 area, formed using DRIE and SF_6 etching, and is plasma treated so that liquid can be transported to the tips in a porous black silicon surface layer. The extractor die incorporates the extractor electrode, a Pyrex layer for insulation, and the springs, which are used to reversibly clamp the emitter die [2]. This versatile assembly method allows the extractor die to be reused with multiple emitter dies and potentially with emitter concepts radically different from the one we have experimented with.

Figure 2 shows data collected when firing the thruster with the ionic liquid EMI-BF_4. Measurable emissions occurred for extraction voltages down to 700 V. The current collected on the extractor electrode was less than 3% of the emitted current over a wide operating range and often less than 0.1 %. Beam-divergence half-angles were between 15 and 30 degrees, depending on the operating conditions. Emitted currents of 500 nA/emitter were observed in stable operation, for expected thrusts of 25 nN/emitter. Time-of-flight measurements prove operation in the ion emission regime, which is most efficient for propulsion.



▲ Figure 1: The assembly mechanism (top-left), the extractor electrodes (top-right), diagram of the thruster (bottom).



▲ Figure 2: Time of flight data (top) and current-voltage characteristic (bottom) of the thruster.

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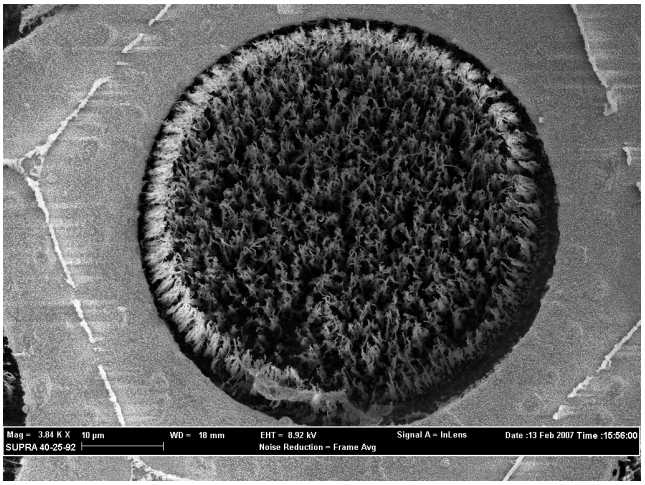
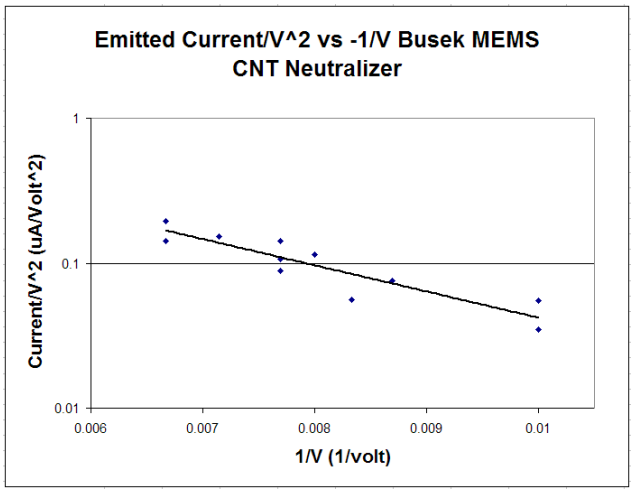
Carbon Nanotube Electron Sources for Space Propulsion Applications

L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

Low-power, low-voltage, efficient field emission neutralizers for FEEPs [1], colloid thrusters [2], and other micro-propulsion engines are attractive for nanosatellites because they do not use mass flowrate to operate, unlike more conventional neutralizing solutions such as hollow cathodes [3]. Electrons are field-emitted from the surface of metals and semiconductors by the application of a high electrostatic field. Field emitters use high aspect ratio structures to generate very high fields even when low voltages are applied. The ideal field enhancing structure is a rounded whisker [4]. Micro-engineered field emission neutralizers would have smaller starting voltages, better area usage, and more uniform I–V characteristics, compared to macro/meso fabricated field emitter versions. Plasma-Enhanced Chemical Vapor Deposited (PECVD) Carbon Nanotubes (CNTs) are rounded whiskers with 100 nm or less of tip radius and 13 µm or more tall. The adoption of CNTs as electron-emitting substrate has recently being shown to have advantages compared to Spindt emitters because of the higher aspect ratio of CNTs and their superior resistance to harsh environments. This research focuses on the development of a batch-fabricated MEMS neutralizer that uses PECVD CNTs as field enhancers (Figure 1). As a reference, a previously made Busek-MIT MEMS CNT device that uses a randomly oriented CNT matrix produced by Busek Co. (Natick MA) with a proprietary arc-based process yielded devices with Fowler-Nordheim emission, startup voltage as low as 100 V, and electron currents as large as 3.2 mA/cm^2 with about 20% of gate current interception.



▲ Figure 1: Top view of a 14-µm-tall CNF forest inside a microfabricated well. The well has integrated a gate to bias voltage to the CNT forest to produce field emission.



▲ Figure 2: The I-V characterization of a similar CNT-based field emitter array. The device was jointly developed with the Busek company (Natick, MA)

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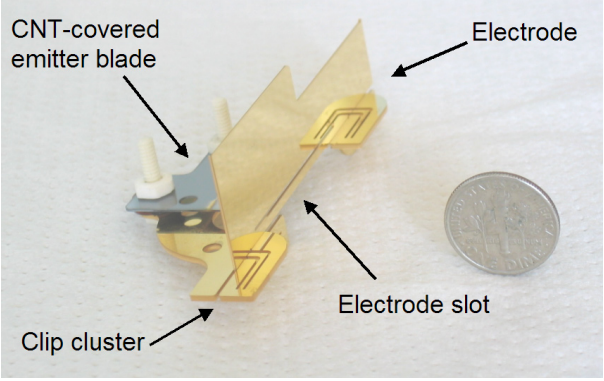
Carbon Nanotubes for Electrospray Nanofluidic Applications

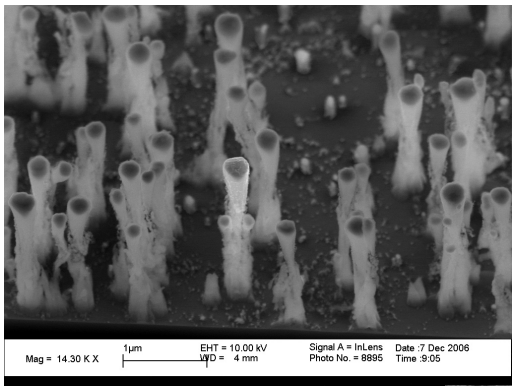
L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

Electrospray is the technique to soft-ionize liquids by applying a high electric potential to a liquid meniscus. The liquid meniscus is deformed into a cone [1], and charged species are emitted from its apex. The emission can be solvated ions, charged droplets, or a mix of the two. This low-divergence charged species source can be used in diverse applications such as mass spectrometry, propulsion, printing, and etching. Our research group has successfully developed several multiplexed MEMS electrospray sources, mainly intended for space propulsion applications. These devices include internal pressure-fed spouts that emit charged droplets [2] and externally surface tension fed spouts that emit solvated ions [3]. In all cases, the emitter field enhancers and the hydraulic impedance are provided using silicon-based structures. Furthermore, the devices use a 3D packaging technology that allows decoupling the process flows of the subsystems without loss in emitter density [4]. Consequently, it is possible to use radically different fabrication techniques and materials to implement MEMS electrospray arrays.

This project intends to investigate the application of Plasma Enhanced Chemical Vapor Deposition Carbon Nanotubes (PECVD CNTs) in multiplexed electrospray sources. Two research directions are currently pursued: the use of CNTs as hydraulic impedance to ballast the emitter array (both in internal and external architectures) and the use of CNTs as emitter field enhancers. On the one hand, PECVD CNT forests can be custom tailored to match a desired morphology. On the other hand, PECVD CNTs have remarkable field enhancing properties. Figure 1 shows a silicon-based externally fed electrospray linear emitter array that uses PECVD CNTs as hydraulic impedance, while Figure 2 shows the PECVD CNT forest grown on top of the silicon structures, using our group's reactor. Current research is focused on exploring the wettability of CNT forests using different liquids, catalysts, and growth conditions. These results will be used to choose the proper nanostructure to be used in an externally fed MEMS electrospray head that will eventually include CNT-based field enhancers.



▲ Figure 1: A 145 externally fed electrospray linear array. The emitter array is about 1-inch long.



▲ Figure 2: An SEM of a zoomed PECVD CNT forest used as hydraulic impedance for the electrospray array. The CNT height is about 1 µm.

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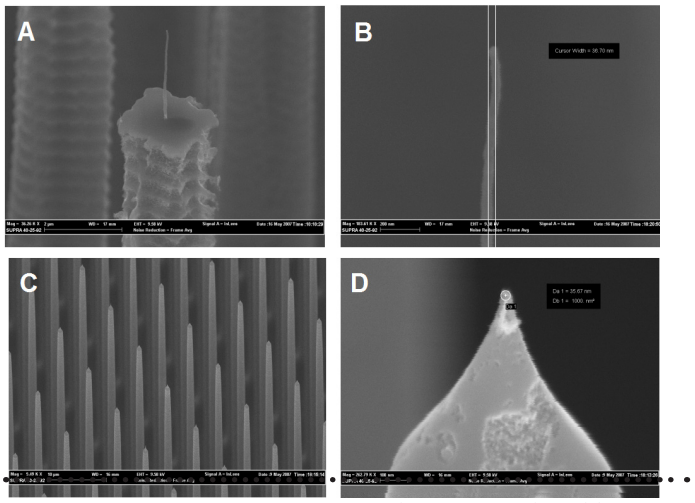
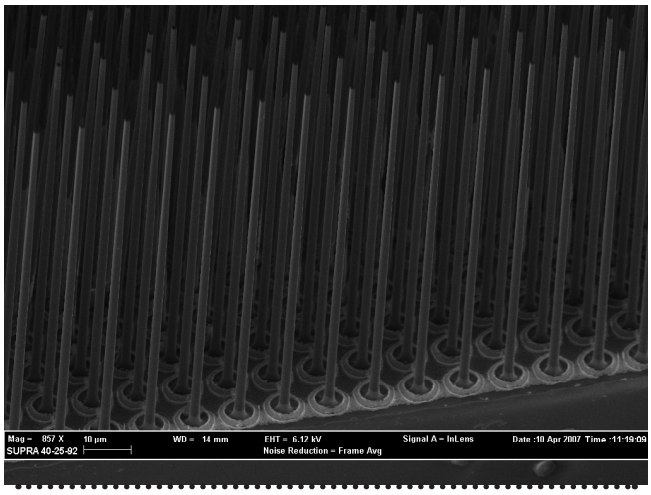
A High-density Electron Source that Uses Un-gated Transistors for Ballasting

L.F. Velásquez-García, A.I. Akinwande
Sponsorship: AFRL

Electrons are field emitted from the surface of metals and semiconductors when the potential barrier (work function) that holds electrons within the metal or semiconductor is deformed by the application of a high electrostatic field. Field emitters use high aspect ratio structures with tips that have nanometer dimensions to produce a high electrostatic field with a low applied voltage. We are implementing two types of field enhancers: carbon nanofibers (CNFs) and silicon conical tips (Figure 1). Spatial variation of tip radius results in the spatial variation of the emission currents and non-uniform turn-on voltages. Small changes in the tip radius result in huge changes in the current density because of the exponential dependence of the emitted current on the bias voltage, as described by the Fowler-Nordheim theory. If the emitters are ballasted, the spatial non-uniformity can then be substantially decreased. Furthermore, ballasting individual emitters prevents destructive emission from the sharper tips allowing higher overall current emission because of the inclusion of duller tips. Ballasting also results in more reliable operation. The use of large resistors in series with the field emitters is an unattractive ballasting approach because of the resulting low emission currents and power dissipation in the resistors. A better approach for ballasting field emitters is the use of un-gated field effect transistors that effectively provide high dynamic resistance with large saturation currents. In the past our research group demonstrated the use of a MOSFET to ballast the emission of electrons from silicon tips [1]. We plan to implement vertical un-gated transistors in series to the field emitters to obtain spatial uniformity in the current emission and I-V characteristics of the array [2]. The ballast structure is an n-doped, single-crystal silicon column, patterned using Deep Reactive Etching, and thinned using wet oxidation. Figure 2 shows a cross section of the un-gated transistors consisting of a 1-million elements in 1 cm^2. The field emitters are formed on top of the columns. Current efforts focus on device testing.



▲ Figure 1: A) An isolated 4 μm-tall CNF on top of a 100 μm-tall silicon column; B) Zoom of the CNF tip –tip diameter equal to 36 nm; C) Field of silicon tips on top of 100 μm-tall silicon columns; D) Zoom of a silicon tip -tip diameter equal to 35 nm.



▲ Figure 2: A 1000×1000 array of 100-μm-tall, 1-μm-wide silicon columns, spaced 10 μm. The columns are un-gated transistors that control the current that the tips field-emit.

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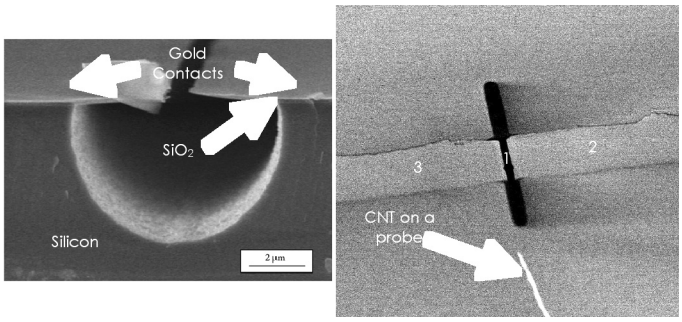
Nanoelectromechanical Switches and Memories

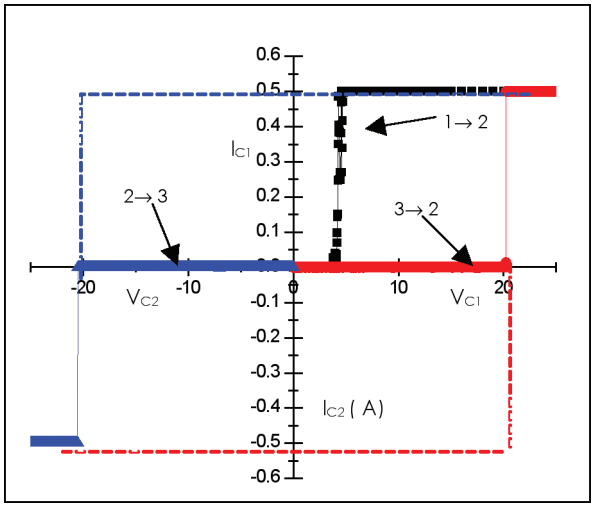
K.M. Milaninia, M.A. Baldo
Sponsorship: SRC/FCRP MSD, ISN

The ability to change shape is a compelling attraction of molecular semiconductors. Compared to rigid inorganic materials, molecules are soft and malleable, and their conformational changes are essential to the functionality of biological systems. Applications of nano-electro-mechanical (NEM) molecular devices include memories and transistors: Information can be stored in the conformation of molecules, potentially leading to very high density memories, and molecular transistors that change shape under bias could exhibit sub-threshold slopes of << 60 mV/decade [1]. Indeed, as an example of the potential of NEMs, voltage-gated ion channels possess sub-threshold slopes of approximately 15 mV/decade [2].

Although many materials are available for NEM applications, carbon nanotubes exhibit low resistance and good mechanical properties. In this project, we are constructing an NEM testbed. The proposed design for our relay is shown in Figure 1. Nanotubes are directly grown at the bottom of an electron-beam defined trench etched in Si. Leaving tube growth to the final step gives us better control of the nanotube and removes the need for additional steps that are required for the removal of surfactants and organics from the surface of the nanotubes. Because the nanotubes are vertically oriented, we are able to take advantage of the smallest size feature of the carbon nanotube, its diameter, which enables us to create dense arrays of relays for applications such as memory or logic devices. The vertical orientation allows NEM structures with very large aspect ratios. Theoretical results [3] have shown that increasing the aspect ratio of a carbon nanotube reduces the voltage needed to pull in the nanotube, thereby reducing the power consumption. Furthermore, because of the ability to easily functionalize the surface of nanotubes, we can functionalize the tube with multiple charges to lower the pull-in voltage even further.



▲ Figure 1: Testing is performed by introducing a probe- mounted CNT in between two gold contacts on silicon and then sweeping it from the center position (1), to the right contact (2), and subsequently to the third contact (3), and then back.



▲ Figure 2: An I-V of the device being switched from state 1→2 by applying a bias between Contact 1 and CNT, then switched from state 2→3 by applying a bias between Contact 2 and CNT, and finally switched from state 3→2 by applying a bias between Contact 1 and CNT.

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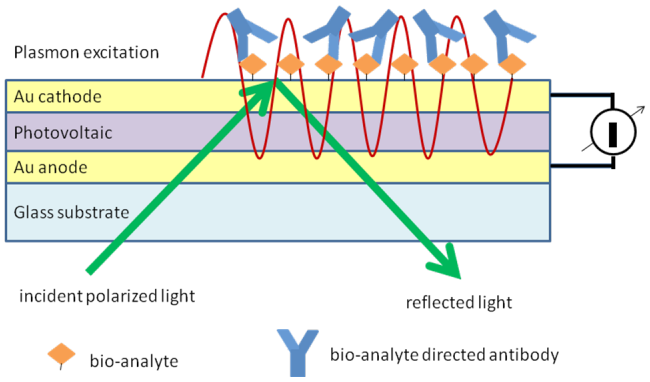
Exciton Coupled Surface Plasmon Resonance Biosensor

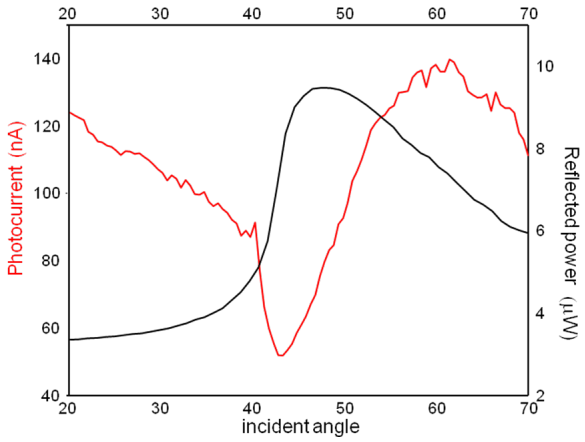
M. Bora, M.A. Baldo
Sponsorship: ISN

The development of portable and cost-effective biological sensors promises benefits to medical care, pharmaceutical testing, and the detection of biological warfare agents. Electronic devices are compact and readily integrated into microfluidic substrates, making them a promising alternative to today's bio-detection requirements. Our sensor design aims to exploit the sensitivity of surface plasmon resonance (SPR). Unlike conventional SPR sensors, the plasmon is detected in the near field using a thin film organic photovoltaic (PV). High absorption coefficients make organic semiconductors ideal candidates for the detection of surface plasmons. Organic materials are also easily deposited on microfluidics, enabling use of these devices outside the laboratory environment in a convenient portable package.

In the initial demonstration, plasmon modes are excited in the top surface of the gold cathode by a p-polarized laser beam, when the horizontal component of the light wavevector matches the plasmon wavevector [1]. The plasmon is absorbed by the organic semiconductor and split into holes and electrons at the interface between the donor and acceptor layers composing the PV cell (Figure 1). The plasmon resonance measured indirectly as reflected power and photocurrent (Figure 2) has a strong angular location dependence on the adjacent layer's dielectric constant that is altered upon binding of bio-molecular species. The steep slope of the resonance enables sensitive detection as well as measurement of kinetic parameters of the binding event.



▲ Figure 1: Device structure for biosensor. An organic photovoltaic cell converts the plasmon excitation resonance into photocurrent, resulting in direct probing of the environment above the top surface of the gold cathode.



▲ Figure 2: Plasmon resonance conversion to photocurrent. A dip in reflectivity above the total internal reflection angle of 43° corresponds to a proportional increase in photocurrent.

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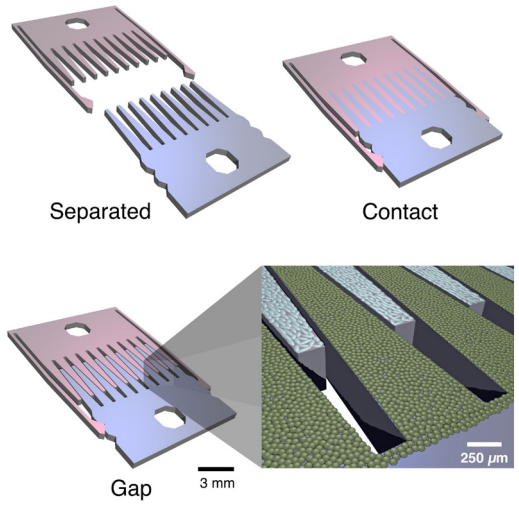
Micromechanical Substrates for Reconfigurable Cell Culture

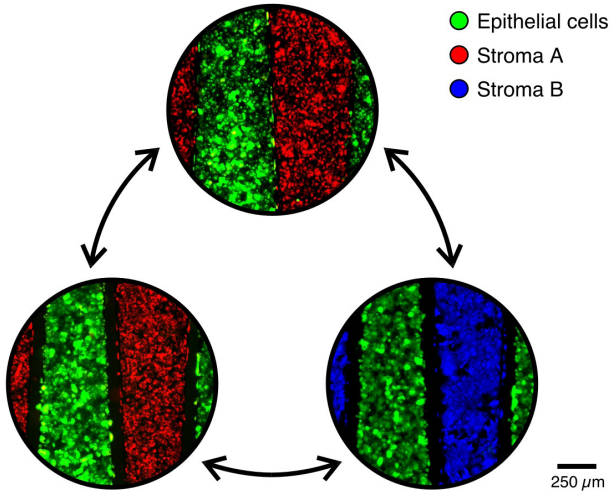
E. Hui, S.N. Bhatia
Sponsorship: NIH NIDDK

We have previously demonstrated the use of microfabricated cell culture substrates (Figure 1) to implement reconfigurable cell culture (Figure 2) [1]. Specifically, we studied interactions between liver hepatocytes and supportive stromal cells. We found that preservation of liver-specific function depended on signaling from the stroma. Specifically, signaling both through direct contact and through diffusible secreted factors was important. However, while the secreted factors needed to be maintained for the entire duration of culture (2 weeks), direct contact was required only for an 18-hour period early in culture. In addition, the secreted factors were found to have a limited effective range of less than 400 μm. Through FEM diffusion modeling, we showed that a half-life on the order of hours would result in such short-range signaling.

Currently, we are exploring the use of this platform in a variety of applications including identification of the signaling factors in hepatocyte co-culture, stabilizing liver endothelial cells in culture, toxicity models for drug testing, preconditioning of hepatocytes prior to encapsulation in a 3D gel, and patterning cells directly on the combs to study contact signaling mechanisms.



▲ Figure 1: Micromechanical substrate is composed of two parts that may be locked together with the fingers in contact or separated by a narrow gap of 80 μm. Switching between these states modulates interactions between cells adhered to the top surface of the fingers.



▲ Figure 2: Fluorescent microscopy of dyed cells on the comb substrates, illustrating the various manipulations possible. Cell populations can be brought into and out of contact with each other. A single population can also be swapped out and replaced.

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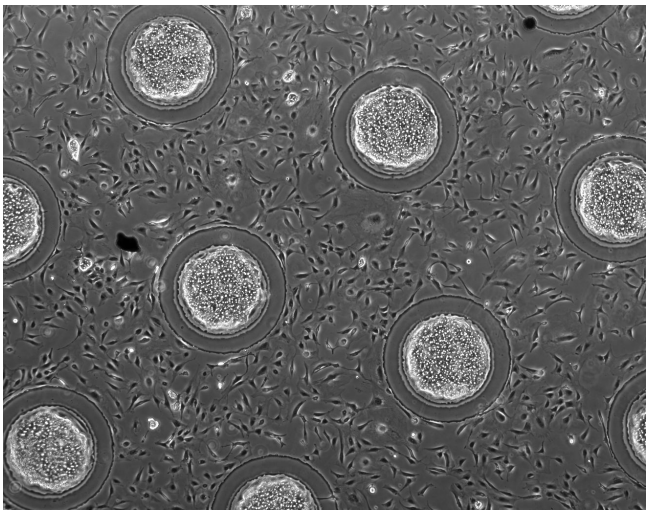
Aligned Multimask Patterning of Biomolecules and Cells

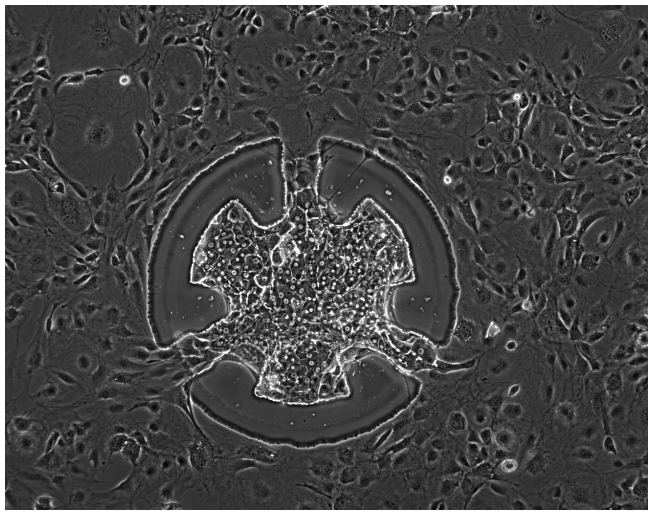
E. Hui, S.N. Bhatia
Sponsorship: NIH NIDDK

Surface engineering of cell culture substrates has developed into a powerful tool for controlling multicellular organization at the micrometer scale. This new capability has brought valuable insight into the biological mechanisms by which the cellular microenvironment determines cell fate and function. However, studies requiring more complex tissue structures have been hindered by limitations in surface patterning. Typically, molecules that mediate cell attachment are patterned against a non-adhesive background, allowing arrays of a single cell type to be formed with control of cell positioning and relative spacing. Alternatively, patterns composed of two different adhesive regions can be employed to form patterned co-cultures of two different cell types, as long as one cell type selectively attaches to a specific region. However, there have been a few examples where multiple attachment chemistries have been successfully combined with non-adhesive surfaces in a multicomponent pattern. This has prevented the realization of configurations in which cell-cell contact and spacing between *different* cell types are controlled.

The use of photolithography with multiple aligned masks is well established for generalized multicomponent patterning, but it is often too harsh for biomolecules. We report a two-mask photolithographic process that is tuned to preserve bioactivity in patterns composed of covalently coupled polyethylene glycol (PEG), adsorbed extracellular matrix protein (e.g., collagen I), and adsorbed serum proteins (e.g., vitronectin). Thereby, we pattern two cell types—primary hepatocytes and 3T3 fibroblasts—demonstrating control over contact and spacing (20-200 μm) between the two cell types for over one week. This method is applicable to the study of intercellular communication in cell biology and tissue engineering.



▲ Figure 1: Hepatocyte islands isolated from surrounding fibroblast support cells by "moats" of PEG-disilane. The moats prevent contact interactions between the two cell types, while preserving communication via diffusible secreted factors.



▲ Figure 2: A closer view of an alternative configuration. Here, the moat is discontinuous in 3 locations. These "bridges" allow local contact at specific points of the hepatocyte island, while contact remains prevented over the rest of the island.

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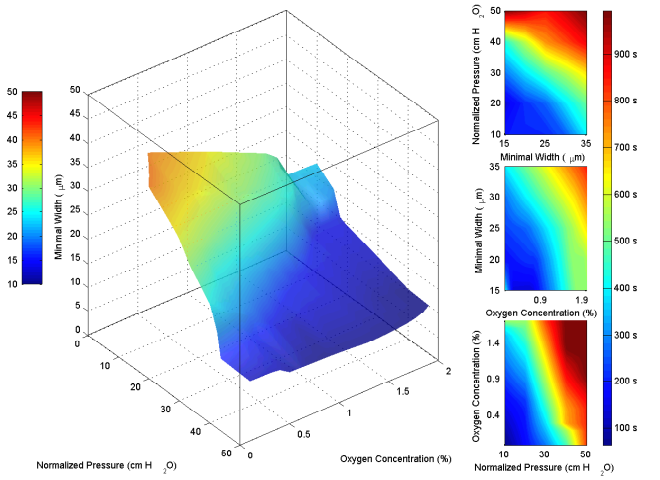
Collective Hydrodynamics and Kinetics of Sickle Cell Vaso-occlusion and Rescue in a Microfluidic Device

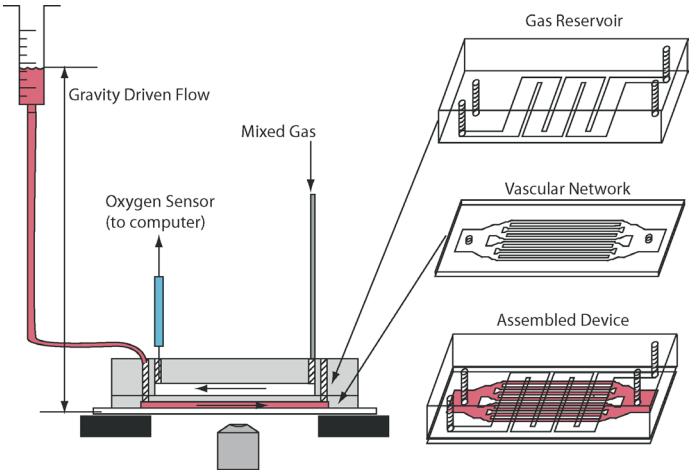
D.T. Eddington, J.M. Higgins, L. Mahadevan, S.N. Bhatia
Sponsorship: NIH

The pathophysiology of sickle cell disease, the first to be implicated with a genetic origin, is complicated by the multi-scale nature of the processes that link the molecular genotype to the organismal phenotype. Here, we show that it is possible to evoke, control and inhibit the vaso-occlusive crisis event in sickle cell disease using an artificial microfluidic environment. We use a combination of geometric, physical, chemical and biological means to quantify the phase space for the onset of a jamming crisis, as well as its dissolution, as shown in Figure 1.

The microfluidic chip designed to independently vary the various parameters that control the onset of vaso-occlusion in a sickle cell crisis is shown in Figure 2. This device allows us to dissect and probe the hierarchical dynamics of this multi-scale process by manipulating the geometrical, physical, chemical and biological determinants of the process. The chip consists of a series of bifurcating channels of varying diameters that grossly mimics the geometry of vasculature. By controlling the physical pressure gradient across the chip, we can vary the kinetic time scale for transit of red blood cells. The channels are separated from a gas reservoir by a thin gas-permeable polydimethylsiloxane (PDMS) membrane. As the geometries are microscopic, gas diffusion is rapid and the oxygen concentration in the microchannels is governed by the concentration in the gas reservoir. By changing the mixture of this reservoir, we control oxygen concentrations in the channels and hence the onset of microscopic hemoglobin polymerization. By using blood with varying concentrations of HbS and different hematocrits, we can mimic the variability among individuals. This device was used to study the phase space of jamming governed by pressure, channel dimensions and oxygen concentration as shown in Figure 1. Our experimental study integrates the dynamics of collective processes at the molecular, polymer, cellular and multi-cellular level; lays the foundation for a quantitative understanding of the rate limiting processes; provides a potential tool for optimizing and individualizing treatment; and serves as a bench test for dynamical drugs.



▲ Figure 1: Phase space of vaso-occlusion. The colored surface represents a fitted hypersurface in 4-dimensional space: width, pressure, oxygen concentration, and occlusion time. The isosurface was computed from 43 data points using Delaunay triangulation. All points on the hypersurface correspond to triples of height, pressure, and oxygen concentration where the fitted time to occlusion was 500 seconds. The color of each point on the surface characterizes the minimal width in the device and is redundant with the point's vertical (width) coordinate. The filled contour plots represent slices through the fitted volume at specific planes (top: oxygen concentration = 0.5%, middle: normalized pressure = 20 cm H_20, bottom: minimal width = 25 μm). This phase space describes the behavior of patients whose samples contained hemoglobin S concentrations of at least 65% (mean 86%, standard deviation 6.7%).



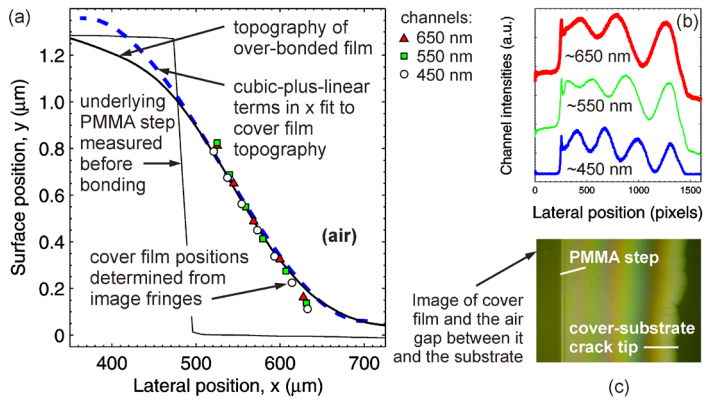
▲ Figure 2: Fabrication and schematic of the device. The oxygen channels and vascular network were fabricated in separate steps. After removal of the device from the SU8 mold master, holes were cored and networks were bonded via oxygen plasma activation and then attached to a glass slide. The widest cross section in the vascular network on the left and right of the device is 4 mm x 12 μm. The vascular network then bifurcates, maintaining a roughly equal cross-sectional area. An open 5 mL syringe was connected to the device and raised and lowered to increase or decrease the flow rates through the device. The gas channels were connected to two rotometers regulating the ratio of 0% and 10% oxygen in the gas mixture that was fed into the device. The outlet of the gas network had an oxygen sensor to validate the oxygen concentration in the microchannels.

Plasma-activated Inter-layer Bonding of Thermoplastics for Micro- and Nano-fluidic Manufacturing

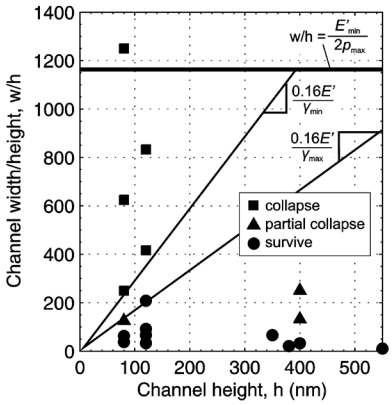
H.K. Taylor, M. Dirckx, D.S. Boning
Sponsorship: Singapore-MIT Alliance

Plasma-activated polymer–polymer bonding is a promising way of encapsulating micro- and nano-fluidic channels across large substrate areas, without the substantial distortion of channel geometries that can plague thermally- and solvent-assisted bonding. The process involves treating the surfaces to be bonded with an oxygen or air plasma, and then pressing the surfaces together to allow an irreversible chemical bond to form [1]. A convenient method is desired for measuring the toughness of such a bonded interface. Simple crack-opening tests (whereby a blade prizes apart the two bonded layers and the length of the interlayer crack determines the bond toughness [2]) are clumsy and hard to automate. We propose that built-in microscopic crack-opening test sites be distributed across manufactured substrates [3]. At each test site, a polymeric film bonded over a step in the substrate would peel back from the step after bonding, by a distance depending on the toughness of the bond. The presence of a wedge-shaped air gap between the covering film and the substrate leads to visible interference fringes, the spacing of which can be used to extract the bond strength (Figure 1). Arrays of these *in situ* cracks might be imaged without removing the substrate from a production line and would allow us to monitor both substrate-to-substrate and cross-substrate bond toughness variation.

Bond toughness and polymer layers' surface energies are of particular relevance in planning the fabrication of very shallow fluidic channels whose widths, w, are much larger than their depths, h. The risk of channels' collapsing during fabrication must be controlled. For channels with $h \sim 1$ μm or less that are fabricated with thermoplastics, we expect collapsing to occur through local deformation of the surrounding material rather than through plate-like bending of the cover plate [4]. Our analysis suggests that the pressure applied during bonding, together with the polymer–polymer interface energies that exist before and after plasma-activated bonding, will delineate, on a w/h against h plot, regions in which collapsing will and will not occur. We have demonstrated nanochannels fabricated from polymethylmethacrylate (PMMA) that are 80 nm deep and 10 μm wide and other channels that are 110 nm deep and 20 μm wide (Figure 2).



▲ Figure 1: Results from a prototype bond toughness measurement feature. The topography of the film covering one side of a PMMA ridge (a) is determined with white-light interferometry (black line); a cubic-plus-linear function of the lateral position has been fit to the film topography, showing good agreement with an analytical small-deflections model of the cover plate. Symbols indicate the varying height of the air gap between substrate and cover film, obtained by interpreting a color interference image of the sample (c). The average red, green, and blue intensities present in the image are plotted (b) above the image.



▲ Figure 2: The PMMA nanochannel fabrication results. Our analysis suggests that provided $w/h < E'/2p$ (where E' is the plate modulus and p is the pressure applied during bonding), channel collapsing is determined by the channel dimensions, the material's stiffness, and the surface energy change γ that occurs when a polymer–polymer interface is *reversibly* formed or broken. Possible lines separating regions of collapsed and intact channels are suggested; many more channel sizes need to be tested to map the w/h–h space confidently.

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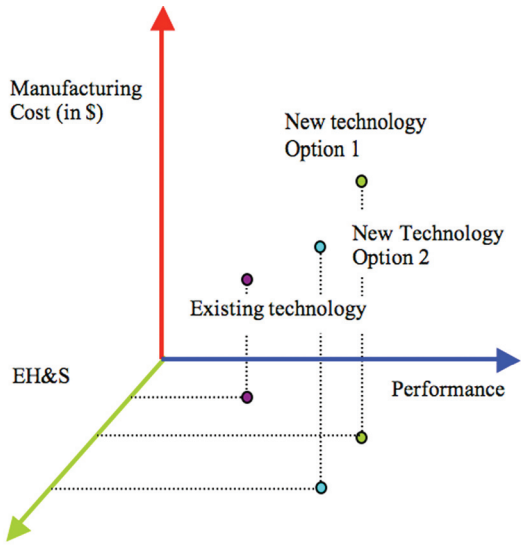
Environmentally Benign Manufacturing of Three-dimensional Integrated Circuits

A. Somani, D.S. Boning
Sponsorship: SRC/SEMATECH Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

Along with scaling down in size, novel materials have been introduced into the semiconductor industry to enable continued improvements in performance and cost as predicted by Moore's law. It has become important now more than ever to include an environmental impact evaluation of future technologies, before they are introduced into manufacturing, in order to identify potentially environmentally harmful materials or processes and understand their implications, costs, and mitigation requirements. In this project we introduce a methodology to compare alternative options on the environmental axis, along with the cost and performance axes, in order to create environmentally aware and benign technologies. This methodology also helps to identify potential performance and cost issues in novel technologies by taking a transparent and bottoms-up assessment approach.

This methodology is applied to the evaluation of the MIT 3D IC technology in comparison to a standard CMOS 2D IC approach. Both options are compared on all three axes–performance, cost, and environmental impact. The "handle wafer" unit process in the existing 3D IC technology, which is a crucial process for back-to-face integration, is found to have a large environmental impact because of its use of thick metal sacrificial layers and high-energy consumption. We explore three different handle wafer options: between-die channel, oxide release layer, and alternative low-temperature permanent bonding. The first two approaches use a chemical handle wafer-release mechanism while the third explores solid liquid inter-diffusion (SLID) bonding using copper-indium at 200°C. Preliminary results for copper-indium bonding indicate that a sub-micron thick multi-layer copper-indium stack, when bonded to a 300-nm-thick copper film, results in large voids in the bonding interface primarily due to rough as-deposited films. Finally, we conduct an overall assessment of these and other proposed handle wafer technologies. The overall assessment shows that none but the oxide release layer approach appears promising; however, each process option has its strengths and weaknesses, which need to be understood and pursued accordingly.



▲ Figure 1: Three axes to manufacturing: Cost, performance and EH&S impact. Emerging silicon technologies can be mapped into three-dimensions for environmentally conscious technologies.

	Al Release Layer	Between-die Channel	Smart Cut	Oxide Release Layer
Performance	✗	✓	✓	○
Cost	✗	○	✗	✓
Environmental Impact	✗	✗	✓	○

▲ Table 1: Demonstration of integrated assessment of handle wafer options. A ✓ indicates acceptable, and a ○ indicates further work is required, while ✗ indicates that an area of high concern. The oxide release layer approach has no ✗, which makes it most appropriate.

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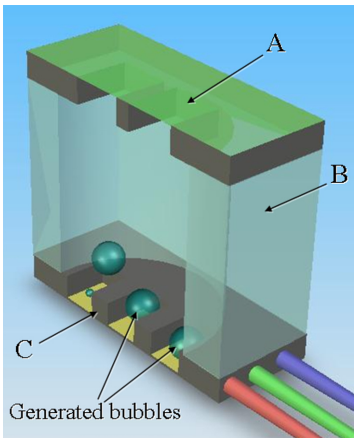
An Implantable MEMS Drug-delivery Device

H.L. Ho Duc, N. Elman, M.J. Cima
Sponsorship: ARO, ISN

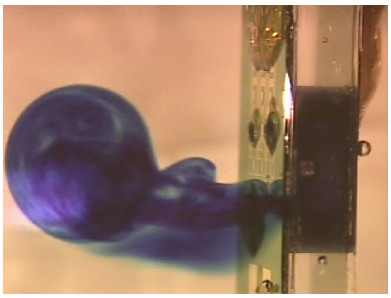
A novel drug-delivery system based on MEMS technology is being developed. This implantable microchip is capable of delivering vasopressin, a known vasoconstrictor that can prevent or delay death by hemorrhagic shock [1]. The device is specially tailored to treat hemorrhagic shock in ambulatory settings and is intended for *in vivo* use as a micro-implant in the peritoneum for people in high-risk situations.

The device has a modular design and is composed of three layers (shown schematically in Figure 1): a large reservoir layer, where the drug solution is stored; a membrane layer from where the drug is ejected; and a bubble-generating layer, where bubbles are formed. The reservoir layer is defined by drilling through a Pyrex 7740 wafer with a diamond bit. Wafer thickness and hole diameter can be modified to change reservoir capacity. The membrane layer is composed of silicon nitride membranes covering through-holes etched by DRIE into a silicon substrate. Thin gold fuses can be patterned on the membranes to detect ruptures, which then shows as an open circuit. The bubble-generating layer is defined by micro-resistors, which can quickly and locally heat the contained fluid to generate bubbles. The pressure exerted by these bubbles causes rupture of the silicon nitride membranes and forces the contained solution out of the device.

In vitro operation of the device has been demonstrated, as shown in Figure 2. Further developments of this device include reduction of power consumption during activation, wireless activation, and adaptation of the device for a pen-size, transdermal delivery system. We believe that the ramifications of this MEMS-based drug delivery system can be useful for a vast number of medical applications.



▲ Figure 1: Schematic representation of drug delivery system with (A) membrane layer, (B) reservoir layer containing the drug solution and (C) bubble-generating layer.



▲ Figure 2: *In vitro* release of methylene blue solution from the drug delivery system.

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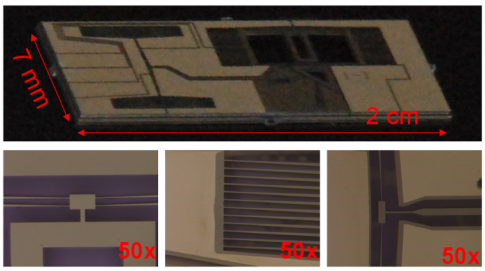
High Speed Three-dimensional Scanner for *in vivo* Non-invasive Optical Biopsy using Two-photon Microscopy

S.-C. Chen, H. Choi, P.T. So, M.L. Culpepper
Sponsorship: NIH

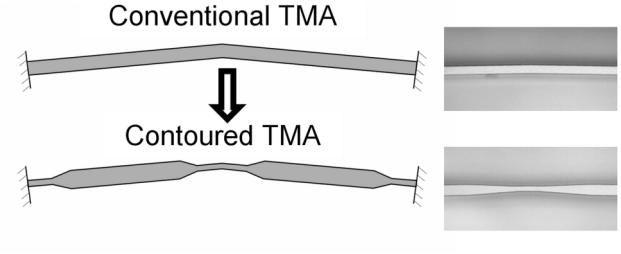
We have recently demonstrated the modeling, design, and microfabrication process of a millimeter-scale, high-speed endoscopic scanner that is to be integrated at the distal end of an endomicroscope [1]. The scanner system consists of (1) an active Silicon optical bench (SOB), as shown in Figure 1, which constrains, aligns, and thermally actuates (1) mm-size optics (GRIN lens and prism) at 5 Hz and (2) a slim fiber resonator that excites the double-clad photonic bandgap fiber at ~1 kHz. The scanner system has a 7-millimeter device envelope with a range of 100 micrometers in X, Y and Z. The design of a two-photon endoscope requires scanning of focused light to create tissue images, and scanning actuator technology still proves to be a bottleneck for practical endoscope design. The performance (force-speed-stroke) criteria for the prototype endomicroscope design are generated based on clinical needs. The strict force, speed, and stroke requirements (~10 mN, 1 kHz, and 100 μm) call for a new method for actuation. The low voltage requirement for future *in vivo* examination/operation makes a new class of thermomechanical actuators (TMAs) a suitable candidate among other micro-actuation technologies.

The two-photon imaging technique requires scanning of focused light to create tissue images. The endoscopic scanner may enable the design and construction of a miniaturized two-photon microscopic system to image the surface and sub-surface cells (up to 200 microns depth) of internal tissues with sub-cellular resolution. The two-photon endomicroscope is designed to perform non-invasive, *in vivo*, optical biopsy, which has numerous benefits over excisional biopsy. For example, non-invasive optical screening may decrease the number of excision biopsies required, and optical biopsy can provide more informed selection of excisional biopsy sites, minimizing incorrect diagnosis due to random sampling. This is useful for detecting cancer at an early stage among other diseases.

The chevron TMAs on the SOB are optimized through the geometric contouring method [2] to provide enhanced force, displacement and reduced power consumption compared to common chevron actuators. This also allows the TMAs to be operated at lower temperature and thus makes the TMAs more suitable for precision actuation. Figure 2 presents an example of a contoured chevron TMA. Early models and experiments of the contour shaping method have confirmed that the maximum achievable thermal strain of a driving beam may be increased by 29%, the actuator stroke may be increased by a factor of 3 or more, and identical force or displacement characteristics may be achieved with 90% reduction in power. A new high-speed pulsing technique has also been investigated recently; it enhances the dynamic performance of the contoured TMAs [3]. Preliminary simulation results indicate a 12% bandwidth increase, 30% stroke enhancement, and 70% power reduction. This technique, together with the geometric contouring method for TMAs, may potentially increase the bandwidth of the endoscopic scanner by a factor of 10 and therefore meet the functional requirements for a two-photon scanning endomicroscope.



▲ Figure 1: Silicon optical bench with integrated contoured TMAs and flexural bearings that generates linear and rotary motions.



▲ Figure 2: Example of a conventional and contoured chevron TMAs.

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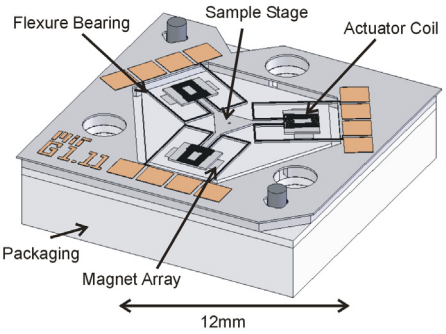
Electromagnetically-driven Meso-scale Nanopositioners for Nano-scale Manufacturing and Measurement

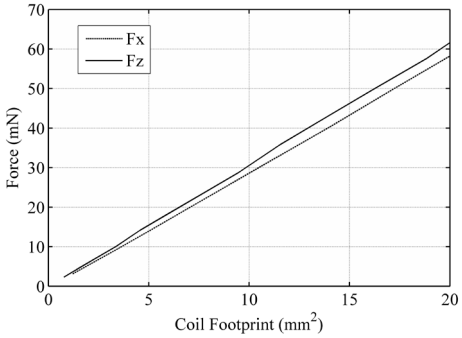
D. Golda, M.L. Culpepper
Sponsorship: NSF, NIH

Nanopositioners – be they nano-, micro-, or macro-scale in physical size – enable us to move large or small parts with nanometer-level or better precision. They therefore set the limits on our ability to measure, understand, manipulate, and affect physical systems. Six-axis small-scale nanopositioners enable a combination of faster speed and better resolution. They are therefore important in scientific and commercial applications where speed and small-dimensions are important: biological sciences, data storage and nanomanufacturing equipment and instruments [1-4]. Emerging applications in these fields will benefit from portable, multi-axis nanopositioners that are capable of nanometer-level positioning over tens-of-microns at speeds of hundreds to thousands of Hertz. Toward this end, our work aims to create a meso-scale, high-speed, six-axis nanopositioner.

The nanopositioner is designed to operate with a range-of-motion of larger than 10 micrometers in the X-, Y- and Z- directions, possess a natural frequency of 1 kHz, and exhibit better-than-10-nm resolution. The nanopositioning system, shown in Figure 1, is composed of three sets of micro-actuators. Within each set, micro-coils are suspended above a linear array of 1 mm^3 permanent magnets via a silicon flexure system [5]. Each actuator is composed of two independent coils that apply in-plane and out-of-plane forces to the flexure. The actuator inputs are combined to control the stage position in six axes. Figure 2, which shows the actuator's force output capability vs. coil footprint, was generated using a numerical model. The micro-coils consist of two stacked copper micro-coils that are electrically isolated by a layer of silicon dioxide. They are created by electroplating copper within silicon and photoresist molds. The flexures are etched using deep reactive-ion etching. The system will be applied to the high-speed and precise positioning of small parts such as probes and thin-films. The system is scheduled to be integrated into a bench-top scanning-probe microscope and within a nano-electro-discharge machining station [4].



▲ Figure 1: Solid model representation of the proposed meso-scale nanopositioner that shows the permanent magnets, microfabricated silicon flexures, and copper coils.



▲ Figure 2: Maximum in-plane (Fx) and out-of-plane (Fz) actuator forces vs. micro-coil footprint. The micro-coils used in the nanopositioner are designed with a footprint of 4 mm^2, resulting in a maximum output force of 10 mN.

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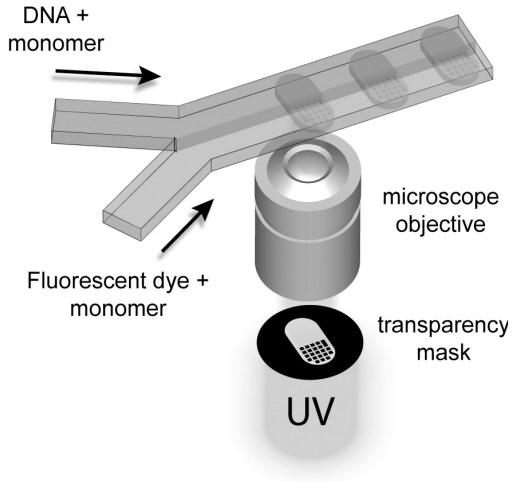
Barcoded Microparticles for Multiplexed Detection

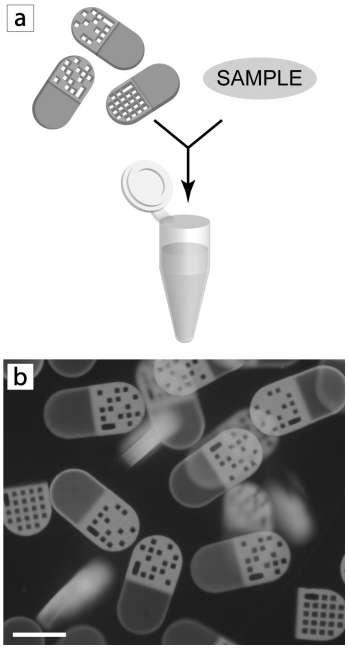
D. Pregibon, M. Toner, P.S. Doyle
Sponsorship: NSF

The detection of multiple targets in a single sample is important for many applications, including medical diagnostics, genotyping, and drug discovery. The current approaches to multiplexing, such as planar arrays (such as DNA microarrays) and suspension (particle-based) arrays, require expensive or cumbersome means of encoding, decoding, or functionalizing substrates. Currently, commercially available approaches for multiplexed analysis are cost-prohibitive for high sample throughput, low-cost applications such as bedside diagnostics.

We have developed a method [1], based on multifunctional barcoded particles, for the sensitive and accurate multiplexed detection of biomolecules. Our method is unique in that (1) we can fabricate, encode, and functionalize particles in a single step, (2) the particles are composed of poly(ethylene glycol) hydrogel to increase both sensitivity and specificity, and (3) only a single fluorescent wavelength is required to decode the particles and quantify the corresponding targets. Using an efficient one-step method based on continuous-flow lithography, we synthesize microparticles with multiple functional regions (Figure 1). Each particle bears a fluorescent dot-pattern barcode (capable of providing over a million unique codes) to identify the target(s) it is looking for and one or more spatially separated regions containing a probe where those targets can bind and be detected via fluorescence. In this way, particles from a library can be mixed and incubated in a single sample to simultaneously detect many targets, such as DNA oligomers (Figure 2). The detection of targets is not only sensitive but also extremely specific due to the porous and bio-inert nature of the hydrogel structure that allows target molecules to diffuse and bind deep into the transparent particle surfaces.



▲ Figure 1: Schematic of one-step particle synthesis in a microfluidic device. Two monomer streams (one with a DNA probe and the other with a fluorescent dye) are flowed adjacently along a channel where they are repeatedly hit with burst of UV light shone through a microscope objective.



▲ Figure 2: (a) Schematic of multiplexed sample analysis. Particles (with unique barcodes corresponding to their target) are mixed and incubated in a single sample. (b) Fluorescence image of particles after incubation with DNA oligomers targets. Positive detection is indicated by fluorescence in the probe-region of the particles. Scalebar = 100 µm.

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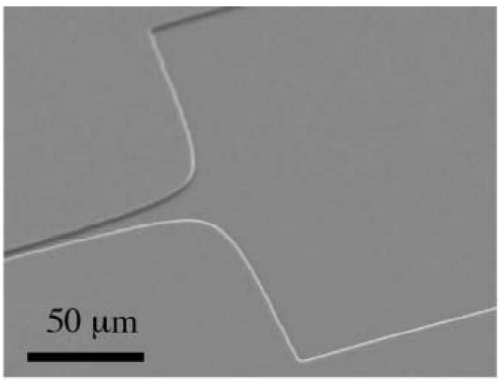
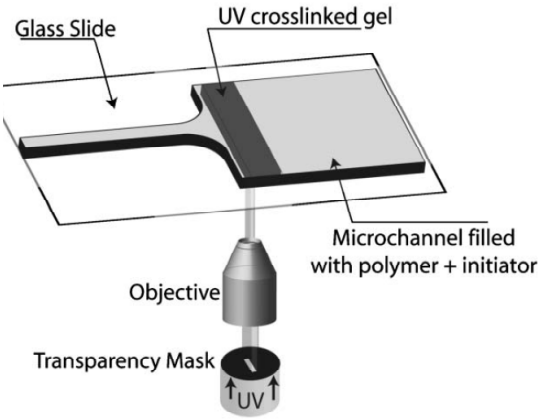
Single-molecule DNA Mapping in a Fluidic Device

J. Tang, G. Randall, P.S. Doyle
Sponsorship: NSF

The ability to controllably and continuously stretch large DNA molecules in a microfluidic format is important for gene-mapping technologies such as Direct Linear Analysis (DLA). We have recently shown that electric field gradients can be readily generated in a microfluidic device and the resulting field is purely elongational. We have performed a single-molecule fluorescence microscopy analysis of T4 DNA (169 kbp), stretching in the electric field gradients in a hyperbolic contraction microchannel. In addition, we are able to selectively pattern a crosslinked gel anywhere inside the microchannel. With an applied electric field, DNA molecules are forced to reptate through the gel and they stretch moderately as they exit the gel. By placing a gel immediately in front of the hyperbolic contraction, we bypass "molecular individualism" and achieve highly uniform and complete stretching of T4 DNA. This device offers a new method to efficiently stretch DNA for single-molecule mapping studies.



▲ Figure 1: An SEM image of a PDMS hyperbolic channel.



▲ Figure 2: Schematic diagram of the method used to create a gel filter just before the hyperbolic contraction.

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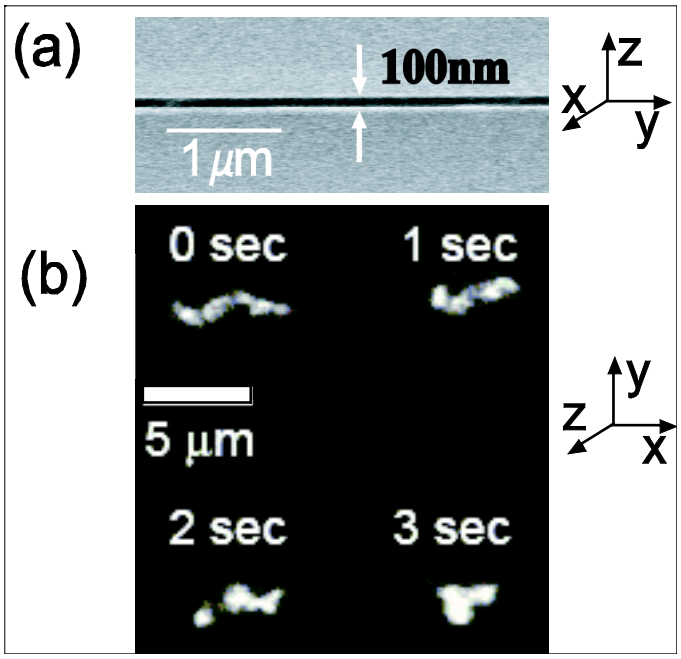
DNA Dynamics in Nanofluidic Devices

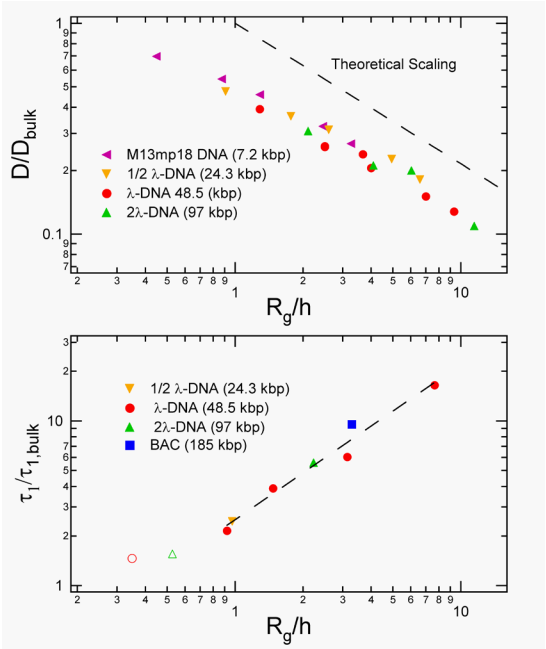
A. Balducci, C.-C. Hsieh, P.S. Doyle

In dilute polymer solutions, the shape, motion, dynamic response, and solvent-interaction (HI) of single polymer molecules change when geometric constraints reach the length scales of the equilibrium polymer conformation. Our study seeks to understand these changes using double-stranded DNA as a model polymer and to utilize these confinement effects to tune the dynamic response of single molecules. This ability is useful in processes that rely on controlling the conformation of a biomolecule for analysis [1] or in the manipulation of molecules for separations and/or reactions

Our experiments [2-3] use thermally-bonded pyrex channels with heights ranging from 75 to 500 nm and widths of 150 μm. The Brownian motion of stained DNA molecules is observed using epi-fluorescence microscopy. By following the time evolution of the center-of-mass and orientation of single molecules, we can obtain the diffusion coefficient (D) and longest relaxation time (τ_1) of the polymer independently. We find that scalings with molecular weight of both D and τ_1 agree with a free-draining polymer model, indicating that, in contrast to bulk solution, HI is not important in slit confinement at length scales comparable to the size of the molecule. We find that the relaxation time of the polymer increases with confinement, which promises easier manipulation of DNA conformations. Our results in well-defined nanofluidic devices may also provide insight into polymer behavior in the less-controlled confinement that occurs in concentrated polymer solutions. We are currently working to stretch DNA in confinement and to study the effects of confinement far from the equilibrium conformation of the polymer



▲ Figure 1: (a) An SEM micrograph of a 100-nm-tall channel. (b) Time-series images of a single 97-kbp DNA molecule undergoing Brownian motion in a 500-nm-tall channel.



▲ Figure 2: Variables D and τ_1 normalized by their bulk values versus a measure of confinement (equilibrium radius divided by gap height) for DNA molecules of varying molecular weight.

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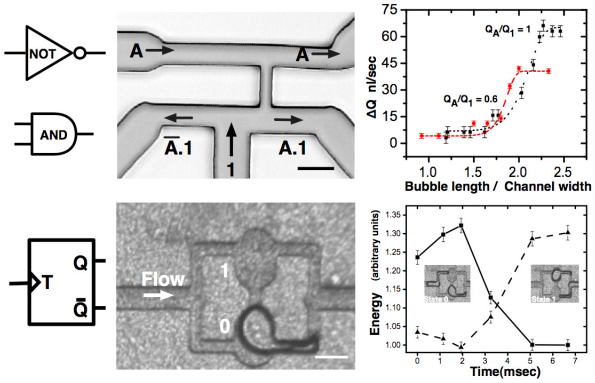
Microfluidic Bubble Logic

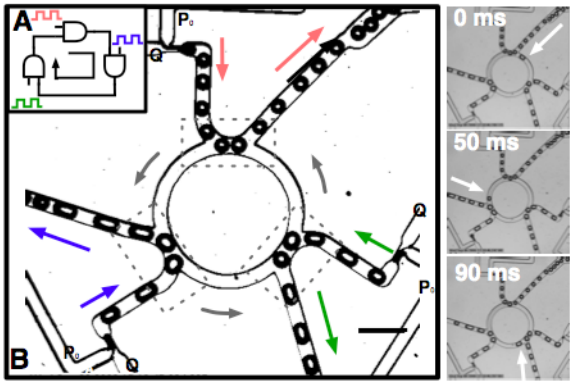
M. Prakash, N. Gershenfeld
Sponsorship: Center for Bits and Atoms

Large-scale microfluidic integration promises to revolutionize the fields of biology and analytical chemistry. The "Lab-on-a-Chip" community has long sought the ability to precisely control very small volumes (nanoliters) of fluid packets . Current mechanisms for fluid routing depend on external control elements with no feedback, limiting scalability and integration. In [1] we describe Bubble logic, an all-fluidic universal logic family implemented in a two-phase microfluidic system. The presence or absence of a drop or a bubble represents a bit of information. Non-linear hydrodynamic interactions of these elements in microfluidic geometries are exploited to build logic gates (AND, NOT), bistable memory (toggle flip-flop), ring oscillators, ripple counters, and synchronizers. This provides an on-chip internal flow control mechanism with all the properties of a digital logic family including gain, bistability, cascadability, feedback and synchronization. Since no external control elements are required, bubble logic can also find applications in diagnostic instrumentation in resource-poor settings, controlled drug delivery or computation in harsh settings.

Previous attempts at an all-fluidic computation mechanism used inertial effects (significant only at high Reynolds numbers) or non-Newtonian fluids (like polymer blends). Bubble logic operates at both low Reynolds and capillary numbers, allowing us to reduce length scales further and thus operate in nanoliter or smaller regimes. Figure 1 depicts device geometries for universal AND-NOT logic gate and a toggle flip-flop. The devices are fabricated using soft-lithography in PDMS bonded to glass. Propagation time for the logic gate and toggle flip-flop is ~10ms. Figure 2 depicts a ring oscillator consisting of three AND gates and a delay line with photomicrographs of the device in operation (recorded by a high speed video camera). We are currently working on integrating bubble logic elements to build high-density, random-access chemical memories.



▲ Figure 1: Universal logic and memory. Top row depicts a universal logic gate (AND and NOT) with a plot depicting gain. Bottom row depicts one bit bistable memory, implemented as a toggle flip-flop with a plot of bistability (surface energy) as a bubble traverses the microfluidic geometry. Scale bar ~100 μm.



▲ Figure 2: Microfluidic ring oscillator depicting cascading and feedback. Top inset depicts the schematic with three microfluidic AND gates connected in a ring configuration. Right column depicts a time series of steady state operation of the oscillator at ~10Hz. Scale bar ~200 μm.

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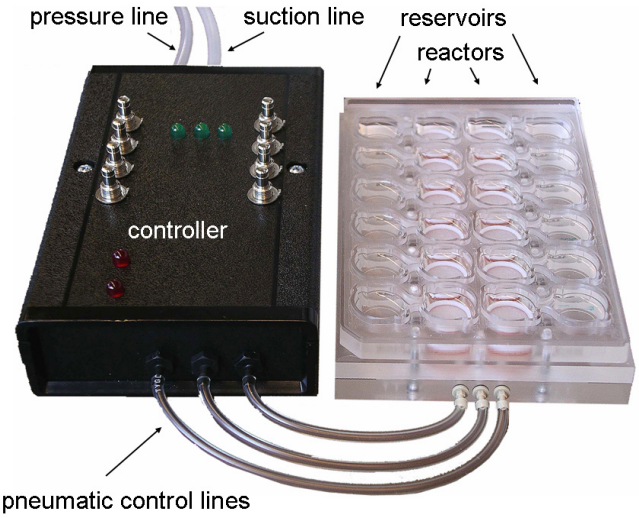
Perfused Multiwell Tissue Culture Plates for Development of Drug and Disease Models

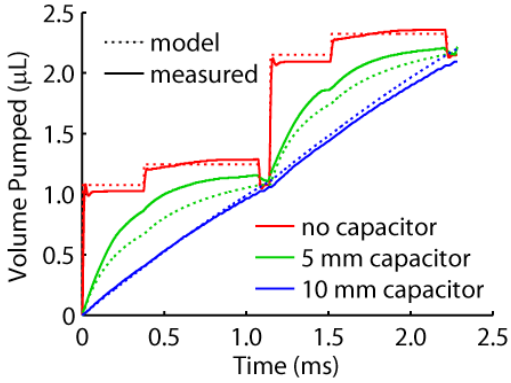
K. Domansky, W. Inman, J. Serdy, B. Owens, S. Karackattu, J.R. Llamas Vidales, R. Littrel, M.H.M. Lim, L. Vineyard, L.G. Griffith
Sponsorship: DuPont-MIT Alliance, Pfizer, Biotechnology Process Engineering Center

A new platform for three-dimensional hepatic tissue engineering has been developed. It is based on the conventional multiwell tissue culture plate format but it allows the tissue to be continuously perfused with cell culture medium [1]. The new capability is achieved by a microfluidic perfusion system that re-circulates cell culture medium between reactors and reservoir (Figure 1). It features a network of microfluidic valves and pumps integrated into the plate [2]. Flow pulsatility is controlled by fluidic capacitors. In order to measure performance of fluidic capacitors, fluid was pumped through a capillary and a high-speed video camera was used to track the end position of the fluid. Figure 2 compares the performance of measured and modeled capacitors. As predicted by the model, the 10-mm capacitor effectively filters fluid pulses and generates a nearly constant flow. Flow with this characteristic is critical during the initial cell attachment time-period.

Phase contrast and fluorescent imaging, measurement of oxygen consumption, accumulation of taurocholic acid, gene expression profiling, and drug metabolism assays are used to characterize the performance of the 3D perfused cultures. Because the new system features a standard multiwell tissue culture plate footprint, it is readily amenable to numerous high-throughput assays compatible with automated technologies commonly used in pharmaceutical development. The system provides a means to conduct assays for toxicology and metabolism and can be used as a model for human diseases such as hepatic disorders, exposure-related pathologies, and cancer.



▲ Figure 1: Photograph of a 12-microbioreactor array with its electro-pneumatic controller. Cell culture medium is re-circulated between the reactor and reservoir wells. All reactor/reservoir pairs are fluidically isolated from each other.



▲ Figure 2: Comparison of measured capacitor performance to the capacitor model for 5- and 10-mm diameter capacitors and a flow rate of 0.05 mL/min.

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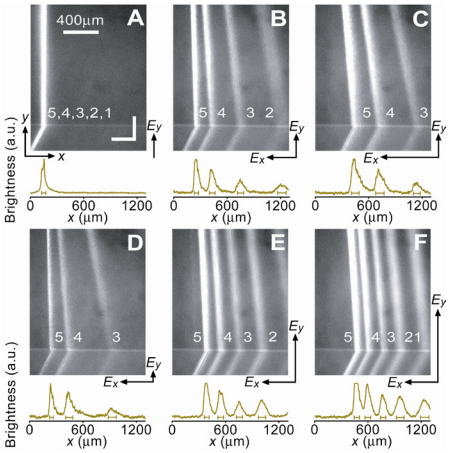
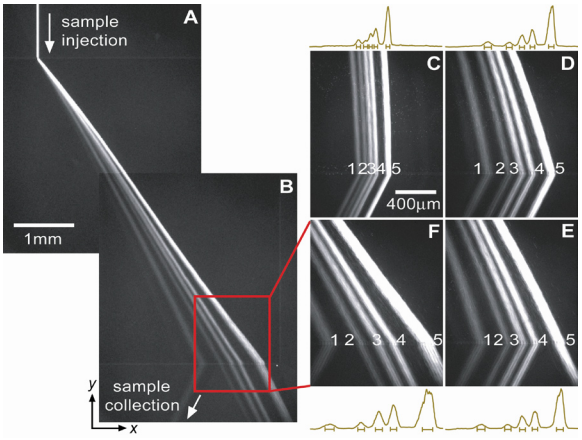
A Patterned Anisotropic Nanofilter Array for Continuous-flow Separation of DNA and Proteins

J. Fu, J. Han
Sponsorship: NIH, NSF, Singapore-MIT Alliance (SMA-II, CE program)

Microfabricated regular sieving structures hold great promise as an alternative to gels to improve biomolecule separation speed and resolution. In contrast to the disordered gel porous network, these regular structures also provide well-defined environments ideal for study of molecular dynamics in confining spaces. However, previous regular sieving structures have been limited for separation of long DNA molecules, and separation of smaller, physiologically-relevant macromolecules, such as proteins, still remains as a challenge. Here we report a microfabricated anisotropic sieving structure consisting of a two-dimensional periodic nanofluidic filter array (an Anisotropic Nanofilter Array, or ANA). The designed structural anisotropy in the ANA causes differently-sized molecules to follow different trajectories, leading to efficient separation. Continuous-flow Ogston sieving-based separation of short DNA and proteins as well as entropic trapping-based separation of long DNA were achieved, thus demonstrating the potential of the ANA as a generic sieving structure for an integrated biomolecule sample preparation and analysis system.



▲ Figure 1: Ogston sieving of the PCR marker through the ANA. For A, only E_y applied and E_y=25 V/cm; for B, E_x=35 V/cm, E_y=25 V/cm; for C, E_x=60 V/cm, E_y=25 V/cm; for D, E_x=35 V/cm, E_y=12.5 V/cm; for E, E_x=35 V/cm, E_y=50 V/cm; for F, E_x=35 V/cm, E_y=75 V/cm. Band assignment: (1) 50-bp; (2) 150-bp; (3) 300-bp; (4) 500-bp; (5) 766-bp.



▲ Figure 2: Entropic trapping of long DNA (the λ DNA–Hind III digest) through the ANA. Fluorescent photographs show separation of λ DNA–Hind III digest with different electric field conditions. In A, B, and F, E_x=185 V/cm and E_y=100 V/cm. In C, E_x=50 V/cm and E_y=100 V/cm. In D, E_x=145 V/cm and E_y=100 V/cm. In E, E_x=170 V/cm and E_y=100 V/cm. Band assignments are 2,322 bp (1), 4,361 bp (2), 6,557 bp (3), 9,416 bp (4), and 23,130 bp (5).

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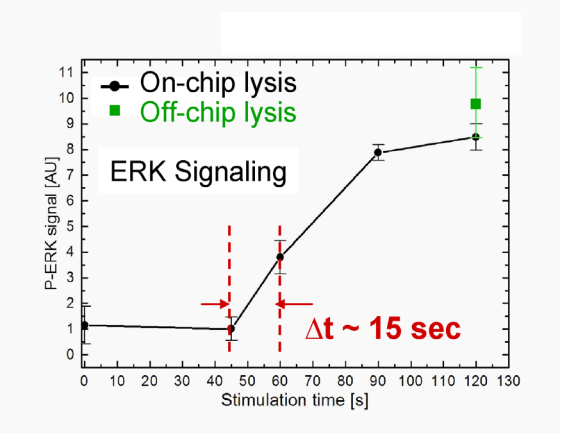
Cell Stimulation, Lysis, and Separation in Microdevices

J. Albrecht, J. El-Ali, S. Gaudet, K.F. Jensen
Sponsorship: NIH

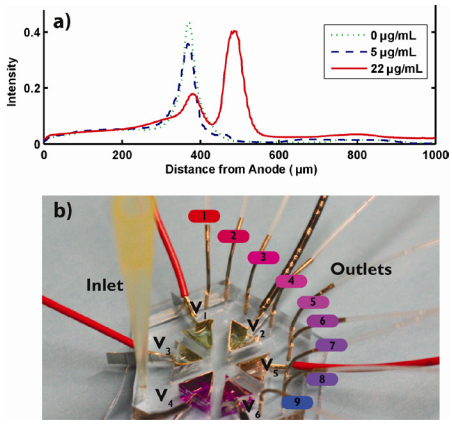
Quantitative data on the dynamics of cell signaling induced by different stimuli requires large sets of self-consistent and dynamic measures of protein activities, concentrations, and states of modification. A typical process flow in these experiments starts with the addition of stimuli to cells (cytokines or growth factors) under controlled conditions of concentration, time, and temperature, followed at various intervals by cell lysis and the preparation of extracts. Microfluidic systems offer the potential to do laborious assays in a reproducible and automated fashion [1].

Figure 1 shows quantification of the stimulation of a T-cell line with antibodies performed in a micro-fluidic device with integrated cell lysis. The device is capable of resolving the very fast kinetics of the cell pathways, with protein activation levels changing 4-fold in less than 15 seconds [2]. The quantification of the lysate is currently performed off-chip using electrophoretic separation. To effectively extract meaningful data from cellular preparations, many current biological assays require similar labor-intensive sample purification steps.

Micro-electrophoretic separators have several important advantages over their conventional counterparts, including shorter separation times, enhanced heat transfer, and the potential to be integrated into other devices on-chip. However, the high voltages required for these separations prohibit using metal electrodes inside the microfluidic channel. A PDMS isoelectric focusing device with polyacrylamide gel walls [3] has been developed to perform rapid separations by using electric fields orthogonal to fluid flow. This device and its variants have been shown to focus organelles, low-molecular-weight dyes, proteins, and protein complexes (Figure 2a) in seconds. Simulations have driven the development of improved device configurations, such as tandem IEF stages (Figure 2b).



▲ Figure 1: The ERK signaling in Jurkat E6-1 cells stimulated with α-CD3 for different times. Stimulation and cell lysis were performed with the microfluidic device (chip stimulation) and with conventional methods (POS control). The error bars denote one standard deviation. This fast ERK response is resolved with relatively small variations between experiments performed with the same stimulation conditions, showing the reproducibility of the stimulation and effectiveness of the integrated lysis in the microfluidic device.



▲ Figure 2: a) Focusing of Alexa 488 conjugated Protein G at various levels of unlabeled mouse IgG. Plotted are fluorescent intensities of Protein G alone (dotted line), 5µg/mL of IgG (dashed line), and 22µg/mL (solid line) that show the focusing of the IgG-Protein G complex. The proteins were focused in less than 20 seconds with an applied voltage of 30 V. b) Photograph of improved tandem-IEF device. Nine outlet fractions enable subsequent orthogonal separation and analysis.

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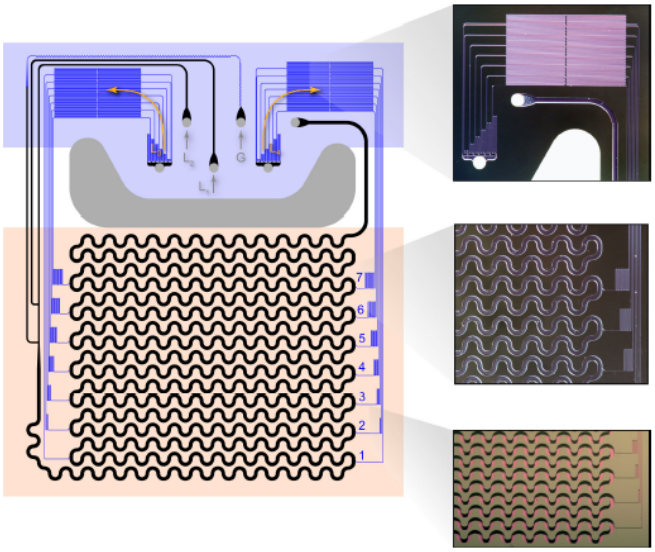
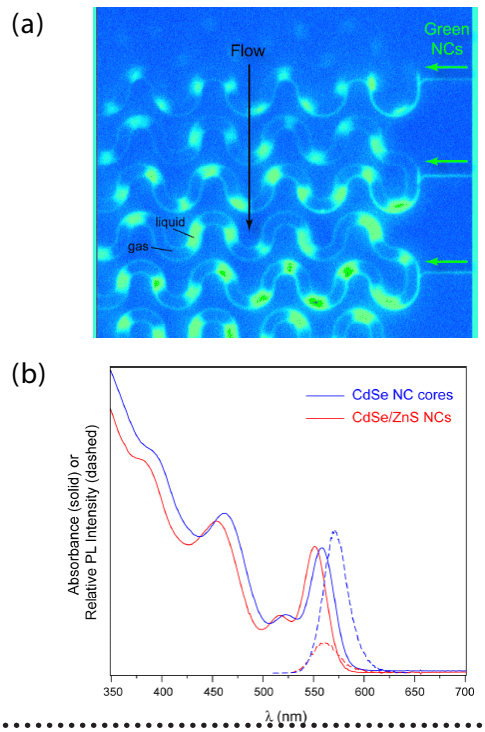
Microreactors for Synthesis of Quantums Dots

S. Marre, J. Guan, J. Park, M.G. Bawendi, K.F.Jensen
Sponsorship: NSF, ISN, Rhodia

We have fabricated gas-liquid, segmented-flow reactors with multiple temperature zones for the synthesis and the overcoating of quantum dots (QDs). In contrast to single-phase flow reactors, the segmented flow approach enables rapid mixing and narrow residence time distribution, factors which strongly influence the ultimate QD size distribution. The silicon-glass reactors accommodate a 1-m-long reaction channel (hydraulic diameter ≈ 400 μm) and swallow side channels for multiple additional injections of precursors inside the main channel (Figure 1). Pressure-drop channels were added in order to avoid backflow into the side channels. Two temperature zones are maintained, a heated region (> 260 °C) and a cooled quenching region (< 70 °C). Measurements of the flow distribution (Figure 2a) show that this side manifold design results in very uniform distribution even at very low nominal flow rates. As a model system, monodispersed CdSe and CdSe/ZnS QDs were prepared using this reactor. For the preparation of CdSe QDs, cadmium and selenium precursor solutions were delivered separately in the cooled region and were thereafter mixed in the heated region. An inert gas stream is introduced further downstream to form a segmented gas-liquid flow, thereby rapidly mixing the precursors and initiating the reaction, as was shown in a previous work [1]. In the case of the synthesis of CdSe/ZnS QDs, CdSe cores are introduced directly inside the main channel, while Zn and S precursors are added through the side swallow channels, allowing the overcoating. The reaction is stopped when the fluids enter the cooled outlet region of the device. When we vary the process parameters (temperature, precursors flow rates). the size of the cores material can be tuned without sacrificing the monodispersity. In addition, the overcoating of CdSe cores allows shifting the absorbance spectrum (5 nm), due to the presence of the ZnS layering (Figure 2b).



▲ Figure 1: Microreactor design with two feeder channels (blue) for adding precursor into the main stream. Each channel has a length of 14 cm and a hydraulic diameter of 50 μm, whereas the main reaction channel (black) is 1 m long and has a hydraulic diameter of 400 μm.



▲ Figure 2: (a) False-color fluorescence image used for measuring the flow distribution. Green-emitting nanocrystals are continuously injected from the side channels from the right into a gas-ethanol segmented flow in the main channel. (b) Absorbance and photoluminescence spectra of CdSe cores and CdSe/ZnS core/shell nanocrystals in hexane.

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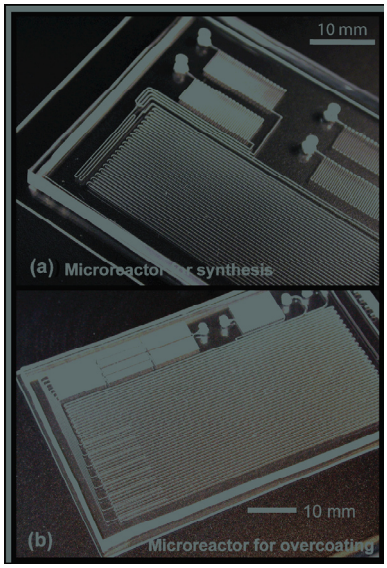
Microfluidic Synthesis and Surface Engineering of Colloidal Nanoparticles

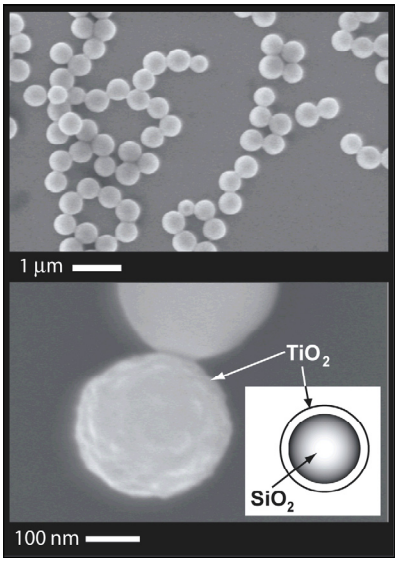
S.A. Khan, E.V. Loewer, K.F. Jensen

There has been considerable research interest over the last decade in fabricating core-shell materials with tailored optical and surface properties. For example, core-shell particles of silica and titania have drawn attention due their potential for trapping light at specific frequencies. This optical property depends on the formation of nanolayers on nano- or micro-cores. To obtain useful particles, these layers need to be uniform and even. These layered particles also need to be distinct and monodispersed. While nanolayer formation is successful in batch reactions, nonuniformity, agglomeration, and secondary nucleation often occur. We have developed microfluidic routes for synthesis and surface-coating of colloidal silica and titania particles.

The chief advantages of a microfluidic platform are precise control over reactant addition and mixing and continuous operation. Microfluidic chemical reactors for the synthesis and overcoating of colloidal particles are shown in Figures 1a and 1b, respectively [1-2]. Figure 2a is an SEM micrograph of silica particles synthesized in a microreactor (Figure 1a) operated in segmented gas-liquid flow mode. Figure 2b shows a silica nanoparticle coated with a thick shell of titania. We have also fabricated integrated devices combining synthesis and overcoating to enable continuous multistep synthesis of core-shell particles.



▲ Figure 1: Microfluidic reactor for (a) synthesis of colloidal silica, fabricated in PDMS, and (b) overcoating thick titania shells on silica particles.



▲ Figure 2: (a) Silica synthesized in microreactor and (b) titania-coated silica.

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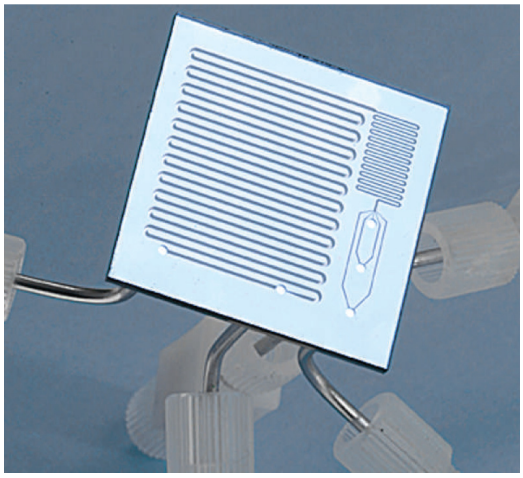
Organic Synthesis in Microreactor Systems

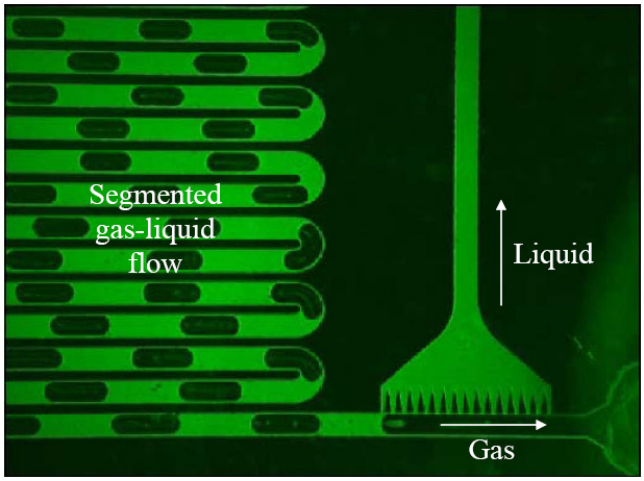
J.P. McMullen, N. Zaborenko, H.R. Sahoo, K.F. Jensen
Sponsorship: Pacific Scientific, Microchemical Systems Consortium

Enhanced heat and mass transfer, reduced reaction volume, and the ability to run several experiments in parallel render microreactors powerful instruments for scanning and optimizing chemical reaction conditions. Furthermore, the high mechanical strength and thermal conductivity of silicon microreactors permit the exploration of organic syntheses at higher temperatures and pressures than can be achieved with conventional bench-scale equipment. An example of these benefits is demonstrated in the aminocarbonylation reaction study [1]. Traditionally, these reactions are performed at atmospheric conditions and with temperatures at or below the boiling point of the solvent (toluene, 110°C). However, in silicon microreactors (Figure 1), it is possible to reach pressures exceeding 100 bar [2] and temperatures above 800°C [3]. Exploration of the aminocarbonylation reaction offers information that can be useful for the optimizing selectivity of the synthesis; higher CO pressures enhance α-ketoamide formation and increased temperatures favor amide formation.

Once the chemical reaction is complete, it is desirable to separate the toxic gas from the liquid phase. Although negligible on the macro-scale, surface forces play a dominant role in microfluidics. Creating a capillary-based system (Figure 2) [4] makes it possible to take advantage of these forces. The liquid phase wets the capillaries and prevents the gas from penetrating the capillary matrix through the proper adjustments of pressure drops across the separator. Similarly, this concept can be applied to heterogeneous reactions that involve two immiscible liquids. Due to this microtechnology, microreactor systems can be assembled for multi-step synthesis and separation that could not easily be achieved in traditional laboratory environments. As a result, high throughput experiments can be performed and entire chemical processes can be optimized efficiently with microreactor systems.



▲ Figure 1: Silicon microreactor. Photograph, F. Frankel.



▲ Figure 2: Capillary system for gas-liquid separation.

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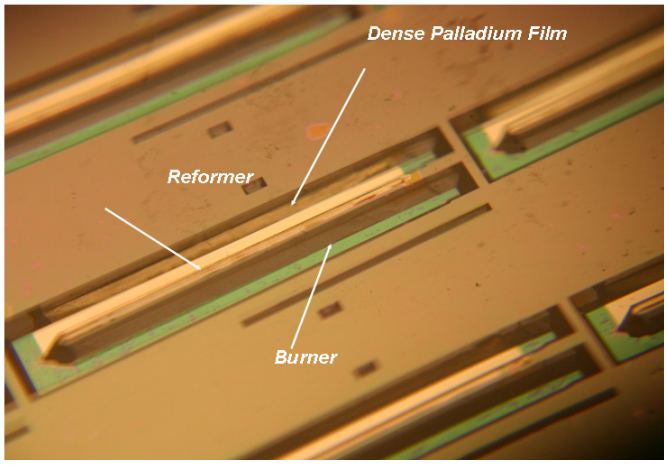
Autothermal Catalytic Micromembrane Devices for Portable High-purity Hydrogen Generation

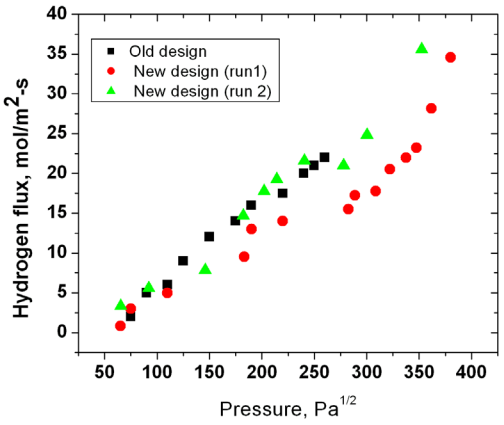
K. Deshpande, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

The high efficiency and energy density of miniaturized fuel cells provide an attractive alternative to batteries in the portable-power-generation market for consumer and military electronic devices [1-3]. The best fuel cell efficiency is typically achieved with hydrogen, but safety and reliability issues remain with current storage options. Consequently, there is continued interest in reforming of liquid fuels to hydrogen. The process typically involves high-temperature reforming of fuel to hydrogen combined with a low-temperature PEM fuel cell, which implies significant thermal loss. Owing to its high hydrogen content (66%) and ease of storage and handling, methanol is an attractive fuel. However, partial oxidation of methanol also generates CO, which can poison the fuel cell catalyst [1].

Previously [4] we have successfully demonstrated hydrogen purification using thin (~200 nm) Pd-Ag membranes using electrical heating. Further, integration of these devices with $LaNiCoO_3$ catalyst allowed methanol reforming at 475°C with 47% fuel conversion [5]. In the current work, we fabricate a novel autothermal reformer for hydrogen generation and purification using bulk micromachining techniques. This device combines the reforming unit with a catalyst loaded microreactor for combustion of hydrogen not recovered through the Pd- Ag membrane, generated CO, and unreacted methanol. The energy from the combustion heats the reformer to the operating temperature (~450C). High thermal conductivity of silicon ensures efficient heat transfer from combustor to reformer. In the first phase, Pd-Ag membrane stability post-fabrication was tested; results indicated a pin-hole- and crack-free layer. Further, we successfully demonstrate high-pressure operation (up to 1.6 atm) of the device for enhanced hydrogen flux. The microburner has also been characterized with hydrogen oxidation over platinum catalyst. Work on reforming methanol for hydrogen generation and characterization of thermal responses is currently under progress.



▲ Figure 1: Fabricated reformer-burner unit with palladium membranes.



▲ Figure 2: Hydrogen flux comparison as a function of applied feed pressure.

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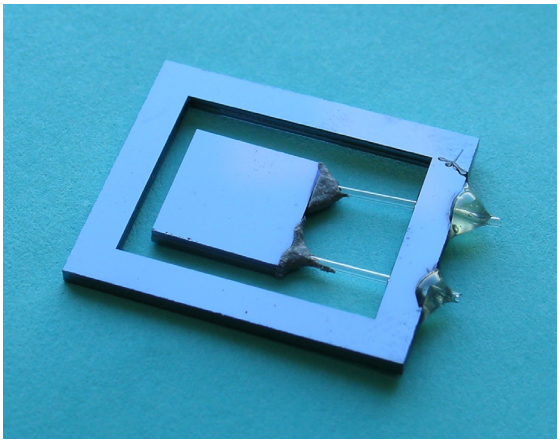
Thermal Management in Devices for Portable Hydrogen Generation

B. Blackwell, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI, Lincoln Laboratory

The development of portable-power systems employing hydrogen-driven solid oxide fuel cells continues to garner significant interest among applied science researchers. The technology can be applied in fields ranging from the automobile to personal electronics industries. This work focuses on developing microreaction technology that minimizes thermal losses during the conversion of fuels – such as light-end hydrocarbons, their alcohols, and ammonia – to hydrogen. Critical issues in realizing high-efficiency devices capable of operating at high temperatures have been addressed: specifically, thermal management, the integration of materials with different thermophysical properties, and the development of improved packaging and fabrication techniques.

A new fabrication scheme for a thermally insulated, high-temperature, suspended-tube microreactor has been developed. The new design improves upon a monolithic design proposed by Arana *et al.* [1]. In the new modular design (Figure 1), a high-temperature reaction zone is connected to a low-temperature (~50°C) package via the brazing of pre-fabricated, thin-walled glass tubes. The design also replaces traditional deep reactive ion-etching (DRIE) with wet potassium hydroxide (KOH) etching, an economical and time-saving alternative. A brazing formulation that effectively accommodates the difference in thermal expansion between the silicon reactor and the glass tubes has been developed. Autothermal combustion of hydrogen, propane (Figure 2), and butane has been demonstrated in ambient atmosphere and in a vacuum.



▲ Figure 1: Suspended-tube microreactor showing 2 pre-fabricated SiO2 tubes, a microfabricated Si reaction chip, and a microfabricated Si frame. The modular design is assembled via a glass braze.

▲ Figure 2: Autothermal combustion of propane under 25-mTorr vacuum.

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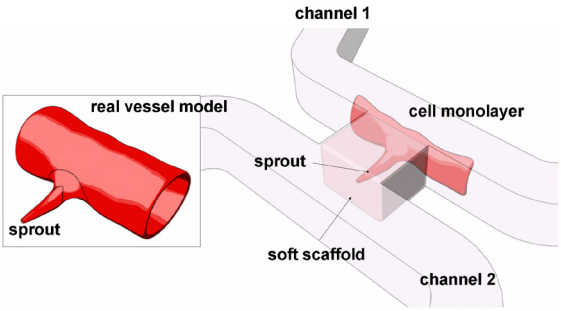
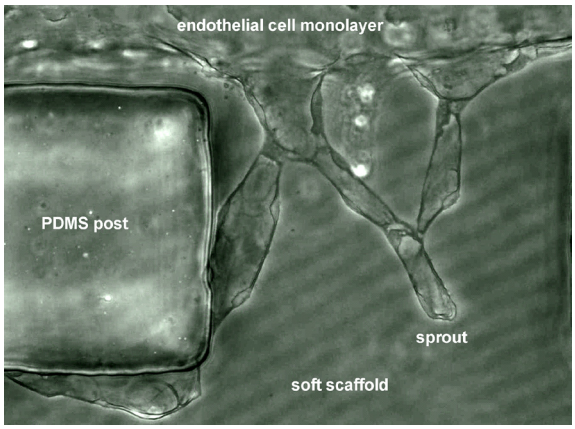
Microfluidic Systems for the Study of Vascular Networks

S. Chung, V. Vickerman Kelly, R. Sudo, R.D. Kamm
Sponsorship: Draper Labs, NIH NIBIB

Mechanical forces are important regulators of cell biology in health and disease. Cells in the vascular system are subjected to fluid shear stress, cyclic stretch, and differential pressure [1-3], and at the same time they receive multiple biochemical cues. All these factor into the integrated response of the tissue. A microfluidic bioreactor has been constructed to facilitate studies into the roles of both biophysical and biochemical factors on capillary morphogenesis. The device is made of PDMS, cured on an SU-8 patterned wafer. Then a scaffold material, collagen, is induced into a specific region of devices that was designed to keep its shape and properties. Cells are seeded via one flow channel on the surface of the scaffold and then subjected to controlled mechanical factors like surface shear and trans-endothelial pressure, or biochemical angiogenic factors, inducing the formation of vascular sprouts that extend across the scaffold to a second flow channel. With the bioreactor, cells on the scaffold form a confluent monolayer and generate sprouts. They show different responses and interactions with the scaffold, following the angiogenic factors, fluidic factors, surface characteristics and scaffold properties. Experiments are now under way to find the relations between cell responses and controlled factors. The developed system is the first system that can control biochemical and mechanical factors together, and it can be used for comparing the effects of angiogenic factors under controlled environment with enhanced view. It can also be applied to study the process of angiogenesis that entails the growth of vascular sprouts emanating from one endothelial surface and connecting with the other.



▲ Figure 1: Concept drawing of the developed device. The seeded monolayer on the scaffold works as the wall of a real vascular system.



▲ Figure 2: The MVC sprout formed in collagen gel from the cell monolayer.

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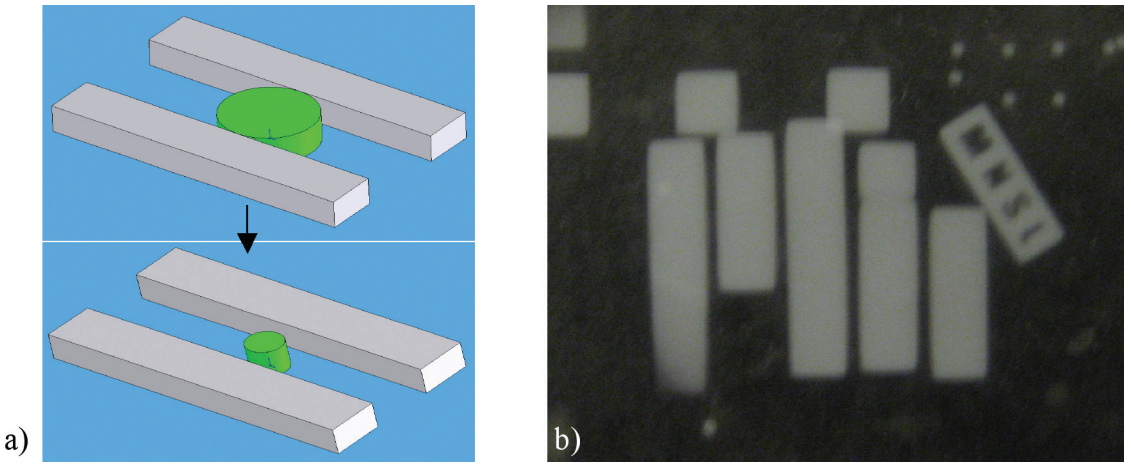
Patterning and Processing of Thermosensitive Hydrogels for Microfluidics Applications

N.E. Reticker-Flynn, H. Lee, S.G. Kim

Hydrogels have been an active area of research for a variety of applications due to their ability to retain large volumes of water within their polymer gel networks. Stimuli-responsive hydrogels provide the added advantage of the ability to control the water retention by means of external stimuli. For example, N-isopropylacrylamide (NIPAAm) is a thermosensitive hydrogel that exhibits a Lower Critical Saturation Temperature (LCST) around 32°C, above which the gel becomes hydrophobic and expels the water molecules, resulting in a drastic swelling/shrinking ratio. The goal of this project is to utilize this pseudo-binary transition in the fields of microfluidics and drug delivery.

By imbedding magnetic nanoparticles into the gel networks, the Hamad-Schifferli group [1] could control the temperature of the gels by inducing eddy currents by means of an oscillating magnetic field. We are developing the concept further into micro-scale devices that can be monolithically integrated into many microfluidic systems. We have demonstrated the ability to photopattern the hydrogels and have shown control of the swelling behavior by controlling the amount of cross-linking in the network. This allowed for the creation of hydrogel valves for microfluidic devices. Unlike pressure controlled valves, these valves do not require any physical interconnects to macro-scale devices. This advantage could prove extremely useful in the commercialization of microfluidic analysis systems where users might not have equipment such as syringe pumps or air compressors available. In addition to valves, applications of the swelling behavior to micropumps are also being examined.



▲ Figure 1: (a) Controlable microfluidic valve activated by means of external magnetic field. (b) NIPAAm MIT logo with top of "T" removed from substrate.

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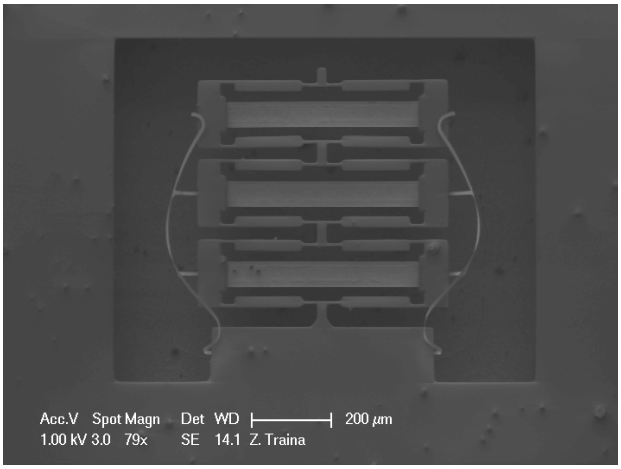
A Large-strain, Arrayable Piezoelectric Microcellular Actuator by Folding Assembly

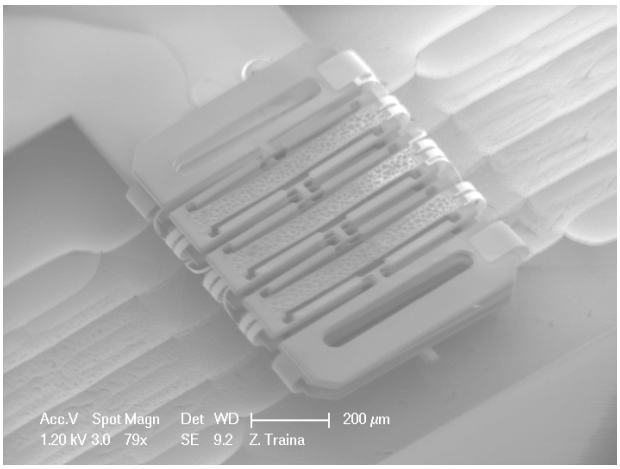
Z.J. Traina, S.G. Kim
Sponsorship: Korean Institute of Machinery and Materials

A low-power, piezoelectric, contracting cellular MEMS actuator has been developed that demonstrates a peak strain of 3% under a 10 V stimulus. Since the motion of the end effecter is linear and in-plane, the actuator can be arrayed in series to amplify the total stroke or in parallel to amplify the total force, as needed. Location of the piezoelectric member through the structural center of stiffness reduces the potential for parasitic out of plane bending present in previous designs [1].

Cellular actuators arrays can be assembled into a larger array of actuators. We demonstrated that sets of cellular microactuators can be assembled out of plane by folding them over thin gold hinges. To our knowledge, this study is the first effort in this field. The gold hinges serve dually as mechanical assembly guides and electrical interconnects. Long chains of devices may be assembled by rolling out of plane. Figure 2 shows a smaller collection, assembled by folding three actuator triplets onto one another. Actuation of the collection is contingent on the manufacturing of functional thin-film PZT.



▲ Figure 1: An array of three cellular actuators fabricated in series, which demonstrates a total static displacement of more than 15 µm under 10V stimulus. The strain of the assembly exceeds that of unmodified PZT by a factor of more than 29:1.



▲ Figure 2: A total of 9 actuators (three actuator triplets) assembled into one collection by folding out of plane over gold hinges. Actuation of a folded device collection is contingent on the manufacturing of functional thin film PZT.

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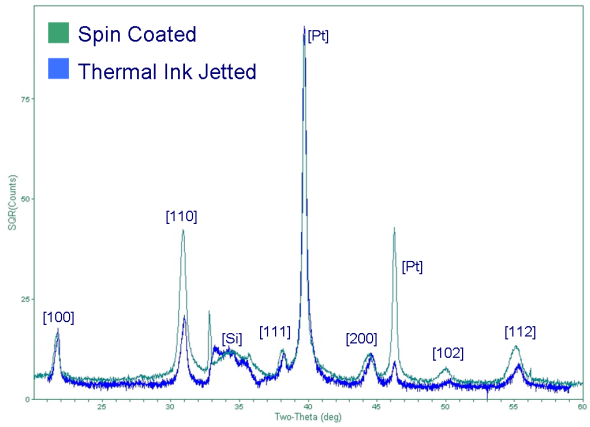
Thermal Ink Jet Printing of Lead Zirconate Titanate Thin Films

S. Bathurst, H.W. Lee, S.G. Kim
Sponsorship: DARPA, Hewlett-Packard

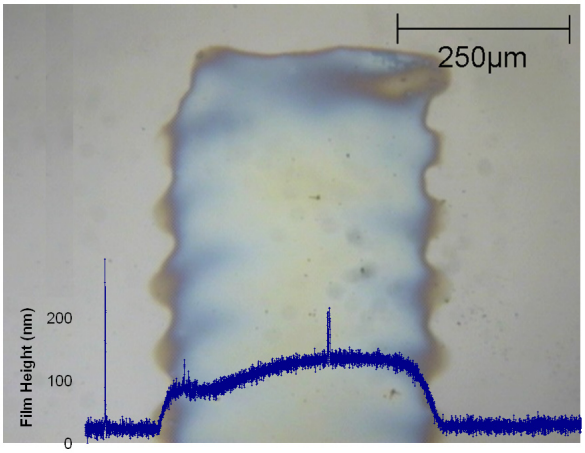
The ferromagnetic and piezoelectric properties of ceramic lead zirconate titanate (PZT) thin films have made PZT an appealing choice for micro-sensors and actuators. Significant work has been done integrating PZT with standard MEMS processes, including the development of PZT sol-gels for spin coating [1-2]. Cracking is often a problem with PZT spin coating due to the brittle nature of the films coupled with the thermal strain experienced during annealing. This propensity for cracking limits the overall thickness deposited and the size out of plane features over which PZT can be reliably coated. Furthermore, spin coating requires a large volume of the expensive PZT precursor solution. We propose thermal ink-jet printing of a modified PZT sol-gel as a new method of depositing PZT films for MEMS applications. Preliminary work has shown ink jetting to be a reliable method for depositing PZT films of the correct thickness for MEMS applications and that annealed films can crystallize into the piezoelectric perovskite phase using the same thermal process developed for spin-coated PZT (see Figure 1) [3]. The goal of this research is to develop a deposition process that will enable reliable manufacturing of high-quality PZT films with greater deposition flexibility and lower material costs than spin coating.

Thermal ink jetting technology supports a wide range of ink viscosities and solid particle contents. The ink composition can therefore be adjusted to control both the contact angle of solution with the substrate (1000Å Pt/ 200Å Ti) and the as-deposited film thickness. This flexibility allows for the deposition of films with thickness and uniformity that are acceptable for the fabrication of piezoelectric devices (see Figure 2). Multiple layers can be deposited to attain the thickness as needed. Currently, annealed films have been prepared as thick as 0.5 μm, corresponding to an as deposited thickness of approximately 1 μm. This is comparable to the current limit of standard spin-coated PZT sol-gel processed; printing of thicker films is under investigation.

We acknowledge Hewlet Packard for providing the POEMS thermal ink-jet printer.



▲ Figure 1: Comparison of X-ray diffraction of spin-coated PZT film with thermal ink-jetted film.



▲ Figure 2: Optical microscope image and profilometry of as deposited thermal ink-jetted lead zirconate titanate thin film.

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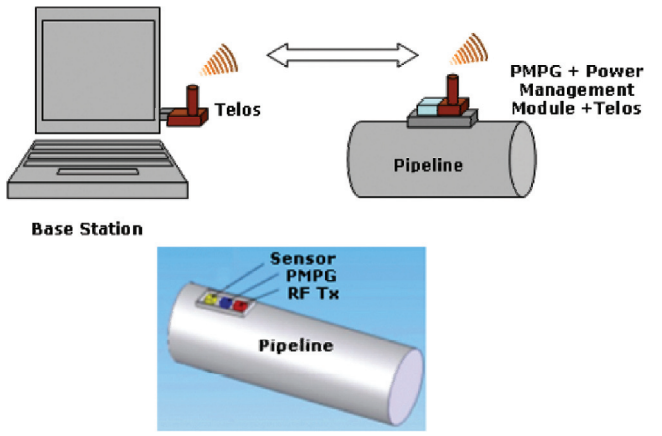
Piezoelectric Micro-power-penerator: MEMS Energy-harvesting Device for Self-powered Wireless Corrosion-monitoring System

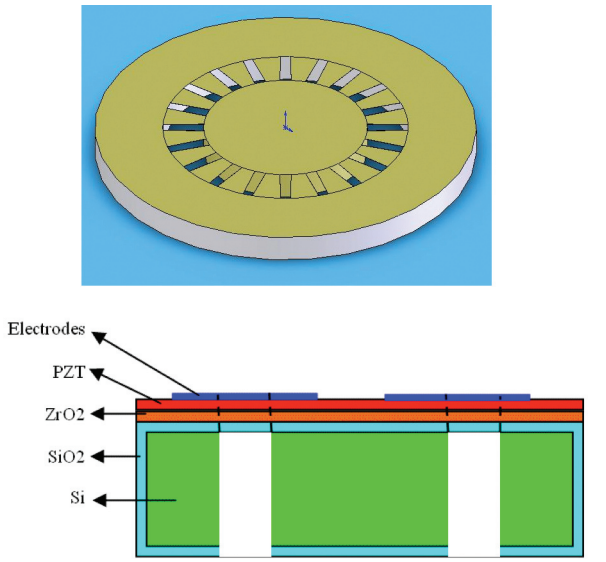
A. Hajati, S.G. Kim
Sponsorship: NSF, Korean Institute of Machinery and Material

A novel thin-film, lead zirconate titanate $Pb(Zr,Ti)O_3$ (PZT), energy-harvesting MEMS device is being developed for autonomous wireless monitoring systems. It is designed to harvest energy from parasitic vibrational energy sources and convert it to electrical energy via the piezoelectric effect. We envision that harvesting parasitic energy from the vortex-induced vibration of the oil pipelines will deploy a massive number of microsensors along the hundreds of miles of pipeline in very cold and remote areas. The proposed system consists of a corrosion sensor, a radio transceiver, a microcontroller, a power management module, and a piezoelectric micro power generator (PMPG) to supply the needed power of the system without replacing batteries.

The new pie-shaped design for the harvester (about a size of a nickel) has a radical departure from previous design concepts. This energy harvester design can be regarded as revolutionary as the first self-rectifying piezoelectric power generator. The new design avoids the high Q resonance, which is also a big change from previous designs. This will enable more robust power generation even if the frequency spectrum of the source vibration varies unexpectedly. Furthermore, the beam shape is optimized to achieve uniform allowable strain throughout the PZT layer. Currently, the first prototype, which is shown schematically, is being fabricated at MTL.



▲ Figure 1: Wireless sensor system schematics. The self-powered sensor node transmits data to a receiver at the base station.



▲ Figure 2: The structure of a pie-shaped PMPG.

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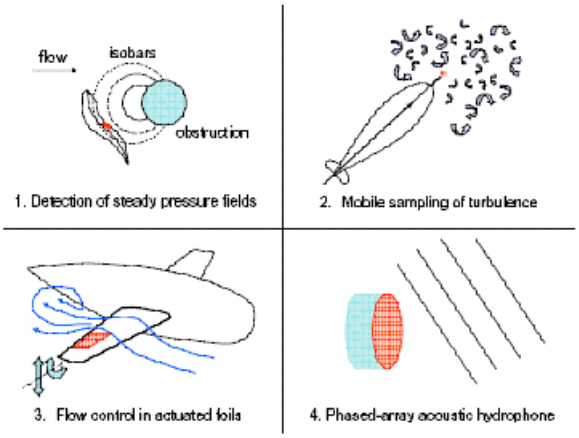
Lateral-line-inspired MEMS-array Pressure Sensing for Passive Underwater Navigation

V. Fernandez, S. Hou, F. Hover, J. Lang, M. Triantafyllou
Sponsorship: NOAA: MIT Sea Grant College Program

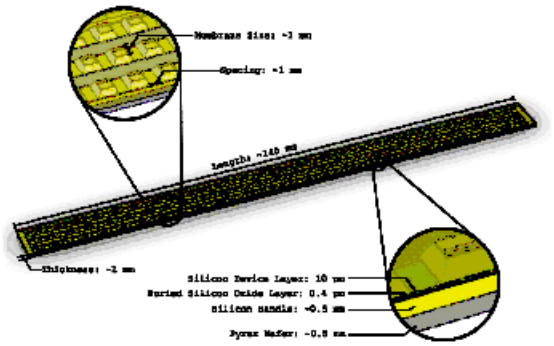
A novel sensing technology for unmanned undersea vehicles (UUVs) is under development. The project is inspired by the lateral line sensory organ in fish, which enable some species to form three-dimensional maps of their surroundings [1-2]. The canal subsystem of the organ can be described as an array of pressure sensors [3]. Interpreting the spatial pressure gradients allows fish to perform a variety of actions, from tracking prey [4] to recognizing nearby objects [2]. It also aids schooling [5]. Similarly, by measuring pressure variations on a vehicle surface, an engineered dense pressure sensor array allows the identification and location of obstacles for navigation (Figure 1). We are demonstrating proof-of-concept by fabricating such MEMS pressure sensors by using KOH etching techniques on SOI wafers to construct strain-gauge diaphragms.

The system consists of arrays of hundreds of pressure sensors spaced about 2 mm apart on etched silicon and Pyrex wafers. The sensors are arranged over a surface in various configurations (Figure 2). The target pressure resolution for a sensor is 1 Pa, which corresponds to the noiseless disturbance created by the presence of a 0.1-m-radius cylinder in a flow of 0.5 m/s at a distance of 1.5 m. A key feature of a sensor is the flexible diaphragm, which is a thin (20 μm) layer of silicon attached at the edges to a silicon cavity. The strain on the diaphragm due to pressure differences across the diaphragm is measured. At this stage, the individual MEMS pressure sensors are being constructed and tested.

In parallel to the construction of a sensor array, techniques are being developed to interpret the signals from a dense pressure array by detecting and characterizing wake structures such as vortices and building a library of pressure distributions corresponding to basic flow obstructions. In order to develop these algorithms, experiments are being performed on coarse arrays of commercial pressure sensors



▲ Figure 1: Pressure-sensor array applications.



▲ Figure 2: Diagram of pressure-sensor array with basic structure depicted.

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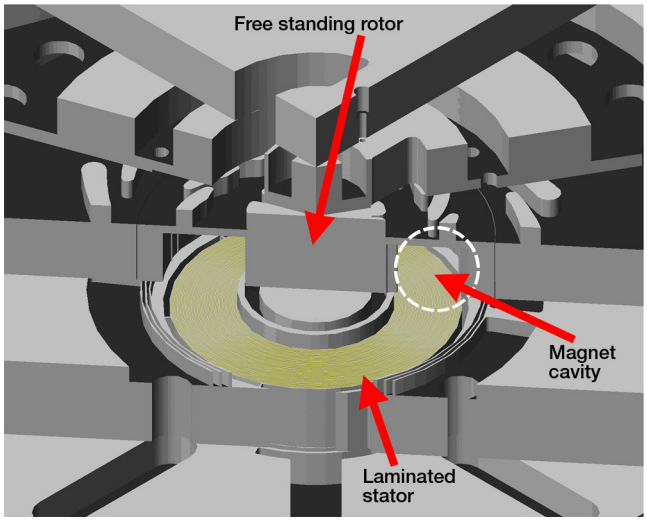
Fabrication of a Fully-integrated Multiwatt µTurboGenerator

B.C. Yen, M. Allen, F.F. Ehrich, A.H. Epstein, F. Herrault, K.J. Hillman, L.C. Ho, S. Jacobson, J.H. Lang, H. Li, Z.S. Spakovszky, C.J. Teo, D. Veazie
Sponsorship: US Army Research Laboratory Collaborative Technology Alliance

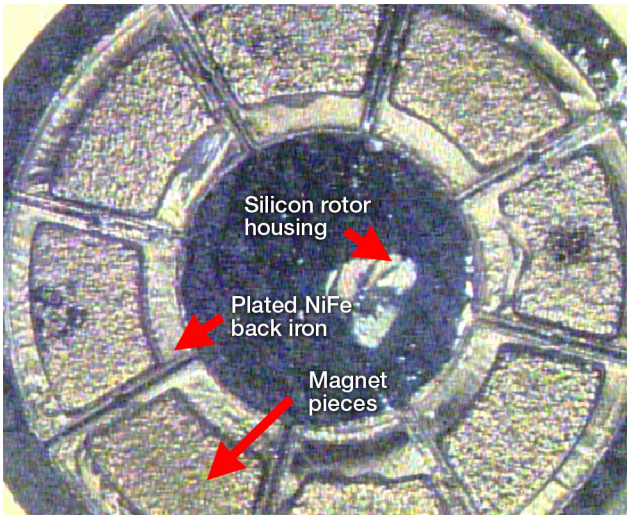
There is a need for compact, high-performance power sources that can outperform the energy density of modern batteries for use in portable electronics, autonomous sensors, robotics, and other applications. Building upon the results presented in [1], the current research is aimed at fabricating a fully-integrated, multiwatt micro turbogenerator on silicon that can produce 10 W DC output power (Figure 1). One of the main challenges involves the seamless integration between silicon and the magnetic components required to generate power. The generator requires a NiFe soft magnetic back iron and laminated stator for flux redirection as well as NdFeB permanent magnet pieces to serve as flux sources (Figure 2). In addition, copper windings must be fabricated above the laminated stator to couple to the alternating flux in order to extract electrical power from the machine.

Great strides have been made in the past year to quantify the requirements on the magnet pieces that will go into the rotor housing. Manufacturing accuracy of the pieces is critical because variations in the magnet geometries create an overall rotor imbalance, which can cause the rotor to crash during transcritical operation. A procedure in which the gaps around the magnet pieces are filled with solder and then polished back using chemical-mechanical planarization has been developed; this process can reduce the effective imbalance of the rotor by an order of magnitude.

The assembly and packaging procedure for the turbogenerator is also critical because the embedded permanent magnets cannot withstand temperatures much above 150 °C. This temperature restriction rules out the use of fusion bonding for the final die-level assembly after rotor insertion. Based on results presented by Choe, *et al.* [2], an eutectic In-Sn bonding scheme that requires only 140 °C has been researched. In this scheme, Cr/Au is deposited on one bonding surface and Cr/Sn/In/Au is deposited on the other surface; both depositions are done using an e-beam evaporator without breaking vacuum. By painting no-clean flux on both surfaces and compressing the dies together on a hot plate, we form the bond.



▲ Figure 1: Conceptual rendering of the fully-integrated generator. Back iron and magnet pieces will be inserted into the empty cavities of the rotor, which will be supported by gas thrust and journal bearings. Electrical connections are taken out from the backside of the die.



▲ Figure 2: Magnetic rotor test structure with back iron plated and sample magnet pieces inserted. The magnets shown in this photo were not manufactured to the correct size, but they demonstrate what a completed rotor might look like. (Courtesy of F. Herreault, GIT)

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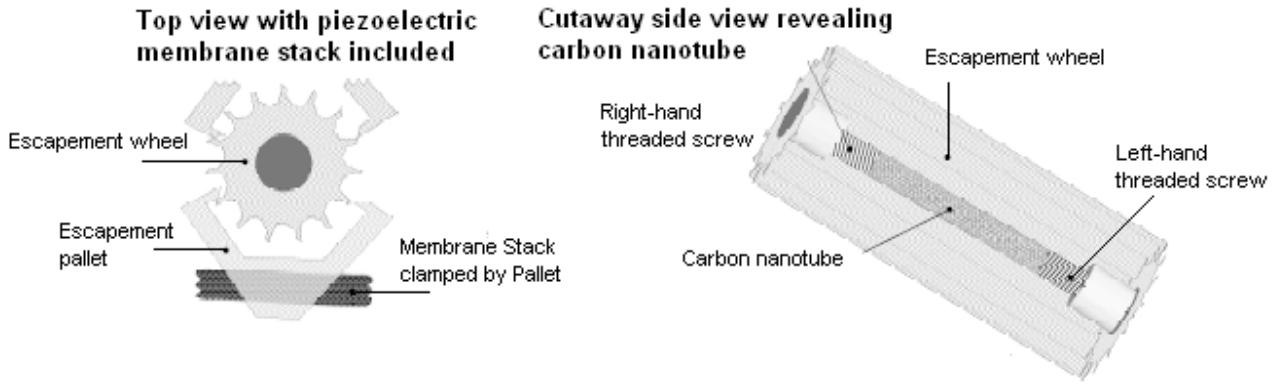
A Portable Power Source Based on MEMS and Carbon Nanotubes

F A. Hill, T.F. Havel, C. Livermore
Sponsorship: Deshpande Center for Technological Innovation

There is a growing need for small, lightweight, reliable, highly efficient and fully rechargeable portable power sources. The focus of this project is the design and modeling of a system in which energy is stored in the elastic deformation of carbon nanotube (CNT)-based springs. The CNTs are coupled to a MEMS electric generator. When the CNT deformation is released, the stored energy actuates the generator, which then converts the energy into electricity. The MEMS generator may be operated in reverse, as a motor, in order to wind the CNT springs and recharge the system. Alternatively, the stored elastic energy may be used to supply a mechanical load directly. This project is motivated by recent research into the mechanical properties of CNTs. The CNTs have a high stiffness, low defect density, and a consequently high yield strain that enables them to store elastic energy with significantly greater energy density than typical spring materials such as high-carbon steel. Models suggest that CNTs can be reversibly stretched by up to 15% [1]; lower strains of up to 6% have been demonstrated experimentally to date [2-3].

This type of system offers several important potential advantages. First, due to CNTs' high strength, high flexibility, and low defect density, they can store energy at very high energy density. Considering just the CNT-based spring itself, the energy density of an array of CNTs stretched to a reversible 15% strain is about 1500 W-hr/kg, about ten times the energy density of Li-ion batteries. The energy density of the final system will be lower because of the finite conversion efficiency of the generator and the weight of both the supporting structure and the generator hardware. In addition, because energy storage in the CNT system is based on stretching chemical bonds rather than breaking and reforming chemical bonds as in batteries, the CNT-MEMS generator system has the potential to operate at higher power densities, under harsher conditions, to deeper discharge levels, and through a greater number of charge-discharge cycles than a chemical battery.

The system architecture consists of a CNT-based energy storage element, an energy release rate mechanism, and a MEMS generator. This project is examining and modeling different variations on this system architecture that incorporate different modes of deformation of the CNT-based energy storage element, various types of generators, different types of coupling between the storage element and the generator, and different size scales for the various components. One conceptual example is illustrated below, in which the axial relaxation of an axially-stretched CNT-based storage element is converted to rotational motion of a wheel. The wheel is coupled to a piezoelectric generator through a mechanism that regulates the rate of energy release, much as in a mechanical watch.



▲ Figure 1: Schematic diagram showing the conceptual design of a MEMS-based energy storage device

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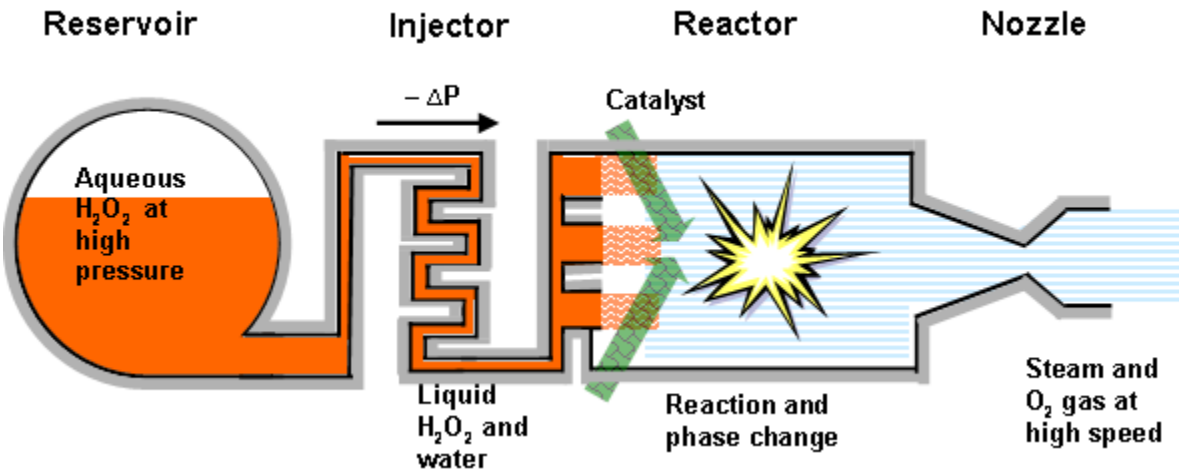
A MEMS Steam Generator

F. Eid, L.F. Velasquez-Garcia, A.H. Epstein, C. Livermore
Sponsorship: DARPA, MDA, AFRL

Previous work [1] has shown that MEMS technology has significant potential to create more compact, higher- performing hardware for chemical oxygen iodine lasers (COIL). In COILs, the laser medium is a flowing gas that must be pumped through the system at high mass flow rates to ensure proper system operation. As a result, compact pumps with high pumping rates are a key element of the COIL system. One promising component of a MEMS COIL system would be a compact MEMS pump system in which the pump action is provided in part by micro steam ejectors and the micro steam generators that supply their driving fluid. This work describes the design and modeling of a microscale hydrogen peroxide (H_2O_2)-based steam generator to supply such a MEMS pump system. Hydrogen peroxide is a readily available, inexpensive, nontoxic, and environmentally friendly fluid that may be catalytically decomposed to form steam. Steam generation by the catalytic decomposition of H_2O_2 also finds other important applications in the MEMS field beyond pumping, particularly in the area of thrust generation. Compared to their macroscale counterparts, MEMS H_2O_2-based steam generators offer better performance, notably improved mixing, and higher uniformity due to the absence of moving parts [2-3].

A complete MEMS steam generator consists of a peroxide reservoir, an injector, a reactor, and a converging-diverging nozzle to accelerate the exiting flow, as shown in Figure 1. Initial work focuses on the design of the reactor and nozzle. Liquid H_2O_2 in aqueous solution is injected into the reactor, where it decomposes into steam and oxygen gas upon contact with the catalyst. A continuous supply of homogeneous liquid catalyst is used, as it avoids the aging problem typically exhibited by heterogeneous catalysts [4]. The gaseous products of the reaction are then accelerated to supersonic velocities through the converging-diverging nozzle. The work to date indicates that a MEMS steam generator designed to minimize heat transfer to the environment can provide complete, compact, uniform decomposition of peroxide into steam suitable to drive a MEMS pumping system.



▲ Figure 1: Schematic diagram of a hydrogen peroxide-based MEMS steam generator, showing the peroxide reservoir, injector, reactor, and nozzle.

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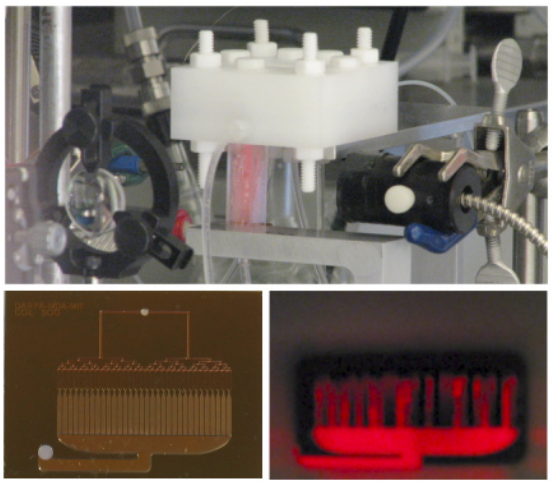
Microscale Singlet Oxygen Generator for MEMS-based COIL Lasers

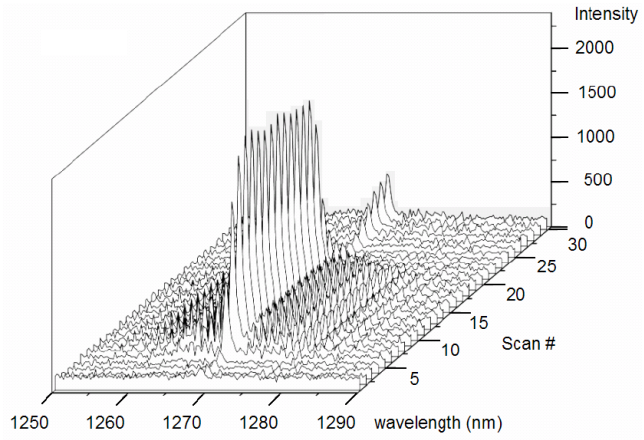
T. Hill, L.F. Velásquez-García, A.H. Epstein, K.F. Jensen, C. Livermore
Sponsorship: DARPA, MDA, AFRL

Conventional chemical oxygen iodine lasers (COIL) offer several important advantages for materials processing, including short wavelength (1.3 μm) and high power. However, COIL lasers typically employ large hardware and use reactants relatively inefficiently. This project is creating an alternative approach called microCOIL. In microCOIL, most conventional components are replaced by a set of silicon MEMS devices that offer smaller hardware and improved performance. A complete microCOIL system includes microchemical reactors, microscale supersonic nozzles, and micropumps. System models incorporating all of these elements predict significant performance advantages in the microCOIL approach [1].

Initial work is focused on the design, microfabrication, and demonstration of a chip-scale singlet oxygen generator (SOG), a microchemical reactor that generates singlet delta oxygen gas to power the laser. Given the extensive experience with microchemical reactors over the last decade [2], it is not surprising that a microSOG would offer a significant performance gain over large-scale systems. The gain stems from basic physical scaling; surface-to-volume ratio increases as the size scale is reduced, which enables improved mixing and heat transfer. The SOG chip being demonstrated in this project employs an array of microstructured packed-bed reaction channels interspersed with microscale cooling channels for efficient heat removal [3]. To date the device has produced oxygen concentrations of 10^{17} cm^{-3}, yields approaching 80% and molar flowrates in excess of $600x10^{-4}$ moles/L/sec [4]. The yield and molar flowrates indicate a significant improvement over the macroscale SOG designs.



▲ Figure 1: A – View of chip surface showing glow resulting from singlet-oxygen production; B – View of packaging and optics surrounding microSOG; C – Photograph of microSOG.



▲ Figure 2: The IR spectra measured at the μSOG gas outlet versus time. The peak at 1268 nm indicates the spontaneous decay of singlet oxygen into its triplet state.

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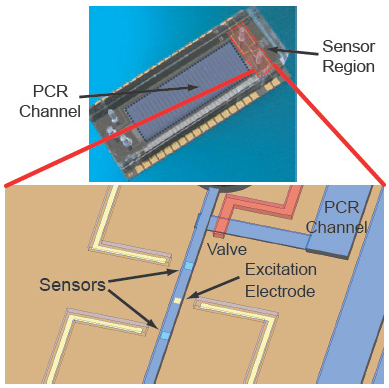
An Integrated Microelectronic Device for Label-free Nucleic Acid Amplification and Detection

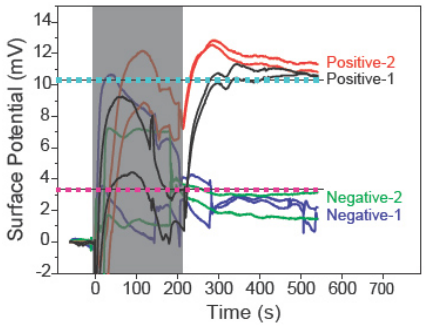
C.J. Hou, M. Godin, K. Payer, S.R. Manalis
Sponsorship: Hewlett-Packard, AFOSR

While there have been extensive advances in miniaturized polymerase chain reaction (PCR) systems, progress on integrated microfabricated readout mechanisms has been rather limited, and most systems rely on off-chip optical detection modules to measure the final product. Existing optical detection platforms typically include CCD cameras, photodiodes, and photomultiplier tubes. While such hardware has adequate sensitivity for detecting PCR products in sample volumes significantly lower than that of bench-top systems, most are difficult to miniaturize and integrate into a compact analytical system. For example, some portable systems incorporating external LEDs and photodetectors can weigh between 1 kg and 4 kg each. To address these limitations, several groups have successfully embedded photodetectors within integrated PCR platforms. However, these devices still rely on external excitation sources.

To address this limitation, we have developed an integrated microelectronic device for amplification and label-free detection of nucleic acids (Figure 1) [1]. Amplification by PCR is achieved with on-chip metal resistive heaters, temperature sensors, and microfluidic valves. We demonstrate a rapid thermocycling with rates of up to 50°C/s and a PCR product yield equivalent to that of a bench-top system. Amplicons within the PCR product are detected by their intrinsic charge with a silicon field-effect sensor. Similar to existing optical approaches with intercalators such as SYBR Green, our sensing approach can directly detect standard double-stranded PCR products while in contrast our sensor occupies a micron-scale footprint, dissipates only nano-watt power during operation, and does not require labeling reagents. By combining amplification and detection on the same device, we show that the presence or absence of a particular DNA sequence can be determined by converting the analog surface potential output of the field-effect sensor to a simple digital true/false readout.



▲ Figure 1: Device layout and concept. (top) Photograph of an integrated device with embedded sensors (right dotted area), PCR microfluidic channel with integrated valves (left dotted area), and metal-resistive heaters and temperature sensors (features above and below PCR channel). (bottom) A 3D rendering of the device centered on sensors (top and bottom squares) and an excitation metal electrode. Adjacent features include gold traces for electrical connections, inlet of the sensor channel, and an integrated valve controlling the interface to the PCR channel.



▲ Figure 2: The integrated PCR and field-effect sensing of product. The sensor was functionalized and pressure was applied to flow the content of PCR channel over electronic sensors, after which valves were closed and measurement buffer flow was restored. The PCR channel was replenished with starting PCR reagent as its contents flowed into the sensing channel. The greyed-out area indicates the period of PCR channel injection during which mechanical operations caused the sensor to lose its baseline value and drift temporarily. The higher and lower dotted segments are arbitrarily defined threshold levels for positive and negative signals, respectively.

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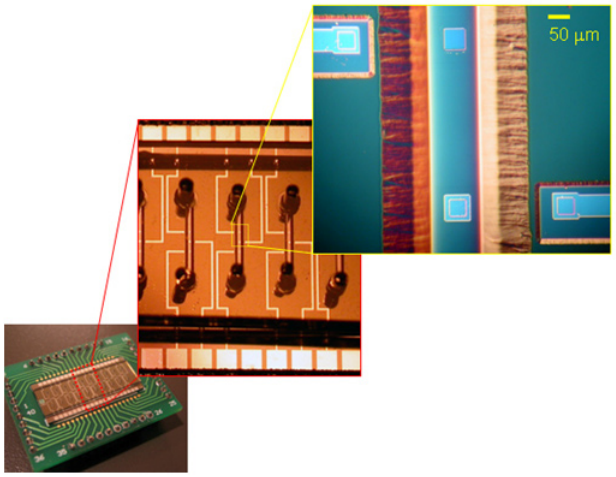
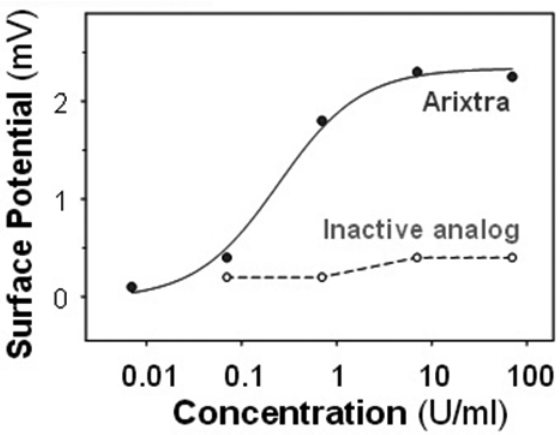
Monitoring of Heparin and its Low Molecular Weight Analogs by Silicon Field Effect

N. Milovic, J. Behr, M. von Muhlen, M. Godin, C.J. Hou, K.R. Payer, A. Chandrasekaran, P.R. Russo, R. Sasisekharan, S.R. Manalis
Sponsorship: Hewlett-Packard, AFOSR

Heparin is a highly sulfated glycosaminoglycan that is used as an important clinical anticoagulant. Monitoring and control of the heparin level in a patient's blood during and after surgery is essential, but current clinical methods are limited to indirect and off-line assays. We have developed a silicon field-effect sensor for direct detection of heparin by its intrinsic negative charge [1]. The sensor consists of a simple microfabricated electrolyte-insulator-silicon (EIS) structure encapsulated within microfluidic channels (Figure 1). As heparin-specific surface probes, we used the clinical heparin antagonist protamine or the physiological partner antithrombin III. The dose-response curves in 10% PBS revealed a detection limit of 0.001 U/ml, which is orders of magnitude lower than clinically relevant concentrations. We also detected heparin-based drugs, such as the low-molecular-weight heparin enoxaparin (Lovenox®) and the synthetic pentasaccharide heparin analog fondaparinux (Arixtra®) (Figure 2), which cannot be monitored by the existing near-patient clinical methods. We demonstrated the specificity of the antithrombin III functionalized sensor for the physiologically active pentasaccharide sequence. As a validation, we showed correlation of our measurements to those from a colorimetric assay for heparin-mediated anti-Xa activity. These results demonstrate that silicon field-effect sensors could be used in the clinic for routine monitoring and maintenance of therapeutic levels of heparin and heparin-based drugs and in the laboratory for quantitation of total amount and specific epitopes of heparin and other glycosaminoglycans.



▲ Figure 1: Optical micrograph of an array of silicon field-effect sensors for the detection of charged biomolecules such as heparin.



▲ Figure 2: Dose-response curve of the AT-III-sensor for the heparin-based pentasaccharide drug fondaparinux (•) and 6-O desulfated fondaparinux (○), which is known to exhibit low binding affinity for AT-III. Data points for fondaparinux fit with a Langmuir isotherm (solid line), and those for and 6-O desulfated fondaparinux are connected with a dashed line. Note that 0.2 U/mL ~ 1mg/ml ~ 50 nM.

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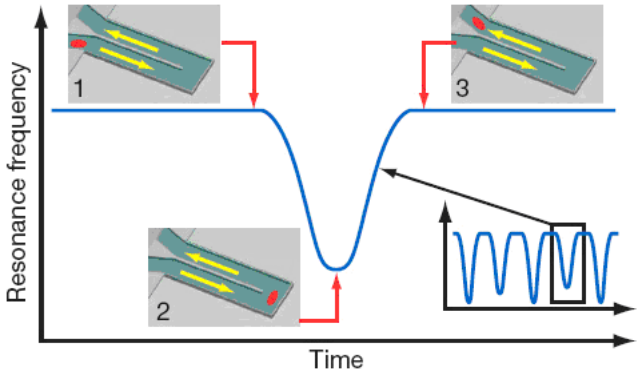
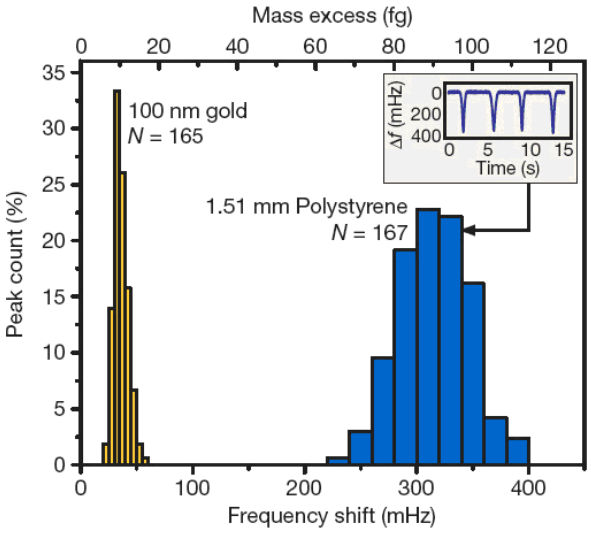
Weighing of Biomolecules, Single Cells and Single Nanoparticles in Fluid

T.P. Burg, M.Godin, W. Shen, G. Carlson, J.S. Foster, K. Babcock, S.R. Manalis
Sponsorship: NIH Cell Decision Process Center Grant, Institute for Collaborative Biotechnologies from the US Army Research Office, AFOSR

Nanomechanical resonators enable the measurement of mass with extraordinary sensitivity. Previously, samples as light as 7 zeptograms (1 zg = 10^{-21} g) have been weighed in vacuum, and proton-level resolution seems to be within reach. Resolving small mass changes requires the resonator to be light and to ring at a very pure tone—that is, with a high quality factor. In solution, viscosity severely degrades both of these characteristics, thus preventing many applications in nanotechnology and the life sciences where fluid is required. Although the resonant structure can be designed to minimize viscous loss, resolution is still substantially degraded when compared to measurements made in air or vacuum. An entirely different approach eliminates viscous damping by placing the solution inside a hollow resonator that is surrounded by vacuum (Figure 1). We have recently demonstrated that suspended microchannel resonators can weigh single nanoparticles (Figures 2), single bacterial cells. and sub-monolayers of adsorbed proteins in water with sub-femtogram resolution (1 Hz bandwidth). Central to these results is our observation that viscous loss due to the fluid is negligible compared to the intrinsic damping of our silicon crystal resonator. The combination of the low resonator mass (100 ng) and high quality factor (15,000) enables an improvement in mass resolution of six orders of magnitude over a high-end commercial quartz crystal microbalance [1]. This gives access to intriguing applications, such as mass-based flow cytometry, the direct detection of pathogens, or the non-optical sizing and mass density measurement of colloidal particles.



▲ Figure 1: A suspended microchannel translates mass changes into changes in resonance frequency. Fluid continuously flows through the channel and delivers biomolecules, cells. or synthetic particles. Sub-femtogram mass resolution is attained by shrinking the wall and fluid layer thickness to the micrometer scale and by packaging the cantilever under high vacuum. In one measurement mode, particles flow through the cantilever without binding to the surface, and the observed signal depends on the position of particles along the channel (inset 1 – 3). The exact mass excess of a particle can be quantified by the peak frequency shift induced at the apex.



▲ Figure 2: Synthetic particles of known size and density were measured to calibrate the mass sensitivity of the device. Gold nanoparticles (100 ± 8 nm) weighing 10 fg more than the water they displace produced a mean frequency shift of 36 mHz with a standard deviation of 6 mHz. On a different device, we measured a frequency shift of 310 ± 30 mHz for polystyrene microspheres (1.51 ± 0.01 um) with 90.1 fg mass excess.

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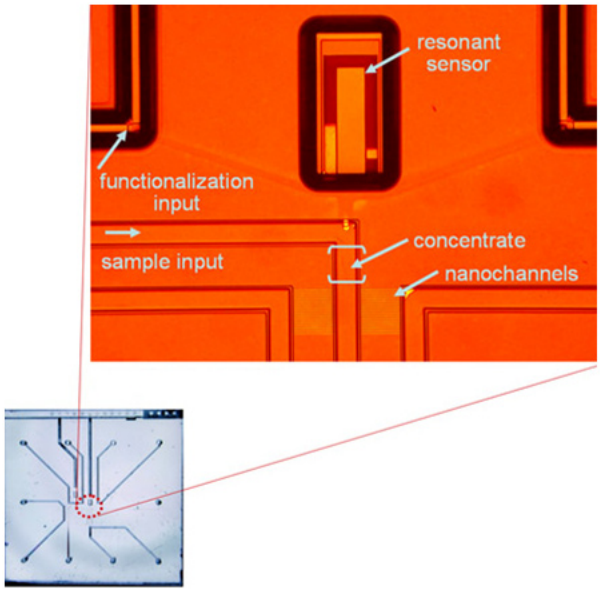
Integrated System for Cancer Biomarker Detection

P. Dextras, K. Payer, T. Burg, R. Chunara, Y.C. Wang, J. Han, S.R. Manalis
Sponsorship: NCI

There is evidence to suggest that the next generation of cancer-screening tests may employ not just one, but a small panel of less than ten biomarkers that together add statistical power to the detection of specific cancers. While immunoassays such as ELISA are well established for detection of antigen-based biomarkers, the fidelity of the assay is governed by the disassociation constant, K_d, of the antibody-antigen complex. If the antigen concentration is significantly below K_d, then the binding kinetics are slow and readout precision of the antigen-antibody complex can be degraded by noise.

We propose a general approach for improving the performance of ligand-receptor assays. The approach is based on a nanofluidic device that controllably concentrates a dilute sample and an ultra-sensitive suspended microchannel resonant mass sensor that detects specific biomarkers within the concentrate. Since the amplification (or gain) of the concentrator is adjustable, the dynamic range and detection limit of the immunoassay can be governed by the properties of the concentrator and not K_d. Since the integrated concentration/detection system is batch-fabricated by conventional foundry-level processing techniques, the cost per device could potentially be less than ten dollars.

Over the past year, we have fabricated the first generation of integrated systems (Figure 1). The devices appear to be functional based on initial visual inspections. We are currently validating the performance of the system by using quantum dots for a calibration assay. We are also in the process of validating the performance of the concentrator and mass sensor (as individual components) with prostate-specific antigen so that we can make comparisons to existing methods in terms of sensitivity and selectivity.



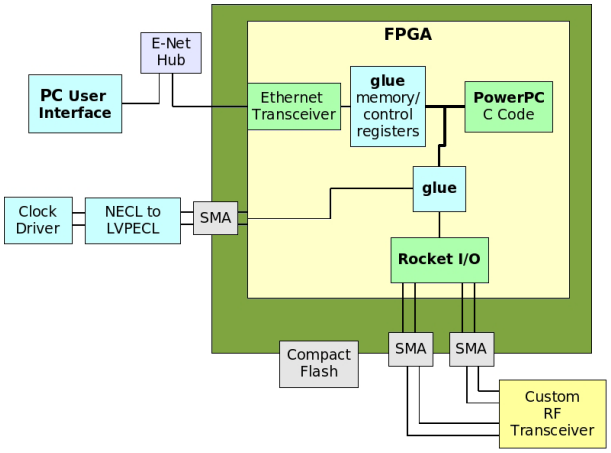
▲ Figure 1: Integrated system for concentration and detecting biomolecules.

Passive Microwave Transponders for Passive, Real-time, and High-sample-rate Localization

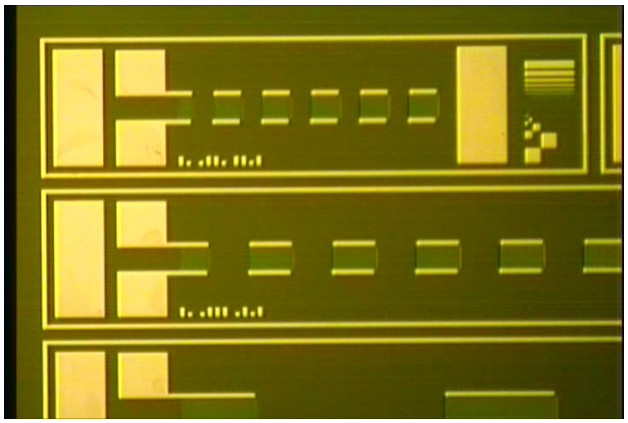
J. LaPenta, J. Paradiso
Sponsorship: Media Laboratory, NanoStructures Laboratory

Passive surface acoustic wave (SAW) transponders have been used for RFID applications because of their zero-power and long-range (100m) capabilities. This work presents current research into utilizing SAW transponders for localizing objects. The SAW transponders have many advantages over existing localization solutions, including small size (mm x mm), zero-power, high-accuracy, longer range (100m), and kilohertz update rates. Unhindered localization of objects is desirable for many applications, from human computer interaction to product tracking to security. The SAW transponders offer improvements to existing solutions for asset tracking, location of lost articles, ubiquitous computing, tracking of people with special needs or prisoners, workers in hazardous situations, human machine interfaces, virtual training environments, security, location of short-range mobile sensors, and biomedical research. The goal of this project is to prototype this tracking system and evaluate the feasibility of a commercial system.

Multiple RADAR measurement stations use phase-encoded chirps to selectively track individual SAW transponders by triangulation of range and/or angle measurements. Update rates on the order of 10kHz with accuracies better than $10cm^3$ are conceivable. A 300-nm deep-uv contact-mask lithography nanofabrication process to create these SAW devices is under development. Figure 1 shows the block diagram of the electronic test setup that is being used to characterize devices. Figure 2 shows a micrograph of a few of our fabricated devices. Recent results from this investigation will be presented, including the characterization of our first devices.



▲ Figure 1: Test electronics block diagram.



▲ Figure 2: The 3µm SAW devices.

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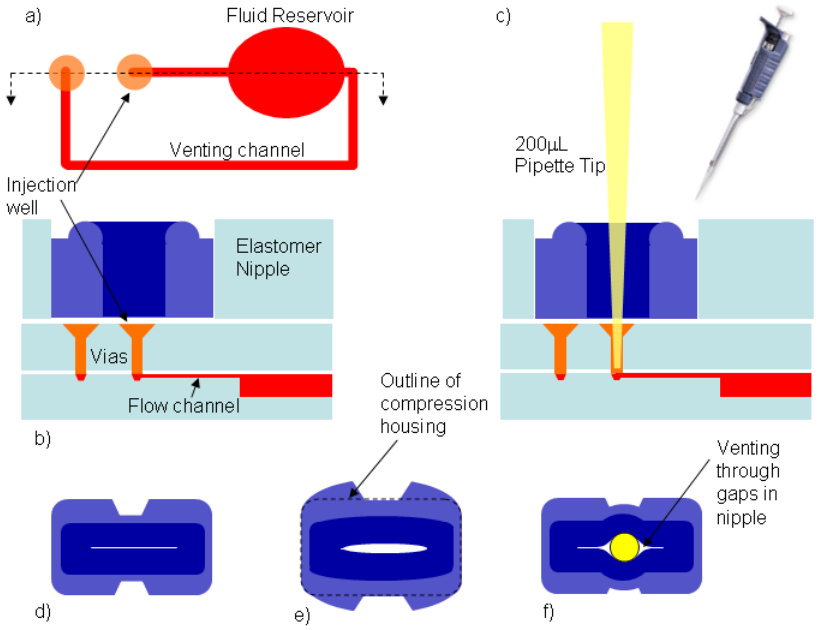
Macroscopic Interfaces to Parallel Integrated Bioreactor Arrays

H. Lee, R.J. Ram, P. Boccazzi, A. Sinskey
Sponsorship: Lincoln Laboratory

Macroscopic fluidic interfaces are important for improving the usability of microfluidic devices. For example, in our previously developed parallel integrated bioreactor arrays [1], two needle punctures were required to fill each fluidic reservoir, one for fluid injection using a syringe and another needle to vent the air displaced by the injected fluid. While suitable for internal laboratory use, such an inconvenient fluid injection procedure impedes the adoption of this new bioreactor technology.

We have developed a fluid injection port that automatically vents the displaced air and is compatible with standard laboratory pipette tips. The principle of operation is shown in Figure 1. On opposite sides of each fluid reservoir (Figure 1a), there is a fluid injection channel and a vent channel. Both of these channels terminate in vias that connect the channels to the seat of the pipette interface nipple. The pipette-interface-nipple (Figure 1e) is an elastomer structure, which, when compressed by its housing (Figure 1c), seals closed both vias such that fluid can neither escape nor enter the fluid reservoir. When a pipette tip is inserted into the interface-nipple, it is deformed and allows air to escape from the vent port (Figure 1f). Meanwhile, the inserted pipette tip seals to the via connected to the fluid injection channel and fluid can be injected into the reservoir. The particular bow-tie shape of the pipette-interface-nipple was chosen such that when it is inserted into a rectangular housing, sufficient compressive force would seal the central slit closed while also allowing space for the nipple to expand upon insertion of the pipette tip.

Fabricated devices exhibited good operating characteristics and provided a seal against a greater-than-10psi back pressure.



▲ Figure 1: Auto-venting and pipette compatible fluid injection port. a) Schematic view of an underlying microfluidic device with channels and a fluid reservoir. b) Cross-section showing device layers along with interface nipple and compression housing. c) Cross-section with inserted pipette tip. d) Interface-nipple inside compression housing; slit is sealed. e) Uncompressed, as-fabricated, interface nipple. Dotted line indicates compression housing dimensions. f) Compressed interface nipple showing inserted pipette tip and consequent deformation of the nipple.

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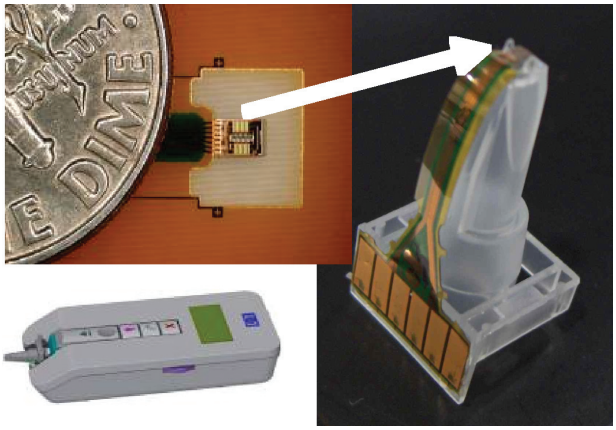
MIT-OSU-HP Focus Center on Non-lithographic Technologies for MEMS and NEMS

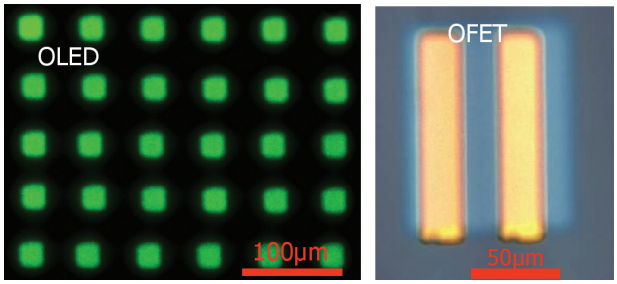
M.A. Schmidt (in coll. with S.G. Kim, C.G. Sodini, V. Bulović, MIT; D. Keszler, J. Wager, M. Subramanian, OSU; P. Benning, M. Chaparala, J. Stasiak, J. Thompson, Hewlett-Packard)
Sponsorship: AFOSR

This newly formed center is part of an overall set of centers on MEMS/NEMS fundamentals supported by DARPA. The MIT-OSU-HP Focus Center aims to develop new methods for fabrication of MEMS and NEMS that do not use conventional lithographic methods. The Center leverages the leading expertise of MIT and OSU in MEMS and printed devices, with the printing expertise of HP. The focus center is organized into four primary areas: tools, materials and devices, circuits, and demonstration systems.

In the area of tools, we are leveraging the existing thermal inkjet (TIJ) technology of HP and augmenting it with specific additional features, which expand the palette of available materials for printing. We are developing materials and devices over a broad spectrum from active materials, photonic and electronic materials, to mechanical materials. In the circuits area, we are studying the behavior of the devices that can be realized in this technology with the goal of developing novel circuit architectures. Lastly, we intend to build several "demonstration" systems that effectively communicate the power of the new technologies that will emerge from this center.



▲ Figure 1: An HP TIPS system for direct printing of a wide range of MEMS and electronic/photonic materials.



▲ Figure 2: Examples of printed optical and electronic devices.

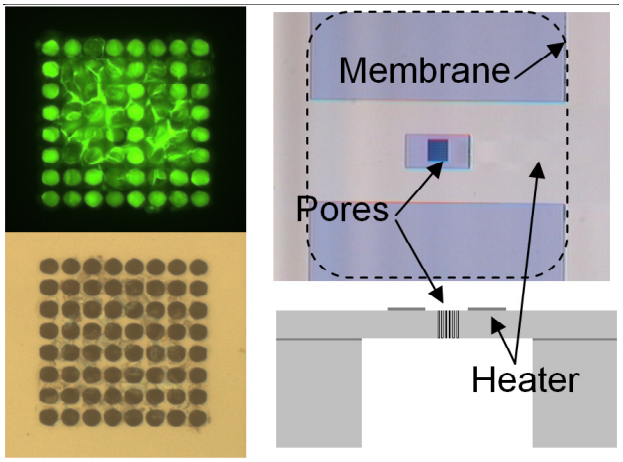
A Micromachined Printhead for the Evaporative Printing of Organic Materials at Ambient Pressure

V. Leblanc, J. Chen, P. Mardilovich, V. Bulović, M.A. Schmidt
Sponsorship: Hewlett-Packard, DARPA

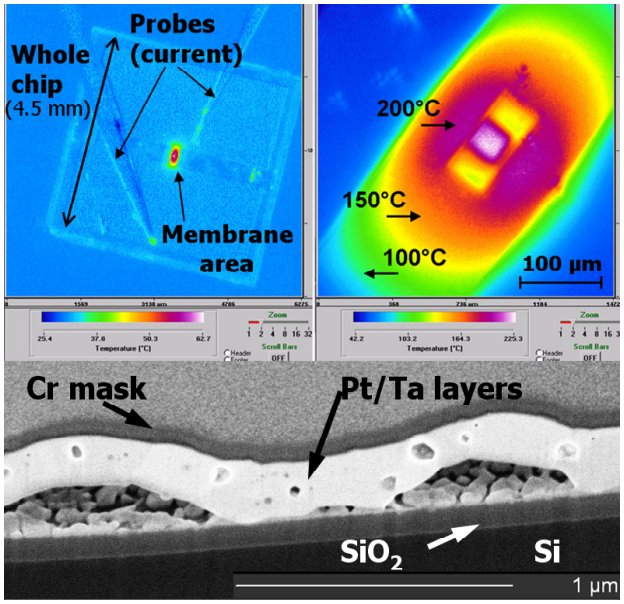
Organic optoelectronic devices are promising for many commercial applications if methods for fabricating them on large-area, low-cost substrates become available. Our project investigates the use of MEMS in the direct patterning of materials needed for such devices. By depositing the materials directly from the gas phase, without the liquid phase coming in contact with the substrate, we aim at avoiding the limitations due to inkjet printing of such materials.

We developed a MEMS-enabled technique for evaporative printing of organic materials. This technique does not require a vacuum ambient, has a fast printing rate (1 kHz), and can be scaled up to an array of individually addressable nozzles. The MEMS printhead comports a microporous layer with integrated heaters for local evaporation of the materials. Figure 1 shows the microfabricated device: an array of 2 micron pores and an integrated thin film platinum heater sit in the center of a silicon membrane. The material to be printed is delivered to the porous region in liquid or gas phase and deposits inside the pores (see Figure 1, top left). The integrated heater then heats up the porous area (see Figure 2, top) and the material is re-evaporated from the pores onto the substrate. The main limitation of this printhead is the failure of the thin-film platinum heater at temperatures above 800°C (see Figure 2 bottom).

This printhead was used, together with inkjet technology for the delivery of material to the pores, to print molecular organic semiconductors (see other abstract in this volume). Our technique enables printing of organic optoelectronics over large areas and can be used to print on a variety of substrates, does not require a vacuum ambient, and thus could enable low-cost printing of optoelectronics.



▲ Figure 1: Left: Pictures of the pores. Top: Fluorescent image after Alq3 material was loaded in the pores. Bottom: Optical image after re-evaporation of the material. Right: Top view and schematic of device.



▲ Figure 2: Top: Infrared microscope measurements of the temperature of a printhead chip. Bottom: An SEM image of a Focused Ion Beam cross-section of a failed heater.

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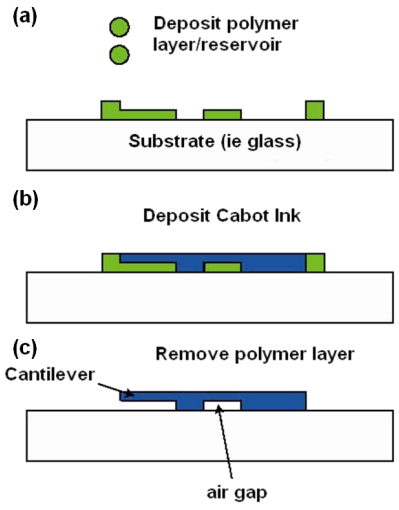
Surface Micromachining Processes using Non-lithographic Technologies

E.W. Lam, V. Leblanc, J. Chen, V. Bulović, M.A. Schmidt
Sponsorship: DARPA, Hewlett-Packard

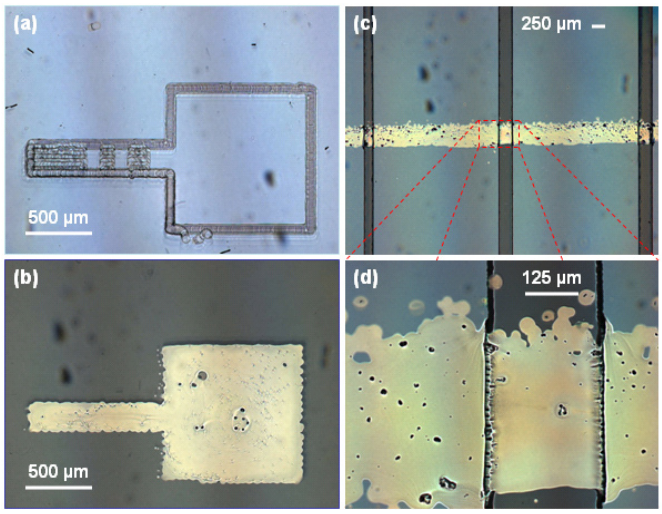
Conventional MEMS fabrication relies heavily on planar lithography and IC technology. While these techniques are well-suited for relatively flat devices such as the semiconductors, they are drastically limited in the design and fabrication of three-dimensional devices such as MEMS. From a commercial viewpoint, the semiconductor paradigm is also a poor fit for MEMS because the lower volume and demands make it more difficult to offset the high production costs. Ridding MEMS fabrication of its reliance on such techniques may introduce several advantages, namely a wider base of substrate materials and decreased costs.

Our project investigates severing MEMS fabrication from the semiconductor paradigm via non-lithographic technologies. We have previously shown how MEMS can be used for the direct patterning of small molecular organics [1]. Using similar concepts, we intend to show that surface micromachining can also be achieved.

The first stage of the project is to directly pattern a structural layer over a spacer and successfully release a cantilever. We have successfully patterned metal silver over various spacer materials, including polyethylene glycol (PEG), polyvinyl acetate (PVA), and UNITY™ sacrificial polymer, and we are currently working on the release process. This technique will ultimately be used to construct simple structures, such as cantilevers and bridges, to test the structural material's mechanical properties. The next stage of this project will consist of using this process to fabricate cantilevers and integrate them with other non-lithographic techniques to fabricate an accelerometer. Subsequent stages will consist of creating a library of non-lithographic processes so that entire MEMS devices can be fabricated without the use lithography.



▲ Figure 1: Basic approach of direct surface micromachining. (a) Spacer layer (green) is deposited. (b) Metal silver ink (blue) is deposited and sintered. (c) Spacer material is removed to release structure.



▲ Figure 2: Experimental results of directly processing spacer or structural materials. (a) Spacer material patterned as a reservoir with raised features. (b) Metal silver deposited in shape of reservoir (no spacer underneath). (c) Silver deposited over patterned photoresist (PR) lines. (d) Magnified view of silver over PR line.

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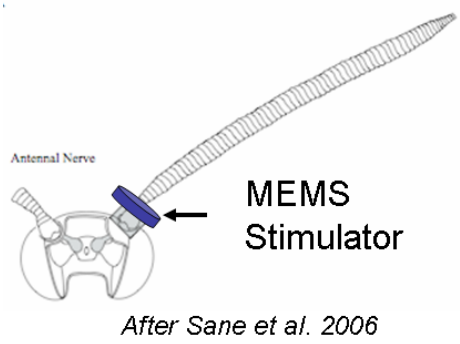
Micromechanical Actuators for Insect Flight Mechanics

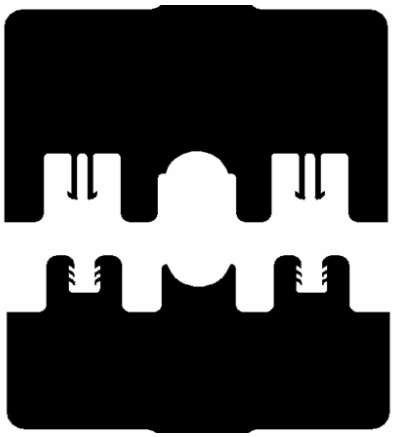
H. Zhou, M.A. Schmidt (in coll. with T.L. Daniel, University of Washington)
Sponsorship: AFOSR

This project aims to develop MEMS actuators to aid in the study of insect flight mechanics. Specifically, we are developing actuators that can stimulate the antennae of the crepuscular hawk moth *Manduca Sexta*. The possible mechanosensory function of antennae as airflow sensors has been suggested [1], and recent discoveries of our collaborators reveal that mechanosensory input from the antennae of flying moths serves a similar role to that of the hind wings of two-winged insects, detecting Coriolis forces and thereby mediating flight stability during maneuvers [2]. Early evidence suggests that mechanical stimulus of the antennae may enable flight control. In addition, the crepuscular hawk moth *Manduca Sexta* has a wide wingspan (~110 mm) and is capable of carrying at least one quarter of its own weight. Thus, studying the flight of *M. Sexta* by attachment of microsystems seems plausible. The goal of our project is to design and fabricate micromechanical actuators, which will be mounted onto the moth antennae (Figure 1). Our collaborators will study the flight control mechanism by mechanical stimulation.

Our first step is to fabricate "dummy" silicon rings for our biologist collaborators for implant experiments. The diameters along the antenna vary from tip to base, being thickest in the middle. As a result, in order to prevent the ring's being thrown off, the mounting of the silicon ring onto the base cannot be as simple as pushing it from the tip with a large inner hole. On the other hand, the sizes of the antennae vary from moth to moth. Two-piece construction was designed and fabricated to be like a "zip strip" to meet the mounting requirements (Figure 2). Future work will focus on refining the design and fabrication of the mounting kit and integrating actuators into it. To generate adequate displacement, strain amplification will be needed, such as reported by Conway, et al. [3].



▲ Figure 1: Schematic view of mechanical actuators for hybrid insects MEMS.



▲ Figure 2: "Zip-strip-" like mounting kit for *M. Sexta* moth antennae.

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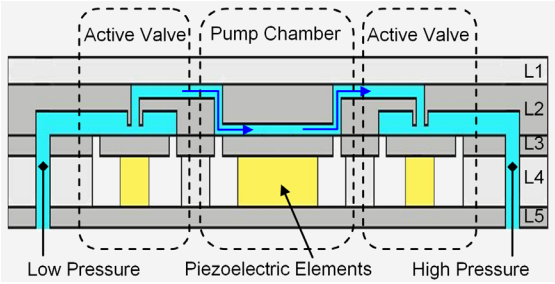
MEMS Micro-vacuum Pump for Portable Gas Analyzers

V. Sharma, M.A. Schmidt
Sponsorship: DARPA

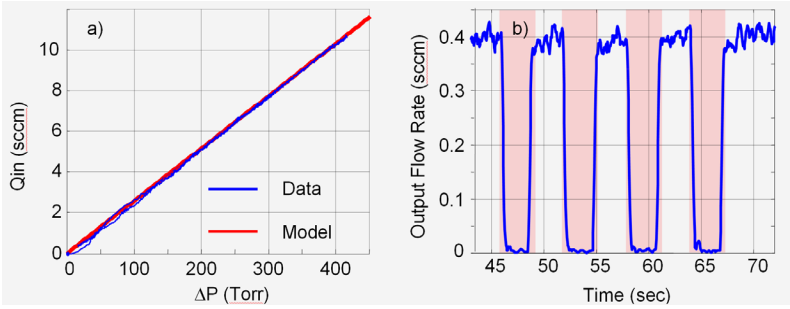
There are many advantages to miniaturizing systems for chemical and biological analysis. Recent interest in this area has led to the creation of several research programs, including a Micro Gas Analyzer (MGA) project at MIT. The goal of this project is to develop an inexpensive, portable, real-time, and low-power approach for detecting chemical and biological agents. Elements entering the MGA are first ionized, then filtered by a quadrupole array, and sensed using an electrometer. A key component enabling the entire process is a MEMS vacuum pump, responsible for routing the gas through the MGA and increasing the mean free path of the ionized particles so that they can be accurately detected.

There has been a great deal of research done over the past 30 years in the area of micro pumping devices [1, 2]. We are currently developing a displacement micro-vacuum pump that uses a piezoelectrically driven pumping chamber and a pair of piezoelectrically driven active-valves; the design is conceptually similar to the MEMS pump reported by Li et al. [3]. We have constructed an accurate compressible mass flow model for the air flow [4] as well as a nonlinear plate deformation model for the stresses experienced by the pump parts [5]. Using these models, we have defined a process flow and fabricated three generations of the MEMS vacuum pump over the past year and are currently working on the fourth.

A schematic of the pump is shown in Figure 1. For ease in testing we have initially fabricated only Layers 1-3 and have constructed a testing platform that, under full computer control, drives the pistons and monitors the mass flows and pressures at the ports of the device. The lessons learned from the first three generations of the pump have led to numerous improvements. Every step from the modeling to the etching and bonding to the testing has been modified and improved along the way. The most recent third generation pump test data is shown in Figure 2. Figure 2a shows the pressure versus flow rate characteristics of the pump; note that the data compares very well with models. Figure 2b shows the output flow rate versus actuation characteristics of the pump. Notice that the flow goes to zero each time the piston is actuated upwards (red bar). All three pistons demonstrated similar performance illustrating a pump with fully functioning pistons and tethers. Next, we hope to characterize the pumping characteristics of this and the upcoming fourth-generation pumps.



▲ Figure 1: Schematic of the MEMS Vacuum Pump. Layers 1 and 4 are glass, Layer 2 forming the chambers and channels is DSP silicon, Layer 3 forming the pistons and tethers is SOI silicon, and Layer 5 is SSP silicon.



▲ Figure 2: a) Pressure versus flow rate characteristics of the pump compares very well with models (ΔP = input pressure – output pressure). b) Output flow rate versus actuation characteristics of the pump. Notice that the flow goes to zero each time the piston is actuated upwards (actuation indicated by transparent red bar).

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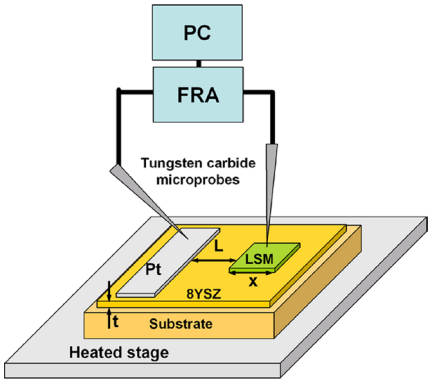
Microfabricated Electrodes for Solid Oxide Fuel Cells

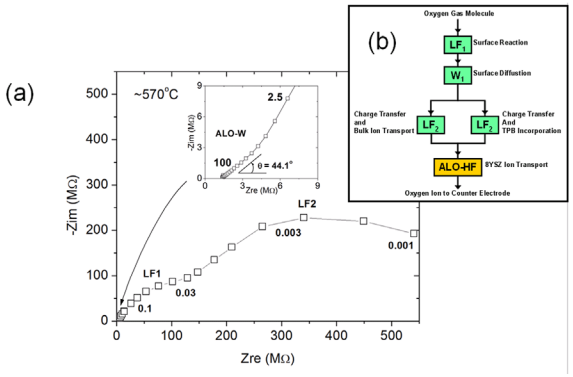
G.J. la O', Y. Shao-Horn
Sponsorship: Ford-MIT Alliance, NSF, CMSE

The solid oxide fuel cell (SOFC) is an energy-conversion device that produces electricity directly through the electrochemical reaction of hydrogen (H_2) and oxygen (O_2). The SOFC also allows utilization of hydrocarbons, such as methane (CH_4), via internal reforming or direct electrochemical oxidation, giving these systems the flexibility of using a variety of commercially available fuels. The high energy-density of hydrocarbon fuels makes the SOFC attractive for large-scale stationary systems and as a replacement to batteries for powering portable electronic devices. Standard SOFCs operate in the temperature range of 800°C-1000°C and have an open circuit voltage of approximately 1-volt. The most common SOFC materials are yttria-stabilized zirconia (YSZ) for the electrolyte, strontium-doped lanthanum manganite (LSM) for the cathode and nickel (Ni)-YSZ for the anode. Although elevated temperature operation allows the use of non-noble metal catalysts and excellent high-grade heat exhaust to be used for additional power generating cycles, there are numerous advantages to lowering the SOFC operating temperature to around 600°C. Benefits such as lower thermal stress, reduced cell degradation, utilization of metallic components, and shorter startup times are a few. However, at these lower temperatures the poor electrochemical activity of the electrodes, in particular the LSM cathode, leads to unacceptable voltage losses that lower the efficiency and performance of the SOFC.

Oxygen reduction mechanisms on the perovskite material $La_xSr_{1-x}MnO_{3-d}$ (LSM) has been widely studied; however, no final conclusion on the molecular level mechanisms for oxygen reduction has been made. To probe the oxygen reduction reaction, we fabricate electrodes with precise geometries (50-200 μm) using thin-film deposition techniques (sputtering and laser ablation) and subsequent photolithography to investigate the fundamental electrode mechanisms and rate-determining reactions. The electrochemical impedance spectroscopy (EIS) response of a $La_{1-x}Sr_xMnO_{3-d}$ (LSM) microelectrode on 8YSZ is then analyzed as a function of geometry and temperature using a microprobe station equipped with a high temperature stage, as Figure 1 shows. Our preliminary EIS results[1] shown in Figure 2a show at least four distinct reaction processes for oxygen reduction on LSM/8YSZ: (i) ion transport in 8YSZ with average activation energy (E_a) of 1.16±0.02eV, (ii) surface diffusion on LSM with E_a ranging from 1.34±0.05eV to 1.65±0.03eV, (iii) at least one surface chemical process on LSM with E_a ranging from 1.71±0.02eV to 1.88±0.02eV and an average capacitance $3.4x10^{-4}$ F/cm^2, and (iv) a mixed bulk/TPB charge transfer process with E_a ranging from 2.42±0.02eV to 3.05±0.03eV and an average capacitance of $3.2x10^{-3}$ F/cm^2. The overall oxygen reduction process is illustrated in Figure 2b, with the rate-limiting reaction for ORR found to be from mixed bulk/TPB charge transfer processes below 700°C and shifts to surface chemical reactions above 700°C.



▲ Figure 1: Electrochemical impedance spectroscopy configuration for microfabricated SOFC cathodes (LSM) tested using a microprobe station with high temperature stage.



▲ Figure 2: Nyquist plot of typical impedance response from LSM microelectrodes on 8YSZ at 570°C in air showing ALO-HF, ALO-W, LF1 and LF2 features that are correlated to 8YSZ ion transport, LSM surface diffusion, surface reaction, and tpb/bulk process, respectively.

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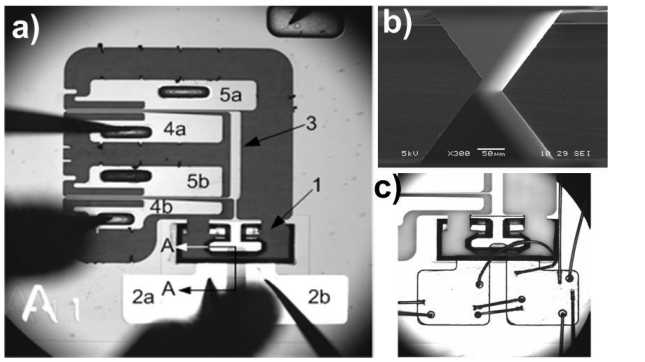
[1] G.J. la O', B. Yildiz, S. McEuen, and Y. Shao-Horn, "Probing oxygen reduction reaction kinetics of Sr-doped $LaMnO_3$ supported on yttria stabilized zirconia: An electrochemical impedance study of dense, thin-film microelectrodes," *Journal of the Electrochemical Society*, vol. 154, no. 4, pp. B427-B438, Apr. 2007.

A MEMS-relay for Power Applications

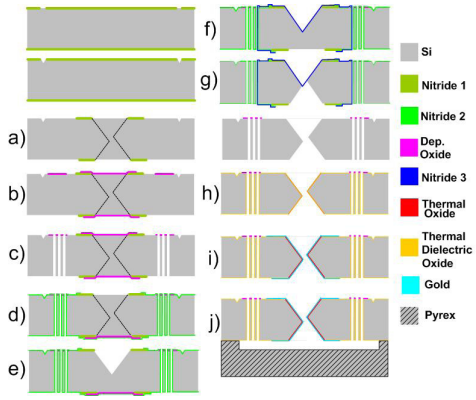
A.C. Weber, J.H. Lang, A.H. Slocum
Sponsorship: NSF Collaborative Research: Atomic Plane Electrical Contacts

Contact travel and heat dissipation are important requirements of electrical power switching devices such as MEMS-relays and MEMS-switches. Whereas low-power MEMS-based RF switches have been vigorously studied, few studies have been reported on high-power MEMS-relays. This paper presents a MEMS-relay for power applications. The device is capable of make-break switching; has large contact travel, on the order of 10's of μm; and has low contact resistance, on the order of 120 mΩ. Testing has demonstrated current carrying capacity on the order of several amperes and hot-switching of inductive loads, on the order of 10mH, without performance degradation.

The MEMS-relay, shown in Figure 1a, is bulk micromachined in (100) silicon and bonded to a glass substrate. Anisotropic etching is used to fabricate the oblique and parallel (111) contact surfaces, having nanometer-scale surface roughness [1]. Figure 1b shows a cross section of the open fabricated contacts. An offset between the wafer-top and the wafer-bottom KOH masks produces the contact geometry shown. The silicon contact metal surfaces are created by evaporation and electroplating with a conductive film, shown in Figure 1c. A thermal oxide layer provides insulation between the actuators and the contacts. Deep reactive ion-etching (DRIE) is used to pattern a parallelogram-flexure compliant mechanism and a pair of rolling-point "zipper" electrostatic actuators [2]. Nested masks are used to pattern both wafer-through etches. Figure 2 illustrates the process used to fabricate the device.



▲ Figure 1: Device after fabrication. Die top view (a), contact cross section A-A of oblique contacts as shown in Figure 1a (b), contact electroplating (c).



▲ Figure 2: Fabrication Process. Nitride mask for KOH-etch (a), sacrificial oxide (b), DRIE (c), nitride passivation; patterning with shadow wafer (d), top KOH-etch (e), nitride passivation (f), bottom KOH-etch (g), dielectric oxide growth (h), metallization (i), bonding (j).

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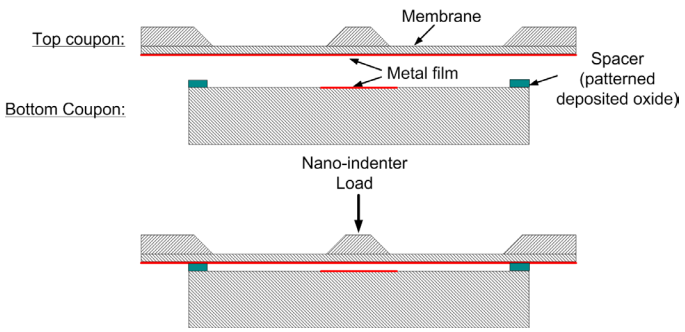
A Silicon-etched, Electrical-contact Tester

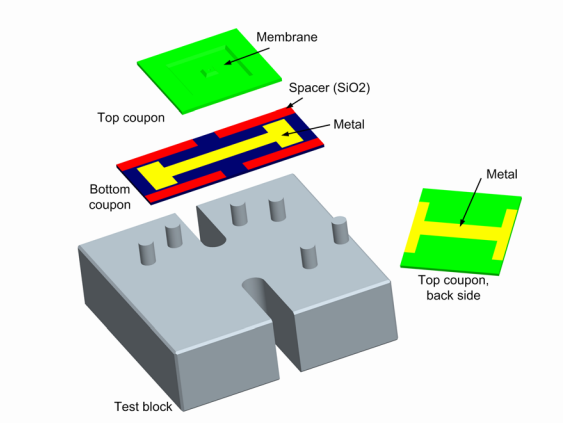
A.C. Weber, A.H. Slocum, J.H. Lang
Sponsorship: NSF Collaborative Research, Atomic Plane Electrical Contacts

We are developing a bulk micromachined contact tester to investigate the electro-tribological performance of micro- and nano-structured planar electrical contacts [1]. The test device features parallel, planar, nanometer-scale surface roughness contacts etched in silicon coated with thin conductive films. Contacts used in microsystems, probes and interconnects are subject to heat dissipation and to electro-mechanical tribological effects. With an understanding of how nanoscale surface and subsurface material structure affect electrical contact resistance and mechanical contact wear, a deterministic manufacturing process could be developed to design electrical contacts from crystalline plane surfaces as potential high performance contacts for MEMS devices and related applications.

The microfabricated contact tester, shown in Figure 1 and in Figure 2, consists of a pair of parallel planar contact surfaces with nanometer roughness patterned onto two (100) Si substrates. Anisotropic etching is used on one of the substrates to create a membrane that serves as a compliant mechanism for the contact tester. A thin conductive film, i.e., Au, is patterned onto the contacts in a Kelvin configuration. The two-piece tester architecture allows for inspection of the contacts before, during, or after testing without destruction of the test device. In one embodiment of the tester, a quasi-kinematic coupling enables the alignment between the substrates while providing the initial gap between the contacts. Similar quasi-kinematic designs fabricated in silicon substrates have reported repeatability on the order of 1 micrometer [2]. In a second embodiment of the MEMS-tester a patterned oxide film is used to provide the initial space between the contacts. The tester will be loaded using a commercial nanoindenter to bring the surfaces into contact as contact resistance is measured as a function of the force.



▲ Figure 1: Schematic view of the contact tester.



▲ Figure 2: Exploded view of the contact tester. The back side of the top coupon indicates the patterned metal used for the Kelvin contact configuration.

REFERENCES

[1] A.C. Weber, G. Bassiri, B.M. Dvorak, A.H. Slocum, D.A. Lucca, and J.H. Lang, "Atomic Plane Electrical Contacts", in *Proceedings of the 7th European Society of Precision Engineering (EUSPEN) International Conference*, Bremen, Germany, May 2007

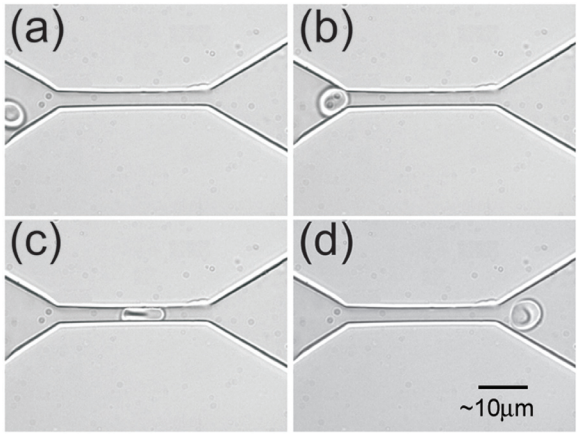
[2] A.H. Slocum and A.C. Weber, "Precision passive mechanical alignment of wafers," *Journal of MEMS*, vol. 12, no. 6, pp. 826-834, Dec. 2003

Microfluidic Studies of Biological Cell Deformability and Rheology

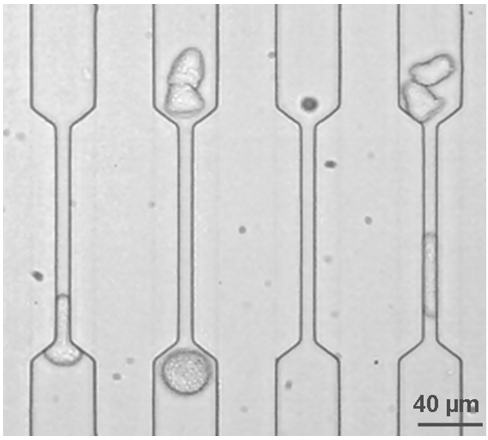
D. Quinn, S. Navlakha, N. Walter, A. Micoulet, S. Suresh
Sponsorship: Singapore-MIT Alliance, NSF

It is well known that many hereditary or infectious diseases, as well as certain types of cancer, produce alterations in mechanical properties of human cells. In certain diseases, such as malaria, infected cells exhibit reduced deformability and increased cytoadherance. Such changes alter the circulatory response of red blood cells (RBCs) and limit physiological responses to such diseases, such as splenic clearance of parasitized RBCs, and restrict circulation of RBCs in the microvasculature. In other diseases, such as pancreatic cancer under certain conditions, cancerous cells may exhibit enhanced deformability, which may contribute to an increased probability of metastasis.

Several projects in the Suresh research group aim to utilize microfabricated structures to experimentally evaluate the circulatory response of diseased human cells. In these studies, microfabricated channels of polydimethylsiloxane (PDMS) are used in conjunction with a fluidic system and a high-speed camera to quantify the biorheological behavior of cells under different conditions. In the case of diseases involving RBCs, cells are made to pass through a narrow (~3 micrometer square) channel under a known pressure differential. During this process, shown in Figure 1, the average velocity and characteristic entrance and exit and shape recovery times are indicative of the overall biorheological response of the cell during microcirculation. Current results indicate large differences in rheological behavior of cells of different ages and incubation times. In addition, initial results from Plasmodium falciparum parasitized RBCs indicate a possible effect of exported proteins from the malaria-inducing parasite to the surface of the RBC membrane on the rheological behavior of RBCs. Similar experiments are also being conducted on pancreatic cancer cells (Panc-1), as seen in Figure 2. In these cells, the biorheology of cells is assessed in environments similar to those experienced during metastasis. Future work with these systems will aim to further identify particular proteins or biochemical interactions that affect the biorheolgical and circulatory behavior of diseased cells with the aim of developing enhanced understanding of the mechanisms of disease progression and possible avenues for treatment.



▲ Figure 1: An experimental *in vitro* demonstration of the "fluidization" of a healthy human RBC through a microfluidic channel at room temperature. The series of images show the shape of an RBC as it is squeezed through a 4 µm x 4 µm channel, made of polydimethylsiloxane (PDMS), under a pressure differential of 1-2 mm of water at approximately 0.4 seconds/frame. Note the recovery of shape upon egress from the channel.



▲ Figure 2: Pancreatic cancer cells (Panc-1) passing through narrow constrictions. The cells pass through 8µm x 18µm PDMS channels under an applied flow rate of ~0.5 ul/min and an approximate pressure differential of 4kPa.

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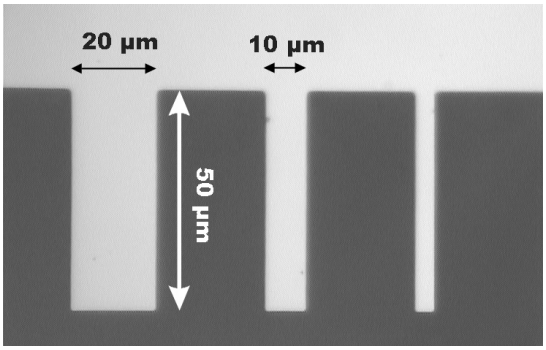
Phase Change Materials for Actuation in MEMS

J.A. Kalb, Q. Guo (Singapore-MIT Alliance), X.Q. Zhang (National University of Singapore), C.H. Sow (National University of Singapore), Y. Li (National University of Singapore), C.V. Thompson
Sponsorship: Alexander von Humboldt Foundation, Singapore-MIT Alliance

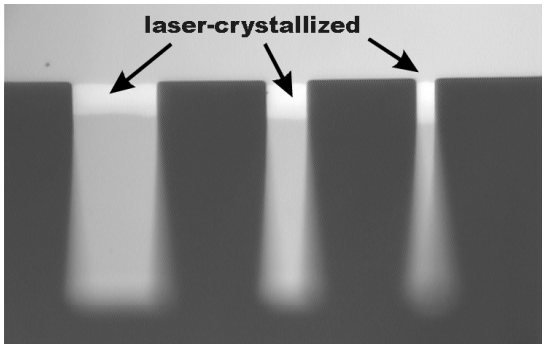
Phase change materials (Sb and Te alloys) are used for optical data storage in commercial phase change memories, such as rewritable compact discs (CD±RW) and rewritable digital video disks (DVD±RW, DVD-RAM) [1]. Recently, they have also shown high potential for the development of phase change random access memories (PC-RAMs or PRAMs), which might replace flash memories in the future [2]. In this project, thin films of phase change materials are systematically analyzed with regard to their transformation behavior under laser-induced amorphization and crystallization. The goal of this project is to gain a better understanding of the relationship among the laser parameters, the material-specific transformation kinetics, and the involved volume changes (and associated mechanical stresses) over a wide range of alloy compositions.

The approach to pursuing this goal is to use microfabricated SiN cantilevers as substrates for thin film deposition: The SiN cantilevers are manufactured by chemical vapor deposition of low-stress SiN on Si wafers, patterning the SiN film using optical lithography and revealing the cantilevers using dry etching and wet etching. Thin films of phase change materials are subsequently sputter-deposited on these SiN cantilevers and are locally switched by laser heating from the amorphous to the crystalline phase (and vice versa). The associated stresses induce a cantilever bending, which is measured by optical microscopy and non-contact interferometry as a function of laser annealing parameters, laser quench rate and alloy composition (Figures 1 and 2). Additionally, amorphous films are hot-stage crystallized, which allows the study of the kinetics associated with the crystallization process as well as the force associated with the cantilever bending.

The results of this project will help to increase the number of write-erase cycles and the data transfer rate in phase change memories and may lead to other applications of phase change materials in MEMS actuation.



▲ Figure 1: Optical micrograph of SiN cantilevers fabricated by optical lithography and dry/wet etching. An amorphous $Ge_2Sb_2Te_5$ film has been deposited on top.



▲ Figure 2: The $Ge_2Sb_2Te_5$ film has been crystallized with a scanning HeNe laser near the support of the cantilevers. As a consequence, the reflectivity increases and the cantilever end moves up by about 7.5 µm, which reveals the laser-induced strain and stress in the film.

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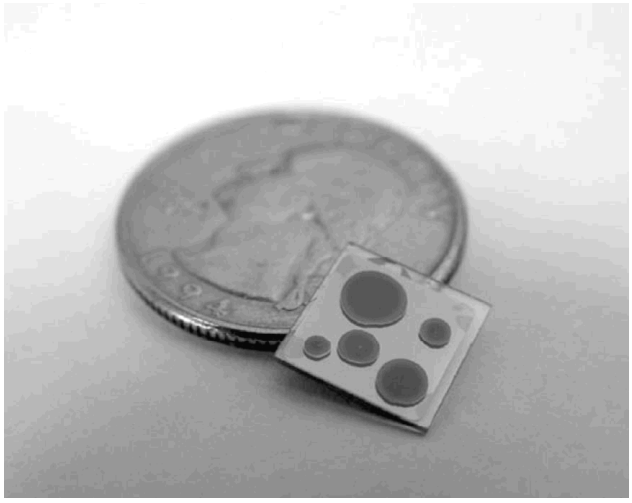
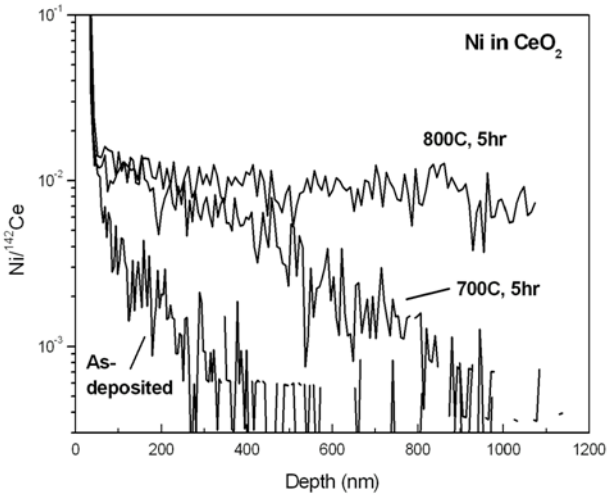
Microfabricated Thin-film Electrolytes and Electrodes for Solid Oxide Fuel Cells

J.L. Hertz, S.J. Litzelman, W.C. Jung, W.S. Kim, A. Rothschild, H.L. Tuller (in coll. with K.F. Jensen, B.L. Wardle, M.A. Schmidt, E. Ivers-Tiffee, D. Gerthsen, U. Karlsruhe; M. Martin, R. DeSousa, U. Aachen)
Sponsorship: DOD MURI, NSF, DOE

There is growing interest in the microfabrication of electrodes for solid oxide fuel cells (SOFCs) in microionic devices [1]. Recently, we reported the fabrication of Pt/(Zr,Y)O_2 (YSZ) nanocomposite electrodes by reactive magnetron co-sputtering [2]. Use of X-ray diffraction and X-ray photoelectron spectroscopy (XPS) characterization show these composites to be a two-phase system with no change of oxidation state from the constituent compounds. Electrical characterization via impedance spectroscopy demonstrated promising electrochemical properties at low temperatures; an area-specific resistance of 500 Ω cm^2 was achieved at 400°C. To test whether microfabricated thin-film electrolytes may suffer from degradation due to grain boundaries acting as short-circuiting diffusion pathways, sputtered NiO diffusion source films were in-diffused along grain boundaries into nanocrystalline CeO_2 thin films grown by pulsed laser deposition (PLD), at temperatures from 700-800°C. The diffusion profiles were measured by Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS) at the Institute for Physical Chemistry at RWTH Aachen University, Germany. These SIMS spectra, shown in Figure 2, point to a single diffusion mechanism, believed to be grain boundary diffusion, at these relatively low temperatures. Further work to systematically determine the unique opportunities and challenges associated with microstructured SOFCs is currently underway.



▲ Figure 1: Photograph of a Pt/YSZ composite microelectrode device fabricated by reactive magnetron sputtering. Five microelectrodes lie on the surface and the counter electrode is visible through the transparent YSZ substrate[2].



▲ Figure 2: The ToF-SIMS spectra of Ni diffusion in CeO_2. The as-deposited profile is shown, as are profiles resulting from anneals at 700 and 800°C for 5 hours. In the 800°C sample, Ni has diffused through the entire film.

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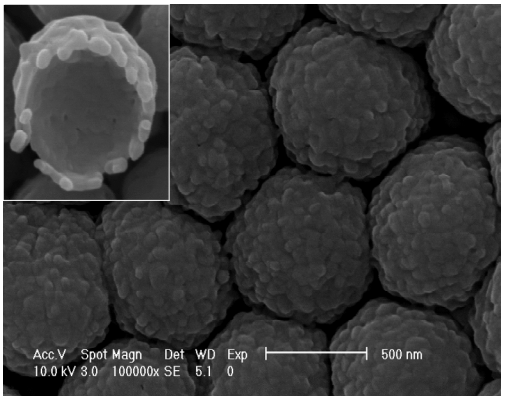
Nanowire- and Microsphere-templated Gas Sensors

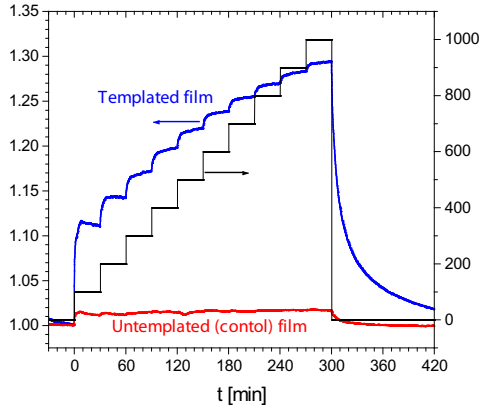
A. Rothschild, K. Sahner, G. Whitfield, H.L. Tuller (in coll. with I.D. Kim)
Sponsorship: NSF

Novel materials synthesis techniques were used to fabricate nanostructured and macroporous semiconducting metal oxide (SMO) films exhibiting exceptionally high sensitivity to reducing and oxidizing gases, as compared to conventionally prepared specimens. Increased sensitivity resulted from an elevated surface area and reduced specimen cross section. Several processing routes were pursued including electronspinning of semiconducting metal oxide (SMO) nanowires into a highly porous mat structure and microsphere templating followed by pulsed laser deposition (PLD) of macroporous SMO material onto the microsphere templates.

The TiO_2/poly(vinyl acetate) composite nanofiber mats were electrospun onto interdigitated Pt electrode arrays, producing a mesh of 200-500 nm sheaths filled with ~10 nm thick single-crystal anatase fibrils. Testing in the presence of NO_2 gas at 300°C demonstrated a minimum detection limit (MDL) of below 1 ppb[1]. Chemical and physical synthesis routes were combined to prepare macroporous $CaCu_3Ti_4O_{12}$ and TiO_2 thin films by PLD onto PMMA microsphere-templated substrates. Stable quasi-ordered hollow hemispheres with diameter and wall thicknesses of 800 nm and 100 nm, respectively, were obtained (Figure 1). Current-voltage and impedance spectroscopy measurements point to the crucial role played by grain boundary barriers in controlling the electrical properties of these films. The macroporous $CaCu_3Ti_4O_{12}$ films exhibited a much superior H_2 gas sensitivity (55ppm MDL) to non-templated films[2] (Figure 2), while macroporous TiO_2 films exhibit excellent NO_x sensitivity. Studies are continuing to more carefully correlate sensor response with SMO microstructure, morphology, and chemistry.



▲ Figure 1: Two SEM micrographs of the macroporous CCTO films. The inset in emphasizes the grain structure of the hemispheres.



▲ Figure 2: The resistance response of CCTO films deposited on templated (blue curve) and plain substrates (red curve) during exposure to increasing concentrations (between 100 and 1000 ppm) of H_2 in air.

REFERENCES

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BioMEMS for Control of the Stem Cell Microenvironment

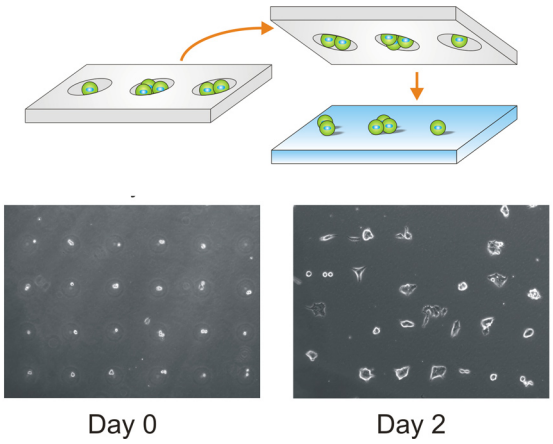
L. Kim, A. Rosenthal, S. Sampattavanich, A. Skelley, J. Voldman
Sponsorship: NIH

The stem cell microenvironment is influenced by several factors including cell-media, cell-cell, and cell-matrix interactions. Although conventional cell-culture techniques have been successful, they offer poor control of the cellular microenvironment. To enhance traditional techniques, we have designed a microscale system to perform parallel cell culture on a chip while controlling the microenvironment in novel ways.

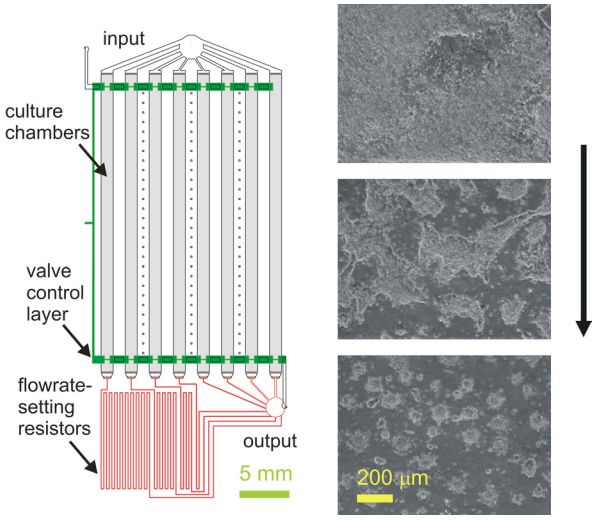
To control cell-matrix and cell-cell interactions, we use cell patterning. We have developed a simple cell-patterning technique (Figure 1 upper) that can pattern single cells onto arbitrary substrates [1]. Using this technique, we patterned clusters of mouse embryonic stem cells (mESCs) with different numbers of cells in each cluster (Figure 1 lower). We have also developed methods for single-cell patterning using dielectrophoresis (DEP), which uses non-uniform AC electric fields to position cells on or between electrodes [2].

To control cell-media interactions, we have developed a microfluidic device for culturing adherent cells over a logarithmic range of flow rates [3]. The device (Figure 2, left) controls flow rates via a network of geometrically-set fluidic resistances connected to a syringe-pump drive. We use microfluidic perfusion to explore the effects of continuous flow on the soluble microenvironment. We cultured mESCs in standard serum-containing media across a 2000× range of flow rates. On day 1, colony areas were roughly constant along the axis of perfusion, implying negligible nutrient depletion. However, by day 3, we observed a significant decrease in colony size along the axis of perfusion at mid-range flow rates (Figure 2, right). At higher flow rates, colonies were uniformly large along the axis of perfusion, implying that nutrient depletion was not significant above certain flow rates.

This microfabricated system will serve as an enabling technology that can be used to control the cellular microenvironment in precise and unique ways, allowing us to perform novel cell biology experiments at the microscale.



▲ Figure 1: The mESCs patterned onto tissue culture polystyrene and tracked over multiple days. The cells attach, proliferate, and move.



▲ Figure 2: Microfluidic 1×8 array of cell culture chambers for creating a logarithmic range of flow rates (left). The three photographs at the right show day 3 mESC colonies at upstream, middle, and downstream locations in a single culture channel. Colony size decreased along the axis of perfusion. Arrow indicates direction of flow (right).

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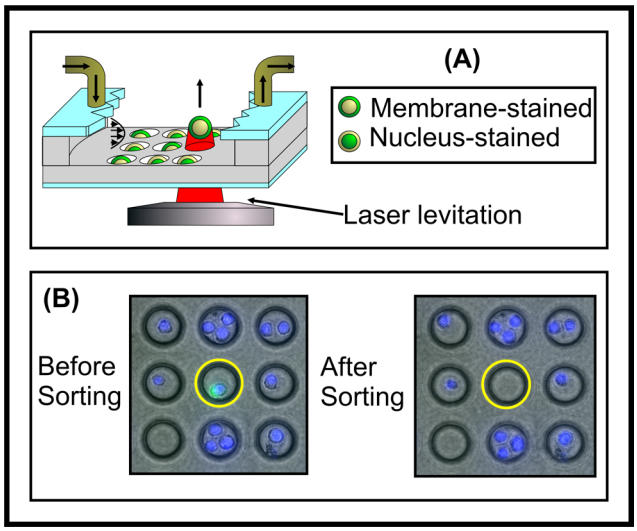
Microfabricated Devices for Sorting Cells Using Complex Phenotypes

S. Desai, J. Kovac, N. Mittal, B. Taff, J. Voldman
Sponsorship: NIH, DOD, Singapore-MIT Alliance

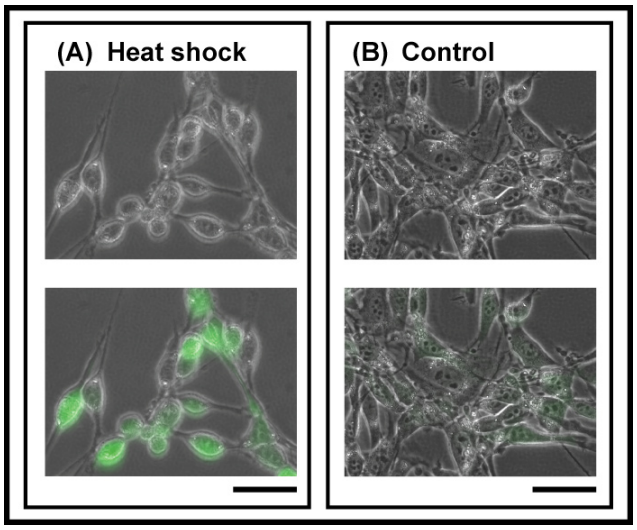
This research involves the development of numerous microfabricated sorting cytometer architectures for genetic screening of complex phenotypes in biological cells. Our various approaches combine the ability to observe and isolate individual mutant cells within surveyed populations. In this work we merge benefits of both microscopy and flow-assisted cell sorting (FACS) to offer unique capabilities in a single platform. Biologists will leverage these new affordances to isolate cells on the basis of observed dynamic and/or intracellular responses, enabling novel avenues for population screening.

Our most recent approach to image-based sorting, which complements our earlier work, utilizes a microfabricated array of PDMS microwell structures positioned in the floor of a microfluidic flow chamber (Figure 1) [1-2]. These microwells capture and hold cells in place for microscopy-based imaging, and can be optimized to trap single cells. After inspecting the array using microscopy to determine cells of interest, we apply radiation pressure from an infrared (IR) laser diode to levitate target cells out of the wells and into a flow stream. Released cells can be collected downstream for further analysis. The interconnect-free architecture scales easily; we have presently implemented trap arrays containing more than 10,000 sites.

Manipulating live cells, irrespective of the technique, will certainly have some effect on cellular behavior and physiology. It is imperative that we understand the effects of our sorting techniques (both optical and electrical) on cellular physiology over a range of operating conditions for two main reasons: (1) to determine whether there are any gross effects (such as viability and changes in proliferation), and (2) to determine whether there are more subtle effects that alter complex phenotypes of interest. To this end we are designing a microfabricated device to perform electrical and optical "dose responses" to determine optimal regions of operation and using fluorescence-based stress reporter cell lines as sensors of physiological state (Figure 2).



▲ Figure 1: Microwell-based optical sorting. (A) Schematic sort based on fluorescence localization (nucleus vs. cytoplasm). Laser levitates target cells into the flow stream for downstream collection. (B) Section of well array. We remove a membrane-stained cell from a population of purely nuclear-stained cells. We used an argon laser here; we now use IR-beams to mitigate cell-damage concerns.



▲ Figure 2: Sensing physiological state. (A) Green fluorescent protein (GFP) based stress reporter cell line which shows significant increase in fluorescence intensity, compared to control (B) after a 30-minute heat shock at 44ºC and a 14-hour recovery at 37ºC. Such a live cell sensor will allow us to perform fluorescence-based cell health assays on thousands of cells. Scale bars 20 μm.

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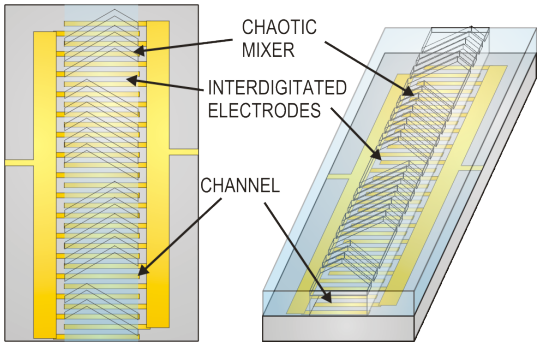
Combined Microfluidic/Dielectrophoretic Microorganism Concentrators

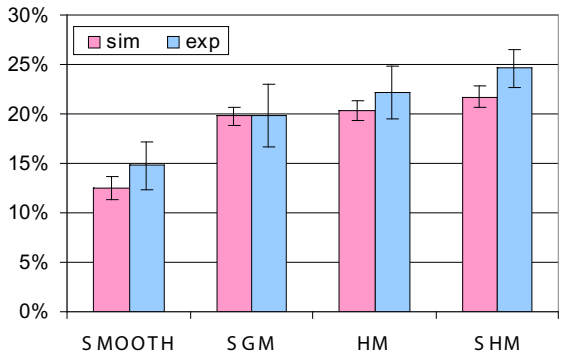
H.-Y. Lee, K. Puchala, J. Voldman
Sponsorship: NASA, Draper Labs

This project focuses on the development of microfabricated microfluidic/dielectrophoretic devices capable of concentrating micron-size particles from complex liquids. The concentrated particles of interest, such as pathogenic bacteria and spores, can then be delivered in small aliquots to the appropriate sensor for identification. Our micro-concentrator exploits the phenomenon of dielectrophoresis (DEP)–the force on polarizable particles in spatially non-uniform electric field [1]–to trap particles from the flow stream in order to subsequently concentrate them by release into a smaller volume of liquid. We create the non-uniform electric field using interdigitated electrodes (IDE) at the bottom of the flow channel (Figure 1).

To maximize the exposure of particles to the DEP field, we employ a passive microfluidic mixer to circulate the liquid (Figure 1). One question that arises is how to determine the optimal mixer geometry for circulating the liquid, which may differ from the ideal geometry for mixing two liquids. To answer this question we developed modeling tools and an experimental methodology to quantitatively predict the trapping behavior of particles in these systems. As Figure 2 shows, our modeling is able to predict the efficiency of different mixer configurations, without any fitting parameters. Among the four mixers tested (herringbone mixer (HM) slanted groove mixer (SGM), staggered herringbone mixer (SHM), and smooth channel (SMOOTH)), the HM and SHM perform similarly. This result is unexpected, as the HM is known to be a poor mixer of two liquids, while here we show that it is fine for circulating one liquid [2].



▲ Figure 1: Device overview. Illustration of the assembled devices, showing the PDMS channel and gold interdigitated electrodes (IDEs) on the Pyrex substrate.



▲ Figure 2: Comparison of simulated and experimental trapping efficiency. The fabricated devices have 16-µm wide electrodes with 24-µm spacing and a groove-to-channel aspect ratio of 0.22 (SGM), 0.23 (HM), and 0.25 (SHM).

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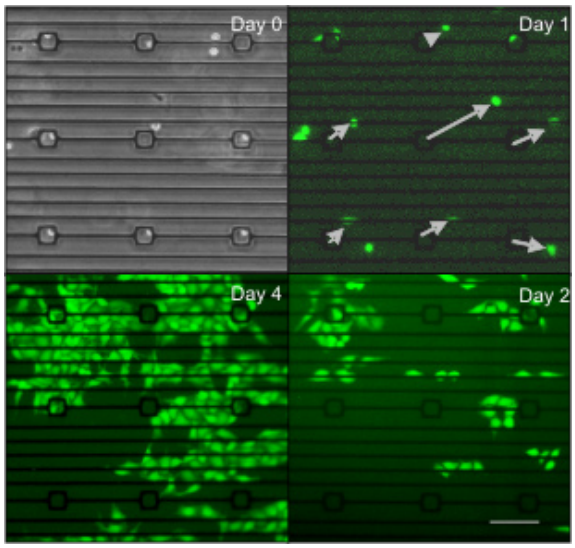
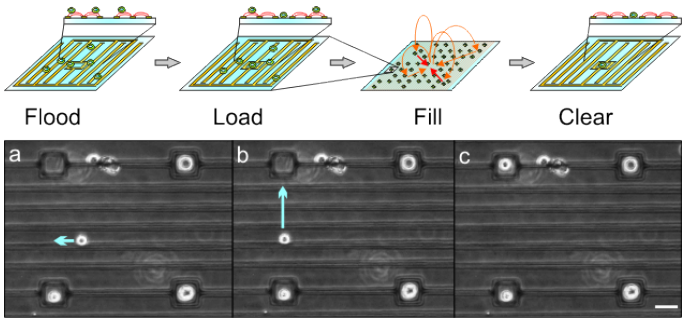
DEP Cell-patterning for Controlling Cellular Organization

N. Mittal, J. Voldman
Sponsorship: Singapore-MIT Alliance

The ability to place cells at specific locations on a substrate is a useful tool to study and engineer interactions between cells [1], perform image-based cell selection [2], and create cell-based biosensors [3]. The ability to pattern with single-cell resolution is necessary in order to perform studies of single-cell physiology in which these cells are interacting with other cells. We have previously created nDEP-based traps that were used to hold single micron-size *beads* at chosen locations on a substrate [4]. We have recently extended this work by modifying the design to allow us to manipulate and pattern single *cells*. We accomplished this modification by adding interdigitated electrodes to minimize non-specific cell adhesion and determining operating parameters that minimized heating and electric field exposure. The resulting structures are termed nDEP microwells to reflect that fact that they present an electrical microwell to incoming cells, allowing only cell-substrate attachment inside the DEP trap. With these nDEP microwells we have been able to place non-adherent cells and pattern adherent cells (Figure 1). Additionally, we have demonstrated that our cell-patterning technique does not affect gross cell phenotype as measured by morphology and proliferation. Finally, we have developed a method that combines pressure-driven and convective flows to manipulate cells in two dimensions (Figure 2).



▲ Figure 1: Phase and fluorescent images of GFP-expressing HeLa cells trapped in an nDEP microwell array, showing that they exhibit normal morphology and proliferation over 4 days after being trapped at 1 V_{pp} and 10 MHz. Arrows in the Day 1 figure (top, right) show the displacement of cells that moved out of the trap. The scale bar represents 100 µm.



▲ Figure 2: Top: Schematic of operating procedure. In the "Fill" step, orange lines show the motion of the fluid while red lines show the motion of (two) untrapped cells. The flow must be kept slow enough (< 5 µm/s) so that cells do not get lifted with the flow. Bottom: Use of convective flow to pattern cells. (a) → (b): Convective flow pushes untrapped cells towards the center of the electrode array (not shown at this scale) when electrodes are driven at 2.5 V_{pp}. Blue arrows show the movement of cells between frames. This flow is used to align cells with the trap. (b) → (c): Transition is made to pressure-driven flow using a syringe pump. All untrapped cells move in the same direction, along the array. The pressure-driven flow is used to push aligned cells into the traps. The scale bar represents 25 µm.

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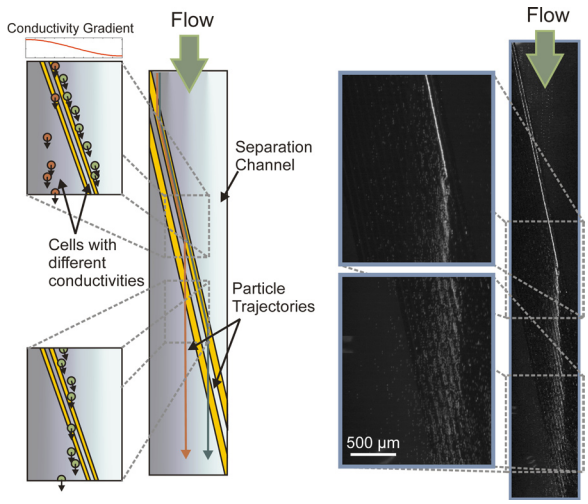
Iso-dielectric Cell Separation

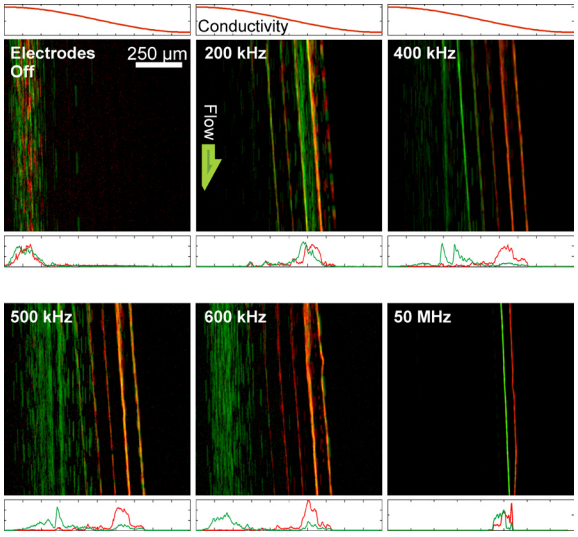
M.D. Vahey, J. Voldman
Sponsorship: NIH NIBIB, MIT Buschbaum Fund, Singapore-MIT Alliance, CSBi/Merck Graduate Fellowship

Increased throughput in the techniques used to engineer new metabolic pathways in unicellular organisms demands similarly high throughput tools for measuring the effects of these pathways on phenotype. For example, the metabolic engineer is often faced with the challenge of selecting the one genomic perturbation that produces a desired result out of tens of thousands of possibilities [1]. We propose a separation method – iso-dielectric separation, or IDS – which separates microorganisms continuously based on their intrinsic dielectric properties [2-3]. Because IDS is an equilibrium method, sorting cells according to their unique equilibrium positions in an energy landscape, it offers enhanced specificity over other label-free separation methods [4]. This technology would enable high throughput screening of cells based upon electrically distinguishable phenotypes.

Iso-dielectric separation uses dielectrophoresis (DEP) and media with spatially varying conductivity to create the energy landscape in which cells are separated according to their effective conductivity (Figure 1). It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis, and is thus applicable to uncharged particles, such as cells [5]. The IDS leverages many of the advantages of microfluidics and equilibrium gradient separation methods to create a device that is continuous-flow, capable of parallel separations of multiple (>2) subpopulations from a heterogeneous background, and label-free. We demonstrate the simultaneous separation of three types of polystyrene beads based upon surface conductance as well as sorting non-viable from viable cells of the budding yeast *Saccharomyces cerevisiae* (Figure 2). Current efforts are focused on the separation of *Escherichia coli* based upon the amount of the intracellular polymer poly(hydroxybutyrate) each cell contains.



▲ Figure 1: (Left) Illustration of iso-dielectric separation, depicting cells with different electric properties following different trajectories in a conductivity gradient. (Right) Fluorescence micrograph showing the trajectory of a single type of polystyrene beads flowing through the device.



▲ Figure 2: Separation of viable and non-viable yeast cells using IDS, showing in particular the frequency-dependent behavior of live and dead cells in the device (σ_h = 0.047 S/m, σ_l = 0.0093 S/m, Q = 3µl/min, V = 20 V_{pp}). Optimal separation is observed at ~600 kHz.

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MEMS Vibration Harvesting for Wireless Sensors

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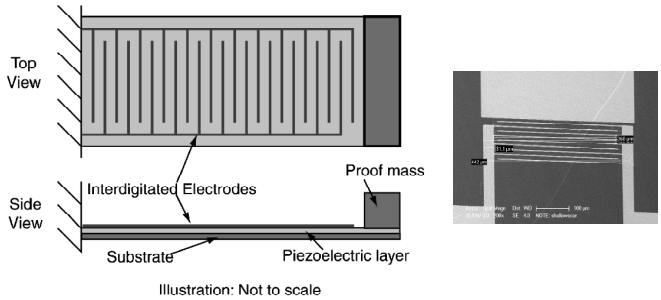
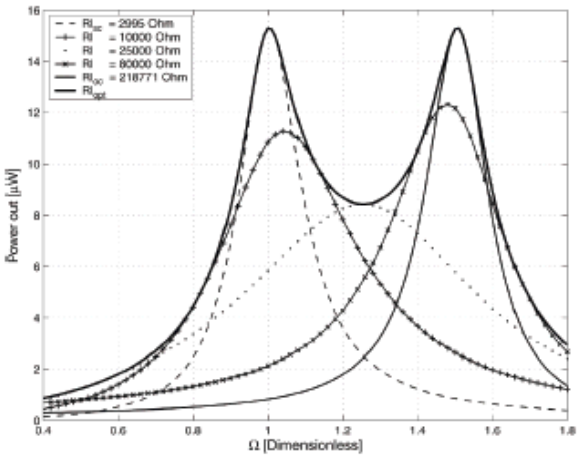
Sponsorship: AFOSR, NSF Fellowship

The recent development of "low power" (10's-100's of μW) sensing and data transmission devices, as well as protocols with which to connect them efficiently into large, dispersed networks of individual wireless nodes, has created a need for a new kind of power source. Embeddable, non-life-limiting power sources are being developed to harvest ambient environmental energy available as mechanical vibrations, fluid motion, radiation, or temperature gradients [1]. While potential applications range from building climate control to homeland security, the application pursued most recently has been that of structural health monitoring, particularly for aircraft.

This SHM application and the power levels required favor the piezoelectric harvesting of ambient vibration energy. Current work focuses on harvesting this energy with MEMS resonant structures of various geometries. Coupled electromechanical models for uniform beam structures have been developed to predict the electrical and mechanical performance obtainable from ambient vibration sources. The optimized models have been validated by comparison to prior published results [2] and verified by comparison to tests on a macro-scale device [3]. A non-optimized, uni-morph beam prototype (Figure 1) has been designed and modeled [4-5]. Dual optimal frequencies with equal peak powers and unequal voltages and currents are characteristic of the response of such coupled devices when operated at optimal load resistances (Figure 2). Design tools to allow device optimization for a given vibration environment have been developed for both geometries. Future work will focus on fabrication and testing of optimized uni-morph and proof-of-concept bi-morph prototype beams. System integration and development, including modeling the power electronics, will be included.



▲ Figure 1: Illustration of MPVEH uni-morph configuration (left) and SEM of a prototype device.



▲ Figure 2: Power vs. normalized frequency with varying electrical load resistance [4].

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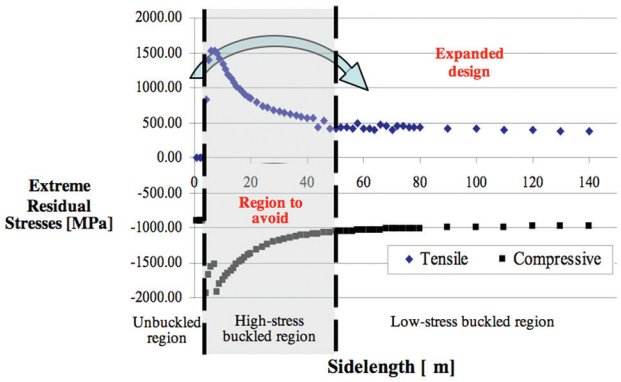
Design, Fabrication, and Testing of Multilayered Microfabricated Solid Oxide Fuel Cells (SOFCs)

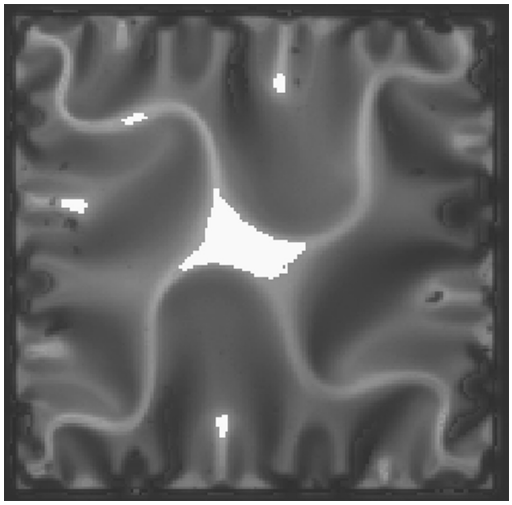
N. Yamamoto, D. Quinn, P. Capozzoli, N. Wicks, B.L. Wardle, S.M. Spearing (in coll. with B.A. Wilhite, J. Hertz, J. Cui, K.F. Jensen, H.L. Tuller, M.A. Schmidt)
Sponsorship: ARO

Microfabricated solid oxide fuel cells were investigated for portable power applications requiring high energy densities [1]. The thickness of the electrolyte, the travel length of oxygen ions, was reduced down to ~150nm. The tri-layers (yttria-stabilized zirconia (YSZ) as an electrolyte and platinum-YSZ cermet as cathode/anode) were sputter-deposited on a silicon wafer, and then they were released as square plates by KOH etching the silicon through patterned silicon nitride masks on the back side. High intrinsic and extrinsic (thermal) stresses due to fabrication and operation (25-600°C) [2], respectively, require careful thermomechanically stable design of μSOFCs.

First, material properties of the ultra-thin YSZ were characterized experimentally and found to be significantly different than those of bulk YSZ [3]. Second, based on the obtained properties, maximum stresses in the plates at 625°C were analyzed using non-linear von Karman plate theory [4]. The stresses showed three regions with sidelength variation: an un-buckled regime, a buckled regime with high stresses, and post-buckling regime with lower stresses (see Figure 1). The μSOFCs were fabricated in the post-buckling regimes with ~80-~180μm sidelength and total ~450nm thickness. With the plates buckled as shown in Figure 2, the μSOFCs produced power output of 0.008mW/cm, lower than the expected power from their electrochemical test. Given the high-performance predicted for the underlying nano-structured ultra-thin electrolyte, anode, and cathode layers, additional studies are needed to improve specimens and test setup and to assess μSOFCs' long-term operational stability.



▲ Figure 1: Maximum stress evolution with sidelength of YSZ square membranes with ~450nm thickness cycled to 600°C.



▲ Figure 2: Top-view of highly buckled, but unfailed, square membrane.

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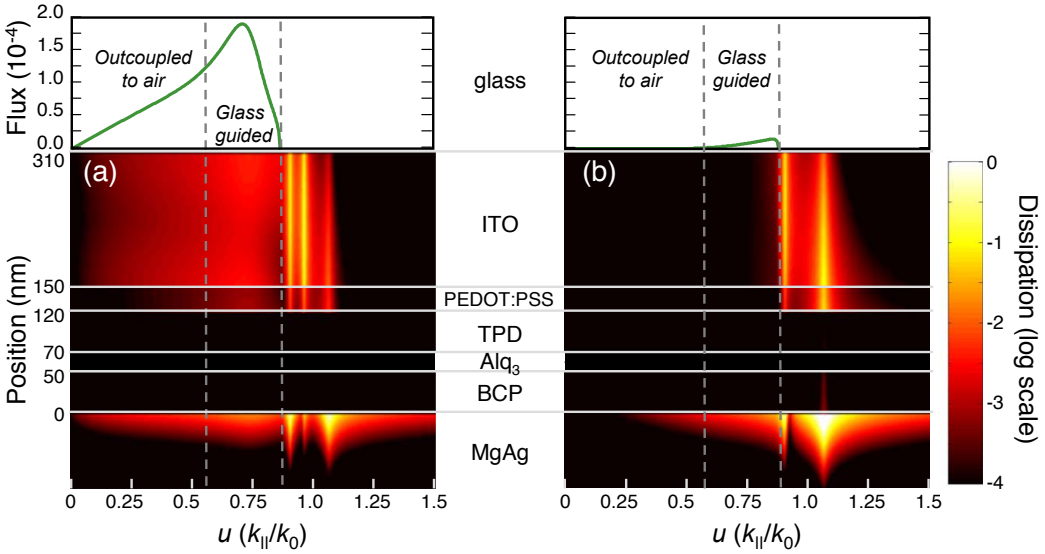
Section 5

PHOTONICS

Optical Models of Organic Light Emitting Devices

K. Celebi, T.D. Heidel, M.A. Baldo
Sponsorship: DARPA, NSF NIRT

We calculate the dipole energy propagation in a multilayer stack by analytically extending the theoretical model of Chance, Prock and Silbey [1], which calculates the field pattern and lifetime of a dipole in this geometry. This analytical extension [2] facilitates numerical calculations to predict the outcoupling and optical dissipation mechanisms of an organic light emitting device (OLED), where the excitons can be modeled as dipoles. We have applied this approach to a previous experimental measurement of an OLED outcoupling by Segal *et al.* [3] The model predictions agree with the experiment, yielding a similar outcoupling efficiency, and in addition shows the mode-resolved spatial dipole energy dissipation of the same device (Figure 1). Thus we conclude that the surface-parallel oriented dipoles generate most of the emitted light, and the main optical loss mechanisms are the waveguiding in the glass and organic layers, along with a smaller loss to the plasmon modes of the cathode. Our method can be used for designing low-loss OLED structures and efficient cavity designs.



▲ Figure 1: (a) Absorption of the parallel dipole energy as a function of the position and normalized surface-parallel wave vector. The dipole is located at the middle of the Alq_3 layer and the emission wavelength is λ = 535 nm. Bright features correspond to a higher absorption. The green curve shows the outcoupled energy flux. (b) Same absorption as in part (a) but for perpendicular dipole. Perpendicular dashed lines divide this flux into air-outcoupled, glass-waveguided, organics-waveguided and surface plasmon polariton (SPP) portions. At λ = 535 nm, the dielectric constants for Mg, BCP, Alq_3, TPD, PEDOT and ITO are the following: $\varepsilon = 1.908 + 0.265i$, $\varepsilon = 2.985 + (4.11 \times 10^{-5})i$, $\varepsilon = 2.962$, $\varepsilon = 2.985 + (4.11 \times 10^{-5})i$, $\varepsilon = 2.304 + (3.33 \times 10^{-2})i$ and $\varepsilon = 3.295 + (3.63 \times 10^{-2})i$, respectively. Note that the dielectric constant of TPD was assumed to be equal that of BCP. (Figure is taken from [2]).

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Electric Field and Temperature Dependent Analytic Model of Charge Carrier Mobility in Amorphous Organic Semiconductors

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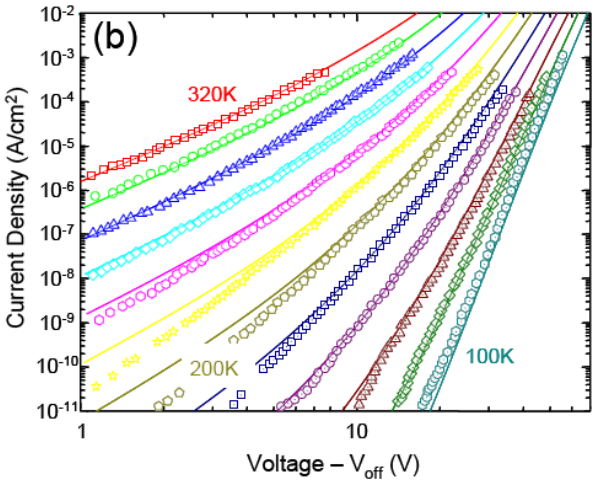
Sponsorship: DuPont, MIT

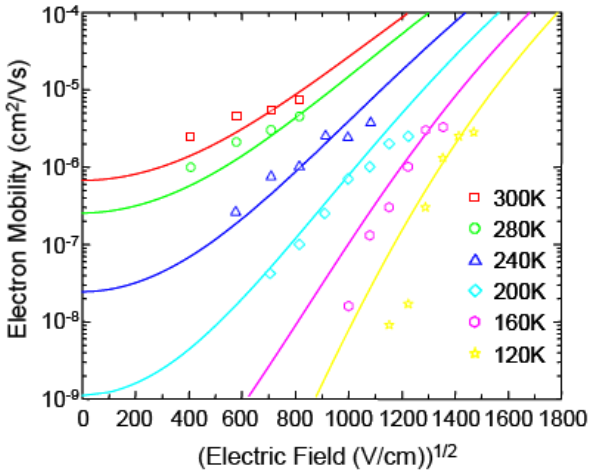
Understanding the electric-field dependence of charge carrier mobility is central to the rational design of organic semiconductor devices [1]. Studies of charge transport in organic semiconductors have observed a log $\mu \sim \sqrt{F}$, or Poole-Frenkel, dependence of charge carrier mobility, μ, on electric field, F. Numerical simulations have established that the Poole-Frenkel dependence is due to disorder, and analytic theories have continued to employ simulation-based empirical models in efforts to jointly summarize the electric-field, temperature-, and charge-density-dependencies [1].

In this research we present a complete analytic description of mobility by considering non-equilibrium carrier distributions within a percolation framework. Only three free parameters are required: the width of the density of states, the decay length of the charge carrier wavefunction, and the maximum conductivity, which depends in turn on the strength of the intermolecular interaction. The electric field dependence of charge carrier mobility is found to be well-modeled by an effective temperature, suggesting that the dominant effect of the electric field is to generate a nonequilibrium charge carrier distribution.

The theory is compared to measurements by Brütting, *et al* [1] of the current-voltage and mobility of the archetype small molecule tris (8-hydroxyquinoline) aluminum. The theory accurately reproduces the temperature, carrier density, and electric field dependencies of the experimental data over a wide range of temperatures, carrier densities, and electric fields. Most significantly, the mobility theory enables predictive models of organic semiconductor devices based on material parameters that may be determined by *ab initio* quantum chemical simulations. Consequently, we expect that the theory will allow the rational design of organic devices in important applications such as video displays and solar cells.



▲ Figure 1: Temperature-dependence of the *J-V* characteristics of an Al/Alq3/Ca device with an Alq3 thickness of 300 nm[1]. Solid lines show theoretical fits. Current-voltage curves were offset by a voltage *Voff* = 2V to compensate for uncertainty in *Vbi* and the contact resistances.



▲ Figure 2: Temperature and electric field dependence of charge carrier mobility obtained from transient electroluminescence measurements [1]. Theoretical fits are shown in solid lines.

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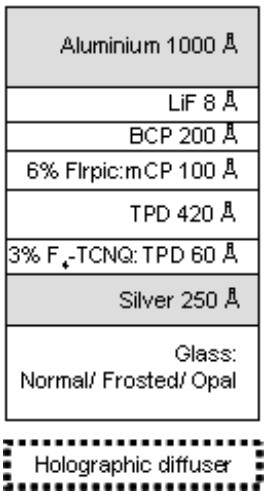
Saturated and Efficient Blue Phosphorescent Organic Light Emitting Devices with Lambertian Angular Emission

C.L. Mulder, K. Celebi, M.A. Baldo
Sponsorship: NSF

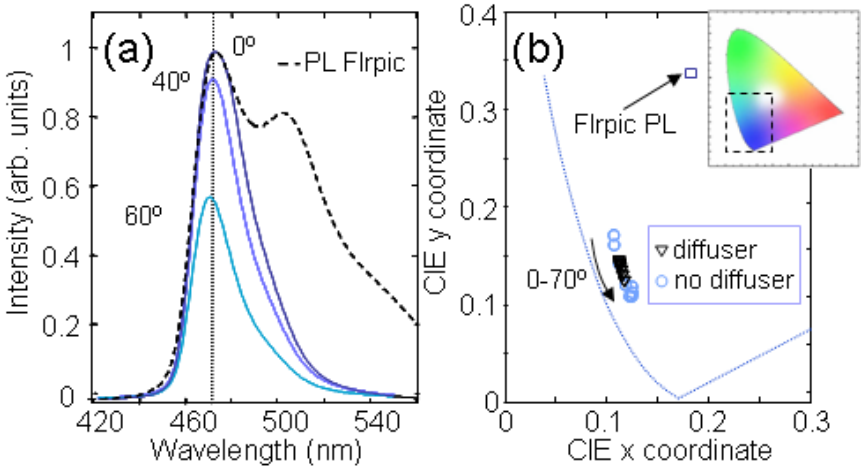
The realization of stable blue phosphorescent organic light emitting devices (OLEDs) has proved challenging. An important limitation is the broad photoluminescent (PL) spectrum characteristic of organic dyes. For example, greenish-blue or "sky-blue" phosphors have strong emission in the blue [1]. But optical transitions to higher vibrational modes of the electronic ground state extend their emission spectrum deep into the green. Because the eye responds strongly at green wavelengths, this broad emission spectrum yields an unsaturated color that is ill suited for most display applications.

In this work a strong microcavity is employed to optimize the color of a phosphorescent organic light emitting device (OLED) based on the sky blue phosphor FIrpic. The usual disadvantages of a strong microcavity, namely the introduction of an angular dependence to the OLED's color and a non-Lambertian angular emission profile [2], are overcome by scattering the emitted radiation. As scattering sources, frosted glass, opal glass, and holographic diffusers are studied.

With a holographic diffuser as the scattering medium, the microcavity OLED achieves an external quantum efficiency of (5.5±0.6)%, as compared to (3.8±0.4)% for a conventional structure. The color coordinates of the microcavity OLED with holographic diffuser are (x,y) = (0.116±0.004, 0.136±0.010), with minimal angular color shift and a nearly ideal Lambertian angular emission profile.



▲ Figure 1: In the strong microcavity, the anode is a thin, semitransparent layer of Ag. The cathode is Al/LiF. Devices were grown directly on the smooth back surface of frosted glass and opal glass diffusers. The holographic diffuser was employed external to devices grown on regular glass.



▲ Figure 2: (a) Electroluminescent spectra of the strong microcavity FIrpic OLED as a function of angle from the surface normal with the holographic diffuser. A color shift with increasing angle is barely perceptible. For comparison we plot the intrinsic photoluminescent spectrum of FIrpic (dotted line). (b) The color coordinates of the strong microcavity devices with and without holographic diffusers. Inset: the full CIE diagram identifying the expanded blue region.

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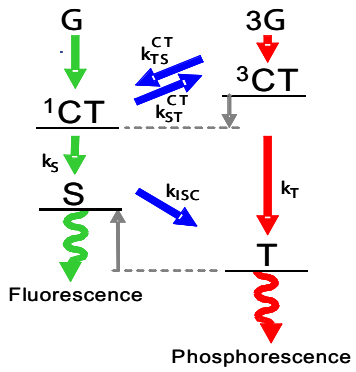
Extrafluorescent Electroluminescence in Organic Light Emitting Devices

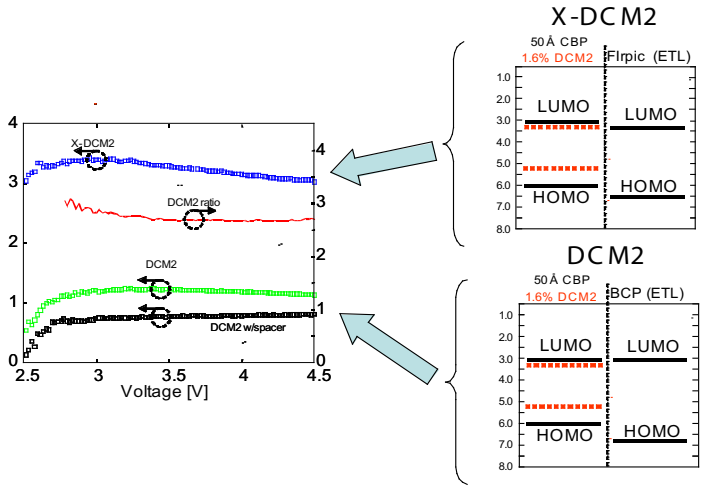
M. Segal, M. Singh, K. Rivoire, S. Difley, T. Van Voorhis, M.A. Baldo
Sponsorship: NSF, NSERC, 3M Corporation

Organic light emitting devices (OLEDs) are a promising technology for flat panel displays and solid-state lighting due to their low cost, low power consumption, and mechanical flexibility. These OLEDs can produce two kinds of light: fluorescence, the result of an allowed transition, and phosphorescence, the result of a partly forbidden transition.[1] Fluorescent OLEDs represent the vast majority of all OLEDs and have better stability in certain colors but have efficiencies that are usually limited by spin conservation to one fourth of phosphorescent efficiencies [1]. We have demonstrated a technology for raising the efficiency of fluorescent OLEDs to approach that of phosphorescent OLEDs [2]. This should prove to be a major step forward in producing stable and high-efficiency OLEDs across all colors.

The efficiency of fluorescent OLEDs is limited by the process in which a neutral molecular excited state, or exciton, is created from oppositely-charged neighboring molecules. Excitons can have triplet or singlet spin symmetry. Typically only singlet excitons are luminescent, and they represent only 25% of all excitons formed. We demonstrate that this percentage can be increased to nearly 100% by mixing the spins of exciton precursor states. We have calculated that the singlet exciton precursor state is lower in energy than the triplet precursor state, which will favor singlet precursors and excitons if mixing of the precursor states is introduced (Figure 1). If at the same time excessive mixing of the exciton state to dark triplets is avoided, an overall efficiency enhancement can result. We demonstrate such an efficiency enhancement using the mixing molecule FIrpic and the fluorescent material DCM2 (Figure 2).



▲ Figure 1: Rate diagram for exciton formation. Triplet (^{3}CT) and singlet (^{1}CT) exciton precursor states form triplet (T) and singlet (S) excitons at rates k_S and k_T. Extrafluorescence occurs when the CT state mixing rate k_{TS}^{CT} is made large with respect to k_T, and the exciton mixing rate k_{ISC} is low. While $\Delta E_{EX} > 0$, we have calculated and measured $\Delta E_{CT} < 0$, so that $k_{TS}^{CT} > k_{ST}^{CT}$, favoring singlet production.



▲ Figure 2: Demonstration of an extrafluorescent OLED, or X-OLED ("X-DCM2"). The mixing molecule iridium(III) bis [(4,6-difluorophenyl) pyridinato-*N*,*C*$^{2'}$] picolinate (FIrpic) is used as an electron transport layer, so that exciton precursor states are preferentially mixed. The laser dye 4-(dicyanomethylene)–2–methyl–6-[(4-dimethylaninostyryl)-4-H-pyran] (DCM2) is used as an emissive material in a host of 4,4'-N,N'-dicarbazolyl-biphenyl (CBP). A control device ("DCM2") where FIrpic is replaced with 2,9-dimethyl-4,7-diphenyl-1,10-phenanthroline (BCP), which has low mixing rates, shows a 2.7× lower efficiency. A second control device ("DCM2 w/ spacer"), wherein the FIrpic layer is moved away from the emissive zone by 100 Å of BCP, shows no efficiency enhancement.

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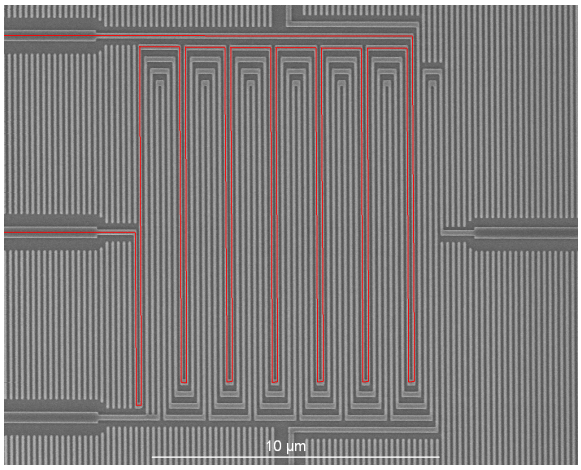
Achieving Photon-number-resolution Using Multi-element Superconducting Photodetectors

E. Dauler, A.J. Kerman, B. Robinson, V. Anant, K. Rosfjord, J. Yang, K.K. Berggren
Sponsorship: USAF

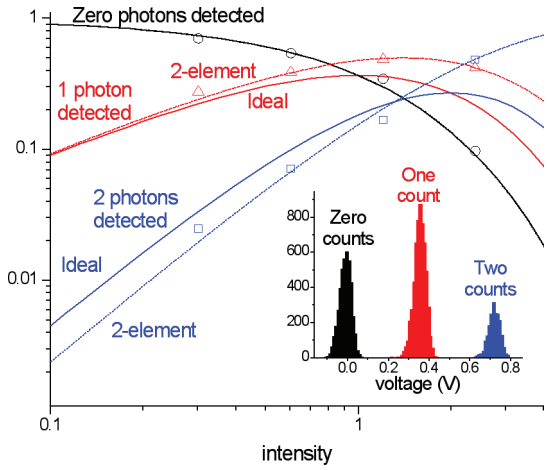
We demonstrate an approach for combining multiple, independent, superconducting nanowire, single-photon detectors to create a high-speed, high-efficiency detector that can resolve photon number [1]. Optical loss in distributing the light between the elements is eliminated by fabricating a detector array with an active area identical to a single device. The scanning-electron-microscope image shown in Figure 1 illustrates one approach for subdividing a ~10 μm × 10 μm active area into four independent elements. This interleaved arrangement ensures that the light will uniformly illuminate all four elements. The fabrication [2] consists of an optical lithography and liftoff process to fabricate metal contact pads and an electron-beam lithography and reactive-ion-etching process to pattern the superconducting nanowires. The additional grating features that are not electrically connected to the detector elements are used to eliminate proximity effects in the electron-beam exposure.

To achieve high-speed photon-number-resolution, the outputs from the independent elements would typically be combined digitally, but to better illustrate the detector's photon-number resolving capabilities, we have chosen to add the analog output signals. A two-element SNSPD was illuminated with attenuated, picosecond laser-pulses and the peak voltage of the summed output was measured. A representative histogram of the measured peak voltages is shown in the inset of Figure 2. It is clear that, even with the two output pulses summed, thresholds between zero, one, and two detection events can be easily selected. The probability of each of these cases can then be measured as a function of the light intensity; Figure 2 shows these probabilities, along with calculated probabilities for the 2-element detector and an ideal photon-number-resolving detector. This approach allows the number of photons to be measured over a wide range of attenuation with a factor of ≤ 2 error due to using only two elements.

This work is sponsored in part by the United States Air Force under Air Force Contract #FA8721-05-C-0002. Opinions, interpretations, recommendations and conclusions are those of the authors and are not necessarily endorsed by the United States Government.



▲ Figure 1: Scanning-electron-microscope micrograph of a 4-element device with an overlaid red curve highlighting one of the four independently biased and read-out detector elements.



▲ Figure 2: Measured and calculated probabilities of zero, one, and two counts with an inset showing the histogram of peak voltages, colored to indicate the regions contributing to the measured probabilities.

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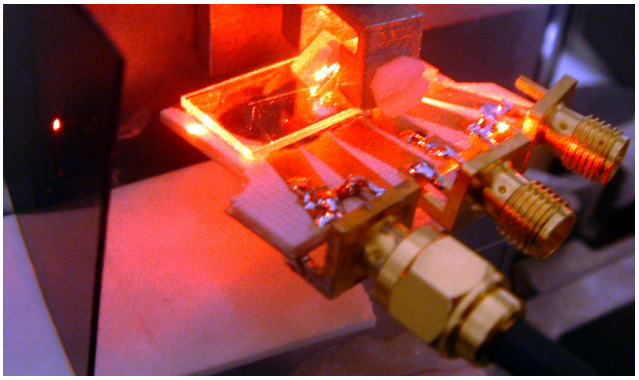
Guided-wave Devices for Holographic Video Display

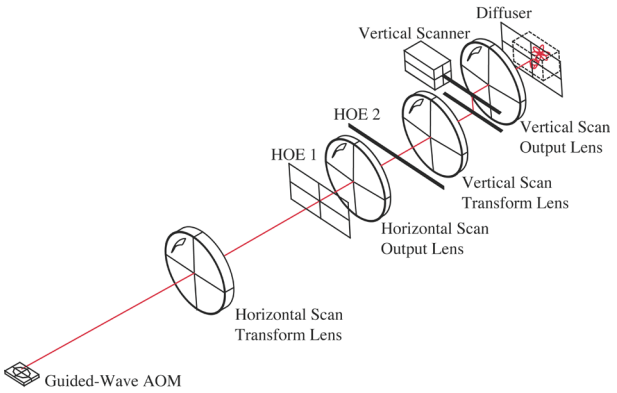
D. Smalley, V.M. Bove, Jr., Q. Smithwick,
Sponsorship: CELab, Digital Life, Things That Think Research Consortia, Media Laboratory

We are developing a guided-wave optical modulator [1-2] with 1 GHz composite bandwidth Surface Acoustic Wave (SAW) transducer arrays for use in video displays. This device is designed to diffract light both vertically and horizontally by creating surface acoustic waves that interact with light trapped in waveguides on the surface of a lithium niobate substrate. To fabricate this modulator, we first mask a wafer of Z-cut lithium niobate with SiO_2 through a PECVD process and then we immerse it in heated benzoic acid and lithium benzoate to create single polarization waveguides. The waveguide is subsequently annealed to restore its acoustic properties. Finally, we pattern aluminum transducers onto the waveguides by conformal contact lithography employing a negative resist lift-off technique.

The goal of this work is to enable the inexpensive manufacturing of Scophony-architecture video displays [3] (both 2D and holographic video [4-5]) without the need for the horizontal scanning mirrors that typically limit the scalability of this technology.



▲ Figure 1: A device undergoing testing.



▲ Figure 2: Architecture of our display system.

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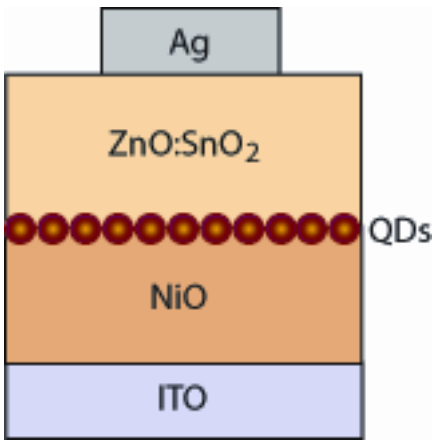
All Inorganic Colloidal Quantum-dot LEDs

V. Wood, J.M. Caruge, J.E. Halpert, M.G. Bawendi, V. Bulović
Sponsorship: NSF MRSEC, NSF NIRT, PECASE, ISN

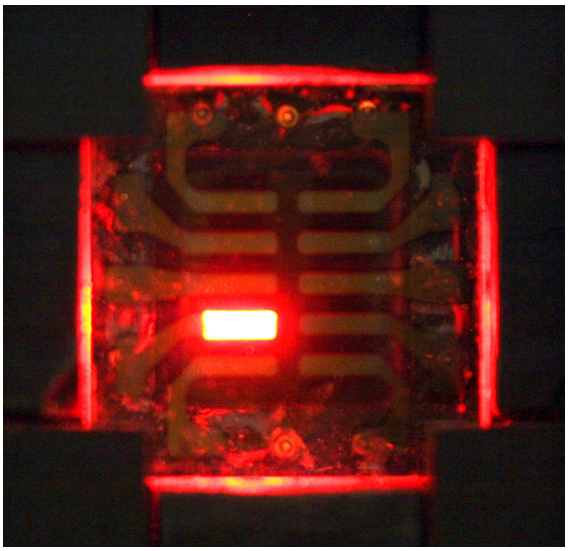
LEDs with a quantum-dot (QD) emissive layer are an attractive technology for display and large-area lighting applications. QDs are nanoparticles that can be synthesized to emit anywhere from the ultraviolet to the infrared regions of the spectrum by changing their size and chemical composition. For example, varying the size of CdSe QDs from 17 to 120 Å tunes them to emit light at a wavelength between 470 nm to 630 nm [1]. Furthermore, QDs possess excellent color saturation and high photoluminescence efficiencies.

QDs have been successfully integrated into LEDs with organic charge transport layers. Such devices boast external quantum efficiencies (EQEs) ranging from of 0.4% for blue emission to 2.4% for red emission [2]. However, despite the high EQE and the ease of fabrication offered by organic semiconductor films, organic materials are susceptible to deterioration from atmospheric oxygen and water vapor. Device lifetimes can be improved with packaging, but this increases cost, making it difficult for QD-LEDs to compete with the already established technology of liquid crystal displays (LCDs). Furthermore, organic materials cannot sustain the high current density needed to realize an electrically pumped colloidal QD laser. In contrast, metal oxides are chemically and morphologically stable in air and can operate at high current densities.

We report the first all-inorganic QD-LEDs consisting of radio-frequency sputtered metal-oxide charge transport layers and a colloidal QD electroluminescent region. These devices manifest a 100-fold increase in EQE over the one previously reported inorganic QD structure [3]. Our device consists of ZnCdSe QDs sandwiched between resistive, p-type NiO and co-deposited ZnO and SnO_2 (see Figure 1). We measured a peak EQE of 0.09% at a current density of 3.2 A/cm² and a peak brightness of 1950 Cd/m² at a current density of 3.7 A/cm². As shown in Figure 2, light emission from the QDs is uniform across the device.



▲ Figure 1: Schematic of the all-inorganic QD-LED structure. Indium tin oxide (ITO) and Ag electrodes are used.



▲ Figure 2: All inorganic QD-LED operating under 6 V of applied bias and showing a brightness of 106 Cd/m².

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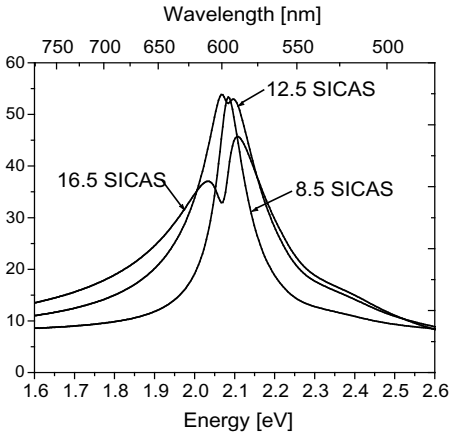
Physics and Fabrication of J-aggregate Thin Films in Optical Microcavities for Nonlinear Optics Applications

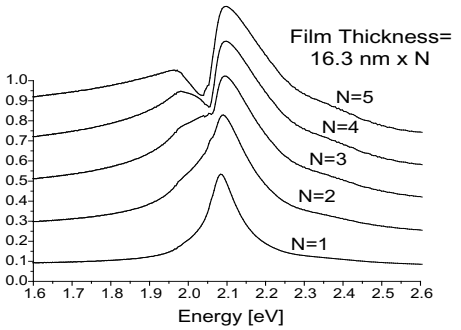
M.S. Bradley, J.R. Tischler, Y. Shirasaki, V. Bulović
Sponsorship: DARPA, NDSEG, NSF MRSEC

Thin films of J-aggregates of cyanine dyes, which found wide use in the 20th century in the photographic film industry, exhibit narrow linewidth and large oscillator strength, enabling their use in the first room-temperature solid-state devices that exhibit the strong-coupling regime of Cavity Quantum Electrodynamics (Cavity QED) [1]. As we demonstrated in a recent study, layer-by-layer (LBL)-assembled J-aggregate thin films can be precisely deposited in a specific location in a microcavity and contain a high density of aggregates, contributing to the observation of a peak thin-film absorption coefficient of 1.05 ± 0.1 x 10^6 cm^{-1}, among the highest ever measured for a neat thin film [2]. As LBL J-aggregate thin films are incorporated into more complex optoelectronic device structures, a more thorough understanding of the properties of exciton-polaritons in J-aggregate thin films is required to evaluate how the properties of the thin films change as deposition parameters are varied.

We investigate the optical and morphological properties of 5,6-dichloro-2-[3-[5,6-dichloro-1-ethyl-3-(3-sulfopropyl)-2(3H)-benzimidazolidene]-1-propenyl]-1-ethyl-3-(3-sulfopropyl) benzimidazolium hydroxide, inner salt, sodium salt (TDBC, anionic dye) J-aggregates, alternately adsorbed with poly-(diallyldimethylammonium chloride) (PDAC, cationic polyelectrolyte) on glass substrates. Figure 1 shows the reflectance spectra for substrates that underwent 8.5, 12.5, and 16.5 sequential immersions in cationic and anionic solution (SICAS) of PDAC/TDBC, where 0.5 SICAS refers to ending the growth on the PDAC immersion step. Figure 2 shows the reflectance spectra generated from T-matrix simulations using the dielectric function derived via quasi-Kramers-Kronig regression and multiples of the 8.5 SICAS film thickness. As the thickness of the film is increased, a photonic band gap develops similar to the "super-radiance" observed in multiple quantum-well structures and thin film organic crystals. The observation that the spectral broadening is due to a photonic band gap effect suggests that thicker LBL films may be used in cavity devices to boost Rabi splitting without sacrificing the linewidth of the cavity exciton-polariton.



▲ Figure 1: Measured reflectance for samples with 8.5, 12.5, and 16.5 SICAS of PDAC/TDBC, where profilometry indicates film thicknesses of 16.3 ± 3.8 nm, 32.1 ± 6.6 nm, and 42.6 ± 5.3 nm, respectively.



▲ Figure 2: Simulated reflectance using a dielectric function derived using a quasi-Kramers-Kronig regression with thickness multiples of 16.3 nm showing similar spectral broadening to that in Figure 1.

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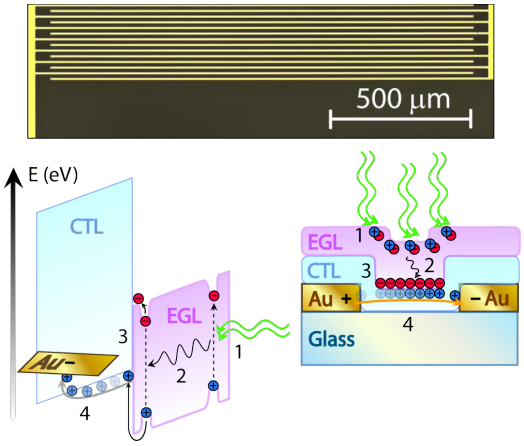
Organic Lateral Heterojunction Photoconductors

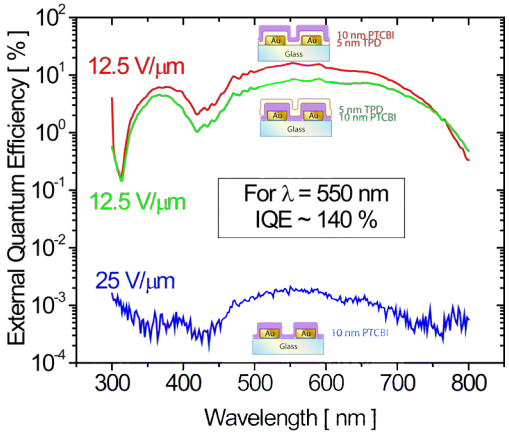
J. Ho, V. Bulović
Sponsorship: ISN

The purpose of this project is to develop solid-state, organic device structures capable of amplifying detection of chemical analytes and of efficiently transducting the chemosensitive response into an attenuated electrical signal. The main advantage to using organic materials in these structures is that they are synthetically flexible and can be tailored to respond to specific analytes. We demonstrated lateral heterostructures with in-plane electrodes consisting of an optically active, chemosensing layer and a charge-transport layer arranged as shown in Figure 1. In these structures, luminescence and corresponding exciton density in the chemosensitive layer are directly proportional to the density of the adsorbed analytes. It is advantageous to physically separate the sensing and transport functions in these chemical sensors as the separation allows us to optimize the transduction of chemosensitivity to the device current and to develop a reusable device platform for a variety of chemosensing applications.

In addition to developing a novel device platform for chemical sensing, we are also using this novel structure to study charge transport and exciton dynamics in organic thin films (Figure 1). Our devices consist of a series of gold interdigitated finger electrodes (W x L = 1500 μm x 4 μm) spaced 10 μm apart. The gold electrodes are photolithographically defined on glass before the organic layers are thermally evaporated. Lock-in measurements of the photocurrent spectra suggest external quantum efficiencies in the range of 10%. Initial experiments indicate an enhancement in photoresponse of the heterostructure devices over devices made from bulk films of both materials (Figure 2).



▲ Figure 1: The interdigitated gold fingers create 100 channels, each 1500 μm long by 10 μm wide, yielding an effective device area of approximately 1.5 mm^2. A digital image (a) of a set of device electrodes under magnification (50X). Energy band diagram (b) of a lateral bi-layer heterojunction photoconductor consisting of an exciton generation layer (EGL) and a charge transport layer (CTL). A cross-sectional view (c) of the same bi-layer device is also shown. Both illustrations depict the physical processes involved in steady-state device operation: (1) absorption, (2) exciton diffusion, (3) exciton dissociation and charge transfer, and (4) charge transport.



▲ Figure 2: Semi-logarithmic plot of external quantum efficiency (EQE) versus wavelength. Inset illustrations depict device structures and film thicknesses next to their corresponding curves, along with the electric fields applied. The Au/TPD device yields no measurable photoresponse and is not shown. Both heterojunction devices (red and green lines) yield orders of magnitude improvement in the (EQE) over the Au/PTCBI device (blue line) despite using lower bias voltages. At λ = 552 nm, the Au/PTCBI/TPD device (green) and Au/TPD/PTCBI device (red) yield EQEs of approximately 8% and 16%, respectively, which correspond to an internal quantum efficiency (IQE) of approximately 140%. This demonstrates that lateral bi-layer heterojunctions are capable of gain.

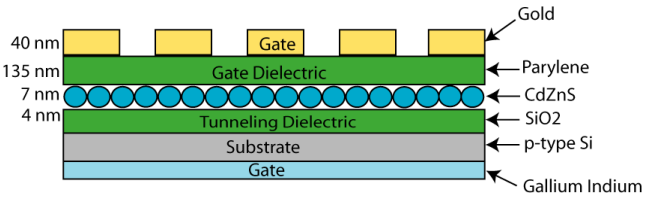
Colloidal Quantum-dot Memories

H. Abdu, J. Leu, K.K. Berggren, P. Anikeeva, O. Nayfeh, D.A. Antoniadis, M. Bawendi, V. Bulović
Sponsorship: SRC/FCRP MSD

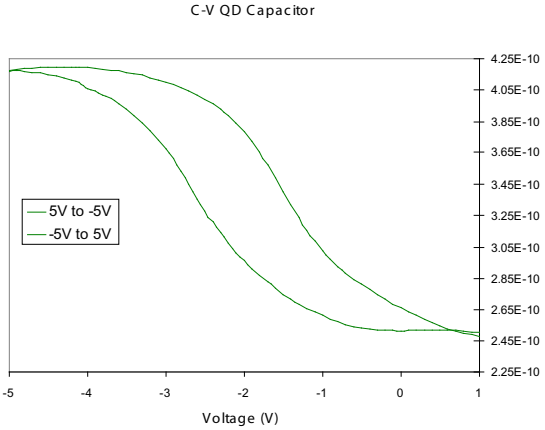
Conventional non-volatile memories face obstacles to continued scaling, such as the inability to use thinner tunneling oxides and poor charge retention due to defects in the tunneling oxide. A possible solution is to replace the continuous floating gate, where charge is stored, with quantum dots (QDs). In the proposed structure, if a defect in the tunneling oxide exists in the oxide below a particular quantum dot, the rest of the quantum dots retain their charge due to poor lateral conduction between QDs. Because of this, quantum dot memories can achieve higher density, decreased power consumption, and improved performance.

We construct a QD capacitor, shown in Figure 1, by using 7nm CdZnS quantum dots as the floating gate. This monolayer of quantum dots was deposited using spin casting. Parylene was used as the gate dielectric because it can achieve good performance at low processing temperatures. This capacitor structure is a first step in achieving a QD memory cell, as it proves significant in understanding the quantum dot's ability to be written (charged), erased (discharged), and read (retain charge).

As shown in Figure 2, we demonstrate the functionality of the QD capacitor. The capacitance voltage (C-V) plot illustrates hysteresis, which indicates the flatband voltage shift that exists due to charge storage. Interestingly, in this device electrons and holes are stored at -5V and at +5V, respectively. Though having both types of charge being charged and discharged is acceptable, it provides insight to the dynamics of charge retention for each type.



▲ Figure 1: Schematic diagram of a QD capacitor structure in which the CdZnS quantum dots have been used as the floating gate.



▲ Figure 2: A C-V plot of QD capacitor with characteristic hysteresis. Electron charging at -5V and hole charging at +5V.

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Recess Integration of Low-threshold VCSELs on Si CMOS ICs

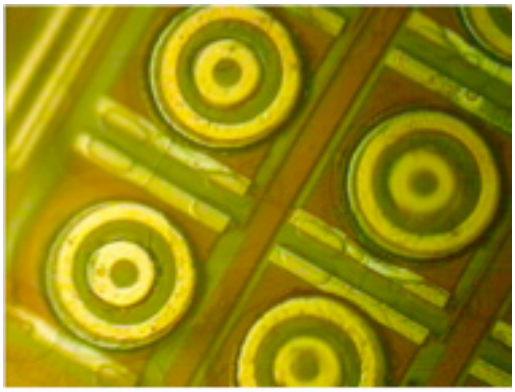
J. Perkins, C.G. Fonstad
Sponsorship: SRC/FCRP IFC, NSF

Vertical Cavity Surface Emitting Lasers (VCSELs) integrated on silicon ICs have long been sought for optical interconnect applications to improve transfer rates in high-performance circuit applications. We have developed a new technique for micro-scale hybrid heterogeneous integration of optoelectronic devices on silicon integrated circuit wafers and have demonstrated it for optical interconnect applications using VCSELs. This technique allows for intimately connected devices to be integrated directly within the metal/dielectric stack covering a Si IC, allowing wafer scale monolithic processing of a multi-material, multi-technology integrated system.

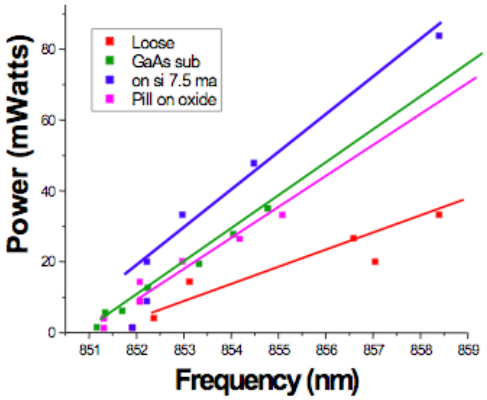
Individual oxide-apertured 850-nm AlGaAs VCSEL device pills 8 μm tall and 90 μm in diameter have been bonded on contact pads at the bottom of recesses etched in the metal/dielectric stack covering a custom-designed, commercially processed silicon integrated circuit chip [1]. These devices are placed using a vacuum pick-up tool and solder-bonded in place. The VCSELs show threshold currents in the 1 to 10 mA range when driven by an on-chip Si transistor, and they display thermal characteristics superior to those of native substrate devices. These same devices can be used in more parallel assembly techniques, such as fluidic self-assembly [2] and magnetically assisted statistical assembly [3].

The superior heat-sinking of VCSELs integrated on Si in this manner is clear from the data shown in Figure 2 below: The thermal impedance of pills on their native (GaAs) substrate is 2.1 °C/mW. It increases to 4 °C/mW if the pill is etched loose of its substrate, but it falls to 2.6 °C/mW if bonded on a pad formed in metal layer 2 of a CMOS process. If it is bonded directly to the silicon substrate, the thermal impedance falls to under 2 °C/mW, the lowest value of all.

To summarize, low threshold VCSELs have been intimately integrated into the dielectric stack of a commercially produced Si IC. These devices showed continuous wave-lasing operation and no performance degradation over native substrate devices. The pseudo-monolithic integration technique demonstrated maintains the planarity of the IC surface and is performed entirely after the Si processing is completed. Devices made of many different materials can be integrated on full Si wafers using this technique, enabling unique hybrid optoelectronic integrated circuits.



▲ Figure 1: A photomicrograph of four 90-μm-diameter VCSEL pills integrated in recesses on a CMOS IC chip. The next steps in the processing are to replanarize the surface, open contact vias, and deposit and pattern interconnect metal lines.



▲ Figure 2: The temperature-tuning of variously mounted VCSEL pills observed as the power dissipated in the pill increases. The loose pills (red) are the most poorly heat-sunk, and the pills bonded on Si (blue) are heat-sunk the best.

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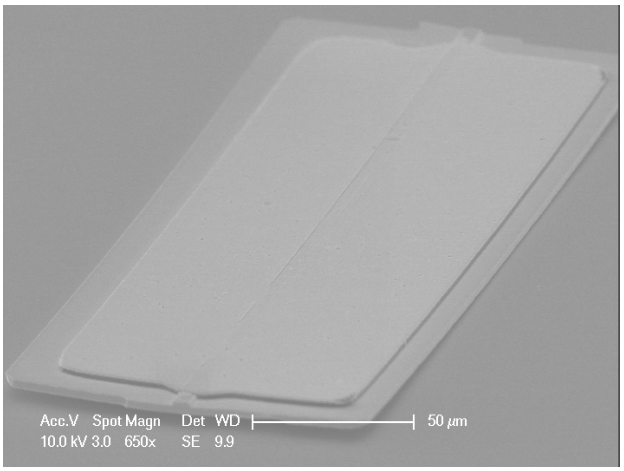
Micro-cleaved Laser Diode Platelets for Integration with Dielectric Waveguides on Silicon IC Wafers

J. Rumpler, C.G. Fonstad
Sponsorship: DARPA through ARL; Lincoln Laboratory IPI Program

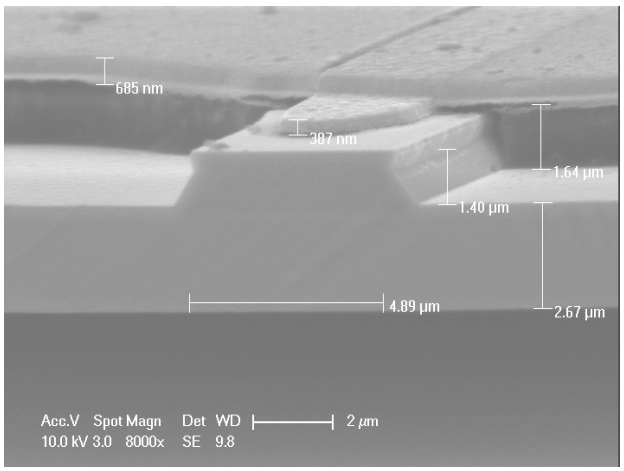
The level of integration seen in commercial active photonic devices is at most a laser monolithically integrated with a modulator or a photodetector flip-chip bonded to an optical waveguide. To perform large scale optoelectronic integration, we have developed a technique that involves optimally fabricating building blocks, such as laser diodes or semiconductor optical amplifiers, and assembling these blocks in dielectric recesses on a system substrate, e.g., a silicon integrated circuit chip [1-2]. Our test case for demonstrating this technology is the integration of 1.55 μm InGaAsP edge-emitting laser diode blocks with planar silicon oxy-nitride waveguides on silicon. To this end, a process has been developed to fabricate freestanding edge-emitting laser platelets using a newly developed micro-cleaving technique. Micro-cleaving is used to simultaneously form highly reflecting end-facets and accurately control the length of the device to ± 1 μm.

The process begins with a device heterostructure that is a total of 5 microns thick and grown on an InGaAs etch-stop layer on an InP substrate. The top laser contact and the waveguide ridge are formed on the upper wafer surface, after which a pattern of long bars extending several laser lengths with notches locating the cleavage sites is etched through the heterostructure and the etch-stop layer. The wafer is embedded in polymer and mounted face down on a handle substrate. The original InP substrate is next removed, back contacts are deposited and patterned, and the polymer is finally removed, freeing the long thin bars from the handle substrate. The released bars are collected in a fluid medium and subjected to ultrasonic agitation, which causes them to cleave at the notches into individual laser platelets. Figure 1 shows a cleaved laser platelet; Figure 2 shows a close-up of the end facet and ridge waveguide. The slight bow in the laser platelet seen in Figure 1 is no longer present after the platelet has been bonded down.

The immediate objectives of the project are to complete characterization of these lasers, to develop an improved back-side metallization process, and to integrate platelet lasers with dielectric waveguides on silicon substrates.



▲ Figure 1: A photomicrograph of an unbonded micro-cleaved edge-emitting ridge waveguide laser diode platelet.



▲ Figure 2: A close-up view of the micro-cleaved end-facet of a laser diode platelet showing the ridge guide and top contact.

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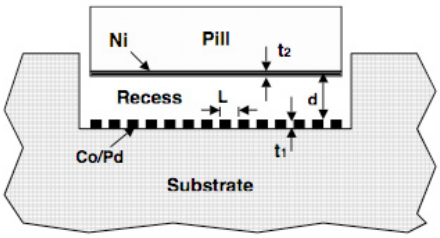
Magnetically Assisted Statistical Assembly, Alignment, and Orientation of Micro-scale Components

D. Cheng, J. Perkins, J. Rumpler, C.G. Fonstad (in coll. with F. Cadieu, Queens College of CUNY, M. Zahn, MIT)
Sponsorship: Vitesse Chair

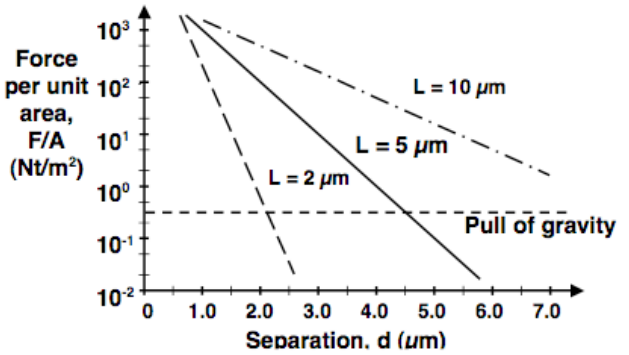
Fluidic assembly offers great promise for automated hybrid assembly of micro-scale components, but it has not yet lived up to its potential. This failure is largely because presently no good way exists to hold properly assembled components in place while simultaneously letting improperly positioned components disassemble and reassemble until they are properly positioned. We are researching the use of magnetic attraction to provide a "glue" to hold properly assembled components in place, eliminate their disassembly, and allow the assembly to go to completion across a wafer [1]. We are also investigating the use of patterned magnetic films to accurately orient, align, and position assembled components.

We call our assembly process magnetically assisted stochastic assembly (MASA). The two unique elements of MASA not present in conventional fluidic assembly are a soft magnetic film on the bottom surface of the component to be integrated and a patterned hard magnetic film on the bottom of the recess in which it is to be located (i.e., assembled). The attraction between these two films holds a component in place in its recess and prevents disassembly. In the basic embodiment of MASA, the soft magnetic film uniformly covers the bottom surface of the component. The hard magnetic film in the recesses is permanently magnetized and is patterned to control the strength and extent of the attracting field experienced by the soft magnetic film on the components. By suitably designing the pattern, calculations indicate that it is possible to tailor the magnetic fields and to create a situation in which the component feels no attraction when it is outside a recess, or is upside down in a recess, and is attracted only toward the hard magnetic film when it is entering a recess in the proper orientation. In second-generation MASA, both the hard and the soft magnetic films will be patterned so that the attractive force will also rotationally orient and laterally position the component in place within the recess.

Our efforts have been hampered for several years by the lack of a good source of hard magnetic thin films, but this situation has changed significantly recently as we have established a collaboration with Professor Fred Cadieu at Queens College of CUNY, an expert in the sputter deposition of Sm-Co films. He has supplied us with several films and we have already developed a wet etch which allows us to pattern these films and remove them from the side-walls of recesses. We presently seek funding for a research program in this area.



▲ Figure 1: A cross-sectional cartoon illustrating the application of magnetically assisted assembly to recess integration. The variables indicated in the drawing correspond to the model used to calculated the magnetic force intensity in Figure 2.



▲ Figure 2: The attractive force per unit area as a function of the separation between the pill and the bottom of the recess. The hard magnetic film is 500 nm thick and the Ni film is 200 nm. The pull of gravity on a 6-μm-thick GaAs pill is also indicated.

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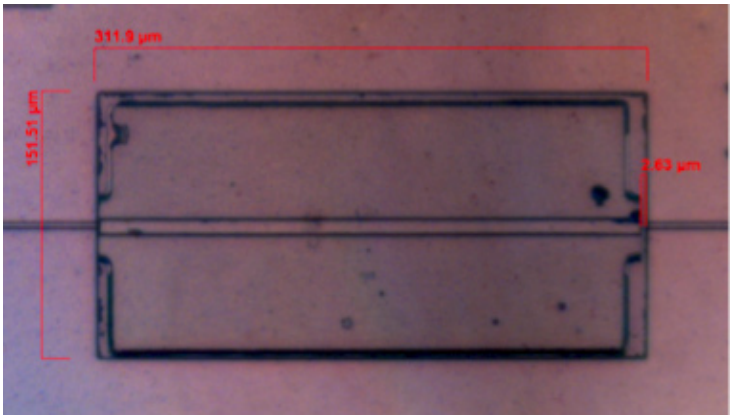
Co-axial Integration of III-V Ridge-waveguide Gain Elements with SiO_xN_y Waveguides on Silicon

E. Barkley, J. Rumpler, J. Perkins, C.G. Fonstad
Sponsorship: DARPA through ARL

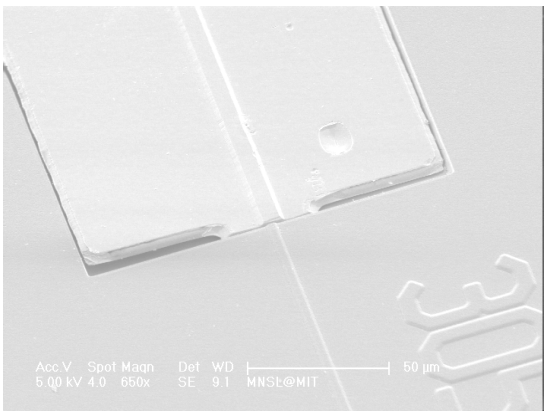
Significant progress has been made fabricating photonic integrated circuits on Si and integrating them with CMOS ICs, but the need for compatible optical gain elements (laser sources and optical amplifiers) still remains. Recently researchers at UCSB and Intel have had good success integrating III-V gain elements with Si-based dielectric waveguides using evanescent coupling [1]. At MIT, we have developed an alternate approach that uses co-axial coupling of III-V ridge waveguide devices and Si-based dielectric waveguides. This integration process includes first fabricating micro-scale device platelets, such as laser diodes (LDs) or optical amplifiers (SOAs), from commercially grown heterostructures, and then assembling these platelets in dielectric recesses etched through silicon oxy-nitride/silicon dioxide waveguides on Si wafers (ultimately this step will be done on IC wafers).

The essential ingredients for efficient coupling between the ridge waveguide devices and the dielectric waveguides are (1) matching the mode profiles, (2) accurately aligning the waveguides laterally and vertically, and (3) minimizing the separation between the guide segments. Standard dry-etch processes can be used to keep the space between the recess wall and the side of the laser small; the vertical offset between the core of the dielectric waveguide and the active region of the in-plane laser is kept small by monitoring layer thicknesses during epitaxy and deposition. To keep the gap between the guide ends small while also having a good cavity end facets, we use precision micro-cleaving; this enables us to control the cavity length to within 1 micron.

Measurements on integrated assemblies with air filling the gap between the guides indicate that coupling losses as low as 5 dB are obtained when the guides are well aligned and the gap is less than 1 micron [2]. Other measurements and computer simulations indicate that using a gap fill with n = 2.2 (e.g., silicon nitride) and improving tailoring of the vertical mode profile in the III-V guide can reduce this loss to below 1 dB. Other work in progress in this program includes integrating angle-mounted SOAs with dielectric waveguides and developing a new laser design using a silicon oxy-nitride waveguide DFB structure and a high-index gap fill.



▲ Figure 1: A photomicrograph showing a top view of a III-V ridge waveguide platelet positioned in a dielectric recess and aligned with a silicon oxy-nitride waveguide. Transmission measurements through passive waveguide assemblies were used to characterize the coupling losses between the two types of guide.



▲ Figure 2: A close-up photomicrograph showing the alignment between an InGaAsP/InP ridge waveguide platelet and a buried silicon oxy-nitride waveguide. Coupling losses as low as 3 dB were measured.

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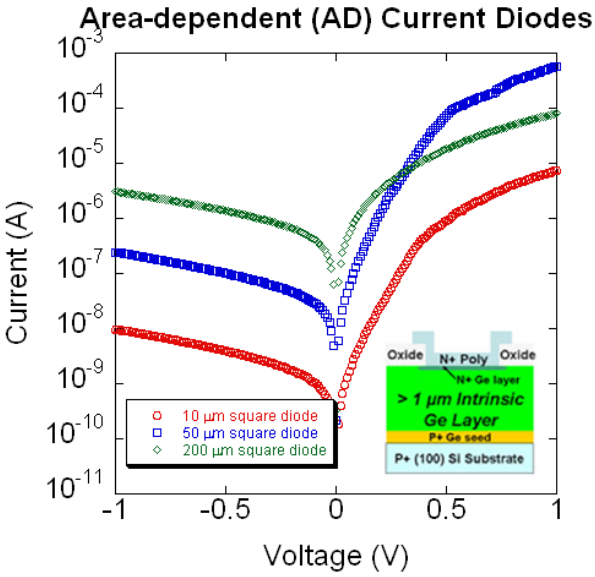
Electrical Characteristics of Ge-on-Si LPCVD-grown Photodiodes

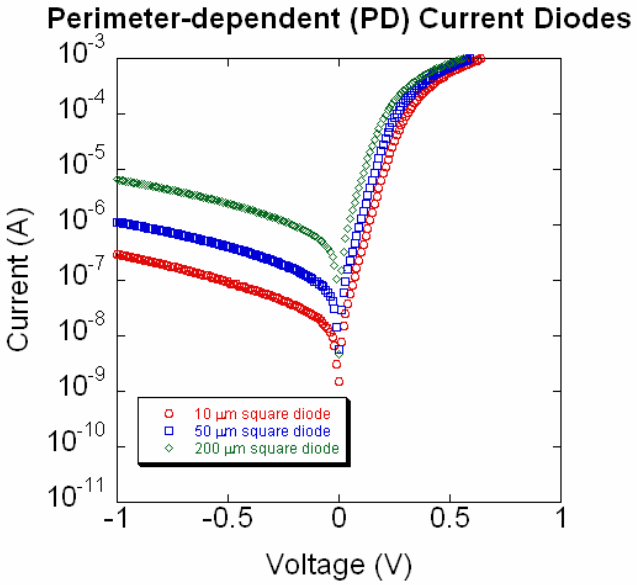
N. DiLello, O.O. Olubuyide, H. Buss, J.L. Hoyt
Sponsorship: DARPA, SRC Student Fellowship

Germanium is a promising candidate for use in CMOS-compatible photodiodes. Its strong absorption in the 1.55-μm range and relative ease of integration on silicon substrates make it suitable for telecommunications systems as well as in other high-speed electronic photonic integrated circuits. An important figure of merit in these photodiodes is the reverse leakage current. o reduce power consumption and improve signal-to-noise ratio, it is important that the diodes have a low leakage current in reverse bias, typically measured at -1 V. This study has investigated the leakage current of germanium photodiodes grown by low-pressure chemical vapor deposition (LPCVD) using an Applied Materials Epitaxial Reactor.

In the diodes that were fabricated and measured, we observed that some had leakage currents that were area-dependent (AD) and some were perimeter-dependent (PD). Figure 1 shows I vs. V curves for area-dominated diodes of various sizes while Figure 2 has the data for PD diodes. Previous measurements of these diodes resulted in an area dependence of $J_A = 8.5$ mA/cm^2 for the AD diodes and $J_A = 2.4$ mA/cm^2 for the PD diodes [1]. Furthermore, these measurements also resulted in a perimeter dependence of $J_P = 50$ nA/cm for the AD diodes and $J_P = 0.06$ mA/cm for the PD diodes [1]. These numbers are quoted at a reverse bias of -1 V. The AD diodes thus have a much lower perimeter leakage current, indicating that the passivation of trap states near the dielectric/Ge interface is much better on the AD diode wafer, compared to the PD diodes. These results motivate further work on materials and processing parameters that improve Ge surface passivation and reduce perimeter leakage currents.



▲ Figure 1: The I vs. V curves for various sizes of square diodes. The leakage current at -1 V scales with the area of the devices. The inset is a cross-sectional view of the Ge-on-Si p-i-n photodiode.



▲ Figure 2: The I vs. V curves for various sizes of square diodes. The leakage current at -1 V scales with the perimeter of the devices.

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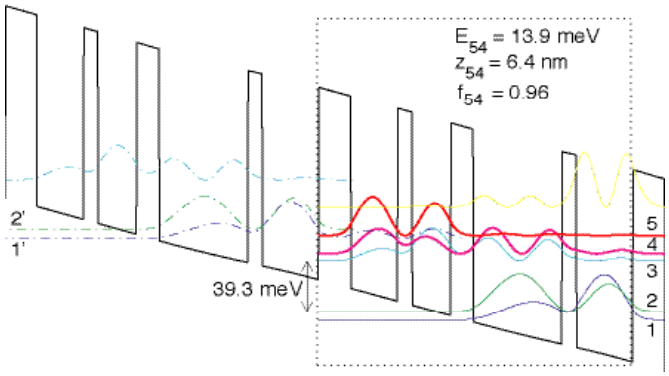
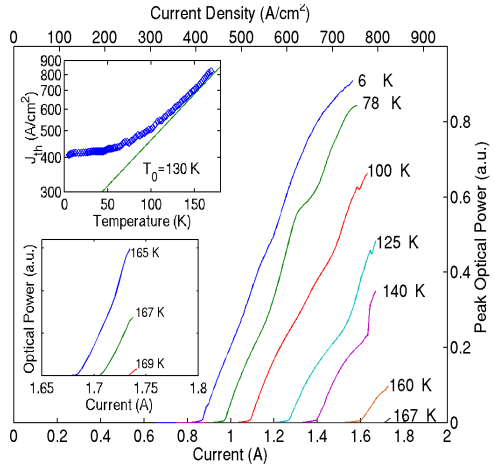
Development of Terahertz Quantum-cascade Lasers

B. Williams, S. Kumar, A. Lee, Q. Qin, Q. Hu (in coll. with J. Reno, Sandia National Lab)
Sponsorship: NSF, NASA, AFOSR

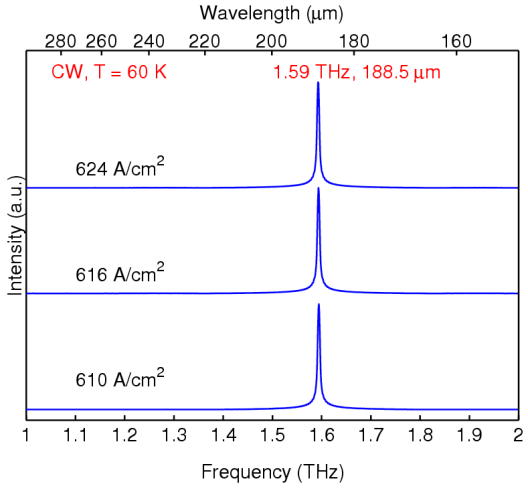
The terahertz frequency range (1-10 THz) has long remained undeveloped, mainly due to the lack of compact, coherent radiation sources. Transitions between sub-bands in semiconductor quantum wells were suggested as a method to generate long wavelength radiation at customizable frequencies. However, because of difficulties in achieving population inversion between narrowly separated sub-bands and mode confinement at long wavelengths, THz lasers based on intersub-band transitions were developed only very recently. We have developed THz quantum-cascade lasers based on resonant-phonon-assisted depopulation and using metal-metal waveguides for mode confinement. The top-left of Figure 2 illustrates schematics of both features are illustrated in the top-left figure. Based on the combination of these two unique features, we have developed many THz QCLs with record performance measurements, including a maximum pulsed operating temperature at ~170 K (top-right), a maximum power of ~250 mW (bottom-right), and the longest wavelength (~190 μm) QCL to date without the assistance of magnetic fields (bottom-left).



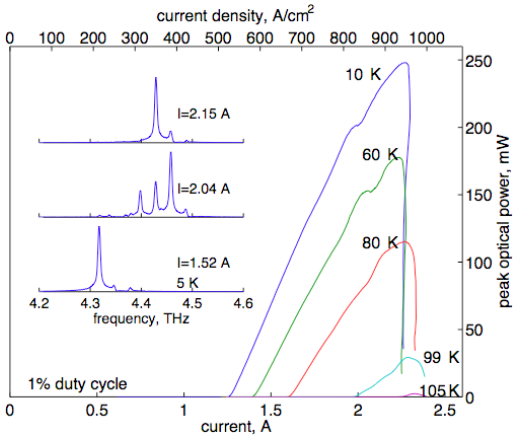
▲ Figure 1



▲ Figure 2



▲ Figure 3

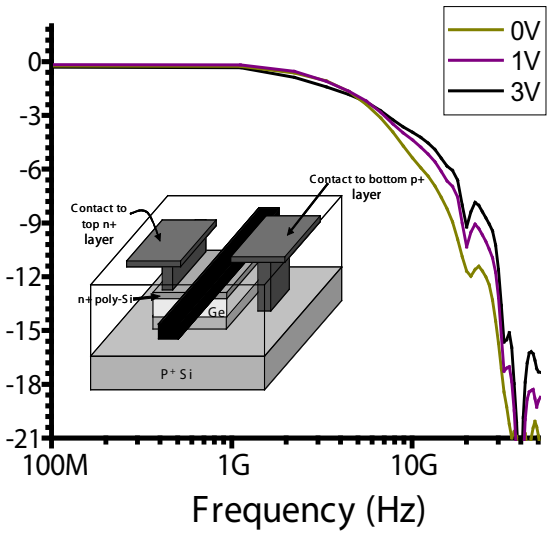


▲ Figure 4

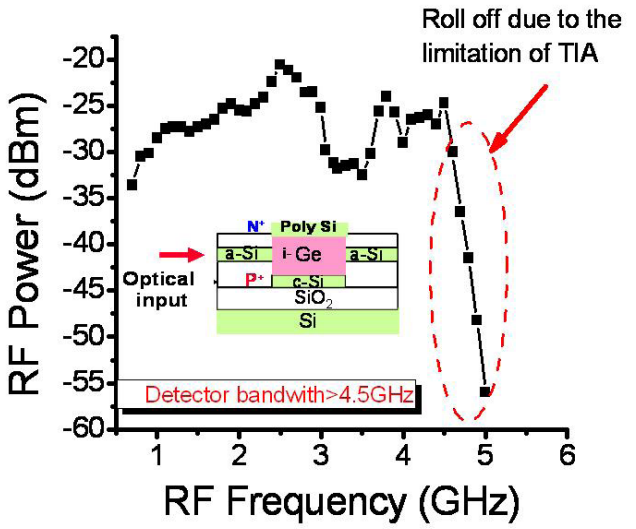
Waveguide-integrated Ge p-i-n Photodetectors on a Si Platform

D. Ahn, J. Liu, C. Hong, M. Beals, J. Michel, L.C. Kimerling
Sponsorship: DARPA EPIC Program

The combined integration of electronic and photonic circuits has become an increasingly promising technology for the high functionality extension of traditional technology shrink. For an electronic-photonic integrated circuit (EPIC) on-chip, an essential component is the waveguide-integrated photodetector on a Si CMOS platform to convert optical signals to electrical ones. We demonstrate high performance Ge p-i-n photodetectors integrated with waveguides on a Si platform with two coupling schemes: vertical coupling and butt-coupling. In the vertical coupling scheme, the light couples evanescently from the waveguide to the Ge detector below it, while in the butt-coupling scheme, the output end of the waveguide directly inputs to the Ge photodetector. With the vertical coupling scheme, a high responsivity of ~1.0 A/W in the wavelength rage of 1470-1570 nm and a 3dB bandwidth of ~7.2 GHz have been demonstrated. With the butt-coupling scheme we have achieved a high responsivity of 1.0 A/W at 1520 nm and a 3dB bandwidth greater than 4.5 GHz. The devices were fabricated completely with a CMOS process, and they can be integrated with CMOS circuitry to achieve electronic and photonic integration on Si.



▲ Figure 1: Frequency response at different reverse biases of a Ge p-i-n photodetector on Si vertically coupled to a silicon nitride waveguide. The inset of the figure schematically shows the structure of the device.



▲ Figure 2: Frequency response at 3V reverse bias of a Ge p-i-n photodetector on Si butt-coupled to a silicon waveguide. The inset of the figure schematically shows the structure of the device.

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[3] J.F. Liu, D. Ahn, C.Y. Hong, D. Pan, S. Jongthammanurak, M. Beals, L.C. Kimerling, J. Michel, A.T. Pomerene, D. Carothers, C. Hill, M. Jaso, K.Y. Tu, Y.K. Chen, S. Patel, M. Rasras, A. White, and D.M. Gill, "Waveguide integrated Ge p-i-n photodetectors on a silicon-on-insulator platform," *Optics Valley of China International Symposium on Optoelectronics*, Nov. 2006, pp. 1-4.

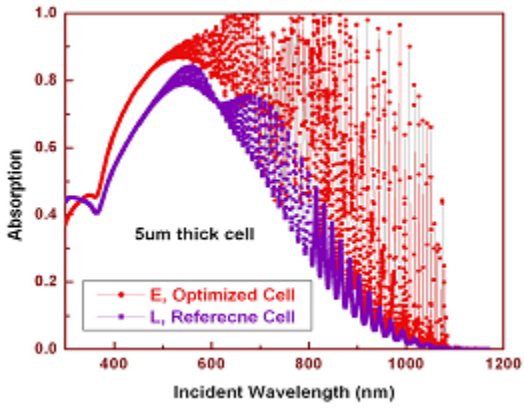
High-efficiency Si Thin-film Solar Cells with Textured Photonic Crystal Backside Reflector

L. Zeng, P. Bermel, Y. Yi, N. Feng, B.A. Alamariu, J. Liu, C. Hong, X. Duan, J.D. Joannopoulos, L.C. Kimerling
Sponsorship: National Renewable Energy Laboratory

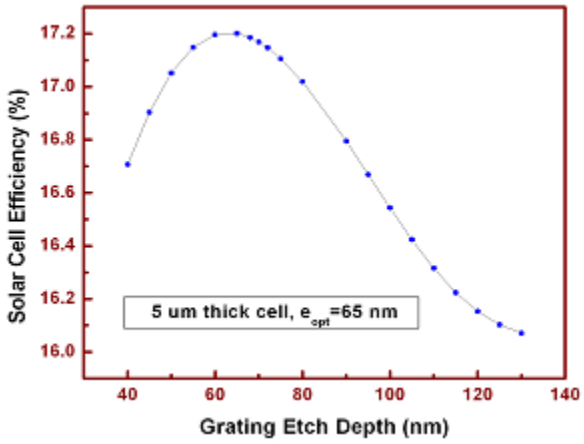
Thin-film solar cells (TFSC) are the leading candidates for next generation photovoltaic applications. Currently, the efficiency of TFSC, however, is very low due to its weak absorption of long wavelength photons. To tackle this problem, we invented a new light-trapping scheme using textured photonic crystal as a backside reflector with a reflectivity as high as 99.8%, which can enormously elongate the optical path length for complete light absorption. It is composed of a reflection grating and a distributed Bragg reflector (DBR) [1]. In this work, optimization of the back reflector is systematically designed and conducted through both simulation and experiments.

The scattering matrix method is used to simulate the efficiency enhancement of solar cells with different back reflector parameters. Specifically, as for the gratings, both 1D and 2D submicron gratings are developed. Regarding 1D gratings, period and etch depth, as well as the duty cycle, are studied in detail and the best combination is realized. In the case of 2D gratings, the influence of variations in two perpendicular directions is explored. As for DBR, SiO_2/Si materials are used, and the period is optimized to make the stopband as wide as required by different solar cell thickness. The highest power conversion efficiency is achieved for a given solar cell thickness with an optimized back reflector structure. Figure 1 shows the significant absorption enhancement in a 5-μm-thick solar cell due to the back reflector. As an example of parameter optimization, Figure 2 depicts grating etch-depth optimization in a 5-μm-thick solar cell, with cell efficiency as the optimization criterion. Furthermore, trends of the variation of optimal back reflector parameters and anti-reflection coating thickness with solar cell thicknesses are identified.

Experimentally, silicon-on-insulator solar cells are fabricated with optimal back reflector parameters to verify the design and avoid complication-of-materials issues. The optimized back reflector design can be readily applied to monocrystalline and polycrystalline Si thin-film solar cells.



▲ Figure 1: Significantly enhanced absorption of a 5-μm-thick Si solar cell due to the back reflector.



▲ Figure 2: Grating etch-depth optimization for a 5-μm-thick Si solar cell to achieve the highest efficiency.

REFERENCES

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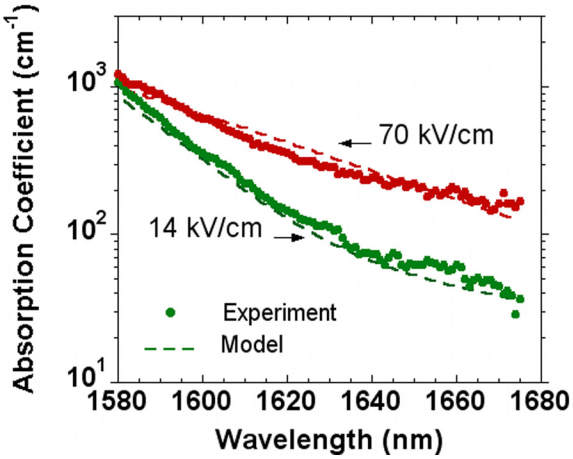
Large Electro-optic Effect in Tensile Strained Ge-on-Si Films

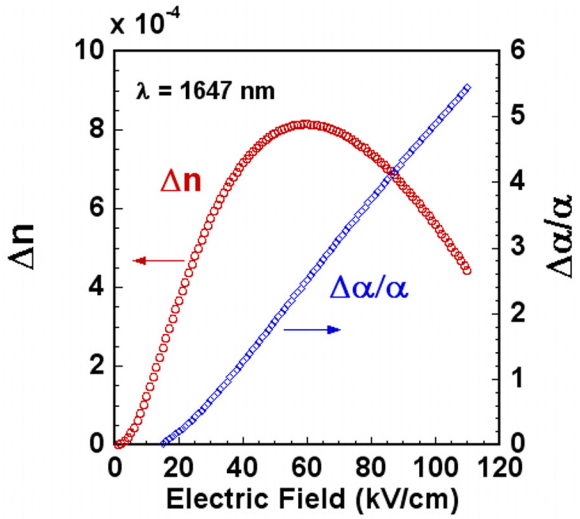
S. Jongthammanurak, J. Liu, K. Wada, D.D. Cannon , D.T. Danielson, D. Pan, L.C. Kimerling, J. Michel
Sponsorship: DARPA EPIC Program

Silicon-based integrated photonic circuits represent a promising technology for high-capacity data communication and high-speed parallel-signal processing [1]. Optical modulators are a key component in these integrated circuits for encoding information on optical carriers. Existing silicon modulators use the plasma dispersion effect to modulate refractive index. The bandwidth limit of these devices is ~1-10GHz [2-3] and is determined by the slower rate of either the injected carrier sweep-out or electron-hole recombination process. While this device represents a new paradigm for electro-optic silicon-based components, its footprint and power dissipation do not scale to levels of high density integration. This report is the first of a study of electric-field modulation of refractive index in silicon-based materials for high-speed applications. We find that germanium integrated monolithically on silicon exhibits a large, field-modulated electro-optic effect in the weakly absorbing regime.

The field-dependence of absorption in the Ge films was measured from spectral responsivity measurements of Ge-on-Si p-i-n diodes. The experimental data were analyzed using the generalized Franz-Keldysh formalism and independently measured valence band edge shifts of the light- and heavy-hole energy positions in response to biaxial stress, using Photoreflectance technique. An electric field of 70kV/cm increased the absorption coefficient from 62 cm^{-1} to 230 cm^{-1} at 1647 nm, in very good agreement with the theory (Figure 1). At 1647 nm, the electro-optic coefficient $\Delta n/F$ for the strained Ge film is 280 pm/V, as compared to 160 pm/V for unstrained Ge. The measured $\Delta\alpha/\alpha$ ratios for the strained and unstrained Ge films are 3.03 and 1.11, respectively (Figure 2). These results show that the Ge-on-Si epitaxial films have significant potential for efficient CMOS-compatible, field-induced, optical modulator devices.



▲ Figure 1: Excellent fit of experimental data to the model based on the generalized Franz-Keldysh formalism without fitting parameters.



▲ Figure 2: Application of the model to predict Δn and $\Delta\alpha/\alpha$ at 1647- nm wavelength *as* a function of the applied electric field.

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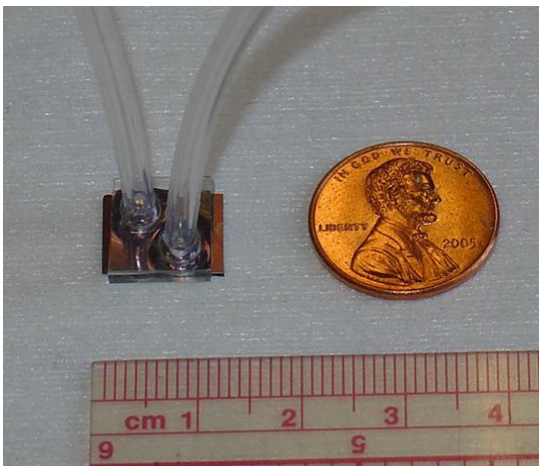
Low-loss Integrated Planar Chalcogenide Waveguides for Microfluidic Chemical Sensing

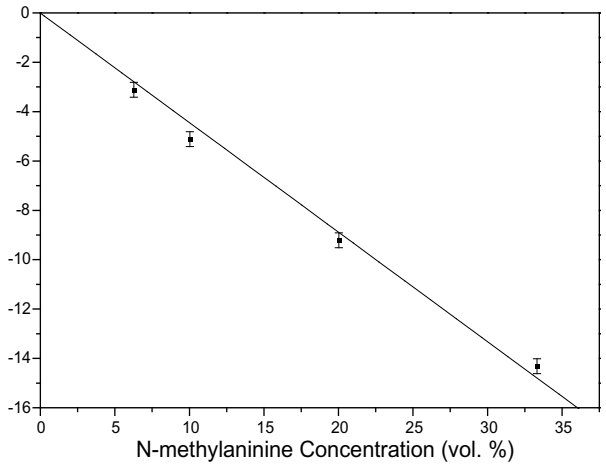
J. Hu, V. Tarasov, N. Carlie, L. Petit, A. Agarwal, K. Richardson, L.C. Kimerling
Sponsorship: DOE

We have fabricated and tested, to the best of our knowledge, the first microfluidic device monolithically integrated with planar chalcogenide glass waveguides on a silicon substrate. High-quality $Ge_{23}Sb_7S_{70}$ glass films have been deposited onto oxide-coated silicon wafers using thermal evaporation, and high-index-contrast channel waveguides have been defined using SF_6 plasma etching. Microfluidic channel patterning in photocurable resin (SU8) and channel sealing by a polydimethylsiloxane (PDMS) cover completed the device fabrication. The chalcogenide waveguides yield a transmission loss of 2.3 dB/cm at 1550 nm.

Sensor performance was tested by monitoring the optical output while injecting a solution of N-methylaniline mixed with a solution of carbon tetrachloride into the microfluidic channel. The N-H bond in N-methylaniline is known to exhibit an absorption peak near 1500 nm, which was used as the characteristic fingerprint for chemical identification in our test. The resultant absorption spectrum exhibits a well-defined absorption peak at 1496 nm, which is in excellent agreement with a traditional absorption measurement carried out on a Cary 5E UV-Vis-NIR dual-beam spectrophotometer. Since carbon tetrachloride is transparent in the wavelength range investigated, this spectral peak is unambiguously assigned to N-H bond vibrational absorption. The peak absorption in dB at 1496 nm was measured for different concentrations of N-methylaniline solution in carbon tetrachloride and the result is shown in Figure 2. The excellent linear fit suggests that the sensor exhibits linear response when varying analyte concentrations. From our experiments, a sensitivity of this sensor down to a N-methylaniline concentration 0.7 vol. % is expected. Given the low-cost fabrication process used and robust device configuration, our integration scheme provides a promising device platform for chemical sensing applications.



▲ Figure 1: Photo of the assembled microfluidic chip with fluid inlet and outlet tubing; The channels and $Ge_{23}Sb_7S_{70}$ waveguides are too small to resolve in the image.



▲ Figure 2: Peak absorption of N-methylaniline solution in carbon tetrachloride at 1496-nm wavelength measured using the waveguide evanescent sensor as a function of N-methylaniline volume concentration, indicating good linearity of the sensor response.

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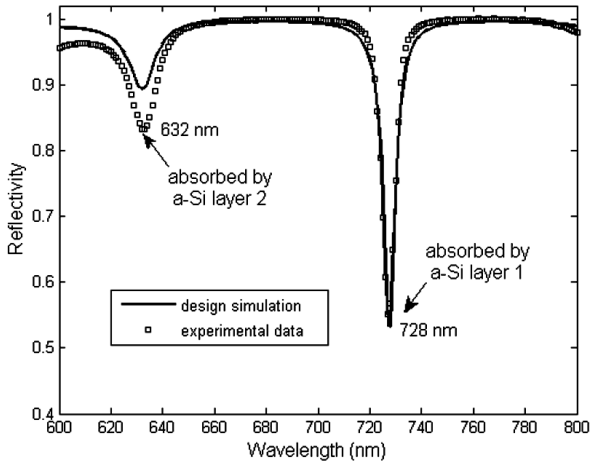
Multispectral One-dimensional Photonic Crystal Photodetector

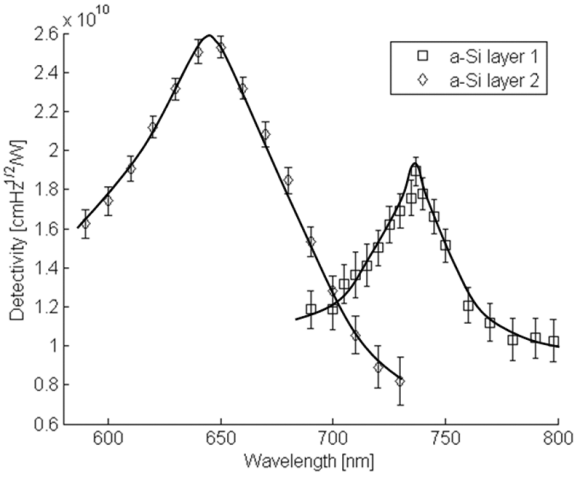
X.C. Sun, J.J. Hu, C.Y. Hong, J.F. Viens, XM. Duan, R. Das, A.M. Agarwal, L.C. Kimerling
Sponsorship: Deshpande Center for Technological Innovation, Lincoln Laboratory

Applications such as multi-chemical detection, biological sensing, multispectral imaging and spectroscopy call for specialized photodetectors that are capable of selectively sensing specific wavelengths simultaneously, namely multispectral photodetection [1-3]. Here we present a designed and fabricated photonic crystal structure incorporating photoconductive layers to achieve simultaneous multispectral detection [4]. This novel photoconductor pixel exploits resonant cavity enhancement (RCE) for multispectral capability, high quantum efficiency, and dramatically suppressed shot noise. In a quarter-wavelength stack (1-D photonic crystal), standing wave patterns (defect modes) form at resonant wavelengths when defect layers are present. If the thicknesses and positions of photoconductive layers are optimally tuned with respect to the modal overlap with the defect modes, each photoconductive layer will selectively absorb only one specific resonant wavelength. Besides multispectral capability, the proposed design features enhanced optical absorption due to the cavity enhancement effect and allows the use of thinner photoconductive layers, which significantly reduces shot noise and improves the performance of photoconductive detectors.

The fabricated device exploits mode discrimination and resonant cavity enhancement to provide simultaneous multispectral detection capability, high quantum efficiency, and dramatically suppressed shot noise. The use of amorphous Si as active material reduces fabrication cost and simplifies device processing by eliminating the complicated single-crystal growth process. Detectivities as high as 2.6×10^{10} cmHz$^{1/2}$W^{-1} and 2.0×10^{10} cmHz$^{1/2}$W^{-1} at the two pre-selected wavelengths, 632nm and 728nm, respectively, were achieved.



▲ Figure 1: Experimental data and transfer matrix simulation result of the photonic crystal stack reflectivity showing two resonant absorption peaks at 632 nm and 728 nm, which are selectively absorbed by the first two of the three amorphous Si layers, respectively.



▲ Figure 2: Detectivity spectra at 10V of the first two amorphous Si photoconductive layers showing wavelength selectivity. Detectivities are calculated from data measured using a tungsten halogen lamp monochromator.

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Super-collimation of Light in Photonic Crystal Slabs

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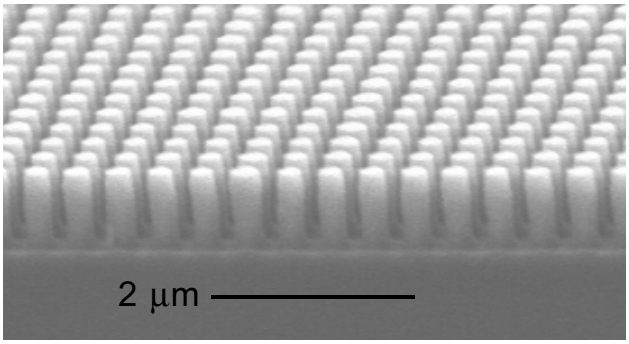
Sponsorship: NSF MRSEC, SRC/FCRP IFC, STTR

A super-collimator is a device in which light is guided by the dispersion properties of a photonic crystal slab rather than by defects or by traditional index guiding. Photonic crystals (PhC) form the essence of the super-collimation effect. The successful fabrication and testing of a super-collimator consisting of a two-dimensional PhC that is composed of a square lattice of cylindrical holes etched into silicon have been performed. Super-collimation for more than 600 isotropic diffraction lengths has been observed for this device (the isotropic diffraction length is the length over which the light beam spreads by square root of 2).

The current goal of the research is to demonstrate super-collimation with a two-dimensional PhC that is composed of a square lattice of cylindrical silicon posts, rather than holes. A super-collimator that is composed of posts allows fluids to more easily fill and flow through the spaces between the posts, making this design more suitable for applications such as chemical sensing. Two fabrication processes have been developed and tested. The device has been fabricated using a silicon-on-insulator wafer in which the low-index silicon dioxide layer (3 μm thick) is used to minimize radiation loss into the high-index silicon substrate. The photonic crystal occupies the entire surface of the super-collimator so that the cleaved edges of the photonic crystal function as input or output facets of the device. The initial design with the help of the Ab Initio Physics Group has focused on realizing super-collimation at a wavelength of 1530 nm so that the lattice constant, post radius, and Si thickness were 437.5 nm, 250 nm, and 700 nm, respectively. Figure 1 is a scanning electron microscope image of the finished device. Testing in collaboration with the Optics and Quantum Electronics Group is in progress.



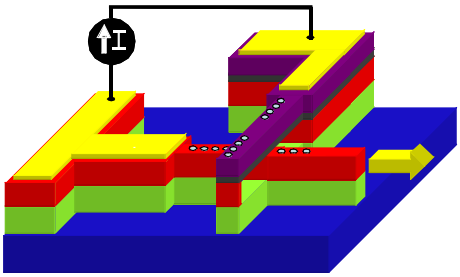
▲ Figure 1: An SEM image of the super-collimator. The silicon posts are 700 nm tall and rest on a 3-μm-thick layer of silicon dioxide on a silicon wafer.

Electrically Activated Nanocavity Laser Using One-dimensional Photonic Crystals

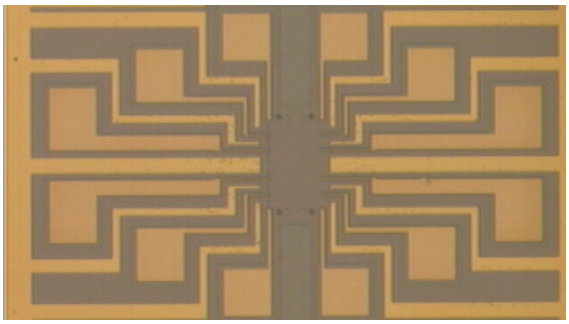
A. Grine, G.S. Petrich, L.A. Kolodziejski
Sponsorship: NSF MRSEC

An electrically-activated nanocavity laser that is capable of being integrated within photonic integrated circuits is being developed. The laser employs two crossed members with embedded one-dimensional photonic crystals in order to create an optical cavity at the intersection. To achieve electrical activation, one of the cross members is doped p-type and the other doped n-type. Hence, a PN-junction is formed at the intersection of the two cross members. Furthermore, one of the cross members is designed to act as a single mode waveguide. By adjusting the reflectivity of the photonic crystals, the light that is generated in the nanocavity is directed towards the output. The electrically-activated nanocavity laser is shown schematically in Figure 1.

The fabrication of the electrically-activated photonic crystal laser is underway. A mixed lithography approach is being employed; conventional contact lithography is being used for the features with dimensions greater than 1 micron while electron beam lithography is being used to define the submicron-sized features. Figure 2 shows a micrograph of the contact pads and wires for twelve lasers on the wafer that is currently being processed. The actual nanocavity portion of the lasers has not been defined yet. At the completion of the fabrication process, the nanocavity lasers will be characterized in collaboration with the Ultrafast Optics and Quantum Electronics Group.



▲ Figure 1: Depiction of the electrically-activated, photonic crystal nanocavity laser. The yellow arrow represents the direction and location of the emitted light.



▲ Figure 2: A micrograph of the contact pads and wiring of the wafer that is currently being processed.

A Nanoelectromechanically Tunable, High-index-contrast, Interference Directional Coupler

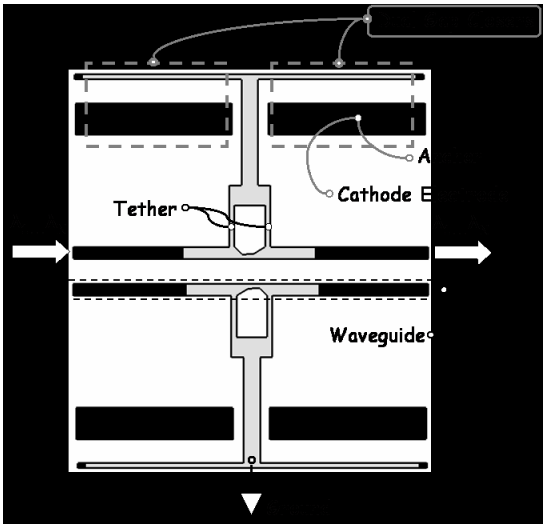
R. Bryant, G.S. Petrich, L.A. Kolodziejski
Sponsorship: NSF MRSEC

Designs that utilize nanoprecision electrostatic mechanical actuation are likely to improve fabrication tolerances for evanescently-coupled, channel waveguide devices. Evanescent couplers, or directional couplers (DC), are notorious for their sensitivity to fabrication irregularities due mainly to the exponential dependence of the evanescent coupling on the waveguide-to-waveguide separations. A design that incorporates growth and fabrication precision as well as electromechanical nanodisplacements can significantly increase fabrication tolerances.

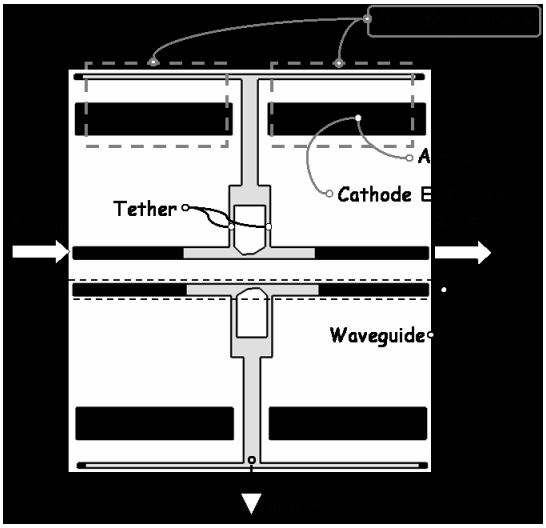
Molecular beam epitaxial (MBE) growth precisely defines channel waveguide heights. The MBE growth is capable of depositing homogeneous planes of material with minimal interdiffusion. Precise channel waveguide separations are achieved by a combination of atomic layer deposition (ALD) of low-index-contrast (LIC) material and nanoelectromechanical (NEM) actuation. The ALD LIC films can uniformly coat features one monolayer at a time, thus precisely defining a waveguide-to-waveguide separation with the coating thicknesses. The NEM actuation establishes intimate contact between the two ALD LIC-coated high-index-contrast channel waveguides. The NEM directional coupler waveguides are only sensitive to fabrication width variations. Optimized DC design can reduce the affect these variations have on the NEM DC.

The NEM-DC waveguides are initially set in an off-resonance state (Figure 1) and are then deflected into an on-resonance state via the application of V_0 volts (Figure 2). The initial off-resonance NEM-DC design scheme allows the waveguides to be lithographically defined as isolated features. All features can also be arranged with separations similar to the waveguide-to-waveguide off-resonances separations without having an optical loss penalty. This arrangement reduces lithographic proximity effects and loading effects associated with species diffusion-based fabrication processes (Reactive Ion Etching, and Oxidation).

Upon being deflected into an on-resonance state (V_0 volts), the two waveguides are brought into mechanically strained intimate contact. Should there be any deviations in width, the separation is preserved by the thickness of the LIC ALD coating. Depending on the application, the static power needed to preserve the strained intimate contact can be removed with the use of mechanical latches.



▲ Figure 1: Schematic of the directional coupler in the unpowered state. The optical signal remains in the upper waveguide.



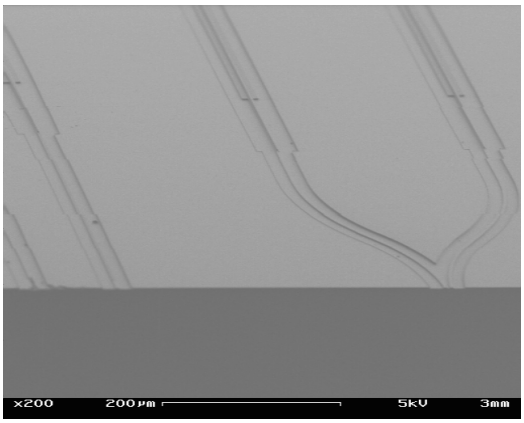
▲ Figure 2: Schematic of the directional coupler in the powered state. The optical signal is coupled into the lower waveguide.

Photonic Integrated Circuits for Ultrafast Optical Logic

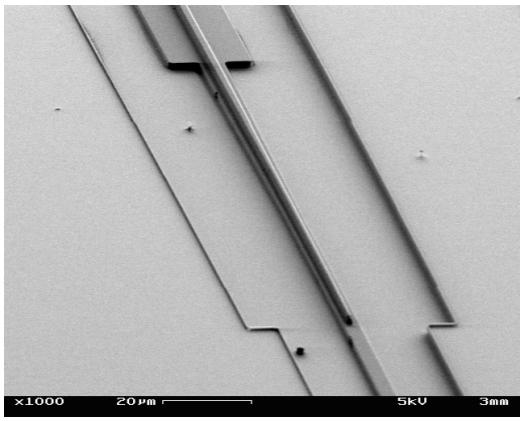
R. Williams, G.S. Petrich, E.P. Ippen, R.J. Ram, L.A. Kolodziejski
Sponsorship: DARPA

The aim of this project is to model and to produce a modular monolithically-integrated, all-optical unit cell capable of performing a complete set of Boolean operations at speeds of hundreds of gigabits per second. Optical logic operations, wavelength conversion, and other advanced optical switching schemes can be implemented using the design. The basic structure consists of a balanced Mach-Zehnder interferometer (Figure 1) with an InGaAsP-based semiconductor optical amplifier in each arm. After investigation of the device design and fabrication tolerances using the beam propagation method and finite-difference time-domain (FDTD) techniques, the critical device dimensions were modeled prior to fabrication.

Fabrication processes have been developed to create the all-optical logic unit cell. The waveguide design calls for the vertical integration of passive waveguides and active amplifiers. With use of an adiabatic taper coupler (Figure 2), the optical mode is transferred between the lower passive waveguide and the upper active waveguide of the twin-waveguide structure. To minimize the amount of InGaAsP material being etched, the waveguides are placed in the center of a trench as seen in the figures. In addition to the optical logic unit cell, isolated components have been fabricated and are being tested to confirm the device design and the computer simulation results.



▲ Figure 1: A scanning electron micrograph of the beginning region of the Mach-Zehnder interferometer (MZI) that is the basis for the optical logic unit cell. Controlling the balance of the semiconductor optical amplifiers in each arm of the MZI permits achievement of basic Boolean functionality.



▲ Figure 2: A scanning electron micrograph showing the active waveguide taper that is used to transfer the optical mode between the lower passive waveguide (lower right) and the upper active waveguide (upper left).

Ultra-broadband Modulator Arrays

O. Shamir, G.S. Petrich, F.X. Kaertner, E.P. Ippen, L.A. Kolodziejski
Sponsorship: DARPA

Creating an arbitrary optical waveform at wavelengths that are centered at 800 nm requires an ultra-broadband modulator array. Since these modulators operate at wavelengths around 800 nm, the material choices are limited to relatively high-Al content AlGaAs and $In_{0.5}(Ga_xAl_{1-x})_{0.5}P$ layers lattice-matched to GaAs. In addition, since GaAs absorbs light with a wavelength less than 870 nm, the lower cladding layer of the modulator must be relatively thick to isolate the modulator from the GaAs substrate. To create the largest optical mode possible and to minimize the coupling loss, the index contrast between the waveguiding layers and the cladding layers should be minimized. Hence, a dilute waveguide structure in which thin layers of high index material are embedded in a low-index material is employed. The resulting layered structure has an effective index slightly higher than the low-index material and is determined by the layer thicknesses as well as the refractive index of the two materials that create the dilute waveguide.

Three slightly different structures were grown by molecular beam epitaxy: (i) an InAlP-based structure in which the dilute waveguide consisted of alternating layers of InAlP and $Al_{0.5}Ga_{0.5}As$, (ii) an $Al_{0.8}Ga_{0.2}As$-based structure in which the dilute waveguide consisted of alternating layers of $Al_{0.8}Ga_{0.2}As$ and InGaP, and (iii) an $Al_{0.8}Ga_{0.2}As$-based structure employing two AlAs layers that can be oxidized. All of the structures are challenging in terms of the epitaxial growth. In the phosphide-based structure, the growth of thick, lattice-matched InAlP cladding layers is challenging due to the need to maintain the lattice-matched condition and due to possible anion ordering. In the arsenide-based structure, although the use of $Al_{0.8}Ga_{0.2}As$ for the cladding layer minimizes the lattice mismatch problem, achieving high-quality, high-Al content AlGaAs cladding layers is difficult due to the low Al adatom mobility on the surface during growth. The third structure with AlAs layers that can be oxidized enables the optical mode to be strongly confined in the vertical direction, allows unipolar operation due to the insulating Al_xO_y layers, and allows high operating voltages to be used. To minimize free-carrier loss in the first two structures, the modulator uses a P-I-N structure in which the Si and Be dopants are graded from the contact layers to the dilute waveguide region.

The first two structures are anticipated to have similar optical mode profiles; the structures are designed to be single mode in a 2-μm-wide ridge waveguide. Using OptiBPM, the fundamental mode for the phosphide-based structure is calculated to be roughly 2 μm x 1 μm (WxH); a similar mode profile exists for the arsenide-based structure. In both structures, if the dilute waveguide is not completely etched, due to the low index contrast of the dilute waveguides, the bending radius is quite large, on the order of a millimeter. The optical mode of the third structure is calculated to be roughly 1.5 μm x 1 μm (WxH). The mode in this structure is more tightly confined due to the low-index Al_xO_y layers.

Fabrication is underway using a mask set containing Mach-Zehnder interferometer modulators of various lengths with multimode interference couplers or Y-splitters. The Mach-Zehnder interferometer modulators as well as conventional modulators are oriented both parallel and perpendicular to the major flat of the 2" GaAs (100) wafers. The mask set also contains a variety of passive components, such as Y-splitters and multimode interference couplers, as well as straight and curved waveguides.

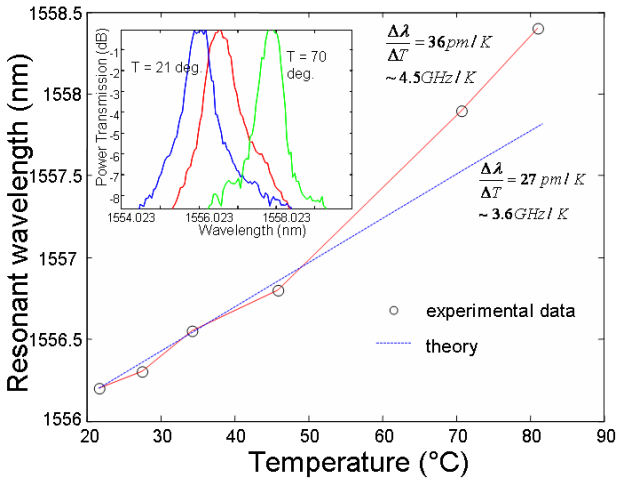
Low-power Thermal Tuning of Second-order Microring Resonator

R. Amatya, R.J. Ram
Sponsorship: DARPA

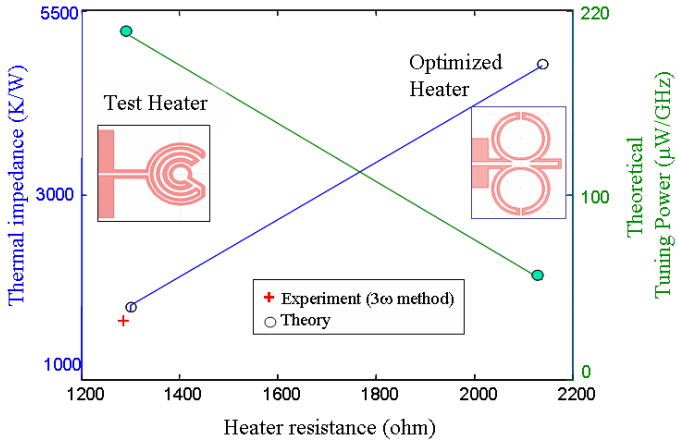
Thermal tuning is one of the mechanisms to achieve active functionality from the ring resonators. These structures can be used as tunable filters, wavelength switches, add-drop multiplexers, converters, and modulators. Polymer waveguides have been reported with very efficient thermal tuning due to their low thermal conductivity and high thermo-optic coefficients. The InP/InGaAsP microrings fabricated with waferbonding using polymer (BCB) have been tuned with power consumption of 26μW/GHz [1]. A CMOS-compatible, SiN ring has been reported with a tuning efficiency of 20pm/K and a tuning power of 400μW/GHz [2]. We show theoretical simulation for efficient thermal tuning of SiN second-order filters using a tuning power of 60μW/GHz. This is the first attempt at such low-power, efficient thermal tuning for a high-order microring resonator.

Second-order filters are fabricated with silicon-rich SiN (n = 2.2) cores and silicon oxide (SiO_2) as a lower cladding and hydrogen silsequioxane (HSQ) as the upper and side cladding. Fabrication and design details for the resonator are described in [3]. The thermo-optic coefficient ($\Delta n/\Delta T$) is temperature- as well as wavelength-dependent. At 1.55 μm, the thermo-optic coefficients for SiN and SiO_2 are 4e-5 K^{-1} and 1.5e-5 K^{-1} respectively. The theoretical tuning range for the waveguide is calculated to be 27pm/K. Before cladding deposition, we performed initial measurements on second-order filters with air as the upper cladding using external heaters. The change in center wavelength (Figure 1) is approximately 36pm/K. Due to slight variation in the group index of the waveguide with air cladding as compared to the HSQ cladding, the experimental tuning range is different from the theoretical value.

Optimized thin film titanium heaters (100nm) are designed to sit on top of the cladding to locally change the temperature of the resonator. Finite-element thermal simulation (FEMLAB) gives the temperature profile for the filter showing approximately one-dimensional heat flow with very low thermal cross-talk. Heaters with high thermal impedance are appropriate in order to minimize power dissipation for thermal tuning. Figure 2 shows the proposed heater design along with test heater data showing thermal impedance and tuning power. The total tuning power for the finalized heater design is less than 60μW/GHz with a tuning range of 150GHz for 40K change in the ring temperature. The 3ω technique has been used to validate the thermal impedance of the test heater.



▲ Figure 1: Thermal tuning for the second-order filter is observed by changing the temperature of the rings. A total shift of 2.2 nm is seen, due to heating the rings from 21°C - 81°C. Inset shows the drop port spectra.



▲ Figure 2: Experimental and theoretical measurements of impedance for a test heater. Final heater design simulation shows low tuning power and high thermal impedance.

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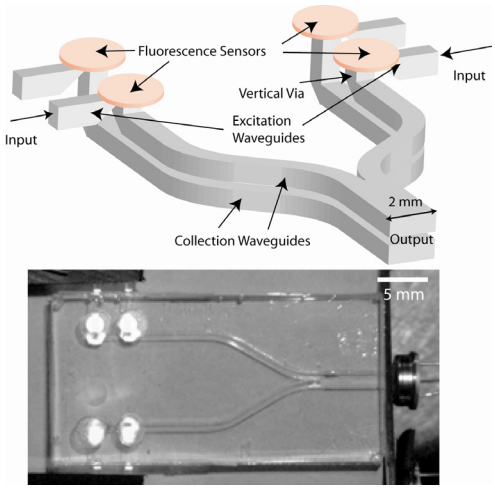
Frequency-multiplexed Fluorescence-detection Arrays in Polymer Waveguide Backplanes

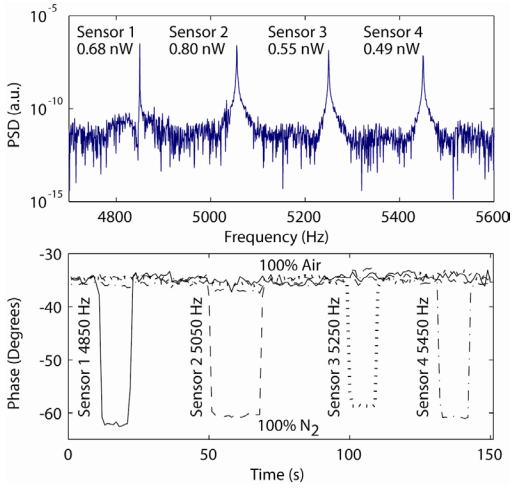
K.S. Lee, R.J. Ram
Sponsorship: CMSE, Government of Malaysia

Many biochip systems require optical detection at discrete locations, such as flow cytometers, PCR chips, and bioreactors [1-3]. As these systems become more integrated and parallel, multiple fluorescence sources in various locations on-chip, often with overlapping spectra, must be detected. To provide sensors for these systems, optical detection must be made scalable, compact, and cheap, utilizing non-imaging optics such as waveguides and reducing off-chip components such as photodetectors and photomultiplier tubes. Frequency division multiplexing (FDM) has been explored as a method to reduce component costs and increase speed for multichannel fluorescence microscopes [4]. We extend this detection approach by combining waveguides with frequency multiplexing as a low-cost and scalable approach for the accurate detection of multiple fluorescence signals located within a single chip.

Figure 1 shows a schematic of the fabricated waveguide array. Four waveguides in the upper layer provide excitation to the fluorescent sources above the chip. The emission is then collected through the vertical vias and reflected into the collection waveguides. All four collected signals are then combined and detected with a single silicon PIN photodiode. To test the multiplexing capability of the system, four oxygen-sensitive lifetime-based fluorophors (PtOEPK) [5] were excited at different frequencies. The step response of each sensor was measured by exposing each sensor to a burst of nitrogen in series and measuring the fluorescence output of all sensors. As shown in Figure 2, the modulation frequency of each sensor is distinguishable and sensor responses can be measured individually with minimal cross-talk. With use of frequency multiplexing, data acquisition can be performed significantly faster with fewer detectors, a necessity for compact integrated systems.



▲ Figure 1: Schematic and image of the waveguide array. Individual excitation waveguides provide different modulation frequencies to sensors located above the waveguide chip. All collected fluorescence is then routed to a single detector, minimizing the number of detection components.



▲ Figure 2: Detected output from four different fluorescence lifetime-based oxygen sensors during nitrogen step responses. Modulated signals are spaced by 200 Hz and phase detection is performed digitally. Since the fluorescence lifetime is sensitive to oxygen, a measured phase change relates to oxygen concentration.

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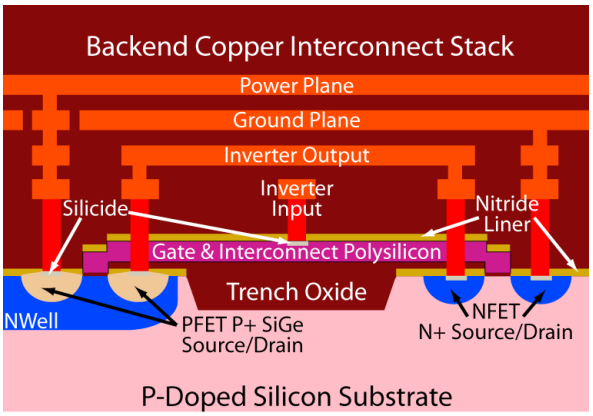
Towards Front-end CMOS-compatible Photonic Devices for High Bandwidth Density, Ultra-low-power, Core-to-Memory Communications

J.S. Orcutt, M. Popovic, F. Gan, A. Khilo, N. Dilello, J.L. Hoyt, F. Kaertner, V. Stojanović, R.J. Ram
Sponsorship: DARPA

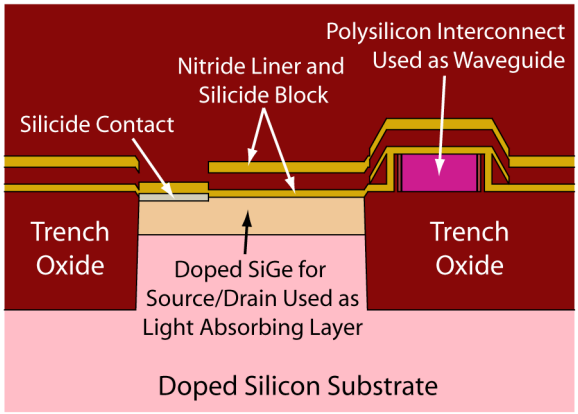
For the past few decades, CMOS technology generation scaling has pushed forward digital electronic chips and all fields that rely upon them. Unfortunately, the overall system performance is no longer improving as rapidly, due to bottlenecks such as interconnect performance. Unfortunately, as the computing cores scale so that many can be fit onto a single chip, the electronic communication busses to supply them with information, especially to and from main memory, do not scale with the required energy and density efficiency.

One solution is to replace the electrical I/O network with an optical one. If wavelength division multiplexing (WDM) is utilized, the bandwidth per micron of chip real-estate used could be drastically improved with respect to electrical links. Additionally, since the relevant challenges for the on-chip optics are to modulate, distribute, and detect light fed in from an off-chip laser source as opposed to providing the energy to drive the capacitance of the electrical interconnect, optics has the potential to be more energy efficient [1].

The optoelectronic components then required for this link are an energy efficient modulator and photodiode. However, since the goal of this project is to replace existing electronics with optics, we are attempting to realize these components in the existing scaled CMOS layers shown in Figure 1. We have chosen to explore using the polysilicon interconnect layer as the waveguide cores for the optical busses. Therefore, the required photon energy must be below that of the silicon band edge to minimize absorption. Given this constraint, we propose using the silicon-germanium already present for strain engineering in the PFET source/drains to act as our absorber (see Figure 2 for details). Previous silicon photonics projects have already demonstrated a promising silicon modulator in a specialized process flow [2]. The remaining challenge for this project is to optimize the existing design for short reach digital communication while changing the active material from single crystalline silicon to polysilicon.



▲ Figure 1: Cross-section cartoon of a typical CMOS inverter in a scaled CMOS node. Relevant features and material layers are labeled above. The challenge for optics is to take these existing layers and use them for a new application.



▲ Figure 2: Cross-section of a proposed silicon-germanium photodetector laterally coupled to a polysilicon waveguide. The first few layers of interconnect metal are left empty so as not to interfere with the optics.

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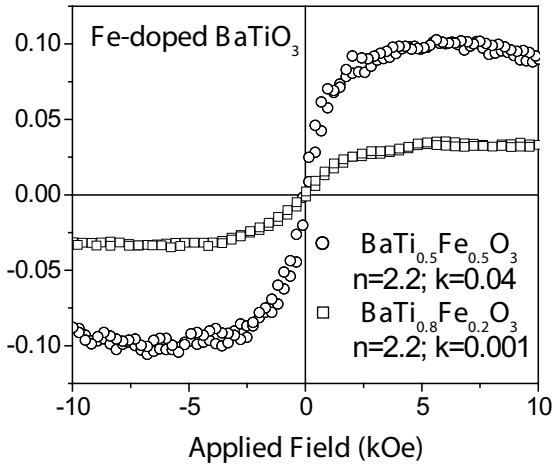
Magnetic Oxides for Optical Isolators and Magnetoelectronic Devices

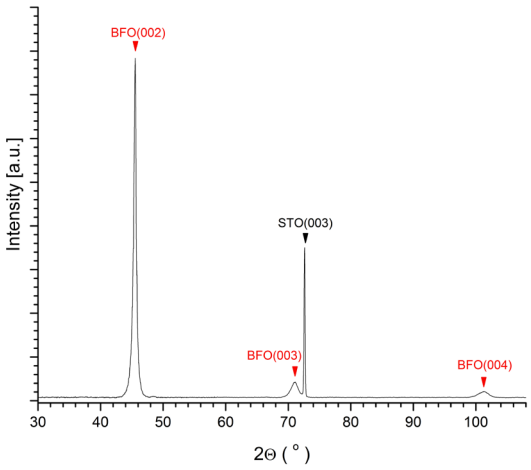
C.A. Ross, G.J. Dionne, A. Taussig, L. Bi, V. Sivakumar, H.S. Kim
Sponsorship: Lincoln Laboratory, ISN, MicroPhotonics Consortium

We have established a thin-film laboratory that includes a pulsed-laser deposition (PLD) system and an ultra-high vacuum sputter/analysis system. In PLD, a high-energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. The PLD is particularly useful for making complex materials such as oxides because it preserves the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magneto-optical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magneto-optical isolators in conventional photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite) grows very well on MgO or Si, with high Faraday rotation but its optical absorption is high. One way to solve this problem is to develop new magneto-optical active perovskite structure materials, which grow well on MgO or $SrTiO_3$. We have examined Fe-doped barium titanate thin film (Figure 1) [1], which shows strong magneto-optical property and weak optical absorption. Recently we are also aiming to fabricate double perovskite thin film with magnetically ordered Fe sites to produce high magneto-optical properties. Epitaxial $BiFeO_3$ thin film on $SrTiO_3$ substrate has been fabricated (Figure 2), and we are trying to modify its magneto-optical property by doping. These films could be useful for waveguide isolators and other magnetoelectronic devices in which optical absorption losses are critical. A second project involves the use of electrochemical methods to control the magnetization of iron oxide spinel structure films (magnetite or maghemite) grown on conducting substrates, making a chemically-switchable material. The insertion of Li ions by electrochemical discharge changes the oxidation state of the Fe(III) to Fe(II) and can reduce the magnetization of the film by about 30%, in a reversible process. Recent experiments on nanoparticles of iron oxide show much greater changes in magnetization, up to ~80%, indicating that the process is kinetically limited.



▲ Figure 1: Faraday rotation vs. applied field for 750-nm-thick $BaTi_{0.5}Fe_{0.5}O_3$ and $BaTi_{0.5}Fe_{0.5}O_3$ films grown in a vacuum on MgO substrates, with the field perpendicular to the film.



▲ Figure 2: X-ray diffraction spectrum of 260-nm-thick $BiFeO_3$ epitaxial film on $SrTiO_3$ substrate.

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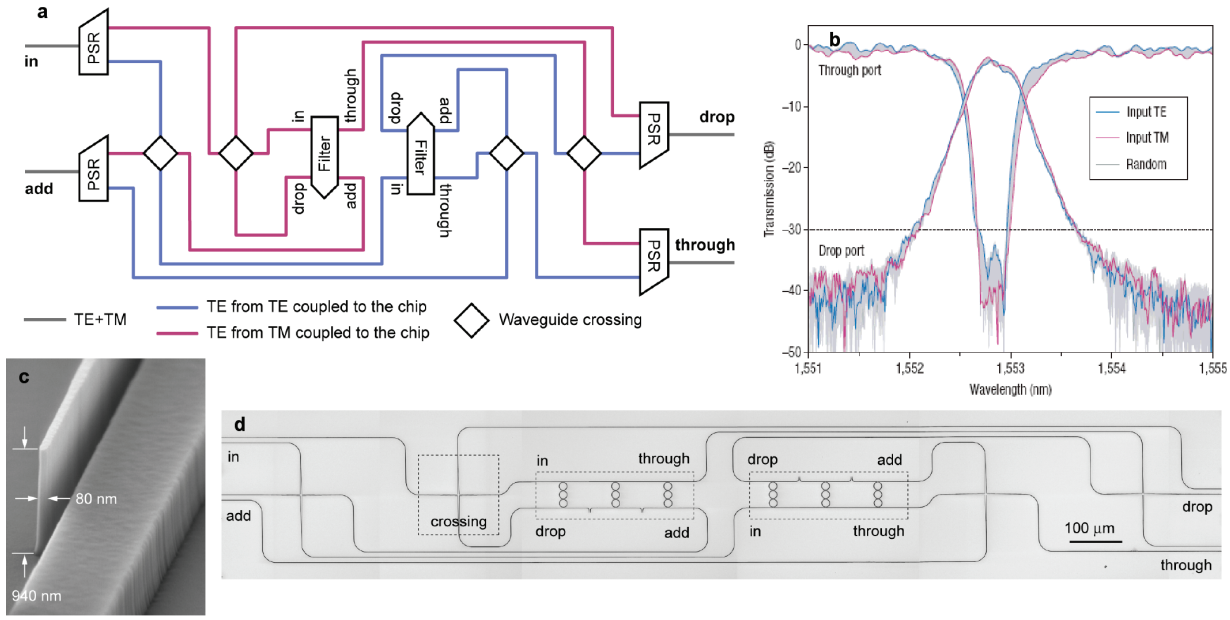
Polarization-transparent Optical Add-drop Multiplexers in Silicon Nitride

T. Barwicz, M.R. Watts, M.A. Popovic, P.T. Rakich, C.W. Holzwarth, E.P. Ippen, F.X. Kaertner, H.I. Smith
Sponsorship: Pirelli S.p.A, internal funds

Microphotonics promises to revolutionize optics through miniaturization and dense integration of optical elements on planar surfaces. Of particular interest are microphotonic devices that employ high refractive-index contrast (HIC). These devices have dimensions on the order of the optical wavelength and functionality often not achievable with macro-scale devices. A long-standing criticism of HIC microphotonic devices, however, is their inherent sensitivity to polarization; i.e., they respond differently to light polarized along different axes. Since the polarization state changes randomly in optical fibers, HIC microphotonic devices are incompatible with the optical fibers necessary to connect them to the outside world.

In the NanoStructures Laboratory, we have developed techniques that enable the fabrication of microphotonic devices, such as microring-based filters, that have unprecedented dimensional accuracy, resulting in unprecedented optical performance. In addition, we have overcome the problem of sensitivity to polarization by means of an integrated polarization-diversity scheme that renders the optical response of HIC microphotonic devices and systems insensitive to polarization. An optical add-drop multiplexer was realized and the polarization-dependent loss reduced to an average of 1 dB [2]. Figure 1 presents the optical circuit diagram implemented, the optical response, and electron micrographs of the structure. The waveguides are fabricated in silicon-rich silicon nitride, and the critical dimensions vary from 70 to 3000 nm. The average waveguide widths of the 18 microrings forming the add-drop multiplexer are matched to 0.15 nm. The aspect ratio of the tallest and thinnest structures reaches 12 to 1.



▲ Figure 1: (a) Optical circuit required to obtain a polarization -nsensitive optical response from polarization-sensitive components. The acronym PSR stands for polarization splitter and rotator. The two filters shown in the schematic are identical. (b) Device response with a mean polarization dependent loss of 1 dB. (c) Electron micrograph of the beginning end of the polarization splitter and rotator. (d) Optical micrograph of the middle part of the circuit. The polarization splitters and rotators, which are not shown, extend to the right and the left of the micrograph. The grayscale was inverted to allow the fine lines to be readable when printed.

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Fabrication of Nanostructured Optical Fiber-to-chip Couplers

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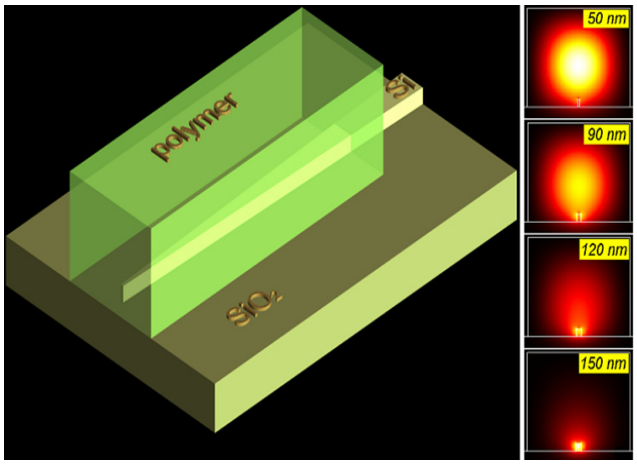
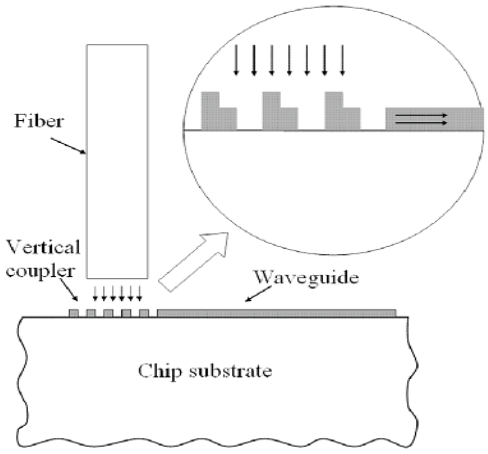
Sponsorship: DARPA

Efficient fiber-to-chip coupling is a significant problem for high-index-contrast (HIC) microphotonics due to the large difference in size and refractive index between the core of an optical fiber (several micrometers in diameter) and the core of a HIC waveguide (less than one micrometer wide). An efficient fiber-to-chip coupler is thus needed to match the mode of the fiber and transform it to a propagating mode within the HIC waveguide. We investigated two different approaches to accomplish the efficient coupling. In the first design, called a horizontal coupler, a large polymer waveguide, with a mode diameter that nearly matches the mode diameter of an optical fiber, sits on a small silicon waveguide whose width tapers from 30 to 450 nm. This taper allows the optical power to be transferred adiabatically from the polymer waveguide to the silicon waveguide. Figure 1 shows a three-dimensional view of the horizontal coupler design. Fabrication is done on silicon-on insulator wafers, so that the buried oxide functions as an undercladding, preventing optical modes from extending into the substrate. With only slight modifications, this design can be made compatible with overclad photonic devices. The second design, the vertical coupler, is based on a grating array composed of nanoscale elements that allow coupling from a vertically oriented fiber to a horizontally oriented waveguide. We are currently demonstrating this concept using silicon-rich silicon-nitride waveguides. Figure 2 shows a sketch of the vertical-coupler design. The minimum feature size is ~100 nm.



▲ Figure 1: Three-dimensional view of horizontal coupler.



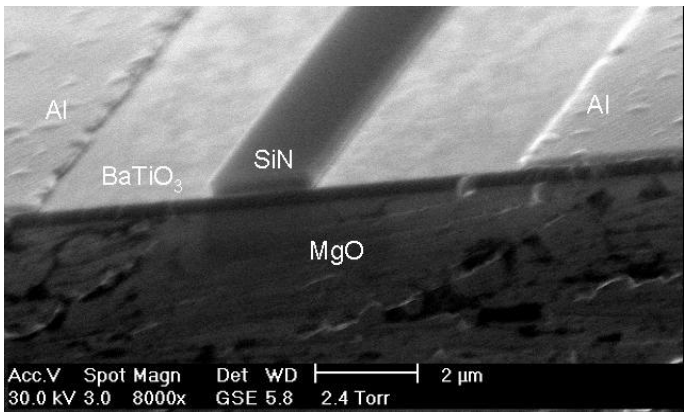
▲ Figure 2: Sketch of a vertical coupler.

A $BaTiO_3$-based Electro-optic Thin-film Waveguide Modulator

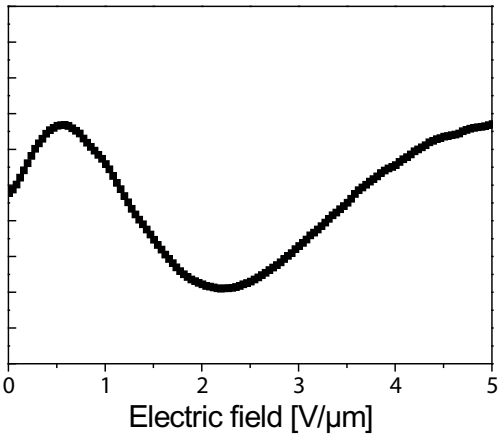
J. Hiltunen, D. Seneviratne, H.L. Tuller (in coll. with J. Yasaitis)
Sponsorship: Analog Devices

The drive towards integrated photonics requires the integration of various optical devices on a chip including an optical modulator. Currently, optical modulation with active waveguiding structures is implemented using $LiNbO_3$ single crystals. These devices require complex and expensive fabrication processes. In addition, their relatively low electro-optic coefficient leads to large component sizes, limiting miniaturization. The current demands for an increased degree of integration with cost-efficient device fabrication can, in principle, be met using thin films of barium titanate [1-3]. In bulk form, this material possesses a superior electro-optic coefficient. Applications using thin-film structures necessitate careful study of processing parameters and their impact on material properties. Our efforts are geared towards gaining a fundamental knowledge of the behavior of thin film barium titanate ($BaTiO_3$) and developing processes to fabricate devices for applications in optical data transmission and processing.

The focus is on optimizing the electro-optic response of $BaTiO_3$ and related thin-film materials deposited by pulsed laser deposition (PLD) and sputtering onto single-crystal substrates directly or with buffer layers. Figure 1 shows a cross section of a waveguide Mach-Zehnder interferometer structure, using a SiN strip-loaded waveguide. The optical waveguide structure is formed by growing a Si_xN_y layer with plasma-enhanced-chemical-vapor-deposition (PECVD) on $BaTiO_3$ and patterning it lithographically. This is followed by the sputtering and patterning of Al electrodes next to one arm of the Mach-Zehnder structure. The operation of the interferometer is characterized by launching polarized light into the waveguide and measuring the modulation of the output intensity as a function of applied voltage. A typical DC response of a sample electro-optic modulator based on barium titanate is shown in Figure 2. We have demonstrated an effective electro-optic coefficient as high as 85pm/V with $BaTiO_3/SrTiO_3$ superlattices, which is considerably greater than that available with bulk $LiNbO_3$ crystals.



▲ Figure 1: Cross section of the Mach-Zehnder waveguide modulator.



▲ Figure 2: Measured optical intensity at the Mach-Zehnder waveguide modulator output as a function of electric field between adjacent electrodes.

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Section 6

MTL RESEARCH CENTERS

Center for Integrated Circuits and Systems

Prof. Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Seven faculty members participate in the CICS: Hae-Seung Lee (director), Michael Perrott (associate director), Anantha Chandrakasan, Joel Dawson, David Perreault, Charles Sodini, and Vladimir Stojanovic. CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, DC-DC converters, among others.

We strongly believe in the synergistic relationship between industry and academia, especially in practical research areas of integrated circuits and systems. We are convinced that CICS is the conduit for such synergy. At present, participating companies include Analog Devices, Bosch, Intel, IBM, Linear Technology, Marvell Technology Group, Maxim Integrated Products, National Semiconductor, NXP, Qualcomm, and Texas Instruments.

CICS's research portfolio includes all research projects that the seven participating faculty members conduct, regardless of source(s) of funding, with a few exceptions. (A very small number of projects have restrictions on information dissemination placed on them due to the nature of funding.)

Technical interaction between industry and MIT researchers occurs both on a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication between MIT faculty and students and industry. We hold two informal technical meetings per year open to participating companies. Throughout each full day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet, giving early access to meeting attendees. Participating companies then offer valuable technical feedback, as well as suggestions for future research. We have held bi-annual meetings each year, and the response from industry has been overwhelmingly positive.

More intimate interaction between MIT researchers and industry takes place while working on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT. The result is truly synergistic, and we strongly believe that it will have a lasting impact in the field of integrated circuits and systems.

MTL RESEARCH CENTERS

Intelligent Transporation Research Center

Dr. Ichiro Masaki, Director

Transportation is an important infrastructure for our society. It is time to propose a new transportation scheme for resolving the increasing transportation problems. In responding to social needs, MIT's Microsystems Technology Laboratories established the Intelligent Transportation Research Center (ITRC) in September 1998 as a contact point of industry, government, and academia for ITS research and development.

ITRC focuses on the key Intelligent Transportation Systems (ITS) technologies, including an integrated network of transportation information, automatic crash & incident detection, notification and response, advanced crash avoidance technology, advanced transportation monitoring and management, etc., in order to improve the safety, security, efficiency, mobile access, and environment. There are two emphasis for research conduced in the center:

- The integration of component technology research and system design research.
- The integration of technical possibilities and social needs.

ITRC proposes the incremental conversion and development process from current to near and far future systems and develops enabling key components in collaboration with the government, industries, and other institutions. Other necessary steps are the integration of technical, social, economical, and political aspects. The integration of the Intelligent Transportation Systems in different countries is also essential. The integration of vehicles, roads, and other modes of transportation, such as railways and public buses, are all imperative.

These integrations are fulfilled with the cooperation of researchers in various fields, including the Microsystems Technology Laboratory (MTL), the Research Laboratory of Electronics (RLE), the Artificial Intelligence Laboratory (AI), the Center for Transportation Studies (CTS), the Age Laboratory, the Department of Electrical Engineering and Computer Science, the Department of Civil and Environmental Engineering, the Department of Aeronautics and Astronautics, and the Sloan School of Management. The research center has 8 MIT faculty and several visiting professors and scientists. The director of the center is Dr. Ichiro Masaki.

MTL RESEARCH CENTERS

MEMS@MIT

Prof. Martin A. Schmidt, Director

The MEMS@MIT Center serves to unite the wide-ranging campus activities in Micro/nano systems and MEMS with forward-looking industrial organizations. Currently, MEMS@MIT is comprised of more than 125 faculty, students, and staff working on a broad research agenda and supported by more than $12 million/year in research sponsorship. The MEMS research efforts on campus focus on three overarching themes:

i) Biological, Chemical and Medical MEMS – includes work on manipulation and processing of biologically-relevant materials of varying size scales from tissue engineering scaffolds and cell manipulation, to devices for separation and sorting of DNA and proteins, sensing platforms for detection of biomolecules, a wide range of microfluidic devices, and microchemical systems for synthesis and characterization

ii) Power MEMS – includes work on energy scavenging by vibration harvesting, various approaches to fuel burning power generation, eg. thermo- photovoltaics, fuel cells, microturbines

iii) Enabling Technologies – includes work on MEMS processes and process modeling (eg. materials characterization, CAD tools and novel metrology methods), and micro and nano-mechanical devices, ie. switches, actuators, and self-assembled devices.

Membership benefits include:

- Insight to newest ideas in MEMS
- Early access to research results
- Early awareness of IP generated for licensing
- Access to high quality continuing education materials
- Partnering for federal or other funding opportunities
- Recruitment of leading MIT graduates

MTL RESEARCH CENTERS

MIT Center for Integrated Photonic Systems

Prof. Rajeev J. Ram, Director

The goals of the Center for Integrated Photonic Systems are:

1. To provide leadership and direction for research and development in photonics.

The core activity of CIPS is the development of a long-range vision for research and the development of integrated photonic devices & systems. CIPS will host forums and facilitate working groups with industrial consortium members to identify and discuss technology and road mapping issues:

- technology directions
- potential disruptive technologies
- technical barriers (gaps)
- actions needed to enable future-generation systems, and
- manufacturing and market issues that drive timing of technology deployment.

As an academic institution we can work openly with a variety of different organizations in developing and gathering input for our models. Whether it is performance data for new devices 'in the lab,' yield data for existing manufacturing processes, planning documents, or first-hand observations of the corporate decision making process, CIPS researchers benefit greatly from the unique relationship between MIT and industry. The level of detail and intellectual rigor of the models being developed here is complemented by the high quality of data available to us. CIPS researchers are developing models of optical and electronic devices, the packages they are wrapped inside, the manufacturing processes that assemble them, the standards that define them, the market that buys them, and the policy processes which influence their deployment.

2. To foster an Institute wide community of researchers in the field of integrated photonics & systems.

The Departments of Electrical Engineering and Computer Science, Materials Science and Engineering, Mechanical Engineering and Economics are consistently ranked as the top graduate programs in the country. Likewise, the Sloan School of Management has consistently ranked first in the nation in the areas of information technology, operations research, and supply chain management. CIPS leverages MIT's strengths, by unifying the photonics researchers in these departments and laboratories to focus on technology developments in photonics. The combined volume of research funds in the photonics area at MIT exceeds $20 million dollars annually. The faculty and staff at MIT in photonics related areas have included Claude Shannon (founder of information theory), Charles Townes (inventor of the laser), Robert Rediker (inventor of the semiconductor lasers), and Hermann Haus (inventor of the single frequency semiconductor laser & ultrafast optical switch). CIPS affiliated faculty and staff continue this tradition of excellence in areas ranging from optical network architectures to novel optical devices to novel photonic materials.

3. To integrate member companies into the MIT photonics community.

CIPS will host annual meetings and seminars in photonics. For CIPS member companies, focused visits to the Institute for individual companies will be organized with faculty and graduate students. In addition, CIPS will hold forums geared towards the creation of campus-industry teams to pursue large-scale research programs. CIPS will host poster sessions at the annual meeting so as to introduce graduate students and their research to industry. CIPS publications will include a resume book of recent graduate students in the area of photonics. Graduates of the Massachusetts Institute of Technology have founded 4,000 firms which, in 1994 alone, employed at least 1.1 million people and generated $232 billion of world sales. Photonics related companies founded by alumni include Sycamore Networks, Analog Devices, Texas Instruments, Hewlett-Packard, and 3Com as well as recent start-up such as OmniGuide.

Member companies have the opportunity to guide the research of CIPS faculty and students through the Working Groups (WGs) and individual graduate student awards.

Section 7

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A. Rosenthal, A. Macdonald and J. Voldman, "Cell patterning for modulating the stem cell microenvironment," presented at the *Biomedical Engineering Society Annual Meeting*, Oct. 2006.

J.R. Kovac, and J. Voldman, "Intuitive, visual, complex phenotype cell sorting using opto-flucs (Opto-Fluidic Cell Sorting)," presented at the *Biomedical Engineering Society Annual Meeting*, Oct. 2006.

J. Voldman, "Electrical forces for microscale cell manipulation," *Annual Review of Biomedical Engineering*, vol. 8, pp. 425-454, Aug. 2006.

A. Rosenthal, A. Macdonald and J. Voldman, "Cell patterning for modulating stem cell diffusible signaling. presented at the *4th International Society of Stem Cell Research Annual Meeting*, June 2006.

L.Y. Kim and J. Voldman, "Microfluidic perfusion culture of mouse embryonic stem cells," presented at the *4th International Society of Stem Cell Research Annual Meeting*, June 2006.

A. Rosenthal, B.M. Taff, and J. Voldman, "Quantitative modeling of dielectrophoretic traps," *Lab on a Chip*, vol. 6, no. 4, pp. 508-515, Apr. 2006.

L. Kim, M.D. Vahey, H.Y. Lee, and J. Voldman, "Microfluidic arrays for logarithmically perfused embryonic stem cell culture," *Lab on a Chip*, vol. 6, no. 3, pp. 394-406, Mar. 2006.

L.Y. Kim, H.-Y. Lee and J. Voldman, "Logarithmically perfused embryonic stem cell culture on chip," in *Micro Total Analysis Systems '05*, Boston, MA, Oct. 2005, pp. 530-532.

B.M. Taff and J. Voldman, "A scalable row/column-addressable dielectrophoretic cell-trapping array," in *Micro Total Analysis Systems '05*, Boston, MA, Oct. 2005, pp. 865-867.

A.D. Rosenthal and J. Voldman, "Dielectrophoretic traps for single-particle patterning," *Biophysical Journal*, vol. 88, no. 3, pp. 2193-2205, Mar. 2005.

A.D. Rosenthal and J. Voldman, "Simple, strong, and size-selective dielectrophoretic trap for single-cell patterning," in *Micro Total Analysis Systems '04*, Malmo, Sweden, Sep. 2004, pp. 228-230.

D.S. Gray, J.L. Tan, J. Voldman, and C.S. Chen, "Dielectrophoretic registration of living cells to a microelectrode array," *Biosensors and Bioelectronics*, vol. 19, no. 12, pp. 1765-1774, July 2004.

J. Voldman, "BioMEMS - building with cells," *Nature Materials*, vol. 2, no. 7, pp. 433-434, July 2003.

J. Voldman, M. Toner, M.L. Gray, and M.A. Schmidt, "A microfabrication-based dynamic array cytometer," *Analytical Chemistry*, vol. 74, no. 16, pp. 3984-3990, Aug. 2002.

J. Voldman, R.A. Braff, M. Toner, M.L. Gray, and M.A. Schmidt, "Holding forces of single-particle dielectrophoretic traps," *Biophysical Journal*, vol. 80, no. 1, pp. 531-541, Jan. 2001.

Brian L. Wardle
Boeing Assistant Professor
Department of Aeronautics and Astronautics

COLLABORATORS

K.F. Jensen, MIT
S. Kessler, Metis Design Corp.
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H. Tuller, MIT
N. Wicks, MIT
C.-Y. Wu, China Steel

GRADUATE STUDENTS

P. Capozzoli, Res. Asst., AA/Sloan
J. Chambers, Res. Asst., AA
N. duToit, Res. Asst., AA
E. Garcia, La Caixa Fellow, AA
A. Mracek, Res. Asst., AA
D. Quinn, NSF Fellow, ME
N. Yamamoto, Res. Asst., AA

UNDERGRADUATE STUDENTS

L. Megalini, Politecnico di Torino (visiting)
D. S. Saito, ITA (visiting)
K. Sorensen, AA
S. Wicks, AA

SUPPORT STAFF

J. Kane, Research Specialist
P. Lee, Financial Officer
M. Prendergast, Admin. Assist. II

PUBLICATIONS

E.J. Garcia, J. Hart, B.L. Wardle, and A. Slocum, "Fabrication of composite microstructures by capillarity-driven wetting of aligned carbon nanotubes with polymers," *Nanotechnology*, vol. 18, no. 16, pp. 165602:1-11, Apr. 2007.

E.J. Garcia, J. Hart, B.L. Wardle, and A. Slocum, "Fabrication and nanocompression testing of aligned carbon-nanotube-polymer nanocomposites," *Advanced Materials*, 2007, to be published.

N.E. duToit and B.L. Wardle, "Performance of microfabricated piezoelectric vibration energy harvesters," *Integrated Ferroelectrics*, vol. 83, pp. 13-23, 2006.

E.J. Garcia, J. Hart, B.L. Wardle, and A. Slocum, "Composite materials reinforced with long CNTS grown on the surface of fibers," presented at the *47th AIAA Structures, Dynamics, and Materials Conference,* Newport, RI, May 1-4, 2006.

N.E. duToit and B.L. Wardle, "Experimental verification of models for microfabricated piezoelectric vibration energy harvesters," presented at the *AIAA-2006-1792, 47th AIAA Structures, Dynamics, and Materials Conference*, 2006.

S.S. Kessler, K.S. Amaratunga, J.T. Chambers, and B.L. Wardle, "Durability assessment of lamb wave-based structural health monitoring nodes," presented at the *AIAA-2006-2263, 47th AIAA Structures, Dynamics, and Materials Conference*, 2006.

B.L. Wardle, "The incorrect benchmark shell buckling solution," presented at the *AIAA-2006-2028, 47th AIAA Structures, Dynamics, and Materials Conference*, 2006.

S.S. Kessler, K. Amaratunga and B.L. Wardle, "An assessment of durability requirements for aircraft structural health monitoring sensors," in *Proc. 5th International Workshop on SHM – 2005*, DesTech Publications, Sep. 2005.

N.E. duToit, B.L. Wardle, and S.-G. Kim, "Design considerations for MEMS-scale piezoelectric vibration energy harvesters," *Integrated Ferroelectric,* vol. 71, pp. 121-160, 2005.

E.J. Garcia, J. Hart,, B.L Wardle, and A. Slocum, "Composite materials reinforced with long CNTS grown on the surface of fibers," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 1854.

N.E. duToit and B. L. Wardle, "Experimental verification of models for microfabricated piezoelectric vibration energy harvesters," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 1792.

J.T. Chambers, B.L. Wardle, and S.S. Kessler, "Durability assessment of Lamb wave-based structural health monitoring nodes," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 2263.

B.L. Wardle, "The incorrect benchmark shell buckling solution," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 2028.

S.S. Kessler, K. Amaratunga, and B.L. Wardle, "An assessment of durability requirements for aircraft structural health monitoring sensors," in *Proc. 5th International Worshop on Structural Health Monitoring*, Stanford, CA, Sept. 2005, p. 9.

N. Yamamoto, N. Wicks, and B.L. Wardle, "Wrapping and through-thickness poisson effects on composite plates and shell contact laws," presented at the *46th AIAA Structures, Dynamics, and Materials Conference*, 2005.

N. Wicks, B.L. Wardle, and D. Pafitis, "Horizontal cylinder-in-cylinder buckling under compression and torsion: review and considerations for oil drilling applications," presented at the *15th International Conference on Composite Materials (ICCM)*, 2005.

D. Quinn, S.M. Spearing, and B. L. Wardle, "Residual stress and microstructural evolution in thin film materials for a micro solid oxide fuel cell (SOFC)," presented at the *Materials Research Society (MRS) Annual Fall Conference,* 2004.

Section 8
THESES AWARDED

Bachelor of Science
S.B.

2007

Roan, T. (M.L. Culpepper), "Design and Control of a Six–axis Nanopositioner for NanoEDM," June 2007.

Segado, M. (M.L. Culpepper), "Investigation of Flexural Contact Bearings on the Repeatability and Stiffness of Passive Kinematic Couplings," June 2007.

Moskwa, M. (J.A. Paradiso), "A Base Station for Data Collection for Sensor-Equipped Active RFID Tags," April 2007.

2006

Lewis, C. (J.A. Paradiso), "Prototyping and Expanding a Tool Set for a Ubiquitous Sensor Infrastructure," December 2006.

Farm, C. (S.G. Kim), "Electro-mechanical Modeling of Energy Harvesting System," June 2006.

Kim, J.S.C. (C.V. Thompson), "The Role of Hydrogen in the Growth of Carbon Nanotubes: A Study of the Catalyst State and Morphology," May 2006.

Above: Joyce Wu, PhD '07, Prof. Jesus A. del Alamo.

THESES AWARDED

Master of Engineering
M.Eng.

2007

Hopkins, J. (M.L. Culpepper), "A Generalized Approach to Constraint–Based Design of Multi–Axis Flexure Systems," June 2007.

Shamir, O. (L.A. Kolodziejski), "The Development of Ultra Broad Band Modulators," June 2007.

Dibiaso, C. (M.L. Culpepper), "Design of a Carbon Nanotube–Based Four Bar Compliant Mechanism," February 2007.

Malinowski, M. (J.A. Paradiso), "Micropower Active Tags for Shipment Monitoring and Identification," February 2007.

Puchala, K.A. (J. Voldman), "Selective Microorganism Concentration using a Dielectrophoresis-Based Microfabricated Device," February 2007.

Qazi, M. (A.P. Chandrakasan), "A 4kb Memory Array for MRAM Development," February 2007.

Pilawa, R. (D.J. Perreault), "Investigation of a Very High Frequency dc-dc Power Converter," January 2007.

2006

Gikandi, S. (J.A. del Alamo), "ELVIS iLab: A Flexible Platform for Online Laboratory Experiments in Electrical Engineering," September 2006.

Kovac, J.R. (J. Voldman), "An Opto-Fluidic Architecture for Image-Based Sorting of Biological Cells and Particles," September 2006.

Smalley, D. (V.M. Bove, Jr.), "Integrated-Optic Holovideo," September 2006.

Ali, H.P.A. (C.V. Thompson), "Carbon Nanotube Interconnects for IC Chips," August 2006.

Guo, Q. (C.V. Thompson), "Evaluation of Thin-Film Phase Change Material-Based Technologies," August 2006.

Kim, D.S. (J.A. Paradiso), "Sensor Network Localization Based on Natural Phenomena," August 2006.

Zou, T. (C.V. Thompson), "Evaluation of Potential Applications for Templated Arrays of Heterostructural Semiconductor Nanowires as Light Emitting Devices," August 2006.

Zhang, J. (D.J. Perreault), "Spread Spectrum Modulation System for Burst Mode DC-DC Converters," June 2006.

THESES AWARDED

Master of Science
S.M.

2007

Truque, D. (D.S. Boning), "Modeling of Planarization Technologies," May 2007.

Grine, A. (L.A. Kolodziejski), "The Design and Fabrication of an Electrically Activated Photonic Crystal Microcavity Laser," June 2007.

Davis, M. (D.S. Boning), "Application of Commercial Best Practices for New Technology Development within the Constraints of Defense Contract Funded R&D," May 2007.

Gan, J. (D.S. Boning), "Decision Support Systems for Tool Reuse and EOL Processes," May 2007.

Hwang, I. (D.S. Boning), "Optimizing Inventory Levels using Financial, Lifecycle, and Forecast Variance Data," May 2007.

Subramanian, N. (D.S. Boning), "Lean Manufacturing in a Semiconductor Environment: Production Leveling," May 2007.

Fucetola, C. (H.I. Smith), "Resolution Limits and Process Latitude of Conformable Contact Nano-Lithography," February 2007.

Joh, J. (J.A. del Alamo), "Degradation Mechanisms of GaN High Electron Mobility Transistors," February 2007.

Sagneri, A. (D.J. Perreault), "Design of a Very High Frequency dc-dc Boost Converter," January 2007.

THESES AWARDED

Master of Science
S.M.

2006

Aylward, R.P. (J.A. Paradiso), "Sensemble: A Wireless Inertial Sensor System for Interactive Dance and Collective Motion Analysis," September 2006.

Barroeta Pèrez, G. (J.A. Paradiso), "S.N.A.K.E.: A Dynamically Reconfigurable Artificial Sensate Skin," September 2006.

Capozzoli, P. (B.L. Wardle), "Residual Stress and Electrochemical Properties of Proton-Conducting Materials for a MEMS Fuel Cell," August 2006.

Chambers, J. (B.L. Wardle), "Durability of Lamb-wave Structural Health Monitoring Sensors," August 2006.

Gomez, L. (J.L. Hoyt), "Electron Transport in Ultrathin-body Fully Depleted n-MOSFETs Fabricated on Strained Silicon Directly on Insulator with Body Thickness Rnaging from 2 to 25 nm," August 2006.

Nguyen, K.M. (C.G. Sodini), "A 77-GHz Power Amplifier in Silicon Germanium BiCMOS Technology," August 2006.

Tandon, N. (J. Voldman), "Biomimetic Electrical Stimulation for Cardiac Tissue Engineering," August 2006.

Yamamoto, N. (B.L. Wardle), "Thermomechanical Testing of Materials and Structures for a Microfabricated Fuel Cell," August 2006.

Bow, H. (J. Han), "Characterization of Nanofilter Arrays for Small Molecule Separation," June 2006.

Doddabasanagouda, S. (S.G. Kim), "Photothermal Nanotemplate via Directed Carbon Nanotube Assembly," June 2006.

Kwong, J. (A.P. Chandrakasan), "A Sub-threshold Cell Library and Methodology," June 2006.

Pierquet, B. (D.J. Perreault), "Inductance Cancellation Techniques with Applications to EMI Filters," June 2006.

Ramadass, Y. (A.P. Chandrakasan), "An Energy Optimal Power Supply for Digital Circuits," June 2006.

Sanchez, D. (K.K. Berggren), "Circuit-based Architectures for Evolvable Hardware," June 2006.

Sze, V. (A.P. Chandrakasan), "An Energy Efficient Sub-Threshold Baseband Processor Architecture For Pulsed Ultra-Wideband Communications," June 2006.

Tan, J.K. (C.G. Sodini), "An Adaptive Orthogonal Frequency Division Multiplexing Baseband Modem for Wideband Wireless Channels," June 2006.

Xia, R. (S.G. Kim), "Wireless Sensor Node with Piezoelectric Energy Harvester," June 2006.

Arfin, S. (R. Sarpeshkar), "A Miniature Implantable Wireless Neural Stimulation System," May 2006.

Balakrishnan, K. (D.S. Boning), "Analysis of Variation in On-Chip Waveguide Distribution Schemes and Optical Receiver Circuits," May 2006.

Lee, H. (J. Voldman), "Optimizing Mixer Geometries for Dielectrophoretic Micro-concentrators," May 2006.

Vasovski, S. (D.S. Boning), "A Global Sourcing Strategy for Durable Tooling," May 2006.

THESES AWARDED

Doctor of Philosophy
Ph.D.

2007

Bryant, R. (L.A. Kolodziejski), "Planar Nanoelectromechanical High-Index-Contrast Photonic Structures," June 2007.

Kern, A.M. (A.P. Chandrakasan), "CMOS Circuits for VCSEL-Based Optical IO," June 2007.

Lee, F.S. (A.P. Chandrakasan), "Energy Efficient Ultra-Wideband Radio Transceiver Architectures and Receiver Circuits," June 2007.

Lifton, J.H. (J.A. Paradiso), "A Sensor Network for Ubiquitous Computing and Example Applications to Virtual Worlds," June 2007.

Rosenthal, A. (J. Voldman), "Cell Patterning Technology for Controlling the Stem Cell Microenvironment," June 2007.

Seneviratne, D. (H.L. Tuller), "Materials and Devices for Optical Switching and Modulation of Photonic Integrated Circuits," June 2007.

Yu, A.A. (F.R. Stellacci), "Supramolecular NanoStamping (SuNS) – Fabricating Nano/Bio Devices using DNA as Movable Type," June 2007.

Cai, H. (D.S. Boning), "Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization," May 2007.

Chen, L. (A.I. Akinwande), "Double-gated Isolated Vertically Aligned Carbon Nanofiber Field Emission and Field Ionization Arrays," May 2007.

Gassend, B. (A.I. Akinwande, M. Martinez-Sanchez), "A Fully Microfabricated Two-Dimensional

Electrospray Array with Applications to Space Propulsion," May 2007.

Gettings, K. (D.S. Boning), "Impact of Variation in Advanced Integrated Circuits," May 2007.

Liptay, T. (R.J. Ram), "Spectral Properties of Semiconductor Nanocrystals and their Properties," May 2007.

Mayer, P. (R.J. Ram), "High-Density Thermal Generation and Nanoscale Thermal Metrology," May 2007.

Somani, A. (D.S. Boning), "Environmentally Benign Manufacturing of Three Dimensional Integrated Circuits (3D ICs)," May 2007.

Xie, X. (D.S. Boning), "Physical Understanding and Modeling of Chemical Mechanical Planarization in Dielectric Materials," May 2007.

Fiorenza, J. (H.-S. Lee), "A Comparator-Based Switched-Capacitor Pipelined Analog-to-Digital Converter," March 2007.

Fu, J. (J. Han), "Microfabricated Nanofilter Array Based Devices for Advanced Biomolecule Separation," March 2007.

Wang, Y.C. (J. Han), "Electrokinetic Trapping of Biomolecules: Novel Nanofluidic Devices for Proteomic Applications," March 2007.

Barsotti, Jr., R.J. (F.R. Stellacci), "Nanomanufacturing for Biological Sensing Applications," February 2007.

Benbasat, A.Y. (J.A. Paradiso), "An Automated Framework for Power-Efficient Detection in Embedded Sensor Systems," February 2007.

Fiorenza, J.K. (C.G. Sodini), "A Comparator-Based Switched-Capacitor Pipelined Analog-to-Digital Converter," February 2007.

THESES AWARDED

Doctor of Philosophy
Ph.D.

2006

Olubuyide, O. (J.L. Hoyt), "Low Pressure Epitaxial Growth, Fabrication and Characterization of Ge-on-Si Photodiodes," December 2006.

Khuon, L. (C.G. Sodini), "Parallel Integrated Receivers for Multiple Antenna Wireless LAN Systems," October 2006.

Tadepalli, R. (C.V. Thompson), "Characterization and Requirements for Cu-Cu Bonds for Three-Dimensional Integrated Circuits," October 2006.

Wu, J. (J.A. del Alamo), "Through-Substrate Interconnects for 3-D Integration and RF Systems," October 2006.

Barkley, E.R. (C.G Fonstad, Jr.), "The Integration of InP/InGaAsP Ridge Waveguide Structures with Dielectric Waveguides on Silicon," September 2006.

Hertz, J. (H.L. Tuller), "Microfabrication Methods to Improve the Kinetics of the Yttria Stabilized Zirconia-Platinum-Oxygen Electrode," September 2006.

Jerng, A. (C.G. Sodini), "Delta-Sigma Digital-RF Modulation for High Data Rate Transmitters," September 2006.

Rivas, J. (D.J. Perreault), "Radio Frequency dc-dc Power Conversion," September 2006.

Sepke, T. (H.-S. Lee, C.G. Sodini), "Comparator Design and Analysis for Comparator-based Switched-capacitor Circuits," September 2006.

Haghgooie, R. (P.S. Doyle), "Structure and Dynamics of MR Fluids Confined in Microfluidic Devices," August 2006.

Nielsen, O.M. (M.A. Schmidt, K.F. Jensen), "A Thermally Efficient Microreactor for Thermophotovoltaic Generation," August 2006.

Salthouse, C. (R. Sarpeshkar), "Analog Adaptive Nonlinear Filtering and Spectral Analysis for Low-Power Audio Applications," August 2006.

Savin, T. (P.S. Doyle), "Multiple Particle Tracking to Assess the Structure of Biological Fluids," August 2006.

Underhill, P.T. (P.S. Doyle), "Systematic Development of Coarse-grained Polymer Models," August 2006.

Aberg, I. (J.L. Hoyt), "Transport in Thin-Body MOSFETs Fabricated in Strained Si and Strained Si/SiGe Heterostructures on Insulator," June 2006.

Bullard, J.W. (M.J. Cima), "Anisotropic and Tunable Characteristics of the Colloidal Behavior of Metal Oxide Surfaces," June 2006.

Dames, C. (G. Chen), "Thermal Properties of Nanowires and Nanotubes: Modeling and Experiments," June 2006.

Honore, F. (A.P. Chandrakasan), "Energy-Aware Architectures, Circuits and CAD for Field Programmable Gate Arrays," June 2006.

Khan, S.A. (K.F. Jensen, M.A. Schmidt), "Microfluidic Synthesis of Colloidal Nanomaterials," June 2006.

Murphy, E.R. (K.F. Jensen, M.A. Schmidt), "Microchemical Systems for Rapid Optimization of Organic Syntheses," June 2006.

Zhang, Z. (K.F. Jensen), "Microfabricated Reactor for Bioprocesses Development," June 2006.

Blasquez, R. (A.P. Chandrakasan), "Ultra-wideband Digital Baseband," May 2006.

Fan, A. (A.I. Akinwande, L.R. Reif), "Three Dimensional Integration Technology Using Copper Bonding," May 2006.

Xia, G. (J.L. Hoyt), "Silicon-Germanium Interdiffusion and Its Impacts on Enhanced Mobility MOSFETs," April 2006.

Section 9

VLSI MEMO SERIES

MTL maintains a comprehensive Memo Series covering the activities of MTL and related microsystems research at MIT. A chronological list of memos issued from 2007 appears below Copies of MTL Memos are available online exclusively to members of the Microsystems Industrial Group (MIG) at MTL. MIG members are invited to sign up for an account that will grant them access to these materials in a password-protected directory. Visit our website at **http://mtlweb.mit.edu** for more information and current memos.

07-1193 **Through-Substrate Interconnects for 3-D Integration and RF Systems**
J.H. Wu

07-1194 **Low Pressure Epitaxial Growth, Fabrication and Characterization of Ge-on-Si Photodiodes**
O.O. Olubuyide

07-1195 **Energy Efficient Ultra-Wideband Radio Transceiver Architectures and Receiver Circuits**
F.S. Lee

07-1196 **Cell Patterning Technology for Controlling the Stem Cell Microenvironment**
A. Rosenthal

07-1197 **Three Dimensional Integration Technology Using Copper Wafer Bonding**
A. Fan

07-1198 **Degradation Mechanisms of GaN High Electron Mobility Transistors**
J. Joh

07-1199 **Photophysics of Carbon Nanotubes**
G. Samsonidze

07-2000 **Comparator Design and Analysis for Comparator-Based Switched-Capacitor Circuits**
T. Sepke

07-2001 **Micromechanical Control of cell–cell interactions**
E.E. Hui, S.N. Bhatia

07-2002 **A Comparator-Based Switched-Capacitor Pipelined Analog-to-Digital Converter**
J.K. Fiorenza

07-2003 **A Microfabricated Electrospray Thruster using Ridge Emitters and Ceramic-Ball Extractor Location**
B. Gassend, L.F. Velasquez-Garcia, P.C. Lozano, A.I. Akinwande

07-2004 **Mechanical Assembly of Electrospray Thruster Grid**
B. Gassend, L.F. Velasquez-Garcia, A.I. Akinwande, M. Martinez-Sanchez

07-2005 **Thermomechanical Properties and Performance of Microfabricated Solid Oxide Fuel Cell (μSOFC)**
N. Yamamoto

07-2006 **Optimizing Wettability of Externally Wetted Microfabricated Silicon Electrospray Thrusters**
T. Cruz Garza

07-2007 **A Fully Microfabricated Two-Dimensional Electrospray Array with Applications to Space Propulsion**
B. Gassend

07-2008 **Micromachined Printheads for the Direct Evaporative Patterning of Organic Materials**
V. Leblanc

07-2009 **Study of CMOS Process Variation by Multiplexing Analog Characteristics**
K.M. Gonzalez-Valentin Gettings

07-2010 **Design, Fabrication, and Characterization of Germanium MOSFETs with High-k Gate Dielectric Stacks based on Nitride Interfacial Layers**
A.P. Ritenour

07-2011 **Enhanced Next Generation Alternator**
L.M. Lorilla

07-2012 **Advanced Filters and Components for Power Applications**
T.C. Neugebauer

07-2013 **Multi-resonant Passive Components for Power Conversion**
J.W. Phinney

07-2014 **Radio Frequency dc-dc Power Conversion**
J. Rivas

Section 10

MTL SEMINAR SERIES

MTL hosts a series of talks each semester known as the MTL Seminar Series. Speakers for the Series are selected on the basis of their knowledge and competence in the areas of microelectronics research, manufacturing, or policy. The MTL Seminar Series is held on the MIT Campus on Tuesdays at 4:00 pm, and is open to the public. A listing of recent seminars is also provided at **http://mtlweb.mit.edu.** Streaming videos of the MTL Seminar Series are available online exclusively to individuals whose companies are members of the Microsystems Industrial Group (MIG) at MTL. For information regarding the MTL Seminar Series, send e-mail to rmaynard@mtl.mit.edu.

fall 2006

September 12, 2006
The Past, Present, and Future of Data Converters and Mixed Signals: A Universal Model
David Robertson, Analog Devices

September 26, 2006
Wafer Cleaning in Semiconductor Manufacturing: The Single-Wafer Inflection Point
John TC Lee, Applied Materials

November 14, 2006
"Brain Repair 101" for Electrical Engineers
Timothy Denison, Medtronic Neurological Technologies

December 5, 2006
Overview of Communication Technology Research at IBM
Mehmet Soyuer, IBM

December 12, 2006
Extended Drain CMOS Devices in Sub-100nm Processes Enabling High-performance Mixed-signal and Direct Battery Connection Analog Blocks
Baher Haroun, Texas Instruments

Spring 2007

February 27, 2007
An Introduction to Ultra-High Speed Data Conversion
Gabriele Manganaro, National Semiconductor

March 6, 2007
High Mobility III-V MOSFET Technology
Matthias Passlack, Freescale Semiconductor

March 13, 2007
Why Are We So Interested in Carbon Nanotubes?
Mildred Dresselhaus, MIT

April 3, 2007
Unconventional Nanofabrication: Nanosciving, Crack Replication, and Related Techniques
George Whitesides, Harvard University

April 10, 2007
Trends and Requirements of Future CMOS FETs Based on a Simple Physical Device Model
Dimitri Antoniadis, MIT

April 24, 2007
Nanoscale CMOS Transistor Scaling Challenges and Strategy for High-Performance Low-Power Logic Technology
Tahir Ghani, Intel

May 1, 2007
MEMS at the Knee of the Curve
Roger Howe, Stanford University

May 15, 2007
MTL Doctoral Dissertation Seminar
Lane Brooks, MIT

Section 11

ABBREVIATIONS

Massachusetts Institute of Technology

ACC .....Advanced Concepts Committee (MIT LL)
CAES .....Center for Advanced Engineering Study
ChE.....Department of Chemical Engineering
ChemE .....Department of Chemical Engineering
CICS .....Center for Integrated Circuits and Systems
CIPS.....Center for Integrated Photonic Systems
CMI .....Cambridge-MIT Institute
CMSE.....Center for Materials Science and Engineering
CSR .....Center for Space Research
DMA.....Dupont-MIT Alliance
DMSE.....Department of Materials Science and Engineering
EECS .....Department of Electrical Engineering and Computer Science
HST .....Health Sciences and Technology, Harvard-MIT
ICL.....Integrated Circuits Laboratory
ISN.....Institute for Soldier Nanotechnologies
ITRC.....Intelligent Transportation Research Center
LEES.....Laboratory for Electromagnetic and Electronic Systems
LFM.....Leaders for Manufacturing
MIG.....Microsystems Industrial Group
MIT .....Massachusetts Institute of Technology
MNSL.....Micro & Nano Systems Laboratory
MPC.....Materials Processing Center
MTL .....Microsystems Technology Laboratories
NSL .....NanoStructures Laboratory
RLE.....Research Laboratory of Electronics
SMA.....Singapore-MIT Alliance
SML .....Space Microstructures Laboratory
SOE .....School of Engineering
TRL.....Technology Research Laboratory
UROP .....Undergraduate Research Opportunities Program

Private Industry

AMD.....Advanced Micro Devices
CSDL .....Charles Stark Draper Laboratory
HP .....Hewlett-Packard
IBM .....International Business Machines Corporation
KIMM.....Korea Institute of Machinery and Materials

MGH.....Massachusetts General Hospital
NTT.....Nippon Telephone and Telegraph
SIA.....Semiconductor Industry Association
SRC .....Semiconductor Research Corporation
SRC/FCRP .....Semiconductor Research Corporation Focused Center Research Program
- C2S2.....Center for Circuits and Systems Solutions
- GSRC .....Gigascale Systems Research Center
- IFC .....Interconnect Focus Center
- MSD.....Center for Materials, Structures and Devices

TI.....Texas Instruments

Government

AFOSR.....U.S. Air Force Office of Scientific Research
AFRL .....Air Force Research Laboratories
ARDA .....Advanced Research and Development Activity
ARL.....Army Research Labotratories
ARO MURI.....Army Research Office M
CSE .....Consortium on Superconducting Electronic
DARPA.....Defense Advanced Research Projects Agency
DOD.....Department of Defense
DOE .....Department of Energy
DURINT .....Defense University Initiative on Nanotechnology
JPL .....Jet Propulsion Laboratories
JSEP .....Joint Services Electronics Program
LANL.....Los Alamos National Laboratory
MDA.....Missile Defense Agency
MRSEC.....Materials Research Science and Engineering Center
MURI .....Multi University Research Initiative
NASA .....National Aeronautics and Space Administration
NCIPT.....National Center for Integrated Photonics Technology
NDSEG.....National Defense Science and Engineering Graduate Fellowship
NIH .....National Institutes of Health
- NCI.....National Cancer Institute
- NCRR .....National Center for Research Resources
- NIDDK .....National Institute of Diabetes and Digestive and Kidney Diseases
- NIBIB .....National Institute of Biomedical Imaging and BioEngineering
- NHLBI.....National Heart, Lung, and Blood Institute

NIST.....National Institute of Standards and Technology
NOAA .....National Atmospheric and Oceanographic Administration
NREL.....National Renewable Energy Laboratory
NRL.....Naval Research Laboratory
NSA .....National Security Administration
NSF.....National Science Foundation
- CMSE .....Center for Materials Science and Engineering
- MRSEC .....Materials Research Science and Engineering Centers
- NIRT .....Nanotechnology and Interdisciplinary Research Initiative
- SGER.....Small Grant for Exploratory Research

ONR .....Office of Naval Research

Other

CFI.....CAD Framework Initiative
CIE.....Commission International de l'Eclairage
CIM.....Computer Integrated Manufacturing
IEEE.....Institute of Electrical and Electronics Engineers
IEDM.....International Electronic Devices Meeting
IME.....Institute of Microelectronics, Singapore
IMEC.....Interuniversity MicroElectronics Center
MCNC.....Microelectronics Center of North Carolina
MRS.....Materials Research Society
NATO.....North Atlantic Treaty Organization
NTCIP.....National Transportation Communications for Intelligent Transportation
WiMAX.....Worldwide Interoperability for Microwave Access, Inc.

Technical

AAO.....Anodic aluminum oxide
ACEO.....AC electro-osmosis
ACPR.....Adjacent channe power ratio
ADC.....Analog-to-digital converter
AFM.....Atomic force microscope
ALD.....Atomic layer deposition
AMOL.....Absorbance-two-wavelength scheme
APCVD.....Atmospheric pressure chemical vapor deposition
ASIC.....Application-specific integrated circuit
BEOL.....Back-end-of-line
BER.....Bit-error-rate
BiCMOS.....Bipolar complementary metal oxide semiconductor
BPSK.....Binary phase shift keying
BPV.....Back-propagation of variance
BTBT.....Band-to-band tunneling
CAD.....Computer aided design
CATV.....Category V
CBSC.....Comparator-based switched-capacitor circuit
CCD.....Charge couple device
CCR.....Critically coupled resonator
CDR.....Clock and data recovery
CFB.....Cartesian feedback
CFT.....Clock feed-through
CML.....Current mode latch
CMOS.....Complementary metal oxide semiconductor
CMP.....Chemical mechanical planarizetion
CNT.....Carbon nanotube
COC.....Cyclic olefin copolymer
COIL.....Chemical oxygen iodine laser
CV.....Capacitance voltage
CVD.....Chemical vapor deposition
DAC.....Digital-to-analog converter
DBR.....Dielectric Bragg reflector
DCA.....Dielectric continuum approximation
DCP.....Dielectrophoretic cell patterning
D-CAP.....Digitally-configurable analog processor
DEM.....Dynamic element matching
DEP.....Dielectrophoresis
DHI.....Digital holographic imaging
DIBL.....Drain-induced barrier lowering
DPD.....Digital predistortion
DRIE.....Deep reactive-ion etching
DSP.....Digital signal processing
DUT.....Devices-under-test
ECG.....Electrocardiogram
EEG.....Electroencephalogram
EEPROM.....Electrically erasable programmable read only memory
EL.....Electroluminescence
EM.....Electromagnetic
ENOB.....Effective number of bits
EPD.....Endpoint detection
FACS.....Flow-assisted Cell Sorting
FDTD.....Finite difference time domain
FEOL.....Front-end-of-line
FET.....Field-effect transistor
FFT.....Fast Fourier transform
FIR.....Finite impulse response
FOM.....Figure of merit
FOV.....Field of view
FPGA.....Field programmable gate array
GeOI.....Germanium-on-insulator
GMR.....Giant magnetoresistance
GOI.....Germanium-on-insulator
GP.....Geometric programming
HD.....Harmonic distortion
HDQ.....Harmonic Differential Quadrature
HEMT.....High-electron mobility
HIC.....High-index-contrast
HM.....Herringbone mixer
HOI.....Heterostructure on insulator
HSQ.....Hydrogen silsesquioxane
ICEO.....Induced charge electro-osmosis
IDE.....Interdigitated electrodes
IMD.....Inter-modulation distortion
INL.....Integral nonlinearity
ISI.....Inter symbol interference
ISM.....Industrial, scientific, medical
ITO.....Indium-tin-oxide
IV.....Current voltage
KOH.....Potassium hydroxide
LED.....Light-emitting device
LINC.....Laboratory instrument computer
LNA.....Low noise amplifier
LPCVD.....Low pressure chemical vapor deposition
LSB.....Lower sideband
MAA.....methacrylic acid
MDLL.....Multiplying delay-locked loops
MEM.....Micro-electro-mechanical
M-HEMT.....Metamorphic high-electron-mobility transistor
MEMS.....Micro-electro-mechanical systems
MGA.....Micro gas analyzer
MMA.....Methylmethacrylate
MMSE.....Minimum mean square error
MMW.....Millimeter-wave
MOCVD.....Metallorganic chemical vapor deposition
MOR.....Model-order-reduction
MOS.....Metal-oxide-semiconductor
MOSFET.....Metal-oxide-semiconductor field-effect transistor

MPIE .....Mixed-potential-integral-equation
MRAM .....Magnetic-random-access memory
NEM.....Nano-electro-mechanical
NIL.....Nanoimprint lithography
NMOS .....Negative-channel metal-oxide semicondutor
OEO .....Optical-electronic-optical
OFDM.....Orthogonal frequency division multiplexing
OFET.....Organic field-effect transistor
OFF .....Off
OHC .....Outer hair cells
OLED .....Organic light-emitting diode
OPL.....Optical projection lithography
PA.....Power amplifier
PAE .....Power-added efficiency
PCR .....Polymerase chain reaction
PDAC .....poly diallyldimethylammonium chloride
PDMS.....Polydimethylsiloxane
PECVD .....Plama enhanced chemical vapor deposition
PEM .....Proton exchange membrane; polymer electrolyte membrane
PFM .....Pulse frequency modulation
PHEMT .....Pseudomorphic high-electron mobility transistor
PHY.....Physical layer
PIV .....Particle image velocimetry
PL.....Photoluminescence
PLL .....Phase-locked loops
PMGI .....Polymethylglutarimide
PMMA.....Polymethylmethacrylate
PMOR.....Parameterized model reduction
PMOS.....Postive channel metal oxide semicondutor
PPM .....Pulse-position modulated
PRF .....Pulse-repetition frequency
PROM.....Parameterized reduced-order models
PSV.....Pseudo-spin-valve
PTM .....Predictive technology models
QCL .....Quantum-cascade laser
QD .....Quantum dot
RC .....Resonant cavity
RFID .....Radio frequency identification
RIE .....Reactive-ion etching
ROI.....Regions of interest
RSM .....Response surface model
RTNIL .....Room-temperature nanoimprint lithography
RVHI .....Rainbow volume holographic imaging
SAR.....Successive approximation register
SAW.....Surface acoustic wave
SBR .....Saturable Bragg reflector
SCE .....Short-channel Effects
SEBL.....Scanning-electron-beam lithography
SEM .....Scanning-electron microscope
SFDR.....Spur-free dynamic range
SGM.....slanted groove mixer
SHM.....Staggered herringbone mixer
SIMS .....Secondary ion-mass spectrometry
SiNW.....Silicon nano-wire
SiNWT .....Silicon nanowire transistors
SMR .....Suspended microchannel resonator
SMU.....Sense-Measurement Unit
SNR .....Signal-to-noise ratio
SOA .....Semiconductor optical amplifier
SoC .....System-on-chip
SOG .....Singlet oxygen generator
SOI.....Silicon on insulator
SOLES .....Silicon on lattice-engineered substrate
SPLEBL .....Spatial-phase-locked electron-beam lithography
SPM .....Scanning probe micrograph
SRAM .....Static random access memory
SSDSOI .....Strained-silicon directly on insulator
STI.....Shallow trench isolation
TAT .....Trap-assisted tunneling
TDC .....Time-to-digital
TDD .....Threading dislocation density
TERS.....Tip enhanced Raman spectroscopy
TIPS .....Thermal inkjet pico-fluidic drop dispensing system
TPV.....Thermophotovoltaic
TTTDD.....Time-temperature threading dislocation density
UHVCVD .....Ultra high vacuum chemical vapor deposition
ULSI.....Ultra Large Scale Integration
UWB.....Ultra-wideband
VCO .....Voltage Controlled Oscillators
VCSEL.....Vertical-cavity Surface-emitting Laser
VDG .....Voltage from Drain to Gate
VLS.....Vapor-liquid-solid
VLSI .....Very Large Scale Integration
VPR.....Versatile Place and Route
VSCEL.....Vertical cavity surface-emitting laser
WiGLAN.....Wireless gigabit local area network
WLAN.....Wireless local area network
WSP .....Water soluble particles
YSZ.....Yttria-stabalized zirconia oxide
ZPAL .....Zone-plate-array lithography

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