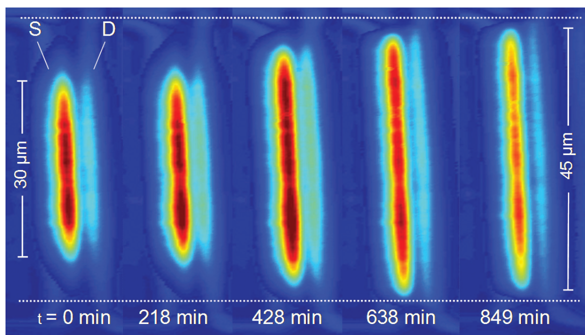
ELECTRONIC DEVICES & EMERGING TECHNOLOGIES



▲ Light-emission photographs from source and drain of PHEMT, at five points during step-stressing experiment. Taken at V_{GS}=0.3 V, V_{DS}=6.6 V. Gate width W_g = 50 µm (A.A. Villanueva, J.A. del Alamo, p. 72).

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Amorphous Zinc-Oxide-Based Thin-film Transistors

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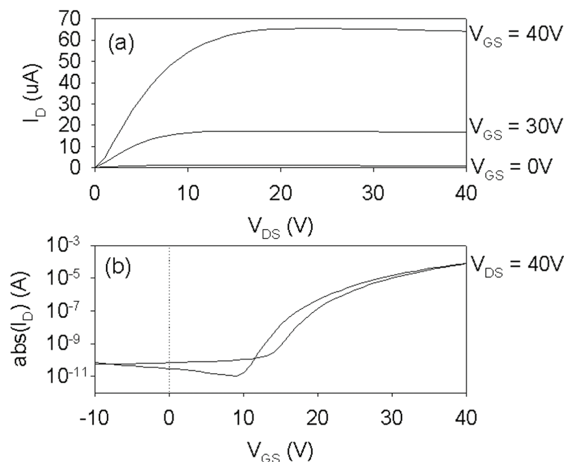
Sponsorship: Hewlett-Packard

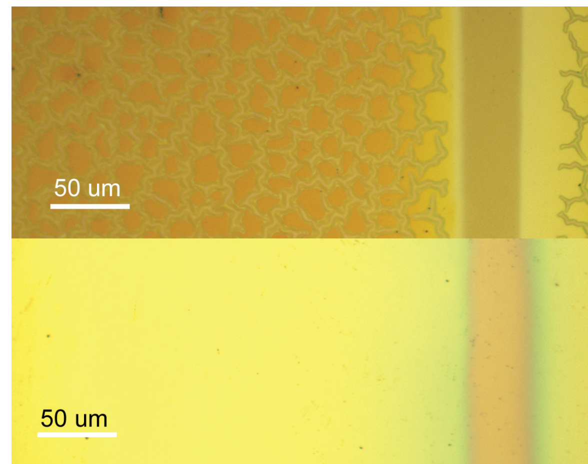
Recently, RF-sputtered zinc oxide-based field effect transisters (FETs) have been demonstrated with higher mobilities and performance than amorphous silicon, the dominant material used for display backplanes [1,2]. The low temperature processing possible for zinc oxide-based FETs [3] makes these materials compatible with flexible polymer substrates, but patterning with shadow masks limits feature size and accuracy. This project aims to develop a low-temperature, lithographic process for zinc oxide-based FETs, similar to one developed for organic FETs [4].

Our initial work focuses on two issues: determining optimal conditions for (1) growing the oxide semiconductor and (2) depositing high-quality oxide semiconductor and contact films on an organic polymer, parylene. For the former, top-contact, bottom gate ZnO FETs were fabricated on Si/SiO_2 substrates, using SiO_2 as the gate dielectric, Si as the gate, and sputtered indium-tin-oxide (ITO) as source/drain contacts. The RF sputtering power, total chamber pressure, and annealing temperatures were varied in a series of experiments; Figure 1 shows the current-voltage characteristics of a device from one set of conditions.

To determine optimal conditions for depositing high-quality films on an organic polymer, ITO films were deposited on an organic polymer dielectric, parylene, at different sputter rates. High stress in the oxide films on top of the soft organic polymer dielectric, parylene, may cause cracking and discontinuities in the film. Figure 2a shows a microscope photograph of the cracked surface of an ITO film sputtered at 80W on parylene; Figure 2b shows a continuous ITO film sputtered at 15W on parylene.



▲ Figure 1: Current-voltage output characteristics (top) and transfer characteristics (bottom) for ZnO field effect transistor sputtered at 375W in 5mTorr Ar ambient, after annealing at 300 degrees C. (W/L = 1250μm/50μm.)



▲ Figure 2: (a) Optical microscope image of cracked 1000Å ITO film on parylene sputtered at 80W. (b) Optical microscope image of smooth ITO film on parylene sputtered at 15W.

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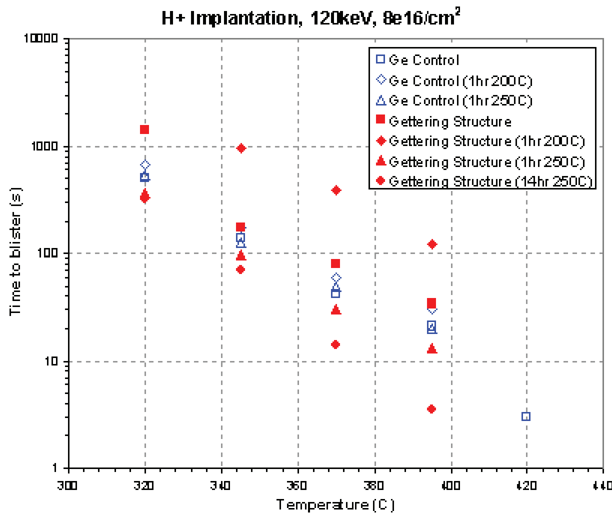
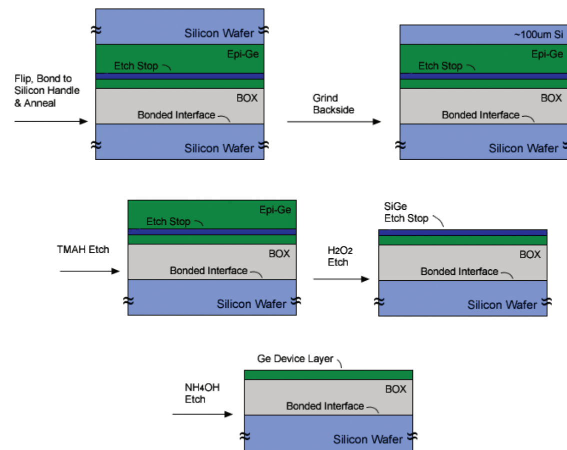
Fabrication of Germanium-on-Insulator by Means of Wafer Bonding and Layer Transfer

J. Hennessy, D.A. Antoniadis
Sponsorship: MARCO MSD

The fabrication of germanium-on-insulator (GeOI) substrates using a hydrogen-induced layer transfer technique and bulk Ge wafers is limited by the mismatch in the thermal coefficients of expansion between Ge and Si. A strained SiGe layer can be used as a hydrogen-gettering layer to attempt to lower the temperature at which the hydrogen-induced layer transfer can occur. Figure 1 illustrates the success of this gettering structure in reducing the time for surface blisters to appear in H+-implanted Ge. However, this technique does not reduce the overall temperature at which layer transfer occurs. A second technique for GeOI fabrication involves the direct epitaxial growth of Ge on a Si substrate. Using a process flow illustrated in Figure 2, a GeOI substrate is fabricated using a grind and etch-back technique. This technique eliminates the thermal mismatch between the bonded wafer pairs; by incorporating an epitaxial etch-stop layer in the transfer wafer, it may potentially allow for the fabrication of arbitrarily thin GeOI substrates.



▲ Figure 1: Blister point measurements for a strained SiGe gettering structure show a significant reduction in the time to blister for some pre-annealing conditions. No corresponding reduction in the layer-transfer temperature after wafer bonding was observed.

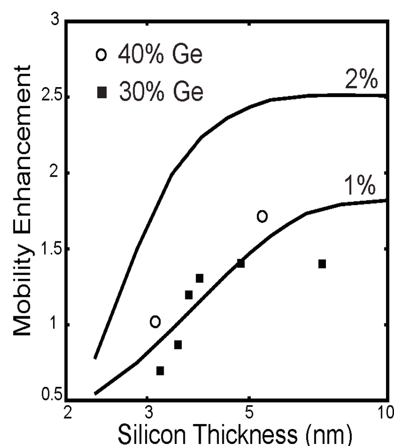


▲ Figure 2: Process flow for GeOI fabrication using epitaxially grown Ge directly on Si. A grind and etch-back technique is used instead of hydrogen-induced layer transfer.

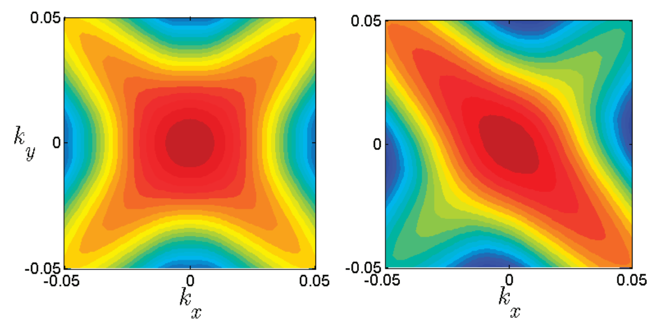
Strain Dependence of Mobility in Ultra-thin SOI and GOI

A. Khakifirooz, D.A. Antoniadis
Sponsorship: MARCO MSD

Significant enhancement of the carrier transport properties is required to continue the scaling of transistor performance. Different approaches to apply uniaxial or biaxial strain to the channel have been proposed to achieve higher mobility and drive current and some of them have been already implement in the state-of-the-art CMOS technology. Whether or not these approaches offer any benefit for ultra-thin semiconductor-on-insulator structures is a key concern. To understand how different parameters that determine the carrier mobility are affected in such atomically thin SOI and germanium-on-insulator (GOI) structures, we explore the effect of biaxial and uniaxial strain on the band structure using a $sp^3d^5s^*$ tight-binding model. As Figure 1 shows, biaxial tensile strain, which is traditionally used in bulk CMOS technology to improve both electron and hole mobility, does not provide any benefit for holes in ultra-thin SOI once the channel is thinner than 3-4 nm [1]. Biaxial tensile strain lifts the degeneracy of the light and heavy holes and preferentially populates the light holes. Carrier confinement imposed by the channel thickness or the gate voltage acts in the opposite directions, preferentially populating the heavy hole band. The net effect is that the biaxial tensile strain is less effective in enhancing the hole mobility in ultra-thin SOI compared to bulk silicon. This observation is in agreement with recent experimental results [2]. However, as illustrated in Figure 2, uniaxial compressive strain continues to provide mobility enhancement in ultra-thin SOI structures via manipulating the effective mass in the [110] channel direction. The fact that the ballistic injection velocity is also enhanced via effective mass reduction is also encouraging.



▲ Figure 1: Calculated mobility enhancement as a function of the silicon thickness for different levels of biaxial tensile strain. Measurement results [2] (symbols) are also shown for comparison. Various scattering mechanisms, including the additional confinement induced by the gate voltage, further reduce the available mobility enhancement. The results should be viewed as the upper limits of the mobility enhancement.



▲ Figure 2: Contours of constant energy vs. in plane wavenumbers for relaxed (left) and uniaxially strained (right) 2.85-nm-thick SOI structure. Uniaxial compressive strain reduces the effective mass in the [110] channel direction, thereby increasing the mobility and ballistic velocity. Uniaxial compressive stress of 1 GPa is applied in the [110] direction and the wavenumbers are in the units of $2\pi/a$, where a is the lattice constant.

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Towards MOS Memory Devices Containing 1 nm Silicon Nanoparticles

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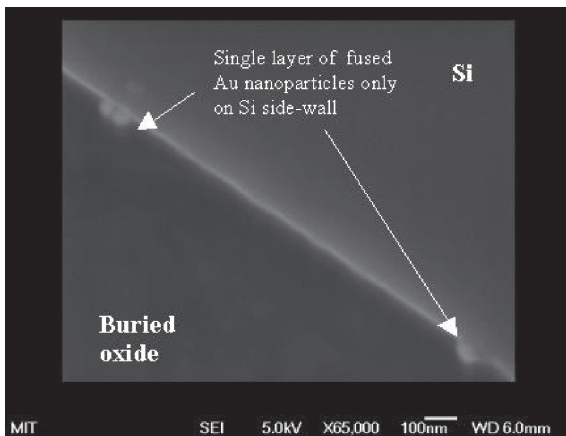
Sponsorship: MTL, University of Illinois at Urbana-Champaign

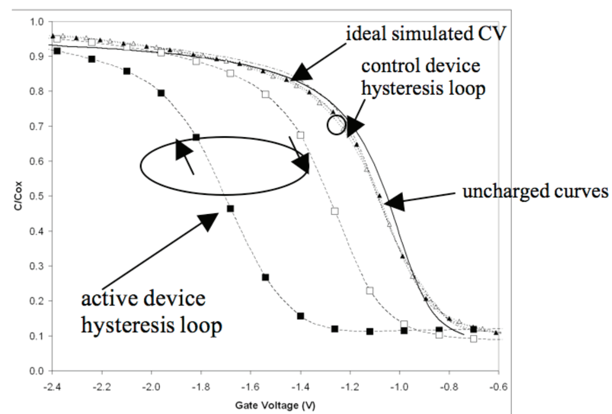
MOS devices containing *ex-situ* produced, identical (constant size), spherical, 1-nm Si nanoparticles were fabricated for use in future flash electrically erasable programmable read only memory (EEPROM) devices [1]. Device fabrication did not require changes to the standard CMOS process. The Si nanoparticles (Figure 1a), 1 nm in diameter and H-terminated, are prepared using electrochemical dispersion of device-quality Si wafers in a mixture of HF/H_2O_2 [2-3]. Figure 1b gives the schematic of the MOS capacitor device. We start with boron-doped substrates at a level of ~10^{15} cm^{-3}. Thin, SiO_2 tunnel-oxide (~ 4.2 nm), was then grown by dry oxidation. We then spread colloidal Si nanoparticles in isoproponol (IPA) on the oxide using spin-coating. We used AFM along with ellipsometry to test uniformity and to estimate the film thickness. We used several particle colloids with decreasing molar concentration that were prepared by successive dilutions to approach sub-monolayer coatings. After the particles were spin-coat, a ~ 10-nm SiO_2 cap layer was deposited by LPCVD at 400 C^o. Thin (~500 nm) Al films were then deposited. Capacitors were defined and chemically etched and Al contact on the wafer backside was deposited. A N_2/H_2 annealing at 450 C^0 for ten minutes completed the process. Control MOS capacitors containing no particles were also fabricated using the same procedure.

The CV measurements were performed on devices fabricated with varying Si nanoparticle density. The hysteresis loops and programming characteristics exhibit well-behaved characteristics, substantial voltage shift, and long charge retention. both the rise and shape and the absence of substructure in the CV agree with similarly constructed control samples and with an ideal simulated device that assumes no interface states (Figure 2). We have tested the charge retention characteristics of several devices. We first obtained an uncharged curve at the much reduced voltage range of 0 to -0.8 V, and we then programmed the device at +7 V for ~ 40 s. We analyzed the threshold voltage shift as a function of time while holding voltage at − 0.8 V. Based on the slope of the response, we extrapolate to a retention time of several years [1].

We believe we have successfully demonstrated the incorporation of identical spherical 1 nm silicon nanoparticles in MOS devices utilizing a simple CMOS compatible process. The process allows for device optimization by control of the density of nanoparticles, where high-density could potentially achieve voltage shift of several volts.



▲ Figure 1: (a) Prototype of a 1-nm particle ($Si_{29}H_{24}$) Si (gray), H (white) . (b) The schematic of the Si nanoparticle MOS device



▲ Figure 2: Hysteresis loops of control device (triangles), active device with density 4.8 x 10^{11} cm^{-2} (squares). The uncharged curves are shown as dotted and dash-dotted; the simulated CV curve issolid. Charging Vg=+/- 7V with 40 s hold time.

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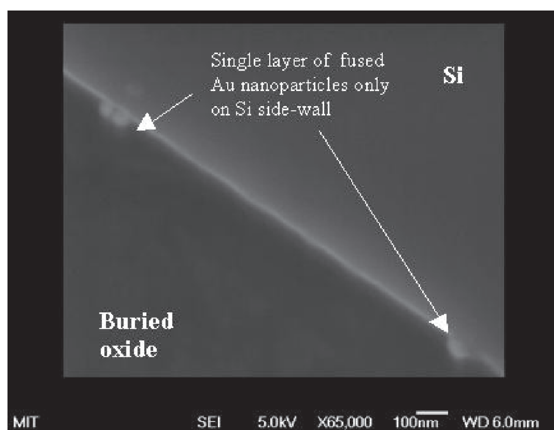
Study of Silicon Nanowire Growth for Electronics Applications

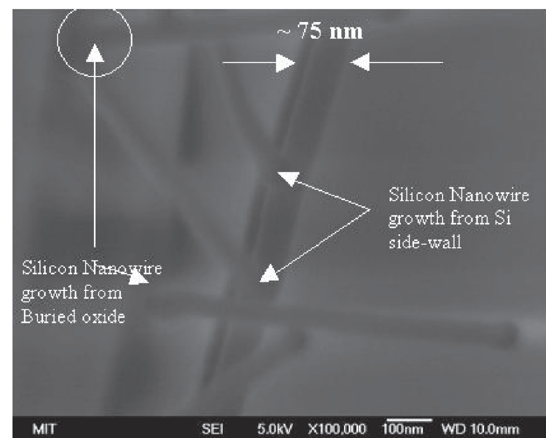
O.M. Nayfeh, S. Boles, D.A. Antoniadis, C.V. Thompson, E.A. Fitzgerald
Sponsorship: Singapore-MIT Alliance

Silicon nanowire transistors (SiNWTs) have been shown to be promising candidates for end-of roadmap devices. This potential is due to both electrostatics and transport properties. The SiNWTs gain potentially better electrostatic control, compared to planar MOSFETs, by utilizing a fully wrapped-around gate [1]. Moreover, some studies have measured higher mobilities than bulk values [2]. Silicon nanowire transistors have been fabricated by both the top-down and bottom-up methods. The top-down method employs lithography and etching to fabricate the SiNWs, whereas the bottom-up method involves the growth of the nanowires from catalyst nanoparticles. The growth from catalyst seeds most often involves the vapor-liquid-solid (VLS) growth method. In this work, we first investigated the formation of catalyst nanoparticle seeds and the growth of SiNWs via VLS growth on Si-substrates. We have successfully grown silicon nanowires from both Au nanoparticle catalysts fabricated via e-beam evaporation and dispersal of Au nanoparticles from solution. After fabrication/dispersal of nanoparticles on a Si substrate, the nanowires are grown in silane by atmospheric pressure chemical vapor deposition (APCVD) in the (500-650 C) temperature range.

We are currently working on fabricating SiNWTs by bridging silicon nanowires across an SOI microtrench [3]. Growth of bridging silicon nanowires from the thin Si side-walls of SOI microtrenches using metal nanoparticles as catalyst is plagued by growth on all faces of the architecture, due to metal catalyst remaining on the top of the active Si layer and on the buried oxide. We developed a protocol that would allow us to selectively attach a single layer of Au nanoparticles only on the thin Si sidewalls of an SOI microtrench. SEM imaging following this procedure shows Au nanoparticles only on the thin Si sidewalls (Figure 1), which will thus enable the selective growth of bridging nanowires only from these sidewalls. Figure 2 shows an SEM image of silicon nanowire growth on a sample that did not have the Au nanoparticles removed from the buried oxide and top Si. As can be seen, growth occurs on all faces of the sample.



▲ Figure 1: SEM image demonstrating the ability to selectively attach a single layer of Au nanoparticles only on the thin Si sidewall. The nanoparticles on the buried oxide and top Si layer have been removed.



▲ Figure 2: SEM image of silicon nanowires grown on samples with Au nanoparticles remaining on the buried oxide and top Si layers. As can be seen, nanowire growth is plagued on all surfaces of the architecture due to the presence of the un-removed Au nanoparticles.

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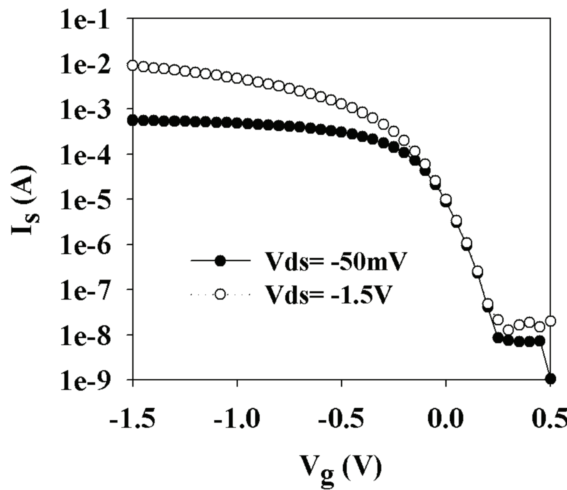
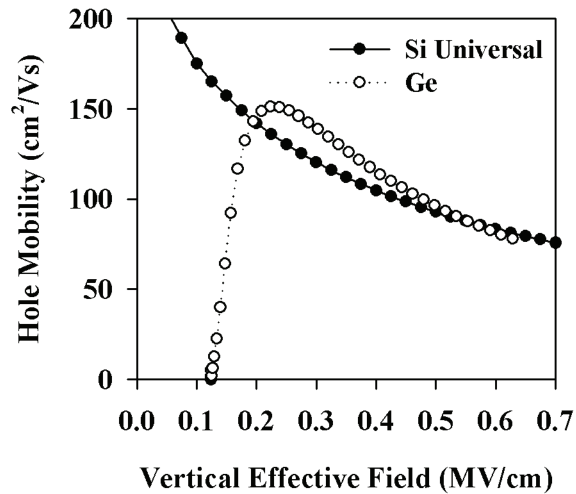
Bulk Germanium MOSFETs Using High-K Dielectrics

A. Ritenour, J. Hennessy, M.L. Lee, R.Z. Lei, E.A. Fitzgerald, D.A. Antoniadis
Sponsorship: MARCO MSD

The advent of high-k gate dielectrics provides a new opportunity to consider semiconductors other than silicon for future ultra-scaled MOSFETs. Germanium has started to receive attention because it simultaneously offers significant enhancements in bulk electron and hole mobility relative to silicon. However, the inherent instability of germanium oxide makes interface engineering particularly challenging. Metallorganic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD) are being explored as options for gate stack deposition. Figure 1 shows the transfer characteristics for a germanium p-MOSFET with an ALD WN/$LaAlO_3$/AlN gate stack. Figure 2 shows the extracted hole mobility for this device. ALD gate stack deposition was performed by K. Kim and R. Gordon at Harvard University.



▲ Figure 1: Typical as-measured Is-Vg characteristics for bulk Ge p-MOSFETs with ALD WN/$LaAlO_3$/AlN gate stack.



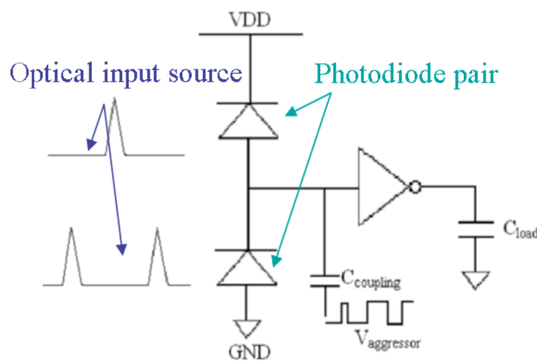
▲ Figure 2: Extracted hole mobility for Ge p-MOSFET. The universal hole mobility for silicon is shown for reference.

Variation Analysis in Optical Interconnect

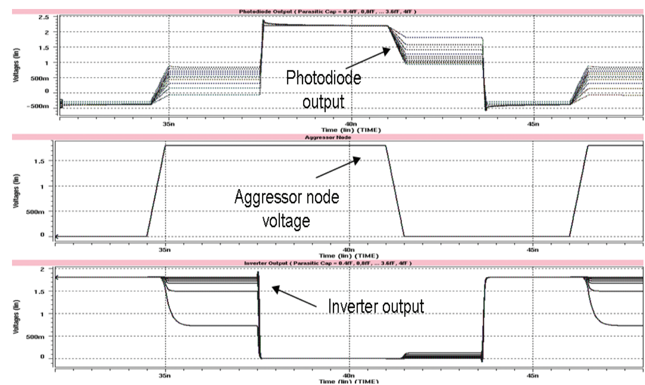
K. Balakrishnan, D.S. Boning
Sponsorship: MARCO IFC

Due to the continuous scaling of CMOS technologies and the resulting need for fast, robust, and accurate signal propagation, electrical interconnect faces many difficult challenges. Optical interconnect is emerging as a possible alternative to meet these challenges; however, the robustness issue must be examined to ensure the viability of this option. The goal of this work is to determine the variation sensitivity of an ultra-fast pulse-based optical receiver circuit [1], which serves to convert incoming optical pulses into an outgoing electrical signal. Specifically, the fast pulse-based scheme must be examined because of its potential advantages in robustness due to its use of precise, mode-locked laser source pulses as an input, which in turn reduces jitter. Particularly in the context of clock-distribution applications, the robustness of this receiver circuit is paramount. Previous work in this area focused on variation analysis in passive optical components of the signal distribution system, such as waveguides and splitters.

Current work examines the effects of different sources of variation on the output of the ultra-fast, pulse-based, optical receiver circuit shown in Figure 1. Possible sources of variation include the mismatch and variation of input power, optical input power mismatch and variation, load capacitance variation, parasitic capacitive coupling, and static and dynamic power supply noise. As an example, Figure 2 shows simulation results of the impact of parasitic capacitive coupling on the output waveform of the optical receiver circuit. Further analysis focuses on the impact of technology scaling on the robustness of the circuit. Current work also compares the optical signal distribution scheme to a traditional electrical H-tree distribution scheme in terms of variation. Possible future work in this area may concentrate on the design and implementation of test circuits to measure variations in optical interconnect.



▲ Figure 1: Ultra-fast pulse-based optical receiver circuit. Alternating short optical input pulses from a mode-locked laser source are received at the top and bottom photodiodes. These pulses are then converted to rising and falling edges, which are buffered by the static CMOS inverter and can be used as a clock signal.



▲ Figure 2: Simulation waveforms depicting the impact of parasitic capacitive coupling on the optical receiver circuit. Because the photodiode pair output is a floating node, the impact of a nearby aggressor node can be detrimental to the inverter output, given a sufficiently large coupling capacitance (~0.4 fF).

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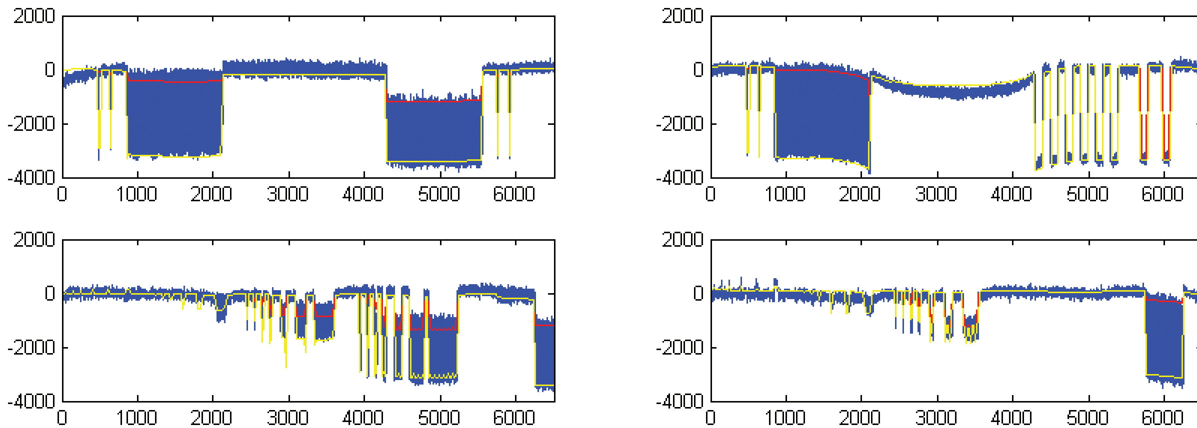
Modeling of Pattern-dependencies in the Fabrication of Multilevel Copper Metallization

H. Cai, D.S. Boning

Sponsorship: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, MagnaChip

This research aims to understand, model, and optimize the interaction between copper electroplating and chemical mechanical polishing (CMP) processes. Currently, this research focuses on the coupling that exists due to pattern-dependent topography, which propagates from the electroplated surface into CMP dishing and erosion. We propose a physics-based time-stepped copper electroplating model taking an IC chip layout as input and producing a map of copper film thickness across the chip with good predictive accuracy and reasonable computational load. In the new model, the additive surface coverage is computed by considering the evolution of the surface geometry during copper film growth and the surface dissolution/absorption processes resulting from two major additives, accelerators and suppressors. With a limited set of parameters, the simulation root-mean-square (RMS) errors of envelope and step-height have been reduced to 100-200 Å, which is comparable to the previously developed, non-time-step, semi-physical electroplating model. Figure 1 shows the simulated topography in comparison with measured data. The new framework can be seamlessly integrated with our chip-scale chemical-mechanical polishing (CMP) model [1] and extended to the multi-level copper metallization case.

The multi-level versions of the time-stepped electroplating model and the physics-based, multi-level CMP model are in progress. Current work is underway to integrate the time-stepped electroplating and CMP models, and to develop a co-optimization methodology that minimizes the thickness of the deposited copper film, process time, and consumable usage to achieve a high-performance and environmentally-friendly copper interconnect process.



▲ Figure 1: Surface height variations resulting from copper electroplating pattern dependencies. High-resolution profile scans are shown in patterned areas (blue) and the corresponding simulated topography (yellow for lower area and red for upper area) in each grid. Horizontal axis is position (in μm); vertical axis is height (in Å).

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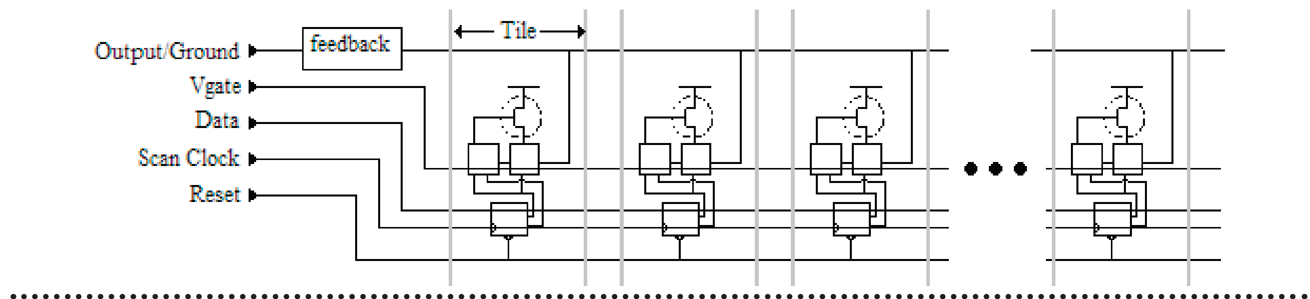
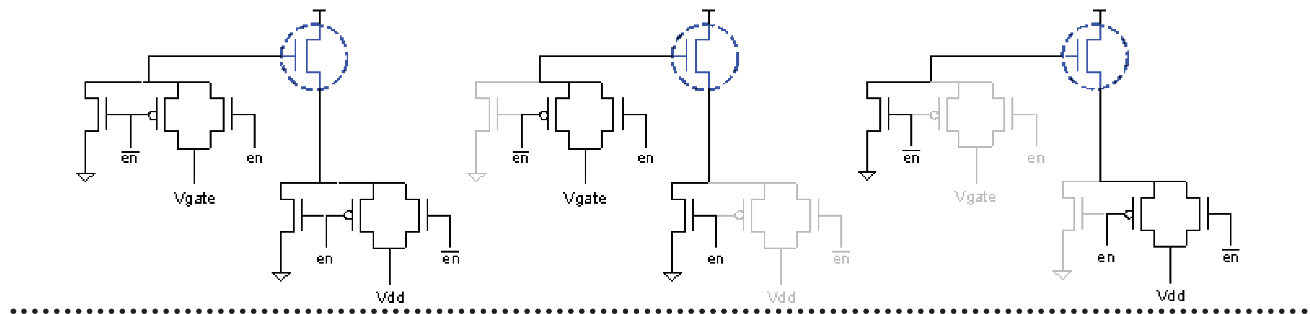
Test Circuits for Assessment of IC Variation

K.G.V. Gettings, D.S. Boning
Sponsorship: Bell Labs CRFP Fellowship, IBM

The study of process variations has greatly increased in importance due to the aggressive scaling of technology. Previous research [1] has shown the substantial impact that process variations in front-end-of-line structures have in reducing yield in integrated circuits. Robust circuit design depends on a more complete characterization of these variations and their impacts on circuit-level parameters. This project addresses this issue by developing a methodology capable of testing a large number of front-end-of-line (FEOL) and back-end-of-line (BEOL) structures and by modeling variations in threshold voltage, leakage currents and power dissipation, among others. This is achieved by designing and implementing test circuits that include a large number of high performance devices-under-test (DUTs) controlled by low-leakage switches and sensors to ensure a nominal value at the DUT terminals. Accessing analog characteristics of a large number of DUTs will make it possible to gather the statistics necessary to identify and model these variations and to prevent them from contributing to performance failure. This architecture provides a replicable methodology so that the effect of variation sources may be quantified in different technologies. This project studies variations in circuits due to the two fundamental sources of variations in integrated circuits, as noted by Nassif [4]: environmental factors, e.g., power supply variation, and physical factors, e.g., variation in polysilicon dimension. Physical factors can fall into two categories: "die-to-die physical variations" and "within-die physical variations." Analysis includes separation of spatial, layout-dependent, and random variation components both within the die and as a function of wafer location. The test chip is currently being built and results should be available soon.



▲ Figure 1: Array of transistors controlled by a limited number of pads.



▲ Figure 2: Low leakage switch (left), when enabled (center) and when not enabled (right) and DUT (circled).

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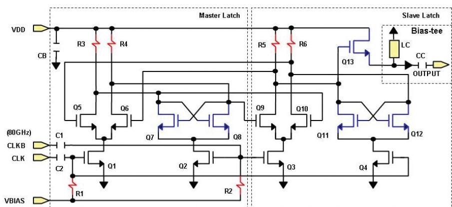
Modeling and Extraction of Variation in Physical Process Parameters

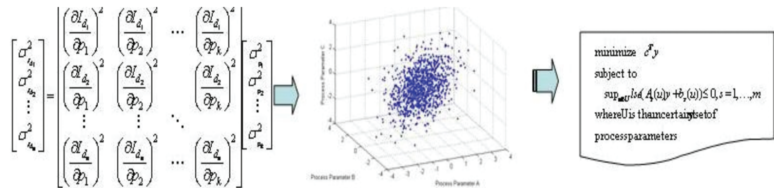
D. Lim, D.S. Boning
Sponsorship: MARCO C2S2, IBM

The impact of process variation on the performance of modern high-speed and low-power integrated circuits has been increasing as the semiconductor technology has scaled down. In modern design process, it is necessary to have an accurate variation model characterizing the statistical variability of process and design parameters. This variation model enables circuit designers to predict parametric yield in an early stage and optimize designs to obtain high-yielding chips. Finding physical process parameters that give critical contribution to circuit response fluctuation and estimating the statistical properties of the process parameters are important in building an accurate variation model. The statistical properties of process parameters can be calculated by a back-propagation of variance (BPV) method, which uses the variance of electrical responses measured by circuits to calculate the variance of process parameters based on a first-order response surface model (RSM) [1]. Test structures have a number of different configurations in terms of bias condition and geometry. First-order derivatives of circuit responses, e.g., drain currents and oscillation frequency, to process parameters are extracted by circuit simulators such as HSPICE and SPECTRE. The original BPV method has been extended to capture the correlation between process parameters and devices in this work.

We suggest a current mode latch (CML) for the characterization of high-speed analog manufacturing processes. A CML in Figure 1 can generate a self-oscillation frequency in different bias conditions, and simple digital circuitry can accurately measure the statistical properties of the self-oscillation frequencies in different configurations [3]. The BPV method can use the measured frequency data to estimate the variation of physical process parameters. Output frequency data can analyze device and passive component mismatch as well. A confidence ellipsoid with a certain probability in *n*-dimensional space captures the variations of process parameters. The variances and co-variances of process parameters extracted from the BPV method determine the shape of the ellipsoid. Traditional deterministic optimization methods can be extended to improve the robustness of circuit outputs by sacrificing reasonable margin in optimal values. Given the ellipsoidal uncertainty model of process parameters, we can find the robust global optimum of circuit performance and power consumption using convex optimization tools [3].



▲ Figure 1: The CML frequency-divider generating a self-oscillation signal to characterize process variation.



▲ Figure 2: Procedure of statistical optimization using the BPV method to characterize variance and the convex optimization to find a robust optimum.

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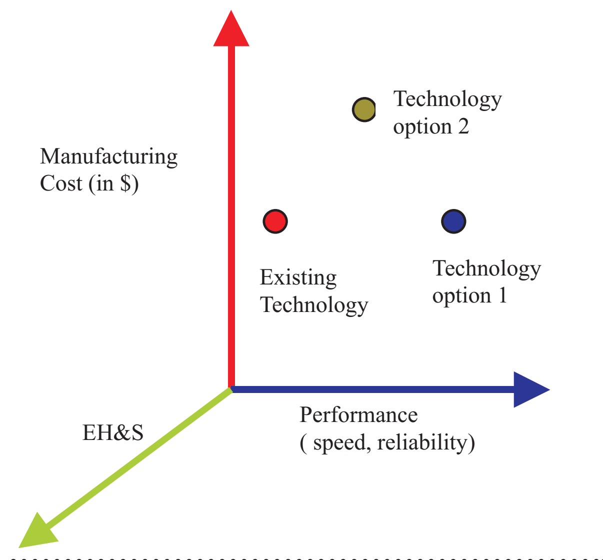
Combined Technology and Environmental Assessment of 3D Integrated Circuit Process Alternatives

A. Somani, P. Gschwend, D.S. Boning

Sponsors: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

According to the International Technology Roadmap for Semiconductors (ITRS), the industry will make significant strides in performance in future technology nodes. There is a need to introduce novel materials and process technologies with innovative integration schemes since scaling is not enough to achieve greater performance in devices. Analyses of the advantages of these new options have conventionally focused on how performance improves and cost reduces with the new material or process. Unfortunately, significant time and investment in materials and process technology development can be lost if environment, health, and safety (EHS) are not factored into the early decision-making process. We suggest that future technology options should be evaluated on three axes, including not only cost and performance but also EHS (Figure 1). Future process technology development must involve an approach to assess the EHS impacts of new technologies and alternatives early in the research and development cycle.

In this present effort, we propose a comparative methodology for environmental impact evaluation along with a method to evaluate emerging silicon-based technologies [1]. The proposed methodology is applied to an emerging technology: three-dimensional (3-D) integrated circuits (ICs). In this work, we focus on a 3-D integration process based on Cu thermo-compression bonding. The MIT 3-D approach [2] is a metal Cu-Cu thin-first via-last process technology in which two active device wafers are stacked in a back-to-face fashion and bonded by means of low-temperature Cu-to-Cu thermo-compression. The comparative methodology was applied to the MIT 3-D IC approach in reference to state-of-the-art IC technology (2-D IC) and then additional and new processes were tabulated (Table 1). The objective is to identify unit processes that neither are environmentally benign nor perform from the technological viewpoint. Handle-wafer attaching and releasing is one unit process that uses thick Al release-layers. Therefore, in on-going research we are trying to find solutions for handle wafer and also low-temperature bonding processes.



▲ Figure 1: New and existing technology options exhibit different trade-offs in performance, cost, and environment, health, and safety.

Unit operation	# Unit steps required in 2D process flow (for one wafer)	# Additional unit steps required in 3D process flow (to add one layer)
Photo/Ashing	25	1
Dry Etch	17	2
Wet etch/Clean	31/14	¾
CVD	11	1
CMP (Cu and Oxide)	14	2
Sputtering Al	1 (0.5 µm for metal 1)	2 (20 µm)
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Bonding	0	2
Grinding	0	1
Implant	9	0
Oxidation/ Annealing	4/7	0/2

▲ Table 1: First-order unit process comparison between 2D and 3D IC flows.

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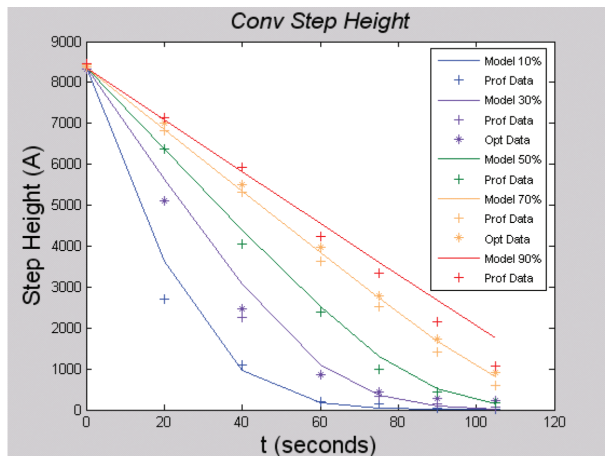
Polishing Pad Effects in CMP

D. Truque, X. Xie, D.S. Boning
Sponsorship: SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

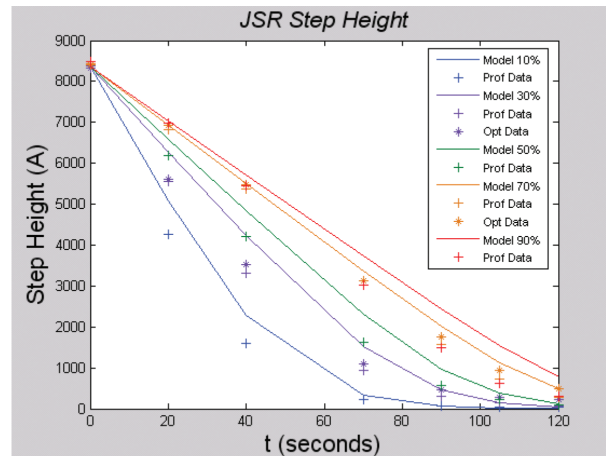
Our group has proposed several chip-scale, pattern-density-dependent chemical mechanical polishing (CMP) models. [1-2] CMP is an enabling technology used in various front- and back-end semiconductor processes as well as in MEMS. A good understanding and modeling of CMP is essential to optimize the process, improve the yield, and reduce consumables. Our model uses parameters related to physical properties of polishing pads and slurries, but they are extracted purely from experimental data as fitting coefficients. In collaboration with JSR Micro, a pad and slurry manufacturer, we will relate these parameters to pad stiffness, pad surface properties, slurry particle size, etc.

The most recent experiments compared the standard industry pad (IC1000) against a novel pad by JSR that includes water soluble particles (WSPs). The WSPs aid in keeping the pad bulk stiff, which improves pad planarization. When the WSPs reach the surface and contact the slurry, they passively dissolve, creating micropores in the pad that help in the slurry transport and material removal to increase removal rate and provide uniform removal.

From the data examined, we concluded that the WSPs improve the planarization length of the polishing process. The results also showed that the IC1000 had a higher removal rate than the JSR pad, but at the expense of pattern density dependencies. Both pads had comparable removal rates for pattern densities around 70%. The JSR pad had a lower pattern-dependency than the IC1000 pad, where regions of lower density polished considerably faster than regions of higher density. We noticed some edge dependencies with the JSR pad, and these dependencies caused regions near the edge to polish faster, but this higher removal rate near the edge might be caused by the wafer-holding ring on the CMP tool used.



▲ Figure 1: Step height evolution for different pattern densities for the conventional IC1000 polishing pad. Data points show profilometry and optical measurements; line shows prediction of model.



▲ Figure 2: Step height evolution for different pattern densities for the JSR water-soluble particle-enhanced pad. Data points show profilometry and optical measurements; line shows prediction of model.

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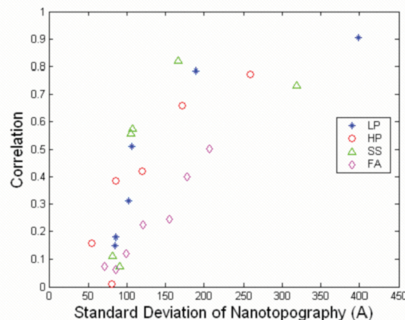
Application of CMP Models to Issues in Shallow Trench Isolation

X. Xie, D.S. Boning
Sponsorship: IMEC, Infineon Technologies, Rohm and Haas, Siltronic AG

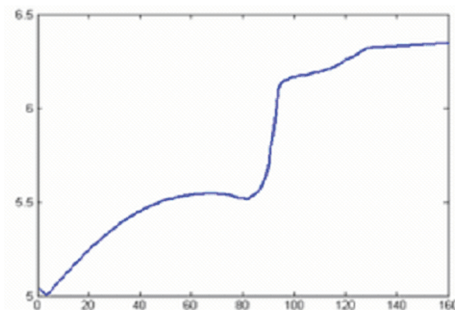
As advancing technologies increase the demand for planarity in integrated circuits, chemical mechanical planarization (CMP) continues to be the enabling technology in IC fabrication, while new challenges emerge and a new process-monitor technique has been proposed. Our CMP models enable us to study various issues in shallow trench isolation (STI) processes.

Nanotopography – a term used to describe (10-100-nm) surface height variation extending across millimeter-scale lateral distance on raw wafer – can result in additional oxide dishing and nitride erosion in STI. In this study, a set of experiments was designed to study nanotopography and CMP interactions in STI layer stacks (oxide/nitride/oxide), in both blanket wafers and patterned wafers. Our blanket wafer data analysis shows that initial nanotopography maps correlate well with the high-frequency part of post-CMP variation (Figure 1), although the low-frequency part (from CMP tool, pad, and process non-uniformity) accounts for a larger magnitude or proportion of post-CMP variation. The result implies weak nanotopography impact for polishing STI-patterned wafers for the starting nanotopography and CMP processes considered here. The analysis of patterned-wafer data also shows that any correlation between the nanotopography map and the electrical test map is very weak, if it exists at all.

Frictional monitoring endpoint detection (EPD) has proven to be feasible for monitoring the STI CMP process. Experimental data indicates that frictional effects generated by the pattern structures and various layered materials on the wafer create distinct and characteristic responses for determining an appropriate endpoint. With the existing CMP model, we studied the underlying physics of the friction model and related the evolution of patterned wafers to friction endpoint traces. The new model accounts for the spatial configuration of the surface profile and its impact on friction. Three sets of experiments were conducted using ceria-based slurries; the resulting motor current signals differ substantially, and the predicted friction traces agree reasonably well with the experiments (Figure 2).



▲ Figure 1: For all the blanket wafer polishes that stopped in the oxide layer, the correlations between the nanotopography map and the oxide amount removal map are shown, versus the standard deviations of nanotopography maps. The plot shows that larger nanotopography height variation results in a stronger correlation with spatial variation.



▲ Figure 2: The model predicted motor current (vertical axis, arbitrary units) versus time (horizontal axis, seconds) based on the surface topography evolution. The prediction agrees well with measured motor current. The relatively flat region starting at 130 seconds signals the endpoint.

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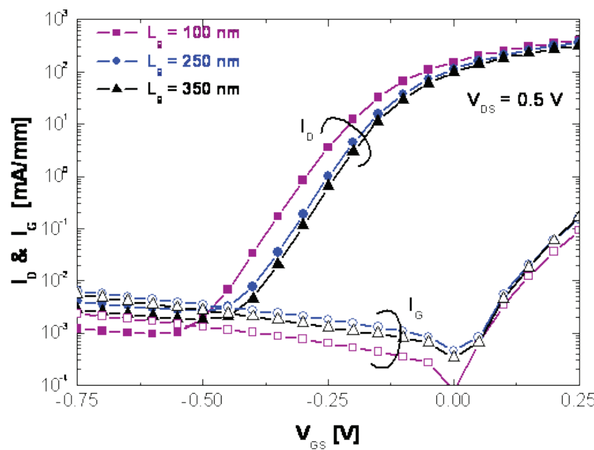
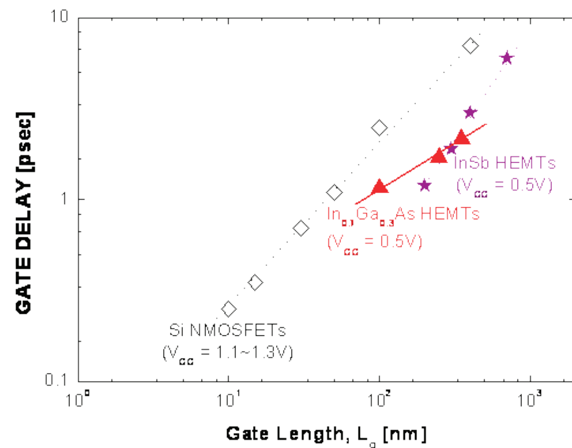
Potential of InGaAs High-electron Mobility Transistors as a Beyond-CMOS Logic Technology

D.H. Kim, J.A. del Alamo
Sponsorship: Intel, MARCO MSD

The InAlAs/InGaAs high-electron mobility transistors (HEMTs) closely lattice-matched to InP exhibit extraordinary frequency response, as measured by cutoff frequency (f_T). The current record is 562 GHz for a gate length (L_g) of 25 nm [1]. However, these devices suffer from poor electrostatic integrity and inadequate scaling behavior and as a result possess questionable usefulness for logic. We have been investigating InGaAs HEMTs as a future high-speed and low-power logic technology for applications beyond CMOS [2-3]. Figures of merit relevant to logic, such as logic-gate delay (CV/I), I_{ON}/I_{OFF}, drain-induced barrier lowering (DIBL), and subthreshold slope (S) are evaluated in this family of the device technology. We have found that these devices exhibit promising logic characteristics. In particular, 100-nm L_g devices yield DIBL as low as 80 mV/V, S of 77 mV/decade, and gate delay of 1.2 psec, at a V_{CC} of 0.5 V. More importantly, we have found that these devices, from a logical point of view, reach their scaling limit at 100-nm gate length of $In_{0.7}Ga_{0.3}As$ HEMTs. Realizing the logic potential of $In_{0.7}Ga_{0.3}As$ HEMTs will require a more scalable device design with better electrostatic integrity. If this requirement can be accomplished, InGaAs HEMTs could well be the technology of choice when the CMOS roadmap comes to an end.



▲ Figure 1: Sub-threshold characteristics of $In_{0.7}Ga_{0.3}As$ HEMTs, at a V_{CC} of 0.5 V. This graph a very sharp sub-threshold slope and a very low off-state current that is mostly limited by gate leakage current through the Schottky gate. The slight softening of the sub-threshold slope as L_g approaches 100 nm is a manifestation of short-channel effects.



▲ Figure 2: Logic gate delay (CV/I) vs. gate length for our InGaAs HEMTs, state-of-the-art Si-MOSFETs and InSb HEMTs [4]. In our devices, CV/I was chosen to have I_{ON}/I_{OFF} ratio of 10^3, at a V_{CC} of 0.5 V. Our 100-nm $In_{0.7}Ga_{0.3}As$ HEMTs exhibit a gate delay of 1.16 ps, which is about a factor of 2 times better than equivalent Si-MOSFETs. This excellent result speed result arises from the superior electron transport properties of our heterostructure.

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Electrical Degradation of GaN High Electron Mobility Transistors

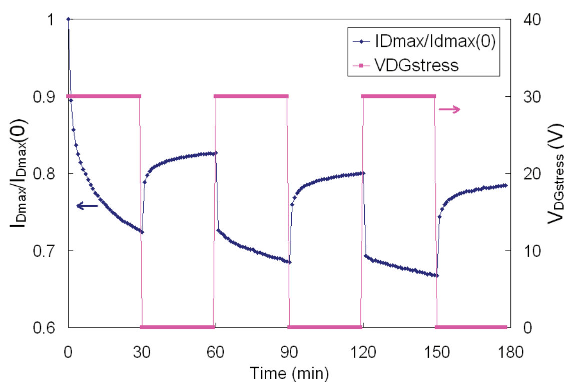
J. Joh, J.A. del Alamo
Sponsorship: DARPA, ARL

Due to their extraordinary RF power performance, GaN-based transistors have recently been under intense research. As a result of their high breakdown electric field (>3 x 10^6 V/cm), GaN-based devices can operate at a voltage as high as 120 V. The AlGaN/GaN high electron mobility transistors (HEMT) have already shown an output power density of 10.7 W/mm at 10 GHz. This outstanding performance makes these devices of great interest for high-power, high-frequency applications such as WiMAX or WLAN base stations. In spite of these superior properties, GaN HEMTs have serious reliability problems that must be solved before this technology can become commercialized. Our research attempts to identify the physical mechanisms responsible for the problematic reliability of GaN HEMTs.

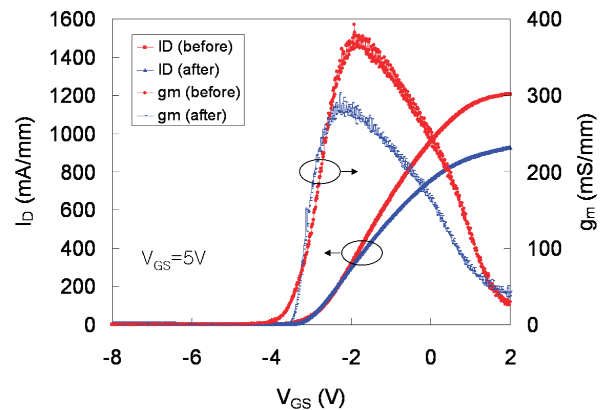
We are studying the fundamental degradation mechanisms of industrial GaN HEMTs. In particular, we are studying the decrease of the maximum drain current (I_{Dmax}) and the increase of the source and drain resistances (R_S and R_D) as the device is electrically stressed. We have constructed an automated stressing and characterizing routine, and we have performed DC stressing tests under various biasing conditions and environments. A typical stress-recovery experiment appears in Figure 1, where I_{Dmax} degradation is shown as the device is stressed with V_{DG}=30 V while maintaining V_{DS}=0. In this experiment, periods of stress on the device alternate with periods of recovery during which the characteristics of the device are also monitored. Before and after the stressing experiments and at selected points in between, complete characterization of the device is performed. Figure 2 shows, for example, the change in the transfer characteristics before and after the stressing experiment of Figure 1.

Based on experiments like this, we have made some preliminary findings. We have found that the degradation of I_{Dmax} strongly correlates with an increase in R_D and R_S. These changes seem to arise from a decrease of the carrier density in the extrinsic portion of the device. This decrease occurs in a process of trap-generation and subsequent electron-trapping in the extrinsic device. The trap-generation process appears to be driven by the magnitude of the electric field between the gate and the source or drain. Electron detrapping is clearly observed in Figure 1 during the recovery periods that are interleaved with stressing.

Our research addresses the fundamental degradation physics of GaN HEMTs. This study will help us to understand failure mechanisms in detail and to develop processes and device designs that minimize these deleterious effects.



▲ Figure 1: Degradation of maximum drain current (normalized to the original value) versus time. The purple line shows the stressing bias V_{DG}. The device was stressed at V_{DG}=30 V and V_{DS}=0 V for 30 minutes. From t=30 to t=60 min, the device was at V_{DG}=V_{DS}=0 V. The same cycle was repeated three times.



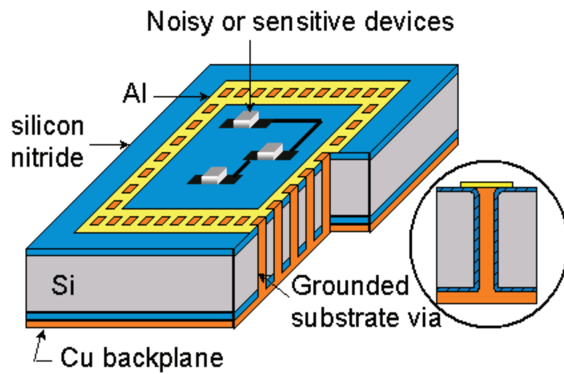
▲ Figure 2: Drain current and transconductance before (t=0) and after (t=180 min) stressing in the experiment of Figure 1.

Through-substrate Interconnects for Millimeter-wave Mixed Signal Systems

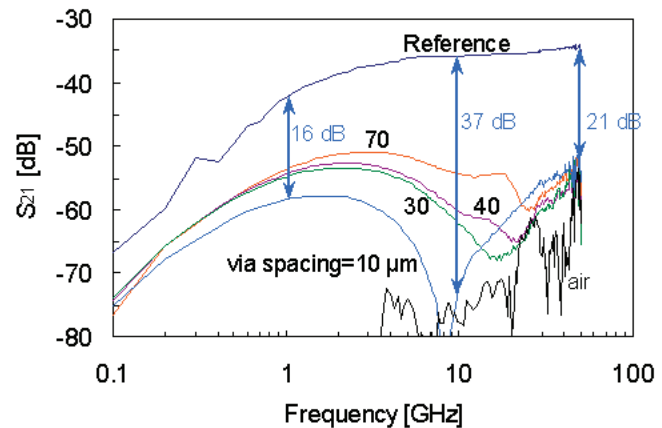
J.H. Wu, J.A. del Alamo
Sponsorship: Applied Materials Graduate Fellowship

Advances in silicon technology may eventually displace III-V semiconductor devices in the mm-wave regime. This would make bandwidth available for affordable and pervasive applications. The challenges for Si are low-loss interconnects and packaging, substrate isolation, and thermal management. We have developed a through-substrate via technology that allows for low-impedance ground distribution and substrate crosstalk isolation up to 50 GHz. This technology also has potential for addressing other substrate issues in the mm-wave regime [1]. The inset of Figure 1 depicts the through-wafer interconnect.

Substrate crosstalk between sensitive RF circuits and analog and digital blocks is one of the most critical problems facing mixed-signal circuit designers. We have developed a Faraday cage isolation structure using through-wafer vias to surround noisy or sensitive circuits (Figure 1). Our Faraday cage exhibits an isolation of 37 dB at 10 GHz and 21 dB at 50 GHz. Figure 2 shows S_{21} measurements of Faraday cages with different via spacing compared to a reference structure. The distance between the transmitter and the receiver is 100 µm. Reducing the density of vias of the Faraday cage diminishes its performance but still significantly suppresses substrate crosstalk into the mm-wave regime. Faraday cage measurements from a previous process show better performance at lower frequencies, 42 dB in isolation at 1 GHz versus 16 dB in isolation for this new process [1-2]. However, this is due to a better silicon nitride liner in our new process, which adds an extra capacitance at low frequencies and hinders the performance of the Faraday cage. This liner can be reduced or eliminated in future processes specifically for this application to boost isolation at lower frequencies.



▲ Figure 1: Drawing of a Faraday cage using through-substrate vias to surround a noisy or sensitive circuit. The substrate via (inset) is etched in silicon, lined with silicon nitride, and filled with electroplated copper, followed by copper CMP. An aluminum pad caps the top of the via.



▲ Figure 2: S_{21} vs. frequency for Faraday cages with different via spacing and a reference test structure at a distance of 100 µm. The diameter of the vias is 10 µm. At the smallest via spacing of 10 µm, the Faraday cage reduces substrate noise by 37 dB at 10 GHz and 21 dB at 50 GHz.

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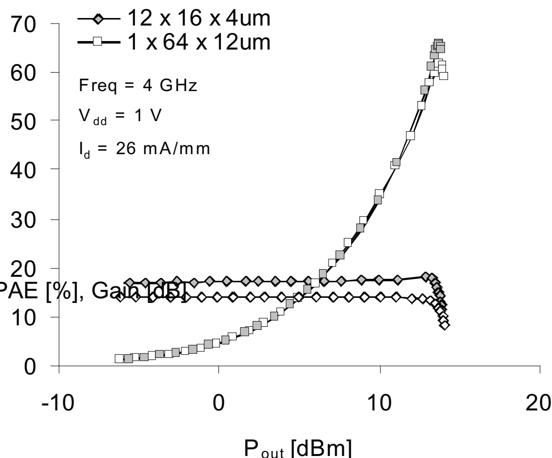
Performance and Limitations of 65-nm CMOS for Integrated RF Power Applications

J. Scholvin, D.R. Greenberg (IBM), J.A. del Alamo
Sponsorship: IBM Faculty Award, IBM Ph.D. Fellowship

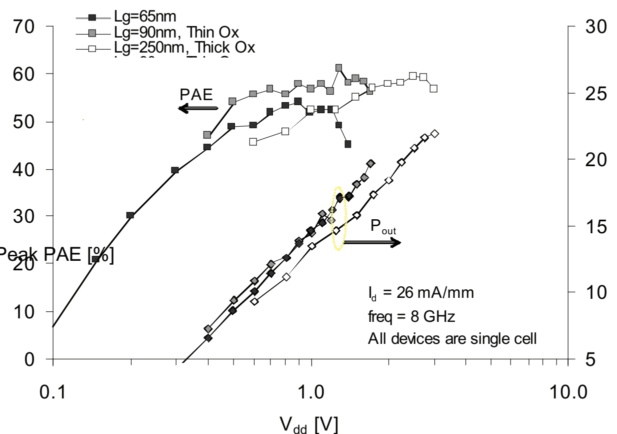
The microelectronics industry is striving to reduce the cost, complexity, and time-to-market of wireless systems through single-chip integration of mixed-signal radio frequency RF/digital functions. Achieving such integration while minimizing the increased cost of technology add-ons demands a great deal from the base CMOS technology. In this regard, the integration of the power amplifier (PA) function remains a particular challenge as technology geometries scale down. Gate length (L_g) scaling yields better high-frequency response, promising higher power-added efficiency (PAE). These benefits come at the cost of a lower drain voltage, which demands a higher output current and thus wider devices in order to produce a given output power level (Pout).

In this work, we have studied the suitability of the 65-nm CMOS node for integrated RF PA applications. We have found that the standard 65-nm logic device is capable of achieving PAE values greater than 65% at 4 GHz (Figure 1), with Pout scalable to about 17 dBm, which is sufficient for many applications. We have also compared the 65-nm node with prior CMOS generations: from 250 to 90 nm (Figure 2). Comparison with the 90-nm node reveals that back-end scaling in the 65-nm technology has lead to increased interconnect resistance, which limits the maximum P_{out}. This problem should be addressed through optimized cell layout and wiring level selection.

For low power levels (below 16 dBm or 40 mW), the 65-nm technology CMOS node offers excellent efficiency over a broad frequency range. Its RF power performance approaches that of 90-nm devices both in peak PAE and output power density. Using cells with multiple short gate-width fingers can optimize performance. . Scaling the power level therefore demands wiring many fingers and cells in parallel. The higher sheet resistance of the BEOL of 65-nm CMOS leads to difficulty in scaling output power using existing layout. Simulation indicates that further optimization of device layout, including the use of stacked or thicker upper metal levels, should mitigate the negative effects of the BEOL scaling. Through this, the 65-nm node can provide efficient integrated power amplifier functionality for many applications, even in a deeply-scaled logic CMOS technology without costly PA-specific adders.



▲ Figure 1: Power measurement of two 768-µm-wide, 65-nm devices. The 12-cell device (12 cells of 16 fingers, each finger 4-µm wide) delivers a peak PAE of 65.7% at a power of 13.8 dBm (31.2 mW/mm) at 4 GHz [2].



▲ Figure 2: Peak PAE and output power density as a function of V_{dd} for the three different CMOS technologies [1-2].

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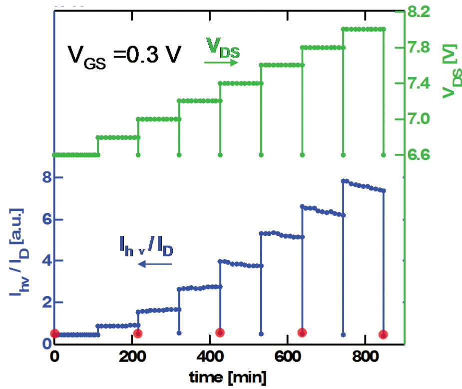
[2] J. Scholvin, D.R. Greenberg, and J.A. del Alamo, "Performance and limitations of 65 nm CMOS for integrated RF power applications," in *Proc. IEDM 2005*, Washington, D.C., Dec. 2005, pp. 369-372.

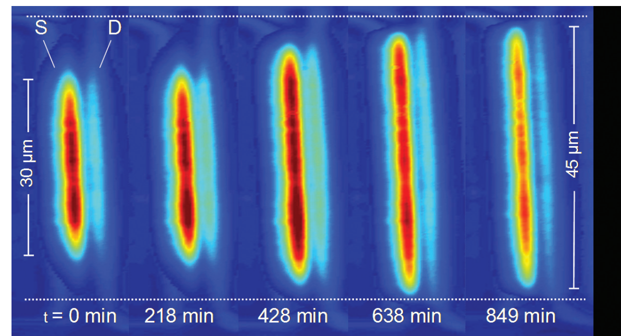
Non-Uniform Degradation Behavior in RF Power GaAs PHEMTs

A.A. Villanueva, J.A. del Alamo
Sponsorship: Mitsubishi Electric

GaAs pseudomorphic high-electron mobility transistors (PHEMTs) are widely used in RF power applications. Since these devices typically operate at high power levels and under high-voltage biasing, their electrical reliability is of serious concern. Previous studies have identified several distinct degradation phenomena in these devices, such as impact-ionization (II), hot electron trapping, and surface corrosion [1-3]. However, so far reliability studies have always assumed that degradation takes place uniformly across the width of the device. In our research, we investigate the degradation behavior across the width of the device by studying light emission. Since light emission is correlated with II [4], a photograph of emitted light gives us a spatial picture of II and electric field. By taking light-emission photographs during bias stressing experiments, we observed the light emitted from a device as it is being stressed. Figure 1 illustrates the bias conditions and total light intensity emitted (normalized to I_D) for such an experiment. As V_{DS} is stepped up, we see that the total light emitted increases (as expected, since the electric field and II are increasing). Examining the light emission photos at select points during the experiment (Figure 2), we see that the light emission is very non-uniform along the width of the device: initially it is heavily concentrated in the center, but then with stressing it spreads out. This behavior suggests that the electric field is higher in the center of the device, and thus degradation is occurring preferentially there. We performed analogous light-emission experiments on test structures (TLMs) and observed similar behavior. Materials analyses of the TLMs showed that a non-uniform recess length was the cause for the non-uniform electric field distribution. Thus, in order to improve long-term device reliability, it is very important to identify and minimize non-uniformities in device geometry which can affect the degradation behavior of a device.



▲ Figure 1: Bias V_{DS} (green) and total light intensity divided by I_D (blue) vs. stressing time in a typical PHEMT light-emission experiment. Each point represents a time when a light emission photograph was taken. Before V_{DS} is stepped up, it is brought to its initial value of 6.6 V in order to get pictures at regular intervals at a constant value of V_{DS}. Points highlighted in red indicate points depicted in Figure 2.



▲ Figure 2: Light-emission photographs from source and drain of PHEMT, at five points during step-stressing experiment. Taken at V_{GS}=0.3 V, V_{DS}=6.6 V. Gate width W_g = 50 µm.

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[4] E. Zanoni, A. Paccagnella, P. Pisoni, P. Telaroli, C. Tedesco, C. Canali, N. Testa, and M. Manfredi, "Impact Ionization, recombination, and visible light emission in AlGaAs/GaAs high electron mobility transistors," *Journal of App. Physics*, vol. 70, pp. 529-531, 1991.

A Self-aligned, InGaAs, High-Electron-Mobility, Transistor-Device Architecture for Future Logic Applications

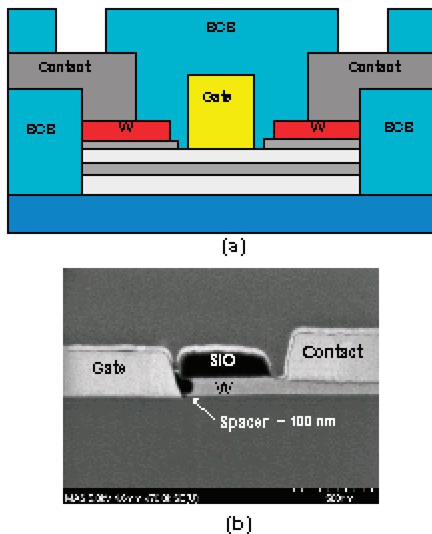
N. Waldron, J.A. del Alamo

Sponsorship: MARCO MSD, Intel Foundation Ph.D. Fellowship

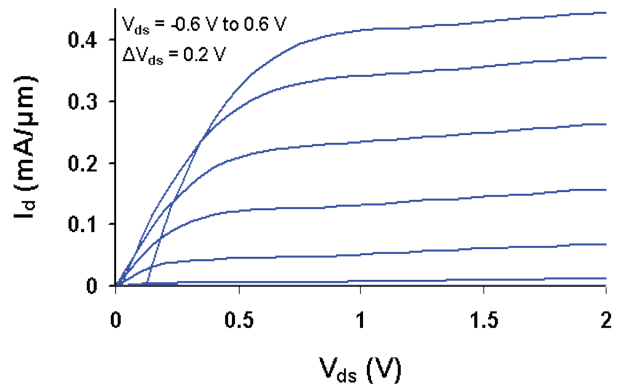
As CMOS approaches the end of the scaling roadmap, the need to identify a new logic device technology is becoming increasingly pressing. The InAlAs/InGaAs high electron mobility transistor (HEMT) has been demonstrated to show great promise for logic applications [1] and we investigate that material system in this project. Traditionally this type of device has been developed for millimeter-wave rather than digital applications, resulting in a large extrinsic footprint and high parasitics. In contrast, Si CMOS, which dominates the digital IC market, has benefited from aggressive gate-scaling coupled with close attention to extrinsics and packing density.

In order to realize the potential of InAlAs/InGaAg HEMTs in large-scale digital circuits, it is necessary to address the problems of the extrinsic resistances and capacitances that the non-self-aligned design and large footprint bring about. To this end we have designed a device architecture that incorporates a novel shallow-trench isolation and self-aligned gate scheme (Figure 1). The BCB shallow trench design provides a low capacitive isolation scheme while maintaining a planar surface. The self-aligned gate process reduces the parasitic source and drain resistances with the added benefit of reducing the footprint of the device. The non-alloyed tungsten ohmic contacts allow for well-defined contact geometries. The process architecture offers the promise of a reliable, highly manufacturable process needed to realize the complex circuits required for large-scale digital applications.

Long channel devices fabricated using the self-aligned process exhibit good DC characteristics (Figure 2). The source resistance (r_s) of the devices was estimated using TLM test structures to be on the order of 130 Ω. μm, an exceptionally low value. This is expected to be of most benefit when we transfer the process to deep submicron devices.



▲ Figure 1: (a) Cross-section of the proposed new device architecture. Features include BCB planar isolation, self-aligned gate and non-alloyed ohmic contacts. (b) The SEM cross-section of a typical device with a gate-to-source metallization distance of 100 nm.



▲ Figure 2: Output characteristics of a long channel device (~ 2.5 μm) fabricated using the self-aligned device architecture. The TLM test structures were used to estimate the source resistance, r_s at 130 Ω μm.

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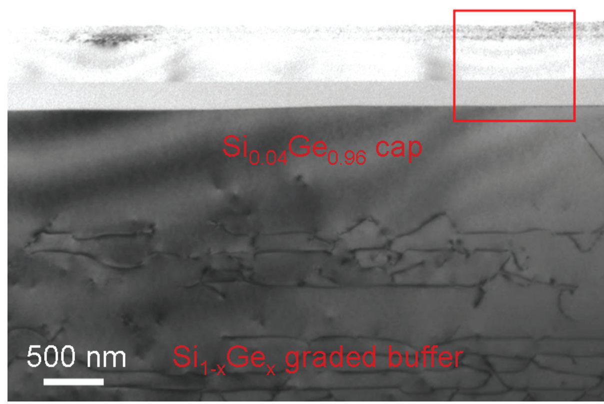
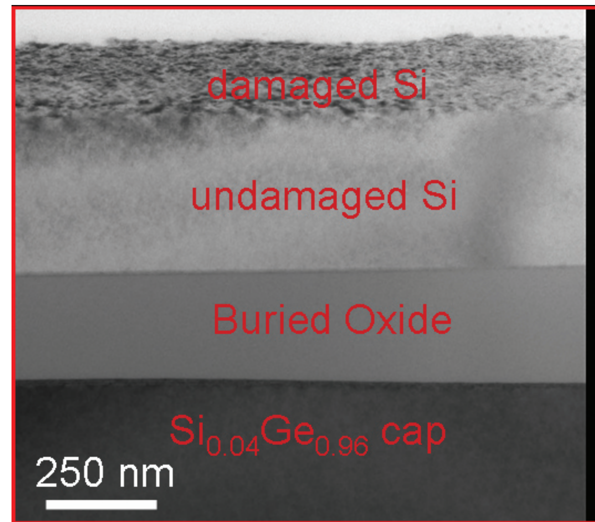
Fabrication of Silicon on Lattice-engineered Substrate (SOLES) as a Platform for Monolithic Integration of Si- and GaAs-based Devices

C.L. Dohrman, K. Chilukuri, D.M. Isaacson, M.L. Lee, E.A. Fitzgerald
Sponsorship: MARCO IFC, CMSE, MTL

We report the fabrication of a novel substrate platform for the monolithic integration of Si-based CMOS and GaAs-based optoelectronic devices. This platform, which we refer to as silicon on lattice-engineered substrate (SOLES), consists of a compositionally graded SiGe buffer buried underneath an SOI structure, all fabricated on a Si substrate. The SiGe graded buffer was grown by UHVCVD and was capped with a Ge-rich alloy that is closely lattice-matched to GaAs ($0.96 < x_{Ge} < 1$); it provides a threading dislocation density (TDD) of ~10^6 cm^{-2}. While previous studies have proved the SiGe graded buffer to be an effective platform for fabrication of GaAs-based LEDs, lasers, and solar cells on Si substrates, the large thickness (~10 μm) of the SiGe graded buffer hampers the integration of both Si- and GaAs-based devices on a single chip using this technique. The SOLES eliminates this drawback by the addition of the SOI structure on top of the Ge-rich cap. This approach provides a Si device layer in close proximity to the GaAs-based device layer, thereby simplifying the monolithic integration of Si- and GaAs-based devices with this platform. Fabrication consists of layer transfer of Si to an oxide-coated graded buffer using oxide-oxide wafer bonding followed by hydrogen-induced layer exfoliation of the Si layer from its donor wafer. The resulting structure was imaged with cross-sectional TEM and appears in Figure 1. Figure 2 (inset of Figure 1) reveals the SOI layer structure more clearly. Our results show that this layer transfer occurs reliably across the entire wafer, making it amenable to commercial applications.



▲ Figure 1: Transmission electron microscopy (TEM) image of SOLES platform. Misfit dislocations of the $Si_{1-x}Ge_x$ graded buffer appear at the bottom of the image. Figure 2 enlarges the red box inset in this image.



▲ Figure 2: Inset of Figure 1. This image illustrates the transferred layers. This image was taken before the removal of the exfoliation-damaged Si surface layer, and this damage is clearly seen here.

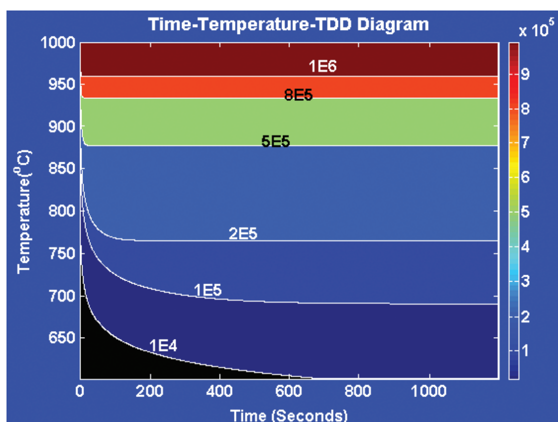
Thermally Relaxed, Ultra-thin, SiGe Buffers

S. Gupta, D.M. Isaacson, Y. Bai, E.A. Fitzgerald
Sponsorship: MARCO MSD

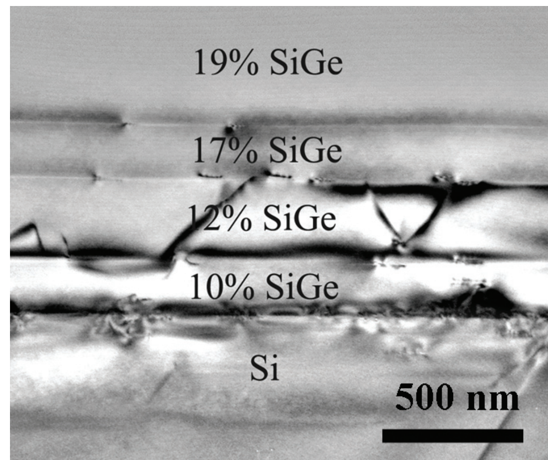
Producing relaxed, nearly defect-free SiGe alloys on Si substrates has been difficult due to the 4% lattice mismatch between Si and Ge. A relaxed $Si_{1-x}Ge_x$ graded buffer creates a larger lattice constant on a Si substrate while providing low threading dislocation densities (TDD) on the order of 10^5 cm^{-2}. Many other concepts for attaining relaxed $Si_{1-x}Ge_x$ buffers on Si wafers have been proposed over the years [1]. However, compositional grading remains the only established technique for attaining low-dislocation density, fully relaxed $Si_{1-x}Ge_x$ alloys on a Si substrate.

Two important variables that affect the dislocation density in a mismatched layer have been identified as the strain rate at which the layer is grown and the surface roughness of the layer. Reducing the TDD in a mismatched SiGe layer on Si requires low strain rates, which could be achieved by growing layers at slower growth rates. The traditional means to reduce the growth rate is to lower the growth temperature. Since the surface mobility of the atoms is reduced, the resulting layer has less surface roughness. However, since dislocation velocity is exponentially dependent on temperature, decreasing the growth temperature results in introduction of metastable strain, thus preventing complete relaxation of the strained layer. Therefore, achieving a completely relaxed, low-TDD layer requires the removal of the metastable strain without increasing the dislocation nucleation. While high temperature annealing is a way to reduce metastability, it also causes TDD escalation. A tool for estimating the TDD after an isothermal anneal has been developed for the first time in literature and is referred to as a TTTDD diagram (Figure 1).

One possible way to remove the metastability of this layer is by annealing or by depositing strained layers on top of the metastable layer and then subjecting it to anneals. The increased stress at the surface will increase the dislocation velocity for a given anneal temperature. We have demonstrated this technique with mismatched $Si_{0.90}Ge_{0.10}$ layers on Si. Complete relaxation and low TDD have been achieved as compared to films grown under high growth temperatures to achieve complete relaxation. Our results demonstrate that, for the 10% Ge layer used in these experiments, we can reduce the buffer thickness by a factor of 2.5 as compared to the conventional graded buffer. This development could prove very helpful in applications requiring extremely thick graded buffers, as is the case for Ge on Si.



▲ Figure 1: A TTTDD diagram for a metastable 10% layer.



▲ Figure 2: Thermally relaxed ultra-thin buffer. Thickness is about 2.5 times less than the conventional graded buffer.

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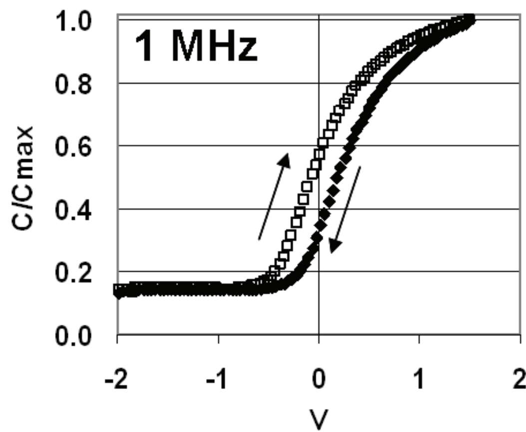
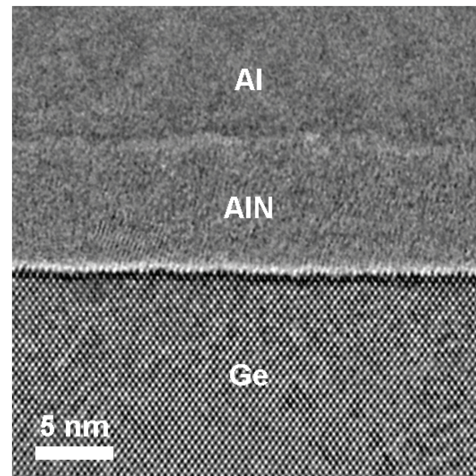
Microstructural and Electrical Characteristics of AlN Gate Dielectrics Deposited on Ge and GaAs Channels

M.L. Lee, A. Ritenour, D.A. Antoniadis, E.A. Fitzgerald
Sponsorship: MARCO MSD

We have fabricated metal-insulator-semiconductor capacitors on both Ge and GaAs channels with an Al/AlN gate stack. The capacitors possess an EOT of 2-4 nm and exhibit clean accumulation with low hysteresis and little frequency dispersion (Figure 1). The AlN dielectric is deposited by low-pressure metal-organic chemical vapor deposition, and the Al gate is deposited by physical vapor deposition. High-resolution transmission electron microscopy studies on the finished devices reveal that the AlN is amorphous or nanocrystalline or both (Figure 2), and correlation of the physical thickness with capacitor data indicates a dielectric constant of approximately 10. The AlN is grown with standard metal-organic precursors in an epitaxial growth reactor; we can therefore deposit both the high-mobility channel and the dielectric *in situ* without exposure to ambient air. We believe that AlN and other wide-bandgap III-N layers are particularly well-suited for III-V channels, since they enable us to eliminate the unintentional formation of native oxides at the insulator/semiconductor interface.



▲ Figure 1: High-frequency C-V measurements of Al/AlN gate stack deposited onto n-Ge.

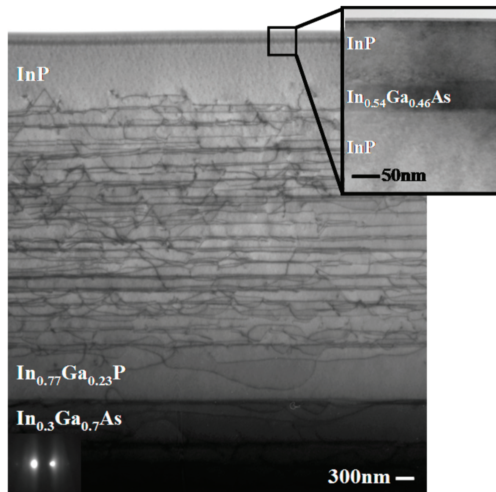


▲ Figure 2: HRTEM image of Al/AlN//Ge capacitor structure.

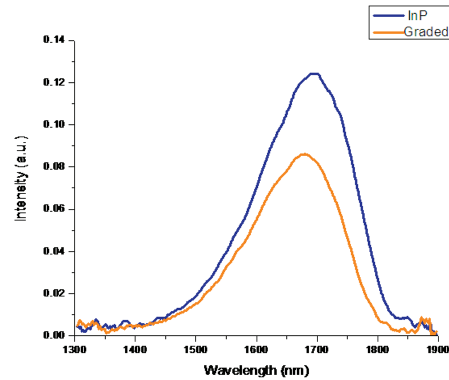
High-Quality InP-on-GaAs using Graded Buffers Grown by Metal Organic Vapor Phase Epitaxy (MOVPE)

N. Quitoriano, E.A. Fitzgerald
Sponsorship: ARO, MARCO MSD

In addition to traditional telecom applications, devices based on InP have received increased attention for high-performance electronics. The InP growth on GaAs is motivated by the facts that InP wafers are smaller and more expensive and they utilize older fabrication equipment than GaAs. Creating high-quality InP-on-GaAs-bulk substrates has proven challenging, however. While a number of commercial growth foundries offer InP-on-GaAs for M-HEMT (Metamorphic High-Electron-Mobility Transistor) applications, the successful demonstration of InP-based, minority-carrier devices on bulk GaAs remains elusive. We demonstrate InP-on-GaAs suitable for minority carrier devices, exhibiting a threading dislocation density of $1.2 \times 10^6/cm^2$ determined by plan-view transmission electron microscopy (see Figure 1, the cross-sectional TEM). This material exhibited nearly equivalent PL data compared to one on bulk InP at room temperature (see Figure 2). To achieve this result, we explored the InGaAs, InGaP, InAlAs and InGaAlAs materials systems. In each of these systems, we found that microscopic compositional inhomogeneities along the growth direction blocked dislocations leading to dislocation densities as high as $10^9/cm^2$. Using scanning-transmission electron microscopy, we determined that surface-driven phase separation leading to Ga-rich regions caused the composition variations. Conditions for avoiding phase separation were identified and explored. We found that we could prevent composition variations in $In_xGa_{1-x}As$ graded buffers grown at 750ºC to yield low dislocation densities of $1.5x10^6/cm^2$ for x<0.34, accommodating ~70% of the lattice mismatch between GaAs and InP. However, further grading to 53% In is required to attain the lattice constant of InP. We have found that compositional grading in $In_yGa_{1-y}P$ (0.8<y<1.0) can accommodate the remaining lattice mismatch with no rise in thread density while avoiding phase separation. Consequently, to achieve high-quality InP-on-GaAs, we started with the InGaAs material system and then completed the graded buffer in the InGaP system to reach InP.



▲ Figure 1: Cross-sectional bright-field TEM micrograph of high-quality InP-on-GaAs. The enlarged top portion highlights the PL structure.

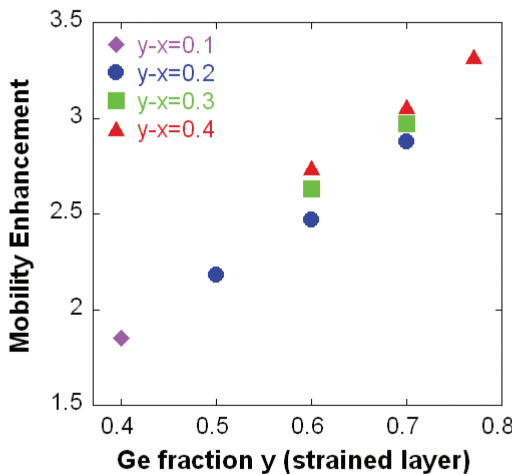


▲ Figure 2: Room temperature PL data from the same PL structure on bulk InP (denoted "InP") and on our graded structure (denoted "Graded," see Figure 1). The graded structure PL integrated intensity is about 70% of the bulk. Since this percentage is the same at 20K, we believe that the reduction in intensity is not due to defects, rather light the laser is penetrating into the graded buffer where the generated carriers recombine.

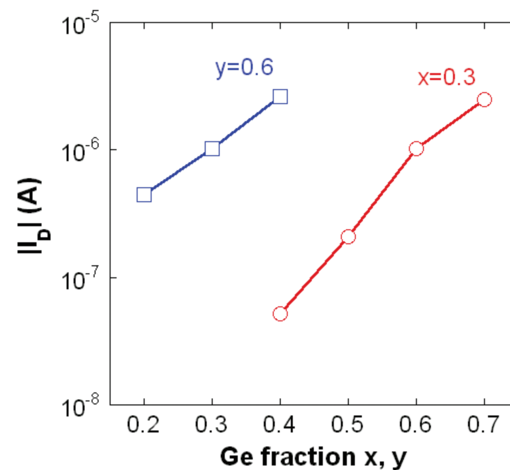
Hole Mobility in High-Ge-content, Strained SiGe-Channel MOSFETs

C. Ní Chléirigh, O.O. Olubuyide, J.L. Hoyt
Sponsorship: SRC, MARCO MSD, Applied Materials

This work presents, for the first time, a comprehensive study of mobility, sub-threshold slope, and off-state leakage current in high-Ge-content, dual-channel strained Si/strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ p-MOSFETs. Hole mobility enhancements of 3X are observed at high inversion charge densities ($N_{inv}=10^{13}$ cm^{-2}) for the strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.7}Ge_{0.3}$ (70/30) structure with 2-nm-thick cap and 3-nm-thick gate oxide. A wide range of Ge fractions and Si cap thicknesses is studied. The Ge fraction in the strained $Si_{1-y}Ge_y$ layer dominates the mobility enhancement, while the level of strain is a second order effect (Figure 1). The off-state drain leakage is studied in detail. At low drain-to-gate bias (VDG), off-state leakage is attributed to a trap-assisted tunneling (TAT) mechanism at the Si surface and is sensitive to the thickness of the Si-cap layer. At high VDG, the leakage increases with the Ge fraction in the strained $Si_{1-y}Ge_y$ and strain in the Si cap layer, consistent with band-to-band tunneling (BTBT) (Figure 2) [1]. The data illustrates trade-offs critical for optimizing the structures with respect to mobility, charge control, and leakage. The results of this work can be used to examine the design space for high-mobility p-MOSFETs. Increasing the Ge content in the SiGe channel increases mobility at the expense of off-state leakage. To minimize sub-threshold swing and increase high-field hole mobility, the Si cap must be as thin as possible. The bandgap and thickness of both the strained Si and strained $Si_{1-y}Ge_y$ layers are critical in determining off-state leakage and must be taken into account when optimizing the heterostructure and drain-region design.



▲ Figure 1: Mobility enhancement factor (referenced to Si control device) at N_{inv} of 10^{13} cm^{-2} versus Ge fraction in the strained layer for various levels of strain (y-x). Data from thin Si cap structures is shown (T_{Si}=2 – 4 nm).



▲ Figure 2: Drain current, I_D at VDG=2 V with VG=0 V for W=1000 µm, L=50 µm p-MOSFET. The Ge fraction in the substrate, x, (and hence the bandgap of the strained Si layer) is varied and Ge in strained layer is fixed at y=0.6 (squares). The Ge fraction in the strained layer, y, is varied on x=0.3 substrate (circles).

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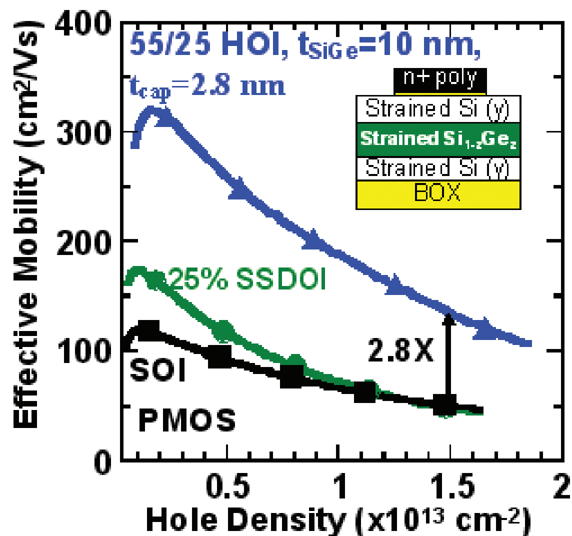
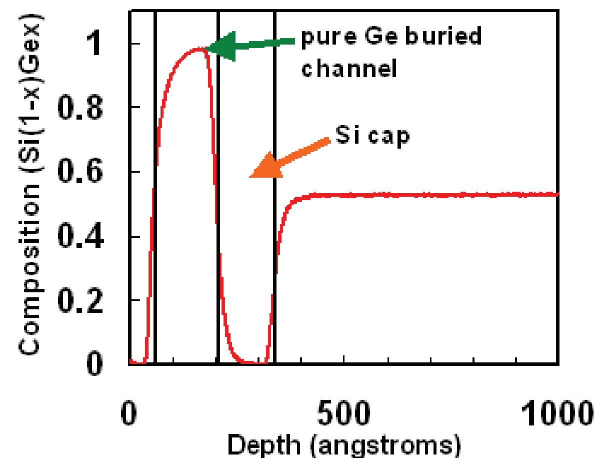
Strained Si/Strained Ge Heterostructure-on-Insulator

L. Gomez, M.K. Kim, C. Ní Chléirigh, I. Åberg, J.L. Hoyt
Sponsorship: MARCO MSD, Applied Materials

Scaling of device dimensions can no longer provide the necessary current drive enhancements to continue historic performance gains. Strain and novel channel materials can provide enhanced transport characteristics to increase device performance. Thin-body devices also provide the benefit of improved electrostatic control in deeply scaled MOSFETs. In previous work, thin-body MOSFETs were fabricated on strained Si/strained SiGe heterostructure on insulator (HOI) to realize enhanced transport for electrons and holes and improved subthreshold characteristics [1]. The HOI material was fabricated in MTL by epitaxial growth and transfer of the strained layers. Sub-threshold swing was observed to be 66-70 mV/dec, improved compared to similar heterostructure-on-bulk devices. Mobility enhancements of 1.9x and 2.8x were observed for electrons and holes, respectively, at an inversion charge density of 1.5 x 10^{13}. Figure 1 illustrates measured hole mobility for HOI MOSFETs with 55% Ge in the SiGe channel. With the potential to observe even higher hole mobility enhancement, with higher levels of strain and Ge content in the SiGe channel, we are developing pure Ge heterostructure-on-insulator. For heterostructure-on-bulk MOSFETs, Ge channels strained to a $Si_{0.5}Ge_{0.5}$ substrate have exhibited enhancement factors of 10x for holes [2]. In the present work, a process was developed to grow thin strained Ge on strained Si (strained to a SiGe substrate with 50% Ge). Figure 2 shows a secondary ion-mass spectrometry (SIMS) profile of the as-grown structure, prior to bond-and-etch-back. A low-temperature bond and etch back process has been developed for strained layer transfer. A low temperature process is critical to minimize both Ge diffusion and strain relaxation.



▲ Figure 1: Measured PMOS effective hole mobility for strained Si directly on insulator (25% SSDOI) and HOI with 55% Ge in the SiGe channel. The SSDOI and HOI materials were grown strained to SiGe virtual substrates with Ge contents of 25%, prior to layer transfer to form the on-insulator substrates. Total body thickness is approximately 17 nm.



▲ Figure 2: SIMS profile of top 1000A of the as-grown Ge HOI structure, prior to bond and etch-back. The complete tri-layer structure can be observed in the SIMS profile. It consists of a 134A Si cap, a 147A Ge buried layer, and an underlying 55A Si layer. Lines are drawn to guide the eye.

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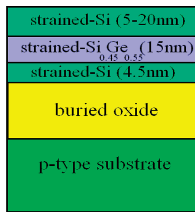
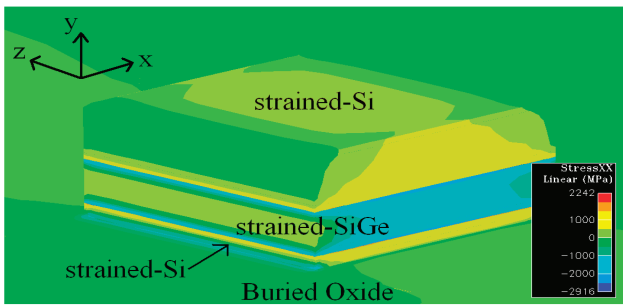
Patterning-induced Strain Changes in Strained Si/Strained SiGe Heterostructures

P. Hashemi, L. Gomez, J.L. Hoyt
Sponsorship: MARCO MSD

Multi-gate silicon-on-insulator (SOI) structures such as FinFETs are one of the promising candidates for deep sub-tenth-micron MOSFET technology due to their enhanced electrostatic control, which is particularly beneficial beyond 50-nm gate-lengths. On the other hand, strain engineering has been an effective means to increase device performance. Partial relaxation has recently been observed when patterning strained-silicon directly on insulator (SSDSOI) structures [1]. High-mobility strained-SiGeOI FinFETs that take advantage of stress-induced performance and immunity to the short-channel effects have also been reported [2]. In this work, we study the pattern-induced stress changes in strained Si/strained SiGe heterostructures on insulator (HOI). The goal is to engineer structures for fabrication of HOI multi-gate MOSFETs. The cross-sectional image of the HOI structure is schematically shown in Figure 1. A bond and etch-back technique is used to fabricate strained HOI substrates. The stress contours of 100-nm-square patterned HOI, simulated using Taurus™ 3D, are also shown in this figure. To engineer the stress in the channel for optimal HOI multi-gate MOSFET design, the effects of several parameters such as fin width, layer thicknesses and aspect ratios were analyzed. For example, the dependence of the average stress components on the fin width of the long-bar patterned HOI in (a) the Si-cap and (b) the SiGe layer (for nominal HOI parameters) are shown in Figure 2. As can be seen, σ_{xx} stress component is almost relaxed in deep-submicron fins where σ_{zz} is nearly maintained. To realize the fins under study, e-beam lithography will be utilized. Raman analysis will be used to verify the stress dependencies on geometry.

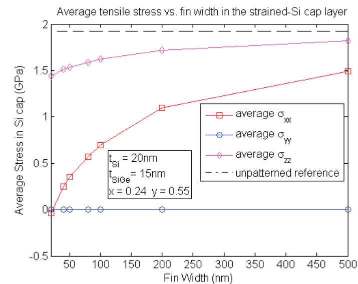


(a)

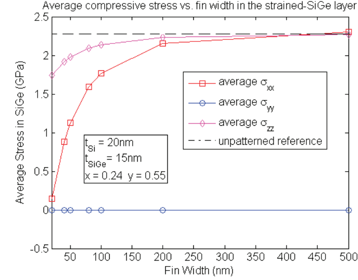


(b)

▲ Figure 1: (a) Schematic cross-sectional image of the biaxially-strained Si/SiGe/Si heterostructure on insulator and (b) the stress (σ_{xx}) contours of the 100 nm×100 nm patterned heterostructure indicating partially strain relaxation in the associated layers.



(a)



(b)

▲ Figure 2: Variation of the average stress components versus the fin width of the long-bar patterned heterostructures in (a) the Si-cap and (b) the SiGe layers.

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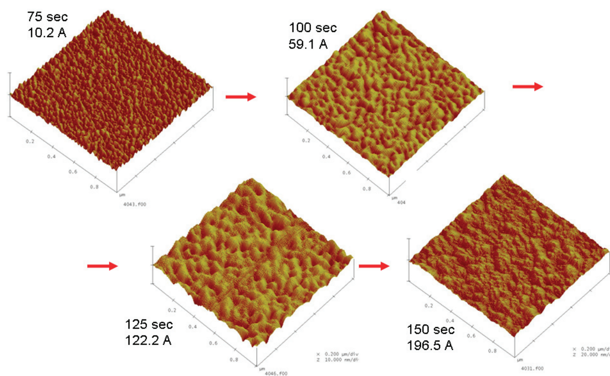
The Initial Stages of Ge-on-Si and Ge-on-SiGe Epitaxial Growth

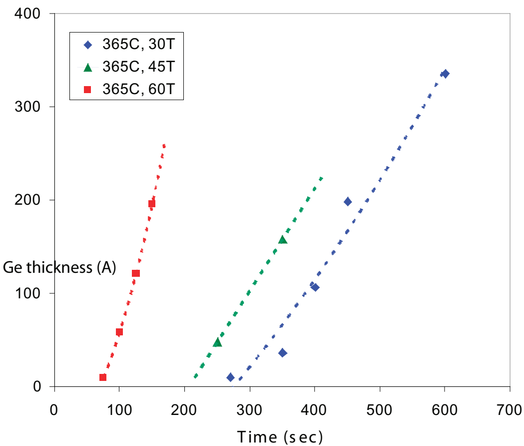
M. Kim, O.O. Olubuyide, L. Gomez, J.L. Hoyt
Sponsorship: DARPA, NSF Graduate Research Fellowship

Growing multilayer structures of Ge and SiGe on Si wafers has several applications to emerging technologies: thick, relaxed Ge films can be grown on a silicon substrate to make CMOS-compatible photodetectors, and thin, strained Ge and SiGe layers are used for enhanced-mobility heterostructure-on-insulator (HOI) MOSFETs. For all applications, it is desirable to grow flat, uniform films with minimal crystal defect density. Past work indicates that smooth, low- temperature Ge films with thickness of 30 to 60 nm can be grown in an LPCVD system [1]; however, the initial stages of Ge-on-Si and Ge-on-SiGe expitaxial growth with film thickness less than 10 nm has is not fully understood. In this project, we explore the morphology and growth rate for both strained and relaxed Ge films on Si and SiGe substrates.

Due to the 4% mismatch in lattice size, Ge on Si substrates show a 3-D growth mode, in which Ge initially forms islands and then coalesces to form a more uniform surface (Figure 1). The growth rate is non-linear during these initial stages. There appears to be an incubation period that depends on the growth parameters (Figure 2). Our findings show that the growth rate for Ge on Si (strained or unstrained) is slower than that of Ge on SiGe. For relaxed Ge on SiGe growth, the Ge film is smoother and growth rate is faster as the Ge content increases.



▲ Figure 1: 1 µm x 1 µm AFM scans of thin Ge films grown on Si substrates, showing the initial stages of Ge epitaxial growth. As the Ge layer gets thicker, the initial islanded morphology changes into a more uniform surface.



▲ Figure 2: The Ge thickness as a function of growth time. The graph suggests that there might be some incubation period for the initial Ge growth. Hydrogen flow for the 30T and 45T samples was 5 slpm to the slit valve and 0 slpm to the top inject. For the 60T sample, the H_2 flow was adjusted to be 5 slpm for both the slit and the top inject.

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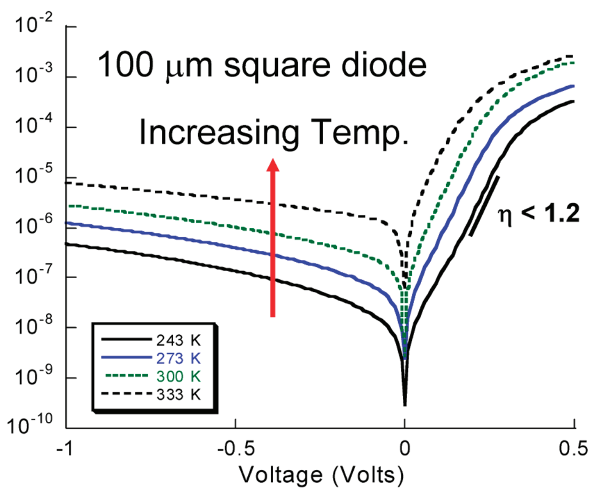
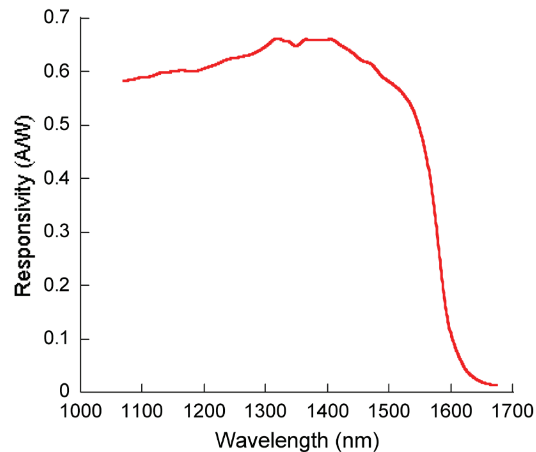
CMOS-compatible Epitaxial LPCVD Ge-on-Si Photodiodes

O.O. Olubuyide, M. Kim, J. Yasaitis, J. Michel, J. Liu, L.C. Kimerling, J.L. Hoyt
Sponsorship: Analog Devices, IBM, SRC

Germanium films have the required responsivity and speed to serve as photodetectors at the 1.55-µm wavelength range. Such detectors can be used in the communications field in a variety of high-speed systems, such as optical samplers. Therefore, integrating Ge films grown on silicon (Ge-on-Si) substrates into a CMOS-compatible process is an attractive goal for making arrays of on-chip detectors for use in a range of electronic and photonic integrated circuit applications. This study explores the growth properties and material quality of Ge-on-Si deposited by low pressure chemical vapor deposition (LPCVD) in an Applied Materials Epitaxial Reactor and the optical and electrical properties of Ge-on-Si photodiodes. It has already been demonstrated in ultra high vacuum chemical vapor deposition (UHVCVD) systems that depositing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature layer (cap layer) with subsequent annealing can create a smooth, planar Ge film on a (100) silicon substrate with threading dislocation density on the order of 10^7 cm^{-2} [1]. We have adapted this two-step deposition process to an LPCVD system. We have explored the effect of growth pressure, temperature, and seed thickness on the material quality for blanket and selective epitaxial growth (SEG) of germanium. Our research identifies an optimum Ge seed layer deposition process window of 335ºC ± 15ºC and 30 T ± 10 T and demonstrates the requirement for a seed layer thickness above 30 nm. For SEG Ge-on-Si, a cap deposition condition of 600ºC and 10 Torr appear to significantly reduce germanium nucleation on oxide films. After annealing at 900ºC for 30 minutes, these blanket and selective Ge films have threading dislocation densities of $\leq 2 \times 10^7$ cm^{-2}. Photodiodes fabricated with the blanket Ge films have been measured to have a reverse leakage current less than 10 mA/cm^2 at a −1 volt bias (Figure 1), a 3-dB frequency response of 1.5 GHz for 40 x 100 µm rectangular diodes, and a responsivity of 0.5 A/W at 1.55 µm wavelength (Figure 2).



▲ Figure 1: Temperature-dependent IV curves between 243 – 333 K for a 100-µm square pin diode fabricated with a blanket Ge-on-Si film. The ideality factor is less than 1.2 for temperatures at or below 300 K. The perimeter-dominated leakage current increases with temperature, indicating a trap-mediated generation process.



▲ Figure 2: Responsivity as a function of wavelength for a 100-µm square *pin* diode fabricated with a blanket Ge-on-Si film. The responsivity is measured at a reverse bias of –1 volt, and an associated perimeter-dominated reverse-leakage current of 1.6 µA. The responsivity is 0.5 A/W at a wavelength of 1.55 µm.

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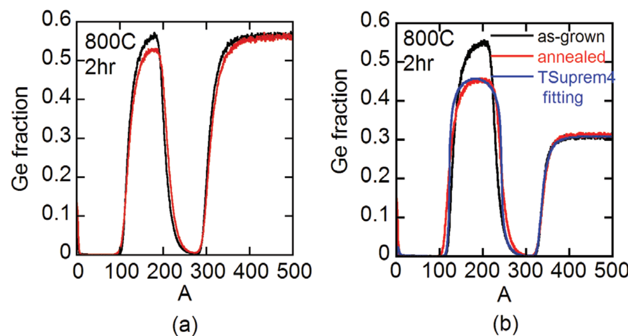
Interdiffusion in SiGe/Si Epitaxial Heterostructures

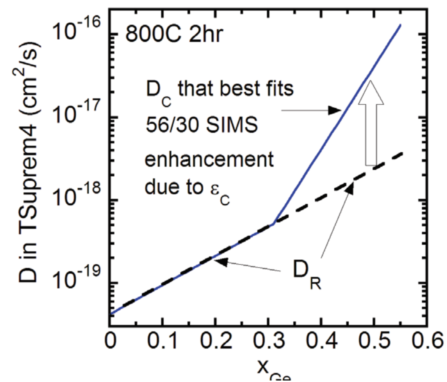
G. Xia, J.L. Hoyt
Sponsorship: MARCO MSD

In the past decade, SiGe-based strain and bandgap engineering have received increasing attention for CMOS applications. Carrier transport is enhanced by applying strain in the Si channel or by the use of strained SiGe or strained Ge as the p-MOSFET channel material, as in dual-channel, heterostructure-on-insulator (HOI), and heterostructure double-gate MOSFETs. One issue for these structures is interdiffusion at the Si/SiGe or Si/Ge interface during processing, which degrades device performance by reducing strain and carrier confinement and increasing alloy scattering. To date, research on Ge diffusion has been focused on Ge self-diffusion in $Si_{1-x}Ge_x$ [1] and interdiffusion in compressively strained SiGe superlattices with low Ge fractions (x < 0.25) grown on Si [2]. Basic understanding of interdiffusion, such as Ge fraction, strain, and temperature dependence, and interdiffusion modeling, is inadequate. In addition, little data is available for SiGe interdiffusion in device structures, such as strained Si/ strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ with Ge content y>0.3.

In this work, we studied interdiffusion in pseudomorphic strained Si/$Si_{1-y}Ge_y$/strained Si/relaxed $Si_{1-x}Ge_x$ structures to emulate the interdiffusion in HOI devices. Boltzmann-Matano analysis is used to extract SiGe interdiffusivity experimentally from SIMS profiles of strained Si/relaxed $Si_{1-x}Ge_x$ structures. The TSuprem-4 simulations are then used to refine the interdiffusivity data. The Si-Ge interdiffusivity for strained Si/relaxed SiGe (D_R) was found to increase by 2.2 x for every 10% increase in local Ge fraction. We observed significantly enhanced Si-Ge interdiffusion in $Si_{1-y}Ge_y$ layers under compressive strain, as seen in Figure 1 [3]. A piece-wise exponential model was used in TSuprem-4 to extract interdiffusivity under compressive strain in the $Si_{1-y}Ge_y$ (D_C). The interdiffusivity was found to increase by 4.4 x for every 0.42% increase in compressive strain, which is equivalent to a 10% decrease in the substrate Ge fraction. These results were incorporated into an interdiffusion model that successfully predicts experimental diffusion profiles for various SiGe heterostructures.



▲ Figure 1: As-grown and annealed Ge profiles measured by SIMS for two strained Si/$Si_{1-y}Ge_y$/strained Si/relaxed $Si_{1-x}Ge_x$ structures. (a) y=0.56 x=0.56 and (b) y=0.56 x=0.30. Significantly enhanced interdiffusion is observed under compressive strain as seen in (b). The TSuprem-4 simulation is also shown in (b). The interdiffusivity model used in TSuprem-4 for this fit is shown in Figure 2 as the solid line.



▲ Figure 2: Piece-wise exponential interdiffusivity (solid blue line) extracted by fitting annealed SIMS profile in Figure 1 (b). For x_{Ge} <0.3, D = D_R (dashed black line), while for x_{Ge} >0.3, D = D_C.

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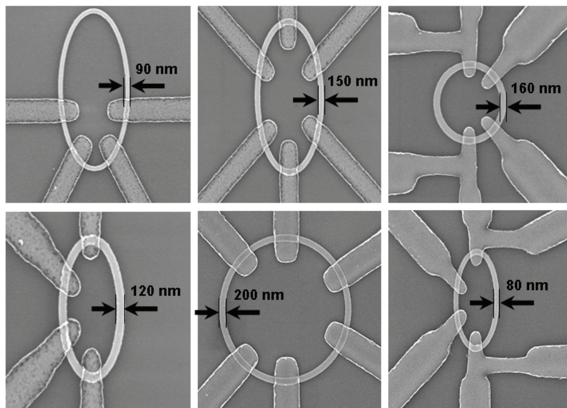
Magnetic Rings for Memory and Logic Devices

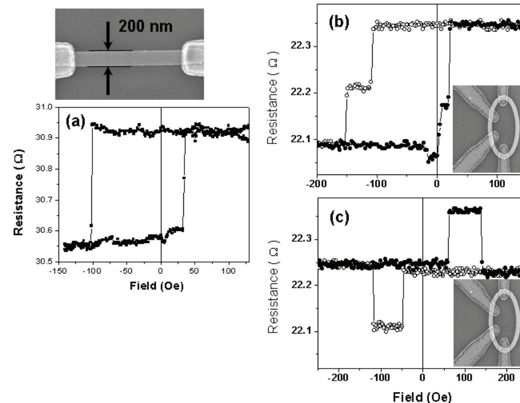
F.J. Castaño, D. Morecroft, W. Jung, J.D. Suh, C.A. Ross
Sponsorship: Cambridge-MIT Institute, Singapore-MIT Alliance, Outgoing Marie Curie Fellowship, NSF

We use fabrication processes combining electron-beam lithography and photo-lithography to create prototypes for magneto-electronic devices based on small ring- and bar-shaped multilayered magnetic elements with widths in the deep-sub-micron regime. These small structures have potential uses in magnetic-random-access memories (MRAM), magnetic logic devices, and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multilayered magnets, containing two magnetic layers separated by a thin layer of either a non-magnetic metal (spin-valves) or an isolator (magnetic tunneling junctions). The resistance of such elements depends on the relative orientation (parallel or anti-parallel) between the magnetization in the read-out (free) and storage (pinned) layers. On switching back and forth the magnetization direction of the free layer two different resistance levels can be detected, allowing for a non-volatile bit of data ("0" or "1") to be stored in each element. As an alternative bit shape, MRAMs based on ring-shaped multilayered magnets have been recently proposed due to their robust magnetization reversal and the existence of flux-closure or "vortex" states.

We recently fabricated ring devices made from NiFe/Cu/Co/Au pseudo-spin-valves (PSVs) with non-magnetic contact-wires (see Figure 1). In these structures magneto-transport behavior is dominated by giant magnetoresistance (GMR). While the resistance of a PSV bar-shape element displays two resistance levels on cycling the free (NiFe) layer (Figure 2a), the rings display additional intermediate resistance levels [1] reached through abrupt transitions (Figure 2b). Additionally, the storage (Co) layer can be cycled into different states [1], allowing for profoundly different device responses on switching the free layer (Figure 2c). We have explored the switching mechanisms of PSV ring structures using micromagnetic simulations, as well as the effect of the contact configuration on the device response [2]. The sharp, low-field resistance changes in these PSV rings, which can be tailored by choice of ring dimensions and multilayer stack, will make them attractive for magnetoelectronic applications such as memories or logic devices that require multiple stable resistance levels. Most recently we are pursuing operating these devices using current pulses, rather than with an applied magnetic field.



▲ Figure 1: Scanning electron micrographs corresponding to elliptical and circular ring devices made from NiFe/Cu/Co/Au multilayers and Ta/Cu non-magnetic contact wires. The outer dimensions of the rings ranges from 930 nm to 20 µm and the widths from 80 nm to 350 nm.



▲ Figure 2: (a) Resistance versus applied field measurements on switching the free (NiFe) layer of a 200-nm-wide NiFe (6 nm)/Cu (5 nm)/Co (6 nm)/Au (4 nm) bar-shaped device. (b-c) resistance versus applied field corresponding to a 120-nm-wide NiFe (4 nm)/Cu (6 nm)/Co (8 nm)/Au (4 nm) elliptical ring, on switching the free layer with the storage layer in different states.

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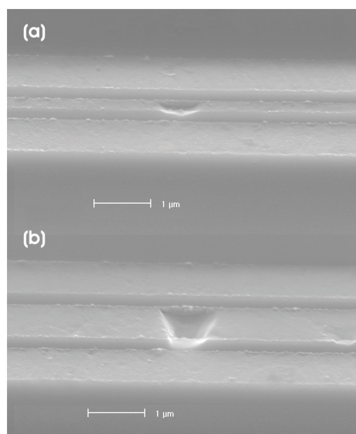
Surface Electromigration and Void Dynamics in Copper Interconnects

Z.S. Choi, R. Moenig, C.V. Thompson
Sponsorship: Intel, AMD, SRC

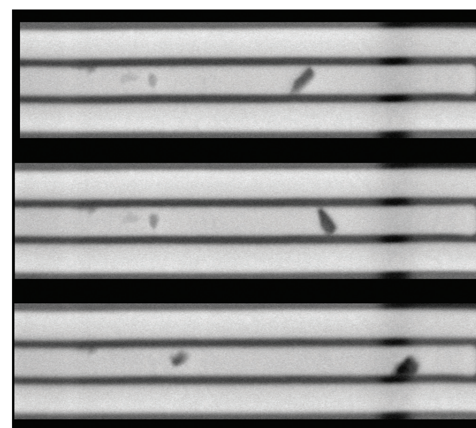
Electromigration is one of the main causes of failures in interconnects [1]. It has been shown that the dominant diffusion path in copper interconnect technology is the interface between the dielectric passivation layer and the copper line [2]. This interface is also the most prone to void nucleation and growth. The dynamics of these processes are critical since voids are the main cause of electrical failure of interconnects. We are carrying out two sets of experiments to investigate the details of void dynamics.

The first type of experiment is performed on interconnects without passivation layers to determine the dependence of copper surface diffusion and electromigration on different grain orientations. The samples are heated in reducing gas to remove copper oxide and then tested in a vacuum ($<10^{-7}$torr). The voids in these samples nucleate and grow at flux divergence sites (Figure 1). The flux divergences occur due to the differences in diffusivity for different grain orientations. After the electromigration tests, we obtain the crystallographic orientations of the grains surrounding the voids using electron backscattered diffraction (EBSD) in an SEM and correlate the results with differences in diffusivities between different grains.

In a second type of experiment, we take a fully fabricated sample and thin the passivation layer using a focused ion beam microscope (FIB), in order to be able to observe the underlying metal line in an SEM. We then test the samples at elevated temperatures in the SEM and observe the voids in the interconnects through the thinned passivation layer in real time, as Figure 2 shows. After the test, we remove the passivation layer and determine the effect of the grain orientations on void nucleation, growth, and motion. These experiments yield detailed information about the dynamics of voids in interconnects. The results can help to improve reliability analysis and design of interconnects.



▲ Figure 1: Voids in interconnects with no dielectric passivation layer, interconnects with length of1000 µm, depth of 0.45 µm, widths of a) 0.3 µm and b) 1.0 µm.



▲ Figure 2: *In situ* SEM images of the cathode of a test structure, showing void drift toward cathode end. The test line is surrounded by a Cu-extrusion monitor.

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Bonded Copper Interconnects and Integrated Microchannels for 3D Integrated Circuits

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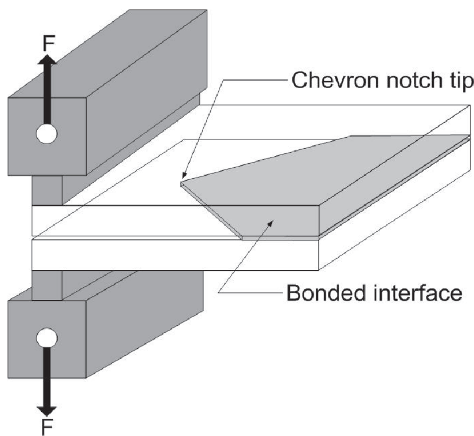
Sponsorship: DARPA (3D Integrated Circuits), Singapore-MIT Alliance, IME

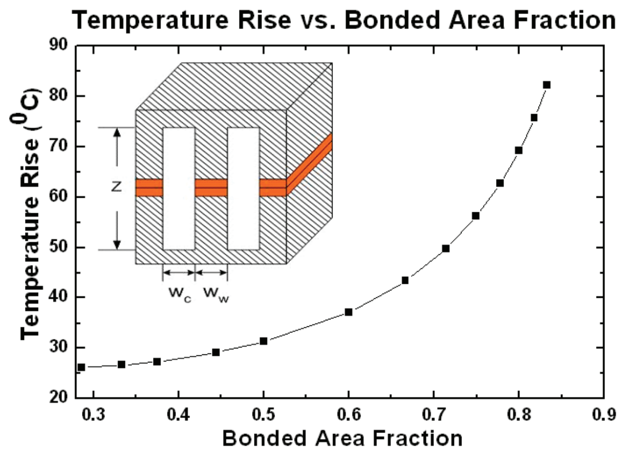
Performance of thermocompression Cu-Cu bonds is critical to reliability of devices created by stacking of individual wafers. Thermal effects in such 3D circuits are expected to be severe compared to conventional devices, owing to multiple heat generation locations and limited heat dissipation pathways. Bond quality and thermal performance issues in Cu wafer bonding technology are investigated using both experiments and modeling.

A novel test method (Chevron test) has been developed to complement the conventional four-point bend test, for bond toughness measurements. The Chevron test is used to measure Mode I (Tensile) toughness of Cu bonds (Figure 1). Nominal toughness values for Cu bonds created at 300°C as measured by Chevron and Four-point bend tests are 2.5 J/m^2 and 17 J/m^2, respectively, the difference attributed to plastic deformation of the Cu stack [1]. Therefore, the Chevron test gives a measure of the true interface strength, minus external contributions. The fundamental limit of Cu adhesion is probed using a UHV-AFM/deposition system. Force of adhesion between pristine oxide-free Cu surfaces deposited on a cantilever tip and a substrate is measured under UHV conditions. The room-temperature bond strength measured in the AFM set-up is comparable to 300°C wafer-level bond strength, thereby showing a significant dependence of bond quality on Cu surface cleanliness. Effects of process and film parameters on ultimate bond quality are being analyzed using bonded ECP damascene-patterned Cu interconnects (NTU, Singapore). Results indicate a strong dependence of bonded die yield on Cu film roughness and applied bonding load. An analytical model is being developed to explain these findings.

One solution to the heat dissipation problem in 3D circuits is integration of microchannels for microfluidic cooling in the 3D stack, using Cu-Cu bonds for channel sealing (Figure 2). The trade-off between cooling and bond strength has been analyzed to find optimum channel dimensions as a function of the achievable Cu-Cu bond strength.



▲ Figure 1: Schematic of Chevron test structure. Triangle-shaped bonded interface enables crack initiation at the notch tip.



▲ Figure 2: Temperature rise as a function of bonded area fraction for microchannel cooling. Lower bonded area fractions lead to increased channel density, and therefore, lower temperature rise. However, bond integrity is compromised at low bonded area fractions.

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