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massachusetts institute of technology

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September 2006

MTL Annual Research Report September 2006

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INTRODUCTION

Martin A. Schmidt
Director, MTL

Welcome to the 2006 MTL Annual Report. This report contains research abstracts from faculty and senior research staff whom are associated with the MTL. The work spans a broad range of topics from Circuits and Integrated Systems to Molecular and Nanotechnology. These investigators come from more than 30 different departments, labs, and centers across the Institute.

Last year we introduced a new format to the Annual Report, and we continue that format this year. As with last year, the entire content of the Annual Report is available from the MTL web site at http://mtlweb.mit.edu. This site also includes links to more detailed content.

The MTL Mission states that we are an Interdepartmental Laboratory that encompasses research and education with an intellectual core of i) Semiconductor Process and Device Technology, and ii) Integrated Circuits and Systems Design. MTL fosters new initiatives in Microsystems at the Institute. MTL provides Microsystems infrastructure to the Institute.

Organizationally, MTL supports this mission by focusing on two major goals; maintaining and supporting a core research community which is aligned with our research mission, and managing a set of shared experimental facilities which support of the core research community as well as the broader campus community. In addition, MTL maintains a strong relationship to industry through a portfolio of relationship options.

The core research community is comprised of approximately 20 faculty and senior research staff that do research in areas of integrated circuits and systems, nanoelectronics, photonics, MEMS, and molecular and nanotechnology. These faculty are closely aligned to the industries which commercialize this research. The community is maintained through a collection of activities including seminars, committees and an annual research conference attended by approximately 150 persons.

The shared experimental facilities are comprised of three different clean-rooms which support micro and nano fabrication technologies from advanced silicon processing, to a diverse range of materials. These three facilities are centrally managed by a professional staff of 16 engineers and technicians. In addition to the fabrication facilities, the MTL also maintains computer infrastructure for CAD as well as testing equipment. More details on the facilities are provided later in this report as well as on the MTL web site.

MTL has a portfolio of industrial engagements from major alliances to individual research grants. The flagship relationship is the Microsystems Industrial Group (MIG) which is a consortium relationship which provides members with priority access to the students and research output of the lab. In addition, four industrial research centers with more focused interests are associated with the MTL; Center for Integrated Circuits and Systems (CICS), Intelligent Transportation Research Center (ITRC), MEMS@MIT, and the Center for Integrated Photonic Systems (CIPS).

ACKNOWLEDGEMENTS

We are grateful to the following organizations for their generosity and participation in the Microsystems Industrial Group (MIG). Their membership makes possible the continuing operations of the Microsystems Technology Laboratories:

- AMD
- Analog Devices
- Applied Materials
- Hewlett-Packard
- IBM Corporation
- Intel Corporation
- National Semiconductor
- Novellus Systems, Incorporated
- Samsung
- Texas Instruments, Inc.

We would also like to acknowledge past support of the Microsystems Technology Laboratories by the following organizations:

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We also wish to acknowledge the support of those organizations who have generously contributed equipment for use at the Microsystems Technology Laboratories:

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Analog Devices
Applied Materials
Compaq Computer Corporation
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University of Illinois at Urbana-Champaign
Whitaker Foundation

RESEARCH THEMES

The research in MTL spans an extraordinarily broad set of activities. If one were to identify a unifying theme associated with these projects, it would be the system-level interest in micro and nano technology. The MTL represents a community which brings experimentalist skilled in materials and technology at the micro and nano-levels together with circuits/systems researchers to realize visions for new systems which are enabled by the integration of these disciplines.

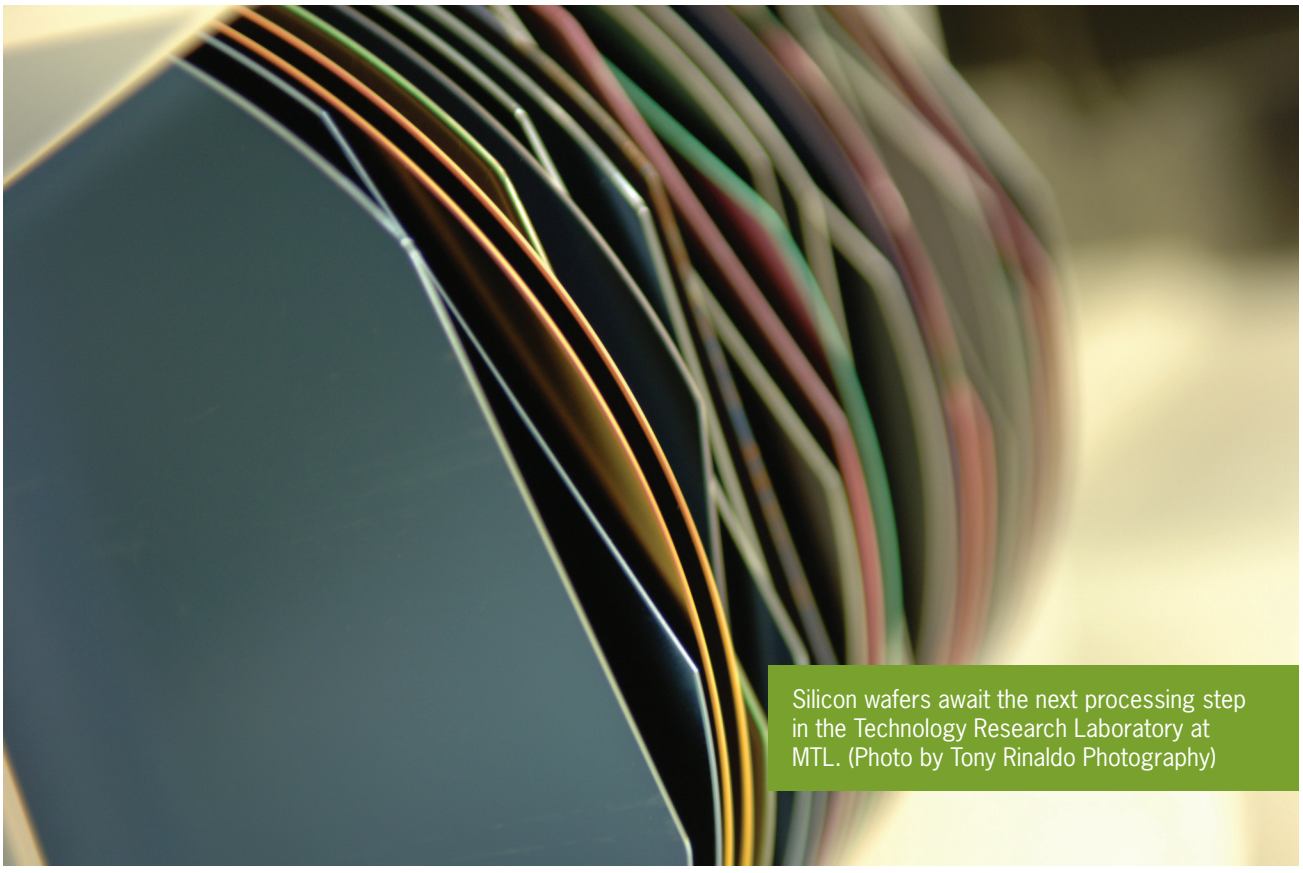
In the past year, the circuits and systems group engaged in research in the areas of RF design, including receivers, modulators and power devices. Wireless systems remained a major focus area in both the high performance and ultra-low power domains. The high performance wireless research was primarily directed towards gigabit LAN, whereas the low power systems were in support of wireless sensor networks primarily. This coupled to an extensive range of research on low-power design in general. Analog to digital conversion and mixed signal circuit design continue to be a major focus area. A new 'comparator-based' circuit architecture was introduced this year. Intelligent transportation systems, and vision systems in support of these were studied. As part of a larger overall effort on interconnect issues, there was considerable work on circuit/systems issues in interconnect and the investigation of 3D systems. Analysis tools for design of circuits and test devices to understand manufacturing issues provided core underpinning research for the entire circuits and systems area.

A wide range of electronic devices were explored and are reported in detail in our Annual Report. 'Substrate engineering,' or the development of optimized silicon-based hetero-structures, was a substantial activity, as was the exploration of novel means to achieve device isolation in integrated systems. Compound semiconductor systems such as InP/GaAs were explored for high performance RF devices. Field emission structures were studied for a variety of applications in devices and displays to name a few. In the areas of advanced fabrication technologies and materials, we saw exciting work on magnetics, metal interconnect materials, and environmentally-benign processes. Lastly, we saw substantial and growing focus on new non-silicon devices in organic and inorganic materials systems.

Photonic devices were studied for a wide range of applications. Quantum dots, photonic crystals and display materials and devices were explored, as well as J-aggregates. Lasers in compound semiconductor materials and heterogeneous integration methods for merging such devices with silicon platforms were pursued. Integrated silicon photonics and silicon-compatible optical interconnect methods were developed. MEMS structures were merged with optics to achieve new functionality in optical systems.

In the area of MEMS, the primary focus areas are; bio/chemical devices and systems, power devices, and a variety of enabling technologies. A large number of microfluidic devices are being developed for manipulation of cells, DNA, proteins, and other molecules. Microreactors are being designed which enable the synthesis of chemicals at a small scale, as well as microbioreactors which can be used in areas such as fermentation studies. Microchemical analysis systems such as portable gas analyzers are also studied. In the area of portable power generation, we are exploring both fuel-burning and energy harvesting approaches. The primary focus of the energy harvesting approaches is to utilize piezoelectric materials for vibration harvesting. In the area of fuel-burning systems, we are exploring microturbines as well as fuel cells and thermophotovoltaics. Beyond these systems focused projects, there are a wide ranging set of projects looking into the applications of MEMS technologies for mechanical devices such as switches, tweezers, and nano-assembly. Lastly, there are some core technology development efforts to understand better, model, and characterize MEMS materials and structures.

Molecular and nanoscale devices are a new and emerging area of work in the lab. Nanoscale assembly methods inspired by origami are studied, as well as nanoscale field ionizers. Nano-dimensioned fluidic channels enable manipulation of chemicals and molecules that are nanoscale. Organic and quantum dot structures are explored for many electronic and photonic purposes. Carbon nanotubes have emerged as potentially exciting structures to explore for many different applications. The work in this area includes not only studying the material, but developing means for fabrication and manipulation of the nanotubes. Magnetic nanoparticles hold great promise in advanced devices and are extensively explored. Self-assembly methods appear as promising methods for creating ordered nanostructures and these methods are being studied in detail. Quantum-effect devices are explored for a variety of applications including quantum computing.



Silicon wafers await the next processing step in the Technology Research Laboratory at MTL. (Photo by Tony Rinaldo Photography)

MTL FACULTY

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
A.I. Akinwande	Display devices: flexible large area electronics, organic and inorganic thin film transistors, field emission displays; high aspect ratio gated microstructure arrays: field emission devices, electrospray thrusters and gas analyzers.	39-553b	617-258-7974	akinwand@mtl.mit.edu
D.A. Antoniadis	Fabrication, measurements and modeling of silicon- and germanium-based devices for high-speed and low-power integrated circuits.	39-427b	617-253-4693	daa@mtl.mit.edu
M.A. Baldo	Molecular electronics, integration of biological materials and conventional electronics, electrical and exciton transport in organic materials, energy transfer, metal-organic contacts, nanomechanical organic transistors.	13-3053	617-452-5132	baldo@mit.edu
G. Barbastathis	3D optical systems, spatial 3D and spectral imaging with a single camera and without scanning, MEMS for integrated optics, Nanostructured Origami™ 3D fabrication and assembly process for nanomanufacturing.	3-461c	617-253-1960	gbarb@mit.edu
K.K. Berggren	Superconductive nanodevice physics and applications; nanofabrication methods, processes, and tool-development for application to superconductive quantum computing, single-photon detection, and reconfigurable devices.	36-219	617-324-0272	berggren@mit.edu
S.N. Bhatia	Micro- and nano-technologies for tissue repair and regeneration. Applications in liver tissue engineering, cell-based BioMEMS, and nanobiotechnology.	E19-502d	617-324-0221	sbhatia@mit.edu
D.S. Boning	Characterization and modeling of variation in semiconductor and MEMS manufacturing with emphasis on chemical mechanical polishing (CMP), plasma etch, and advanced interconnect processes. Understanding the impact of process and device variation on circuit performance, and design for manufacturability.	38-435	617-253-0931	boning@mtl.mit.edu
V.M. Bove, Jr.	Sensing, display, and computation for consumer electronics applications, particularly self-organizing ecosystems of devices. Advanced data representations for multimedia.	E15-368B	617-253-0334	vmb@media.mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
V. Bulović	Physical properties of organic and organic/ inorganic nanocrystal composite thin films and structures; development of nanostructured electronic and optoelectronic devices.	13-3138	617-253-7012	bulovic@mit.edu
A.P. Chandrakasan	Design of digital integrated circuits and systems, emphasis on the energy efficient implementation of microsensor networks and ultra-wideband systems, circuits techniques for deep sub-micron technologies and 3-D integration.	38-107	617-258-7619	anantha@mtl.mit.edu
G. Chen	Heat transfer and energy conversion at micro- and nanometer scales, including microelectronics, photonics, thermoelectrics, thermionics, and thermophotovoltaics; solid-state micro- energy conversion devices and materials, radiation transport and electromagnetic metamaterials; micro and nanofabrication.	3-260	617-253-0006	gchen2@mit.edu
M.J. Cima	Forming methods for complex macro and micro devices, using three dimensional printing. Development of chemically-derived epitaxial oxide films for HTSC coated conductors. Implantable MEMS devices for drug delivery and biomedical applications. Devices and processes for high throughput combinatorial screening of complex materials formulations.	12-011	617-253-6877	mjcima@mit.edu
M.L. Culpepper	Macro-, micro- and nano-scale machines for precision positioning, assembly and manipulation. Basic and applied research on physical principles, modeling approaches, synthesis/simulation tools, design methods and manufacturing practices. Design and manufacture of multi-scale, multi-physics mechanical systems. Hands-on education applied to the mechanical design of micro and nano-scale devices.	35-209	617-452-2395	culpepper@mit.edu
L. Daniel	Parameterized model order reduction of linear and nonlinear dynamical systems; mixed-signal, RF and mm-wave circuit design and robust optimization; power electronics, MEMs design and fabrication; parasitic extraction and accelerated integral equation solvers.	36-849	617-253-2631	luca@mit.edu
J.L. Dawson	Analog system theory and its applications. RF transceivers, power amplifier linearization, high-speed data conversion, problems in nonlinear control.	39-527a	617-324-5281	jldawson@mtl.mit.edu
J.A. del Alamo	Microelectronics device technologies for gigahertz and gigabit-per-second communication systems: physics, modeling, technology and design. Technology and pedagogy of online laboratories for engineering education.	39-415a	617-253-4764	alamo@mit.edu

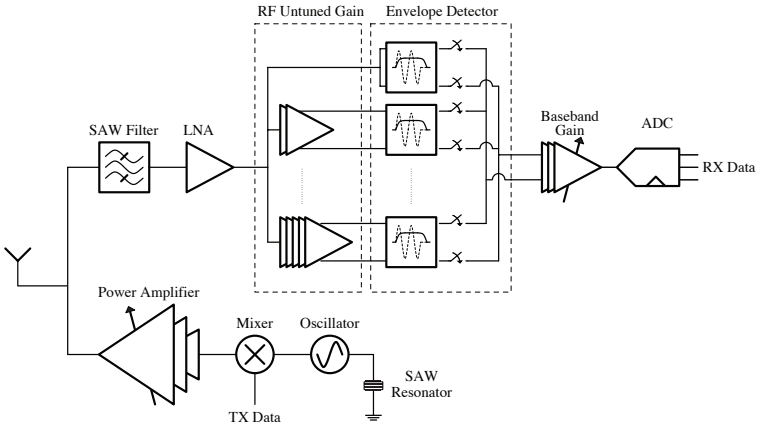
Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
E.A. Fitzgerald	Electronic materials, novel semiconductor heterostructures and devices, heterostructure energy devices (thermoelectrics and thin film batteries), heteromaterial integration, and commercializing fundamental technology.	13-5153	617-258-7461	eafitz@mit.edu
C.G. Fonstad, Jr.	Compound semiconductor heterostructure devices and physics. Optoelectronics: laser diodes, photodiodes, quantum effect devices, and OEICs. Monolithic heterogeneous integration. Microscale thermophotovoltaics.	13-3050	617-253-4634	fonstad@mit.edu
J. Han	Nanofluidic / Microfluidic technologies for advanced biomolecule analysis and sample preparation: novel nanofluidic phenomena, nanofluidic biomolecule separation and pre-concentration, Molecular transport in nano-confined space.	36-841	617-253-2290	jyhan@mit.edu
J.L. Hoyt	Novel processes, materials, and device concepts for silicon technology. Device physics and epitaxial growth of silicon-based heterostructures and nanostructures. Strained Si MOSFETs, heterojunction bipolar transistors, CMOS front-end processing, and silicon-germanium photodetectors.	39-427A	617-452-2873	jlhoyt@mtl.mit.edu
Q. Hu	Physics and applications of millimeter-wave, terahertz, and infrared devices.	36-465	617-253-1573	qhu@mit.edu
K.F. Jensen	Design, fabrication, testing, and integration of microsystems for chemical and biological discovery, synthesis and processing. Microsystems for energy applications, including micro-combustors,-reformers, thermophotovoltaic, and solid oxide fuel cells. Chemical kinetics and transport phenomena related to processing of materials for biomedical, electronic and optical applications.	66-566	617-253-4589	kfjensen@mit.edu
R.D. Kamm	Fluid mechanics, biomedical fluid mechanics, molecular, cell and tissue biomechanics, respiratory physiology, transport phenomena	NE47-321	617-253-5330	rdkamm@mit.edu
S.-G. Kim	Nanomanufacturing, tunable optical MEMS devices and packaging, self-cleaning RF MEMS switch, piezoelectric energy harvesting for autonomous sensors, carbon nanotube transplanting and assembly.	1-310	617-452-2472	sangkim@mit.edu
L.A. Kolodziejski	Research in integrated photonic devices and optoelectronic components. Design and fabrication of photonic crystals and III-V semiconductor devices. Electronic materials growth and characterization.	36-287	617-253-6868	leskolo@mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
J. Kong	Synthesis and characterization of carbon nanotubes, applications of nanotube electrical devices	13-3065	617-324-4068	jingkong@mit.edu
J.H. Lang	Analysis, design and control of electromechanical systems. Application to traditional electromagnetic actuators, micron scale actuators and sensors, and flexible structures	10-176	617-253-4687	lang@mit.edu
H.-S. Lee	Analog and mixed-signal integrated circuits, with a particular emphasis in data conversion circuits in scaled CMOS.	39-553	617-253-5174	hslee@mtl.mit.edu
C. Livermore	Microelectromechanical systems (MEMS). Design and fabrication of high power microsystems, including electrical generators and MEMS components for lasers. Self-assembly techniques for nano- and micro-scale manufacturing.	3-449C	617-253-6761	livermor@mit.edu
S.R. Manalis	Microdevices for biomolecular detection and their application to systems biology and medicine.	E15-422	617-253-5039	scottm@media.mit.edu
I. Masaki	VLSI architecture. Emphasis on interrelationship among applications, systems, algorithms, and chip architectures. Major application fields include intelligent transportation systems, video, and multimedia.	38-107	617-253-8532	imasaki@aol.com
T.P. Orlando	Our focus is on the implementation of the major components of a quantum computer using superconducting circuits. This includes the study of single and coupled qubit behavior, qubit measurement, algorithm implementation, and scalability.	13-3006	617-253-5888	orlando@mit.edu
M.H. Perrott	Circuit and architecture design for high speed mixed-signal circuits such as phase-locked loops and A/D converters: circuit topologies, architectural approaches, design methodologies, modeling, simulation techniques. Communication system simulation software and tutorials for engineering education.	38-344b	617-452-2889	perrott@mit.edu
R.J. Ram	Novel optical and electronic devices for applications ranging from communication networks, efficient energy production, to biosensing and bioprocess development.	36-491	617-253-4182	rajeev@mit.edu
C.A. Ross	Fabrication, properties and applications of magnetic films and nanostructures; self assembly.	13-4005	617-258-0223	caross@mit.edu
R. Sarpeshkar	Bioelectronics: bio-inspired and biomedical electronics.	38-294	617-258-6599	rahuls@mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
M.L. Schattenburg	Advanced lithography, including x-ray, electron-beam, ion-beam, and optical. Nanotechnology and nanofabrication. Precision engineering and nano-accuracy dimensional metrology. Advanced interference lithography technology for high-accuracy patterning of general grating and grid patterns. Micro and nanometer fabrication technology applied to advanced astronomical and laboratory instrumentation. Silicon micromachined structures applied to high-precision optical assembly. X-ray optics and instrumentation.	37-487	617-253-3180	marks@space.mit.edu
M.A. Schmidt	Microelectromechanical systems (MEMS). Microfabrication technologies for integrated circuits, sensors, and actuators; design of micromechanical sensor and actuator systems; mechanical properties of microelectronic materials, with emphasis on silicon wafer bonding technology; integrated microsensors, and microfluidic devices. Novel applications of MEMS and nanotechnologies to a variety of fields, including miniature gas turbines, miniature chemical reactors, miniature gas analyzers, microswitches, biological applications, and sensors monolithically integrated with electronics.	39-521	617-253-7817	schmidt@mtl.mit.edu
A.H. Slocum	Precision machines and mechanisms from macro to nanoscale.	3-445	617-253-0012	slocum@mit.edu
H.I. Smith	Director, NanoStructures Lab. Development of nanofabrication tools and techniques aimed at reaching molecular dimensions and sub-1nm positional accuracy; nanophotonics; templated self assembly.	36-225	617-253-6865	hismith@mit.edu
C.G. Sodini	Design of technology intensive microsystems emphasizing integrated circuit design at the device level, including organic integrated circuits, high data rate wireless LANs, and low data rate wireless sensor systems.	39-527b	617-253-4938	sodini@mit.edu
V. Stojanović	Modeling of noise and dynamics in circuits and systems. Application of convex optimization to digital communications, and analog and VLSI circuits. Communications and signal processing architectures. High-speed electrical and optical links, on-chip signaling, and clock generation and distribution. High-speed digital and mixed-signal IC design.	38-260	617-324-4913	vlada@mit.edu
C.V Thompson	Processing and properties of thin films and nanomaterials for applications in electronic, microelectronic, and photonic micro- and nano-systems.	13-5077	617-253-7652	cthomp@mit.edu

Faculty Name	*Research Areas & Special Interests*	*Office*	*Phone*	*E-mail*
T.A. Thorsen	Microfluidics; microfluid rheology and device development for chemical engineering and biomedical applications	3-248	617-253-9379	thorsen@mit.edu
J. Voldman	Microtechnology for basic and applied cell biology. Electrostatics at the microscale, especially dielectrophoresis.	36-824	617-253-2094	voldman@mit.edu
B.L. Wardle	Nano-engineered composites, MEMS Power devices and energy harvesting, advanced composite materials and systems, structural health monitoring (SHM), fracture, fatigue and damage mechanics, durability modeling/testing, finite-element modeling,; structural response and testing, buckling mechanics, project design and management, business strategy and growth, cost modeling	33-314	617-252-1539	wardle@mit.edu

CIRCUITS & SYSTEMS



▲ Transceiver architecture (D.C. Daly, A.P. Chandrakasan, p. 8).

for additional reading...

Error-correcting Codes that Minimize Receiver Turn-on Time

M. Bhardwaj, A.P. Chandrakasan
Sponsorship: NSF, IBM Fellowship

The profusion of wireless client devices and sensor networks has led to a need for communications links that consume the lowest energy per information bit under a specified range and reliability constraint. To achieve an aggressive metric like 1 nJ/bit over tens of meters with a 10^{-5} BER, we need to carefully pick physical layer (PHY) parameters like modulation, coding, signaling rate etc. Communications theory arguments that optimize transmit power or spectral efficiency typically drive such PHY choices. However, in systems like low-range, low data-rate, pulse-based ultra-wideband (UWB) operating in the unlicensed bands, these are irrelevant metrics. The FCC Tx power limit for such systems is about 40 μW/500 MHz and spectral efficiencies are on the order of 1/1000. For such systems, total energy is determined by the complexity of the receiver, a quantity that classical information theory disregards. Furthermore, since receive energy is proportional to receiver turn-on time, Rx rate (the number of information bits per every bit the Rx looks at) is a more relevant metric than the classical definition of rate (the number of information bits per every bit the transmitter sends). Hence, the objective of our work is to redefine classical communication theoretic problems in terms of receive rates rather than transmit rates. We believe that doing so will lead to fundamental lower bounds on the energy efficiency of a class of receivers.

Thus far our work has revealed that simple repetition codes allow Rx rates to be dropped by 2-3x with only an insignificant increase in Tx rates. We are now working to completely characterize the class of linear block codes that would minimize receive rates. Subsequently, we hope to characterize both systematic and non-systematic convolutional codes.

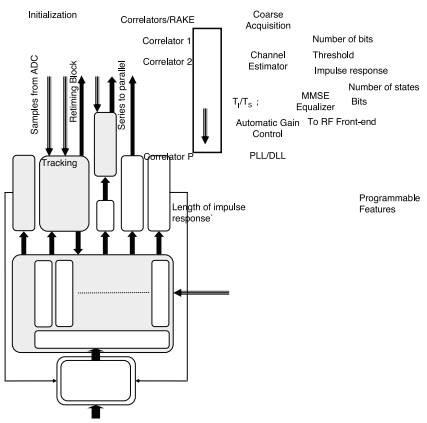
A Robust Digital Baseband for UWB Communications

R. Blázquez, A.P. Chandrakasan
Sponsorship: NSF

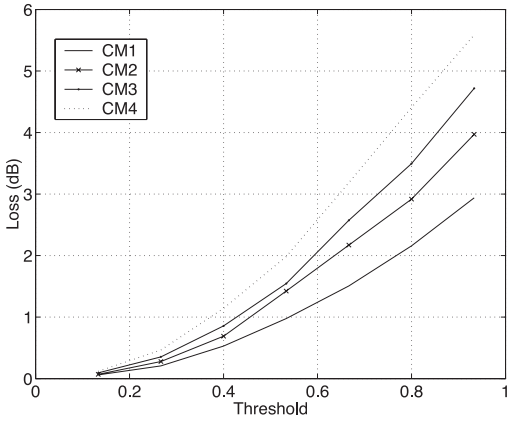
The FCC approved the use of ultra-wideband signals for communication purposes in February 2002 in the band from 3.1 GHz to 10.6 GHz, effectively opening 7.5 GHz of free unlicensed bandwidth. The purpose of this baseband is to achieve 100 Mbps at 10 m in a robust pulsed UWB receiver using 500 MHz of this bandwidth while providing the programmability to expose useful functionality knobs.

Due to the bandwidth of UWB signals, the multipath becomes very relevant as the data rate is increased into the range of the hundreds of megabits per second. The current multipath model, used for the development of IEEE standard 802.15.3a is a modified Saleh-Valenzuela model that has a root mean square duration of the impulse response from 5 to 25 ns [1]. This constraint implies that the receiver must be designed to cope with this multipath in the form of an important inter symbol interference (ISI) that requires, for a pulsed signal, an MMSE demodulator [2]. A digital back-end for UWB applications has been designed that estimates the channel impulse response and uses this information to compensate for it with a RAKE receiver and an MMSE demodulator. Its block diagram is shown in Figure 1. It is also fully programmable, allowing reduction of its complexity and power dissipation whenever the channel quality is high or to provide a robust demodulation if the channel quality is low. Figure 2 shows the trade-off between the complexity of the RAKE receiver and the SNR loss.

The signal processing algorithms for this digital back-end have been tested in a discrete prototype designed also in the Microsystems Technology Laboratory. We acknowledge National Semiconductor for providing the IC fabrication services.



▲ Figure 1: Block diagram of the UWB baseband.



▲ Figure 2: Losses in the modified RAKE receiver as a function of the normalized threshold and the channel model.

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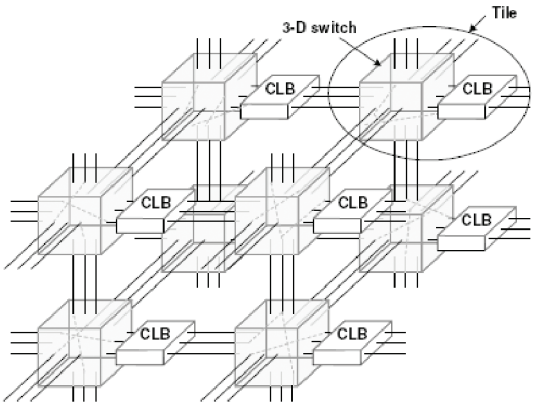
[2] G.D. Forney, "Maximum-likelihood sequence estimation of digital sequences in the presence of intersymbol interference," *IEEE Trans. on Information Theory*, vol. 18, pp. 363-378, May 1972.

CAD for Tile-based 3-D Field Programmable Gate Arrays

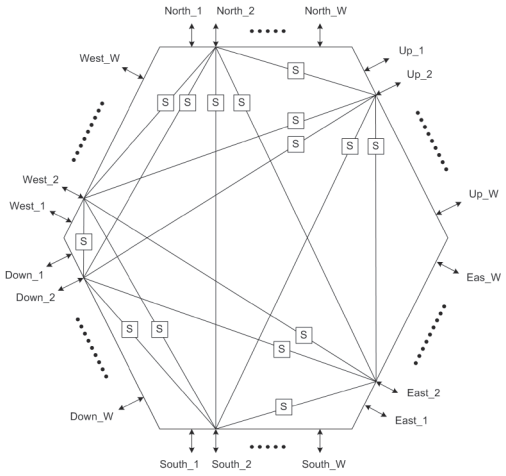
V. Chandrasekhar, A.P. Chandrakasan, D. Troxel
Sponsorship: DARPA

The performance of integrated circuits is limited mainly by the growing interconnect delay as a result of increasing circuit complexity. Three-dimensional integration helps in reducing the interconnect delay by bringing the circuit blocks physically closer to each other. By using the appropriate routing architecture, the relatively small distance between two adjacent vertical layers can be exploited to significantly reduce the interconnect delay of the circuit (see Figure 1) [1]. This work analyzes the benefits of 3-D integration in terms of performance and power consumption in field programmable gate arrays. Instead of partitioning a circuit into layers, the entire circuit is mapped onto the asymmetric 3-D grid of the FPGA. The VPR CAD tool [2] for 2-D FPGAs is modified to route circuits on a 3-D FPGA architecture. The circuit blocks are placed using a simulated annealing algorithm and the pathfinder algorithm is used for routing the nets in the placed circuit.

We are also exploring the use of asymmetric switch matrix architectures (Figure 2) for the 3-D FPGA instead of extending the standard 2-D switch architectures such as the disjoint switch or the Woolton switch matrix. Since the vertical interconnect channel is much shorter, the router tends to route more nets through the vertical channels. However, such a routing increases the capacitance seen by the drivers of the vertical channels inside the switch matrix, which increases the interconnect delay. Since the simulated annealing algorithm places the circuit blocks close together, congestion is more common in the central parts of the FPGA layers. By allowing more routing flexibility in these parts of the FPGA and using sparse routing resources elsewhere, we can significantly reduce the critical path delay of the circuit without losing routability. Moreover, the power consumption can be significantly reduced by using a lower supply voltage to achieve the same operating frequency as a 2-D FPGA.



▲ Figure 1: Block diagram of a 3-D FPGA with switches and CLBs [1].



▲ Figure 2: A 3-D disjoint switch matrix [3].

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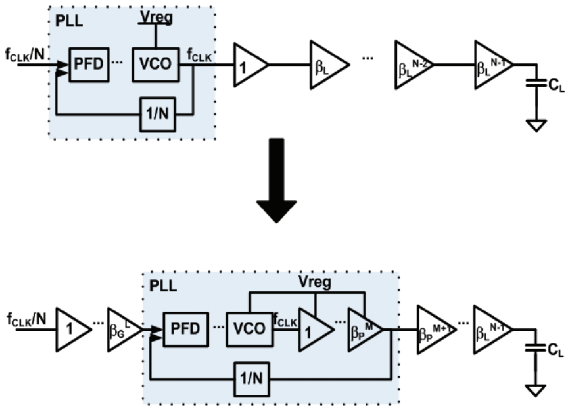
A Power-efficient Multi-local PLL Clock Distribution

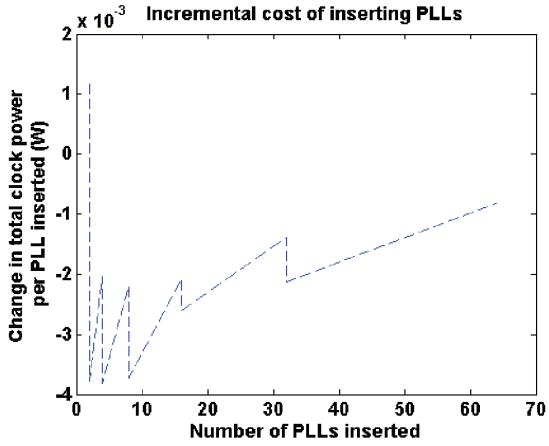
F. Chen, V. Stojanović, A.P. Chandrakasan
Sponsorship: MARCO IFC

In recent generations of high-performance microprocessors, the use of phase-locked loops (PLL) for clock distribution has become more common. As microprocessor operating frequencies increase, the relative impact of clock jitter on the performance of the clock distribution network also increases. Because PLLs have the property of attenuating some of the jitter presented at their input, there have been several investigations [1, 2] into the use of multiple PLLs to distribute the clock. However, the conclusions of these investigations have indicated that the marginal cost of power and complexity for additional PLLs has been too great to warrant more than a single PLL.

In this work, we propose a scalable methodology that utilizes multiple PLLs to reduce the picoseconds of jitter per milliwatt of power in the clocking network. A block diagram of the distribution methodology for a single branch is shown in Figure 1. Distributing the global clock at a lower frequency and locally multiplying up the delivered clock can reduce the cost associated with power, shown in Figure 2, while regulating the buffers local to the PLL can offset jitter accumulation in the PLL. By inserting the PLL deeper into the clock distribution network, fewer unregulated repeaters are needed following the PLL resulting in a net reduction in clock jitter.



▲ Figure 1: The diagram shows the effective change for a given branch of the clock network for the proposed distribution method.



▲ Figure 2: Plot of the incremental change in power for each PLL inserted versus the number of PLLs inserted into the network.

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Carbon Nanotube - CMOS Chemical Sensor Integration

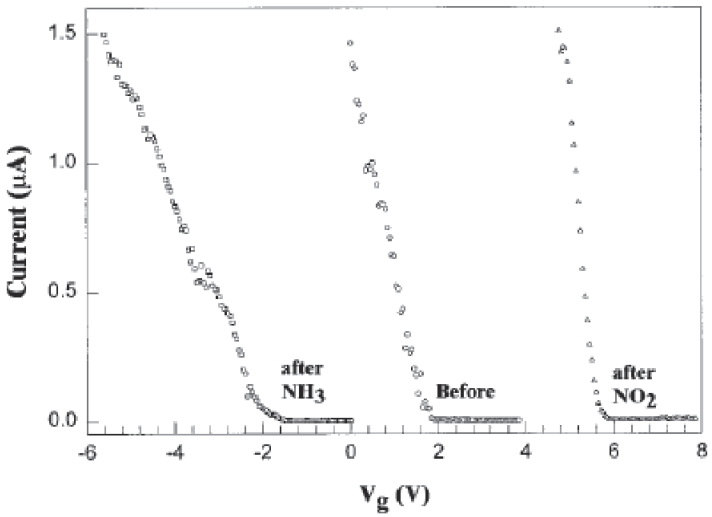
T.S. Cho, A.P. Chandrakasan
Sponsorship: MARCO IFC, Samsung Lee Kun Hee Scholarship Foundation

In this research, we propose an energy-efficient architecture to interface carbon nanotube (CNT) chemical sensors, and the development of signal processing algorithm to reliably infer the chemical concentration in air based on the sensor read-out results. The CNT changes its conductance when exposed to certain chemicals [1] (Figure 1), and thus we can effectively utilize CNTs as resistive chemical sensors. The room-temperature operation of the chemical-sensing mechanism makes CNT an appealing candidate for low-power chemical sensor application.

However, poor control over the CNT process, the resolution requirements in conductance measurements, and the changes in conductance due to specific chemicals in air require that the front-end circuitry has a dynamic range of more than 18 bits. While such accuracy is power-consuming to attain [2], the reduction in power-supply voltage further aggravates the dynamic-range limitations in analog circuits. In order to surmount such problems, we are developing a new architecture suitable for this application.

The stochastic nature of CNT chemical sensors calls for multiple deployments of CNT sensors in one sensor node. This constraint, in turn, requires an efficient algorithm to infer the concentration of the chemical we are interested in. Thus, this research will also delve into developing an energy-efficient algorithm that can be operated in real time.

This project is currently carried out in collaboration with Kyeongjae Lee and Professor Jing Kong from the department of Electrical Engineering and Computer Science at MIT to design an integrated gas sensor.



▲ Figure 1: Conductance change in response to gas detection. Courtesy: J. Kong et al, *Science* [1].

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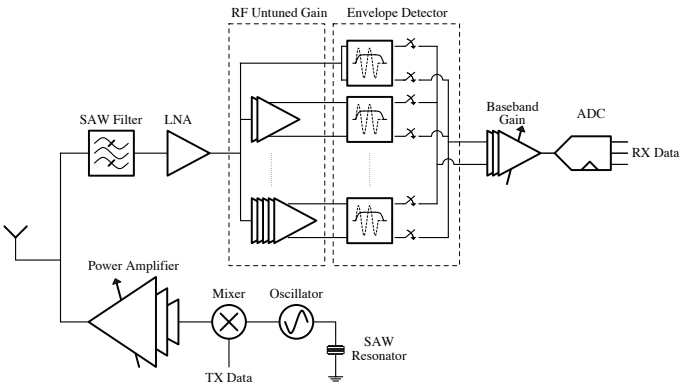
An Energy Efficient Transceiver for Wireless Micro-Sensor Applications

D.C. Daly, A.P. Chandrakasan
Sponsorship: DARPA Power Aware Computing/Communication Program

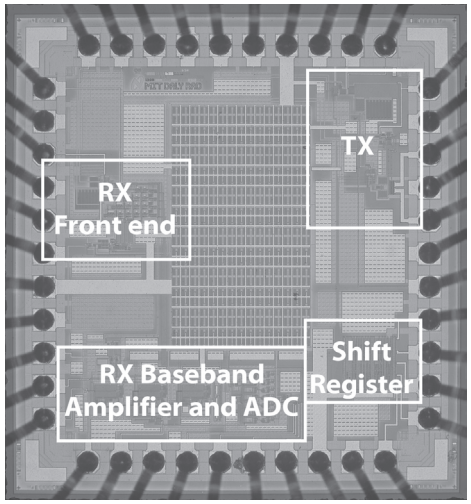
Large-scale wireless sensor networks require a low-power, energy-efficient transceiver that can operate for years on a single battery. To meet this demand for microwatt average power consumption, the transceiver must be scalable, support duty cycling, and be energy-efficient when "on." A key metric for measuring the energy efficiency of the transceiver is the energy per bit ratio, which is equal to the power consumption of the transmitter or receiver divided by the instantaneous data rate. We have fabricated a custom radio for wireless micro-sensor applications that achieves energy-per-bit ratios down to 0.5 nJ/bit in receive mode and 3.8 nJ/bit in transmit mode [1]. These low ratios, combined with a fast receiver startup time of 2.5 μs, allow for energy-efficient operation.

The transceiver operates at 1 Mbps in a single channel centered at 916.5 MHz and employs on-off keying (OOK) modulation. A non-coherent, envelope-detection receiver architecture removes the need for a local oscillator and allows for a fast receiver startup time. Figure 1 shows a block diagram of the transceiver. The RF front end supports several gain settings, so that the power consumption of the receiver can be reduced in the presence of large input signals. The transmitter supports 7 digitally controlled output power levels to enable power-scaling based on node proximity. The receiver power consumption scales from 0.5 mW to 2.6 mW, with an associated sensitivity ranging from -37 dBm to -65 dBm at a bit error rate of 10^{-3}. The transmitter supports output power levels from -11.4 dBm to -2.2 dBm.

The chip was fabricated using 0.18 μm CMOS technology; a chip micrograph is shown in Figure 2. We acknowledge National Semiconductor for providing the IC fabrication services and NSERC for funding. Denis Daly is partially supported by an NSERC fellowship.



▲ Figure 1: Transceiver architecture.



▲ Figure 2: Chip micrograph of the transceiver in 0.18 μm CMOS.

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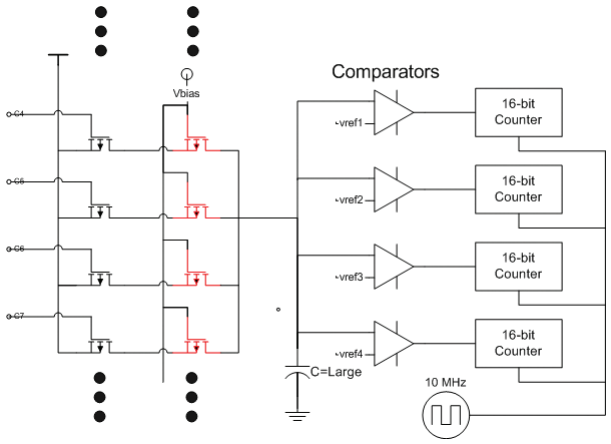
Prediction of Variation in Advanced Process Technology Nodes

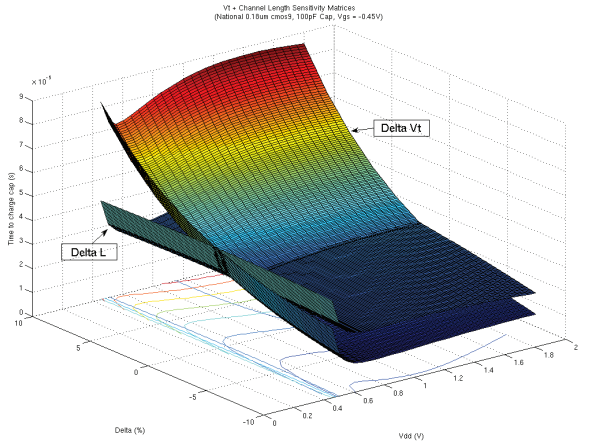
N. Drego, A.P. Chandrakasan, D. Boning
Sponsorship: MARCO C2S2

As Moore's Law forces the semiconductor industry into the sub-50-nm regime, process variability is proportionally becoming larger. Design cycles must simultaneously accommodate this increase in process variability and are thus being extended in order to ensure product robustness in the face of such manufacturing uncertainty. To facilitate the designer's need to accurately model and simulate circuits in the face of variation, we seek to provide predictive statistical models for advanced technology nodes and/or novel transistor architectures. Coupled with predictive technology models (PTM) [1], these statistical models will allow designers to simulate designs in a robust manner during, or even prior to, the development phase of a new process technology.

As a basis for providing such models, we are developing simple digital circuits that ease the measurement and extraction of parameters. An example of such a circuit appears in Figure 1. This circuit employs a delay-based measurement to measure the current drive of each of the transistors highlighted in red. If the transistor is biased in the sub-threshold regime and the DIBL coefficient of the process is small enough, we can use the delay measurement as a proxy for threshold-voltage (V_T) variation (i.e., variations in time to charge the capacitor and disable the counter are dominated by V_T variation as Figure 2 shows). However, if the DIBL coefficient is large enough, ΔV_T is no longer as dominant a source of current variation due to the increasing effect of channel-length variation (ΔL). As a result, the circuit no longer functions as a proxy for V_T variation. Nevertheless, the same circuit can be used to determine I_{ON}/I_{OFF} and the sub-threshold slope of a given transistor. In advanced process technologies, a primary factor in determining the viability of the process will be the performance of the process with regard to short-channel effects (SCE), among which the I_{ON}/I_{OFF} ratio and subthreshold slope are extremely significant. Furthermore, the SCE performance of novel transistor architectures such as the FinFET depends heavily on new critical dimensions such as body (fin) thickness [2]. The ability to efficiently measure variability due to such critical dimensions will enable quick determination of process feasibility. Future work includes fabrication of the aforementioned circuit on both mature as well as novel processes such as a FinFET process. Additionally, we would like to identify other circuits capable of such variation measurement to enable us to build complete statistical models.



▲ Figure 1: Circuit to measure sub-threshold variability performance.



▲ Figure 2: Circuit sensitivities to variation in V_T and L vs. V_{DD}.

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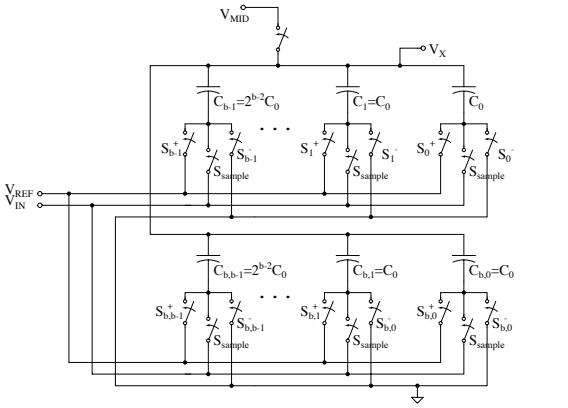
Deep Sub-micron CMOS Analog-to-Digital Conversion for Ultra-wideband Radio

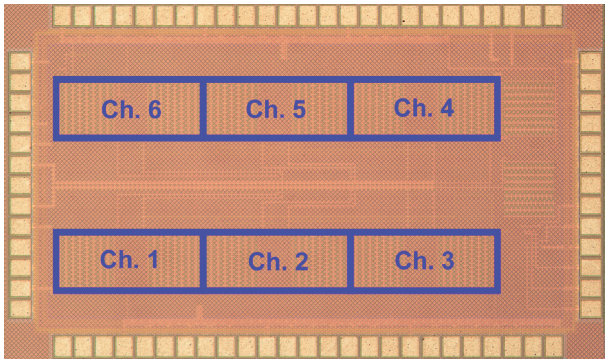
B.P. Ginsburg, A.P. Chandrakasan
Sponsorship: NDSEG Fellowship, DARPA

Ultra-wideband radio can be used for very high data rate (≥480 Mb/s) communication over short distances. For proper reception, the receiver requires a 500-MS/s analog-to-digital converter (ADC) with 4 bits of resolution. While flash is the typical architecture chosen, time-interleaved successive approximation register (SAR) ADCs that operate at these specifications with very low power have recently been demonstrated [1-3]. As feature sizes in CMOS technology continue to scale, new challenges arise for the design of analog and mixed-signal circuits, including reduced voltage supplies, increased variability, and lower transistor output impedances. The SAR architecture is well suited to meet these challenges. It uses only open loop amplification in a comparator, as opposed to the operational amplifier for the pipelined architecture. There is significant digital complexity on the critical path in a SAR converter, but the reduced feature sizes directly improve the digital logic's performance.

A prototype 500-MS/s, 5-b, 6-way time-interleaved SAR ADC [4] has been designed and fabricated in Texas Instruments' 65-nm CMOS process. The prototype includes the first implementation of the split capacitor array [5], seen in Figure 1. This array conserves charge between bit-cycles to lower the overall switching energy, and it settles faster because fewer capacitors switch during each period. The prototype also includes a variable delay line to optimize the instant of latch strobing and lengthen the maximal settling time available for the preamplifiers. The ADC achieves Nyquist performance and consumes 6 mW from a 1.2 V supply. Its die photo is shown in Figure 2.



▲ Figure 1: Block diagram of the split capacitor array. The MSB capacitor has been split into an identical copy of the rest of the array, which improves both switching energy and speed.



▲ Figure 2: Die photograph of 65-nm CMOS ADC. Total die area is 1.2 x 1.8 mm^2.

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Fine-grain Power Control for Field Programmable Gate Arrays

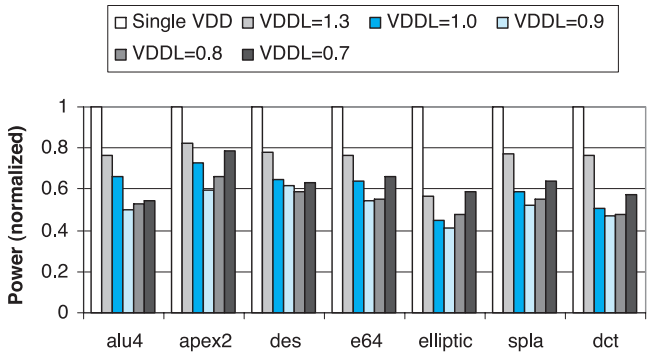
F. Honoré, A.P. Chandrakasan, D. Troxel
Sponsorship: MARCO IFC

Implementation flexibility through hardware reconfiguration has become an important factor in the design of digital systems. Field programmable gate arrays (FPGAs) are extending their application area from system prototyping to custom application implementation but they are much slower and less power-efficient than ASIC systems. We have developed a power- and performance-scalable multi-V_{DD} FPGA. The interconnect overhead for FPGAs is a large fraction of the power and delay, due to the use of programmable switch elements. Fine-grain voltage domains allow low-energy operation in non-critical areas of logic and routing segments.

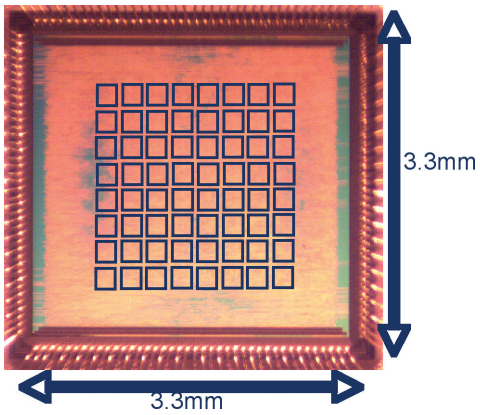
We modified a public domain FPGA place-and-route tool to handle the assignment of the voltage domains for non-critical paths. Thus, by selecting either a low or high voltage for each domain, this method achieves an average of 2x improvement in power for the same performance, as shown in Figure 1. The high V_{DD} is kept at 1.8 V and the low V_{DD} can vary depending on the application. Low-overhead level converters provide voltage conversion between domains when necessary. The area overhead for the power switches and level converters is less than 10%. With these fine-grain controls, the software is able to reduce dynamic power while maintaining performance.

We have fabricated and tested a 3mm x 3mm chip (Figure 2) using a semi-custom ASIC flow to validate the approach and have developed custom CAD tools to automate the implementation of some of these techniques. The test chip contains 64 tiles of logic. Testing confirmed functionality at a range of voltages from 1.8 V down to 550 mV.

The chip was fabricated using 0.18 µm CMOS technology. We acknowledge National Semiconductor for providing IC fabrication services.



▲ Figure 1: Benchmark results showing an average improvement of 52% at a V_{DDH} of 1.8 V and V_{DDL} of 0.9 V.



▲ Figure 2: Die photo of fabricated test chip.

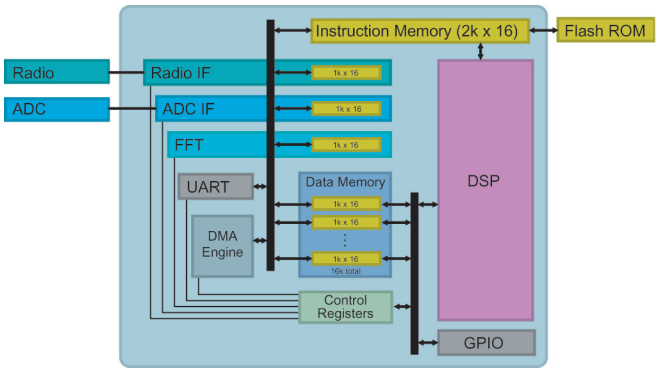
A Micropower DSP Architecture for Self-powered Microsensor Applications

N. Ickes, D. Finchelstein, A.P. Chandrakasan
Sponsorship: DARPA Power Aware Computing/Communication Program

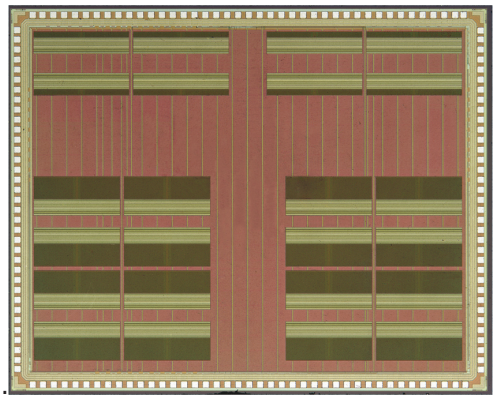
Distributed microsensor networks consist of hundreds or thousands of miniature sensor nodes. Each node individually monitors the environment and collects data as directed by the user, and the network collaborates as a whole to deliver high-quality observations to a central base station. The large number of nodes in a microsensor network enables high-resolution, multi-dimensional observations and fault-tolerance that are superior to more traditional sensing systems. However, the small size and highly distributed arrangement of the individual sensor nodes make aggressive power management a necessity.

The aim of our project is to build a highly integrated yet versatile sensor system with a strong focus on energy efficiency and agility. Tracking the optimal operating point in the dynamic environments typical for sensor networks requires hardware that can vary clock rates, power supply voltages, and other circuit parameters in real time. We have developed an architecture consisting of a micropower DSP surrounded by dedicated accelerator blocks for frequently used, complex functions—such as Fourier transforms and FIR filtering. This architecture of highly optimized, on-demand hardware support for energy intensive tasks allows for ultra-low-power data manipulation and lowers the processing burden on the general-purpose DSP core.

An initial implementation of the architecture was fabricated in 0.18 μm CMOS by National Semiconductor. This implementation included a custom 16-bit DSP core, an FFT accelerator, and interfaces to custom ADC and radio chips, as illustrated in Figure 1. The fabricated chip operates at supply voltages as low as 0.5 V, consuming only 110 μW. A die photo of the chip is shown in Figure 2. A complete, miniature microsensor node was built around this chip, incorporating custom ADC and radio chips developed by other students in our group. A second-generation architecture is currently being fabricated in 90 nm CMOS by ST Microelectronics. This version features a streamlined datapath and extensive power- and clock-gating for further power reduction.



▲ Figure 1: First-generation DSP architecture.



▲ Figure 2: Die photo of first-generation DSP chip.

CMOS Circuit Techniques for Data-rate Enhancement in VCSEL-based Chip-to-chip Optical Links

A.M. Kern, A.P. Chandrakasan
Sponsorship: MARCO IFC, Intel, NSF

Optical chip-to-chip signaling promises to replace electrical serial links when data-rate requirements increase beyond the bandwidth limits of conventional copper traces. Recent advances in VCSEL technology have dramatically increased the performance of short-distance optical links and VCSELs nominally suitable for 10 Gb/s links are now commercially available. However, substantially higher data rates may be achieved by designing optical transceiver architectures and circuits to compensate for VCSEL bandwidth limitations.

The designed 90 nm CMOS VCSEL driver uses pre-emphasis to enable 20 Gb/s data rates with a 10 Gb/s VCSEL. The driver uses dual-edge pre-emphasis of the modulation current to compensate for the bandwidth limitation introduced by the significant parasitic capacitance of the VCSEL. The VCSEL is modulated with the summed output of two current-mode drivers, where the output of the second driver is delayed, inverted, and attenuated with respect to the first in order to introduce current emphasis at data transitions. The pre-emphasis portion of the output current is primarily absorbed by the parasitic capacitor, thereby reducing the charging time and opening the eye of the VCSEL junction current.

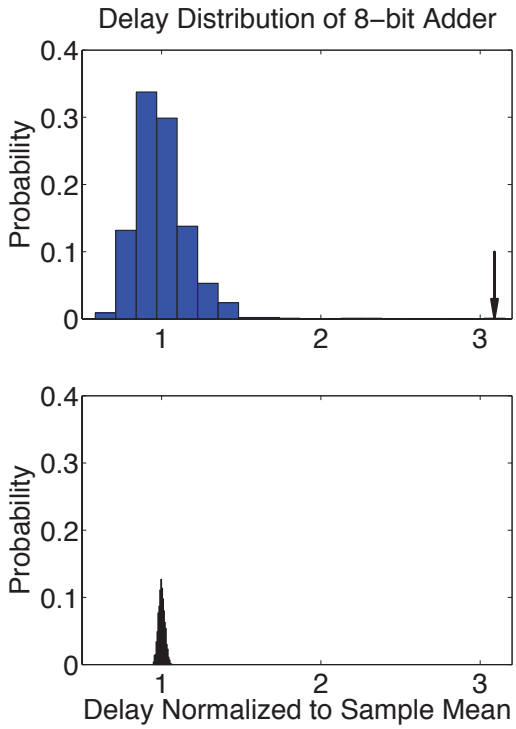
The driver design includes digital controls to allow for post-fabrication programming of the pre-emphasis pulse duration, the modulation current, and the pre-emphasis current. The modulation and pre-emphasis current are controlled independently by two 5-bit DACs and the width of the pre-emphasis pulse is controlled by a 4-tap digital delay line. This programmability improves robustness to variations and allows characterization of the effect of varying the height and width of the pre-emphasis pulse. The VCSEL driver simulation results, based on extracted layout, demonstrate 20 Gb/s operation without the use of inductors. Preliminary testing of the fabricated chip is ongoing at the time of publication.

A Sub-threshold Cell Library and Methodology

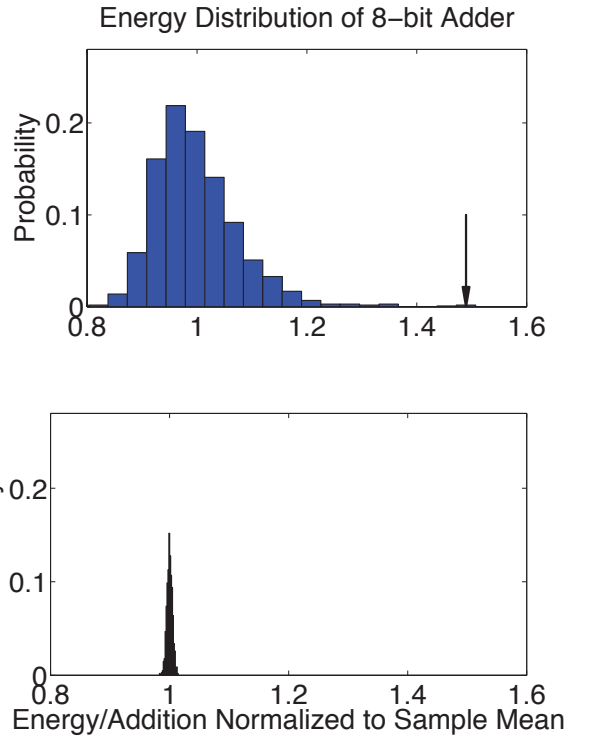
J. Kwong, A.P. Chandrakasan
Sponsorship: Texas Instruments, DARPA

In this work, we develop a sub-threshold library and design methodology that addresses the unique challenges and trade-offs in ultra-low voltage operation. Drive currents become comparable in magnitude to idle leakage currents, causing reduced output swings and possible functional errors. Due to the exponential dependence of sub-threshold currents on threshold voltage, sub-threshold circuits are particularly sensitive to environmental and process variations. Figure 1a compares the delay distributions of an 8-bit adder in the sub-threshold and above-threshold regimes under transistor threshold voltage variation. Figure 1b performs the same comparison for energy. Circuit performance exhibits much larger variability in the sub-threshold regime, which can be mitigated through device sizing and choice of logic styles.

The sub-threshold library employs a device sizing methodology with functionality as the primary consideration while implementing appropriate trade-offs among energy, delay, and variability. Different logic styles are also evaluated during cell design. When device sizes are adjusted for equal functional yield, a transmission gate full adder [1] offers an energy benefit because it avoids the large device stacks in static CMOS logic. Particular attention is given to robustness of memory storage elements, where idle leakage can significantly degrade data retention capabilities. This library serves as a platform for further exploration of error-resilient architectures in the sub-threshold regime.



▲ Figure 1a: Delay distribution of 8-bit adder at sub-threshold (top) and nominal (bottom) power supplies, under threshold voltage variation. Arrow points to outliers.



▲ Figure 1b: Energy distribution of 8-bit adder at sub-threshold (top) and nominal (bottom) power supplies, under threshold voltage variation. Arrow points to outliers.

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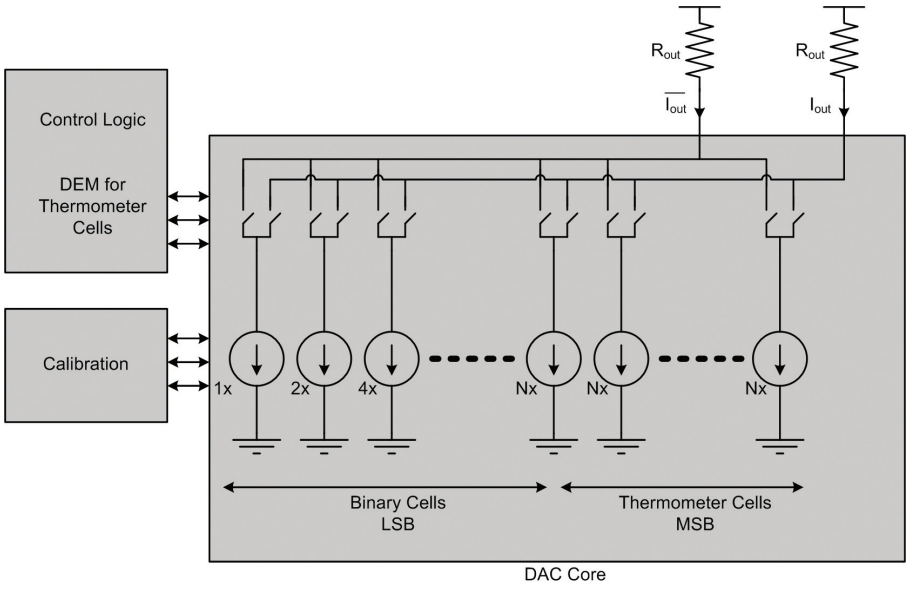
Design of a High-speed, High-resolution DAC in 2-D and 3-D Processes

P. Lajevardi, A.P. Chandrakasan
Sponsorship: DARPA

A 2-D 16-b 100-MS/s digital to analog converter (DAC) is being designed for multi-carrier communication applications. In this type of DACs, the important challenge is to minimize the harmonic distortion (HD) and Inter-modulation distortion (IMD) and to maximize spurious free dynamic range (SFDR). Some important factors that affect HD, SFDR, and output noise of a DAC include glitch on the clock and control signals, jitter on the control signals, mismatch, settling error, clock feed-through (CFT), and the circuit noise.

Analog and digital techniques such as dynamic element matching (DEM) and calibration have been explored to optimize the performance of DACs[1]. A 3-D version of a DAC is expected to show additional improvement in DAC performance. Since timing mismatch between the control signals is one of the main sources of dynamic distortion in DACs, 3-D fabrication improves the harmonic distortion by providing more connectivity for active cells and allowing lower distance between cells. In addition, calibration blocks can be placed on the upper die above each analog cell to provide more feedback. Substrate isolation between analog and digital circuits also improves the coupling noise.

Current steering DACs have shown a good performance for high-speed, high-resolution applications. The DAC architecture is partitioned in 3 active layers. The partitioning is being optimized for minimizing SFDR which is the main performance metric in high-speed, high-resolution DACs.



▲ Figure 1: Block diagram of a current steering DAC.

REFERENCES

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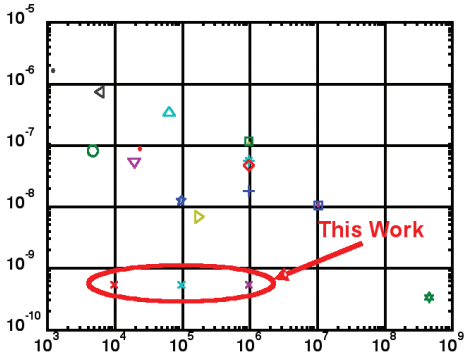
An Energy-efficient Ultra-wideband Radio Receiver

F.S. Lee, A.P. Chandrakasan
Sponsorship: NSF

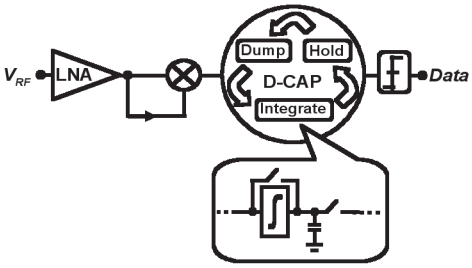
The development of energy-efficient short-range (30 cm to 10 m) wireless radio transceivers has become an active area of research with the growth of high data-rate wireless battery-operated appliances, as well as with the onset of low data-rate ad-hoc wireless networks [1]. The primary figure of merit for energy efficient radios is energy/bit. Within reasonable energy costs, it is also desirable to keep the bit-error-rate (BER) less than the worst-case value of 10^{-3}. This research explores the utilization of ultra-wideband (UWB) signals to achieve improvements in wireless receiver energy/bit consumption by an order of magnitude or more at low data-rates.

Figure 1 plots energy/bit of recent receivers against data-rate. As the data-rate increases, the energy/bit decreases as the fixed-costs for radio energy consumption in the oscillator and bias currents for the analog circuits are amortized over more bits per unit time. Therefore, to reduce energy/bit at low data-rates it is necessary to build circuits that can be duty-cycled with low settling time and to choose a signaling architecture that does not require power-hungry high frequency oscillators and clock buffers. Because UWB signals are essentially short impulses in time, they inherently lend themselves to receiver architectures that can be deeply duty-cycled.

This work focuses on developing an extremely low energy receiver operating at low data-rates using UWB signaling. Figure 2 shows a block diagram of the receiver architecture. Proper choices of the signaling technique, adjustable filters to address in-band interferers and channel selectivity, amplifier and mixer circuit innovations, a novel low-power digitally-configurable analog processor (D-CAP) for mixed-signal correlation, and duty-cycling of circuits all work in tandem to realize a sub-nJ/bit, 10 kbps – 1 Mbps receiver in a 0.5 V, 90 nm CMOS process.



▲ Figure 1: Energy/bit verses data-rate for recent receivers [2].



▲ Figure 2: Block diagram of low-energy receiver.

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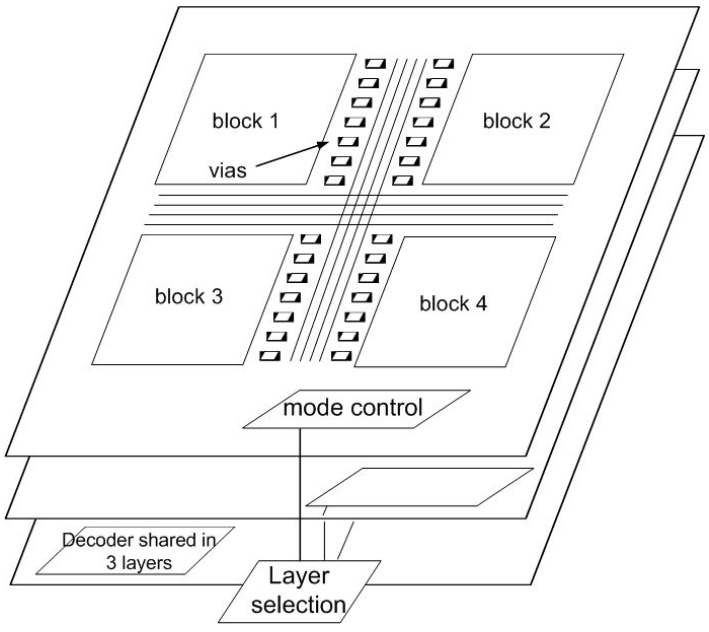
3-D SRAM Architecture and Circuits

T. Pan, A.P. Chandrakasan
Sponsorship: DARPA

Long global interconnect limits the performance of high-performance SRAM. Large leakage power dissipation is another concern in scaled SRAM design. The 3-D technology is a promising approach to reduce interconnect delay and power dissipation by replacing long global wires with short vertical interconnects. In preliminary simulations using 3-D layout, we see a 20% reduction in access time compared to a conventional 2-D implementation. The use of 3-D technology decreases the number of buffers needed to drive long global wires, further reducing propagation delay. Our architecture introduces a layer selection signal in addition to a block, row and column decoder. The layer selection can be used to reduce active and leakage power. Since transistors are closer together in 3D, blocks and columns can share part of the control circuits, such as the sense-amplifier. Figure 1 shows the block diagram of the SRAM memory.

We are developing a model that takes both horizontal and vertical parameters into account and gives the optimized memory architecture once the total size of the memory is specified. An optimum partition between layers and the block size will be generated. The optimum buffer insertion will also be determined. A SRAM layout generator based on 0.18 μm Lincoln Labs SOI 3-D integration technology is being developed.



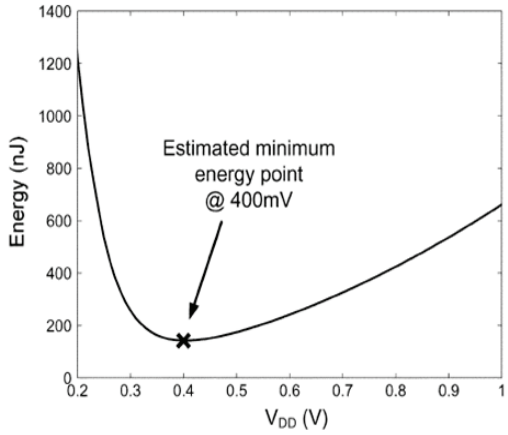
▲ Figure 1: Proposed 3-D SRAM architecture.

An Energy-optimal Power Supply for Digital Circuits

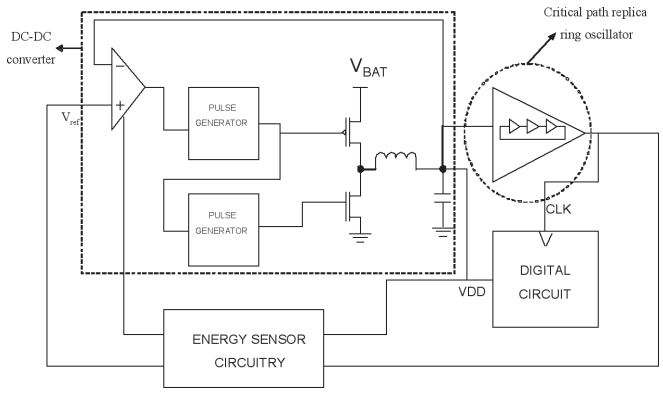
Y.K. Ramadass, A.P. Chandrakasan
Sponsorship: DARPA, Texas Instruments

Substantial savings in the energy consumed by a digital circuit can be obtained by operating the circuit below the threshold voltage of its devices. The variation of the energy consumed per operation with the operating voltage for a FFT circuit is shown in Figure 1. This curve is dynamic in nature and changes with temperature, workload of the circuit, nature of operations performed by the circuit and data handled. The optimum energy point shifts widely as the curve changes, which necessitates a circuit to track the optimum energy point with changing conditions. The optimal supply voltage for minimum energy-operation usually falls into the sub-threshold region of operation of digital circuits (i.e., below the device thresholds). At these voltages, the circuits operate substantially more slowly. A minimum energy feedback loop would fit well with energy-driven class of circuits where performance is not a key issue.

The energy minimization circuitry (Figure 2) consists of a buck converter that operates in the pulse frequency modulation (PFM) mode. The digital circuit under test, which operates at the V_{dd} set by the converter, is clocked by a critical path replica ring oscillator. The energy-sensor circuitry determines the energy consumed per operation at different operating voltages. Based on the energy per operation at a given operating voltage obtained from the energy-sensing circuitry, an energy minimization algorithm changes the reference voltage to the buck converter suitably and the system approaches the minimum energy operating voltage of the digital circuit using a slope-detection strategy. A test chip containing the minimum energy tracking loop and an embedded DC-DC converter has been fabricated in Texas Instruments' 65 nm CMOS process.



▲ Figure 1: Estimated minimum energy point for an FFT using a typical transistor in a 0.18-µm technology (from [1]).



▲ Figure 2: Block diagram of the energy minimization loop with the DC-DC converter.

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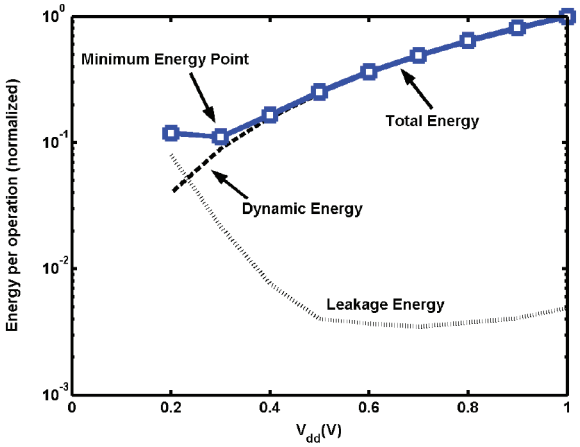
An Energy-efficient Digital Baseband Processor for Pulsed UWB Using Extreme Parallellization

V. Sze, R. Blázquez, A.P. Chandrakasan
Sponsorship: DARPA

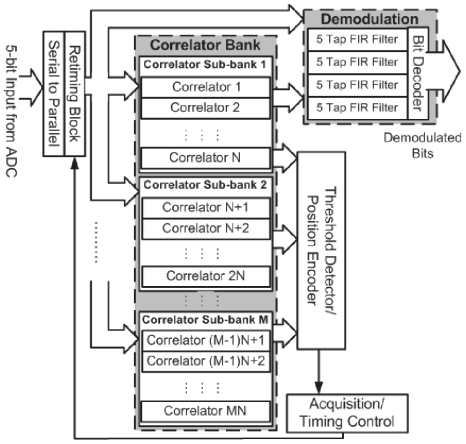
The use of ultra-wideband (UWB) as a medium for high - data rate last meter links creates a need for integrating UWB radios into battery-operated devices such as mobile phones, handheld devices, and sensor nodes. Consequently, there is a strong demand for an energy-efficient UWB system. We propose using parallelism in the digital baseband processor to reduce the energy required to receive UWB packets.

An energy-efficient baseband can be achieved by exploiting two forms of parallelism. First, the supply voltage of the digital baseband can be lowered so that the correlator operates near its minimum energy point, which occurs below the threshold voltage, placing the circuit in the sub-threshold region [1]. Figure 1 shows the energy per operation of a single correlator for various supply voltages. The correlator and the rest of the baseband must then be parallelized to maintain a throughput of 500 MSPS at this reduced voltage. While sub-threshold operation is traditionally used for low-energy, low-frequency applications such as wrist-watches, this work examines how sub-threshold operation can be applied to low-energy, high-performance applications.

Second, the correlators can be further parallelized for a significant reduction in the synchronization time. The reduced synchronization time allows the baseband and the rest of the receiver to be turned off earlier, resulting in a system-wide reduction in energy. The architecture shown in Figure 2 will be implemented in STMicroelectronics 90 nm process. The baseband processor will be designed to deliver a maximum of 100 Mbps.



▲ Figure 1: Simulated energy plot for correlators [2].



▲ Figure 2: System level diagram of UWB digital baseband. The N and M are parameters for the different forms of parallelism.

REFERENCES

[1] B.H. Calhoun and A.P. Chandrakasan, "Characterizing and modeling minimum energy operation for sub-threshold circuits," *Int'l. Symposium on Low Power Electronics and Design*, 2004.

[2] V. Sze, R. Blázquez, M. Bhardwaj, and A.P. Chandrakasan, "An energy-efficient sub-threshold baseband processor architecture for pulsed ultra-wideband communications," *Int'l. Conf. on Acoustics, Speech, and Signal Processing*, 2006.

An Ultra Low-power ADC for Wireless Micro Sensor Applications

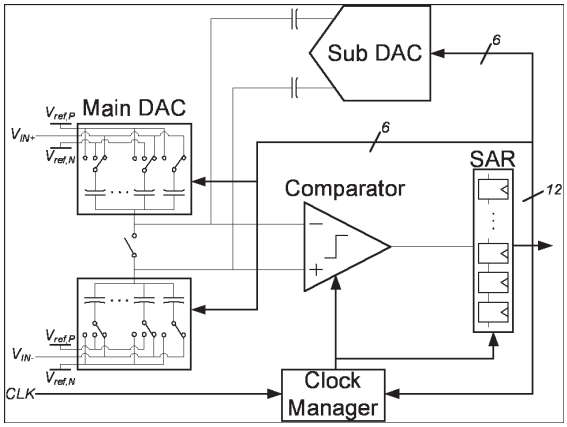
N. Verma, A.P. Chandrakasan
Sponsorship: DARPA Power Aware Computing/Communication Program

Autonomous micro-sensor nodes rely on low-power circuits to enable energy harvesting as a means of sustaining long-term, maintenance free operation. This work presents the design of an ultra low-power analog-to-digital converter (ADC) whose sampling rate and resolution can be scaled to dynamically recover power savings [1].

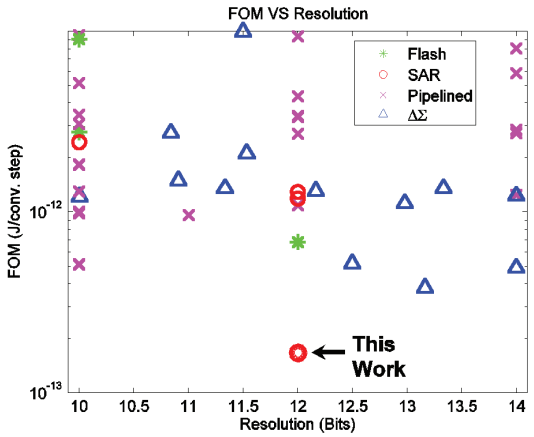
The ADC has a sampling rate of 0-100 kS/s and a resolution of either 12 or 8 bits. The design is based on the successive approximation register architecture (SAR), which is shown in Figure 1. Several techniques improve the efficiency of the ADC: analog offset calibration in the latch improves the comparator power-delay product; weak-inversion operation increases preamplifier g_m/I; robust self-timing eases settling requirements; sub-DAC gain adjustment compensates non-linearities from top-plate parasitics; and switched-capacitor auto-zero reference generation maximizes common-mode rejection.

The ADC was fabricated in a 0.18 μm, 5M2P CMOS process. In 12b mode, the measured SNDR, with a 48 kHz input tone, is 65 dB (10.55 ENOB), and the SFDR is 71 dB. The total power consumption of the ADC is 25 μW at 100kS/s and decreases linearly towards zero as the sampling rate is reduced. This corresponds to a figure-of-merit ($P/(2F_{IN}2^{ENOB})$) of 165 fJ/conv.Step which, as shown in Figure 2, is best reported among medium to high resolution ADCs.

We acknowledge National Semiconductor for providing the IC fabrication services.



▲ Figure 1: System block diagram of low-power SAR ADC.



▲ Figure 2: Figure-of-merit comparison with state of the art ADCs.

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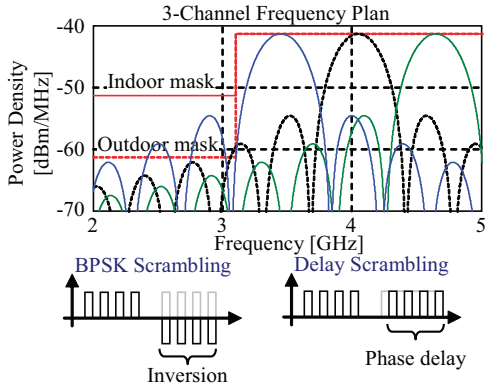
[1] N. Verma and A.P. Chandrakasan, "A 25μW 100kS/s ADC for wireless micro-sensor applications," *ISSCC Dig. Tech. Papers*, pp. 222-223, Feb. 2006.

An All-digital, Pulsed-UWB Transmitter in 90-nm CMOS

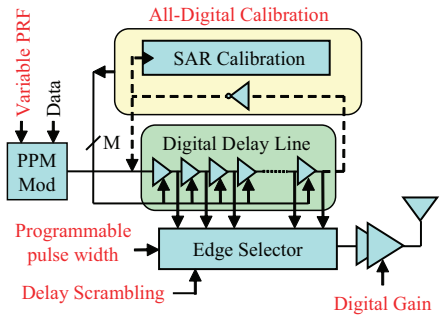
D.D. Wentzloff, A.P. Chandrakasan
Sponsorship: NSF

A common metric for comparing the performance of energy-constrained wireless radios is energy consumed per bit transmitted. As the maximum data rate is reduced in a typical wireless link, the energy/bit increases due to the increased on-time of the analog electronics. For low data-rate applications such as RFID tags and wireless sensor nodes, the energy/bit of the wireless link is optimized by employing a very high data-rate radio with a low duty-cycle. This radio can be undesirable from a system perspective when considering network latency and baseband processing. Furthermore, finite startup time of the analog electronics limits the minimum energy/bit that can be obtained. Conversely, pulsed ultra-wideband (UWB) radios can exploit the inherent duty-cycled nature of their signaling to overcome the date rate/on-time tradeoff that leads to increased energy/bit in other radios [1]. The pulsed-signaling also makes UWB transmitters well-suited for an all-digital implementation, resulting in energy/bit proportional to CV_{dd}^2, which scales with process technology. The proposed transmitter will simultaneously achieve sub-nJ/bit energy consumption with a data rate variable from 1 kb/s-1 Mb/s. The data rate may be reduced with very little penalty in energy/bit by avoiding the use of any constant-biased analog circuits such as local oscillators.

The transmitter is designed to operate in a custom transceiver architecture that trades off spectral efficiency for total energy/bit. The frequency plan utilizes the 3.1-5.0-GHz UWB band, divided into three non-overlapping channels of 550 MHz each, as shown in Figure 1. Binary pulse-position modulated (PPM) square pulses are generated in the selected channel at a variable pulse-repetition frequency (PRF) of 1 kHz-1 MHz. The spectrum of PPM signals contains spectral lines that reduce the spectral efficiency [2]. Therefore PPM signals are phase scrambled in order to eliminate these lines. Conventional BPSK scrambling requires differential signaling, adding to the complexity and energy consumption of the transmitter. However, spectral lines may be sufficiently reduced by scrambling with a phase delay as shown in Figure 1. This delay can be fully synthesized and requires no analog components, keeping complexity and energy low. Figure 2 shows the transmitter architecture. Pulses are synthesized by combining a variable number of edges of a delay line clocked at the PRF. The center frequency of the pulse is selected by calibrating the delay/stage in the delay line with an off-line digital calibration loop. The digital pulse is amplified by an inverter chain with power gating for gain control and leakage reduction. The transmitter is capable of driving a 50-Ω UWB antenna with 800-mVppk while consuming <1-nJ/bit.



▲ Figure 1: Spectrum of the three-channel frequency plan with the FCC indoor and outdoor spectral masks (top). Illustration of phase-delay scrambling of PPM pulses to reduce spectral lines (bottom).



▲ Figure 2: Block diagram of the all-digital transmitter.

REFERENCES

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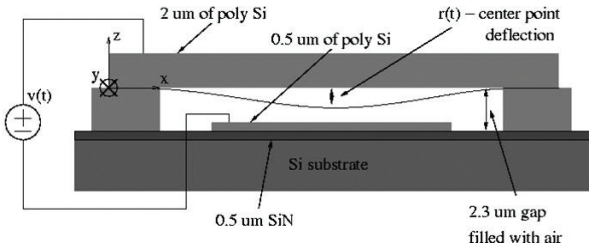
[2] Y.-P. Nakache and A.F. Molisch. "Spectral shape of UWB signals - influence of modulation format, multiple access scheme and pulse shape," *Vehicular Tech. Conf.*, vol. 4, Apr. 2003, pp. 2510-2514.

Parameterized Model Order Reduction of Nonlinear Circuits and MEMS

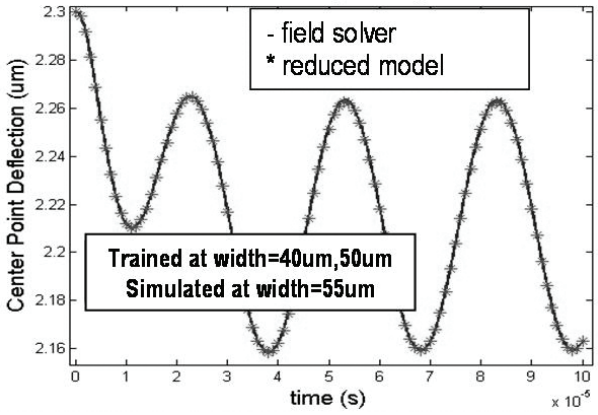
B. Bond, L. Daniel
Sponsorship: MARCO GSRC, NSF

The presence of several nonlinear analog circuits and micro-electro-mechanical (MEM) components in modern mixed-signal system-on-chips (SoC) makes the fully automatic synthesis and optimization of such systems an extremely challenging task. Our research is the development of techniques for generating parameterized reduced-order models (PROM) of nonlinear dynamical systems. These reduced-order models could serve as a first step towards the automatic and accurate characterization of geometrically complex components and subcircuits, eventually enabling their synthesis and optimization. Our approach combines elements of an existing non-parameterized trajectory piecewise linear method [1] for nonlinear systems with an existing moment matching parameterized technique [2] for linear systems. By building on these two existing methods, we have created four different algorithms for generating PROMs for nonlinear systems. The algorithms were tested on three different systems: a MEM switch, shown in Figure 1, and two nonlinear analog circuits. All of the examples contain distributed strong nonlinearities and possess some dependence on several geometric parameters.

The reduced-order models can be constructed to possess strong local or global accuracy in the parameter-space, depending on which algorithm is used. Figure 2 shows the output of one PROM created for the example in Figure 1 and compared to the field solver output of the full nonlinear system. In this example the system was parameterized in the width of the device and simulated at a parameter value different from the values at which the model was created. We found that in general the best algorithm is application-specific, but the PROMs are very accurate over a practical range of parameter values. For further details on parameter-space accuracy and cost of the algorithms, see [3].



▲ Figure 1: Application example: MEM switch realized by a polysilicon beam fixed at both ends and suspended over a semiconducting pad and substrate expansion.



▲ Figure 2: Center point deflection predicted by our parameterized reduced model of order 40, compared to a finite difference detailed simulation.

REFERENCES

[1] M. Rewienski and J.K. White. "A trajectory piecewise-linear approach to model order reduction and fast simulation of nonlinear circuits and micromachined devices," in *Proc. of IEEE/ACM International Conf. on Computer Aided-Design*, pp. 252-257, Nov. 2001.

[2] L.Daniel, C.S. Ong, S.C. Low, K.H. Lee, and J.K. White, "A multiparameter moment matching model reduction approach for generating geometrically parameterized interconnect performance models," *IEEE Trans. On Computer-Aided Design of Integrated Circuits and Systems*, 23(5), pp. 678-693, May 2004.

[3] B. Bond and L. Daniel. "Parameterized model order reduction of nonlinear dynamical systems," in *Proc. of the IEEE Conf. on Computer-Aided Design*, pp. 487-494, 2005.

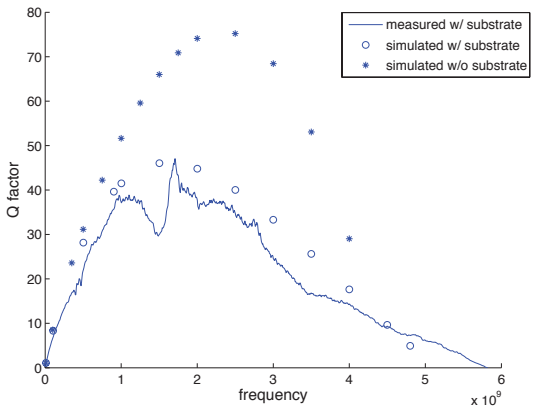
Development of Specialized Basis Functions and Efficient Substrate Integration Techniques for Electromagnetic Analysis of Interconnect and RF Inductors

X. Hu, T.A.E. Moselhy, J. White, L. Daniel
Sponsorship: SRC, MARCO GSRC, NSF

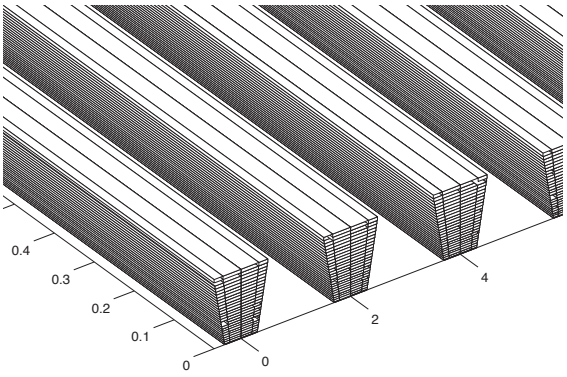
The performance of several mixed-signal and RF-analog platforms depends on substrate effects that need to be represented in the library model with critical field solver accuracy. For instance, substrate-induced currents in RF inductors can severely affect quality and hence RF filter selectivity. We have developed an efficient approach to full-wave impedance extraction that accounts for substrate effects through the use of two-layer media Green's functions in a mixed-potential-integral-equation (MPIE) solver. In particular, we have developed accelerated techniques for both volume and surface integrations in the solver.

In this work, we have also introduced a technique for the numerical generation of basis functions that are capable of parameterizing the frequency-variant nature of cross-sectional conductor current distributions. Hence skin and proximity effects can be captured utilizing many fewer basis functions in comparison to the prevalently-used piecewise-constant basis functions. One important characteristic of these basis functions is that they only need to be pre-computed once for a frequency range of interest per unique conductor cross-sectional geometry, and they can be stored off-line with a minimal associated cost. In addition, the robustness of these frequency-independent basis functions is enforced using an optimization routine.

We have shown in [2] that the cost of solving a complex interconnect system using our new basis functions can be reduced by a factor of 170 when compared to the use of piecewise-constant basis functions over a wide range of operating frequencies. Furthermore our volume and surface integration routines result in additional efficient improvement by a factor of 9.8 as shown in [1]. Our solver accuracy is validated against measurements taken on fabricated devices.



▲ Figure 1: Measured and simulated Q-factors for a square RF inductor with an area of 15 mm x 15 mm and surrounded by a ground ring.



▲ Figure 2: Our basis functions avoid the expensive cross-sectional discretization shown in figure necessary to account for trapezoidal cross-sections or skin and proximity effects.

REFERENCES

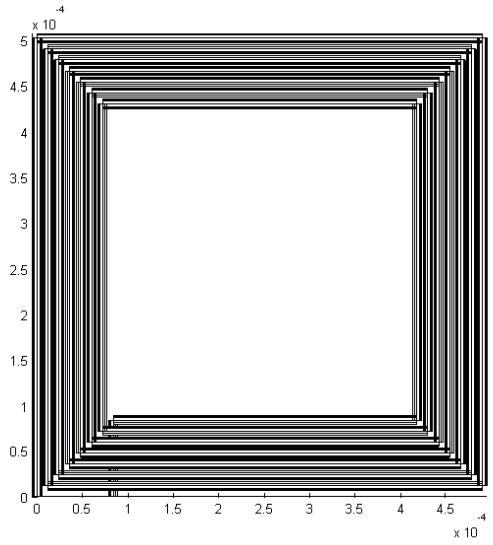
[1] X. Hu, J.H. Lee, J. White, and L. Daniel, "Analysis of full-wave conductor-system-impedance over substrate using novel integration techniques," in *Proc. of the IEEE/ACM Design Automation Conference*, June 2005.

[2] X. Hu, T.A.E. Moselhy, J. White, and L. Daniel, "Novel development of optimization-based, frequency-parameterizing basis functions for the efficient extraction of interconnect system impedance," submitted to *the IEEE/ACM Design Automation Conference*, July 2006.

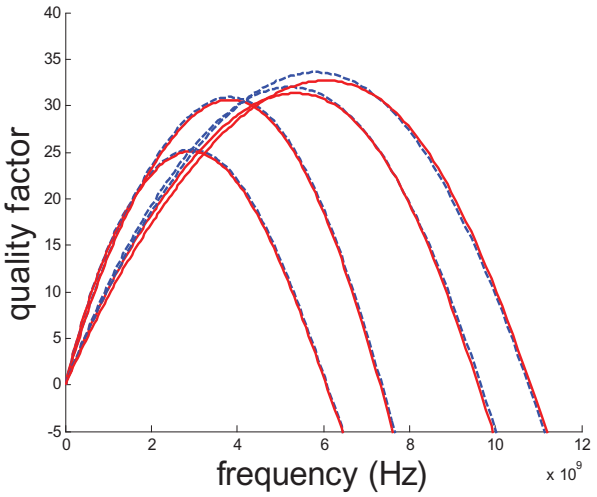
A Quasi-convex Optimization Approach to Parameterized Model-order Reduction

K.C. Sou, L. Daniel, A. Megretski
Sponsorship: MARCO GSRC, SRC, NSF

This work proposes an optimization-based model-order-reduction (MOR) framework. The method involves setting up a quasi-convex program that explicitly minimizes a relaxation of the optimal H-infinity norm MOR problem. The method generates guaranteed stable and passive reduced models and it is very flexible in imposing additional constraints. The proposed optimization approach is also extended to the parameterized model reduction problem (PMOR). The proposed method is compared to existing moment-matching and optimization-based MOR methods in several examples. For example, a 32nd order parameterized reduced model has been constructed for a 7-turn RF inductor with substrate (infinite order) and the error-of-quality factor matching was less than 5% for all design parameter values of interest.



▲ Figure 1: A 7-turn RF inductor for which a parameterized (with respect to wire width and wire separation) reduced model has been constructed.



▲ Figure 2: Matching of quality factor of 7-turn RF inductor when wire width = 16.5 μm, wire separation = 1, 5, 18, and 20 μm. Blue dash line: Full model. Red solid line: ROM.

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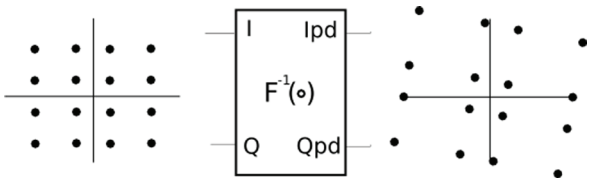
RF PA Linearization: Open-loop Digital Predistortion Using Cartesian Feedback for Adaptive PA Characterization

J.W. Holloway, S. Chung, J. Huang, J.L. Dawson
Sponsorship: MARCO C2S2

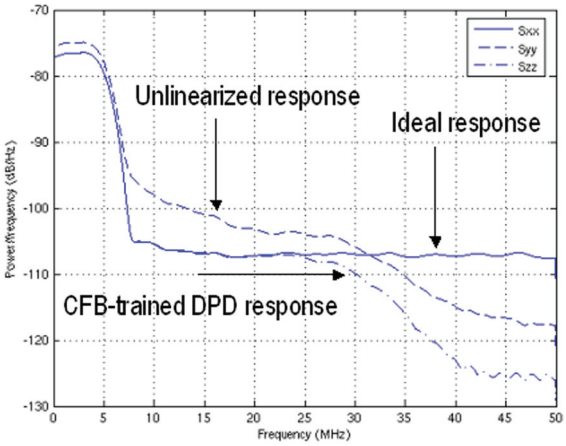
This work combines the advantages of two different RF power amplifier (PA) linearization techniques: digital predistortion (DPD) and Cartesian feedback (CFB). Cartesian feedback, an extension of classical continuous-time feedback, is limited by the bandwidth of its loop transfer function; this bandwidth, in turn, puts an upper limit on the bandwidth of the data input. However, this limitation gives one the ability to continuously linearize the PA without extensive knowledge of the PA characteristics [1].

Digital predistortion is an inherently open-loop technique and thus does not suffer from bandwidth limitations. This technique requires detailed modeling or characterization of the PA to produce the new, distorted baseband symbols [2].

One can use CFB to characterize the PA over the input symbol constellation, creating a digital lookup table (Figure 1) to be used for open-loop DPD [3]. Behavioral simulations have shown substantial improvement in PA output spectrum (Figure 2) and ACPR. These advantages can be had for little increase in power or die area. In addition, techniques to speed training time are being investigated (i.e., describing the tradeoff between accuracy in the lookup table and the speed at which the table is produced). Moreover, the DPD scheme used is much less computationally intensive than most adaptive digital predistortion schemes in the literature [2].



▲ Figure 1: A schematic representation of the CFB-created lookup table, showing a simple IQ constellation distortion due to a nonlinear PA.



▲ Figure 2: Results from a behavioral simulation of the CFB-trained DPD system showing improved linearity.

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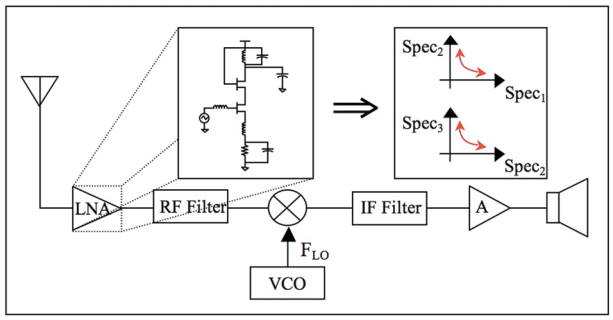
Convex Optimization of Integrated Systems Using Geometric Programming

T. Khanna, R. Sredojevic, J.L. Dawson, V. Stojanović
Sponsorship: MIT Lincoln Laboratory Advanced Concepts Committee

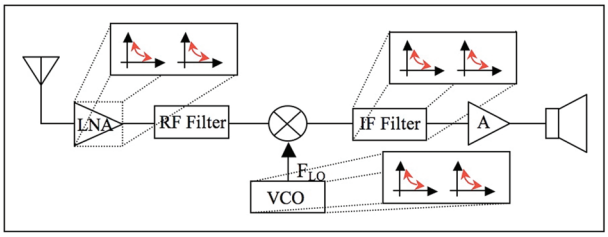
In system design, allocation of circuit resources, like power and noise budgets, is a problem with an often unclear solution and it results in long negotiations between both circuit and system designers. It is difficult to know the optimal distribution or even the feasible set of distributions of resources. This uncertainty results in an iterative approach with frequent re-design of circuit blocks for different distribution schemes. Insight into the trade-offs among resources within each circuit block can aid in finding optimal distribution and eliminate the need for re-design, ultimately speeding up the design cycle.

Thus far, work done in analog circuit optimization has applied convex optimization techniques, specifically geometric programming (GP), in order to formulate and solve for optimality. Geometric programming is convenient because there is a specific formulation that can efficiently be solved [1]. We plan to follow the style of past circuit optimization attempts [2 – 4] but reformulate them in our more general hierarchical approach to optimize a fully integrated system.

With a hierarchical optimization, GP is used to formulate and optimize each circuit block in a given system. We stress that formulation is not trivial and requires circuit design experience for correctness. From this optimization, we create trade-off curves describing the performance specifications. In other words, the trade-off curves are a continuous representation of the design space for each block. The generated trade-off curves are then related in the system formulation to produce optimal performance criteria foroptimal system design. Figures 1 and 2 show this optimization flow can be seen. We also anticipate that a hierarchical approach will allow for an interchange of block topologies, which has not been allowed in the past.



▲ Figure 1: Using a given topology, circuit performance trade-off curves are generated.



▲ Figure 2: System optimization for performance specifications. Circuit blocks are abstracted into trade-off curves, and performance specifications are optimized.

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High-Resolution, Pipelined Analog-to-Digital Conversion Using Comparator-Based Switched-Capacitor Techniques

L. Brooks, H.-S. Lee
Sponsorship: NSDEG Fellowship, CICS

Recently, a comparator-based switched-capacitor circuit (CBSC) design methodology was proposed [1]. CBSC replaces op-amps with comparators and current sources and offers many advantages. This research seeks to realize several of these advantages with the application to high resolution pipelined analog-to-digital converters (ADC). The specific goal is to design and fabricate a 12-bit, 1-GHz, 100-mW ADC. This type of ADC has applications such as software radio, general test equipment, wide bandwidth modems, smart radios for wireless communications, advanced radar systems, multi-beam adaptive digital beam-forming array transceivers, and anti-jam GPS receivers.

Theoretically, CBSC circuits offer more than an order of magnitude improvement in figure of merit (FOM) over traditional op-amp based pipelined ADCs. This means, for example, that for the same speed and resolution, a CBSC ADC can operate with more than an order of magnitude lower power consumption. In switched-capacitor circuits a charge transfer phase must be realized. In an op-amp based implementation, the op-amp drives or forces the exact charge transfer via a high-gain, high-bandwidth feedback loop. In CBSC, a current source provides the charge and a comparator detects the time when the transfer is complete and turns off the current source. So where op-amps drive the charge transfer, CBSC searches for the correct charge transfer by sweeping the output over the voltage range and shutting off the current when the correct charge transfer is found. A two phase search can help to maximize the FOM. The first phase is a coarse, fast search, and the second phase is a fine, slower search over a much smaller range. The FOM advantages of CBSC come from reduced bandwidth requirements, reduced device count, reduced complexity, increased voltage range, and increased power efficient biasing.

This project is to develop and optimize innovative circuits and architectures to achieve an aggressive design goal. The work focuses on the design of into two prototype chips. First, we are fabricating a single-ended 10-bit CBSC ADC with a single-phase (coarse phase) search only. This single-phase design embodies novel techniques and requires no static current. For this reason, this implementation overcomes the FOM shortfalls of the single phase search. The goal of this chip was to focus on speed at a lower resolution. The second prototype will use the first prototype as the back-end but will add fully-differential front-end stages with an additional a fine search phase that improves the resolution to 12 bits. In addition, several channels will be time-interleaved to achieve the desired speed.

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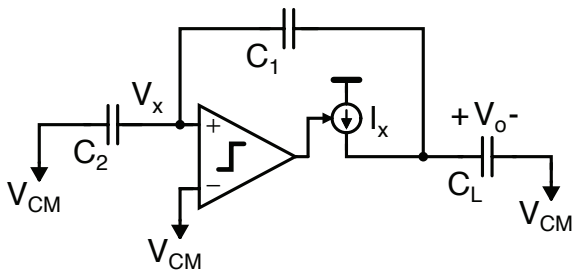
High Speed Time-Interleaved Comparator-Based Switch Capacitor ADC

A. Chow, H.-S. Lee
Sponsorship: MARCO C2S2

With an increasing need for higher data rates, both wireless applications and data links are demanding higher speed analog-to-digital converters (ADC) with medium resolution. In particular, this work will investigate ADCs with sampling rate up to 10 Gs/s with 6-8 bits of resolution. Time interleaved converters achieve their high sampling rate by placing several converters in parallel. Each individual converter, or channel, has a delayed sampling clock and operates at reduced sampling rate. The reduced sampling rate of each channel allows transistors to be biased in a more power-efficient region, thus saving on the overall use of power. Therefore each channel is responsible for digitizing a different slice. This method requires that the individual converters, which make up the parallel combination, be matched. Mismatches in non-idealities, such as gain error, timing error, and voltage offset, greatly degrade the performance of such systems. Therefore channel matching is an important design consideration for time-interleaved ADCs.

Although digital calibration can mitigate many of these non-idealities, timing mismatches is a non-linear error, which is more difficult to remove. At sampling rates up to 10 Gs/s, such complicated digital calibration would consume large amounts of power. An alternative solution uses a global switch running at the full speed of the converter to determine the sampling instance. This technique works well for medium high-speed ADC's [1-2]. At higher speeds the ability to turn the switch on and off at the full sampling rate becomes a major challenge. We will investigate whether the global clocking can function satisfactorily at a 10 Gs/s sampling rate in scaled technologies.

Power optimization is a major design consideration when implementing a time-interleaved ADC. If the power efficiency of the individual channels can be optimized, then the power dissipation of the entire system can be optimized. We are exploring ways to lower power consumption in high-speed ADCs with the adaptation of innovative circuit topologies. In particular, we will further investigate the use of the Comparator-Based Switch Capacitor (CBSC) for high-speed applications. This work is investigating a fast, single-slope architecture (Figure 1). The faster each channel can operate, the lower the number of channels and hence the lower the power in clock and buffer circuits. The primary emphasis is the development of highly powered efficient single-slope CBSC architecture. Since the single slope architecture is more sensitive to non-idealities such as ramp nonlinearity, we are carefully studying the sources of non-idealities and developing clever techniques to address the accuracy issues.



▲ Figure 1: One stage of a single slope CBSC based pipelined ADC.

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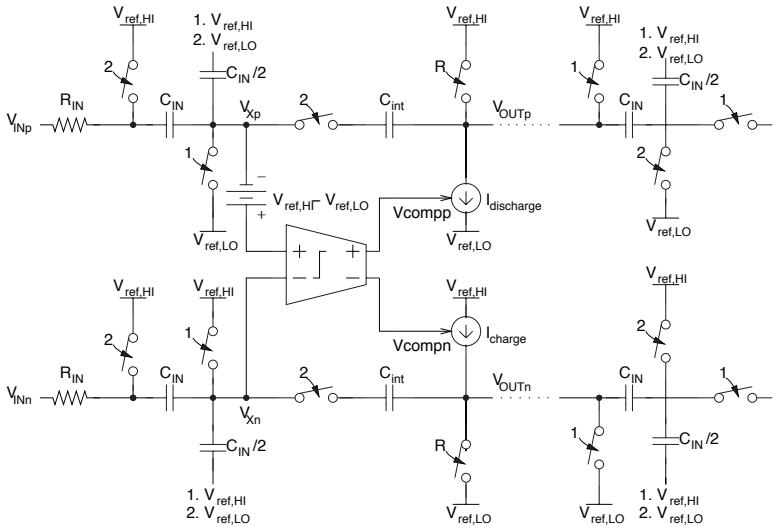
Low-Voltage Comparator-Based Switched-Capacitor Sigma-Delta ADC

M. Guyton, H.-S. Lee
Sponsorship: CICS

Many analog signal processing circuits use operational amplifiers (op-amps) in a negative feedback topology. Error in these feedback systems is inversely proportional to the gain of the op-amp. Because scaled CMOS technologies use smaller channel lengths and require lower power supply voltages, it becomes more difficult to implement high gain op-amps. Recently, a comparator-based switched-capacitor (CBSC) technique was proposed [1] that uses a comparator rather than an op-amp to implement switched-capacitor topologies. One of the biggest challenges of low voltage circuits is the transmission gates that must pass the signal. If the signal is near the middle of the power supply range, neither the NMOS nor the PMOS transistor has sufficient gate drive to pass the signal properly. The switched-op-amp technique [2] was proposed to mitigate this problem. In this technique, the output of the op-amp is directly connected to the next sampling capacitor without a transmission gate. During the charge transfer phase, the op-amp is switched off, and the output is grounded.

Much like the standard switched-capacitor technique, CBSC circuits use two-phase clocking, having both sampling and evaluation clock phases. Unlike a standard switched-capacitor circuit, in a CBSC circuit all current sources connected to the output node are off at the end of the evaluation phase. Thus, the CBSC technique is inherently better suited to low-voltage applications than switched-op-amp circuit topologies. Although the previous CBSC implementation was a single-ended version, many high-resolution systems require fully differential implementation for better power supply and substrate noise rejection properties. Since the CBSC is a new technique without an op-amp, existing fully differential circuitry cannot be applied. In this program, we are developing fully-differential CBSC topologies for applications in high resolution data conversion. Figure 1 shows a fully-differential low-voltage CBSC integrator stage using the combined techniques. We recently designed a fourth-order sigma-delta ADC for operation at 1-V power supply using this integrator stage.



▲ Figure 1: Fully-differential comparator-based switched-capacitor integrator. The input of the next integrator stage is also shown. Common-mode feedback circuits are not shown.

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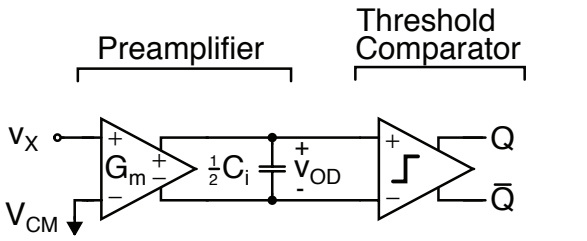
Noise Analysis of Threshold Detection Comparators

T. Sepke, J.K. Fiorenza, P. Holloway, C.G. Sodini, H.-S. Lee
Sponsorship: MARCO C2S2, CICS

Recently, a comparator-based switched-capacitor circuit (CBSC) design methodology was proposed [1]. A fundamental limitation to the accuracy of CBSC systems is the noise of the threshold-detection comparator. Unlike traditional clocked comparators that compare voltages at a specific point in time, the virtual ground threshold-detection comparators must detect the time a voltage ramp crosses the virtual ground condition and open the output sampling switch. Threshold-detection comparators are usually thought of as a wide-bandwidth, high-gain amplifier, possibly implemented as a cascade of low-gain amplifiers. The first stage of the cascaded amplifier typically dominates the input-referred noise power spectral density. Due to the rather large noise bandwidth of the cascaded amplifiers, the input referred noise of such a comparator can be quite large.

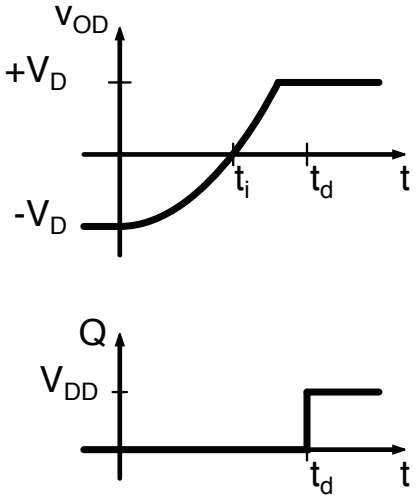


▲ Figure 1: Threshold detection comparator with ideal band-limiting preamplifier to lower the input-referred noise of the threshold detection comparator.

One possible method for lowering the input-referred noise of the comparator is to add a preamplifier as shown in Figure 1. The noise of the comparator is improved if the preamplifier has a lower input-referred noise than the threshold-detection comparator alone and if the preamplifier has enough gain to dominate the input-referred noise of the comparator.

In linear small-signal amplifiers, the frequency of the transfer function poles determines speed. However, in preamplifiers for threshold-detection comparators, the time it takes the output to reach a threshold voltage determines speed because the preamplifier does not require small-signal steady-state conditions. If the band-limiting preamplifier output is always clamped to the same voltage for the same load capacitance and transconductance, the preamplifier with the highest gain is the fastest to a given output threshold [2]. Intuitively, a band-limiting stage should be lower noise than a broadband stage, but care must be taken in applying knowledge of small-signal amplifier noise behavior to systems that do not necessarily reach steady state. A non-stationary noise analysis for the preamplifier shows that the noise bandwidth of an ideal band-limiting preamplifier is inversely proportional to twice the time it takes the preamplifier to transition from its clamped state to the comparator threshold (Figure 2).

To measure and verify the noise analysis and modeling of the threshold detection comparator, the prototype CBSC pipeline ADC in [1] is being used. Because the converter was implemented as a cascade of identical stages, the total input-referred noise of the ADC less the kT/C noise of the input sampler is proportional to the comparator noise. Therefore, a spectral analysis of the converter output codes is a measure of the comparator noise.



▲ Figure 2: Threshold-detection comparator timing showing preamplifier noise integration time ti that determines the preamplifier noise bandwidth. Total comparator delay is t_d.

REFERENCES

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Massively Parallel ADC with Self-Calibration

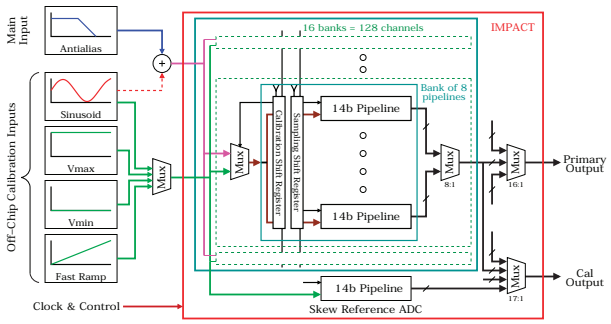
M. Spaeth, H.-S. Lee
Sponsorship: CICS

In this program we are developing an analog-to-digital converter (ADC), which can quantize a wideband 150-MHz signal at 600 mega-samples per second, with signal-to-noise ratio and linearity in excess of 75 dB (12 bits). Use of a massively parallel, time-interleaved architecture, with 128 active ADC channels, reduces the requisite speed for each channel, and enables the devices to be biased in the sub-threshold region for an extremely low-power (<50mW, core) solution. In a parallel time-interleaved system, any mismatches between channels result in undesired spurious tones. Most existing time-interleaved ADCs employ either a low degree of parallelism, such that the tones appear outside the signal band, or are low enough in resolution that the tones are below the quantization noise floor. In this design, however, all inherent gain, offset, and timing skew mismatches must be calibrated away to achieve the stated high-performance goals.

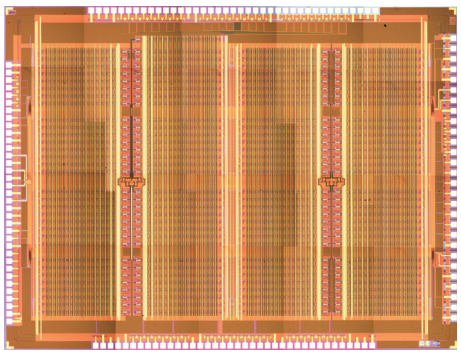
The 128 14-bit pipeline ADCs are arranged into 16 blocks of 8 channels each, as shown in Figure 1. The hierarchal organization of the design allows individual blocks to be pulled out for background calibration, while the remaining blocks continue to quantize the input signal. Due to the large number of channels to be calibrated, the calibration algorithm must be simple, but effective. The sub-radix-2 calibration algorithm [1] is very effective in removing offset and linearity errors but poses a challenge due to the complexity when applied to the massively parallel converter. We have modified the algorithm to allow nominal radix-2 operations to be employed, for similar calibration efficiency with reduced complexity. Also, we are exploring several innovative techniques to calculate and remove systematic timing skew between channels. An additional channel is included in the design to act as a timing reference for some of the timing skew measurement algorithms. A novel token-passing control scheme is used to generate local clock phases for the individual blocks and channels, minimizing the number of clock lines that must be routed across the chip.

The design was fabricated in a 0.18-µm digital CMOS process by National Semiconductor and is currently under test.

A micrograph of the finished chip is shown in Figure 2.



▲ Figure 1: Top-level block diagram of the IMPACT ADC architecture.



▲ Figure 2: Micrograph of the fabricated chip.

REFERENCES

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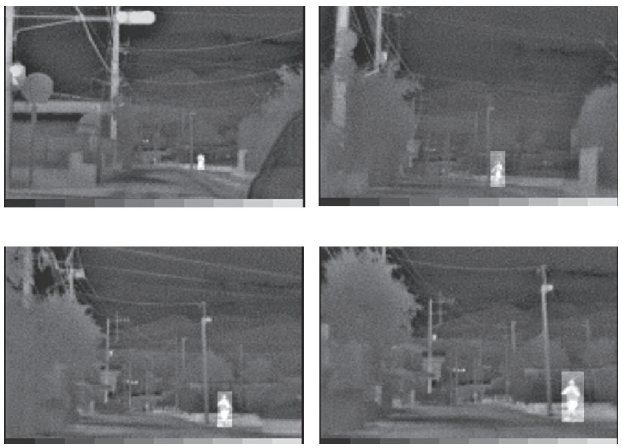
Intelligent Night-Vision Human Detection System

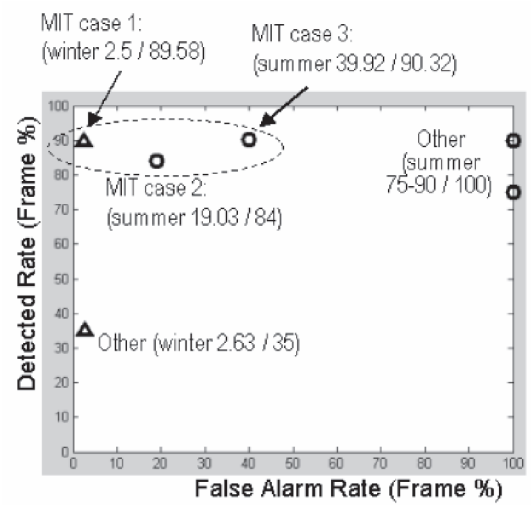
Y. Fang, I. Masaki, B.K.P. Horn
Sponsorship: Intelligent Transportation Research Center

Our objective is to apply machine vision techniques to develop a new generation of night-vision systems with intelligent human detection and identification functions. Currently, more and more infrared-based night-vision systems are mounted on the vehicles to enhance drivers' visual ability. Such mounting does allow drivers to see better, but it also introduces new safety concerns. A driver needs to switch their attention between the windshield and a separate infrared-display screen. Specifically for senior drivers, it is still difficult to identify any abnormal scenario or potential danger in its early stage. For safety purposes, an intelligent human detection and identification system based on infrared-video sequences is expected to automatically track pedestrians' location and to detect any potential dangers based on the targets' action in a monitored environment.

Compared with conventional shape-based pedestrian detection, our new "shape-independent"detection methods include the following two innovations. First, we propose an original "horizontal-first, vertical-second" segmentation scheme that divides infrared images into several vertical image stripes and then searches for pedestrians only within these image stripes. Second, we have defined unique new shape-independent multi-dimensional classification features. We demonstrated both the similarities of these features among pedestrian image regions with different poses and the differences of these features between pedestrian and non-pedestrian regions of interest (ROI). Our preliminary test results (as shown in Figure 1, Figure 2) based on limited sample images were very encouraging in terms of reliability and accuracy when our algorithms are applied to detect pedestrians with arbitrary poses. Our overall goal is to design systems for future transportation systems to make driving safer and less stressful for all travelers regardless of age and ability.



▲ Figure 1: Four pedestrian-detection results in a sequence.



▲ Figure 2: Preliminary results with limited samples.

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Vision-Based System for Occupancy and Posture Analysis

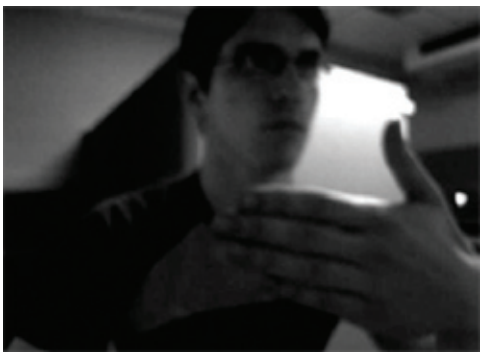
M. Farrell, I. Masaki, B.K.P. Horn
Sponsorship: Intelligent Transportation Research Center

Over the past few years, advances in computer vision have given hope for robust systems for safety applications in cars. In particular, we seek to develop a way to deploy a passenger-side airbag that is aware of the occupant in the passenger seat. The use of such devices may help avoid extensive injury due to airbag deployment in multiple classes of passengers; babies, children, adults.

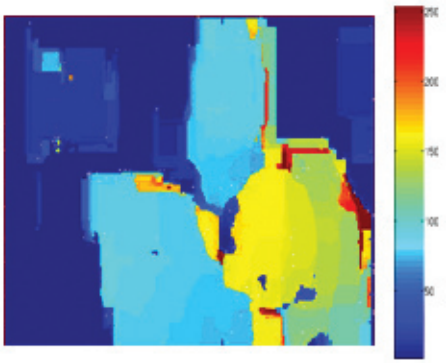
Our approach is to use a combination of two computer vision methods: invisible structured lighting and correlation-based stereo matching. The environment of an automobile poses challenges for these methods. Computer vision relies heavily on intensity values to function properly, and the interior environment of a car has many different lighting conditions. To get around this caveat the monochrome cameras cut light below 850 nm. This filtering on the cameras reduces our consideration of illumination values to near infrared and produces a monochrome image of the target.

Structured lighting improves texture on the passenger seat and further constrains the depth of the target [1]. By projecting a sine-wave grating onto the scene with stripes of random width we are ensured greater accuracy. Then, using correlation-based window-matching, as well as brightness values in each image we avoid "phase ambiguity" when determining which pixel belongs to a specific stripe in each image. The method just described eliminates this problem or poor depth resolution when using unstructured lighting.

Stereo matching uses a correlation window that is applied to the "reference" image and scans the other image in the stereo pair for a matching brightness [3]. The correlation window achieves its best results when it is larger than the largest stripe in the image. This constraint on window size avoids the problem of areas in the disparity map where we can lose depth information due to a window that is too small. For a good treatment of a correlation window based matching see [3].



▲ Figure 1: Example of a source target used to obtain depth maps, as in Figure 2. Image was taken with near -infrared sensitivity and no visible light cuts.



▲ Figure 2: Example of disparity map obtained from two-frame stereo matching under structured lighting. The correlation window size is 32 x 32 pixels with maximum disparity of 60 pixels. Brighter colors imply a short distance to the camera and darker colors imply the opposite. Values are in pixels and indicate disparity.

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Techniques for Low-jitter Clock Multiplication

B. Helal, M.H. Perrott
Sponsorship: MARCO C2S2 (partial)

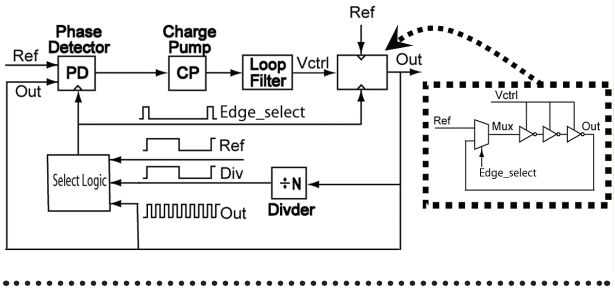
High-frequency clocks are essential to high-speed digital and wireless applications. The performance of such clocks is measured by the amount of jitter, or phase noise, their outputs exhibit. Phase-locked loops (PLLs) are typically used to generate high-frequency clocks. However, a major disadvantage of PLLs is the accumulation of jitter within their voltage controlled oscillators (VCOs) [1]. Multiplying delay-locked loops (MDLLs) have been developed in recent years to drastically reduce the problem of jitter accumulation in PLLs [2].

Jitter accumulation is reduced in an MDLL by resetting the circulating edge in its ring oscillator using a clean edge from the reference signal. The Select-logic circuitry commands the multiplexer, using the Edge_select signal, to pass the reference edge instead of the output edge at the proper time, as shown in Figure 1.

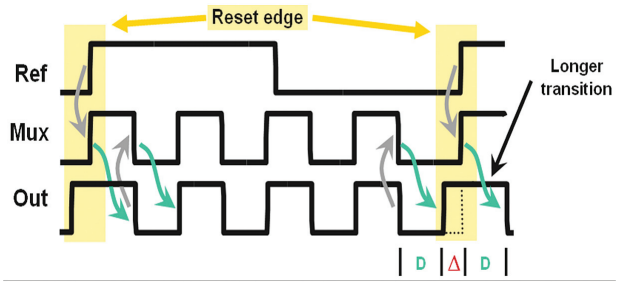
The major drawback of a typical MDLL is that it suffers from static delay offset, which causes its output to exhibit deterministic jitter. Static delay offset is caused mostly by phase offset in the phase detector and by various device mismatches. Figure 2 illustrates the problem of static delay offset in a locked MDLL, showing a deterministic jitter of Δ seconds peak-to-peak.

The goal of this research is to develop a technique that detects and cancels static delay offset in MDLLs, thereby allowing their use in applications that require low-jitter, high-frequency clocks. Behavioral simulations were used to validate the feasibility of the technique and a test chip implementing the proposed approach will be fabricated using National Semiconductors' 0.18-μm process.

We acknowledge National Semiconductor for providing the fabrication services.



▲ Figure 1: MDLL block diagram.



▲ Figure 2: Timing diagram illustrating the problem of static delay offset. Transition time, D seconds, is less than ideal, causing the transition of Out, after the edge reset, to be longer by Δ seconds.

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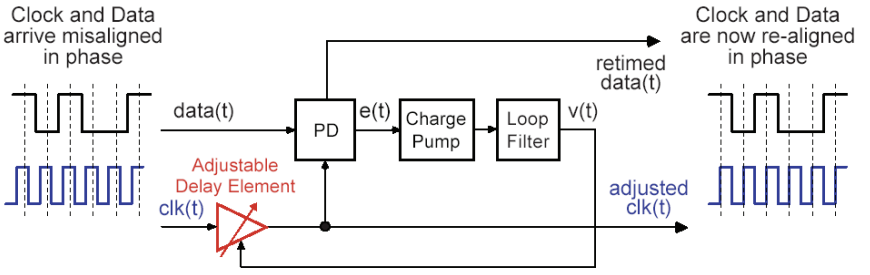
Advanced Delay-locked Loop Architecture for Chip-to-Chip Communication

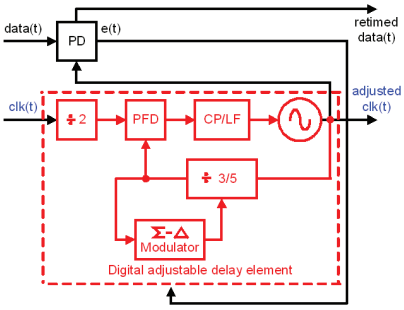
C.-M. Hsu, M.H. Perrott
Sponsorship: MARCO C2S2

A challenging component in high-speed data links is the clock and data recovery circuit (CDR). Two primary functions of a CDR are to extract the clock corresponding to the input data and then to resample the input data. The conventional technique uses a phase-locked loop (PLL) to tune the frequency and phase of a voltage-controlled oscillator (VCO) to match that of the input data. In some applications, such as chip-to-chip communication, a reference clock that is perfectly matched in frequency to the signal sequence is available. However, the clock and data signals are often mismatched in phase due to different propagation delays on the PC board. In such cases, using a delay-locked loop (DLL), as shown in Figure 1, instead of a PLL allows for much simpler design, since only a phase adjustment is necessary [1].

The aim of this research is to develop advanced DLL architectures for chip-to-chip communication. In order to provide a fine-resolution and wide-range delay, a digital adjustable delay element consisting of a sigma-delta fractional-N frequency synthesizer is proposed, as shown in Figure 2 [2]. This new architecture also provides low-sensitivity to process, temperature, and voltage variations compared to conventional techniques using analog adjustable delay elements, as shown in Figure 1. In addition, a new sigma-delta modulator architecture is proposed to provide a compact design with reasonable power dissipation.



▲ Figure 1: DLL-based data recovery circuit with an analog adjustable delay element.



▲ Figure 2: Proposed DLL-based data recovery circuit with digital adjustable element.

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Digital Techniques for the Linearization of RF Transmitters

K. Johnson, M.H. Perrott

Linear and power-efficient transmitters improve mobile communications systems. In a mobile device the power consumption of the transmitter directly affects the battery life of the device. Hence, it is desirable to operate the transmitter at the highest efficiency possible. However, nonlinearity causing distortion and spectral re-growth increases at higher drive levels. Specifications limiting distortion and spectral re-growth force the transmitter to operate at a back-off from the optimal efficiency.

Improving the linearity of the transmitter reduces the required back-off and increases the overall efficiency. Linearization techniques exist for a variety of transmit architectures: IQ modulation, linear amplification using non-linear components (LINC), and envelope elimination and restoration. They all require an additional high linearity analog down-conversion path, increasing the complexity of the transmitter. The more sophisticated algorithms require extensive DSP, limiting the application to more expensive solutions.

We propose a highly digital, algorithmically simple linearization technique suitable for mobile devices with limited DSP capability. The highly digital down-conversion architecture reduces the complexity and chip area cost of the down-conversion path. In combination a simple DSP algorithm takes advantage of a priori architectural information to estimate the transmitter transfer function.

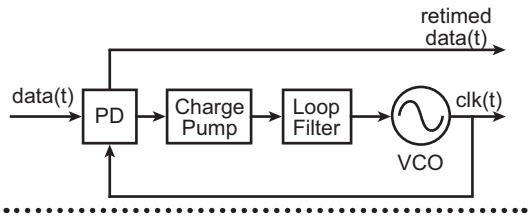
Techniques for Highly Digital Implementation of Clock and Data Recovery Circuits

C. Lau, M.H. Perrott
Sponsorship: MARCO C2S2

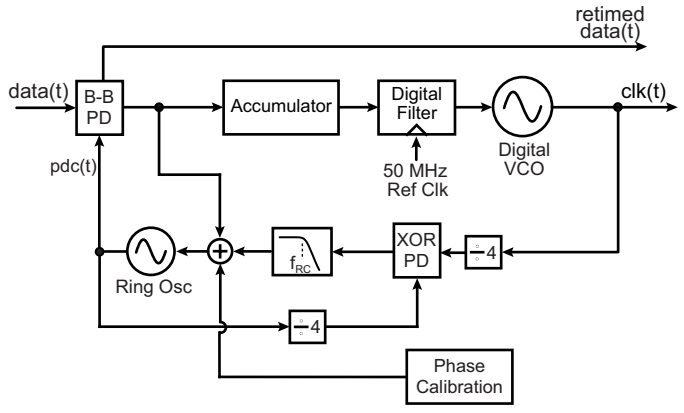
Clock and data recovery (CDR) is a critical function in high-speed digital communication systems. Data received in these systems are asynchronous and noisy, so they must be properly recovered. The CDR circuits must also satisfy stringent specifications defined by communication standards such as the SONET specification. Other desirable performance metrics, such as fast acquisition time, must also be considered.

A conventional CDR, as shown in Figure 1, employs a phase-locked loop with analog components including a phase detector, charge pump, loop filter, and a voltage-controlled oscillator (VCO). Although this analog implementation works well in most current applications, we have already started to see its limitations, as with the scaling of CMOS fabrication technology. For example, this analog system relies on low-leakage capacitors to hold values when the phased-locked loop is locked. The input of the VCO must be held stable in order to minimize frequency drift and jitter in the recovered clock. However, the leakage problem is becoming more significant as CMOS technology process continues to scale.

In view of this problem, we propose a highly digital CDR circuit that leverages digital circuits to achieve high performance; specifically, the circuit achieves fast acquisition and low-jitter performance. As shown in Figure 2, we use a bang-bang phase detector to generate error pulses of fixed width, which are then directly treated as digital signal in the subsequent digital blocks in the major loop. In this way, we can preserve the digital nature in the control path to the VCO, thus alleviating the need for high-performance, low-leakage analog components. We also utilize a simple analog feedback loop to linearize the nonlinear dynamics of the bang-bang phase detector. Simulation results show that the achievable recovered clock jitter is around 2ps RMS and verify that this architecture meets the OC-48 SONET specification. This design is being designed in the 0.18-μm CMOS process.



▲ Figure 1: A conventional CDR architecture.



▲ Figure 2: The proposed digital CDR architecture.

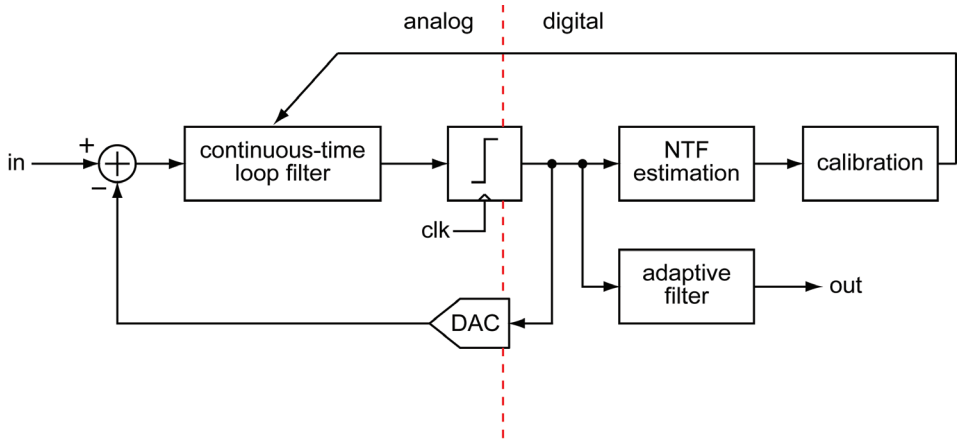
Digital Implementation and Calibration Technique for High-speed Continuous-time Sigma-Delta A/D Converters

M. Park, M.H. Perrott
Sponsorship: MARCO C2S2, Applied Materials

A/D converters are essential building blocks for many applications. Mobile communication devices require low cost, low power, and high performance A/D converters. A sigma-delta A/D converter is often chosen for wireless applications because high resolution and wide bandwidth are achievable by increasing the oversampling ratio and designing the appropriate loop filter. High oversampling ratio is relatively easy to achieve through state-of-the-art digital technology. However, implementing a low power discrete-time loop filter is challenging as the sampling-frequency increases. Therefore, a continuous-time sigma-delta A/D converter is better for a mobile application than a discrete-time counterpart because of its low power consumption.

Device mismatch is a serious issue for a continuous-time loop filter, however. Since the mismatch of passive and active elements directly degrades the performance, calibration or compensation is necessary to implement a high resolution and wide bandwidth A/D converter. In this work, we propose implementing an automatic calibration and compensation technique for a continuous-time loop filter. The proposed architecture is shown in Figure 1.

The core technique is an algorithm that estimates the values of individual components of the loop filter. The spectrum of the output digital signal from the sigma-delta converter contains the quantization noise that is shaped by a noise transfer function, which can be estimated by system identification techniques. A DSP building block is designed to evaluate the parameters of passive and active elements from the estimated noise transfer function. Then, a feedback loop calibrates the passive and active elements. The adaptive digital filter is also employed to deal with non-ideality, which cannot be calibrated due to the limitation of the technology such as finite rising or falling time of signal.



▲ Figure 1: Continuous-time sigma-delta A/D converter using digital calibration and compensation.

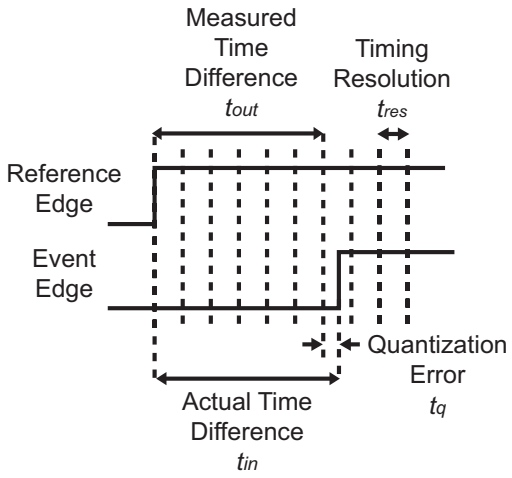
High-performance Time-to-Digital Conversion and Applications

M. Straayer, M.H. Perrott
Sponsorship: Lincoln Laboratory

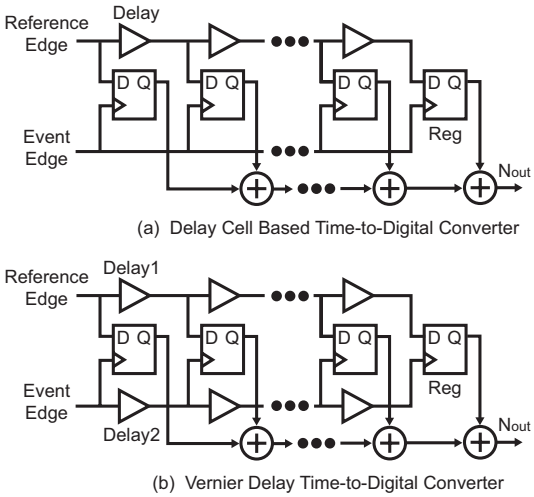
Time-to-digital converter (TDC) structures are used to quantify time information of a signal event with respect to a reference event. Traditionally, TDCs have found application in experimental physics and laser range-finding. More recently, fully integrated TDCs have attracted significant commercial interest as a core building block for a variety of clocking and phase-locked loop systems and applications [1]. The basic operation of a TDC is shown in Figure 1.

When a TDC is used in closed-loop feedback such as a phase-locked loop (PLL), the resolution of the TDC can limit the noise performance of the system. A simple TDC implementation with digital circuits has a resolution limited to a single inverter delay, shown in Figure 2(a). More intricate and involved circuit techniques such as Vernier delay lines [2], illustrated in Figure 2(b), achieve more precision, but at the expense of design complexity. This research aims to improve the overall resolution of a TDC with simple and elegant circuit techniques.

The authors wish to acknowledge MIT Lincoln Laboratory for research support through the Lincoln Scholars Program.



▲ Figure 1: Basic time-to-digital converter functionality.



▲ Figure 2: Common time-to-digital converter implementations.

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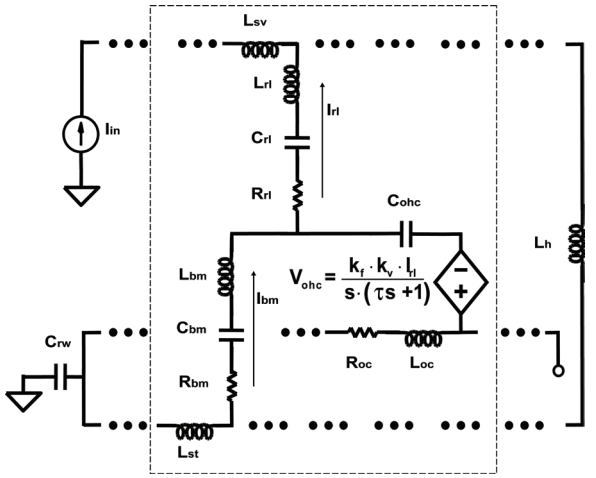
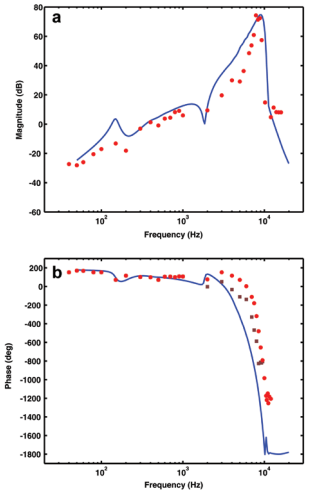
Fast Cochlear Amplification with Slow Outer Hair Cells

T.K. Lu, S. Zhak, P. Dallos, R. Sarpeshkar
Sponsorship: NSF, David and Lucille Packard Foundation, ONR, Howard Hughes Medical Institute

In mammalian cochleas, outer hair cells (OHCs) produce mechanical amplification over the entire audio-frequency range (up to 100 kHz). Under the "somatic electromotility" theory, mechano-electrical transduction modulates the OHC transmembrane potential, driving an OHC mechanical response that generates cycle-by-cycle mechanical amplification. Yet, though the OHC motor responds up to at least 70 kHz, the OHC membrane RC time constant (in vitro upper limit ~1000 Hz) reduces the potential driving the motor at high frequencies. Thus, the mechanism for high-frequency amplification with slow OHCs has been a two-decade-long mystery. Previous models that fit experimental data incorporated slow OHCs but did not explain how the OHC time constant limitation was overcome. Our key contribution is showing that negative feedback due to organ-of-Corti functional anatomy with adequate OHC gain significantly extends closed-loop system bandwidth and increases resonant gain [1]. Figure 1 shows our macromechanical model of the cochlea. The OHCs implement negative feedback by exerting a corrective force on the reticular lamina (designated "rl" in Figure 1) that opposes changes to the system output caused by changes in the input stimuli. Our model produces realistic results (Figure 2) and demonstrates that the OHC gain-bandwidth product, not just bandwidth, determines whether high-frequency amplification is possible. Due to the cochlea's collective traveling-wave architecture, the gain of a single OHC needs not be great. The OHC piezoelectricity increases the effectiveness of negative feedback but is not essential for amplification. Thus, emergent closed-loop network dynamics differ significantly from open-loop component dynamics, a generally important principle in complex biological systems.



▲ Figure 1: Macromechanical model of the cochlea composed of local micromechanical sections coupled by fluid. The local micromechanical section is enclosed in the dotted box and is repeated consecutively to simulate the traveling-wave response of the cochlea to input stimuli (I_{in}). Standard electrical representation of acoustic analogs was used for simulations. The dependent voltage source is the OHC-force generator with an RC time constant.



▲ Figure 2: Results from simulation of the macromechanical model of the cochlea composed of local micromechanical sections coupled by fluid. (a) Basilar-membrane (BM)-to-stapes-velocity ratio from the model at section 320 (*solid line, blue*) compares favorably with experimental chinchilla data [2] (*red circles*). Volume velocity to linear velocity conversion is 62.7 dB. (b) Phase response from the model matches experimental results [2] (*red circles*, *brown squares*). Note that the experimental phase data shows "the full range of variation in BM phase data" [2] and is not drawn from the same animal as the magnitude data in (a).

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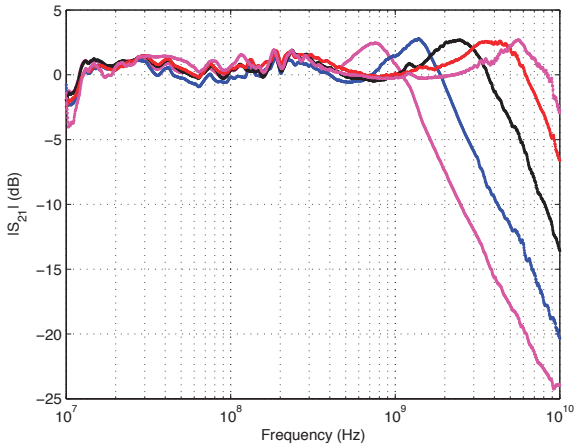
Circuits for an RF Cochlea

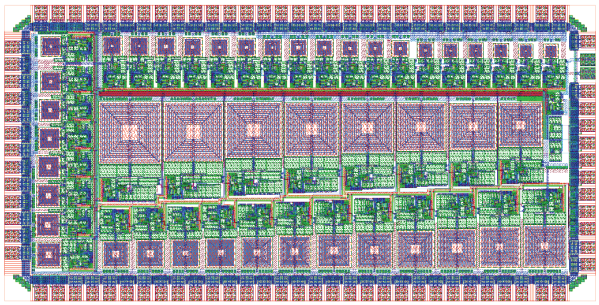
S. Mandal, S. Zhak, R. Sarpeshkar
Sponsorship: NSF, Center for Bits and Atoms

The RF cochlea uses ideas from the biological cochlea and extends them into RF for performing fast, broadband, low-power spectrum analysis [3, 4]. We have designed and built the first RF cochlea on silicon. Our inspiration, the biological cochlea, is a sophisticated signal processing system that acts as a traveling-wave spectrum analyzer. In healthy humans, it has 120 dB of input-referred dynamic range and consumes only about 14 μW of power [1]. The cochlea spatially separates frequency components in incoming sound signals, thereby performing a frequency-to-place transformation. High (or low) frequencies excite peak responses towards the beginning (or end) of the structure.

Electrically, the cochlea can be modeled as an active, nonlinear transmission line with properties that scale exponentially with position [2]. Nonlinear behavior is important in the biological cochlea, particularly for spectral masking and gain control. We have developed a simplified cochlear model that consists of a cascade of unidirectional lowpass filters with exponentially decreasing cutoff frequencies (see Figures 1 and 2). There are several advantages of such a biologically-inspired system. Firstly, exponentially tapered traveling-wave architectures like the cochlea are more hardware-efficient than banks of bandpass filters for performing spectral analysis [1]. As a result, they are simpler and faster than conventional spectral analysis techniques with comparable resolution. Secondly, the RF cochlea has inherently higher dynamic range than audio-frequency silicon cochleas, mainly because integrated passive inductors can be used at RF. Active inductors, which produce Q^2 times as much noise as passive inductors with the same quality factor Q, must be used at audio. Finally, the RF cochlea is a complex signal-processing system that uses collective computation to reduce power consumption and improve dynamic range. It allows us to explore the design, calibration, and control of large systems with many interacting components.



▲ Figure 1: Measured frequency response of five individual cochlear stages with center frequencies one octave apart. The stages were fabricated in 0.18-μm CMOS technology.



▲ Figure 2: Layout of complete RF cochlea chip, to be fabricated in 0.13-μm CMOS technology. The chip contains 46 filter stages, with center frequencies ranging from 8 GHz to 400 MHz.

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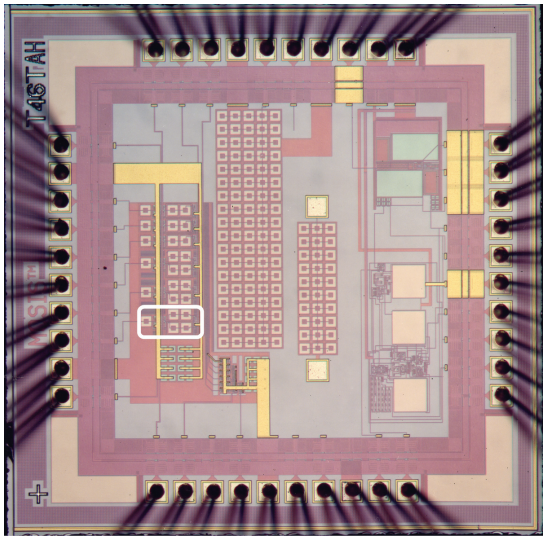
An Analog Storage Cell with 5 Electrons/sec Leakage

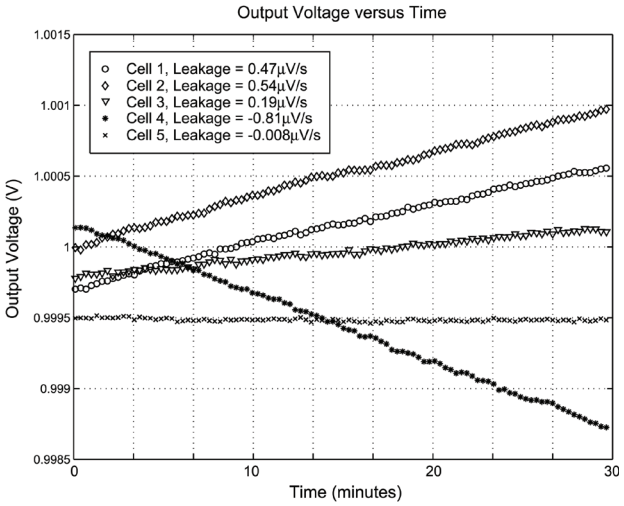
M. O'Halloran, R. Sarpeshkar

Sponsorship: Center for Bits and Atoms, NSF Research Grant, ONR, Catalyst Foundation, David and Lucille Packard Foundation, Swartz Foundation.

Medium-term analog storage offers a compact, accurate, and low-power method of implementing temporary local memory that can be useful in adaptive circuit applications. The performance of these cells is characterized by the sampling accuracy and voltage droop that can be achieved with a fixed level of die area and power. Typically, the droop rate is limited by the OFF state leakage of a single MOS switch. Past low-leakage switch designs have assumed that subthreshold conduction and drain-to-bulk diode leakage dominate other effects [1-2]. However, measurements of MOS leakage in a 1.5-µm CMOS process revealed a third important mechanism that can contribute significant leakage [3]. It was demonstrated that incorporating a novel MOS switch topology into a high-accuracy switched-capacitor storage cell can minimize all of the experimentally observed leakages, achieving 10-aA average leakage in a 1.5-µm process [3]. New experimental data from storage cells fabricated in a 0.5-µm process (see Figures 1 & 2) exhibit 0.8-aA (5e−/sec) average leakage, a 100× reduction over the leading alternative cell in the literature [2]. This implies that with a 1-pF storage capacitor and a 3.3-V supply, this cell can store a 12-bit accurate voltage for 14.5 minutes and an 8-bit accurate voltage for 3.9 hours. The leakage reduction between the 1.5-µm and 0.5-µm implementations appears to be reasonable based on simple scaling arguments [4].



▲ Figure 1: Die photograph of 0.5-µm implementation (1.5 mm × 1.5 mm). A differential analog storage cell, which exhibits 5 electrons/sec average leakage current at room temperature is circled in white.



▲ Figure 2: Leakage response of the 0.5-µm storage cells with 2.0-pF storage capacitor.

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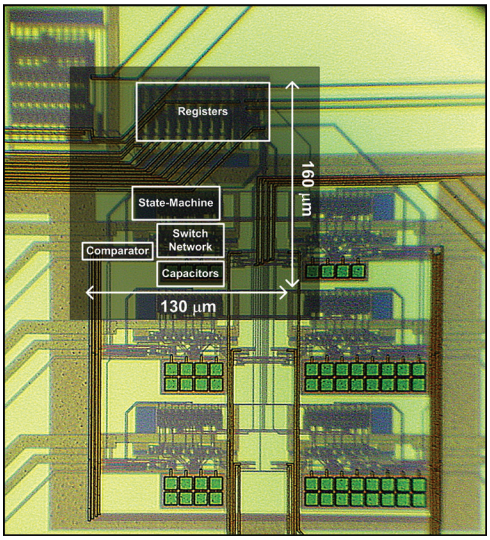
A Time-based Energy-efficient Analog-to-Digital Converter

H. Yang, R. Sarpeshkar
Sponsorship: Center for Bits and Atoms, NSF Research Grant, ONR

There is an increasing trend in several biomedical applications such as pulse-oximetry, ECG, PCG, EEG, neural recording, temperature sensing, and blood pressure for signals to be sensed in small portable wireless devices. Analog-to-digital converters for such applications need only modest precision (≤ 8-bits) and modest speed (≤ 40 kHz) but must be very energy-efficient [1-3]. Analog-to-digital converters for implanted medical devices need micropower operation to run on a small battery for decades. We present a bio-inspired analog-to-digital converter that uses successive integrate-and-fire operations such as spiking neurons to perform analog-to-digital conversion on its input current. The proof-of-concept design and implementation in the 0.35 μm process demonstrated very good energy-efficient operation [4]. In a 0.18-μm sub-threshold CMOS implementation, we were able to achieve 8 bits of DNL-limited precision and 7.4 bits of thermal-noise-limited precision at a 45-kHz sample rate with a total power consumption of 960 nW. The energy-efficiency of a data converter is derived from the figure-of-merit presented in [5]. This converter's net energy-efficiency of 0.12 pJ/quantization level appears to be the best reported so far. The converter is also very area-efficient (< 0.021mm^2) and can be used in applications that need several converters in parallel. Its algorithm allows easy generalization to higher-speed applications through interleaving, to performing polynomial analog computations on its input before digitization, and to direct time-to-digital conversion of event-based cardiac or neural signals.



▲ Figure 1: Die photograph of an 8-bit, 45-kHz A/D converter in the TSMC 0.18 μm process consumes 960 nW of total (analog + digital) power. The effective area is 130 μm x 160 μm (~0.021mm2).

Performance Metric	Value
Technology	MOSIS TSMC 0.18 μm
Voltage Supply	
Analog	1.2 Volts
Digital	0.75 Volts
Reference Current	80 nA
Input Current Range (w/ DC offset)	10 nA to 320 nA
Integrating Capacitor	500 fF
T_{clk}	1 μS
Sampling Rate	45 kHz
INL	≤ ±1.0 LSB [8 bits] typical
DNL	≤ ±0.5 LSB [8 bits] typical
SNR	47 dB
SFDR	51 dB
ENOB	7.4 bits
Power Dissipation	
Analog	360 nW
Digital	600 nW
Thermal Noise-Limited Energy per Quantization Level	0.12 pJ/State
Active Area	0.021 mm^2

▲ Figure 2: Summary of performance specifications.

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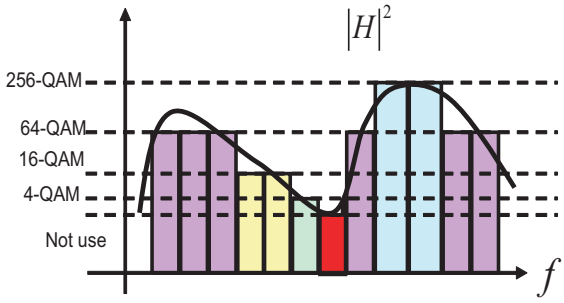
Optimization of System and Circuit Parameters in Wideband OFDM Systems

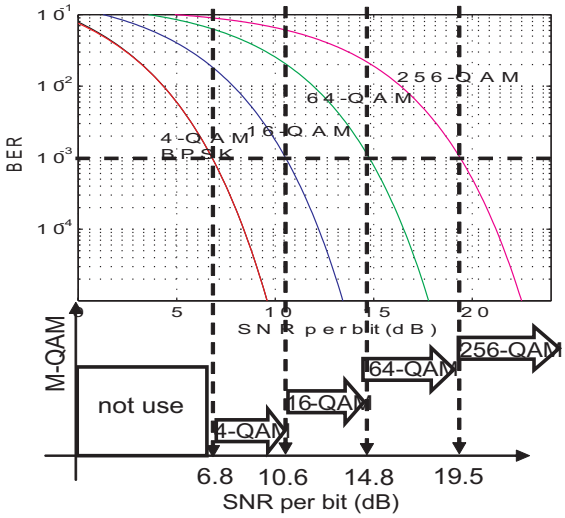
F. Edalat, C.G. Sodini
Sponsorship: NSF, Texas Instruments

In the wireless giga-bit local area network (WiGLAN) research effort, the goal is to achieve Giga-bit data rates by methods fundamentally different from the proposed IEEE 802.11n, next-generation WLAN. In other words, instead of using multiple antennas as multiplexing to increase the capacity, WiGLAN uses a much wider bandwidth (150 MHz compared to 20 MHz) and adaptive modulation per bin of a multi-carrier system. However, both systems employ orthogonal frequency division multiplexing (OFDM) to combat inter-symbol interference from multipath fading of the indoor channel and to eliminate equalization. We have simulated the WiGLAN system using CppSim [1]. The wideband characteristic of WiGLAN, while enabling high throughput, imposes several challenges. The system simulation is used as one of the initial steps to identify such challenges and to examine optimum system solutions and circuit design techniques. For instance, we are investigating various adaptive modulation techniques to choose the most appropriate one for such systems. In addition to simulation, we have implemented the transceiver's baseband processing on an FPGA (Xilinx Virtex 4) to examine the implementation practicality and performance of the adaptive modulation algorithms in the real wireless environment using our test-bed WiGLAN nodes.

In such multi-carrier systems with a frequency-selective channel, higher capacity can be obtained by adapting modulation of each bin to the channel response over its band (Figure 1). The modulation per bin is selected (Figure 2) based on the estimated signal-to-noise ratio (SNR) per bin at the input of detector at the receiver and the target bit-error-rate (BER) of the overall system performance. In addition to achieving higher capacity, since adaptive modulation is based on SNR per bin independent of other bins, it can avoid interference and as a result enable co-existence of two or more wireless systems.



▲ Figure 1: Adaptive modulation per bin in WiGLAN based on the channel response over each bin. The modulation scheme is chosen from 4-, 16-, 64-, and 256-rectangular QAM modulations.



▲ Figure 2: How the Adaptive modulation algorithm dictates the modulation scheme for each bin in WiGLAN.

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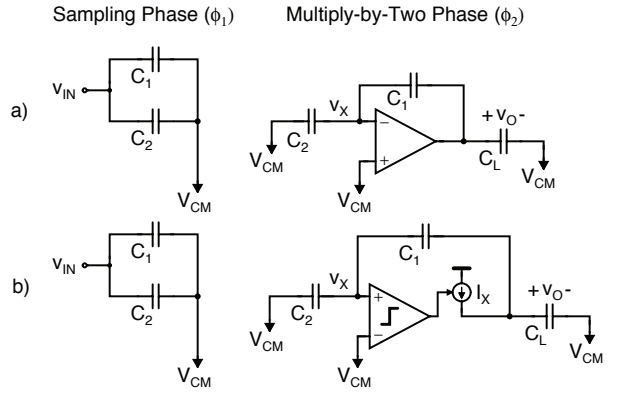
Comparator-based Switched-capacitor Circuits (CBSC)

J.K. Fiorenza, T. Sepke, P. Holloway, H.-S. Lee, C.G. Sodini
Sponsorship: MARCO C2S2, CICS

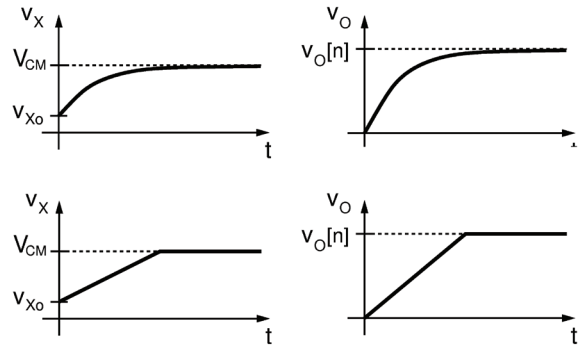
Two side effects of technology scaling that have a significant impact on analog circuit design are the reduced signal swing and the decrease in intrinsic device gain. Gain is important in feedback-based, analog signal processing systems because it determines the accuracy of the output value. Cascoded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swings of scaled technologies. An alternative method for achieving high gain in an operational amplifier without reducing signal swing is to cascade several lower gain amplifiers. Nested-Miller compensation approaches can be used to stabilize the cascaded feedback system, but the frequency response of the closed loop system is significantly sacrificed to ensure stability. In this project [1-2], we explore a new comparator based switched capacitor (CBSC) circuit design methodology that eliminates the use of op-amps in sampled data systems

A sampled-data system typically operates in two phases, a sampling phase (ϕ1) and a charge transfer phase (ϕ2). An important property of these systems is that the output voltage needs to be accurate only at the moment the output is sampled. No constraint is placed on how the stage gets to the final output value. Feedback systems use a high-gain operational amplifier to force a virtual ground condition at the op-amp input. The top circuit in Figure 1a shows the conventional op-amp-based switched-capacitor gain stage. The circuit in Figure 1b shows the proposed CBSC approach, where a comparator and a current source have replaced the op-amp. Assuming the comparator input v_X starts below the common-mode voltage at v_Xo, the current source charges the output circuit until the comparator detects the virtual ground condition and turns the current source off. At this instant, the output is sampled on C_L. Because the CBSC design ensures the same virtual ground condition as the op-amp based design, both circuits produce the same output value at the sampling instant. This property of the CBSC technique is demonstrated by the waveforms for the two circuits shown in Figure 2.

The CBSC concept is general and can be applied to any sampled-data analog circuit. For example, the CBSC design approach can be applied to a pipelined ADC. A prototype 1.5-b/stage CBSC pipeline ADC was constructed and operates similarly to the op-amp version of the ADC. The prototype CBSC ADC was implemented in a 0.18-µm CMOS technology. The active die area of the ADC is 1.2 mm^2. At a 7.9 MHz sampling frequency, the DNL is +0.33/-0.28 LSB, and the INL is +1.59/-1.13 LSB. Its ADC achieves an SFDR of 62 dB, an SNDR of 53 dB, and an ENOB o f 8.7 b for input frequencies up to the Nyquist rate. The core ADC power consumption of all 10 stages of the pipeline converter is 2.5mW at a 1.8V power supply, resulting in a 0.8 pJ/b figure of merit.



▲ Figure 1: (a) Traditional op-amp-based multiply-by-two amplifier versus (b) proposed comparator-based multiply-by-two amplifier.



▲ Figure 2: Multiply-by-two waveforms.

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[2] J.K. Fiorenza, T. Sepke, C.G. Sodini, P. Holloway, and H.-S. Lee, "Comparator-based switched capacitor circuits for scaled CMOS technologies," *IEEE Journal of Solid-State Circuits*, Dec. 2006, to be published.

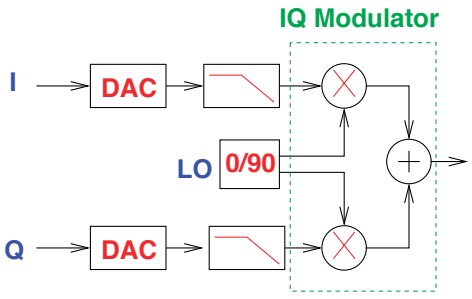
A Wideband ΔΣ Digital-RF Modulator

A. Jerng, C.G. Sodini
Sponsorship: CICS

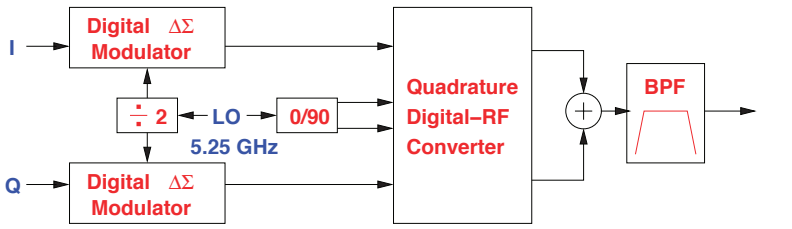
This research focuses on the implementation of a direct digital-RF transmitter for use in the wireless gigabit local area network (WiGLAN) system that is capable of providing a throughput of 1 Gb/s in the 5.15 – 5.35 GHz U-NII bands. This architecture takes advantage of digital process scaling trends by replacing high dynamic range analog circuits with digital circuits. In the conventional IQ transmitter depicted in Figure 1, the I and Q signal paths from the DAC to the output of the analog mixer must maintain noise and distortion to levels satisfying the required dynamic range of the system. As the baseband signal bandwidth increases, the analog reconstruction filter consumes more power for the same dynamic range. DAC accuracy becomes degraded by dynamic errors at high frequencies rather than static DC errors. Furthermore, as transistors continue to scale and supply voltages continue to decrease, it becomes more challenging to design high dynamic range analog circuits over a wide bandwidth.

Direct digital modulation of an RF carrier can eliminate the DAC, reconstruction filter, and analog mixer, resulting in power and area savings. Luschas [1] introduced the RF DAC, which combines a conventional DAC and mixer into one stage. The RF DAC uses one of the high-frequency Nyquist images of the DAC as an RF output. We further develop this concept by modulating an RF carrier using digitally controlled RF phase shifters. In this way, the output power is concentrated at the RF carrier frequency, rather than at DC and at Nyquist image frequencies. Oversampling ΔΣ concepts are applied to convert digital baseband data into a bitstream of +/- 1s, corresponding to phase shifts of 0˚ and 180˚. A 2-level RF phase selector can then be implemented using differential signaling and simple CMOS switches. By applying quadrature RF and baseband components to the phase selectors, we create a quadrature digital modulator capable of arbitrary I,Q modulation, as shown in Figure 2. As the noise-shaping transfer function (NTF) of the baseband ΔΣ modulators push their quantization noise outside the signal bandwidth, a bandpass filter at the output can remove the up-converted quantization noise, acting as an RF reconstruction filter.

The new transmitter architecture requires circuit design in both the digital and RF domains. The main challenges include designing a high-speed digital ΔΣ modulator and realizing a high-Q on-chip passive bandpass filter.



▲ Figure 1: Conventional Transmitter.



▲ Figure 2: IQ ΔΣ Digital-RF Modulator Block Diagram.

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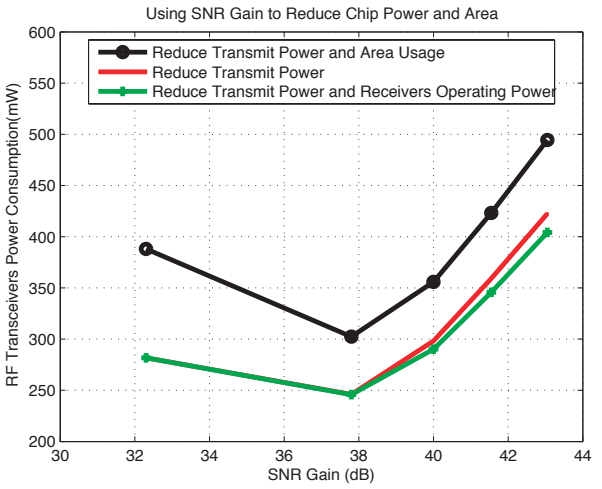
Area- and Power-Efficient Integrated Transceivers for Gigabit Wireless LAN

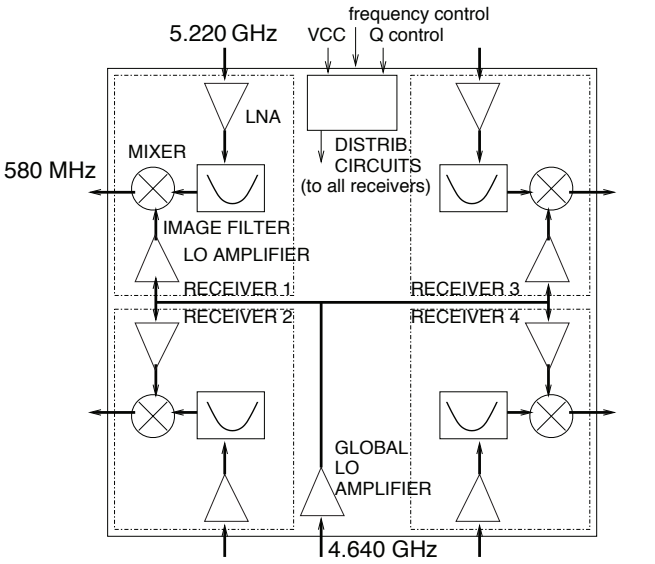
L. Khuon, C.G. Sodini
Sponsorship: MARCO C2S2, CICS

For a given transmit distance and data rate, diversity available from multiple antennas significantly decreases the signal-to-noise ratio (SNR) necessary for low bit error rate transmission. As a result, transceivers for multiple antenna systems with low transmit power, low receiver operating power, and smaller chip area become possible [1-2]. Using multiple antenna systems for wireless LAN increases both data rates and transmission distance. Reduced power and area consumptions for these systems motivate their use for portable applications and allow for a cost-effective on-chip implementation.

As shown in Figure1, the proper application of this SNR gain balances the decrease in power consumption due to a lower transmit power with the increase in power consumption due to the increase in overhead electronics. However, when overhead electronics power dominates, lowering the receivers' operating power reduces power consumption. Application of SNR gain for area-efficient circuits minimizes area consumption and also reduces power consumption to a lesser degree. An area-efficient 5.22 GHz four receivers chip, shown in Figure 2, was implemented in 0.18 μm SiGe BiCMOS. Each receiver has a low noise amplifier, Q-enhanced image reject filter, mixer, and local oscillator amplifier and distribution circuits for bias and filter tuning. The receivers dissipate 225 mW, occupy 4 mm^2, and provide 14 dB conversion gain with over 30 dB image rejection [3].



▲ Figure 1: Power consumptions for various SNR gains. Increasing the number of antennas yields SNR gains.



▲ Figure 2: The WiGLAN receivers. Each receiver includes a low noise amplifier, image reject filter, mixer, and local oscillator amplifier but shares the local oscillator and filter tuning signals and bias circuits.

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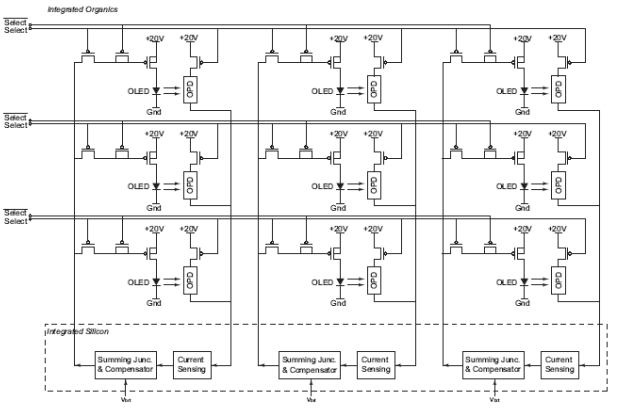
Optical-feedback OLED Display Using Integrated Organic Technology

I. Nausieda, I. Kymissis, V. Bulović, A.I. Akinwande, C.G. Sodini
Sponsorship: MARCO C2S2, MARCO MSD

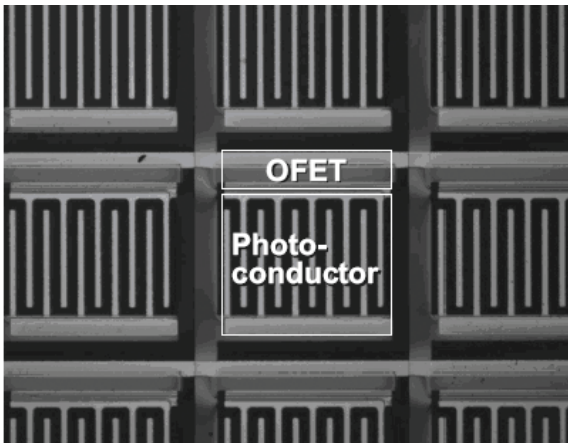
Organic light-emitting diodes (OLEDs) are a promising technology for large, thin, flexible displays. The OLEDs are emissive, thereby removing the need for a backlight and decreasing display thickness and power dissipation. Compared to typical light-valve displays, OLEDs exhibit improved contrast ratio, faster response times, and a larger color gamut. However, OLEDs possess non-linear light output characteristics, and their response drifts over time due to operational degradation. This degradation produces pixel-to-pixel variation in output characteristics, as well as decreasing the display's overall lifetime. We propose to drive OLEDs to the desired brightness using optical feedback on the pixel level. Preliminary research [1] has shown that feedback will improve the display lifetime by six to tenfold. This project aims to build a complete system that encompasses the design and fabrication of an integrated silicon control chip and an organic pixel/imaging array, which will together form a stable, usable display.

The integrated silicon control chip is composed of multiple channels, each of which contains two main blocks: the current sensing block and the feedback compensation block (Figure 1). The former is a transimpedance amplifier that converts the organic photodetector output current to a voltage. The feedback compensation block stabilizes the loop, ensuring a desirable response time and phase margin, and is implemented using a National Semiconductor .35-µm CMOS process. The organic pixel/imager array consists of organic field effect transistors (OFETs) that select and control OLED pixels and photodetectors. The OFET and photoconductor electrode arrays are fabricated using a photolithographic process [2] (Figure 2). Currently, a technique to thermal ink-jet print the organic photoconductor to save photolithographic steps is being explored.

We acknowledge National Semiconductor for providing the fabrication services.



▲ Figure 1: A sample 3 x 3 portion of the pixel/imager array. The display pixels in a row are driven simultaneously in a column-parallel architecture.



▲ Figure 2: Micrograph of photolithographically fabricated OFET select transistor and photodetector.

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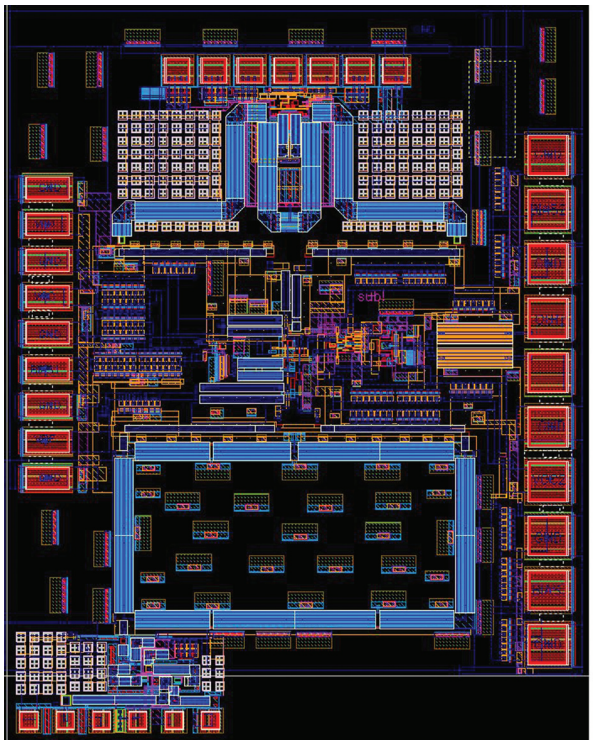
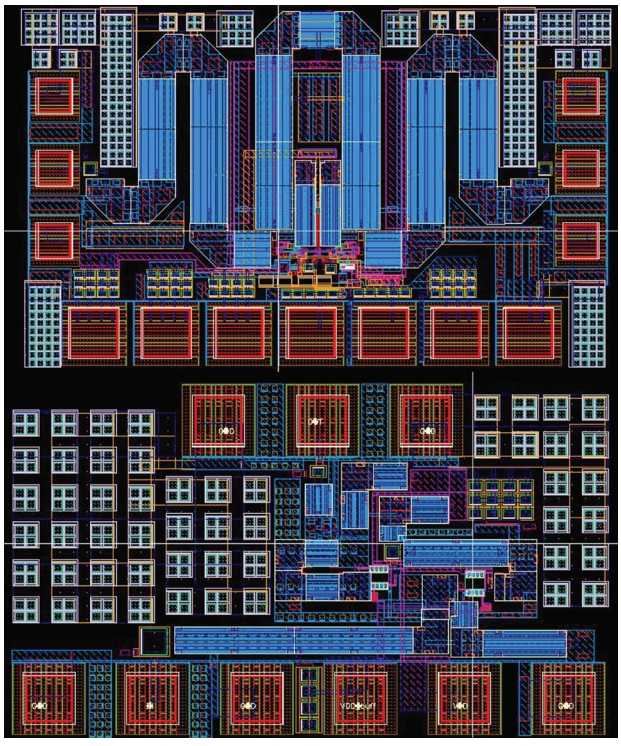
A 77-GHz Receiver for Millimeter Wave Imaging

J. Powell, K.M. Nguyen, C.G. Sodini
Sponsorship: NSF, Lincoln Laboratory

The area of millimeter-wave (MMW) integrated circuits has recently generated a great deal of interest in several applications including automotive radar, concealed weapons detection, and wireless communications in the 60-GHz industrial, scientific, medical (ISM) band. This is due, in part, to the rapid advancement of silicon germanium (SiGe) technology, which achieves oscillation frequencies (fT, fMAX) exceeding 200 GHz. [1] In this research, a 77-GHz receiver and transmitter will be designed for imaging applications including automotive radar and concealed weapons detection. Several key transceiver circuits have been designed and submitted for fabrication, including a 77-GHz two-stage LNA, VCO and a double-balanced mixer. These blocks were also assembled together as a first step toward implementing an RF receiver system (Figure 1). The LNA is expected to achieve less than 6 dB NF at 77-GHz, with a gain of 23 dB; the VCO is expected to achieve a tuning range of greater than 12%, spanning from 68-GHz to 77-GHz. The separate LNA and VCO blocks are depicted in Figure 2. The double-balanced mixer is expected to achieve a noise figure of approximately 13 dB at 77-GHz, with a conversion gain of approximately 9 dB. A 77-GHz class AB power amplifier is currently being designed for the 77-GHz transmitter.



▲ Figure 1: Layout photo of front end RX system composed of the 77-GHz LNA, VCO and Mixer. (Mixer courtesy of Helen Kim of Lincoln Laboratory.)



▲ Figure 2: VCO layout (top) and LNA layout (bottom).

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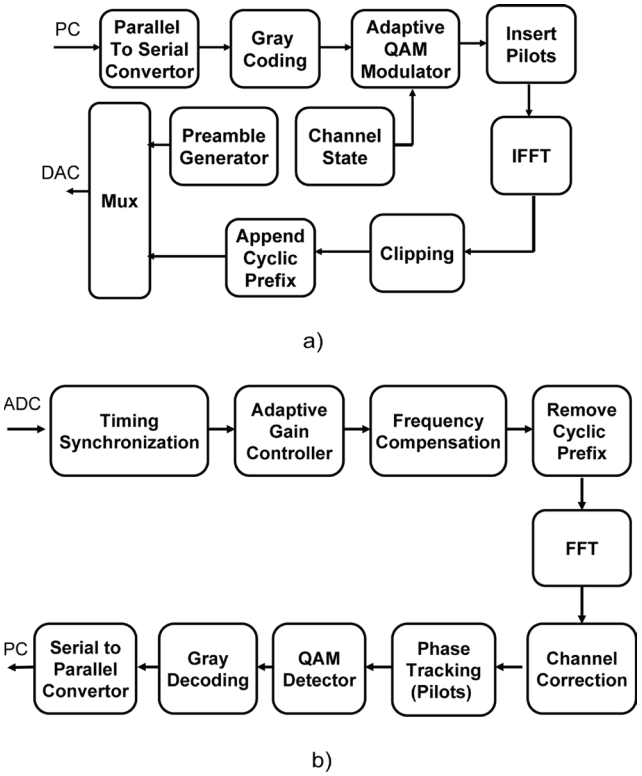
[1] B.A. Floyd, S.K. Reynolds, U. Pfeiffer, and T. Beukema, "SiGe bipolar transceiver circuits pperating at 60 GHz," *IEEE J. of Solid State Circuits*, vol. 40, no. 1, pp. 156-167, Jan. 2005.

Realization of Baseband DSP Core for the Wireless Gigabit LAN

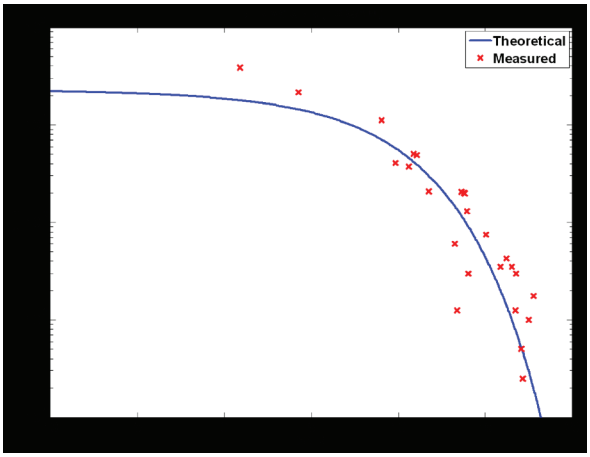
J.K. Tan, K.M. Nguyen, C.G. Sodini
Sponsorship: NSF, CICS

The wireless gigabit lan (WiGLAN) aims to achieve a high data-rate of 1 Gbps through the combination of orthogonal frequency division multiplexing (OFDM), a wide bandwidth of 128 MHz and adaptive modulation. Adaptive modulation decisions are based on the channel conditions, which stay static on the order of tens of milliseconds to a couple of seconds. Hence to demonstrate the WiGLAN concept, a baseband DSP core is implemented to adapt to the channel conditions, in real-time.

The hardware platform of choice is a field programmable gate array (FPGA). The baseband design implemented is shown in Figure 1. The DSP core is integrated with a RF front-end [1] and wireless measurements are taken. Figure 2 shows that the measured SNR/BER of each sub-carrier matches up closely to a theoretical Gaussian channel.



▲ Figure 1: OFDM with a) Transmitter and b) Receiver.



▲ Figure 2: Theoretical Curve for a 16-QAM Gaussian channel and the measured SNR/BER for each 16-QAM sub-channel.

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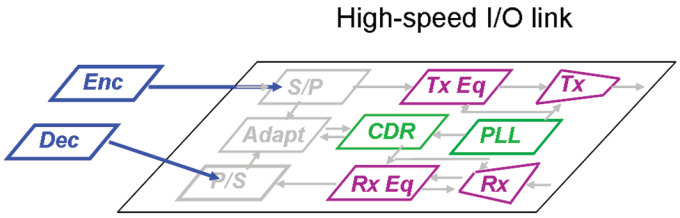
Channel-and-Circuits-Aware, Energy-Efficient Coding for High-speed Links

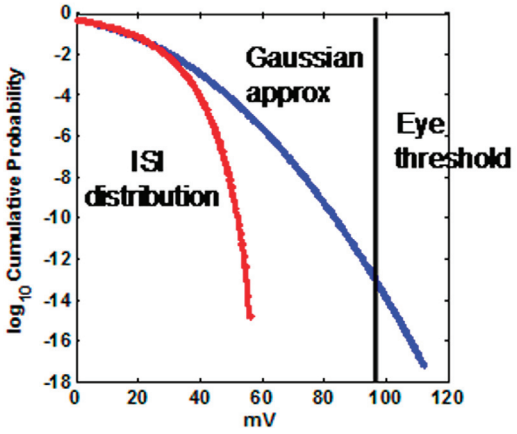
N. Blitvic, M. Lee, L. Zheng, V. Stojanović
Sponsorship: MARCO IFC

In order to achieve high throughput while satisfying energy and density constraints, both the data rates and the energy efficiency of high-speed chip-to-chip interconnects need to increase. In this project we aim to extend the link system design to incorporate energy-efficient channel coding techniques. Using novel energy-efficient coding techniques for non-Gaussian noise and residual interference, we will increase both the achievable data rates and the energy-efficiency of links by drastically off-loading the low-BER target burden and hence decreasing the complexity of the equalization/modulation level (Figure 1). Presently, both a statistical simulator and an experimental setup are being developed with the purpose of streamlining the code design process. The statistical simulator will be the first link simulator to include channel coding and the effects of data correlation. The current focus is on the modeling of the residual inter-symbol interference (ISI), but the approach will be extended to deal with cross-talk, timing jitter, and other circuit-related effects. Our recent developments have addressed the difficulty in computing ISI probability distributions for realistic channel lengths, in presence of data correlation in the form of a single parity bit. This approach is presently being extended to linear block codes.

The resulting simulator will provide the capability to model data correlation both as a plug-in for the existing analytical statistical link simulators or as the basis of time-domain behavioral link simulation software. In order to mitigate the inadequacies of analytical system models (Figure 2), limited by system complexity and link-specific noise sources, we consider advanced statistical methods based on modifications of the standard Monte Carlo technique. The generality of the Monte Carlo technique will allow us to accurately encompass the system's complexity in a behavioral time-domain framework, without resorting to overly restrictive simplifications (like linearity) necessary in the fully analytical approach. Furthermore, the sample-size reduction techniques, such as importance sampling, coupled with conditioning through our interference calculation methods, will allow us to efficiently simulate very low target BERs not reachable by standard Monte Carlo simulation. The promise of this approach lies in the large deviation theory and the theory of asymptotically efficient estimators.



▲ Figure 1: Model of the high-speed link where the decoder/encoder replaces the serializer/deserializer blocks. By relaxing the target BER, channel coding will have the benefit of lowering the energy associated with timing and equalization.



▲ Figure 2: Error incurred in modeling the link noise by additive white Gaussian noise (AWGN). As shown, the simplification can be adequate at low BER but becomes largely inaccurate by the time we reach the target BER range (~ 10^{-15}) [1].

REFERENCES

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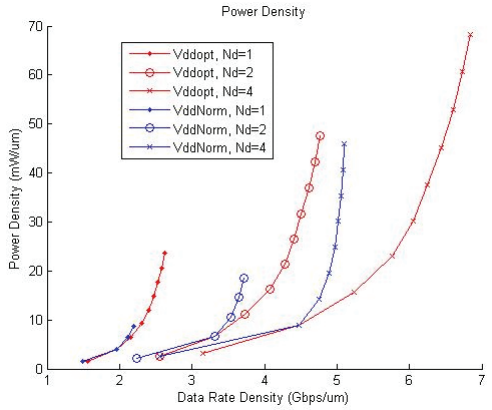
Efficiency of High-speed On-Chip Interconnect: Trade-off and Optimization

B. Kim, V. Stojanović
Sponsorship: NEC research fund

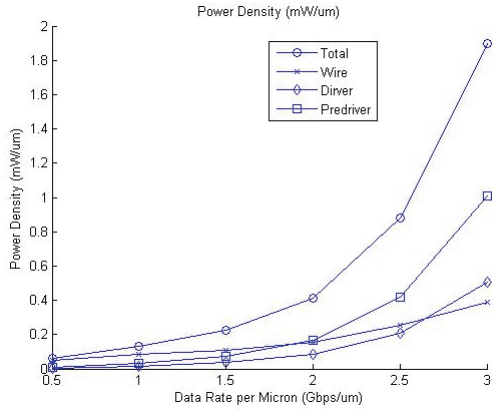
Signaling over global on-chip wires has been an increasingly difficult problem for the last several generations of VLSI technologies. As the technology scales, global wires scale poorly, causing a large increase in module-to-module communication. Traditionally, a repeater insertion [1] is used to overcome the latency problem but the power consumption of the signaling increases due to the high-speed requirement for the repeater. To address the limited latency and energy-efficiency of the repeater chains, alternative techniques such as RF-modulation [2] and pulse width modulation [3] have been suggested.

These past studies, however, have not considered the interconnect as a part of a dense on-chip network which must be optimized for the area-normalized metric such as cross-sectional throughput and power density instead of single link metric such as throughput and power consumption. Given the global constraints such as power and total die area, the designer must jointly optimize interconnect circuits and wires to find the best trade-off between energy dissipated in circuits and wires. In this project, we aim to establish a framework for analysis and comparison of various interconnect methods under a set of performance and cost metrics including bandwidth, latency, chip area, and power consumption.

Figure 1 shows power density versus data rate density of optimized repeater-inserted interconnect of predicted bulk 32-nm CMOS process model for a given target delay-to-symbol period ratio, Nd=1, 2, 4. Figure 2 shows the power density versus data rate density of optimized pulse-width modulation interconnect of the same 32-nm CMOS model. The latency of this point-to-point link is one bit time at highest data rate (equivalent to Nd=1 repeater case). The trade-off curves are calculated when all practical design parameters (such as driver size, wire width and space) are optimized to meet given performance specifications. The two figures show that the pulse width modulation is a more energy-efficient signaling method than repeater for comparable data rate density. Our analytical method also provides the information of best interconnect design for given performance specifications.



▲ Figure 1: Power density (mW/um) versus data rate density (Gbps/um) of repeater-inserted interconnect for given delay to symbol period ratios (Nd=Td/Ts=1,2,4).



▲ Figure 2: Power density (mW/um) versus data rate density (Gbps/um) of PWP with one delay to symbol period ratio (Nd ~1).

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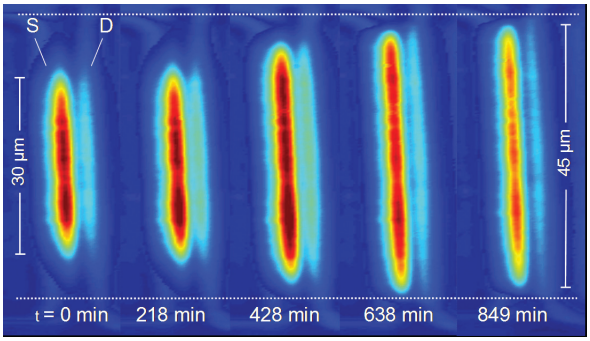
ELECTRONIC DEVICES & EMERGING TECHNOLOGIES



▲ Light-emission photographs from source and drain of PHEMT, at five points during step-stressing experiment. Taken at V_{GS}=0.3 V, V_{DS}=6.6 V. Gate width W_g = 50 µm (A.A. Villanueva, J.A. del Alamo, p. 72).

for additional reading...

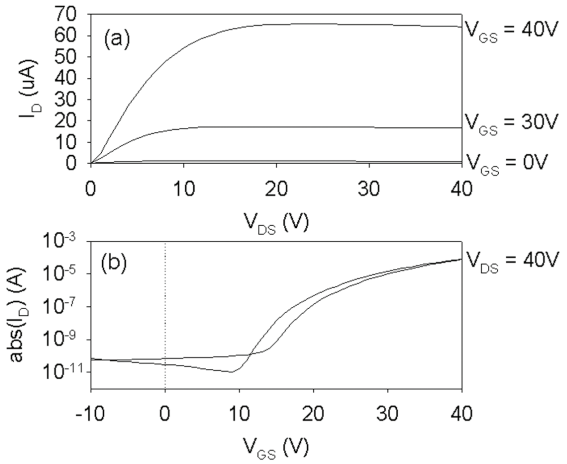
Amorphous Zinc-Oxide-Based Thin-film Transistors

A. Wang, I. Kymissis, P. Mardilovich, V. Bulovic, C.G. Sodini, A.I. Akinwande
Sponsorship: Hewlett-Packard

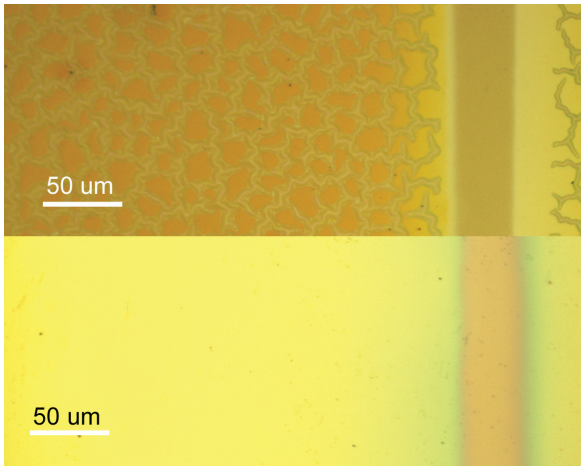
Recently, RF-sputtered zinc oxide-based field effect transisters (FETs) have been demonstrated with higher mobilities and performance than amorphous silicon, the dominant material used for display backplanes [1,2]. The low temperature processing possible for zinc oxide-based FETs [3] makes these materials compatible with flexible polymer substrates, but patterning with shadow masks limits feature size and accuracy. This project aims to develop a low-temperature, lithographic process for zinc oxide-based FETs, similar to one developed for organic FETs [4].

Our initial work focuses on two issues: determining optimal conditions for (1) growing the oxide semiconductor and (2) depositing high-quality oxide semiconductor and contact films on an organic polymer, parylene. For the former, top-contact, bottom gate ZnO FETs were fabricated on Si/SiO_2 substrates, using SiO_2 as the gate dielectric, Si as the gate, and sputtered indium-tin-oxide (ITO) as source/drain contacts. The RF sputtering power, total chamber pressure, and annealing temperatures were varied in a series of experiments; Figure 1 shows the current-voltage characteristics of a device from one set of conditions.

To determine optimal conditions for depositing high-quality films on an organic polymer, ITO films were deposited on an organic polymer dielectric, parylene, at different sputter rates. High stress in the oxide films on top of the soft organic polymer dielectric, parylene, may cause cracking and discontinuities in the film. Figure 2a shows a microscope photograph of the cracked surface of an ITO film sputtered at 80W on parylene; Figure 2b shows a continuous ITO film sputtered at 15W on parylene.



▲ Figure 1: Current-voltage output characteristics (top) and transfer characteristics (bottom) for ZnO field effect transistor sputtered at 375W in 5mTorr Ar ambient, after annealing at 300 degrees C. (W/L = 1250µm/50µm.)



▲ Figure 2: (a) Optical microscope image of cracked 1000Å ITO film on parylene sputtered at 80W. (b) Optical microscope image of smooth ITO film on parylene sputtered at 15W.

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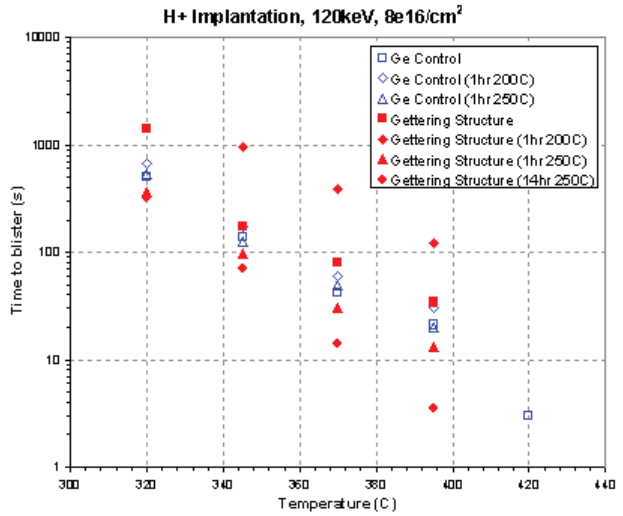
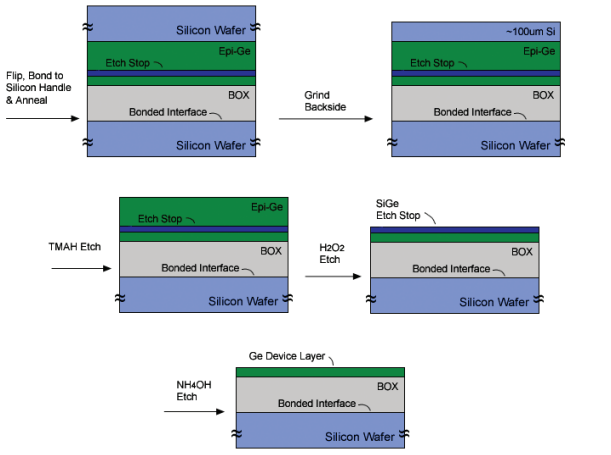
Fabrication of Germanium-on-Insulator by Means of Wafer Bonding and Layer Transfer

J. Hennessy, D.A. Antoniadis
Sponsorship: MARCO MSD

The fabrication of germanium-on-insulator (GeOI) substrates using a hydrogen-induced layer transfer technique and bulk Ge wafers is limited by the mismatch in the thermal coefficients of expansion between Ge and Si. A strained SiGe layer can be used as a hydrogen-gettering layer to attempt to lower the temperature at which the hydrogen-induced layer transfer can occur. Figure 1 illustrates the success of this gettering structure in reducing the time for surface blisters to appear in H+-implanted Ge. However, this technique does not reduce the overall temperature at which layer transfer occurs. A second technique for GeOI fabrication involves the direct epitaxial growth of Ge on a Si substrate. Using a process flow illustrated in Figure 2, a GeOI substrate is fabricated using a grind and etch-back technique. This technique eliminates the thermal mismatch between the bonded wafer pairs; by incorporating an epitaxial etch-stop layer in the transfer wafer, it may potentially allow for the fabrication of arbitrarily thin GeOI substrates.



▲ Figure 1: Blister point measurements for a strained SiGe gettering structure show a significant reduction in the time to blister for some pre-annealing conditions. No corresponding reduction in the layer-transfer temperature after wafer bonding was observed.

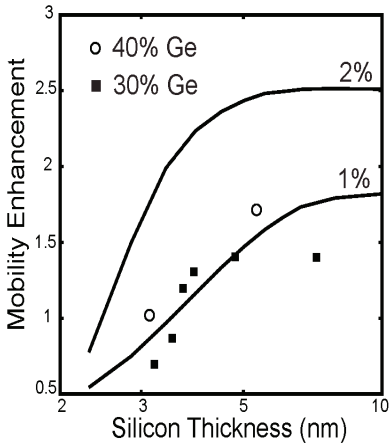


▲ Figure 2: Process flow for GeOI fabrication using epitaxially grown Ge directly on Si. A grind and etch-back technique is used instead of hydrogen-induced layer transfer.

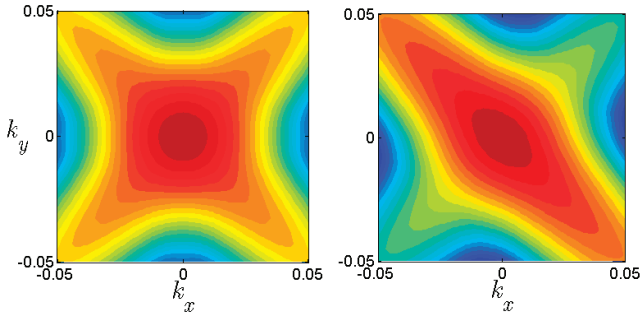
Strain Dependence of Mobility in Ultra-thin SOI and GOI

A. Khakifirooz, D.A. Antoniadis
Sponsorship: MARCO MSD

Significant enhancement of the carrier transport properties is required to continue the scaling of transistor performance. Different approaches to apply uniaxial or biaxial strain to the channel have been proposed to achieve higher mobility and drive current and some of them have been already implement in the state-of-the-art CMOS technology. Whether or not these approaches offer any benefit for ultra-thin semiconductor-on-insulator structures is a key concern. To understand how different parameters that determine the carrier mobility are affected in such atomically thin SOI and germanium-on-insulator (GOI) structures, we explore the effect of biaxial and uniaxial strain on the band structure using a $sp^3d^5s^*$ tight-binding model. As Figure 1 shows, biaxial tensile strain, which is traditionally used in bulk CMOS technology to improve both electron and hole mobility, does not provide any benefit for holes in ultra-thin SOI once the channel is thinner than 3-4 nm [1]. Biaxial tensile strain lifts the degeneracy of the light and heavy holes and preferentially populates the light holes. Carrier confinement imposed by the channel thickness or the gate voltage acts in the opposite directions, preferentially populating the heavy hole band. The net effect is that the biaxial tensile strain is less effective in enhancing the hole mobility in ultra-thin SOI compared to bulk silicon. This observation is in agreement with recent experimental results [2]. However, as illustrated in Figure 2, uniaxial compressive strain continues to provide mobility enhancement in ultra-thin SOI structures via manipulating the effective mass in the [110] channel direction. The fact that the ballistic injection velocity is also enhanced via effective mass reduction is also encouraging.



▲ Figure 1: Calculated mobility enhancement as a function of the silicon thickness for different levels of biaxial tensile strain. Measurement results [2] (symbols) are also shown for comparison. Various scattering mechanisms, including the additional confinement induced by the gate voltage, further reduce the available mobility enhancement. The results should be viewed as the upper limits of the mobility enhancement.



▲ Figure 2: Contours of constant energy vs. in plane wavenumbers for relaxed (left) and uniaxially strained (right) 2.85-nm-thick SOI structure. Uniaxial compressive strain reduces the effective mass in the [110] channel direction, thereby increasing the mobility and ballistic velocity. Uniaxial compressive stress of 1 GPa is applied in the [110] direction and the wavenumbers are in the units of $2\pi/a$, where a is the lattice constant.

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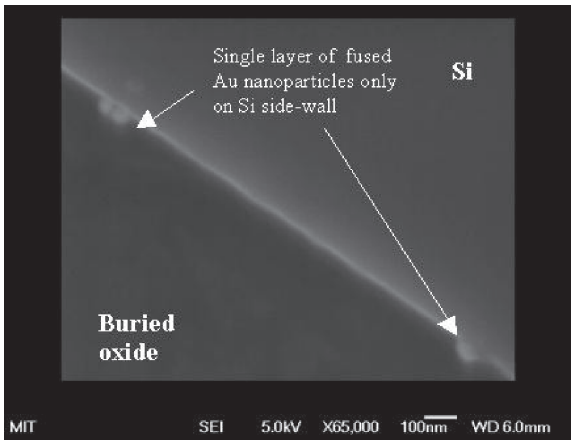
Towards MOS Memory Devices Containing 1 nm Silicon Nanoparticles

O.M. Nayfeh, D.A. Antoniadis, K. Mantey, M.H. Nayfeh (University of Illinois at Urbana-Champaign)
Sponsorship: MTL, University of Illinois at Urbana-Champaign

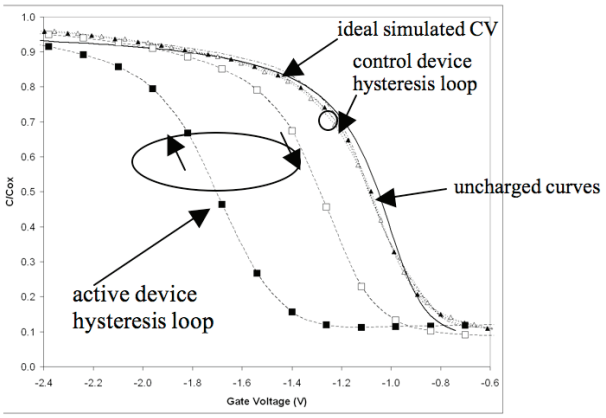
MOS devices containing *ex-situ* produced, identical (constant size), spherical, 1-nm Si nanoparticles were fabricated for use in future flash electrically erasable programmable read only memory (EEPROM) devices [1]. Device fabrication did not require changes to the standard CMOS process. The Si nanoparticles (Figure 1a), 1 nm in diameter and H-terminated, are prepared using electrochemical dispersion of device-quality Si wafers in a mixture of HF/H_2O_2 [2-3]. Figure 1b gives the schematic of the MOS capacitor device. We start with boron-doped substrates at a level of $\sim 10^{15}$ cm^{-3}. Thin, SiO_2 tunnel-oxide (~ 4.2 nm), was then grown by dry oxidation. We then spread colloidal Si nanoparticles in isoproponol (IPA) on the oxide using spin-coating. We used AFM along with ellipsometry to test uniformity and to estimate the film thickness. We used several particle colloids with decreasing molar concentration that were prepared by successive dilutions to approach sub-monolayer coatings. After the particles were spin-coat, a ~ 10-nm SiO_2 cap layer was deposited by LPCVD at 400 C^o. Thin (~500 nm) Al films were then deposited. Capacitors were defined and chemically etched and Al contact on the wafer backside was deposited. A N_2/H_2 annealing at 450 C^0 for ten minutes completed the process. Control MOS capacitors containing no particles were also fabricated using the same procedure.

The CV measurements were performed on devices fabricated with varying Si nanoparticle density. The hysteresis loops and programming characteristics exhibit well-behaved characteristics, substantial voltage shift, and long charge retention. both the rise and shape and the absence of substructure in the CV agree with similarly constructed control samples and with an ideal simulated device that assumes no interface states (Figure 2). We have tested the charge retention characteristics of several devices. We first obtained an uncharged curve at the much reduced voltage range of 0 to -0.8 V, and we then programmed the device at +7 V for ~ 40 s. We analyzed the threshold voltage shift as a function of time while holding voltage at – 0.8 V. Based on the slope of the response, we extrapolate to a retention time of several years [1].

We believe we have successfully demonstrated the incorporation of identical spherical 1 nm silicon nanoparticles in MOS devices utilizing a simple CMOS compatible process. The process allows for device optimization by control of the density of nanoparticles, where high-density could potentially achieve voltage shift of several volts.



▲ Figure 1: (a) Prototype of a 1-nm particle ($Si_{29}H_{24}$) Si (gray), H (white) . (b) The schematic of the Si nanoparticle MOS device



▲ Figure 2: Hysteresis loops of control device (triangles), active device with density 4.8 x 10^{11} cm^{-2} (squares). The uncharged curves are shown as dotted and dash-dotted; the simulated CV curve issolid. Charging Vg=+/- 7V with 40 s hold time.

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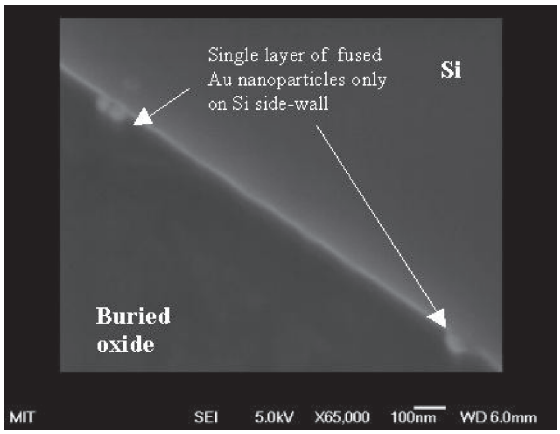
Study of Silicon Nanowire Growth for Electronics Applications

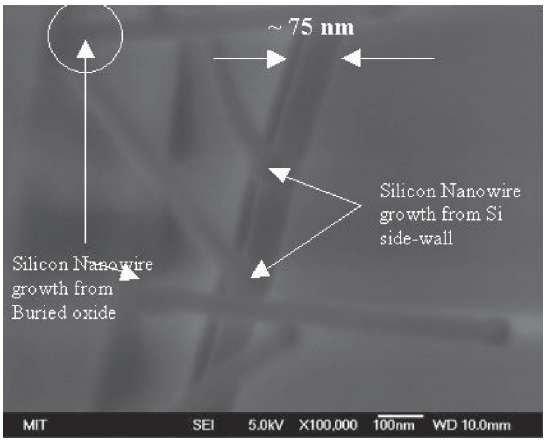
O.M. Nayfeh, S. Boles, D.A. Antoniadis, C.V. Thompson, E.A. Fitzgerald
Sponsorship: Singapore-MIT Alliance

Silicon nanowire transistors (SiNWTs) have been shown to be promising candidates for end-of roadmap devices. This potential is due to both electrostatics and transport properties. The SiNWTs gain potentially better electrostatic control, compared to planar MOSFETs, by utilizing a fully wrapped-around gate [1]. Moreover, some studies have measured higher mobilities than bulk values [2]. Silicon nanowire transistors have been fabricated by both the top-down and bottom-up methods. The top-down method employs lithography and etching to fabricate the SiNWs, whereas the bottom-up method involves the growth of the nanowires from catalyst nanoparticles. The growth from catalyst seeds most often involves the vapor-liquid-solid (VLS) growth method. In this work, we first investigated the formation of catalyst nanoparticle seeds and the growth of SiNWs via VLS growth on Si-substrates. We have successfully grown silicon nanowires from both Au nanoparticle catalysts fabricated via e-beam evaporation and dispersal of Au nanoparticles from solution. After fabrication/dispersal of nanoparticles on a Si substrate, the nanowires are grown in silane by atmospheric pressure chemical vapor deposition (APCVD) in the (500-650 C) temperature range.

We are currently working on fabricating SiNWTs by bridging silicon nanowires across an SOI microtrench [3]. Growth of bridging silicon nanowires from the thin Si sidewalls of SOI microtrenches using metal nanoparticles as catalyst is plagued by growth on all faces of the architecture, due to metal catalyst remaining on the top of the active Si layer and on the buried oxide. We developed a protocol that would allow us to selectively attach a single layer of Au nanoparticles only on the thin Si sidewalls of an SOI microtrench. SEM imaging following this procedure shows Au nanoparticles only on the thin Si sidewalls (Figure 1), which will thus enable the selective growth of bridging nanowires only from these sidewalls. Figure 2 shows an SEM image of silicon nanowire growth on a sample that did not have the Au nanoparticles removed from the buried oxide and top Si. As can be seen, growth occurs on all faces of the sample.



▲ Figure 1: SEM image demonstrating the ability to selectively attach a single layer of Au nanoparticles only on the thin Si sidewall. The nanoparticles on the buried oxide and top Si layer have been removed.



▲ Figure 2: SEM image of silicon nanowires grown on samples with Au nanoparticles remaining on the buried oxide and top Si layers. As can be seen, nanowire growth is plagued on all surfaces of the architecture due to the presence of the un-removed Au nanoparticles.

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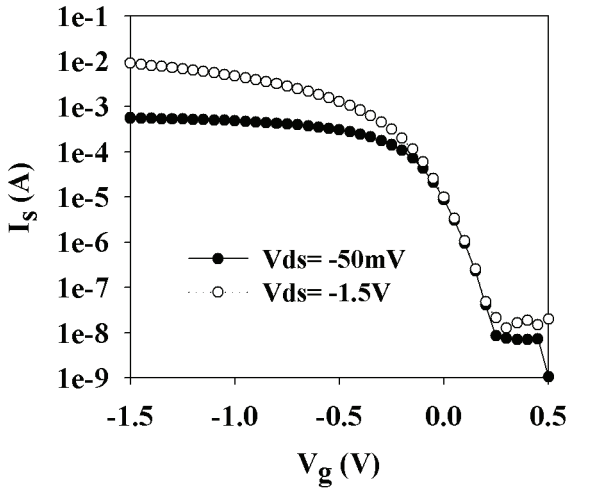
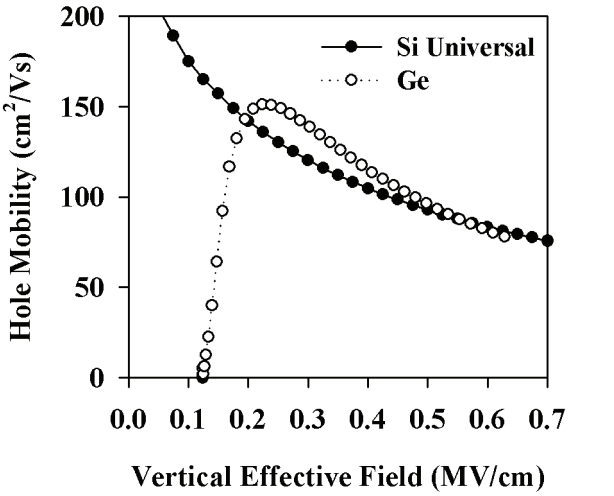
Bulk Germanium MOSFETs Using High-K Dielectrics

A. Ritenour, J. Hennessy, M.L. Lee, R.Z. Lei, E.A. Fitzgerald, D.A. Antoniadis
Sponsorship: MARCO MSD

The advent of high-k gate dielectrics provides a new opportunity to consider semiconductors other than silicon for future ultra-scaled MOSFETs. Germanium has started to receive attention because it simultaneously offers significant enhancements in bulk electron and hole mobility relative to silicon. However, the inherent instability of germanium oxide makes interface engineering particularly challenging. Metallorganic chemical vapor deposition (MOCVD) and atomic layer deposition (ALD) are being explored as options for gate stack deposition. Figure 1 shows the transfer characteristics for a germanium p-MOSFET with an ALD WN/$LaAlO_3$/AlN gate stack. Figure 2 shows the extracted hole mobility for this device. ALD gate stack deposition was performed by K. Kim and R. Gordon at Harvard University.



▲ Figure 1: Typical as-measured Is-Vg characteristics for bulk Ge p-MOSFETs with ALD WN/$LaAlO_3$/AlN gate stack.



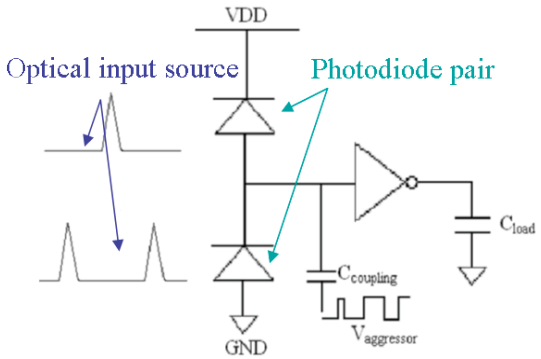
▲ Figure 2: Extracted hole mobility for Ge p-MOSFET. The universal hole mobility for silicon is shown for reference.

Variation Analysis in Optical Interconnect

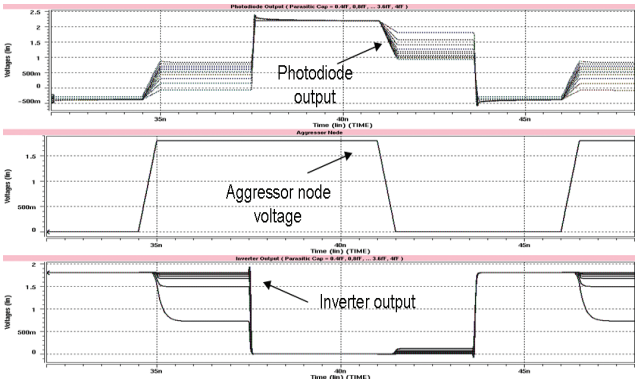
K. Balakrishnan, D.S. Boning
Sponsorship: MARCO IFC

Due to the continuous scaling of CMOS technologies and the resulting need for fast, robust, and accurate signal propagation, electrical interconnect faces many difficult challenges. Optical interconnect is emerging as a possible alternative to meet these challenges; however, the robustness issue must be examined to ensure the viability of this option. The goal of this work is to determine the variation sensitivity of an ultra-fast pulse-based optical receiver circuit [1], which serves to convert incoming optical pulses into an outgoing electrical signal. Specifically, the fast pulse-based scheme must be examined because of its potential advantages in robustness due to its use of precise, mode-locked laser source pulses as an input, which in turn reduces jitter. Particularly in the context of clock-distribution applications, the robustness of this receiver circuit is paramount. Previous work in this area focused on variation analysis in passive optical components of the signal distribution system, such as waveguides and splitters.

Current work examines the effects of different sources of variation on the output of the ultra-fast, pulse-based, optical receiver circuit shown in Figure 1. Possible sources of variation include the mismatch and variation of input power, optical input power mismatch and variation, load capacitance variation, parasitic capacitive coupling, and static and dynamic power supply noise. As an example, Figure 2 shows simulation results of the impact of parasitic capacitive coupling on the output waveform of the optical receiver circuit. Further analysis focuses on the impact of technology scaling on the robustness of the circuit. Current work also compares the optical signal distribution scheme to a traditional electrical H-tree distribution scheme in terms of variation. Possible future work in this area may concentrate on the design and implementation of test circuits to measure variations in optical interconnect.



▲ Figure 1: Ultra-fast pulse-based optical receiver circuit. Alternating short optical input pulses from a mode-locked laser source are received at the top and bottom photodiodes. These pulses are then converted to rising and falling edges, which are buffered by the static CMOS inverter and can be used as a clock signal.



▲ Figure 2: Simulation waveforms depicting the impact of parasitic capacitive coupling on the optical receiver circuit. Because the photodiode pair output is a floating node, the impact of a nearby aggressor node can be detrimental to the inverter output, given a sufficiently large coupling capacitance (~0.4 fF).

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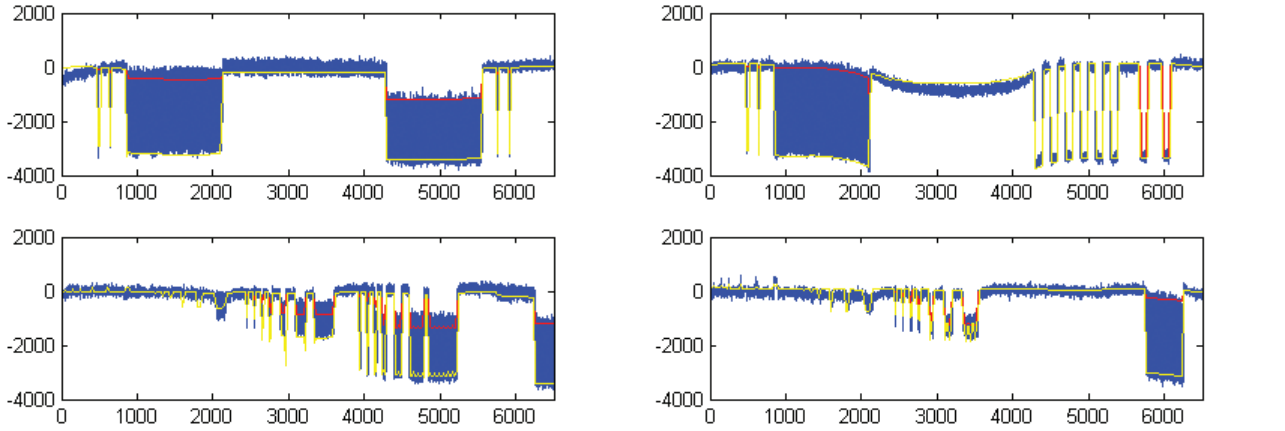
Modeling of Pattern-dependencies in the Fabrication of Multilevel Copper Metallization

H. Cai, D.S. Boning
Sponsorship: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, MagnaChip

This research aims to understand, model, and optimize the interaction between copper electroplating and chemical mechanical polishing (CMP) processes. Currently, this research focuses on the coupling that exists due to pattern-dependent topography, which propagates from the electroplated surface into CMP dishing and erosion. We propose a physics-based time-stepped copper electroplating model taking an IC chip layout as input and producing a map of copper film thickness across the chip with good predictive accuracy and reasonable computational load. In the new model, the additive surface coverage is computed by considering the evolution of the surface geometry during copper film growth and the surface dissolution/absorption processes resulting from two major additives, accelerators and suppressors. With a limited set of parameters, the simulation root-mean-square (RMS) errors of envelope and step-height have been reduced to 100-200 Å, which is comparable to the previously developed, non-time-step, semi-physical electroplating model. Figure 1 shows the simulated topography in comparison with measured data. The new framework can be seamlessly integrated with our chip-scale chemical-mechanical polishing (CMP) model [1] and extended to the multi-level copper metallization case.

The multi-level versions of the time-stepped electroplating model and the physics-based, multi-level CMP model are in progress. Current work is underway to integrate the time-stepped electroplating and CMP models, and to develop a co-optimization methodology that minimizes the thickness of the deposited copper film, process time, and consumable usage to achieve a high-performance and environmentally-friendly copper interconnect process.



▲ Figure 1: Surface height variations resulting from copper electroplating pattern dependencies. High-resolution profile scans are shown in patterned areas (blue) and the corresponding simulated topography (yellow for lower area and red for upper area) in each grid. Horizontal axis is position (in μm); vertical axis is height (in Å).

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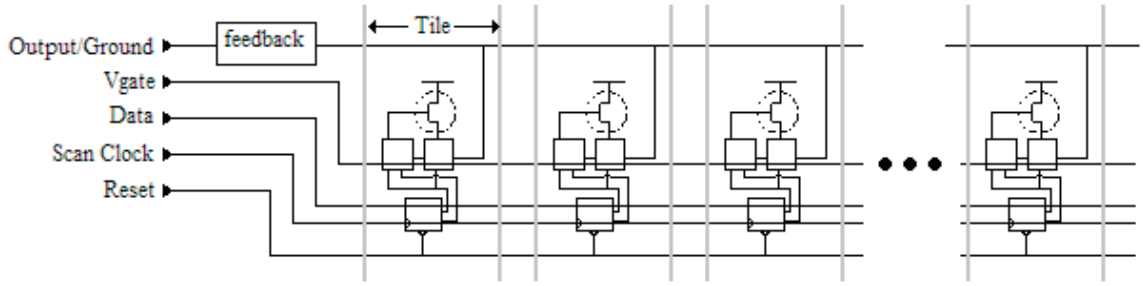
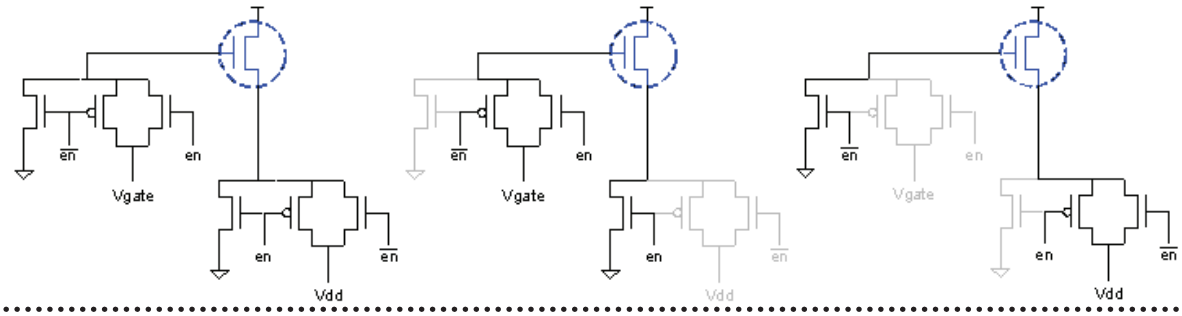
Test Circuits for Assessment of IC Variation

K.G.V. Gettings, D.S. Boning
Sponsorship: Bell Labs CRFP Fellowship, IBM

The study of process variations has greatly increased in importance due to the aggressive scaling of technology. Previous research [1] has shown the substantial impact that process variations in front-end-of-line structures have in reducing yield in integrated circuits. Robust circuit design depends on a more complete characterization of these variations and their impacts on circuit-level parameters. This project addresses this issue by developing a methodology capable of testing a large number of front-end-of-line (FEOL) and back-end-of-line (BEOL) structures and by modeling variations in threshold voltage, leakage currents and power dissipation, among others. This is achieved by designing and implementing test circuits that include a large number of high performance devices-under-test (DUTs) controlled by low-leakage switches and sensors to ensure a nominal value at the DUT terminals. Accessing analog characteristics of a large number of DUTs will make it possible to gather the statistics necessary to identify and model these variations and to prevent them from contributing to performance failure. This architecture provides a replicable methodology so that the effect of variation sources may be quantified in different technologies. This project studies variations in circuits due to the two fundamental sources of variations in integrated circuits, as noted by Nassif [4]: environmental factors, e.g., power supply variation, and physical factors, e.g., variation in polysilicon dimension. Physical factors can fall into two categories: "die-to-die physical variations" and "within-die physical variations." Analysis includes separation of spatial, layout-dependent, and random variation components both within the die and as a function of wafer location. The test chip is currently being built and results should be available soon.



▲ Figure 1: Array of transistors controlled by a limited number of pads.



▲ Figure 2: Low leakage switch (left), when enabled (center) and when not enabled (right) and DUT (circled).

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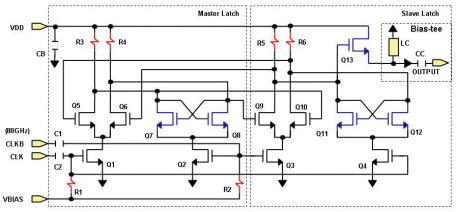
Modeling and Extraction of Variation in Physical Process Parameters

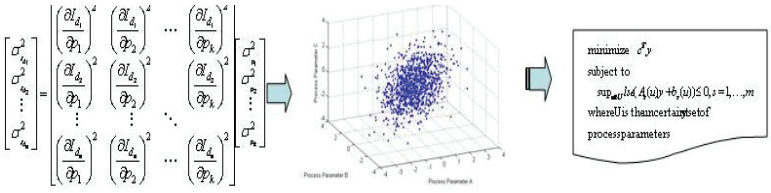
D. Lim, D.S. Boning
Sponsorship: MARCO C2S2, IBM

The impact of process variation on the performance of modern high-speed and low-power integrated circuits has been increasing as the semiconductor technology has scaled down. In modern design process, it is necessary to have an accurate variation model characterizing the statistical variability of process and design parameters. This variation model enables circuit designers to predict parametric yield in an early stage and optimize designs to obtain high-yielding chips. Finding physical process parameters that give critical contribution to circuit response fluctuation and estimating the statistical properties of the process parameters are important in building an accurate variation model. The statistical properties of process parameters can be calculated by a back-propagation of variance (BPV) method, which uses the variance of electrical responses measured by circuits to calculate the variance of process parameters based on a first-order response surface model (RSM) [1]. Test structures have a number of different configurations in terms of bias condition and geometry. First-order derivatives of circuit responses, e.g., drain currents and oscillation frequency, to process parameters are extracted by circuit simulators such as HSPICE and SPECTRE. The original BPV method has been extended to capture the correlation between process parameters and devices in this work.

We suggest a current mode latch (CML) for the characterization of high-speed analog manufacturing processes. A CML in Figure 1 can generate a self-oscillation frequency in different bias conditions, and simple digital circuitry can accurately measure the statistical properties of the self-oscillation frequencies in different configurations [3]. The BPV method can use the measured frequency data to estimate the variation of physical process parameters. Output frequency data can analyze device and passive component mismatch as well. A confidence ellipsoid with a certain probability in n-dimensional space captures the variations of process parameters. The variances and covariances of process parameters extracted from the BPV method determine the shape of the ellipsoid. Traditional deterministic optimization methods can be extended to improve the robustness of circuit outputs by sacrificing reasonable margin in optimal values. Given the ellipsoidal uncertainty model of process parameters, we can find the robust global optimum of circuit performance and power consumption using convex optimization tools [3].



▲ Figure 1: The CML frequency-divider generating a self-oscillation signal to characterize process variation.



▲ Figure 2: Procedure of statistical optimization using the BPV method to characterize variance and the convex optimization to find a robust optimum.

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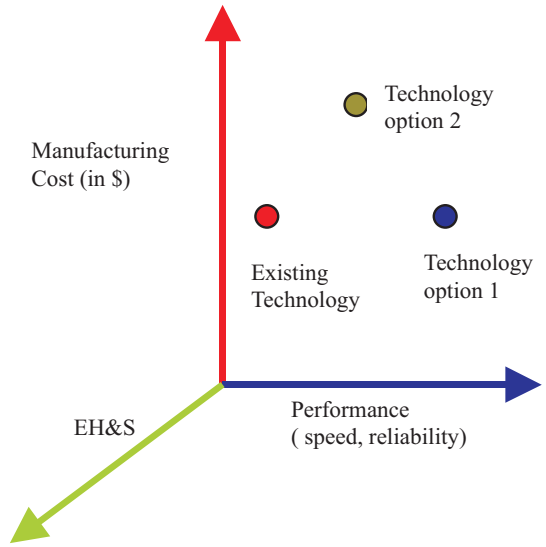
Combined Technology and Environmental Assessment of 3D Integrated Circuit Process Alternatives

A. Somani, P. Gschwend, D.S. Boning
Sponsors: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

According to the International Technology Roadmap for Semiconductors (ITRS), the industry will make significant strides in performance in future technology nodes. There is a need to introduce novel materials and process technologies with innovative integration schemes since scaling is not enough to achieve greater performance in devices. Analyses of the advantages of these new options have conventionally focused on how performance improves and cost reduces with the new material or process. Unfortunately, significant time and investment in materials and process technology development can be lost if environment, health, and safety (EHS) are not factored into the early decision-making process. We suggest that future technology options should be evaluated on three axes, including not only cost and performance but also EHS (Figure 1). Future process technology development must involve an approach to assess the EHS impacts of new technologies and alternatives early in the research and development cycle.

In this present effort, we propose a comparative methodology for environmental impact evaluation along with a method to evaluate emerging silicon-based technologies [1]. The proposed methodology is applied to an emerging technology: three-dimensional (3-D) integrated circuits (ICs). In this work, we focus on a 3-D integration process based on Cu thermo-compression bonding. The MIT 3-D approach [2] is a metal Cu-Cu thin-first via-last process technology in which two active device wafers are stacked in a back-to-face fashion and bonded by means of low-temperature Cu-to-Cu thermo-compression. The comparative methodology was applied to the MIT 3-D IC approach in reference to state-of-the-art IC technology (2-D IC) and then additional and new processes were tabulated (Table 1). The objective is to identify unit processes that neither are environmentally benign nor perform from the technological viewpoint. Handle-wafer attaching and releasing is one unit process that uses thick Al release-layers. Therefore, in on-going research we are trying to find solutions for handle wafer and also low-temperature bonding processes.



▲ Figure 1: New and existing technology options exhibit different trade-offs in performance, cost, and environment, health, and safety.

Unit operation	# Unit steps required in 2D process flow (for one wafer)	# Additional unit steps required in 3D process flow (to add one layer)
Photo/Ashing	25	1
Dry Etch	17	2
Wet etch/Clean	31/14	¾
CVD	11	1
CMP (Cu and Oxide)	14	2
Sputtering Al	1 (0.5 μm for metal 1)	2 (20 μm)
Sputtering Ta/Cu	6	1
Electrodeposition Cu	6	1
Bonding	0	2
Grinding	0	1
Implant	9	0
Oxidation/ Annealing	4/7	0/2

▲ Table 1: First-order unit process comparison between 2D and 3D IC flows.

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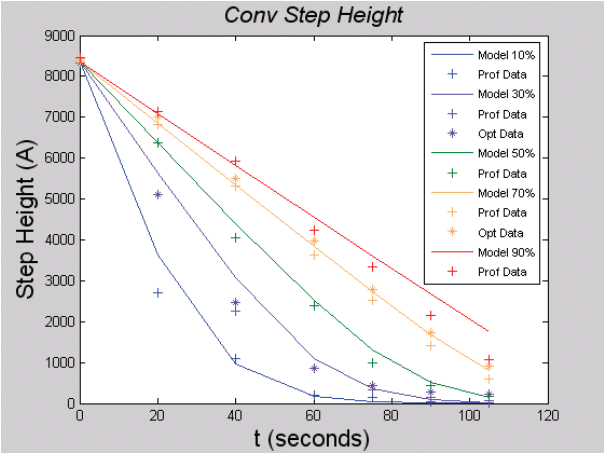
Polishing Pad Effects in CMP

D. Truque, X. Xie, D.S. Boning
Sponsorship: SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing

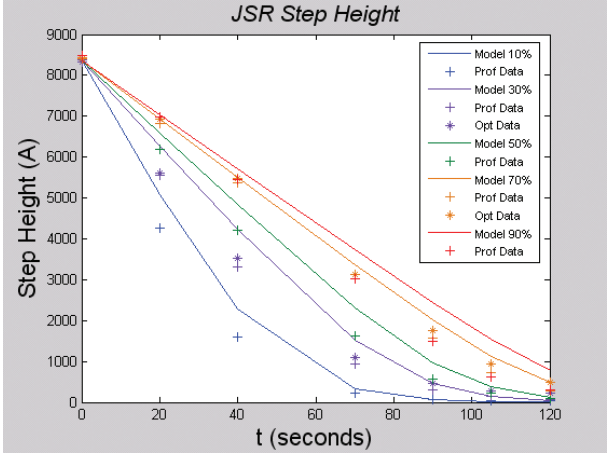
Our group has proposed several chip-scale, pattern-density-dependent chemical mechanical polishing (CMP) models. [1-2] CMP is an enabling technology used in various front- and back-end semiconductor processes as well as in MEMS. A good understanding and modeling of CMP is essential to optimize the process, improve the yield, and reduce consumables. Our model uses parameters related to physical properties of polishing pads and slurries, but they are extracted purely from experimental data as fitting coefficients. In collaboration with JSR Micro, a pad and slurry manufacturer, we will relate these parameters to pad stiffness, pad surface properties, slurry particle size, etc.

The most recent experiments compared the standard industry pad (IC1000) against a novel pad by JSR that includes water soluble particles (WSPs). The WSPs aid in keeping the pad bulk stiff, which improves pad planarization. When the WSPs reach the surface and contact the slurry, they passively dissolve, creating micropores in the pad that help in the slurry transport and material removal to increase removal rate and provide uniform removal.

From the data examined, we concluded that the WSPs improve the planarization length of the polishing process. The results also showed that the IC1000 had a higher removal rate than the JSR pad, but at the expense of pattern density dependencies. Both pads had comparable removal rates for pattern densities around 70%. The JSR pad had a lower pattern-dependency than the IC1000 pad, where regions of lower density polished considerably faster than regions of higher density. We noticed some edge dependencies with the JSR pad, and these dependencies caused regions near the edge to polish faster, but this higher removal rate near the edge might be caused by the wafer-holding ring on the CMP tool used.



▲ Figure 1: Step height evolution for different pattern densities for the conventional IC1000 polishing pad. Data points show profilometry and optical measurements; line shows prediction of model.



▲ Figure 2: Step height evolution for different pattern densities for the JSR water-soluble particle-enhanced pad. Data points show profilometry and optical measurements; line shows prediction of model.

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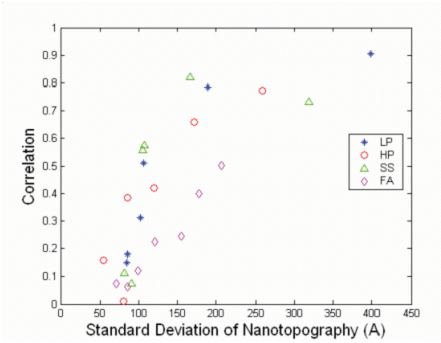
Application of CMP Models to Issues in Shallow Trench Isolation

X. Xie, D.S. Boning
Sponsorship: IMEC, Infineon Technologies, Rohm and Haas, Siltronic AG

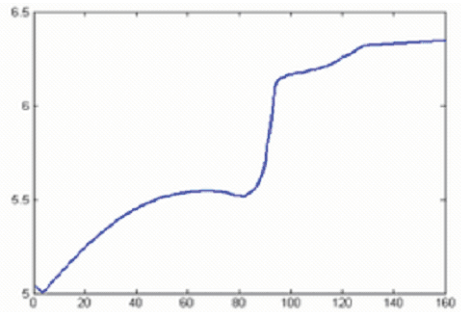
As advancing technologies increase the demand for planarity in integrated circuits, chemical mechanical planarization (CMP) continues to be the enabling technology in IC fabrication, while new challenges emerge and a new process-monitor technique has been proposed. Our CMP models enable us to study various issues in shallow trench isolation (STI) processes.

Nanotopography – a term used to describe (10-100-nm) surface height variation extending across millimeter-scale lateral distance on raw wafer – can result in additional oxide dishing and nitride erosion in STI. In this study, a set of experiments was designed to study nanotopography and CMP interactions in STI layer stacks (oxide/nitride/oxide), in both blanket wafers and patterned wafers. Our blanket wafer data analysis shows that initial nanotopography maps correlate well with the high-frequency part of post-CMP variation (Figure 1), although the low-frequency part (from CMP tool, pad, and process non-uniformity) accounts for a larger magnitude or proportion of post-CMP variation. The result implies weak nanotopography impact for polishing STI-patterned wafers for the starting nanotopography and CMP processes considered here. The analysis of patterned-wafer data also shows that any correlation between the nanotopography map and the electrical test map is very weak, if it exists at all.

Frictional monitoring endpoint detection (EPD) has proven to be feasible for monitoring the STI CMP process. Experimental data indicates that frictional effects generated by the pattern structures and various layered materials on the wafer create distinct and characteristic responses for determining an appropriate endpoint. With the existing CMP model, we studied the underlying physics of the friction model and related the evolution of patterned wafers to friction endpoint traces. The new model accounts for the spatial configuration of the surface profile and its impact on friction. Three sets of experiments were conducted using ceria-based slurries; the resulting motor current signals differ substantially, and the predicted friction traces agree reasonably well with the experiments (Figure 2).



▲ Figure 1: For all the blanket wafer polishes that stopped in the oxide layer, the correlations between the nanotopography map and the oxide amount removal map are shown, versus the standard deviations of nanotopography maps. The plot shows that larger nanotopography height variation results in a stronger correlation with spatial variation.



▲ Figure 2: The model predicted motor current (vertical axis, arbitrary units) versus time (horizontal axis, seconds) based on the surface topography evolution. The prediction agrees well with measured motor current. The relatively flat region starting at 130 seconds signals the endpoint.

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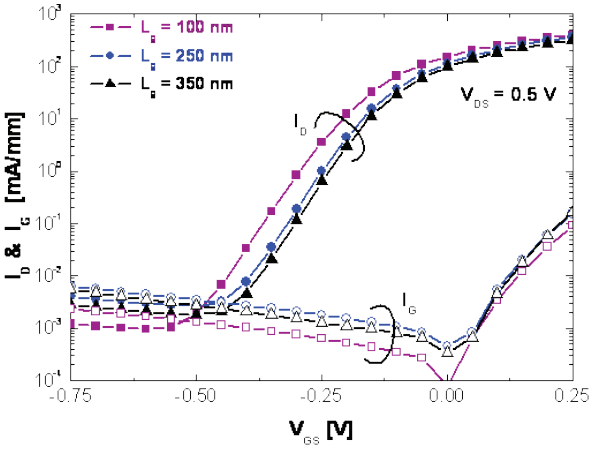
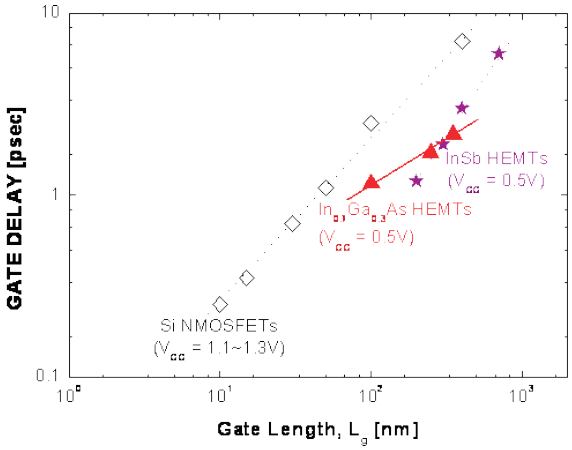
Potential of InGaAs High-electron Mobility Transistors as a Beyond-CMOS Logic Technology

D.H. Kim, J.A. del Alamo
Sponsorship: Intel, MARCO MSD

The InAlAs/InGaAs high-electron mobility transistors (HEMTs) closely lattice-matched to InP exhibit extraordinary frequency response, as measured by cutoff frequency (f_T). The current record is 562 GHz for a gate length (L_g) of 25 nm [1]. However, these devices suffer from poor electrostatic integrity and inadequate scaling behavior and as a result possess questionable usefulness for logic. We have been investigating InGaAs HEMTs as a future high-speed and low-power logic technology for applications beyond CMOS [2-3]. Figures of merit relevant to logic, such as logic-gate delay (CV/I), I_{ON}/I_{OFF}, drain-induced barrier lowering (DIBL), and subthreshold slope (S) are evaluated in this family of the device technology. We have found that these devices exhibit promising logic characteristics. In particular, 100-nm L_g devices yield DIBL as low as 80 mV/V, S of 77 mV/decade, and gate delay of 1.2 psec, at a V_{CC} of 0.5 V. More importantly, we have found that these devices, from a logical point of view, reach their scaling limit at 100-nm gate length of $In_{0.7}Ga_{0.3}As$ HEMTs. Realizing the logic potential of $In_{0.7}Ga_{0.3}As$ HEMTs will require a more scalable device design with better electrostatic integrity. If this requirement can be accomplished, InGaAs HEMTs could well be the technology of choice when the CMOS roadmap comes to an end.



▲ Figure 1: Sub-threshold characteristics of $In_{0.7}Ga_{0.3}As$ HEMTs, at a V_{CC} of 0.5 V. This graph a very sharp sub-threshold slope and a very low off-state current that is mostly limited by gate leakage current through the Schottky gate. The slight softening of the sub-threshold slope as L_g approaches 100 nm is a manifestation of short-channel effects.



▲ Figure 2: Logic gate delay (CV/I) vs. gate length for our InGaAs HEMTs, state-of-the-art Si-MOSFETs and InSb HEMTs [4]. In our devices, CV/I was chosen to have I_{ON}/I_{OFF} ratio of 10^3, at a V_{CC} of 0.5 V. Our 100-nm $In_{0.7}Ga_{0.3}As$ HEMTs exhibit a gate delay of 1.16 ps, which is about a factor of 2 times better than equivalent Si-MOSFETs. This excellent result speed result arises from the superior electron transport properties of our heterostructure.

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Electrical Degradation of GaN High Electron Mobility Transistors

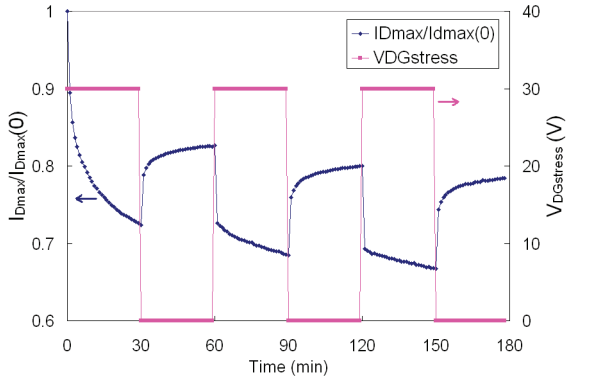
J. Joh, J.A. del Alamo
Sponsorship: DARPA, ARL

Due to their extraordinary RF power performance, GaN-based transistors have recently been under intense research. As a result of their high breakdown electric field (>3 x 10^6 V/cm), GaN-based devices can operate at a voltage as high as 120 V. The AlGaN/GaN high electron mobility transistors (HEMT) have already shown an output power density of 10.7 W/mm at 10 GHz. This outstanding performance makes these devices of great interest for high-power, high-frequency applications such as WiMAX or WLAN base stations. In spite of these superior properties, GaN HEMTs have serious reliability problems that must be solved before this technology can become commercialized. Our research attempts to identify the physical mechanisms responsible for the problematic reliability of GaN HEMTs.

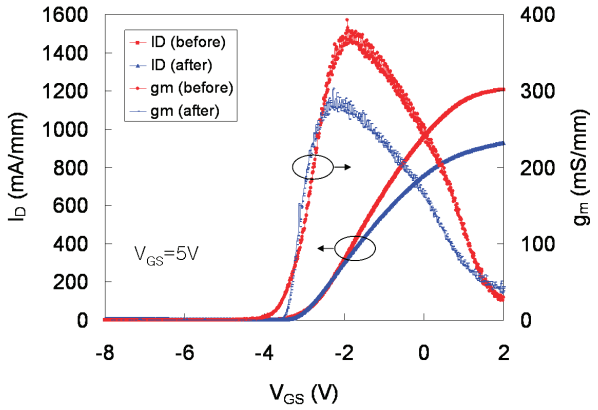
We are studying the fundamental degradation mechanisms of industrial GaN HEMTs. In particular, we are studying the decrease of the maximum drain current (I_{Dmax}) and the increase of the source and drain resistances (R_S and R_D) as the device is electrically stressed. We have constructed an automated stressing and characterizing routine, and we have performed DC stressing tests under various biasing conditions and environments. A typical stress-recovery experiment appears in Figure 1, where I_{Dmax} degradation is shown as the device is stressed with V_{DG}=30 V while maintaining V_{DS}=0. In this experiment, periods of stress on the device alternate with periods of recovery during which the characteristics of the device are also monitored. Before and after the stressing experiments and at selected points in between, complete characterization of the device is performed. Figure 2 shows, for example, the change in the transfer characteristics before and after the stressing experiment of Figure 1.

Based on experiments like this, we have made some preliminary findings. We have found that the degradation of I_{Dmax} strongly correlates with an increase in R_D and R_S. These changes seem to arise from a decrease of the carrier density in the extrinsic portion of the device. This decrease occurs in a process of trap-generation and subsequent electron-trapping in the extrinsic device. The trap-generation process appears to be driven by the magnitude of the electric field between the gate and the source or drain. Electron detrapping is clearly observed in Figure 1 during the recovery periods that are interleaved with stressing.

Our research addresses the fundamental degradation physics of GaN HEMTs. This study will help us to understand failure mechanisms in detail and to develop processes and device designs that minimize these deleterious effects.



▲ Figure 1: Degradation of maximum drain current (normalized to the original value) versus time. The purple line shows the stressing bias V_{DG}. The device was stressed at V_{DG}=30 V and V_{DS}=0 V for 30 minutes. From t=30 to t=60 min, the device was at V_{DG}=V_{DS}=0 V. The same cycle was repeated three times.



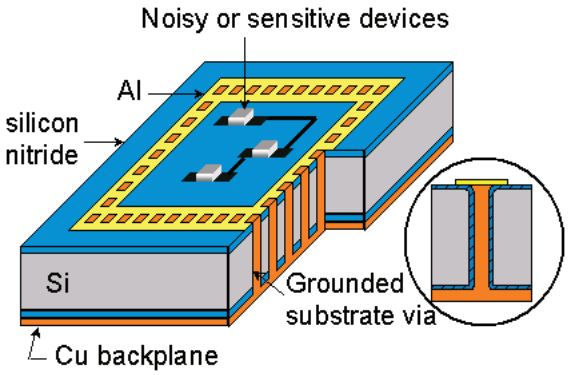
▲ Figure 2: Drain current and transconductance before (t=0) and after (t=180 min) stressing in the experiment of Figure 1.

Through-substrate Interconnects for Millimeter-wave Mixed Signal Systems

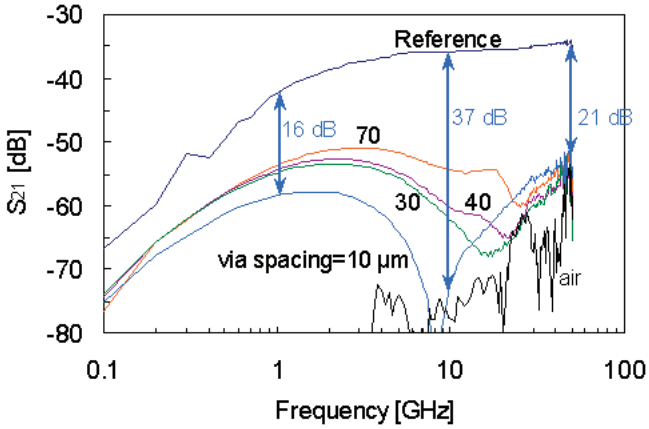
J.H. Wu, J.A. del Alamo
Sponsorship: Applied Materials Graduate Fellowship

Advances in silicon technology may eventually displace III-V semiconductor devices in the mm-wave regime. This would make bandwidth available for affordable and pervasive applications. The challenges for Si are low-loss interconnects and packaging, substrate isolation, and thermal management. We have developed a through-substrate via technology that allows for low-impedance ground distribution and substrate crosstalk isolation up to 50 GHz. This technology also has potential for addressing other substrate issues in the mm-wave regime [1]. The inset of Figure 1 depicts the through-wafer interconnect.

Substrate crosstalk between sensitive RF circuits and analog and digital blocks is one of the most critical problems facing mixed-signal circuit designers. We have developed a Faraday cage isolation structure using through-wafer vias to surround noisy or sensitive circuits (Figure 1). Our Faraday cage exhibits an isolation of 37 dB at 10 GHz and 21 dB at 50 GHz. Figure 2 shows S_{21} measurements of Faraday cages with different via spacing compared to a reference structure. The distance between the transmitter and the receiver is 100 µm. Reducing the density of vias of the Faraday cage diminishes its performance but still significantly suppresses substrate crosstalk into the mm-wave regime. Faraday cage measurements from a previous process show better performance at lower frequencies, 42 dB in isolation at 1 GHz versus 16 dB in isolation for this new process [1-2]. However, this is due to a better silicon nitride liner in our new process, which adds an extra capacitance at low frequencies and hinders the performance of the Faraday cage. This liner can be reduced or eliminated in future processes specifically for this application to boost isolation at lower frequencies.



▲ Figure 1: Drawing of a Faraday cage using through-substrate vias to surround a noisy or sensitive circuit. The substrate via (inset) is etched in silicon, lined with silicon nitride, and filled with electroplated copper, followed by copper CMP. An aluminum pad caps the top of the via.



▲ Figure 2: S_{21} vs. frequency for Faraday cages with different via spacing and a reference test structure at a distance of 100 µm. The diameter of the vias is 10 µm. At the smallest via spacing of 10 µm, the Faraday cage reduces substrate noise by 37 dB at 10 GHz and 21 dB at 50 GHz.

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[2] J.H. Wu and J.A. del Alamo, "An equivalent circuit model for a Faraday cage substrate crosstalk isolation structure," *IEEE Radio Frequency Integrated Circuits Symposium*, June 2004, pp. 635-638.

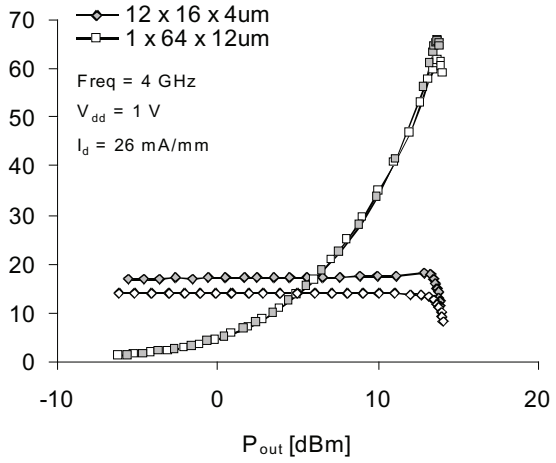
Performance and Limitations of 65-nm CMOS for Integrated RF Power Applications

J. Scholvin, D.R. Greenberg (IBM), J.A. del Alamo
Sponsorship: IBM Faculty Award, IBM Ph.D. Fellowship

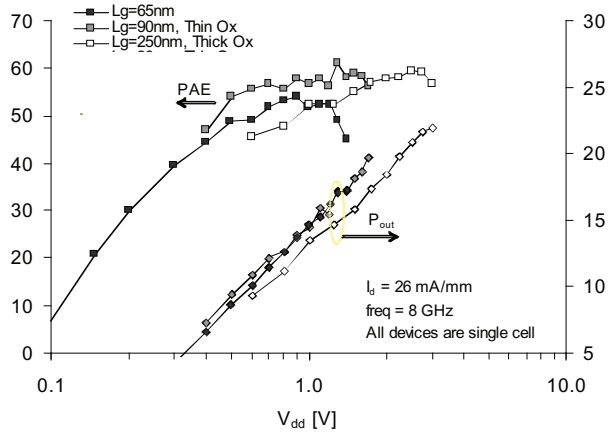
The microelectronics industry is striving to reduce the cost, complexity, and time-to-market of wireless systems through single-chip integration of mixed-signal radio frequency RF/digital functions. Achieving such integration while minimizing the increased cost of technology add-ons demands a great deal from the base CMOS technology. In this regard, the integration of the power amplifier (PA) function remains a particular challenge as technology geometries scale down. Gate length (L_g) scaling yields better high-frequency response, promising higher power-added efficiency (PAE). These benefits come at the cost of a lower drain voltage, which demands a higher output current and thus wider devices in order to produce a given output power level (Pout).

In this work, we have studied the suitability of the 65-nm CMOS node for integrated RF PA applications. We have found that the standard 65-nm logic device is capable of achieving PAE values greater than 65% at 4 GHz (Figure 1), with Pout scalable to about 17 dBm, which is sufficient for many applications. We have also compared the 65-nm node with prior CMOS generations: from 250 to 90 nm (Figure 2). Comparison with the 90-nm node reveals that back-end scaling in the 65-nm technology has lead to increased interconnect resistance, which limits the maximum P_{out}. This problem should be addressed through optimized cell layout and wiring level selection.

For low power levels (below 16 dBm or 40 mW), the 65-nm technology CMOS node offers excellent efficiency over a broad frequency range. Its RF power performance approaches that of 90-nm devices both in peak PAE and output power density. Using cells with multiple short gate-width fingers can optimize performance. . Scaling the power level therefore demands wiring many fingers and cells in parallel. The higher sheet resistance of the BEOL of 65-nm CMOS leads to difficulty in scaling output power using existing layout. Simulation indicates that further optimization of device layout, including the use of stacked or thicker upper metal levels, should mitigate the negative effects of the BEOL scaling. Through this, the 65-nm node can provide efficient integrated power amplifier functionality for many applications, even in a deeply-scaled logic CMOS technology without costly PA-specific adders.



▲ Figure 1: Power measurement of two 768-µm-wide, 65-nm devices. The 12-cell device (12 cells of 16 fingers, each finger 4-µm wide) delivers a peak PAE of 65.7% at a power of 13.8 dBm (31.2 mW/mm) at 4 GHz [2].



▲ Figure 2: Peak PAE and output power density as a function of V_{dd} for the three different CMOS technologies [1-2].

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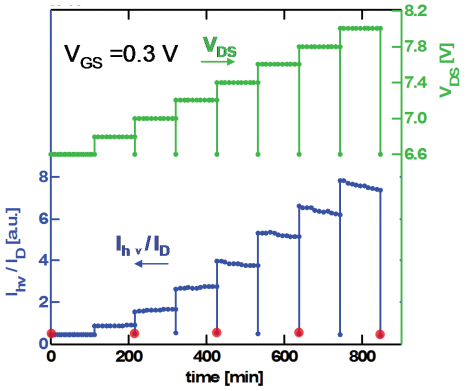
[2] J. Scholvin, D.R. Greenberg, and J.A. del Alamo, "Performance and limitations of 65 nm CMOS for integrated RF power applications," in *Proc. IEDM 2005*, Washington, D.C., Dec. 2005, pp. 369-372.

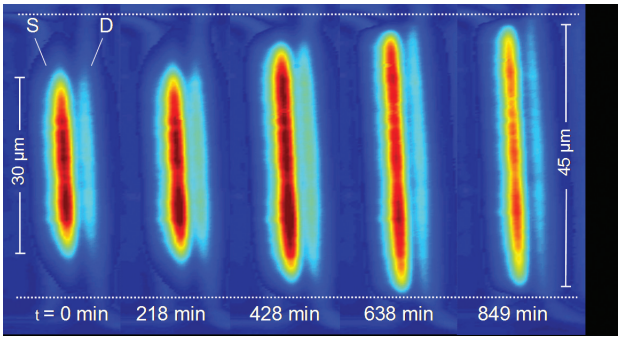
Non-Uniform Degradation Behavior in RF Power GaAs PHEMTs

A.A. Villanueva, J.A. del Alamo
Sponsorship: Mitsubishi Electric

GaAs pseudomorphic high-electron mobility transistors (PHEMTs) are widely used in RF power applications. Since these devices typically operate at high power levels and under high-voltage biasing, their electrical reliability is of serious concern. Previous studies have identified several distinct degradation phenomena in these devices, such as impact-ionization (II), hot electron trapping, and surface corrosion [1-3]. However, so far reliability studies have always assumed that degradation takes place uniformly across the width of the device. In our research, we investigate the degradation behavior across the width of the device by studying light emission. Since light emission is correlated with II [4], a photograph of emitted light gives us a spatial picture of II and electric field. By taking light-emission photographs during bias stressing experiments, we observed the light emitted from a device as it is being stressed. Figure 1 illustrates the bias conditions and total light intensity emitted (normalized to I_D) for such an experiment. As V_{DS} is stepped up, we see that the total light emitted increases (as expected, since the electric field and II are increasing). Examining the light emission photos at select points during the experiment (Figure 2), we see that the light emission is very non-uniform along the width of the device: initially it is heavily concentrated in the center, but then with stressing it spreads out. This behavior suggests that the electric field is higher in the center of the device, and thus degradation is occurring preferentially there. We performed analogous light-emission experiments on test structures (TLMs) and observed similar behavior. Materials analyses of the TLMs showed that a non-uniform recess length was the cause for the non-uniform electric field distribution. Thus, in order to improve long-term device reliability, it is very important to identify and minimize non-uniformities in device geometry which can affect the degradation behavior of a device.



▲ Figure 1: Bias V_{DS} (green) and total light intensity divided by I_D (blue) vs. stressing time in a typical PHEMT light-emission experiment. Each point represents a time when a light emission photograph was taken. Before V_{DS} is stepped up, it is brought to its initial value of 6.6 V in order to get pictures at regular intervals at a constant value of V_{DS}. Points highlighted in red indicate points depicted in Figure 2.



▲ Figure 2: Light-emission photographs from source and drain of PHEMT, at five points during step-stressing experiment. Taken at V_{GS}=0.3 V, V_{DS}=6.6 V. Gate width W_g = 50 µm.

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[4] E. Zanoni, A. Paccagnella, P. Pisoni, P. Telaroli, C. Tedesco, C. Canali, N. Testa, and M. Manfredi, "Impact Ionization, recombination, and visible light emission in AlGaAs/GaAs high electron mobility transistors," *Journal of App. Physics*, vol. 70, pp. 529-531, 1991.

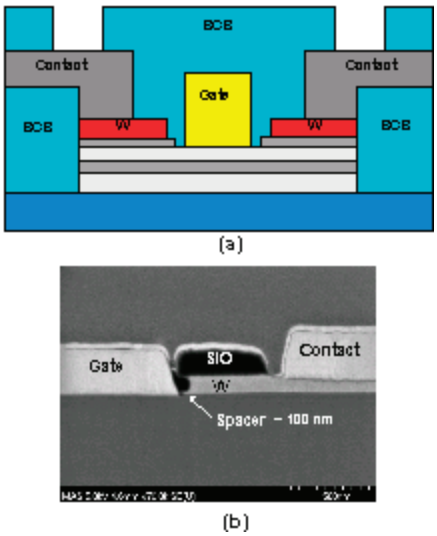
A Self-aligned, InGaAs, High-Electron-Mobility, Transistor-Device Architecture for Future Logic Applications

N. Waldron, J.A. del Alamo
Sponsorship: MARCO MSD, Intel Foundation Ph.D. Fellowship

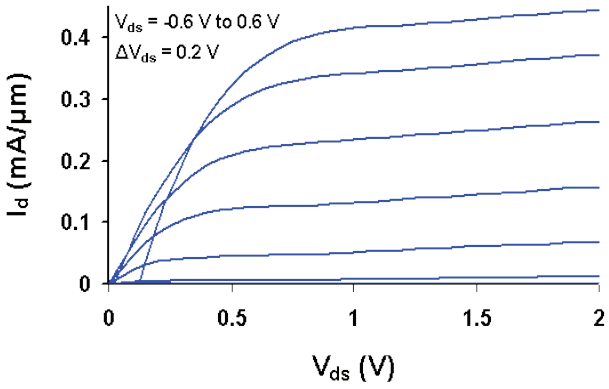
As CMOS approaches the end of the scaling roadmap, the need to identify a new logic device technology is becoming increasingly pressing. The InAlAs/InGaAs high electron mobility transistor (HEMT) has been demonstrated to show great promise for logic applications [1] and we investigate that material system in this project. Traditionally this type of device has been developed for millimeter-wave rather than digital applications, resulting in a large extrinsic footprint and high parasitics. In contrast, Si CMOS, which dominates the digital IC market, has benefited from aggressive gate-scaling coupled with close attention to extrinsics and packing density.

In order to realize the potential of InAlAs/InGaAg HEMTs in large-scale digital circuits, it is necessary to address the problems of the extrinsic resistances and capacitances that the non-self-aligned design and large footprint bring about. To this end we have designed a device architecture that incorporates a novel shallow-trench isolation and self-aligned gate scheme (Figure 1). The BCB shallow trench design provides a low capacitive isolation scheme while maintaining a planar surface. The self-aligned gate process reduces the parasitic source and drain resistances with the added benefit of reducing the footprint of the device. The non-alloyed tungsten ohmic contacts allow for well-defined contact geometries. The process architecture offers the promise of a reliable, highly manufacturable process needed to realize the complex circuits required for large-scale digital applications.

Long channel devices fabricated using the self-aligned process exhibit good DC characteristics (Figure 2). The source resistance (r_s) of the devices was estimated using TLM test structures to be on the order of 130 Ω. μm, an exceptionally low value. This is expected to be of most benefit when we transfer the process to deep submicron devices.



▲ Figure 1: (a) Cross-section of the proposed new device architecture. Features include BCB planar isolation, self-aligned gate and non-alloyed ohmic contacts. (b) The SEM cross-section of a typical device with a gate-to-source metallization distance of 100 nm.



▲ Figure 2: Output characteristics of a long channel device (~ 2.5 μm) fabricated using the self-aligned device architecture. The TLM test structures were used to estimate the source resistance, r_s at 130 Ω μm.

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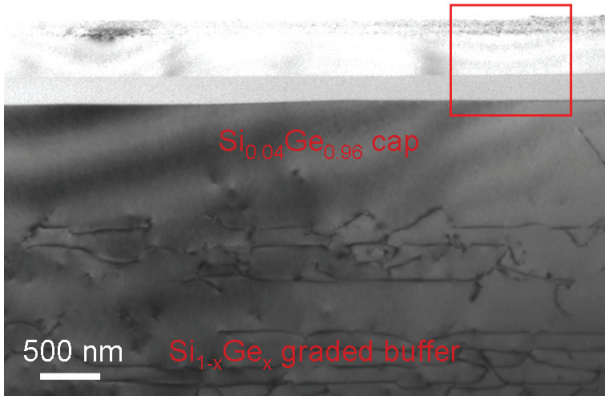
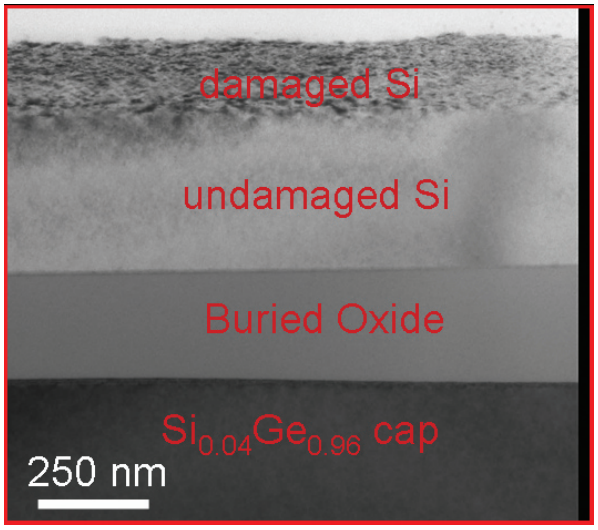
Fabrication of Silicon on Lattice-engineered Substrate (SOLES) as a Platform for Monolithic Integration of Si- and GaAs-based Devices

C.L. Dohrman, K. Chilukuri, D.M. Isaacson, M.L. Lee, E.A. Fitzgerald
Sponsorship: MARCO IFC, CMSE, MTL

We report the fabrication of a novel substrate platform for the monolithic integration of Si-based CMOS and GaAs-based optoelectronic devices. This platform, which we refer to as silicon on lattice-engineered substrate (SOLES), consists of a compositionally graded SiGe buffer buried underneath an SOI structure, all fabricated on a Si substrate. The SiGe graded buffer was grown by UHVCVD and was capped with a Ge-rich alloy that is closely lattice-matched to GaAs ($0.96 < x_{Ge} < 1$); it provides a threading dislocation density (TDD) of $\sim 10^6$ cm^{-2}. While previous studies have proved the SiGe graded buffer to be an effective platform for fabrication of GaAs-based LEDs, lasers, and solar cells on Si substrates, the large thickness (~10 μm) of the SiGe graded buffer hampers the integration of both Si- and GaAs-based devices on a single chip using this technique. The SOLES eliminates this drawback by the addition of the SOI structure on top of the Ge-rich cap. This approach provides a Si device layer in close proximity to the GaAs-based device layer, thereby simplifying the monolithic integration of Si- and GaAs-based devices with this platform. Fabrication consists of layer transfer of Si to an oxide-coated graded buffer using oxide-oxide wafer bonding followed by hydrogen-induced layer exfoliation of the Si layer from its donor wafer. The resulting structure was imaged with cross-sectional TEM and appears in Figure 1. Figure 2 (inset of Figure 1) reveals the SOI layer structure more clearly. Our results show that this layer transfer occurs reliably across the entire wafer, making it amenable to commercial applications.



▲ Figure 1: Transmission electron microscopy (TEM) image of SOLES platform. Misfit dislocations of the $Si_{1-x}Ge_x$ graded buffer appear at the bottom of the image. Figure 2 enlarges the red box inset in this image.



▲ Figure 2: Inset of Figure 1. This image illustrates the transferred layers. This image was taken before the removal of the exfoliation-damaged Si surface layer, and this damage is clearly seen here.

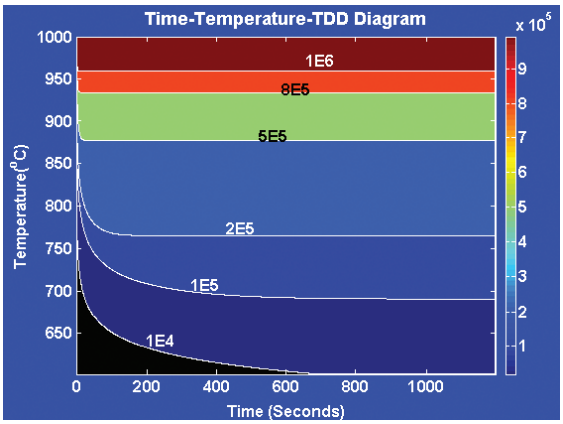
Thermally Relaxed, Ultra-thin, SiGe Buffers

S. Gupta, D.M. Isaacson, Y. Bai, E.A. Fitzgerald
Sponsorship: MARCO MSD

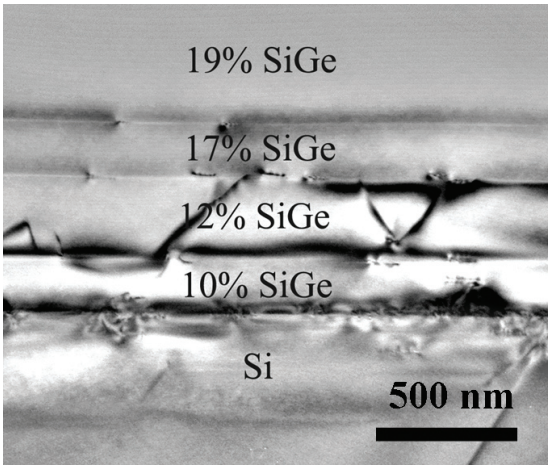
Producing relaxed, nearly defect-free SiGe alloys on Si substrates has been difficult due to the 4% lattice mismatch between Si and Ge. A relaxed $Si_{1-x}Ge_x$ graded buffer creates a larger lattice constant on a Si substrate while providing low threading dislocation densities (TDD) on the order of 10^5 cm^{-2}. Many other concepts for attaining relaxed $Si_{1-x}Ge_x$ buffers on Si wafers have been proposed over the years [1]. However, compositional grading remains the only established technique for attaining low-dislocation density, fully relaxed $Si_{1-x}Ge_x$ alloys on a Si substrate.

Two important variables that affect the dislocation density in a mismatched layer have been identified as the strain rate at which the layer is grown and the surface roughness of the layer. Reducing the TDD in a mismatched SiGe layer on Si requires low strain rates, which could be achieved by growing layers at slower growth rates. The traditional means to reduce the growth rate is to lower the growth temperature. Since the surface mobility of the atoms is reduced, the resulting layer has less surface roughness. However, since dislocation velocity is exponentially dependent on temperature, decreasing the growth temperature results in introduction of metastable strain, thus preventing complete relaxation of the strained layer. Therefore, achieving a completely relaxed, low-TDD layer requires the removal of the metastable strain without increasing the dislocation nucleation. While high temperature annealing is a way to reduce metastability, it also causes TDD escalation. A tool for estimating the TDD after an isothermal anneal has been developed for the first time in literature and is referred to as a TTTDD diagram (Figure 1).

One possible way to remove the metastability of this layer is by annealing or by depositing strained layers on top of the metastable layer and then subjecting it to anneals. The increased stress at the surface will increase the dislocation velocity for a given anneal temperature. We have demonstrated this technique with mismatched $Si_{0.90}Ge_{0.10}$ layers on Si. Complete relaxation and low TDD have been achieved as compared to films grown under high growth temperatures to achieve complete relaxation. Our results demonstrate that, for the 10% Ge layer used in these experiments, we can reduce the buffer thickness by a factor of 2.5 as compared to the conventional graded buffer. This development could prove very helpful in applications requiring extremely thick graded buffers, as is the case for Ge on Si.



▲ Figure 1: A TTTDD diagram for a metastable 10% layer.



▲ Figure 2: Thermally relaxed ultra-thin buffer. Thickness is about 2.5 times less than the conventional graded buffer.

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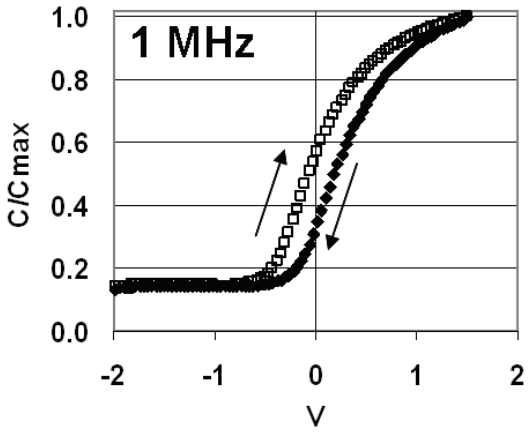
[1] M.L. Lee, E.A. Fitzgerald, M.T. Bulsara, M.T. Currie, and A. Lochtefeld, *J. of App. Physics*, vol. 97, p. 011101:1-28, 2005.

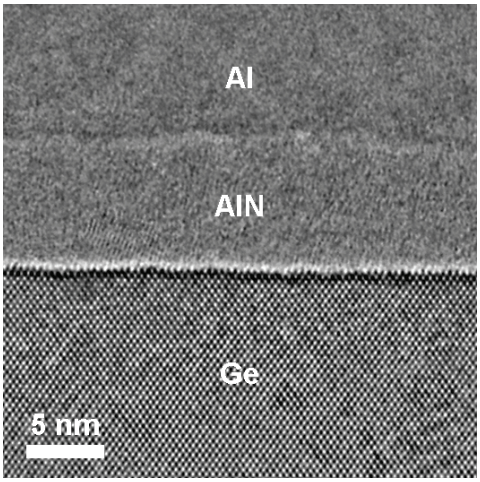
Microstructural and Electrical Characteristics of AlN Gate Dielectrics Deposited on Ge and GaAs Channels

M.L. Lee, A. Ritenour, D.A. Antoniadis, E.A. Fitzgerald
Sponsorship: MARCO MSD

We have fabricated metal-insulator-semiconductor capacitors on both Ge and GaAs channels with an Al/AlN gate stack. The capacitors possess an EOT of 2-4 nm and exhibit clean accumulation with low hysteresis and little frequency dispersion (Figure 1). The AlN dielectric is deposited by low-pressure metal-organic chemical vapor deposition, and the Al gate is deposited by physical vapor deposition. High-resolution transmission electron microscopy studies on the finished devices reveal that the AlN is amorphous or nanocrystalline or both (Figure 2), and correlation of the physical thickness with capacitor data indicates a dielectric constant of approximately 10. The AlN is grown with standard metal-organic precursors in an epitaxial growth reactor; we can therefore deposit both the high-mobility channel and the dielectric *in situ* without exposure to ambient air. We believe that AlN and other wide-bandgap III-N layers are particularly well-suited for III-V channels, since they enable us to eliminate the unintentional formation of native oxides at the insulator/semiconductor interface.



▲ Figure 1: High-frequency C-V measurements of Al/AlN gate stack deposited onto n-Ge.

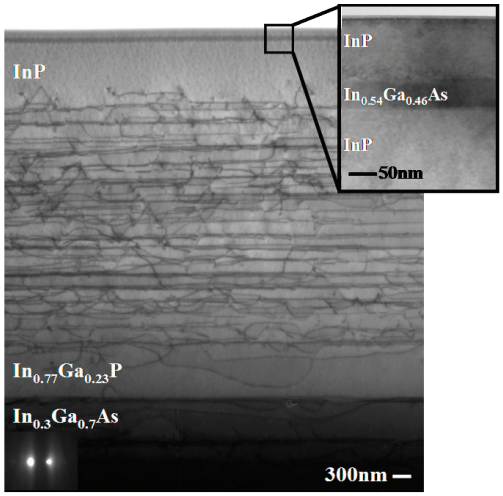


▲ Figure 2: HRTEM image of Al/AlN//Ge capacitor structure.

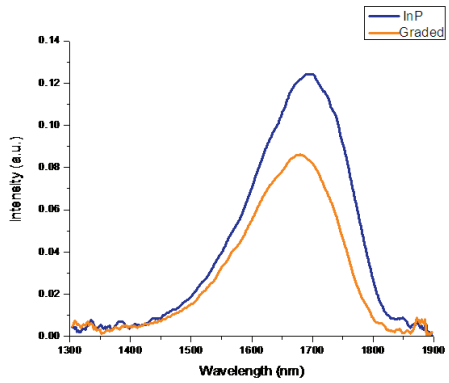
High-Quality InP-on-GaAs using Graded Buffers Grown by Metal Organic Vapor Phase Epitaxy (MOVPE)

N. Quitoriano, E.A. Fitzgerald
Sponsorship: ARO, MARCO MSD

In addition to traditional telecom applications, devices based on InP have received increased attention for high-performance electronics. The InP growth on GaAs is motivated by the facts that InP wafers are smaller and more expensive and they utilize older fabrication equipment than GaAs. Creating high-quality InP-on-GaAs-bulk substrates has proven challenging, however. While a number of commercial growth foundries offer InP-on-GaAs for M-HEMT (Metamorphic High-Electron-Mobility Transistor) applications, the successful demonstration of InP-based, minority-carrier devices on bulk GaAs remains elusive. We demonstrate InP-on-GaAs suitable for minority carrier devices, exhibiting a threading dislocation density of $1.2 \times 10^6/cm^2$ determined by plan-view transmission electron microscopy (see Figure 1, the cross-sectional TEM). This material exhibited nearly equivalent PL data compared to one on bulk InP at room temperature (see Figure 2). To achieve this result, we explored the InGaAs, InGaP, InAlAs and InGaAlAs materials systems. In each of these systems, we found that microscopic compositional inhomogeneities along the growth direction blocked dislocations leading to dislocation densities as high as $10^9/cm^2$. Using scanning-transmission electron microscopy, we determined that surface-driven phase separation leading to Ga-rich regions caused the composition variations. Conditions for avoiding phase separation were identified and explored. We found that we could prevent composition variations in $In_xGa_{1-x}As$ graded buffers grown at 750°C to yield low dislocation densities of $1.5x10^6/cm^2$ for $x<0.34$, accommodating ~70% of the lattice mismatch between GaAs and InP. However, further grading to 53% In is required to attain the lattice constant of InP. We have found that compositional grading in $In_yGa_{1-y}P$ $(0.8<y<1.0)$ can accommodate the remaining lattice mismatch with no rise in thread density while avoiding phase separation. Consequently, to achieve high-quality InP-on-GaAs, we started with the InGaAs material system and then completed the graded buffer in the InGaP system to reach InP.



▲ Figure 1: Cross-sectional bright-field TEM micrograph of high-quality InP-on-GaAs. The enlarged top portion highlights the PL structure.

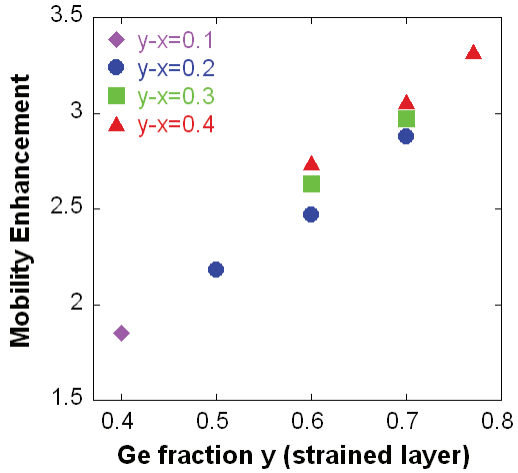


▲ Figure 2: Room temperature PL data from the same PL structure on bulk InP (denoted "InP") and on our graded structure (denoted "Graded," see Figure 1). The graded structure PL integrated intensity is about 70% of the bulk. Since this percentage is the same at 20K, we believe that the reduction in intensity is not due to defects, rather light the laser is penetrating into the graded buffer where the generated carriers recombine.

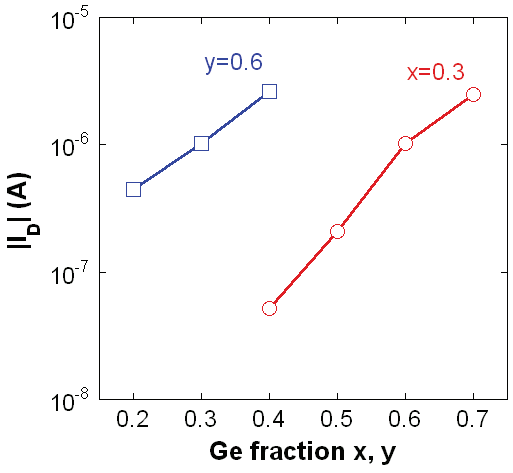
Hole Mobility in High-Ge-content, Strained SiGe-Channel MOSFETs

C. Ní Chléirigh, O.O. Olubuyide, J.L. Hoyt
Sponsorship: SRC, MARCO MSD, Applied Materials

This work presents, for the first time, a comprehensive study of mobility, sub-threshold slope, and off-state leakage current in high-Ge-content, dual-channel strained Si/strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$ p-MOSFETs. Hole mobility enhancements of 3X are observed at high inversion charge densities ($N_{inv}=10^{13}$ cm^{-2}) for the strained $Si_{0.3}Ge_{0.7}$ on relaxed $Si_{0.7}Ge_{0.3}$ (70/30) structure with 2-nm-thick cap and 3-nm-thick gate oxide. A wide range of Ge fractions and Si cap thicknesses is studied. The Ge fraction in the strained $Si_{1-y}Ge_y$ layer dominates the mobility enhancement, while the level of strain is a second order effect (Figure 1). The off-state drain leakage is studied in detail. At low drain-to-gate bias (VDG), off-state leakage is attributed to a trap-assisted tunneling (TAT) mechanism at the Si surface and is sensitive to the thickness of the Si-cap layer. At high VDG, the leakage increases with the Ge fraction in the strained $Si_{1-y}Ge_y$ and strain in the Si cap layer, consistent with band-to-band tunneling (BTBT) (Figure 2) [1]. The data illustrates trade-offs critical for optimizing the structures with respect to mobility, charge control, and leakage. The results of this work can be used to examine the design space for high-mobility p-MOSFETs. Increasing the Ge content in the SiGe channel increases mobility at the expense of off-state leakage. To minimize sub-threshold swing and increase high-field hole mobility, the Si cap must be as thin as possible. The bandgap and thickness of both the strained Si and strained $Si_{1-y}Ge_y$ layers are critical in determining off-state leakage and must be taken into account when optimizing the heterostructure and drain-region design.



▲ Figure 1: Mobility enhancement factor (referenced to Si control device) at N_{inv} of 10^{13} cm^{-2} versus Ge fraction in the strained layer for various levels of strain (y-x). Data from thin Si cap structures is shown (T_{Si}=2 – 4 nm).



▲ Figure 2: Drain current, I_D at VDG=2 V with VG=0 V for W=1000 µm, L=50 µm p-MOSFET. The Ge fraction in the substrate, x, (and hence the bandgap of the strained Si layer) is varied and Ge in strained layer is fixed at y=0.6 (squares). The Ge fraction in the strained layer, y, is varied on x=0.3 substrate (circles).

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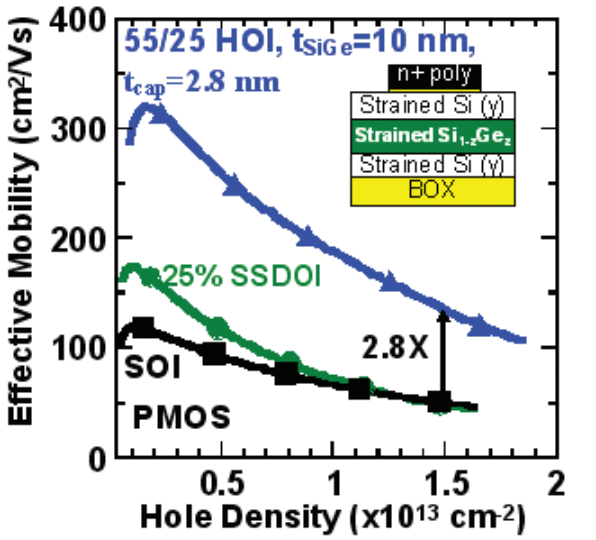
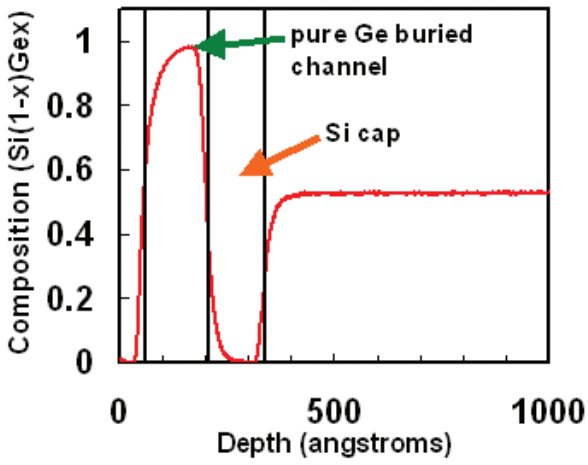
Strained Si/Strained Ge Heterostructure-on-Insulator

L. Gomez, M.K. Kim, C. Ní Chléirigh, I. Åberg, J.L. Hoyt
Sponsorship: MARCO MSD, Applied Materials

Scaling of device dimensions can no longer provide the necessary current drive enhancements to continue historic performance gains. Strain and novel channel materials can provide enhanced transport characteristics to increase device performance. Thin-body devices also provide the benefit of improved electrostatic control in deeply scaled MOSFETs. In previous work, thin-body MOSFETs were fabricated on strained Si/strained SiGe heterostructure on insulator (HOI) to realize enhanced transport for electrons and holes and improved subthreshold characteristics [1]. The HOI material was fabricated in MTL by epitaxial growth and transfer of the strained layers. Sub-threshold swing was observed to be 66-70 mV/dec, improved compared to similar heterostructure-on-bulk devices. Mobility enhancements of 1.9x and 2.8x were observed for electrons and holes, respectively, at an inversion charge density of 1.5 x 10^{13}. Figure 1 illustrates measured hole mobility for HOI MOSFETs with 55% Ge in the SiGe channel. With the potential to observe even higher hole mobility enhancement, with higher levels of strain and Ge content in the SiGe channel, we are developing pure Ge heterostructure-on-insulator. For heterostructure-on-bulk MOSFETs, Ge channels strained to a $Si_{0.5}Ge_{0.5}$ substrate have exhibited enhancement factors of 10x for holes [2]. In the present work, a process was developed to grow thin strained Ge on strained Si (strained to a SiGe substrate with 50% Ge). Figure 2 shows a secondary ion-mass spectrometry (SIMS) profile of the as-grown structure, prior to bond-and-etch-back. A low-temperature bond and etch back process has been developed for strained layer transfer. A low temperature process is critical to minimize both Ge diffusion and strain relaxation.



▲ Figure 1: Measured PMOS effective hole mobility for strained Si directly on insulator (25% SSDOI) and HOI with 55% Ge in the SiGe channel. The SSDOI and HOI materials were grown strained to SiGe virtual substrates with Ge contents of 25%, prior to layer transfer to form the on-insulator substrates. Total body thickness is approximately 17 nm.



▲ Figure 2: SIMS profile of top 1000A of the as-grown Ge HOI structure, prior to bond and etch-back. The complete tri-layer structure can be observed in the SIMS profile. It consists of a 134A Si cap, a 147A Ge buried layer, and an underlying 55A Si layer. Lines are drawn to guide the eye.

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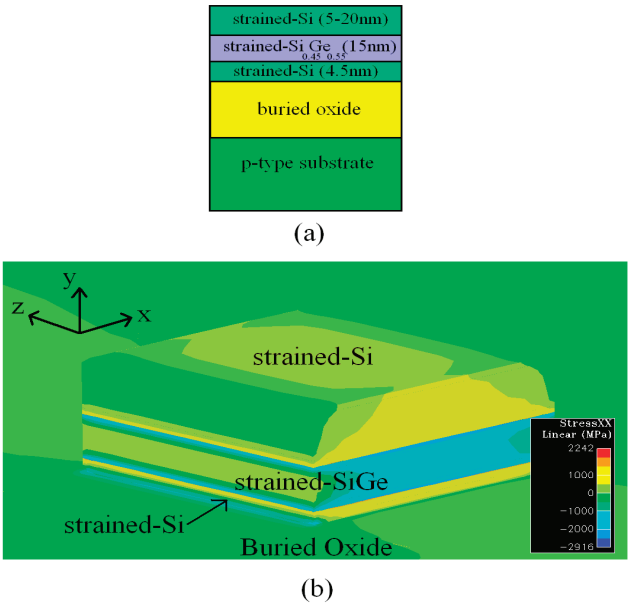
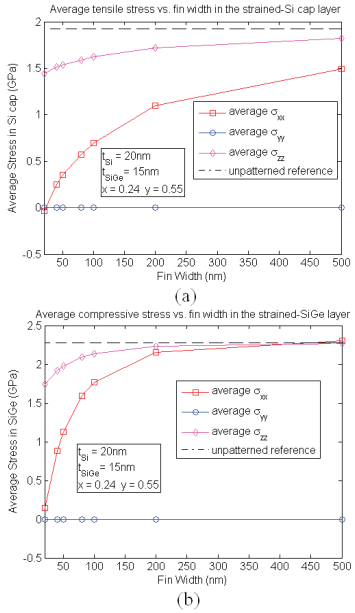
Patterning-induced Strain Changes in Strained Si/Strained SiGe Heterostructures

P. Hashemi, L. Gomez, J.L. Hoyt
Sponsorship: MARCO MSD

Multi-gate silicon-on-insulator (SOI) structures such as FinFETs are one of the promising candidates for deep sub-tenth-micron MOSFET technology due to their enhanced electrostatic control, which is particularly beneficial beyond 50-nm gate-lengths. On the other hand, strain engineering has been an effective means to increase device performance. Partial relaxation has recently been observed when patterning strained-silicon directly on insulator (SSDSOI) structures [1]. High-mobility strained-SiGeOI FinFETs that take advantage of stress-induced performance and immunity to the short-channel effects have also been reported [2]. In this work, we study the pattern-induced stress changes in strained Si/strained SiGe heterostructures on insulator (HOI). The goal is to engineer structures for fabrication of HOI multi-gate MOSFETs. The cross-sectional image of the HOI structure is schematically shown in Figure 1. A bond and etch-back technique is used to fabricate strained HOI substrates. The stress contours of 100-nm-square patterned HOI, simulated using Taurus™ 3D, are also shown in this figure. To engineer the stress in the channel for optimal HOI multi-gate MOSFET design, the effects of several parameters such as fin width, layer thicknesses and aspect ratios were analyzed. For example, the dependence of the average stress components on the fin width of the long-bar patterned HOI in (a) the Si-cap and (b) the SiGe layer (for nominal HOI parameters) are shown in Figure 2. As can be seen, σ_{xx} stress component is almost relaxed in deep-submicron fins where σ_{zz} is nearly maintained. To realize the fins under study, e-beam lithography will be utilized. Raman analysis will be used to verify the stress dependencies on geometry.



▲ Figure 1: (a) Schematic cross-sectional image of the biaxially-strained Si/SiGe/Si heterostructure on insulator and (b) the stress (σ_{xx}) contours of the 100 nm×100 nm patterned heterostructure indicating partially strain relaxation in the associated layers.



▲ Figure 2: Variation of the average stress components versus the fin width of the long-bar patterned heterostructures in (a) the Si-cap and (b) the SiGe layers.

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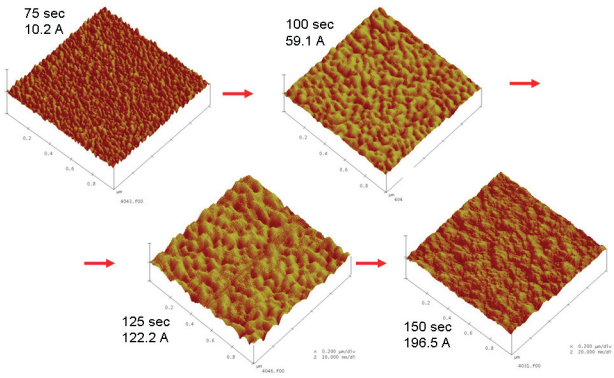
The Initial Stages of Ge-on-Si and Ge-on-SiGe Epitaxial Growth

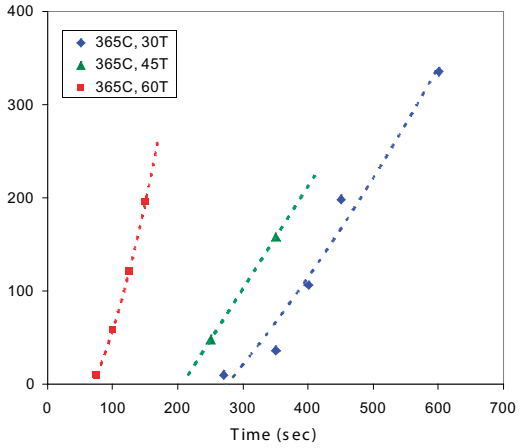
M. Kim, O.O. Olubuyide, L. Gomez, J.L. Hoyt
Sponsorship: DARPA, NSF Graduate Research Fellowship

Growing multilayer structures of Ge and SiGe on Si wafers has several applications to emerging technologies: thick, relaxed Ge films can be grown on a silicon substrate to make CMOS-compatible photodetectors, and thin, strained Ge and SiGe layers are used for enhanced-mobility heterostructure-on-insulator (HOI) MOSFETs. For all applications, it is desirable to grow flat, uniform films with minimal crystal defect density. Past work indicates that smooth, low- temperature Ge films with thickness of 30 to 60 nm can be grown in an LPCVD system [1]; however, the initial stages of Ge-on-Si and Ge-on-SiGe expitaxial growth with film thickness less than 10 nm has is not fully understood. In this project, we explore the morphology and growth rate for both strained and relaxed Ge films on Si and SiGe substrates.

Due to the 4% mismatch in lattice size, Ge on Si substrates show a 3-D growth mode, in which Ge initially forms islands and then coalesces to form a more uniform surface (Figure 1). The growth rate is non-linear during these initial stages. There appears to be an incubation period that depends on the growth parameters (Figure 2). Our findings show that the growth rate for Ge on Si (strained or unstrained) is slower than that of Ge on SiGe. For relaxed Ge on SiGe growth, the Ge film is smoother and growth rate is faster as the Ge content increases.



▲ Figure 1: 1 µm x 1 µm AFM scans of thin Ge films grown on Si substrates, showing the initial stages of Ge epitaxial growth. As the Ge layer gets thicker, the initial islanded morphology changes into a more uniform surface.



▲ Figure 2: The Ge thickness as a function of growth time. The graph suggests that there might be some incubation period for the initial Ge growth. Hydrogen flow for the 30T and 45T samples was 5 slpm to the slit valve and 0 slpm to the top inject. For the 60T sample, the H_2 flow was adjusted to be 5 slpm for both the slit and the top inject.

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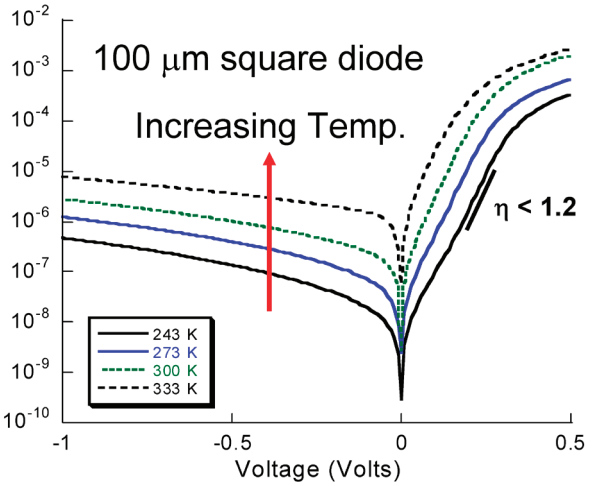
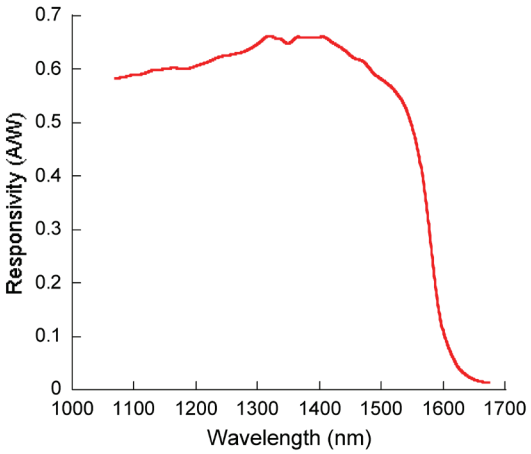
CMOS-compatible Epitaxial LPCVD Ge-on-Si Photodiodes

O.O. Olubuyide, M. Kim, J. Yasaitis, J. Michel, J. Liu, L.C. Kimerling, J.L. Hoyt
Sponsorship: Analog Devices, IBM, SRC

Germanium films have the required responsivity and speed to serve as photodetectors at the 1.55-μm wavelength range. Such detectors can be used in the communications field in a variety of high-speed systems, such as optical samplers. Therefore, integrating Ge films grown on silicon (Ge-on-Si) substrates into a CMOS-compatible process is an attractive goal for making arrays of on-chip detectors for use in a range of electronic and photonic integrated circuit applications. This study explores the growth properties and material quality of Ge-on-Si deposited by low pressure chemical vapor deposition (LPCVD) in an Applied Materials Epitaxial Reactor and the optical and electrical properties of Ge-on-Si photodiodes. It has already been demonstrated in ultra high vacuum chemical vapor deposition (UHVCVD) systems that depositing a low temperature Ge layer (seed layer), followed by the deposition of a high temperature layer (cap layer) with subsequent annealing can create a smooth, planar Ge film on a (100) silicon substrate with threading dislocation density on the order of 10^7 cm^{-2} [1]. We have adapted this two-step deposition process to an LPCVD system. We have explored the effect of growth pressure, temperature, and seed thickness on the material quality for blanket and selective epitaxial growth (SEG) of germanium. Our research identifies an optimum Ge seed layer deposition process window of 335°C ± 15°C and 30 T ± 10 T and demonstrates the requirement for a seed layer thickness above 30 nm. For SEG Ge-on-Si, a cap deposition condition of 600°C and 10 Torr appear to significantly reduce germanium nucleation on oxide films. After annealing at 900°C for 30 minutes, these blanket and selective Ge films have threading dislocation densities of ≤2 x 10^7 cm^{-2}. Photodiodes fabricated with the blanket Ge films have been measured to have a reverse leakage current less than 10 mA/cm^2 at a −1 volt bias (Figure 1), a 3-dB frequency response of 1.5 GHz for 40 x 100 μm rectangular diodes, and a responsivity of 0.5 A/W at 1.55 μm wavelength (Figure 2).



▲ Figure 1: Temperature-dependent IV curves between 243 – 333 K for a 100-μm square pin diode fabricated with a blanket Ge-on-Si film. The ideality factor is less than 1.2 for temperatures at or below 300 K. The perimeter-dominated leakage current increases with temperature, indicating a trap-mediated generation process.



▲ Figure 2: Responsivity as a function of wavelength for a 100-μm square *pin* diode fabricated with a blanket Ge-on-Si film. The responsivity is measured at a reverse bias of –1 volt, and an associated perimeter-dominated reverse-leakage current of 1.6 μA. The responsivity is 0.5 A/W at a wavelength of 1.55 μm.

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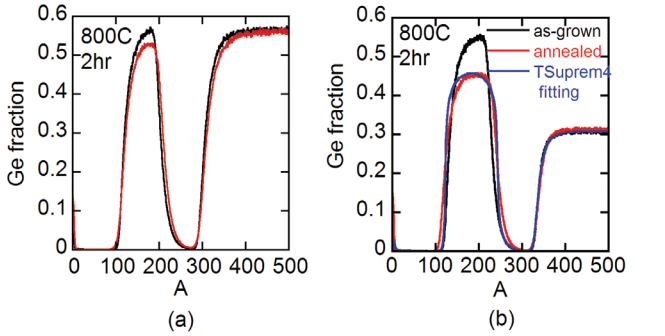
Interdiffusion in SiGe/Si Epitaxial Heterostructures

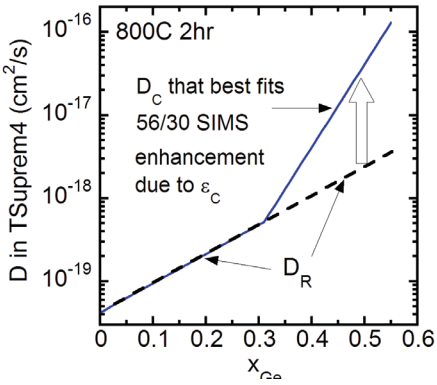
G. Xia, J.L. Hoyt
Sponsorship: MARCO MSD

In the past decade, SiGe-based strain and bandgap engineering have received increasing attention for CMOS applications. Carrier transport is enhanced by applying strain in the Si channel or by the use of strained SiGe or strained Ge as the p-MOSFET channel material, as in dual-channel, heterostructure-on-insulator (HOI), and heterostructure double-gate MOSFETs. One issue for these structures is interdiffusion at the Si/SiGe or Si/Ge interface during processing, which degrades device performance by reducing strain and carrier confinement and increasing alloy scattering. To date, research on Ge diffusion has been focused on Ge self-diffusion in $Si_{1-x}Ge_x$ [1] and interdiffusion in compressively strained SiGe superlattices with low Ge fractions ($x < 0.25$) grown on Si [2]. Basic understanding of interdiffusion, such as Ge fraction, strain, and temperature dependence, and interdiffusion modeling, is inadequate. In addition, little data is available for SiGe interdiffusion in device structures, such as strained Si/strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ with Ge content $y>0.3$.

In this work, we studied interdiffusion in pseudomorphic strained $Si/Si_{1-y}Ge_y$/strained Si/relaxed $Si_{1-x}Ge_x$ structures to emulate the interdiffusion in HOI devices. Boltzmann-Matano analysis is used to extract SiGe interdiffusivity experimentally from SIMS profiles of strained Si/relaxed $Si_{1-x}Ge_x$ structures. The TSuprem-4 simulations are then used to refine the interdiffusivity data. The Si-Ge interdiffusivity for strained Si/relaxed SiGe (D_R) was found to increase by 2.2 x for every 10% increase in local Ge fraction. We observed significantly enhanced Si-Ge interdiffusion in $Si_{1-y}Ge_y$ layers under compressive strain, as seen in Figure 1 [3]. A piece-wise exponential model was used in TSuprem-4 to extract interdiffusivity under compressive strain in the $Si_{1-y}Ge_y$ (D_C). The interdiffusivity was found to increase by 4.4 x for every 0.42% increase in compressive strain, which is equivalent to a 10% decrease in the substrate Ge fraction. These results were incorporated into an interdiffusion model that successfully predicts experimental diffusion profiles for various SiGe heterostructures.



▲ Figure 1: As-grown and annealed Ge profiles measured by SIMS for two strained $Si/Si_{1-y}Ge_y$/strained Si/relaxed $Si_{1-x}Ge_x$ structures. (a) y=0.56 x=0.56 and (b) y=0.56 x=0.30. Significantly enhanced interdiffusion is observed under compressive strain as seen in (b). The TSuprem-4 simulation is also shown in (b). The interdiffusivity model used in TSuprem-4 for this fit is shown in Figure 2 as the solid line.



▲ Figure 2: Piece-wise exponential interdiffusivity (solid blue line) extracted by fitting annealed SIMS profile in Figure 1 (b). For $x_{Ge} < 0.3$, $D = D_R$ (dashed black line), while for $x_{Ge} > 0.3$, $D = D_C$.

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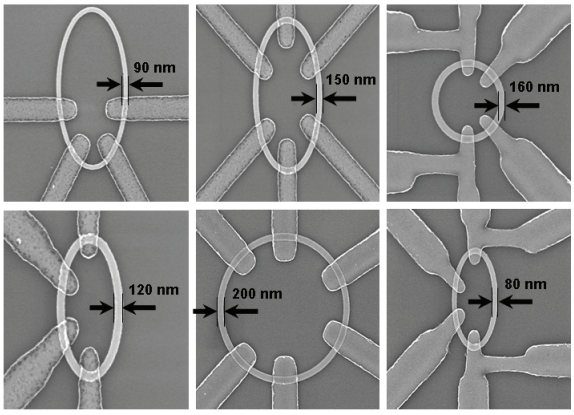
Magnetic Rings for Memory and Logic Devices

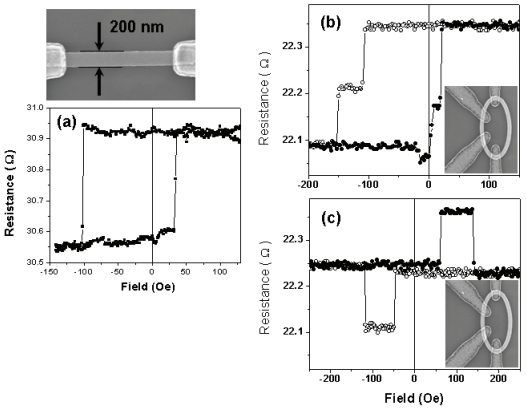
F.J. Castaño, D. Morecroft, W. Jung, J.D. Suh, C.A. Ross
Sponsorship: Cambridge-MIT Institute, Singapore-MIT Alliance, Outgoing Marie Curie Fellowship, NSF

We use fabrication processes combining electron-beam lithography and photo-lithography to create prototypes for magneto-electronic devices based on small ring- and bar-shaped multilayered magnetic elements with widths in the deep-sub-micron regime. These small structures have potential uses in magnetic-random-access memories (MRAM), magnetic logic devices, and other magneto-electronic applications. Current MRAM devices rely on bar-shaped multilayered magnets, containing two magnetic layers separated by a thin layer of either a non-magnetic metal (spin-valves) or an isolator (magnetic tunneling junctions). The resistance of such elements depends on the relative orientation (parallel or anti-parallel) between the magnetization in the read-out (free) and storage (pinned) layers. On switching back and forth the magnetization direction of the free layer two different resistance levels can be detected, allowing for a non-volatile bit of data ("0" or "1") to be stored in each element. As an alternative bit shape, MRAMs based on ring-shaped multilayered magnets have been recently proposed due to their robust magnetization reversal and the existence of flux-closure or "vortex" states.

We recently fabricated ring devices made from NiFe/Cu/Co/Au pseudo-spin-valves (PSVs) with non-magnetic contact-wires (see Figure 1). In these structures magneto-transport behavior is dominated by giant magnetoresistance (GMR). While the resistance of a PSV bar-shape element displays two resistance levels on cycling the free (NiFe) layer (Figure 2a), the rings display additional intermediate resistance levels [1] reached through abrupt transitions (Figure 2b). Additionally, the storage (Co) layer can be cycled into different states [1], allowing for profoundly different device responses on switching the free layer (Figure 2c). We have explored the switching mechanisms of PSV ring structures using micromagnetic simulations, as well as the effect of the contact configuration on the device response [2]. The sharp, low-field resistance changes in these PSV rings, which can be tailored by choice of ring dimensions and multilayer stack, will make them attractive for magnetoelectronic applications such as memories or logic devices that require multiple stable resistance levels. Most recently we are pursuing operating these devices using current pulses, rather than with an applied magnetic field.



▲ Figure 1: Scanning electron micrographs corresponding to elliptical and circular ring devices made from NiFe/Cu/Co/Au multilayers and Ta/Cu non-magnetic contact wires. The outer dimensions of the rings ranges from 930 nm to 20 μm and the widths from 80 nm to 350 nm.



▲ Figure 2: (a) Resistance versus applied field measurements on switching the free (NiFe) layer of a 200-nm-wide NiFe (6 nm)/Cu (5 nm)/Co (6 nm)/Au (4 nm) bar-shaped device. (b-c) resistance versus applied field corresponding to a 120-nm-wide NiFe (4 nm)/Cu (6 nm)/Co (8 nm)/Au (4 nm) elliptical ring, on switching the free layer with the storage layer in different states.

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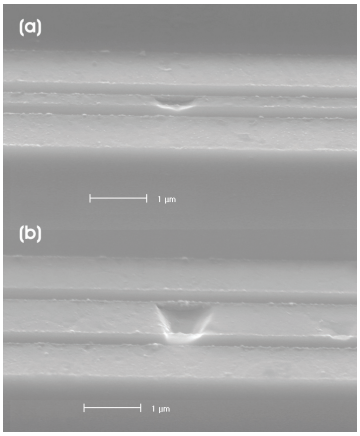
Surface Electromigration and Void Dynamics in Copper Interconnects

Z.S. Choi, R. Moenig, C.V. Thompson
Sponsorship: Intel, AMD, SRC

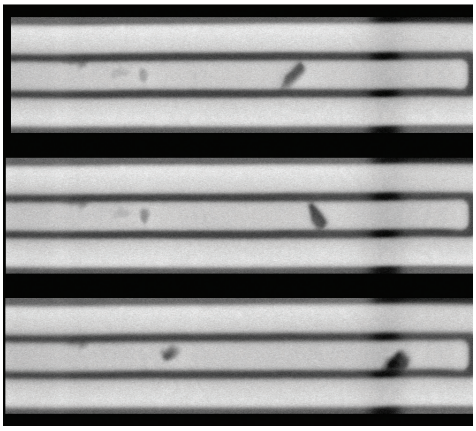
Electromigration is one of the main causes of failures in interconnects [1]. It has been shown that the dominant diffusion path in copper interconnect technology is the interface between the dielectric passivation layer and the copper line [2]. This interface is also the most prone to void nucleation and growth. The dynamics of these processes are critical since voids are the main cause of electrical failure of interconnects. We are carrying out two sets of experiments to investigate the details of void dynamics.

The first type of experiment is performed on interconnects without passivation layers to determine the dependence of copper surface diffusion and electromigration on different grain orientations. The samples are heated in reducing gas to remove copper oxide and then tested in a vacuum ($<10^{-7}$torr). The voids in these samples nucleate and grow at flux divergence sites (Figure 1). The flux divergences occur due to the differences in diffusivity for different grain orientations. After the electromigration tests, we obtain the crystallographic orientations of the grains surrounding the voids using electron backscattered diffraction (EBSD) in an SEM and correlate the results with differences in diffusivities between different grains.

In a second type of experiment, we take a fully fabricated sample and thin the passivation layer using a focused ion beam microscope (FIB), in order to be able to observe the underlying metal line in an SEM. We then test the samples at elevated temperatures in the SEM and observe the voids in the interconnects through the thinned passivation layer in real time, as Figure 2 shows. After the test, we remove the passivation layer and determine the effect of the grain orientations on void nucleation, growth, and motion. These experiments yield detailed information about the dynamics of voids in interconnects. The results can help to improve reliability analysis and design of interconnects.



▲ Figure 1: Voids in interconnects with no dielectric passivation layer, interconnects with length of1000 μm, depth of 0.45 μm, widths of a) 0.3 μm and b) 1.0 μm.



▲ Figure 2: *In situ* SEM images of the cathode of a test structure, showing void drift toward cathode end. The test line is surrounded by a Cu-extrusion monitor.

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[2] C.L. Gan, M. Burns, C.V. Thompson, K.L. Pey, W.K. Choi, H.L. Tay, B. Yu, and M.K. Radhakrishnan, "Effect of current direction on the lifetime of different levels of Cu dual-damascene metallization," *Appl. Phys. Lett.*, vol.79, no. 27, pp. 4592-4594, Dec. 2001.

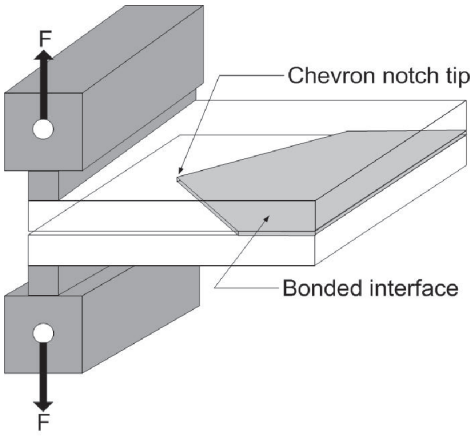
Bonded Copper Interconnects and Integrated Microchannels for 3D Integrated Circuits

R. Tadepalli, H.L. Leong, C.L. Gan, K.L. Pey, D.E. Troxel, K. Turner, C.V. Thompson
Sponsorship: DARPA (3D Integrated Circuits), Singapore-MIT Alliance, IME

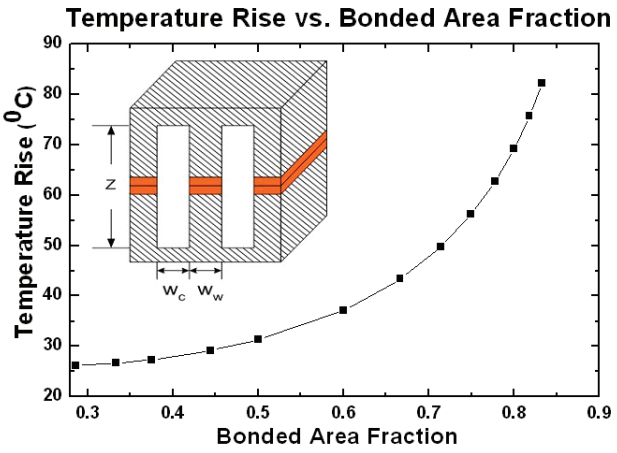
Performance of thermocompression Cu-Cu bonds is critical to reliability of devices created by stacking of individual wafers. Thermal effects in such 3D circuits are expected to be severe compared to conventional devices, owing to multiple heat generation locations and limited heat dissipation pathways. Bond quality and thermal performance issues in Cu wafer bonding technology are investigated using both experiments and modeling.

A novel test method (Chevron test) has been developed to complement the conventional four-point bend test, for bond toughness measurements. The Chevron test is used to measure Mode I (Tensile) toughness of Cu bonds (Figure 1). Nominal toughness values for Cu bonds created at 300°C as measured by Chevron and Four-point bend tests are 2.5 J/m^2 and 17 J/m^2, respectively, the difference attributed to plastic deformation of the Cu stack [1]. Therefore, the Chevron test gives a measure of the true interface strength, minus external contributions. The fundamental limit of Cu adhesion is probed using a UHV-AFM/deposition system. Force of adhesion between pristine oxide-free Cu surfaces deposited on a cantilever tip and a substrate is measured under UHV conditions. The room-temperature bond strength measured in the AFM set-up is comparable to 300°C wafer-level bond strength, thereby showing a significant dependence of bond quality on Cu surface cleanliness. Effects of process and film parameters on ultimate bond quality are being analyzed using bonded ECP damascene-patterned Cu interconnects (NTU, Singapore). Results indicate a strong dependence of bonded die yield on Cu film roughness and applied bonding load. An analytical model is being developed to explain these findings.

One solution to the heat dissipation problem in 3D circuits is integration of microchannels for microfluidic cooling in the 3D stack, using Cu-Cu bonds for channel sealing (Figure 2). The trade-off between cooling and bond strength has been analyzed to find optimum channel dimensions as a function of the achievable Cu-Cu bond strength.



▲ Figure 1: Schematic of Chevron test structure. Triangle-shaped bonded interface enables crack initiation at the notch tip.



▲ Figure 2: Temperature rise as a function of bonded area fraction for microchannel cooling. Lower bonded area fractions lead to increased channel density, and therefore, lower temperature rise. However, bond integrity is compromised at low bonded area fractions.

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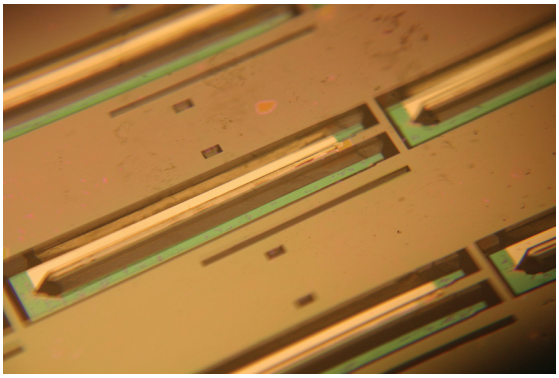
MEMS



▲ Fabricated reformer-burner unit with palladium membranes (K. Deshpande, M.A. Schmidt, K.F. Jensen, p. 119).

for additional reading...

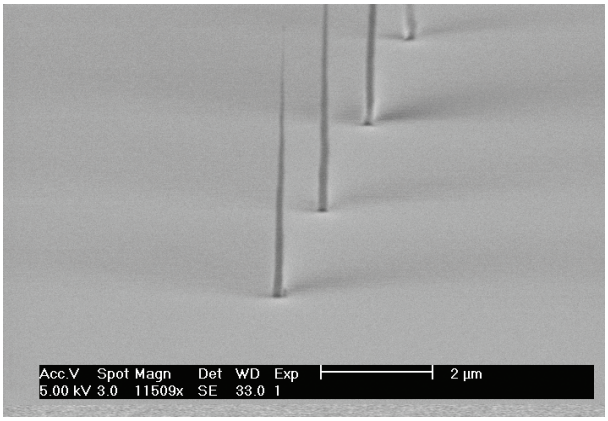
A Double-gated CNF Tip Array for Electron-impact Ionization and Field Ionization

L.-Y. Chen, L.F.V. Garcia, A.I. Akinwande
Sponsorship: DARPA

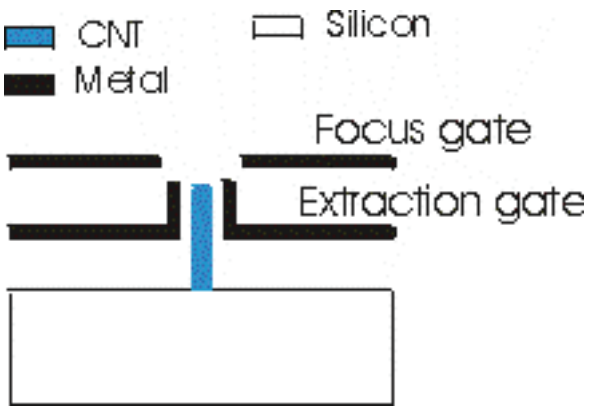
Carbon nanofibers have been investigated for a wide range of applications today. In particular, due to their remarkable conductivity, carbon nanofibers have generated a lot of interest for applications in vacuum microelectronic devices [1-2]. For example, the ionization sensor for gases is one of the most important applications since the conventional ionization sensors are bulky, require high-voltages, and consume high power. The purpose of this project is to fabricate carbon nanofiber field emission and field ionization arrays, which can be utilized in a micro-gas sensor. This device can help reduce the size of the sensor and operating voltages required for gas analysis.

In this project, the PECVD method is used to grow vertically oriented carbon nanofibers. The number of carbon nanofibers per site is controlled by the Ni catalyst dot size. It has been demonstrated that the diameter of the Ni catalysts disk must be 300 nm or less to ensure the growth of only a single carbon nanofiber [3]. The 250-nm Ni dots used in this work were defined by ebeam lithography. Figure 1 shows a close-up SEM picture of vertically aligned single carbon nanofiber array grown by PECVD. Later, these vertically-aligned single carbon nanofibers will be integrated into a double-gated field emission/ionization structure developed by L. Dvorson [4]. Figure 2 shows the schematic drawing of the final device.

Using the device shown in Figure 2, two approaches for ionizing gas molecules will be investigated for micro-gas sensors. One approach is electron impact ionization, which uses strong electric fields to emit electrons followed by collision between the energetic electrons and neutral gas molecules resulting in ionization. The second approach is field ionization, which is a gentler process in comparison to electron impact ionization. It results in molecular ionization and a simpler mass spectrum due to lower fragmentation of molecules.



▲ Figure 1: A close-up SEM picture of vertically aligned single carbon nanofiber grown in an array patterned by PECVD.



▲ Figure 2: The schematic drawing of the CNF field emission and field ionization device.

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[2] W. Zhu, C. Bower, O. Zhou, G. Kochanski, and S. Jin, "Large current density from carbon nanotube field emitters," *App. Phys. Lett*, vol. 75, no. 6, pp. 873-875, Aug. 1999.

[3] K.B.K. Teo, S.-B. Lee, M. Chhowalla, V. Semet, V.T. Binh, O. Groening, M. Castignolles, A. Loiseau, G. Pirio, P. Legagneux, D. Pribat, D.G. Hasko, H. Ahmed, G.A.J. Amaratunga, and W.I. Milne, "Plasma-enhanced chemical vapour deposition carbon nanotubes/nanofiberes- how uniform do they grow?" *Nanotechnology*, vol. 14, no. 2pp. 204-211, Feb. 2003.

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Hand-assembly of an Electrospray Thruster Electrode Using Microfabricated Clips

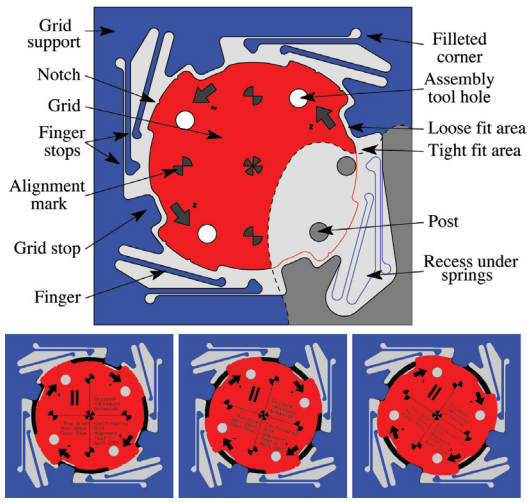
B. Gassend, L.F. Velasquez-Garcia, A.I. Akinwande, M. Martinez-Sanchez
Sponsorship: AFOSR, DARPA

This work [1] explores a method to precisely assemble two planar MEMS components. Our intended application is the assembly of the extractor electrode of an electrospray thruster, in which holes in the extractor must be aligned precisely with emitter needles or ridges (see [2] in this volume). In this method, the components can be accurately assembled by hand. Moreover, the assembly is made using a system of flexures, allowing considerable flexibility in the choice of materials and coatings for the components.

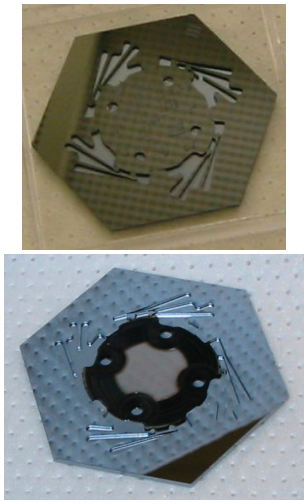
Figure 1 shows a diagram of our device. The extractor electrode (red) needs to be assembled in a recess on the base of the electrospray thruster (blue). To do this, the extractor is placed by hand in its recess. This step is easy as there are a few hundred micrometers of slack. The extractor is then rotated. As it rotates, features around its periphery force it to align its center to within 50 micrometers of its final position. As it continues the rotation, flexible fingers on the base part get flexed by the extractor, until the fingertips fall into notches in the sidewalls of the extractor.

Our devices, shown in Figure 2, were initially made out of Silicon using deep reactive-ion etching (DRIE). To show the flexibility of the method, we have also produced laser-cut polyimide extractors. The polyimide extractors have allowed us to achieve electrical insulation between the extractor and the rest of the device, which is vital for our intended application.

We have measured front-to-back alignment on all our silicon devices and found that they are within 9 micrometers RMS of their intended location. However, multiple assembly/disassembly cycles on a specific device show that the position is repeatable to within 1.5 micrometers of standard deviation. This measurement suggests that much of the misalignment we are observing occurs due to misalignments during the various photolithography and bonding steps.



▲ Figure 1: Diagram of the device (top). Main assembly steps (bottom): first the extractor is placed in its recess, then it is brought into rough alignment, and finally the fingers lock into their notches.



▲ Figure 2: Pictures of some assembled devices: a silicon extractor (top), an aluminum coated polyimide extractor (bottom).

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[2] B. Gassend, L.F. Velasquez-Garcia, A.I. Akinwande, and M. Martinez-Sanchez, "A fully microfabricated array of electrospray ridge emitters for space propulsion applications," Massachusetts Institute of Technology, Cambridge, MA, Microsystems Technology Laboratories Annual Research Report, 2006.

A Fully Microfabricated Planar Array of Electrospray Ridge Emitters for Space Propulsion Applications

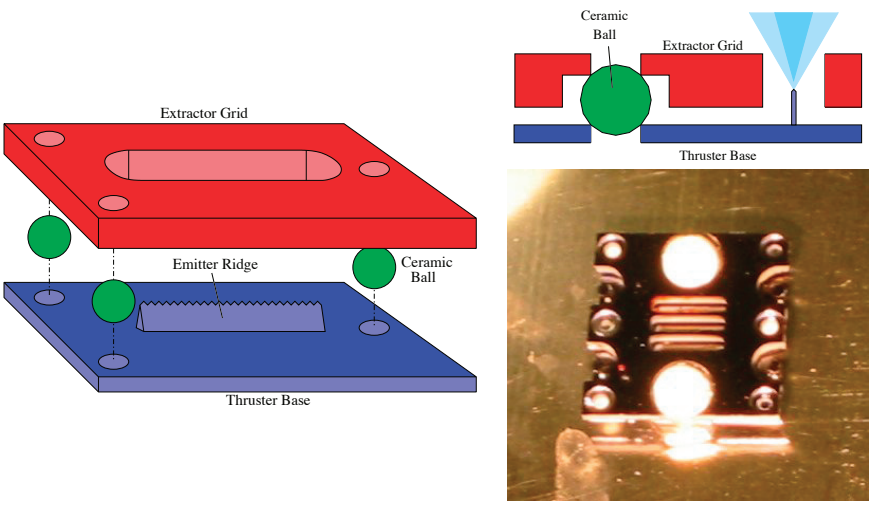
B. Gassend, L.F. Velasquez-Garcia, A.I. Akinwande, M. Martinez-Sanchez
Sponsorship: AFOSR, DARPA

Electrospray thrusters work by extracting ions or charged droplets directly from a liquid surface using an electrostatic field and accelerating them in that field to produce thrust. This method could lead to more efficient and precise thrusters for space propulsion applications. The propellant liquid is generally placed at the tip of a needle to enhance the electrostatic field. The electrospray process limits the thrust from a single emitter needle. To get into the millinewton range will require an array with thousands of emitters. Batch microfabrication is well suited to making such an array.

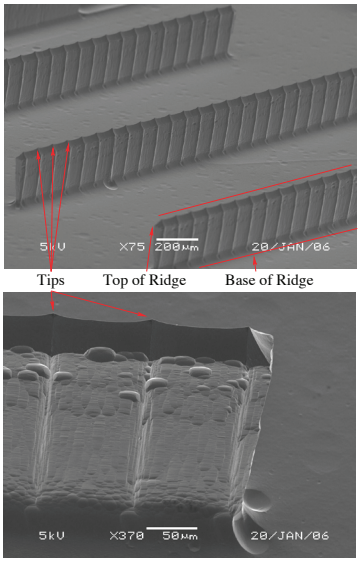
We have designed and built a prototype thruster that consists of two silicon parts (Figure 1) made using deep reactive ion etching (DRIE) and SF6 plasma etching. The thruster base holds the electrospray emitters. Its surface is treated to control the areas where propellant can go. The extractor produces the electric field, which generates the electrospray. It is equipped with slits to allow the accelerated particles through. The two parts are positioned relative to each other using a kinematic mount, in which alumina balls rest in holes on the silicon dies (Figure 1). Alumina screws hold the assembly together.

In this design, we have replaced the needles that are typically used in electrospray thrusters by ridge emitters: vertical slabs with sharp tips spaced along their length (Figure 2). We have shown that our process for needles [1] can be extended to ridge shapes, and a modeling effort is underway to better control the shapes of the emitters.

Our thruster has been fired with the ionic liquid EMI-BF4. This experiment shows successful electrical insulation, even in the presence of the liquid. Challenges we now face are reducing the amount of emission that is intercepted by the extractor and determining where on the ridges the emission is coming from.



▲ Figure 1: Diagrams and picture of an electrospray thruster in which the extractor grid (red) is aligned to the base (blue) using ceramic balls (green). In the picture, the white alumina balls are visible in the top-left, bottom-left and center-right. Three slits in the center accommodate three ridge emitters.



▲ Figure 2: Three parallel ridge emitters with tips spaced 100 micrometers apart (top). Close-up on one of the ridges (bottom).

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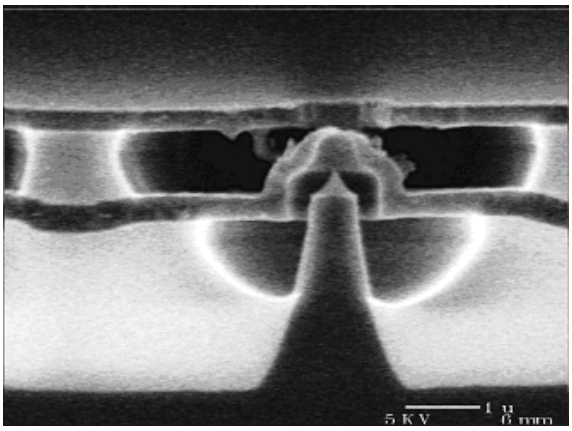
A Double-gated Silicon Tip, Electron-Impact Ionization Array

L.-Y. Chen, A.I. Akinwande
Sponsorship: CreatV Micro Tech, NIH, DARPA

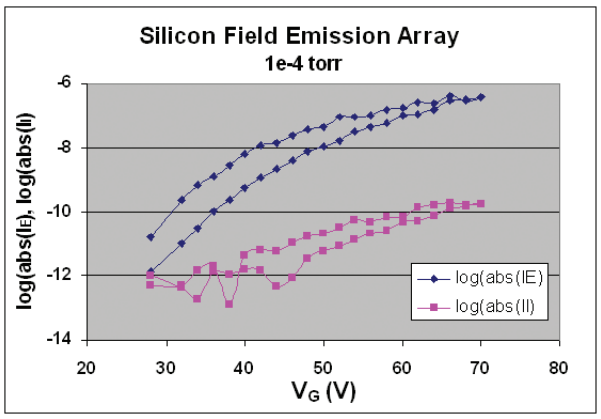
A device with the ability to ionize gases is needed for a variety of applications, of which the mass spectrometer (MS) [1-2] is one of the most important. The ionization method in the majority of gas analyzers in MS is electron-impact ionization, which uses a beam of electrons that collides with gas molecules. Through this collision process, energy is transferred from the electrons to the gas molecules, which causes electrons on the gas molecules to be stripped off (i.e., ionization of the gas molecules).

Traditionally, thermionic emission, which consists of a filament that produces electrons when heated, is the most common way of generating electrons for MS using electron impact ionization. However, thermionic emission has several disadvantages: slow switch-on time, large power consumption, and lack of robustness. These disadvantages, however, are eliminated when field emission is used instead.

In this project, a double-gated silicon field emission device is used to generate the electron source for electron impact ionization. Figure 1 shows a SEM picture of a double-gated silicon field emission device used here. Using this device, we have demonstrated the linear relationship between the emission current (IE) and the ion current (II) at a fixed pressure (10-4 torr) as shown in Figure 2.



▲ Figure 1: The SEM picture of the cross section of the silicon field emission and field ionization array.



▲ Figure 2: Plot of emission current (I_E) and ion current (I_I) versus gate voltage (VG).

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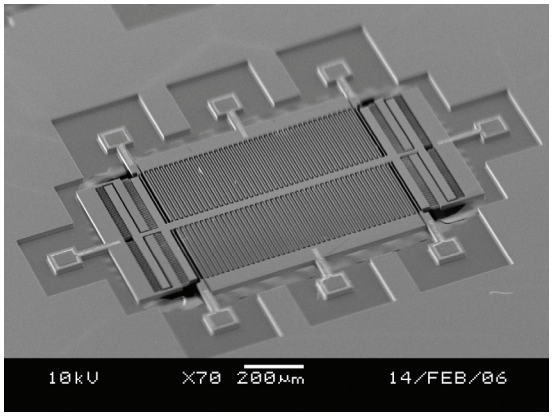
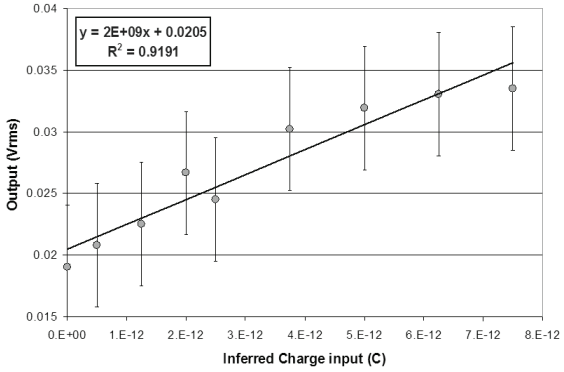
A MEMS Electrometer for Gas Sensing

J. Lee, L.F. Velásquez-García, A. Seisha, A.I. Akinwande
Sponsorship: DARPA

The DARPA-funded micro gas analyzer program aims to develop portable, low-power, fast, and reliable gas analyzer technology for a wide range of applications. The system architecture of the gas analyzer contemplates a MEMS electrometer at the end of the system. The electrometer characterizes the ionized species that are filtered by the quadrupole. The sensitive element of the electrometer is a MEMS structure embedded in a feedback loop of a precise oscillator circuit. The electrometer has a comb drive that sets the electrometer to oscillate. Shifts in the oscillation frequency are related to changes in the capacitance of the electrometer due to ion interception. The resolution of the device is estimated at 100 e/√Hz in vacuum [1]. Figure 1 shows a fabricated MEMS electrometer. Figure 2 shows the experimental data of one of these MEMS electrometers, in air. The experimental resonant frequency is 6.2 kHz, and the conversion gain was estimated at 2×10^9 V/C (theoretical value is 7×10^9 V/C). Current research focuses on implement lock-in detection, which will remove the noise from the drive signal because the output has twice the frequency of the input signal.



▲ Figure 1: A micro-fabricated MEMS electrometer. The comb drive (central part) sets the electrometer in oscillation. Changes in the variable capacitors (comb structures at both sides of the central comb drive) cause shifts in the oscillation frequency that are directly related to the ion current that impact the MEMS.



▲ Figure 2: Voltage versus charge characteristics for the MEMS quadrupole in air.

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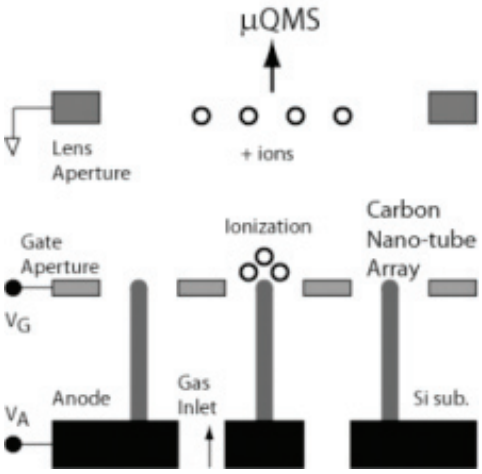
[1] P. Riehl *et al.*,"Electrostatic charge and field sensors based on micro-mechanical resonators," *J. of Micromechanical Systems*, vol. 12, no. 5, p. 577, Oct. 2003.

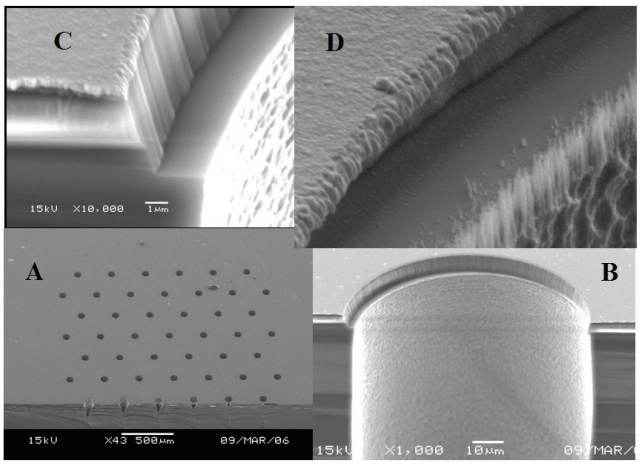
A Single-Gated CNT Field-Ionizer Array with Open Architecture

L.F. Velasquez-Garcia, L.Y. Chen, A.I. Akinwande
Sponsorship: DARPA

The micro gas analyzer project aims to develop the technology for portable, real-time sensors intended for chemical warfare and civilian air purity control. The device is composed of four micro-fabricated subsystems: an ionizer, a mass filter based on a quadrupole array [1], an electrometer [2], and a positive displacement pump [3]. We are developing a single-gated fieldionizer array based on gated carbon nanotubes (CNTs). The devices achieve species ionization by tunneling of outer shell electrons due to the presence of high electric fields that the device sets. We use CNTs as field enhancers because of their small radii and high aspect ratio while the gate proximity ensures high fields at low voltage. State-of-the-art ionizers use electron-impact ionization (thermionic cathodes), incurring in excessive power consumption, low current, current density, ionization efficiency, and short lifetime. The field-ionizer arrays (Figure 1) are able to soft-ionize species, thus achieving molecule ionization. The reliability and lifespan of the field-ionizer arrays are larger than the corresponding values for electron-impact ionizer arrays because the CNTs are biased at the highest potential in the circuit, thus making it unlikely for ionized molecules to back-stream. Figure 2 shows two SEM pictures of a single-gated CNT array that implements a selective CNT-growth process. This process reduces the fabrication complexity of the device because it grows CNTs from an un-patterned catalyst (Ni). Current research efforts concentrate on improving the device and data acquisition, including benchmarking the performance of the ionizer in low-pressure oxidizing environments.



▲ Figure 1: Schematic of a field-ionizer array. The gas inlet provides neutral species to the field enhancers. If the molecules of the gas come close enough to the CNT tips, an electron from the outer shell of the molecule will tunnel to the CNT, thus ionizing the molecule.



▲ Figure 2: A single-gated CNT field-ionizer array grown at MIT. (A) Field view of an array section; (B) cross section of a single ionizer well; (C) detail of the well foot intended to grow CNTs; (D) detail of the well foot when CNTs are grown. The ionizer well has a film of silicon dioxide 5-µm-thick below the gate that acts as electrical insulator between the gate and the CNTs. The gate can be made of either Ti, Au, or W. The CNT catalyst was 4-nm-thick Ni.

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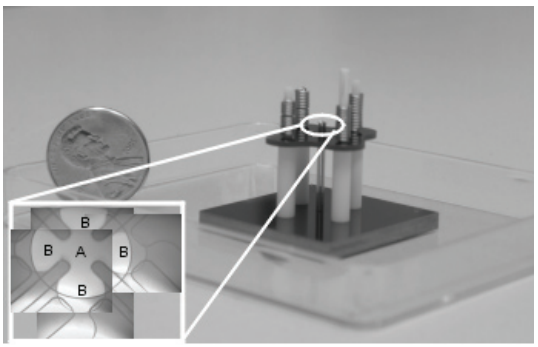
[3] H.Q. Li, *et al.*, "A high-frequency, high-flow-rate piezoelectrically-driven MEMS micro-pump," in *Proc. IEEE Solid State Sensors and Actuators Workshop*, Hilton Head, SC, June 2000.

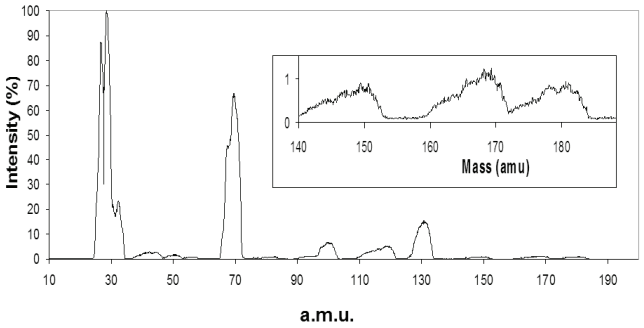
A MEMS Quadrupole that Uses a Meso-scaled DRIE-patterned Spring Assembly System

L.F. Velásquez-García, A.I. Akinwande
Sponsorship: DARPA

The DARPA-funded micro gas analyzer program aims to develop portable, low-power, fast, and reliable gas analyzer technology for a wide range of applications. One of the subsystems of the gas analyzer is a mass filter. An array of micro-fabricated quadrupole mass filters is being developed for this purpose. The quadrupoles will sort out the ions based on their specific charge. Both high sensitivity and high resolution are needed over a wide range of ion masses, from 20 to 200 atomic mass units. In order to achieve this performance, multiple micro-fabricated quadrupoles, each operating at a specific stability region and mass range, are operated in parallel. The proof-of-concept device is a single, linear quadrupole that has a micro-fabricated mounting head with meso-scaled DRIE-patterned springs. The mounting head allows micron-precision hand assembly of the quadrupole rods [1]–critical for good resolution and ion transmission. The micro-fabricated mounting head can implement quadrupoles with a wide range of aspect ratios for a given electrode diameter. There are currently two versions of the mounting head, able to interact with rods of diameters equal to 1588 and 559 micrometers. The choice of electrode diameter results from pondering the dimensional uncertainties and alignment capabilities with respect to the expected resolution and transmission goals. Figure 1 shows an assembled MEMS quadrupole, including some detail of the spring structure near the quadrupole transmission region. The quadrupoles that have been implemented so far span the aspect ratio range from 30 to 60. Figure 2 shows the experimental data of one of these quadrupoles on a FC-43 sample, where a mass resolution of 2 amu and a full mass range of 200 amu are demonstrated, while using a 1.2-MHz RF power supply to drive the quadrupole. Current research efforts concentrate on developing RF power supplies of higher frequency to obtain better performance from the same device.



▲ Figure 1: A micro-fabricated quadrupole with electrode diameter equal to 559 micrometers, near a 1-cent coin for size reference. The micro-fabricated part of the device is the square base, which contains a system of meso-scaled DRIE-patterned springs. The structure of the quadrupole spring head near the transmission region is shown in a set of superimposed IR microscope pictures (lower left corner). The electrodes occupy the four cavities (A) that surround the axis of the quadrupole (B). The ion transmission occurs through the latter region.



▲ Figure 2: Experimental characterization of a MEMS quadrupole, using the compound FC-43 to get peaks in the 1 – 200 amu mass range. The resolution is estimated at 2 amu, using an 1.2 MHz RF power supply On the upper right corner there is a zoom of the data near 200 amu.

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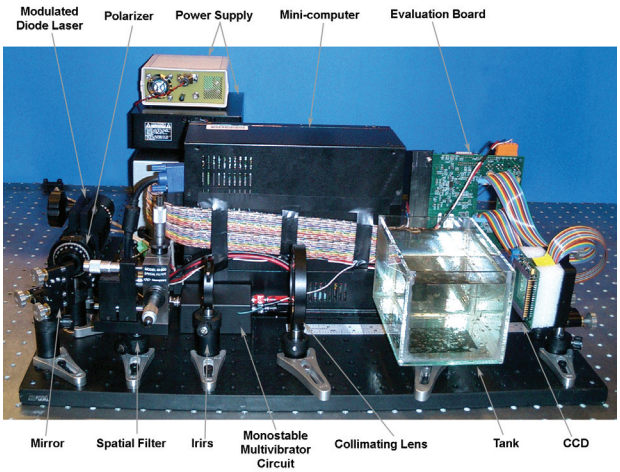
Digital Holographic Imaging of Micro-structured and Biological Objects

J.A. Dominguez-Caballero, N. Loomis, J.H. Milgram, G. Barbastathis
Sponsorship: MIT Sea Grant

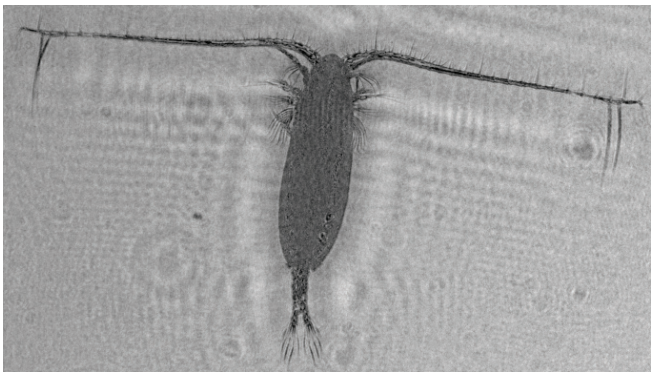
The need for understanding the trophodynamics of the ocean has led to the development of several instruments for monitoring plankton communities, critical indicators of the ocean's health and the base of the aquatic food chain. The three competing methods for plankton observation utilize direct, acoustic, and optical sampling techniques; however none of the current systems can provide the complete data set required for predictive modeling capabilities. The goal of this project is to develop a small, low-power, digital holographic imaging (DHI) system that allows for *in situ* monitoring of plankton and other aquatic communities. This system allows microbiologists to collect high-resolution, spatio-temporal data on species-specific population structures. In addition to biological studies, the DHI camera can be utilized in diverse areas such as medical analysis, quality control inspection, and MEMS device characterization.

DHI uses a digital sensor to record holograms, formed by the interference pattern between a reference wave and a field produced by scattered light from an illuminated object. The illumination source is coherent and typically provided by a laser. The recorded images are processed on a computer to reconstruct the original object field at a given axial location [1]. From the reconstructed images, information about the object such as morphology, topology, and 3D coordinates can be computed throughout a large sample volume. In addition, velocity and 3D trajectories are available under slightly modified methods.

Experiments have focused on biological applications, including marine and microbial organisms ranging from 5 to 2000 microns. In addition to the inline configuration (Figure 1), several setups have been implemented to explore smaller scales, including the use of spherical reference waves, 4f telescopes, and microscope objectives. Figure 1 shows our compact benchtop prototype DHI camera, currently being developed to be used as a sea-going instrument for deep-sea microbiology. Using a lens-free spherical configuration with a working distance of 50 mm, all lines on a 1951 USAF resolution target can be resolved, down to 2.2 microns in width. A 4f system was used to track the trajectories of 7 micron algae over several seconds. Small plankton, 50 to 500 microns long, have been imaged using all three setups with excellent clarity. Figure 2 shows a reconstruction from an inline configuration of an adult copepod. Future work includes incorporating the DHI camera into an underwater vehicle. Additional work will focus on tracking small particles under turbulent flow conditions.



▲ Figure 1: The compact DHI camera developed for use in a deep-sea-going vehicle. An inline configuration is shown.



▲ Figure 2: Reconstruction of an adult copepod (*Calanus finmarchicus*) using the in-line setup with a modulated diode laser. The reconstruction distance is 101 mm.

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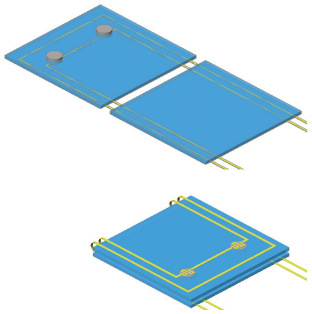
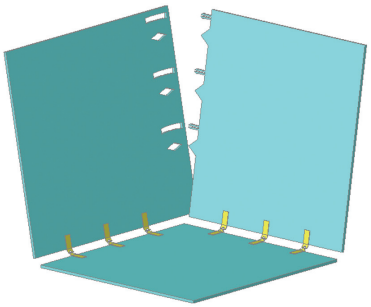
Aligning and Latching Nano-structured Membranes in 3D Micro-Structures

N.S. Shaar, G. Barbastathis, C. Livermore
Sponsorship: ISN

The 3D micro-electro-mechanical systems (MEMS) manufacturing is an emerging technology that promises to solve many of the problems in the microfabrication industry. In microelectronics, as the feature sizes of the components approach their physical limits, packing more transistors on a microprocessor or on a memory chip requires expanding the circuitry into the third dimension. In optical switches, the traditional 2D MEMS-based switches do not scale easily beyond 32 ports; to increase the number of ports, companies have been developing 3D micro-mirror arrays that can reflect light in multiple directions. The Nanostructured Origami™ 3D fabrication process is a two-step method for fabricating 3D MEMS; it involves patterning films on a surface and then folding the patterned films to create three-dimensional structures [1]. This method is advantageous because it uses state-of-the-art 2D patterning methods and it involves patterning all the parts of the structure in one step, eliminating problems of feature misalignment. However, in creating the 3D structures, two major challenges arise; the first is to accurately place the folded membranes in their desired positions and the second is to fix the membranes in those positions to maintain the final 3D configuration. Current positioning solutions involve the use of mechanical motion-limiters that prevent folded membranes from moving beyond a certain point [2]. We propose two methods for aligning and latching folded nano-patterned membranes in 3D microstructures. The first method uses photoresist pads to glue together two mating surfaces of the structure (Figure 1). What distinguishes this method from previous polymer gluing attempts is that we use dense gold patterns as a local heater to melt the photoresist pads. This allows us to control the membranes we latch and the time when we latch them. We use patterned gold wires to form the hinges that hold the membranes together. Thin dense gold patterns also serve as local heaters to melt the photoresist gluing pads. The surface tension in the molten pads aligns the surfaces and solidification of the photoresist latches them together. The second method uses mechanical alignment and latching features that allow edges-to-surface latching (Figure 2). One major advantage of this method is that the structural components and the alignment features are patterned in the same lithographic step, which lowers costs and minimizes misalignment errors. Another interesting aspect is the cascaded alignment; the alignment features are designed so that they function sequentially, starting from the features closest to the hinge. With proper design of those features, the alignment system can achieve accurate positioning using the features away from the hinge while tolerating a large initial positioning error range by virtue of the short radius sustaining the features closest to the hinge.



▲ Figure 1: Surface-to-surface alignment and latching of membranes by local heating of photoresist pads.



▲ Figure 2: Edge-to-surface alignment and latching of folded membranes using mechanical features.

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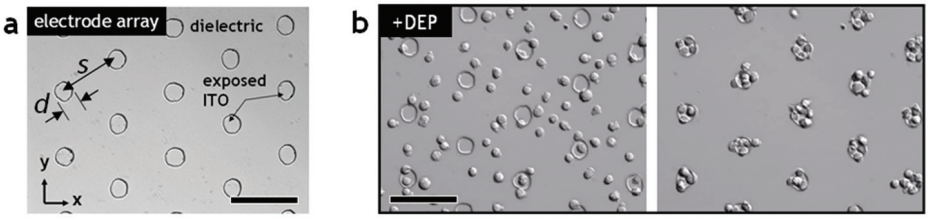
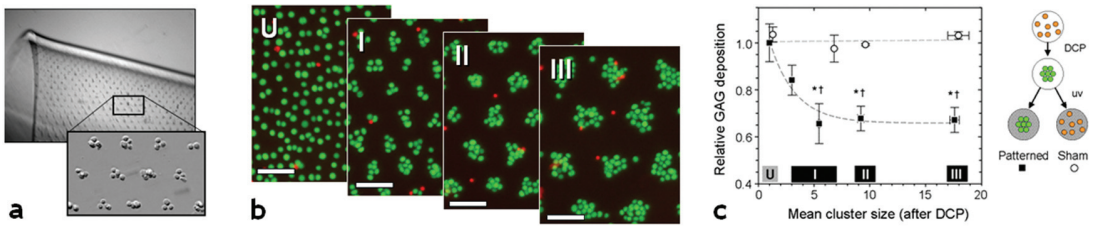
A Microfabricated Platform for Investigating Multicellular Organization in 3-D Microenvironments

D.R. Albrecht, R.L. Sah, S.N. Bhatia
Sponsorship: Whitaker Foundation, NSF, NIH

Understanding how complex intrinsic and external cues are integrated to regulate cell behavior is crucial to the success of cell-based therapies in the treatment of human disease. Systematic and quantitative investigation of these microenvironment signals was first enabled by precise cell positioning using 2-D micropatterning tools [1]. However, cellular signaling is often altered in adherent tissue culture where structural cues are lacking (including tumor, stem, and differentiated cells), in contrast to 3-D culture systems that more closely resemble *in vivo* cell behavior [2]. Our goal was to develop new micropatterning tools capable of micron-scale cell patterning and organization within a 3-D hydrogel with tissue-like properties. We developed a technique for the rapid formation of reproducible, high-resolution, 3-D cellular structures within a photo-crosslinkable hydrogel using dielectrophoretic forces (Figure 1) [3]. We demonstrate parallel formation of ~20,000 cell clusters of precise size and shape within a 1 x 2 cm^2 slab of tissue (Figure 2a), with high cell viability and differentiated cell function maintained over 2 weeks in culture. By modulating cell-cell interactions in clusters of various size (independent of hydrogel geometry, chemistry, or volumetric seeding density; Figure 2b), we present the first evidence that 3-D microscale tissue organization regulates chondrocyte behavior (Figure 2c) [3]. This dielectrophoretic cell patterning (DCP) technology enables further investigation of the role of tissue architecture in many other multicellular processes from embryogenesis to regeneration to tumorigenesis.



▲ Figure 1: Rapid, parallel dielectrophoretic cell patterning method. (**a**) Assembled DCP chamber viewed in inverted microscopy demonstrates the hexagonal electrode array. (**b**) Swiss 3T3 fibroblasts before and after electropatterning within a 15 wt% PEG-diacrylate prepolymer (viscosity: 3.3 cP) by +DEP toward high electric field at the electrodes, s = 100 μm apart, after 60 s exposure to 3.0 V_{rms} at 3.0 MHz.



▲ Figure 2: Microscale organization alters cell function. (a) Thousands of micropatterned cell clusters are embedded within a thin hydrogel. (b) Cluster size (and cell-cell interaction) can be varied from single cells (U) to large clusters (III) within a single hydrogel slab. Cells have high viability (green), indicated by fluorescent staining. Scale bars, 100μm. (c) In articular chondrocytes, biosynthesis of a matrix molecule, GAG, is downregulated over 14 days in clusters of increasing size, independent of volumetric seeding density. "Sham" DCP hydrogels, in which cells were initially electropatterned but then randomized prior to hydrogel crosslinking, were indistinguishable from unpatterned controls. Data are mean ± s.e.m., n = 5 - 6. *, p<0.001 vs. "U"; †, p<0.001 vs. "Sham."

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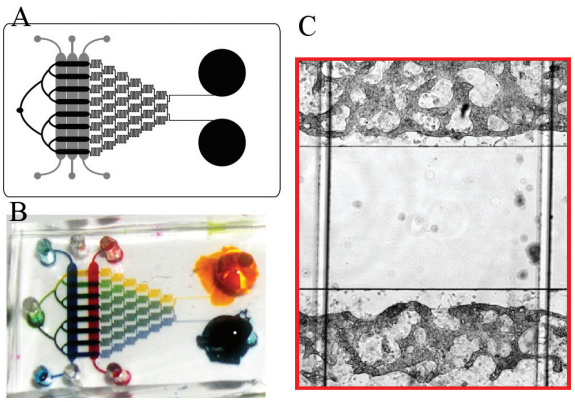
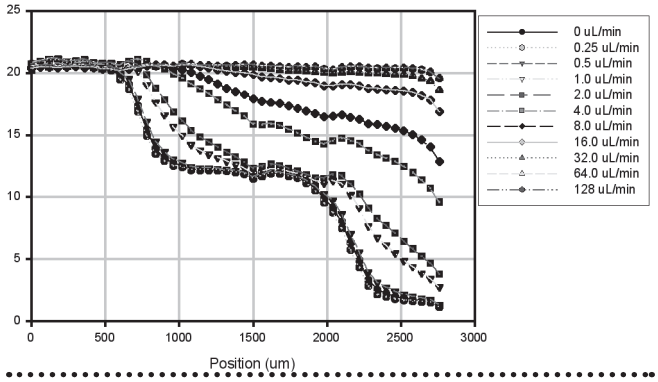
Microfluidic Hepatocyte Bioreactor

D.T. Eddington, S.N. Bhatia

This project utilizes microfluidic systems to study how groups of liver cells acquire emergent tissue properties. Hepatocytes (the parenchymal cells of the liver) respond to many cues in their microenvironment: neighboring cells, growth factors, extracellular matrix, dissolved oxygen, and their interactions. One tissue property of interest is the compartmentalization of gene expression in multicellular domains along the liver sinusoid. This process, often described as "zonation," underlies much of liver physiology and regional susceptibility to toxins. We have previously shown oxygen gradients can be used to compartmentalize mixed populations of hepatocytes in a large-scale reactor [1]. Here, we present a microdevice that enables one to explore the crosstalk between two inputs (oxygen gradients and soluble growth factors) in a systematic fashion. The device consists of a two-layer PDMS microfluidic network with an on-chip dilution tree bound to a glass slide with an array of microreactors. Hepatocyte zonation is induced in each microreactor through local oxygen concentration, which is modulated through gas channels separated from the bioreactor by a 100-μm PDMS layer as shown in Figure 1. The local oxygen concentration in the microchannels is quantified in Figure 2. Primary rat hepatocytes are seeded into microreactors together with 3T3 fibroblasts, which act to stabilize the hepatocyte phenotype as described previously. This device will be useful to further explore liver tissue biology *in vitro* including the dynamics of zonation, mechanisms of oxygen sensing, and the role of growth factors in zonal response.



▲ Figure 1: A.) Schematic and B.)Picture of the microfluidic network. Two inlets (yellow and blue) feed a dilutiongradient generator to yield a titration, which feeds into 8 discreet bioreactors. Gas channels (dyed red and blue) run perpendicular to the bioreactors and each connected to a separate gas cylinder with a premixed oxygen concentration (21%, 10%, and 1 %). The gas channels are separated from the PDMS microchannels through a thin PDMS membrane. C.) Magnification of the red box in A showing two bioreactors and the gas channels. The arrows indicate how the gas and liquid flow in the channels.



▲ Figure 2: Oxygen concentration along the length of the bioreactor as a function of distance and flow rate. This data was acquired through a rutheniummodified substrate which fluoresces under 450nm light and is quenched by oxygen. The data was calibrated and the intensities are directly related to the local oxygen concentration through the Stern-Vollmer logorithm.

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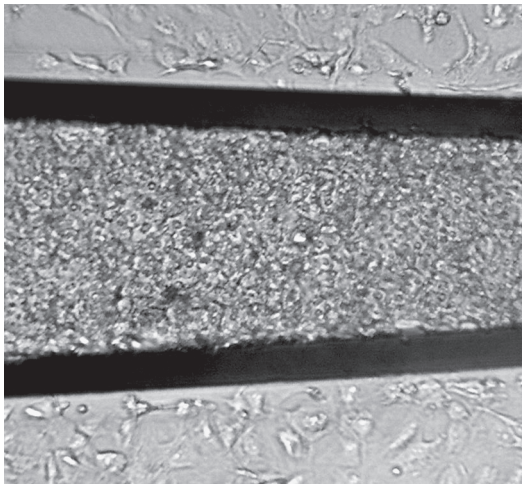
Micromechanical Control of Cell-Cell Interaction

E.E. Hui, S.N. Bhatia
Sponsorship: NIH NIDDK

Cellular behavior within tissues is driven by environmental cues that vary temporally and spatially with granularity on the order of individual cells. Local cell-cell interactions via secreted and contact-mediated signals play a critical role in these pathways. In order to study these dynamic small-scale processes, we have developed a micromechanical platform to control microscale cell organization so that cell patterns can be reconfigured dynamically. This tool has been employed to deconstruct the mechanisms by which liver-specific function is maintained in hepatocytes upon co-cultivation with stromal support cells. Specifically, we examine the relative roles of cell contact and short-range soluble signals, duration of contact, and the possibility of bi-directional signaling.

The device consists of two silicon parts that can be locked together either to allow cell-cell contact across the two parts or to separate the cells by a uniform gap of approximately 80 μm (Figs. 1 and 2). Switching between these two states is actuated simply by pushing the parts manually using tweezers; no micromanipulation machinery is necessary. Micron-scale precision is possible due to a 10:1 mechanical transmission ratio and microfabricated snap locks, both of which are monolithically incorporated into the silicon structure. The entire device is fabricated in a simple single-mask process using through-wafer deep reactive ion etching. To provide a surface compatible with cell culture, the surface is coated with a layer of polystyrene and plasma-treated, providing a standard tissue-culture surface.



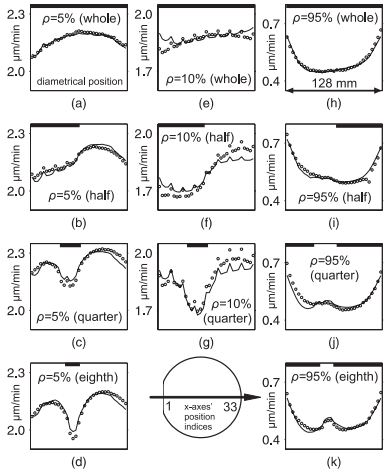
▲ Figure 1: Hepatocytes separated from stromal cells by 80-micron gaps, which prevent contact between the two cell types.

▲ Figure 2: Hepatocytes and stromal cells cultured with no separation. The system can be switched back and forth between the states shown in Figures 1 and 2.

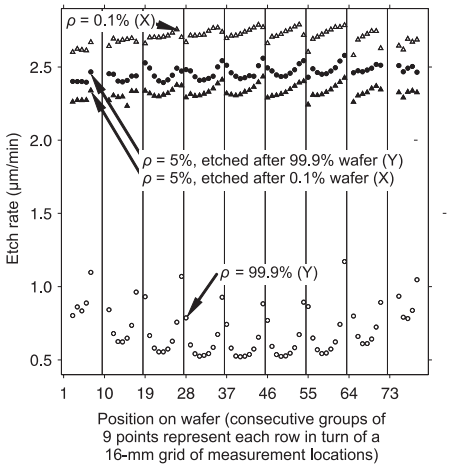
Characterization and Modeling of Non-uniformities in DRIE

H.K. Taylor, H. Sun, A. Farahanchi, D.S. Boning
Sponsorship: Singapore-MIT Alliance

Our previous work on spatial non-uniformities in deep-reactive ion etch (DRIE) has provided a method by which an etching tool and associated "recipes" of operating parameters may be pre-characterized [1]. That work allowed the wafer-average pattern opening density (or "loading") to be related to wafer-scale etch rate variations. Such variations have been attributed to loading-dependent interactions of the flux densities of S_xF_y ions and F neutrals and to shifts in the gross flows of fluorine across the wafer [2]. Unlike some other approaches [3–5], our method captures asymmetries in the fluxes within the chamber. Our approach is now supplemented by an understanding of how uniformity depends on the localization of etched patterns within the wafer (Figure 1). A semi-physical model represents the diffusion of monatomic fluorine etchant parallel to the wafer's surface, giving a two-dimensional filter which translates a discretized map of pattern density into a prediction of how etch rate will vary within and between dies [6]. This die-level model is readily combined with the existing wafer-level model. To tune this combined model for a new recipe, a set of about five test wafers is etched, and fitting algorithms are run with etched-depth data. Collaborative experiments with Surface Technology Systems Ltd have demonstrated our approach in use with a prototype etch tool. Further experiments have compared the characteristics of different manufacturers' tools. We have also quantified a memory effect whereby the average pattern density of one etched wafer can affect the average rate and non-uniformity with which a subsequent wafer etches (Figure 2). In the future we aim to incorporate well-known feature size or aspect ratio effects into our model [7]. We envisage our approach being integrated into computer-aided design systems for MEMS and believe that it will be of particular use when one is keen to preserve a fast-average etch rate and is thus loath to win uniformity by reducing the chamber pressure.



▲ Figure 1: Diametrical variation of etch rate for 11 wafers with differing average pattern density. Heavy bars indicate the portion of the diameter into which etched silicon was concentrated.



▲ Figure 2: The influence of the average pattern density (ρ) of one etched wafer upon the rate and uniformity with which the subsequent wafer etches. It is observed that a wafer's etch rate is slightly accelerated when the preceding wafer has a very high etched density; moreover, the shape of the nonuniformity is also echoed.

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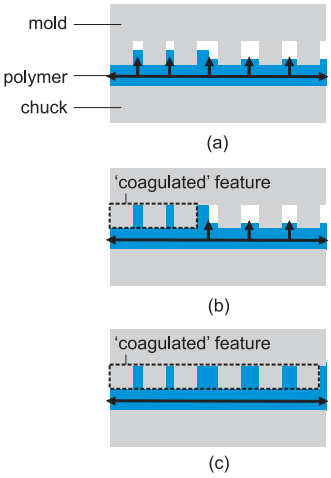
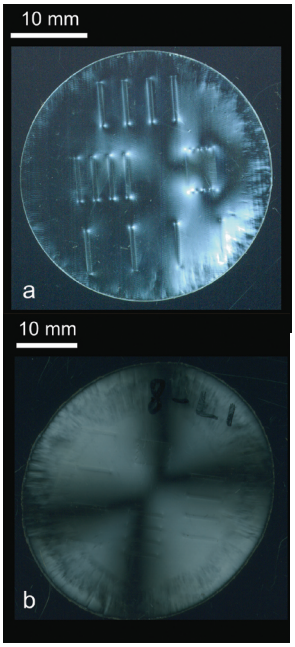
Understanding Uniformity and Manufacturability in MEMS Embossing

H.K. Taylor, D.S. Boning
Sponsorship: Singapore-MIT Alliance

The hot embossing of thermoplastic materials, such as polymethylmethacrylate (PMMA) or cyclo- olefin copolymer (COC), is a promising way to manufacture microfluidic channels and networks [1]. Hot embossing potentially offers lower per-area cost than the micromachining of quartz or silicon and easier scaling-up of production than soft lithography using polydimethylsiloxane [2]. In hot embossing, a microfabricated mold (typically of silicon or nickel) is pressed into a flat sample of polymeric material that has been softened by heating it above its glass-transition temperature. We are particularly interested in how the spatial distribution of mold features—their diameters, shapes, and areal densities—may influence the quality of embossed patterns. We are developing a simulation approach whose building-block is a simple model in which, for given embossing conditions, a feature-sized disk of viscous polymer is compressed at a rate inversely proportional to the square of the radius of the disk [3] (Figure 1). Such a model implies that the mold will sink into the substrate at a spatially uniform rate when the product of the areal density of mold features and the square of their average radius remains constant across the mold. We aim to construct a reliable model that is computationally efficient and that can predict the combination of embossing pressure and duration required by any mold design. We are investigating the measurement of birefringence of embossed samples [4] as a way of monitoring the embossing process (Figure 2). We are also pursuing a technique for the bonding of polymer surfaces that promises minimal deformation of pre-embossed features: the polymer surfaces are exposed to an oxygen plasma for ~1 minute and then pressed together [5].



◀ Figure 1: Proposed model for the spatially non-uniform filling of embossing mold features with heated thermoplastic material (blue). Arrows indicate the displacement of material. Regions of the mold with higher areal densities of protruding features, e.g., on the left in this figure, are expected to be filled more quickly (a), and to "coagulate" into effectively larger features (b). Eventually all features would be filled and the polymeric substrate may continue to be compressed as one large disk (c).



◀ Figure 2: Light transmitted by each of two embossed PMMA samples sandwiched between perpendicular polarizers. The two samples were embossed under ~1 MPa for equal lengths of time. At 110 °C (a), material within about 1 mm of the corners of embossed, 30 μm-deep rectangular channels exhibits substantially higher birefringence than the rest of the sample, implying concentrations of residual stress there. At 150 °C (b), feature-scale birefringence becomes less important than sample-scale birefringence. Samples fabricated by Wang Qi.

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A MEMS Drug Delivery Device for the Prevention of Hemorrhagic Shock

H.L. Ho Duc, M.J. Cima
Sponsorship: ARO (Institute for Soldier Nanotechnology)

Hemorrhagic shock is the number one cause of preventable death on today's battlefield [1]. It is a hypotensive state of deficient organ perfusion caused by blood loss from wounds of the extremities or internal injuries. Hemorrhagic shock is normally treated by hemorrhage control, fluid replacement, and the injection of vasoconstrictors. Battlefield conditions, however, can prevent the timely administration of these measures. Hemostatic dressings developed for battlefield application are useful in controlling open wound hemorrhage but cannot stop internal bleeding or avert shock if too much blood has been lost [1]. Arginine vasopressin is a vasoconstrictor that causes peripheral and abdominal arteries to constrict, shunting blood to the vital organs in case of hemorrhage [2]. It improved survival by restoring blood pressure in pre-clinical experiments and clinical case studies of hemorrhagic shock when treatment was not immediately available [3-7]. This property makes it a perfect candidate for battlefield injection to keep wounded soldiers alive until they can be properly treated. Self-injection may not always be possible, however, due to the nature of these traumas.

We are currently developing an implantable drug delivery microelectromechanical system (MEMS) to deliver vasopressin to wounded soldiers on the battlefield. This device consists of a silicon substrate in which pyramidal wells are etched using common MEMS processing techniques. The wells are capped by metallic membranes and the chip is hermetically bonded to a Pyrex macroreservoir (Figure 1). The macroreservoir can be injected with 25 μL of a vasopressin solution to be released on demand. Applying an electric pulse through a metallic membrane melts it by resistive heating, exposing the macroreservoir to the environment. We also observed the formation of multiple thermal bubbles inside the macroreservoir, which enabled rapid delivery of the solution. We are redesigning the device to better control this mechanism. Future challenges include insuring long-term hermeticity and wireless activation of the device.

◀ Figure 1: Picture of the MEMS device showing the Pyrex macroreservoir (left) bonded to the silicon chip (right). The metallic layer on the silicon chip controls the opening of micro-wells allowing vasopressin out of the macroreservoir.

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Application of Input Shaping® and HyperBit™ Control to Improve the Dynamic Performance of a Six-axis MEMS Nano-positioner

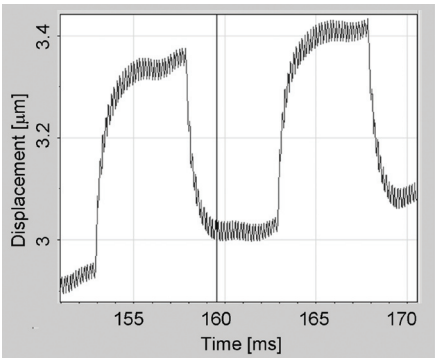
S. Chen, M.L. Culpepper, S. Jordan, J. Danieli, J. Wenger
Sponsorship: NSF

We have recently demonstrated how Input Shaping® and HyperBit™ control may be used to obtain fine-resolution motion and minimize vibration errors in all six axes of a six-axis, MEMS nano-positioner [1]. The dynamic problems in MEMS positioners, e.g., ringing/overshoot, that are conventionally addressed by damping must be resolved using control techniques since it is difficult to incorporate damping into micro-scale devices. Secondly, a positioner's range to resolution ratios has to be 1 million or larger and also its "on-chip" digital-to-analog converters would need to be minimized on the expensive silicon real estate. These issues will be resolved by the applying the Input Shaping and HyperBit control.

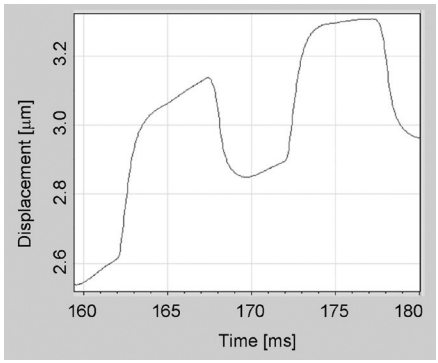
We first study the dynamic characterization of the nanopositioner, the microHexFlex [2], including the natural frequencies and their corresponding mode shapes. We then demonstrate the effect of Input Shaping and HyperBit on the nano-positioner's resolution and settling time. Using these techniques, it is possible to obtain ms settling times with sub-nanometer resolution. The practical implications of this work are that future small-scale precision devices will be able to use these techniques to provide low-cost, multi-axis positioning at high-speeds speed and with fine resolution.

The micro-HexFlex nanopositioner possess a 2.5-mm footprint and consists of two layers of single crystalline silicon with one layer of silicon dioxide in between. The stage of the micro-HexFlex is supported by axi-symmetric micro-scale flexures. Thermomechanical actuators are used to drive the Micro-HexFlex. In our tests, the thermomechanical actuators were driven via a voltage that was preconditioned using an Input-shaping controller. The controller [3] is an implementation of a feed-forward technique that acts to remove ringing and overshoot by modifying the input signal to the actuators so as to obtain the best possible performance from the positioner.

We also add HyperBit DAC technology, a recently developed technique [4] for extending the resolution of digital-to-analog converters (DACs), for instance using a 4-bit DAC to obtain 12-bit functionality. Since DAC update rate capabilities are significantly faster than the bandwidths of the devices being driven, this technique allows the idle time-domain capacity of "low-bit" DACs to emulate that of "high-bit" DACs. The improvement in resolution is therefore obtained with simpler DAC equipment/circuitry that is more easily fabricated and integrated with micro- and meso-scale devices. Experimental results indicate reduction in dynamic errors by two orders of magnitude when the positioner was given 100-Hz square wave commands.



▲ Figure 1: Displacement response of microHexFlex to a 100-Hz square-wave without Input Shaping.



▲ Figure 2: Displacement response of microHexFlex to a 100-Hz square-wave with Input Shaping.

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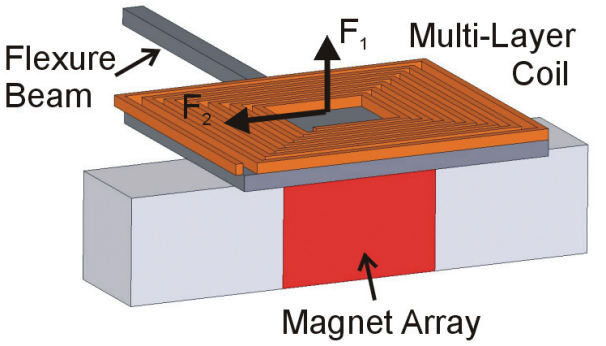
Multi-Axis Electromagnetic Moving-Coil Microactuator

D.S. Golda, M.L. Culpepper
Sponsorship: NSF

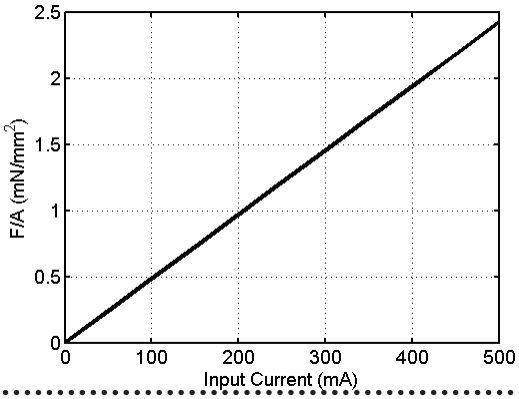
Electromagnetic (EM) micro-actuators are becoming increasingly important in micro-systems requiring moderate forces operating over a large range of motion. The applications that benefit from the performance advantages of EM micro-actuators include micro-scanning systems, micro-fluidic pumps, and positioning systems. Advantages of electromagnetic actuation over other classes of micro-actuators include low-voltage operation, moderate power density, large operating distances, linear response, multi-axis capability, and high bandwidth [1]. This work leverages the advantages of EM interactions to design a moving-coil micro-actuator that enables two-axes actuation with moderate forces (10+ mN) over large operating distances (10+ micrometers) at moderate mechanical frequencies (1+ kHz) using assembled permanent magnet field sources.

The two-axes electromagnetic actuator consists of moving coils suspended on compliant silicon flexure springs above an array of 3 rectangular permanent magnets, as shown in Figure 1. The phase of the stacked coils results in Lorentz forces that are independently controllable in-the-plane and out-of-the-plane. The coil-spring fabrication scheme includes electroplating of copper coils, followed by a deep reactive-ion etch (DRIE) to pattern and release the compliant springs. Millimeter-sized permanent magnets are then aligned to the spring layer using an alignment chip. Successfully fabricated micro-coil structures have been shown to sustain current densities over 1000 Amps per square millimeter.

A quasi-analytic electromagnetic force model for the device has been developed and experimentally validated against a centimeter-size bench-level prototype actuator. Figure 2 shows the predicted lateral-actuator force per coil-footprint versus current input for a typical actuator with 900-μm^2 coil cross section. The actuator will be implemented in a high-speed meso-scale nano-positioner with applications in nano-fabrication and scanning-probe microscopy. When equipped with this micro-actuator, the nano-positioner is expected to be able to position millimeter-sized samples in six axes of motion (x, y, z, tip, tilt, yaw) with repeatability better than 10 nanometers at frequencies greater than 1 kHz.



▲ Figure 1: Schematic representation of the electromagnetic moving-coil microactuator.



▲ Figure 2: Predicted force per coil area versus input current for a typical EM moving-coil microactuator.

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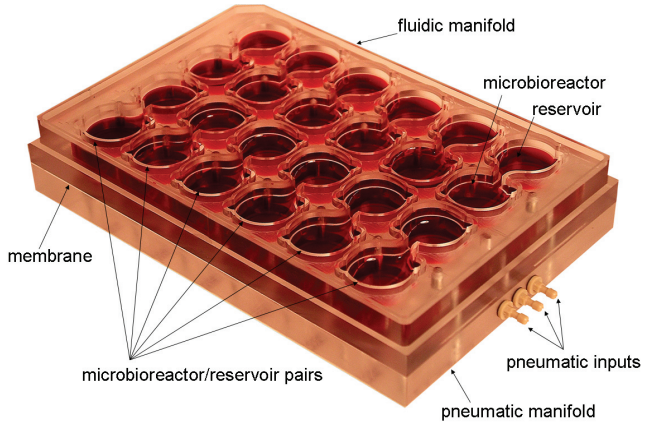
Multiwell Cell Culture Plate Format with Integrated Microfluidic Perfusion System

K. Domansky, S.W. Inman, J. Serdy, L.G. Griffith
Sponsorship: DuPont-MIT Alliance, Pfizer, Biotechnology Process Engineering Center

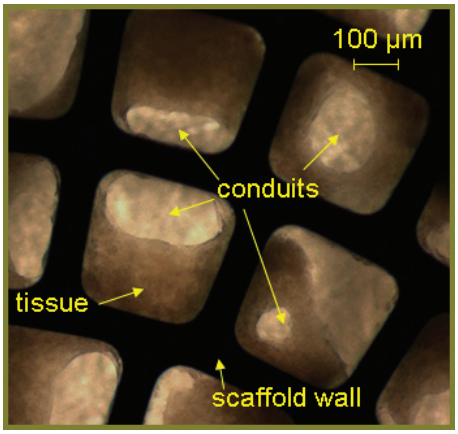
Recent reports indicate that it takes nearly $800 million dollars and 10-15 years of development to bring a drug to market. Nearly 90% of the lead candidates identified by current *in vitro* screens fail to become marketable drugs. One of the reasons for the high failure rate of drug candidates is the lack of adequate models. To address the problem, we have developed a new cell culture analog amenable to routine use in drug development. It is based on the standard multiwell cell culture plate format but it provides perfused three-dimensional cell culture capability.

The multiwell plate microbioreactor array [1, 2] consists of a fluidic and a pneumatic manifold with a diaphragm sandwiched in between them. The fluidic manifold contains an array of microbioreactor and reservoir pairs (Figure 1). Each microbioreactor/reservoir pair is fluidically isolated from all other microbioreactors on the plate. A key component of a microbioreactor is a scaffold for tissue morphogenesis (Figure 2). The scaffold is a thin wafer containing an array of channels in which cells self-assemble into 3D pieces of tissue. It is backed by a filter and a support scaffold. Tissue in the scaffold is perfused by cell culture medium. The medium is re-circulated between the reactor and reservoir by a diaphragm pump. The diaphragms of all pumps and rectifying valves are actuated in parallel via three pneumatic lines distributed by the pneumatic manifold. Fluidic capacitors control flow pulsatility.

The system provides a means to conduct high throughput assays for target validation and predictive toxicology in the drug discovery and development process. It can be also used for evaluation of long-term exposure to drugs or environmental agents and as a model to study viral hepatitis, cancer metastasis, and other diseases and pathological conditions.



▲ Figure 1: Photograph of a 12-microbioreactor array occupying 24 wells. Cell culture medium is re-circulated between the reactor and reservoir wells. All reactor/reservoir pairs are fluidically isolated from each other.



▲ Figure 2: Primary rat hepatocytes seeded in a silicon scaffold (day 7 after isolation). The channels were microfabricated by deep reactive ion etching. The size of each channel is 300 x 300 x 230 µm. Each channel can accommodate 500-1000 cells.

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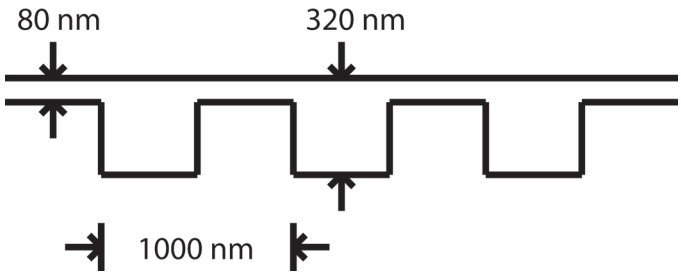
Characterization of Nanofilter Arrays for Biomolecule Separation

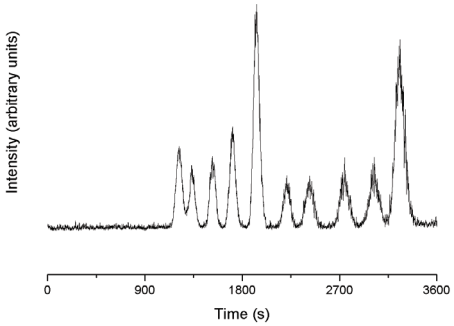
H. Bow, J. Fu, J. Han
Sponsorship: DuPont-MIT Alliance, NIH, Singapore-MIT Alliance

In the past decade, microfabricated devices have been developed that can separate, detect, and analyze various biomolecules [1]. In contrast to the sieving gels that are historically used in these studies, microfabricated devices are precisely designed and constructed. The deterministic structure of these devices facilitates experiment design and testing of theory. Periodic nanofilter arrays have been shown to separate DNA from 100 bp to 10 kbp [2]. These nanofilters consist of a regular sequence of free and constricted regions, with 50-100 nm being the characteristic dimension of the constricted region. In this context, the DNA is smaller than the constriction size, suggesting applicability of the Ogston sieving mechanism. Movement is characterized by the partitioning between the free and constricted regions due to steric constraints [3-4]. DNA has a persistence length of 50 nm (150 bp) and can be approximated as semi-rigid rods in this size range, facilitating theoretical analysis.

We investigated the effects on separation efficiency and resolution of changing various device and experiment parameters. These parameters include the strength of the electric field; depth of the deep region; depth of the thin and deep regions, while maintaining their ratio; silicon substrate bias; buffer strength; and period of the nanofilter array.



▲ Figure 1: Cross-section of basic device. The typical separation region length is 1 cm.



▲ Figure 2: Fluorescence intensity as a function of time. Separation of 100 bp to 1000 bp (100 bp interval) is achieved in less than 1 hr at 20 v/cm in an 80-nm thin-gap device.

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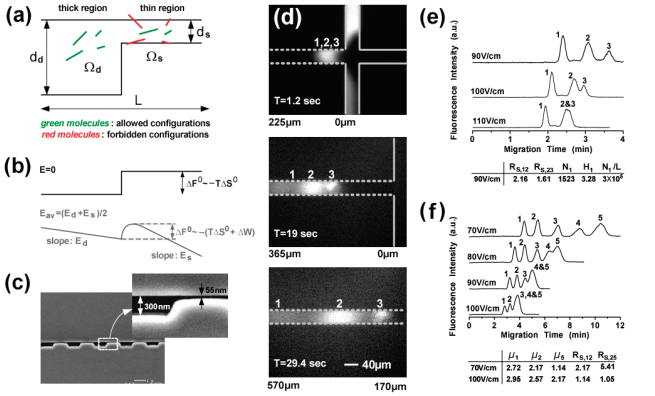
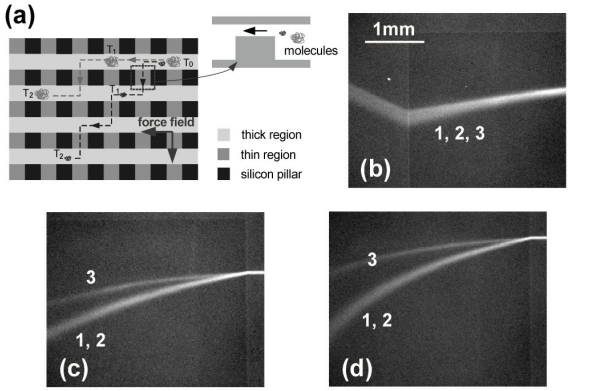
Patterned Periodic Potential-energy Landscape for Fast Continuous-flow Biomolecule Separation

J. Fu, J. Han
Sponsorship: NSF, Singapore-MIT Alliance, NIH NIBIB

Manipulation of charged biomolecules through confining environments has broad applications in life science. Recent progress in fabricating well-defined spatial constraints allows direct observation of novel molecular dynamic behavior in molecular-sized confining structures. Further, it shows exceptional promise for providing regular sieving media with superior separation performance. Here we demonstrate a continuous-flow, biomolecule-separation device that makes use of a patterned anisotropic sieving matrix consisting of a two-dimensional periodic array of nanofilters. The electrophoretic drift of biomolecules in the sieving medium involves a differential bidirectional motion through two-dimensional, periodically modulated, free-energy landscapes that results in a vectorial apparent electrophoretic mobility that directs molecules of different sizes to follow radically different paths. This method provides a novel basis for dispersing small fluid-borne biomolecules into distinct fractions. A fluorescently labeled dsDNA mixture (50-766 bp) used to characterize the device was separated in 1 minute with a resolution of about 10%. The patterned anisotropic sieve was also used for size-fractionation of SDS-protein complexes of size ranging from 11 to 200 kDa in 1 minute. By virtue of its gel-free and continuous-flow operation, this device suggests itself as a key component of an integrated microsystem that prepares and analyzes biomolecule samples.



▲ Figure 1: (a) Partitioning of rigid, rod-like molecules in a slit-like nanofilter. (b) Free energy landscape of a nanofilter. (c) An SEM images of a periodic array of nanofilters with alternating thin and thick regions. (d-f) Separation of SDS-protein complexes (d & e) and dsDNA molecules (f) in a one-dimensional nanofilter array chip (d_s: 55 nm, d_d: 300 nm, L: 1 μm). Band assignment for SDS-protein complexes: (1) cholera toxin subunit B (MW: 11.4 kDa); (2) lectin phytohemaglutinin-L (MW: 120 kDa); (3) low-density human lipoprotein (MW: 179 kDa), for DNA: (1) 50 bp; (2) 150 bp; (3) 300 bp; (4) 500 bp; (5) 766 bp.



▲ Figure 2: (a) Bidirectional transport of biomolecules in the 2-D nanofilter arrays. (b) Fluorescence images of pulsefield separation of SDS complexes inside the 2-D nanofilter arrays. Different values of vertical and horizontal fields can be applied with different durations. Band assignments for SDS-protein are the same as in Figure 1.

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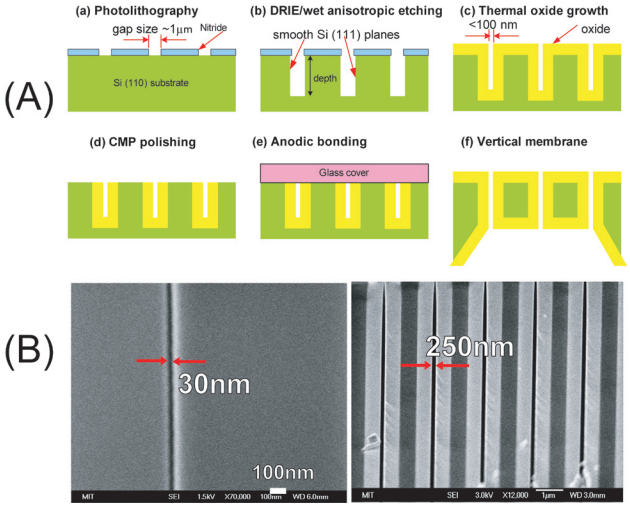
Fabrication of Massively-parallel Vertical Nanofluidic Membranes for High-throughput Applications

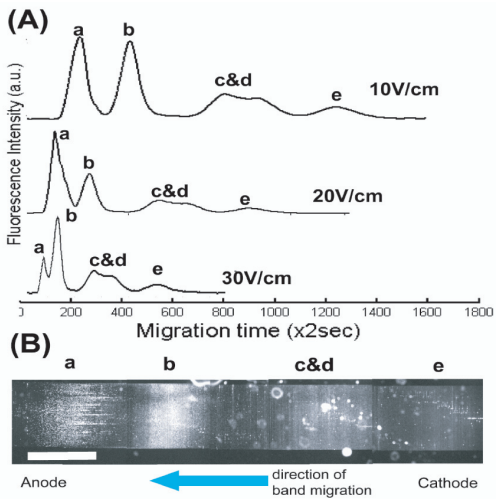
P. Mao, J. Han
Sponsorship: KIST IMC, NSF

Nanofluidics has gained tremendous successes in the last few years because they provide unique capability in biomolecular manipulation and control. For nanofluidic applications, one critical issue is the availability of reliable, reproducible fabrication strategies for nanometer-sized structures. A simple technique, without nanolithography or special tools, has been developed to generate planar nanochannels with precise control of depths to the nanometer scale for many applications including separation [1] and preconcentration [2]. However, one big issue with these planar nanofluidic channels is the limited fluidic conductance that results in low throughput.

Here we describe a novel fabrication approach to generate massively-parallel vertical nanochannels with the well-controlled gap size down to 100 nm [3]. We use anisotropic wet etching (KOH) to make deep, vertical trenches on Si (110) substrate (Figure 1A). Alternatively, conventional deep reactive ion etching (DRIE) can be performed to produce very deep trenches, and then the sidewalls can be smoothed by a short KOH etching. Then the width of the trench channel is further decreased to a desired thickness even below 50 nm (Figure 1B), by growing thermal oxide. Also, backside etching of the Si wafer can yield thin membranes over a wide area (~ 6-inch wafer) with well-defined membrane thickness, if needed. Our method requires neither expensive nanolithography expertise nor other tools and allows the integration of a large number of narrow, vertical nanofluidic filters with fluidic conductance 10~100 times higher than planar nanochannels. Furthermore, we have demonstrated efficient, high-throughput separation of large DNA molecules in our vertical nanofilter array device based on the entropic trapping mechanism (Figure 2). We believe that these membrane devices could be a key to the high-throughput nanofluidic sample-preparation microsystems.



▲ Figure 1: (A) Schematic diagram of fabricating massively-parallel vertical nanofluidic membranes. (B) Cross-sectional SEM micrograph of vertical nanochannels with lateral gap sizes (widths) of 250 nm (left) and 30 nm (right).



▲ Figure 2: (A) Separation of the mixture of λ-DNA and λ-DNA digested by Hind III in a lateral nanofilter array chip under different electrical fields. Peak assignment: (a) 48.5kbp,(b) 23kbp,(c) 9.4kbp,(d) 6.5kbp,and (e) 4.4kbp. (B) Direct observation of DNA bands separated at 10 V/cm. The scale bar is 1 mm.

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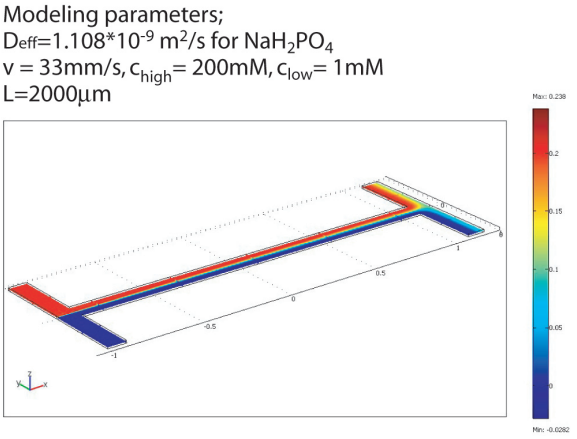
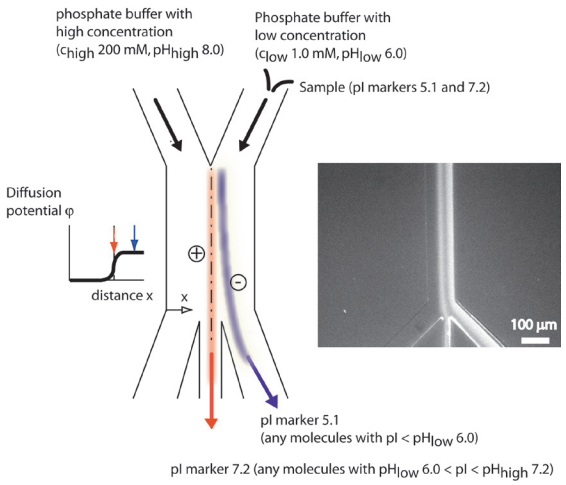
Continuous-flow pI-based Sorting of Proteins and Peptides in a Microfluidic Chip Using Diffusion Potential

Y.-A. Song, J. Han
Sponsorship: NSF CAREER Award, KIST-IMC, CSBi/Merck Fellowship

In this work, we have developed a simple microfluidic chip that can sort biomolecules based on their isoelectric point (pI) values in a simple buffer system. The new method differs from previous approaches such as transverse isoelectric focusing [1] or free-flow electrophoresis [2] in that this process involves no external power supply and no special ampholyte. Instead, we utilize the diffusion potential generated by the diffusion of different buffer ionic species *in situ* at the laminar flow junction. The use of diffusion potential in microfluidics was previously demonstrated with the mass transport of dye molecules between the two streams in [3]. However, they did not explicitly demonstrate a separation of two species. In our device, we establish a laminar flow junction between two buffers with different pH and concentrations. A potential gradient is developed across the liquid junction, generating a high-enough electric field to mobilize and to collect biomolecules at the boundary when their pI values fall between the two buffer pH values. The computational modeling shows a decreasing potential gradient from 17.1 V/cm to 6.9 V/cm along the 2-mm-long microchannel (20 μm deep, 100 μm wide), as the concentration gradient becomes shallower toward the end of the channel due to mixing (Figure 1). In our initial experiment, two pI-markers (Figure 2) as well as two proteins were successfully sorted in this device, with a flow rate of 5~10 μL/min. To characterize the accuracy of this pI-based sorting process, we tested sorting behavior of the device by changing the pH value of the sample buffer in 0.1 pH step. It was shown that a peptide can be sorted into a different output stream with a ~0.1pH unit resolution. We are currently working on the development of new buffer systems as well as on the hybrid approach with a superimposed external electric field to increase the sorting efficiency and resolution. Once fully developed, it can potentially be a pI-based sample fractionation tool for proteomic analysis of complex biomolecule samples.



▲ Figure 1: A 3D steady-state concentration distribution in a 2-mm-long microfluidic channel with a concentration ratio of 200. Based on this concentration distribution, the diffusion potential as well as the potential gradient can be calculated.



▲ Figure 2: Schematic view of the pI-based sorting process and separation of two pI markers with pI values of 5.1 and 7.2 using diffusion potential at a concentration difference of 200 and at a flow rate of 10 μl/min.

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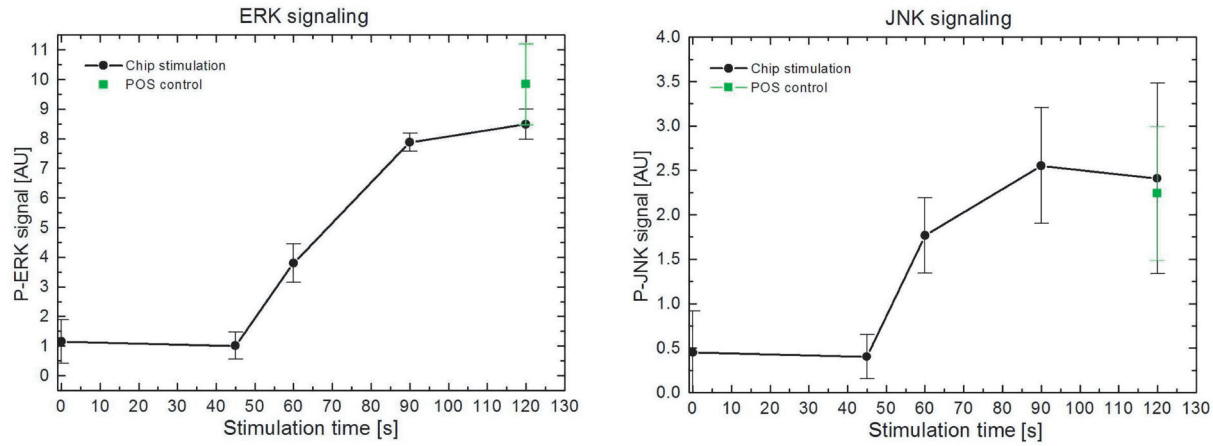
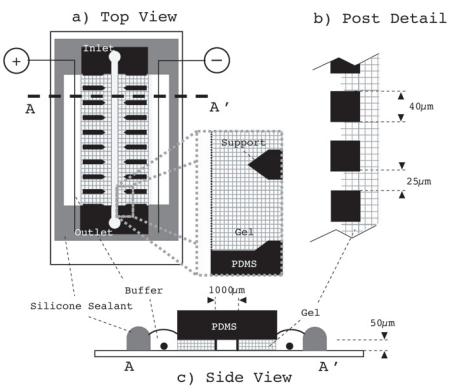
Cell Stimulation, Lysis, and Separation in Microdevices

J. Albrecht, J. El-Ali, S. Gaudet, K.F. Jensen
Sponsorship: NIH

Quantitative data on the dynamics of cell signaling induced by different stimuli require large sets of self-consistent and dynamic measures of protein activities, concentrations, and states of modification. A typical process flow in these experiments starts with the addition of stimuli (cytokines or growth factors) to cells under controlled conditions of concentration, time, and temperature, followed at various intervals by cell lysis and the preparation of extracts. Microfluidic systems offer the potential to do this in a reproducible and automated fashion. Figure 1 shows quantification of the stimulation of a T-cell line with antibodies performed in a microfluidic device with integrated cell lysis. The device is capable of resolving the very fast kinetics of the cell pathways, with protein activation levels changing 4-fold in less than 15 seconds. The quantification of the lysate is currently performed off-chip using electrophoretic separation. To extract meaningful data from cellular preparations, many current biological assays require similar labor-intensive sample purification steps to be effective. Micro-electrophoretic separators have several important advantages over their conventional counterparts including shorter separation times, enhanced heat transfer, and the potential to be integrated into other devices on-chip. However, the high voltages required for these separations prohibit metal electrodes inside the microfluidic channel. A PDMS isoelectric focusing device with polyacrylamide gel walls has been developed to perform rapid separations by using electric fields orthogonal to fluid flow (Figure 2). This device has been shown to focus low molecular weight dyes, proteins, and organelles in seconds.



▲ Figure 1: ERK and JNK signaling in Jurkat E6-1 cells stimulated with α-CD3 for different times. Stimulation and cell lysis were performed with the microfluidic device (Chip stimulation) and with conventional methods (POS control). The error bars denote one standard deviation.



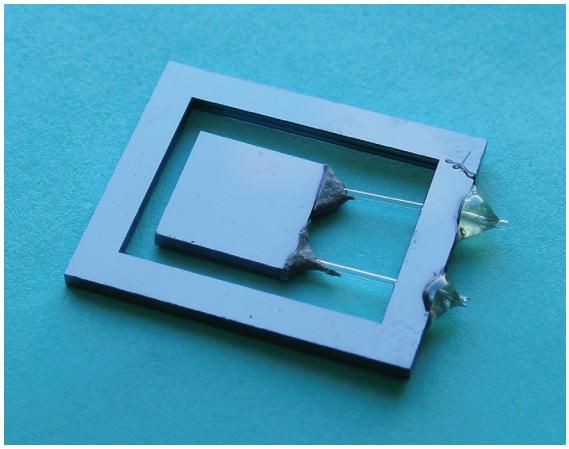
◀ Figure 2: Layout of transverse IEF device. Top view (a) shows the PDMS device with the sample channel bordered by left and right gel regions (cross-hatched areas) and anode and cathode, respectively. It is separated from the gel sections by 40 µm × 40 µm, 50 µm tall posts (b). The device presented has a single inlet and single outlet. Side view (c) shows the device in cross-section (not to scale).

Thermal Management in Devices for Portable Hydrogen Generation

B. Blackwell, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

The development of portable-power systems employing hydrogen-driven solid oxide fuel cells continues to garner significant interest among applied science researchers. The technology can be applied in fields ranging from the automobile to personal electronics industries. This work focuses on developing microreaction technology that minimizes thermal losses during the conversion of fuels – such as light-end hydrocarbons, their alcohols, and ammonia – to hydrogen. Critical issues in realizing high-efficiency devices capable of operating at high temperatures have been addressed, specifically, thermal management, the integration of materials with different thermophysical properties, and the development of improved packaging and fabrication techniques.

A new fabrication scheme for a thermally insulated, high temperature, suspended-tube microreactor has been developed. The new design improves upon a monolithic design proposed by Arana *et al.*[1]. In the new modular design (Figure 1), a high-temperature reaction zone is connected to a low-temperature (~50°C) package via the brazing of pre-fabricated, thin-walled glass tubes. The design also replaces traditional deep reactive ion etching (DRIE) with wet potassium hydroxide (KOH) etching, an economical and time-saving alternative. A brazing formulation that effectively accommodates the difference in thermal expansion between the silicon reactor and the glass tubes has been developed.



▲ Figure 1: Suspended-tube microreactor showing 2 pre-fabricated SiO_2 tubes, a microfabricated Si reaction chip, and a microfabricated Si frame. The modular design is assembled via a glass braze.

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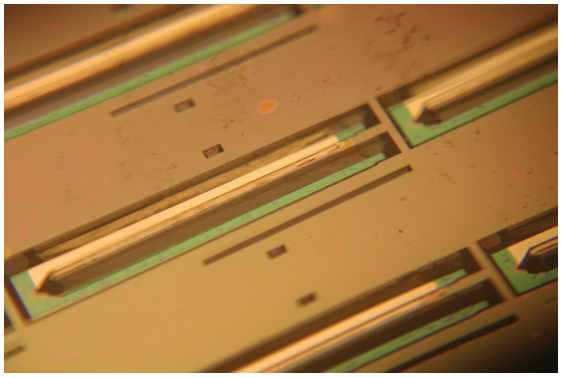
Autothermal Catalytic Micromembrane Devices for Portable High-Purity Hydrogen Generation

K. Deshpande, M.A. Schmidt, K.F. Jensen
Sponsorship: ARO MURI

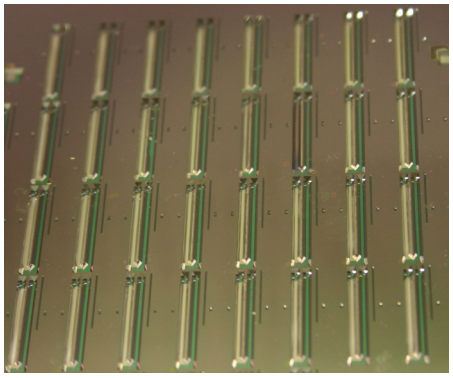
The high efficiency and energy density of miniaturized fuel cells provide an attractive alternative to batteries in the portable power generation market for consumer and military electronic devices [1-3]. The best fuel cell efficiency is typically achieved with hydrogen, but safety and reliability issues remain with current storage options. Consequently, there is continued interest in reforming liquid fuels to hydrogen. The process typically involves high temperature reforming of fuel to hydrogen combined with a low temperature PEM fuel cell, which implies significant thermal loss. Owing to its high hydrogen content (66%) and ease of storage and handling, methanol is an attractive fuel. However, partial oxidation of methanol also generates some CO, which may poison the fuel cell catalyst.

Previously [4] we successfully demonstrated hydrogen purification using thin (~200 nm) Pd-Ag membranes using electrical heating. Further, integration of these devices with $LaNiCoO_3$ catalyst allowed methanol reforming at 475°C with 47% fuel conversion [5]. Since microreactors possess high surface area to volume ratio, minimizing heat loss is important. Hydrogen flux across the Pd membranes is an equilibrium controlled process. Thus to achieve thermal management, the unextracted hydrogen, generated CO, and unreacted methanol can be completely oxidized in a separate reactor.

In the current work, we explore the realization of autothermal hydrogen generation by fabricating silicon-based reactors using bulk micromachining techniques. The hydrogen generation unit comprises a 200-nm palladium-silver membrane coated with a reformer catalyst while the combustor is loaded with platinum catalyst. High thermal conductivity of silicon ensures autothermal operation. Upon thermal isolation using vacuum packaging [6], we characterize the performance of this integrated, autothermal hydrogen generation system in terms of energy efficiency and hydrogen production.



▲ Figure 1: Fabricated reformer-burner unit with palladium membranes.



▲ Figure 2: Plan of silicon wafer with multiple reformer-burner units.

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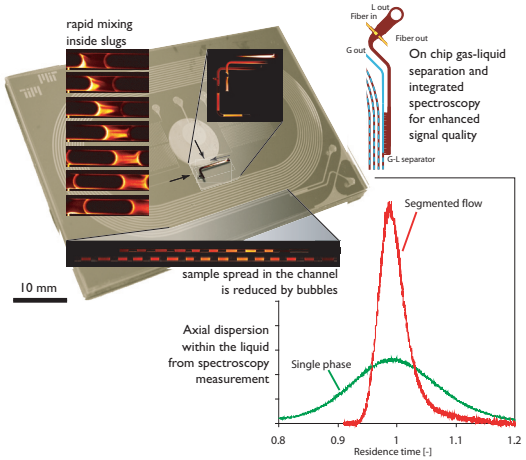
Multiphase Transport Phenomena in Microfluidic Systems

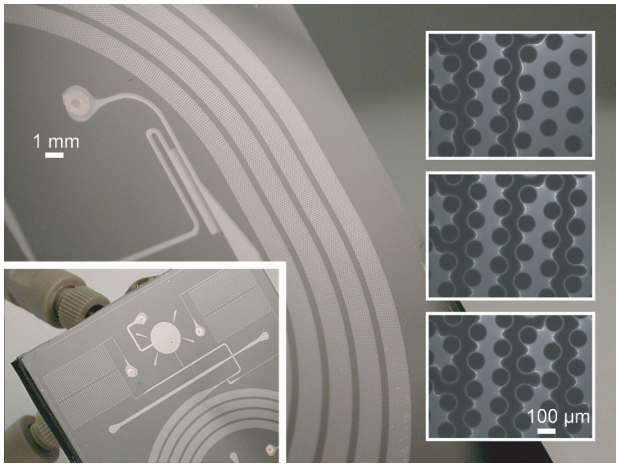
A. Guenther, M.T. Kreutzer, K.F. Jensen
Sponsorship: Microchemical Systems Technology Center, ISN, Dutch Foundation for Applied Sciences (MTK)

Fluid interfaces provide unique opportunities for microfluidic and nanofluidic systems. Applications range from microscale heat exchangers and miniature fuel cells to microreactors for materials synthesis. Multiphase flow in such devices can be challenging, as the interfacial forces naturally favor axisymmetric geometries that are difficult to microfabricate. The advantages of surface tension dominated microfluidics include a much richer dynamic flow behavior and enhancement of heat and mass transfer by creating secondary flows. These advantages offer many uses beyond enabling gas-liquid and fluid-solid reactions [1].

In particular, we are interested in segmented flow of gas and liquid in hydrophilic channels. Figure 1 shows several key features of this flow for reaction purposes. The presence of bubbles reduces the amount of dispersion of liquid flowing through the channels, ensuring that reactants and products spend a uniform amount of time in the system. For nanoparticle synthesis in microfluidic networks, a uniform residence time distribution translates into narrowly distributed particle sizes [2-3]. Liquid segments are efficiently mixed by circulation motion and gas bubbles are separated from microchannel walls by only a thin film (thickness < 1 μm). Thin films reduce mass transfer resistance to components immobilized on the walls, such as catalysts [4] or analytical reagents and antibodies. We are also interested in the dynamics of multiphase flow through microchannels that are populated with a forest of micropillars (diameters: 50 μm – 100 μm). The observed flow patterns (Figure 2) connect to fundamental studies of flow in porous media and to catalysis. Gas-liquid and liquid-liquid flow patterns and their dynamics are determined in pulse-laser fluorescent micrographs and with microscale particle image velocimetry (PIV) measurements. Characteristics of such three-phase systems, such as persistent static fractions, axial dispersion and mixing, are compared with multiphase flow in macroscopic unstructured beds and porous media.



▲ Figure 1: Measurement of axial dispersion in single-phase (green curve) and segmented flow (red curve) through a 1.5 m long microchannel (300 μm wide, 300 μm deep) that is soft-lithographically patterned. To reduce background fluorescence in the integrated spectroscopy measurement, carbon black is dispersed in the PDMS, prior to molding.



▲ Figure 2: Microchannel (width 1 mm, depth 300 μm) populated with 100 μm wide micropillars. The left inset shows the integrated gas-liquid feeding system. On the right side, fluorescent micrographs of instantaneous gas (dark) and liquid (bright) flow patterns between pillars are shown.

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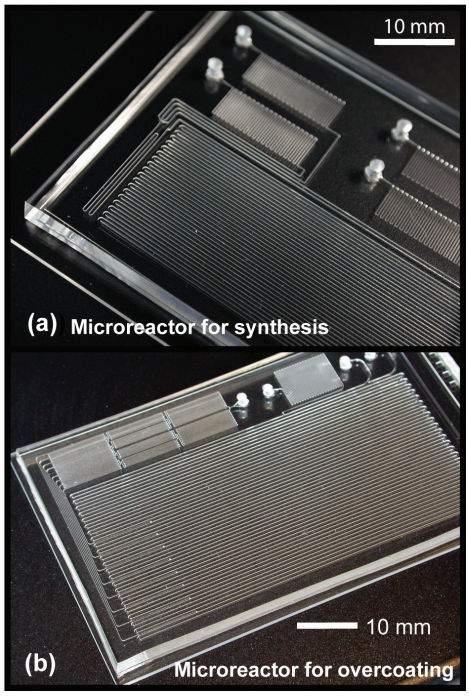
Microfluidic Synthesis and Surface Engineering of Colloidal Nanoparticles

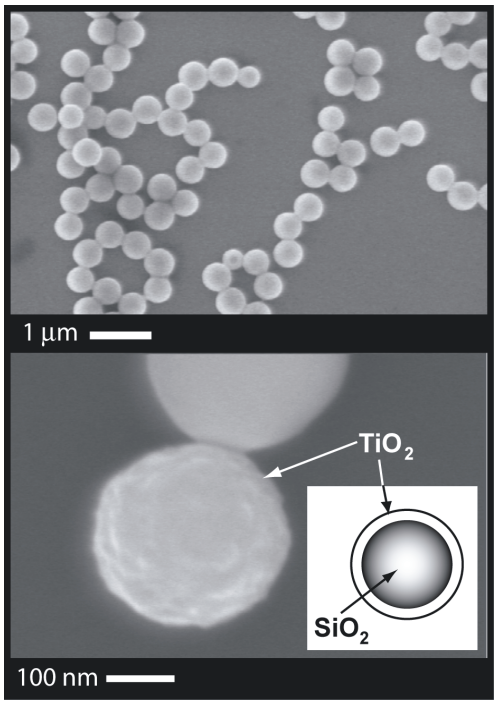
S.A. Khan, K.F. Jensen
Sponsorship: Microchemical Systems Technology Center

Metal oxide colloidal particles such as silica (SiO_2) and titania (TiO_2) have many diverse applications ranging from catalysis, pigments and photonic band-gap materials to health care products. There has also been considerable research interest over the last decade in fabricating core-shell materials with tailored optical and surface properties. Core-shell particles such as titania-coated silica often exhibit improved physical and chemical properties over their single-component counterparts and hence are potentially useful over a broader range of applications. Newer methods of engineering such materials with controlled precision are required to overcome the difficulties with conventional production techniques, which are limited to multi-step batch processes. We have developed microfluidic routes for synthesis and surface-coating of colloidal silica and titania particles.

The chief advantages of a microfluidic platform are precise control over reactant addition and mixing and continuous operation. Microfluidic chemical reactors for the synthesis and overcoating of colloidal particles are shown in Figure 1a and Figure 1b, respectively [1-2]. Figure 2a is an SEM micrograph of silica particles synthesized in a microreactor (Figure 1a) operated in segmented gas-liquid flow mode. Figure 2b shows a silica nanoparticle coated with a thick shell of titania. We have also fabricated integrated devices combining synthesis and overcoating to enable continuous multi-step synthesis of core-shell particles.



▲ Figure 1: Microfluidic reactor for (a) synthesis of colloidal silica, fabricated in PDMS, and (b) overcoating thick titania shells on silica particles.



▲ Figure 2: (a) Silica synthesized in microreactor and (b) titania-coated silica.

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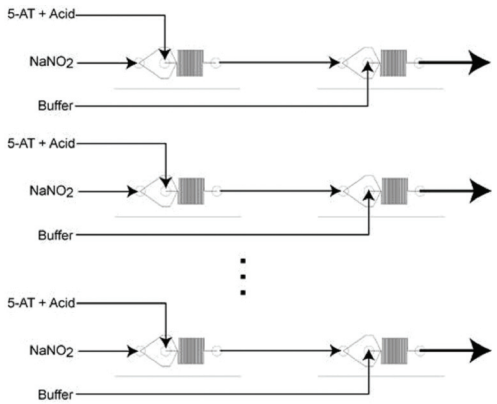
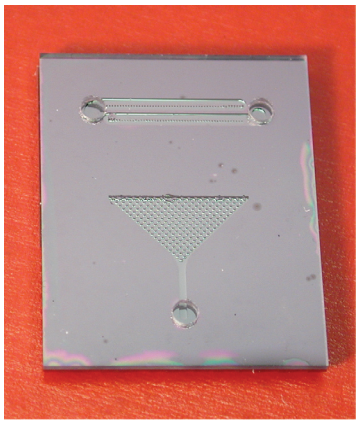
Microreactor Enabled Multistep Chemical Synthesis

E.R. Murphy, H. Sahoo, J. Kralj, N. Zaborenko, K.F. Jensen
Sponsorship: Pacific Scientific

As a demonstration of how microsystems can enable quantitative study and improved production of chemistries that have been too hazardous to pursue via traditional means, the kinetics of direct sodium nitrotetrazolate (NaNT) synthesis were characterized and a microsystem for its commercial production has been constructed (Figure 1). A PDMS modular microreactor system capable of both multi-step synthesis and rapid scale-out was constructed. This system minimized the necessary volume of the unstable diazonium intermediate, enabling the study of NaNT, an energetic material used in the construction of fire suppression systems that was too dangerous to test with traditional techniques. In the direct synthesis of NaNT, 5-aminotetrazole (5-AT) reacts with nitrous acid to produce the diazonium intermediate that, in a second reaction, undergoes a Sandmeyer type reaction that displaces the diazonium group by the nitrite ion. The rapid mixing and safety advantages of microsystems were incorporated into a flexible architecture, presenting an improved ability to safely probe the conditions of the reaction. The modular design of this system also enabled the same set of modules to be rearranged as parallel reactor chains for small-scale production. A second generation microsystem was constructed from silicon micromixer modules (Figure 2); this micro-system is not only more robust than the PDMS design but also capable of accommodating higher flow rates (>2 mL/min) and higher temperatures. This system allows higher throughput and longer operational lifetimes and is currently being optimized for use as a full-scale production platform.



▲ Figure 1: Modular microsystem serial and parallel micromixer modules.



▲ Figure 2: Silicon micromixer module (top view).

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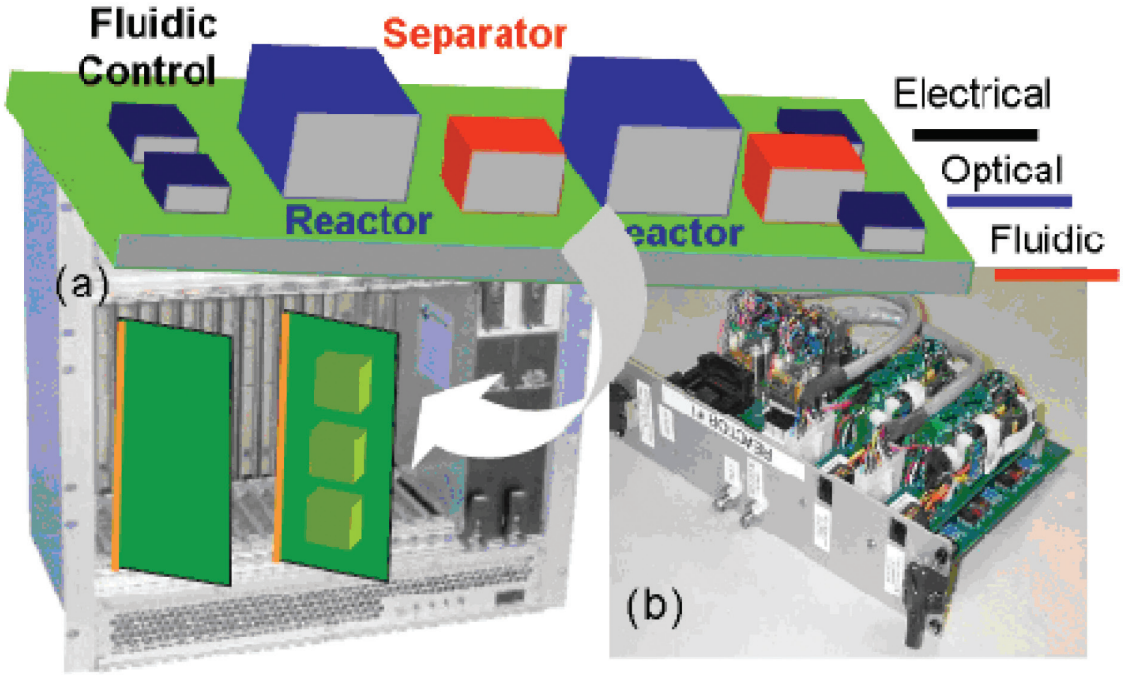
Integrated Microreactor System

H.R. Sahoo, E.R. Murphy, A. Guenther, N. Zaborenko, K.F. Jensen
Sponsorship: Deshpande Center for Technological Innovation

The realization of integrated microchemical systems will revolutionize chemical research by providing flexible tools for rapid screening of reaction pathways, catalysts, and materials synthesis procedures, as well as faster routes to new products and optimal operating conditions. Moreover, such microsystems for chemical production will require less space, use fewer resources, produce less waste, and offer safety advantages. The need for synthesizing sufficient quantities of chemicals for subsequent evaluation dictates that microchemical systems are operated as continuous systems. Such systems require fluid controls for adjusting reagent volumes and isolating defective units. The integration of sensors enables optimization of reaction conditions as well as the extraction of mechanistic and kinetic information.

We are developing integrated microchemical systems that have reactors, sensors, and detectors with optical fibers integrated on one platform. We are exploring new approaches for connecting modular microfluidic components into flexible fluidic networks. Real-time control of reaction parameters using online sensing of flowrate, temperature, and concentration allows for precise attainment of reaction conditions and optimization over a wide range of temperatures and flow-rates. The multiple microreactors on the system can be used together to give higher throughputs or they can be used independently to carry out different reactions at the same time. Figure 1 shows a schematic of an integrated microreactor platform along with an early stage microreactor "circuit board" [1].



▲ Figure 1: Schematic of an integrated microreactor platform along with an early stage microreactor "circuit board" [1].

REFERENCES

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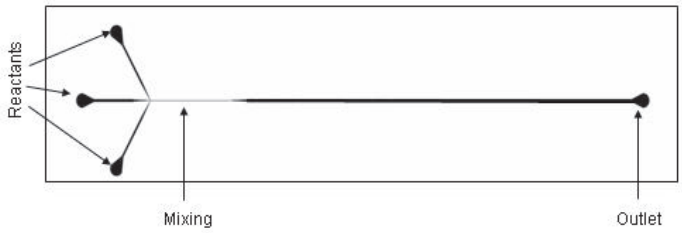
Crystallization in Microfluidic Systems

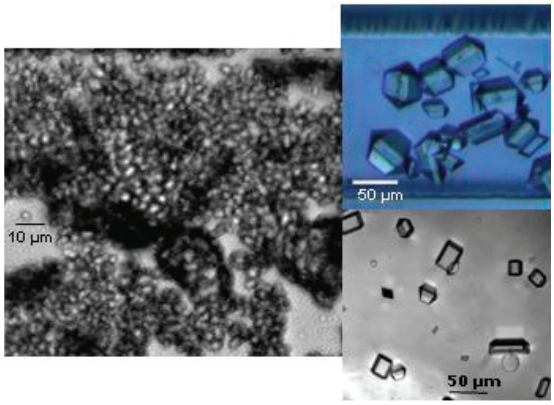
M. Sultana, K.F. Jensen
Sponsorship: Merck, Lucent Technologies

Microfluidic systems offer a unique toolset for discovering new crystal polymorphs and for studying the growth kinetics of crystal systems because of well-defined laminar flow profiles and online optical access for measurements. Traditionally, crystallization has been achieved in batch processes that suffer from non-uniform process conditions across the reactors and chaotic, poorly controlled mixing of the reactants, resulting in polydisperse crystal size distributions (CSD) and impure polymorphs. This reduces reproducibility and manufactures products with inhomogeneous properties. The short length scale in microfluidic devices allows for better control over the process parameters, such as the temperature and the contact mode of the reactants, creating uniform process conditions. Thus, these devices have the potential to produce crystals with a single morphology and a more uniform size distribution. In addition, microfluidic systems decrease waste, provide safety advantages, and require only minute amounts of reactants, which is most important when dealing with expensive materials such as pharmaceutical drugs.

Figure 1 shows a microfluidic device used for crystallization and Figure 2 shows optical images of different shapes and sizes of glycine crystals produced in reactor channels. A key issue for achieving continuous crystallization in microsystems is to eliminate heterogeneous crystallization – irregular and uncontrolled formation and growth of crystals at the channel surface, which ultimately clogs the reactor channel. We have developed a sheath flow microcrystallizer using microfabrication and hot embossing of poly(dimethylsiloxane) (PDMS) and cyclic olefin copolymer (COC) to prevent heterogeneous crystallization. We are currently working on integrating an online spectroscopy tool for *in situ* polymorph detection. Our ultimate goal is to develop an integrated microfluidic system for continuous crystallization with the ability to control polymorphism and online detection.



▲ Figure 1: Microfluidic reactor used for crystallization.

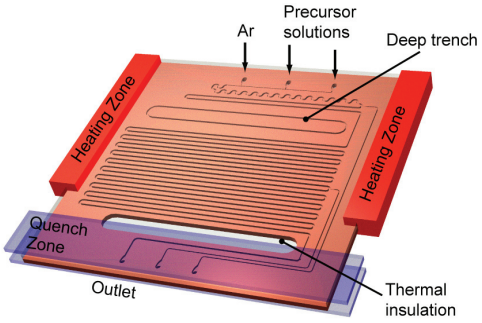


▲ Figure 2: Different sizes and shapes of glycine crystals produced in reactor channel.

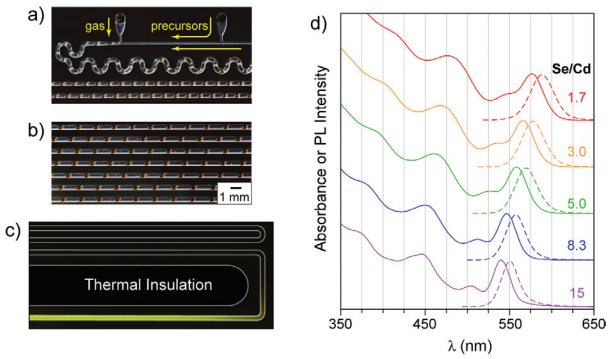
Microreactors for Synthesis of Quantum Dots

B.K.H. Yen, A. Günther, M.A. Schmidt, M.G. Bawendi, K.F. Jensen
Sponsorship: Microchemical Systems Technology Center, NSF, ISN

We have fabricated a gas-liquid segmented flow reactor with multiple temperature zones for the synthesis of quantum dots (QDs). In contrast to single-phase flow reactors, the segmented flow approach enables rapid mixing and narrow residence-time distributions, factors which have a strong influence on the ultimate QD size distribution. The silicon-glass reactor accommodates a 1-m long reaction channel (hydraulic diameter ~400-μm) and two shallow side channels for collecting reaction aliquots (Figure 1). Two temperature zones are maintained, a heated reaction region (>260°C) and a cooled quenching region (<70°C). As a model system, monodisperse CdSe QDs with excellent optical properties were prepared using the reactor. Cadmium and selenium precursor solutions are delivered separately into the heated section. An inert gas stream is introduced further downstream to form a segmented gas-liquid flow, thereby rapidly mixing the precursors and initiating the reaction. The reaction is stopped when the fluids enter the cooled outlet region of the device. Under conditions for a typical synthesis, the gas and liquid segments are very uniform (Figure 2a-b), and the QDs produced in the reactor possess narrow spectral features, indicative of monodisperse samples. The narrow particle size distributions arise directly from the enhanced mixing and narrow residence-time distribution realized by the segmented flow approach. Furthermore, the QD size can be tuned without sacrificing monodispersity by varying the Cd and Se precursor flow rates. In Figure 2d, the Se/Cd molar ratio was varied while keeping the total liquid and gas flow rates constant. Decreasing Se/Cd results in a substantial red shift of the QD effective band-gap (first absorption feature and photoluminescence peak), corresponding to larger QD diameters.



▲ Figure 1: Diagram of the reactor with heated reaction and cooled outlet regions. A through-etch section ensures that the two regions are thermally isolated. Channels etched in silicon (0.65-mm thick) were first passivated with an oxide layer (0.5-μm) and then sealed with an anodically bonded Pyrex wafer (0.76-mm thick).



▲ Figure 2: Images of the a) heated inlet and b) main channel sections of device during synthesis. Red segments: CdSe QD reaction solution. Dark segments: Ar gas. c) Time-exposure image of the cooled outlet region under UV irradiation. At reaction temperature (260°C), the QD photoluminescence (PL) is completely quenched, but once the fluid reaches the cooled region (<70°C), yellow PL is observed. d) The QD absorbance (solid) and PL (dotted) spectra obtained by varying the precursor feed ratio. The Se/Cd molar ratio is indicated.

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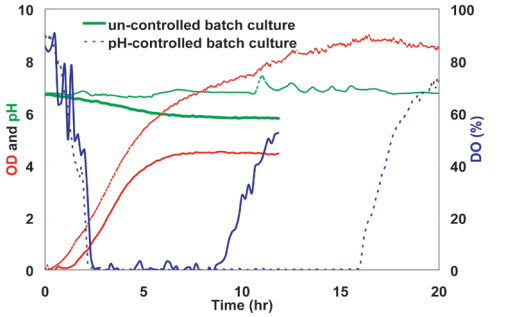
Polymer-based Microbioreactors for High Throughput Bioprocessing

Z. Zhang, G. Perozziello, Patrick Boyle, P. Boccazzi, A.J. Sinskey, K.F. Jensen
Sponsorship: DuPont-MIT Alliance

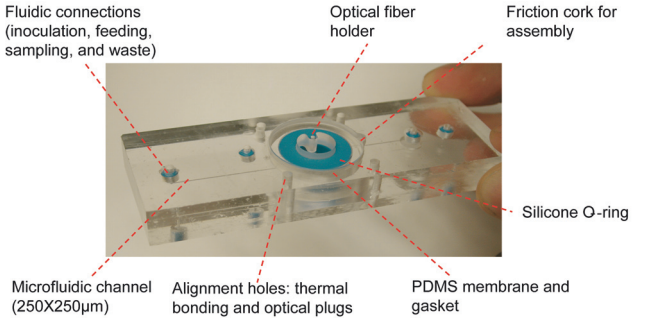
This project aims at developing high-throughput platforms for bioprocess developments. Based on the membrane-aerated microbioreactor [1], we have realized a microliter-volume, actively-mixed, and polymer-based microbioreactor by microfabrication and precision machining of PDMS and PMMA for batch [2] and continuous cultures [3] of microbial cells. Biological applications of microbioreactors, such as global gene expression of yeast cells [4], were demonstrated, and the parallel operation of multiple batch fermentations was realized by a multiplexed system [5].

As a very important operation for bioprocess developments, fed-batch process allows extensive control over environmental conditions in fermentations. Fed-batch fermentations in the microbioreactor were made possible by applying water evaporation through the PDMS membrane as a fluidic exit, and by combining passive feeding of water and active feeding of base, acid, and glucose solutions. Commercial microvalves were used to control pressure-driven liquid feeds to realize closed-loop pH control in the microbioreactor. For *Escherichia coli* fermentations, the pH value was successfully maintained within a certain range (Figure 1). Cells were physiologically healthier and remained active for longer periods of time (as shown by the dissolved oxygen curve), which in return yielded significantly higher biomass concentration at the end of experiments.

The microbioreactor was also integrated with the plug-*n*-pump microfluidic connectors [6], as well as incorporation of fabricated polymer micro-optical lenses and connectors for biological measurements to realize "cassettes" of microbioreactors (Figure 2). The fabrication process included precision machining and thermal bonding of PMMA devices. These integrations greatly simplified the setup and operation procedure and increased the signal-to-noise ratio for optical measurements for the cassettes, thus made the microbioreactors more compatible with high-throughput bioprocessing in multiplexed systems.



▲ Figure 1: Comparison of batch culture of E. coli FB21591 in rich LB media containing 8g/L glucose and 0.1 mol/L MES.



▲ Figure 2: Top view photograph of assembled and bonded microbioreactor "cassette."

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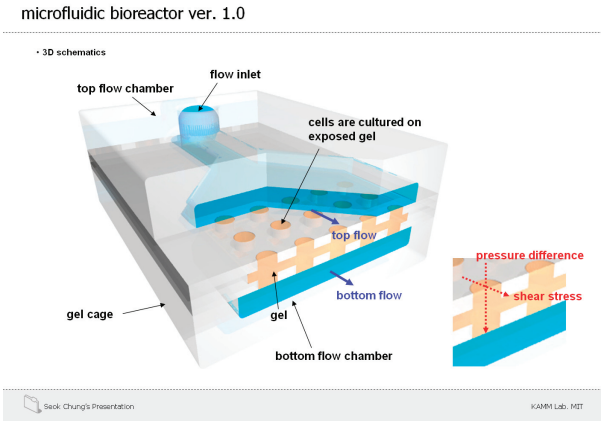
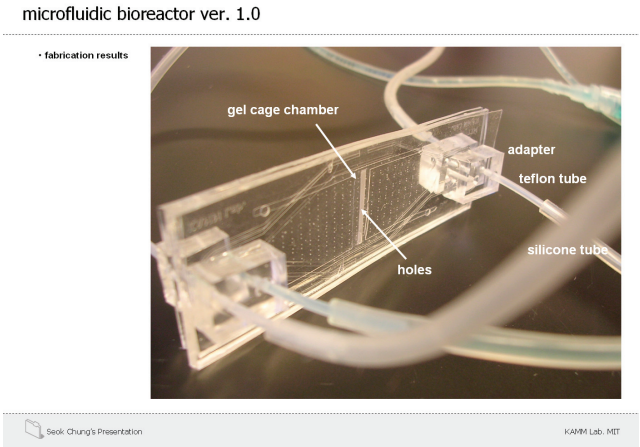
Micro-fluidic Bioreactors for Studying Cell-Matrix Interactions

S. Chung, P. Mack, V. Vickerman, J. Hsu, R. Kamm
Sponsorship: NIBIB, Draper Laboratories

Mechanical forces are important regulators of cell biology in health and disease. Cells in the vascular system are subjected to fluid shear stress, cyclic stretch, and differential pressure [1]. Numerous investigations have revealed the vast pathological and physical responses of endothelial cells to fluid shear stress by culturing the cells on the rigid surfaces of a flow chamber. This approach, however, fails to mimic the true environment of cells *in vivo* that grow on flexible, porous basement membranes with a defined microstructure [1-4]. In order to create an improved model for this *in vivo* condition, we developed a new microfluidic bioreactor system that enables us to study cell-matrix interactions on soft substrates made of gel under conditions of controlled shear stress and pressure difference. A gel cage consisting of three thin layers (Figure 1) is constructed from PDMS using a silicon master made by the deep RIE process. Flow chambers, also made of PDMS, are cured on an SU-8 patterned master. Separate channels are included that allow for filling this central chamber with a gel that mimics the extracellular matrix and also allows for independent control over the flows in the upper and lower channels. The assembled bioreactor is shown in Figure 2. To conduct experiments, we introduce a peptide solution into the gel cage, allow it to gel, and then seed cells on the gel surface exposed through the holes of gel cage. After cell adhesion, the flow chambers are sealed by the application of a vacuum to the top and bottom sides of the gel cage. Flows are then applied to each chamber with controlled pressures and flow rates. With this system, we will apply controlled shear stress and pressure on the cell layers. We plan to study the process of angiogenesis that entails the growth of vascular sprouts emanating from one endothelial surface and connecting with the other.



▲ Figure 1: Schematic drawing of microfluidic bioreactor. All layers are made of PDMS. Cells are cultured on exposed surfaces of gel in the holes of the gel cage; flows are induced in the channels above and below the gel cage.



▲ Figure 2: Photograph of the fabricated and bonded bioreactor. The gel cage consists of 3 PDMS layers, bonded by oxygen plasma. Flow chambers above and below the gel cage are fixed by vacuum connected by silicon tubes.

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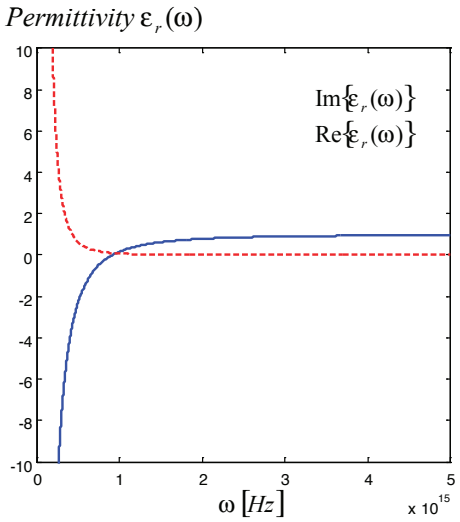
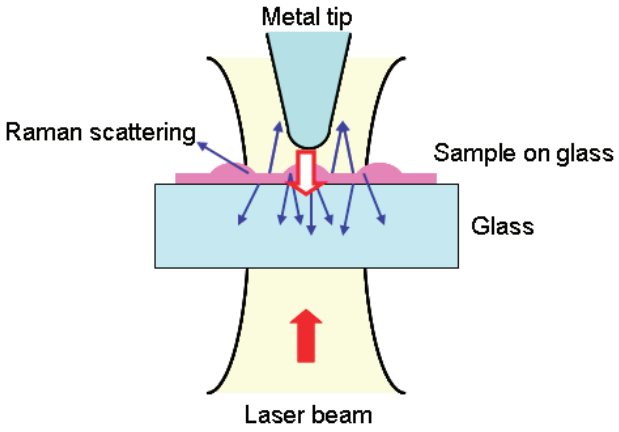
A Nanoscanning Platform for Biological Assays

S. Kim, S. Gouda, S.-G. Kim (P. So group)
Sponsorship: Intelligent Microsystems Center

An in-plane nanoscanning platform with switchable stiffness being developed at the Micro & Nano Systems Laboratory (MNSL) [1] can be an alternative to the existing atomic force microscope (AFM) system. The nanoscanning platform has a carbon nanotube (CNT) tip, which is known as one of the ideal candidates for AFM tips because of their superior mechanical and chemical properties. Raman Spectroscopy has gained a lot of interest as a tool for single molecule detection since it has easy and fast sample preparation and measurement compared to the existing technologies, such as X-ray crystallography and nuclear magnetic resonance. Among the several approaches attempted in order to enhance the weak Raman signals is tip enhanced raman spectroscopy (TERS). The enhancement of the electric field due to the plasmon resonance on the coated metal surface was predicted qualitatively [2]. The metal-coated CNT or CNT filled with Ag, Au, or Cu with a small diameter tip and high aspect ratio is ideal for TERS. The switchable stiffness AFM can work as a tool for imaging and placing the tip at the sub-nanometer proximity to a soft, molecular-scale biological sample, which would enhance the Raman signals.



▲ Figure 1: Dependency of frequency on the permittivity of silver. The negative sign of the real part of permittivity contributes to the enhancement of the electric fields near the metal surface.



▲ Figure 2: Schematic of TERS showing the enhancement of electric fields near the metal tip or metal-coated CNT tip.

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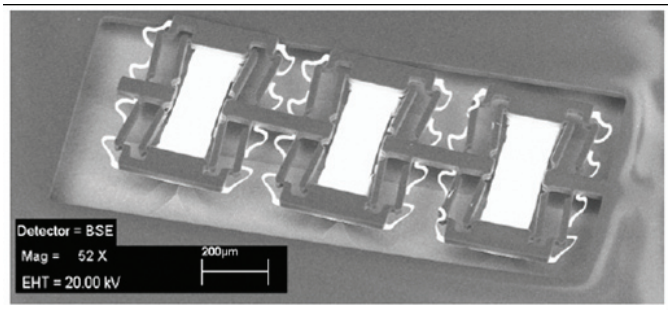
A Large Strain, Arrayable Piezoelectric Microcellular Actuator

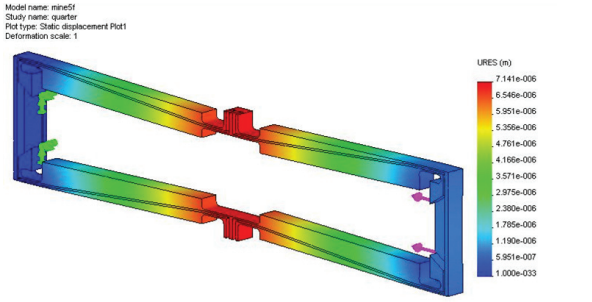
Z.J. Traina, S.-G. Kim
Sponsorship: Korean Institute of Metallurgy and Manufacturing (KIMM)

To provide a competitive actuating solution, micro-electromechanical-systems (MEMS)-based actuators need low operating power and form factors. Piezoelectrics provide substantially higher work-output/volume for a given voltage, when compared to other actuating solutions. A bow amplifier constructed of SU-8 beams and short length flexural pivots has been designed [1] and has demonstrated an amplification ratio of greater than 10:1. Current research focuses on increasing this amplification ratio and achieving the goal of 10% axial strain, while reducing parasitic out-of-plane bending inherent in the current fabrication process.

The overall goal of this project is to array one such actuator massively in series and in parallel in order to create a macro-scale, muscle-like actuator. Such a device would have widespread applications in mobile robotics, medicine, and aero/astronautics, where low power, high efficiency, and small form factors might be required.



▲ Figure 1: SEM image of three-unit cell bow actuators developed by N. Conway and S.G Kim, fabricated in series. Peak static displacement measured via microvision was 1.18 µm at 10V, with peak blocking force 55 µN.



▲ Figure 2: Finite Element Analysis (FEA) of a second revision micro-cellular actuator, showing axial strain in excess of 10%, (up to 15 µm per cell), with an amplification ratio greater than 14:1. Predicted blocking force is on the order of 10 µN.

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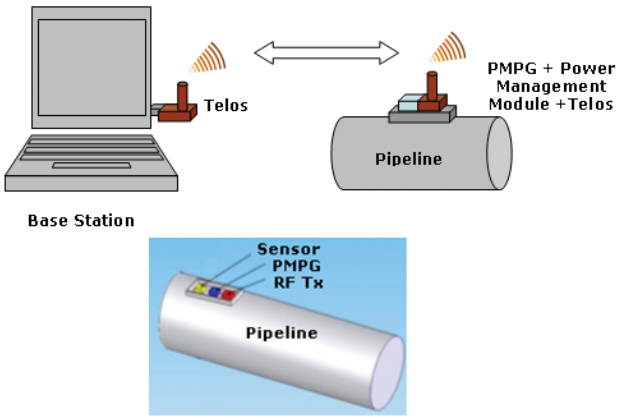
Self-powered Wireless Monitoring System Using MEMS Piezoelectric Micro Power Generator

R. Xia, C. Farm, W. Choi, S.-G. Kim
Sponsorship: NSF, Korean Institute of Machinery and Materials

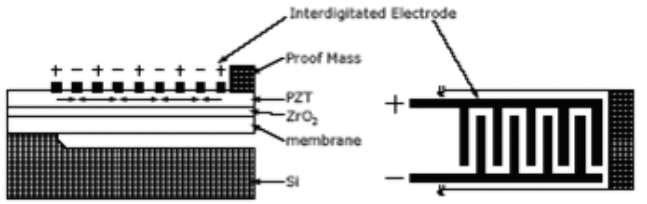
A thin-film lead zirconate titanate $Pb(Zr,Ti)O_3$ (PZT), MEMS Piezoelectric Micro Power Generator has been integrated with a commercial wireless sensor, Telos, to simulate a self-powered RF temperature monitoring system (Figure 1). Such a system has many important applications, ranging from structure to rotary system monitoring. Telos consumes 2270 μJ for 221 ms per measurement. The PMPG and power management module are designed to satisfy such power requirements

The first prototype of PMPG provides an average 1 μW, with a natural frequency of 13.9 kHz (Figure 2). It has an energy density of 0.74 mW-h/cm^2, which compares favorably to lithium ion batteries [1]. The second generation PMPG is designed to provide 0.173 mW of power at 3 V with a natural frequency of 150 Hz and maximum strain of 0.12% [2]. We increased the effective mass of the PMPG by adding a Si substrate with thickness of 525 μm to the beam structure. The increase in the effective mass increases the energy store in the device and its power output. The beam length is also increased to achieve a low resonant frequency. The third generation PMPG will use a serpentine structure, which can achieve a low frequency with minimum volume.

Since PMPG offers limited power, a storage capacitor and a power management module are implemented to power the sensor node at discrete time intervals [3]. The PMPG is first connected to a rectifier that converts AC to DC voltage. Each cycle consists of a charging interval, in which PMPG charges the capacitor, and operation intervals, in which Telos uses the energy from capacitor. We developed a test bed, which mimics that of a liquid gas pipe used in the Alaska where the PMPG device will be used to generate power for temperature sensors. Scaling/dimension factors as well as cost and robustness are considered in the design.



▲ Figure 1: Schematic of self-powered wireless monitoring system.



▲ Figure 2: First prototype for PMPG.

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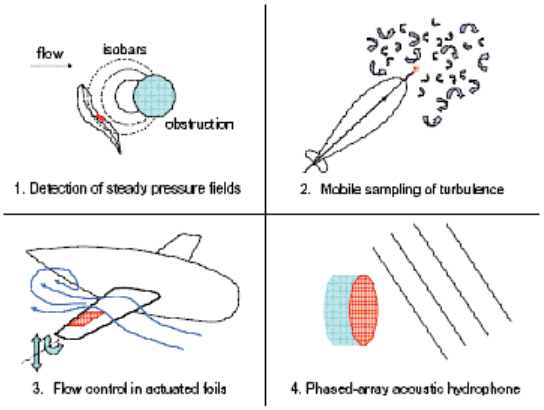
MEMS Pressure-sensor Arrays for Passive Underwater Navigation

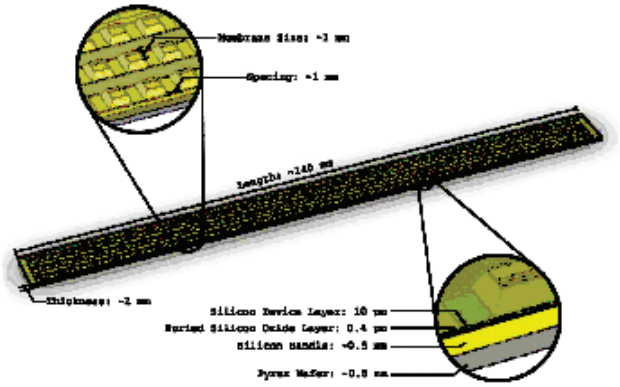
V.I. Fernandez, S.M. Hou, F.S. Hover, J.H. Lang, M.S. Triantafyllou
Sponsorship: NOAA: MIT Sea Grant College Program

MEMS pressure sensors have had broad applications in fields such as mining, medicine, automobiles, and manufacturing. Another application to be explored is in underwater vehicular navigation. Objects within a flow generate pressure variations that characterize the objects' shape and size. Sensing these pressure variations allows the unique identification and location of obstacles for navigation (Figure 1). This concept is inspired by existing biological systems. Fish have such a sensory lateral line, which they use to monitor all aspects of their hydrodynamic environment, including obstacles [2,5].

We propose to develop low-power sensors that passively measure dynamic and static pressure fields with sufficient resolution to detect objects generating the disturbance. We will also develop processing schemes that use the information from the sensors to identify objects in the flow environment. These sensors and processing software emulate the capabilities of the lateral line in fish. While active acoustic means can be used for object detection, the process is power-intensive, and depends strongly on the acoustic environment. A simpler alternative is to use a passive system that can resolve the pressure signature of obstacles. The system consist of arrays of hundreds or thousands of piezoresistive pressure sensors fabricated on etched silicon and Pyrex wafers [1,3,4,6] with diameters around 1 mm; the sensors are arranged over a flat or curved surface in various configurations, such as a single line, a patch consisting of several parallel lines (Figure 2), or specialized forms to fit the hull shape of a vehicle or its fins. The sensors will be packaged close together at distances of a few millimeters apart in order to resolve pressure and flow features near the array spacing, which in turn can be used to identify the overall features of the flow.



▲ Figure 1: Pressure-sensor array applications.



▲ Figure 2: Diagram of pressure-sensor array with basic structure depicted.

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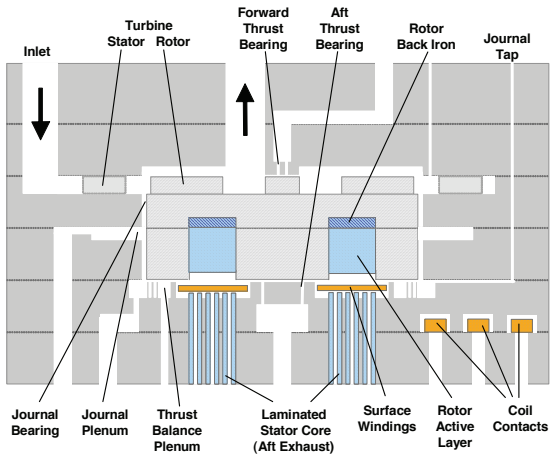
An Integrated Multiwatt Permanent Magnet Turbine Generator

B.C. Yen, M. Allen, F.F. Ehrich, A.H. Epstein, F. Herrault, L.C. Ho, S. Jacobson, J.H. Lang, H. Li, Z.S. Spakovszky, C. Teo, D. Veazie
Sponsorship: ARL Collaborative Technology Alliance

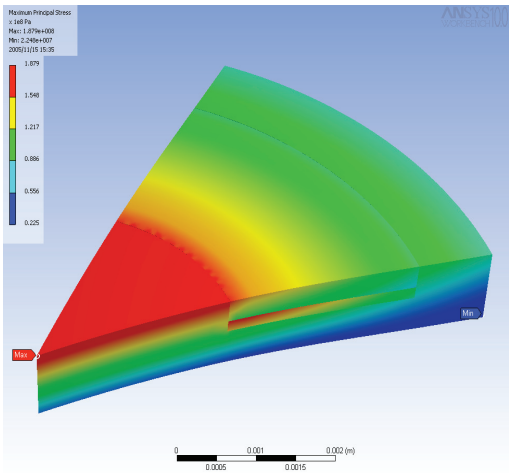
There is a need for compact, high-performance power sources that can outperform the energy density of modern batteries for use in portable electronics, autonomous sensors, robotics, and other applications. Previous research efforts on a micro-scale, axial-flux, permanent-magnet turbine generator [1-2] culminated in a spinning rotor test stand that delivered 8 W DC output power through a diode bridge rectifier with an overall generator system efficiency of 26.6%. In these experiments, the generator rotor was mounted via a steel shaft to an air-driven, ball-bearing supported spindle and spun to the desired operational speed.

Current research efforts aim to fully integrate the permanent-magnet (PM) generator design into the silicon micro-turbine engine fabrication process and create devices that can deliver 10 W DC output power when driven by compressed air. The integrated generator will couple energy from the compressed air to the rotor through microfabricated turbine blades attached to the backside of the rotor. One important challenge in this integration process is the structural integrity of the magnetic rotor spinning at a tip speed near 300 m/s, or equivalently 450 krpm.

Based on power requirements, a 300-μm thick circular NdFeB PM with an inner radius of 2.5 mm and an outer radius of 5 mm must be embedded into the silicon rotor on top of a 150 μm FeCoV back iron. FEA analysis shows that the maximum principle stress at 450 krpm in the silicon rotor, 900-μm thick and 12 mm in diameter, with bonded annular PM and back iron pieces, will be approximately 180 MPa through the entire structure. This stress is well below the tensile strength of silicon and FeCoV. However, because the PM is brittle and has a typical tensile strength around 83 MPa, it is unclear whether the material will fracture. Tests are currently underway to characterize the reference strength and Weibull modulus of the PM, and from these results, a working rotor design will be proposed.



▲ Figure 1: Conceptual schematic of the fully integrated surface-wound permanent magnet turbine generator. The bottom two wafers constitute the stator and coil winding of the generator while wafers 3, 4, and 5 form the magnetic rotor. A center-fed journal-bearing design is shown in the schematic, but an axial-fed design is also possible.



▲ Figure 2: An FEA simulation for the magnetic rotor structure spinning at 450 krpm. Because of the fully-bonded boundary conditions, most of the load is carried by the silicon hub. The maximum principal stresses in the silicon, PM, and back iron are 176.7 MPa, 188.0 MPa, and 184.5 Mpa, respectively.

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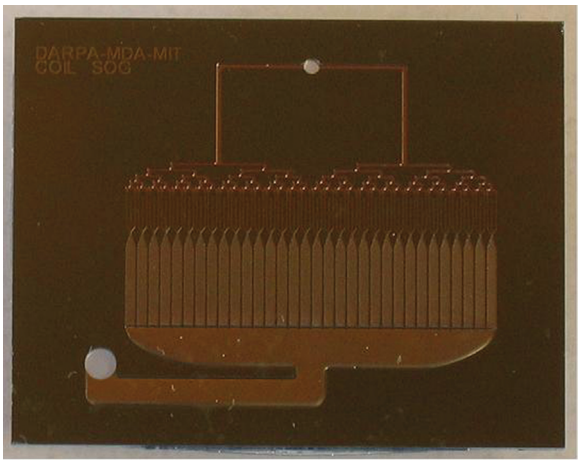
Micro-scale Singlet Oxygen Generator for MEMS-based COIL Lasers

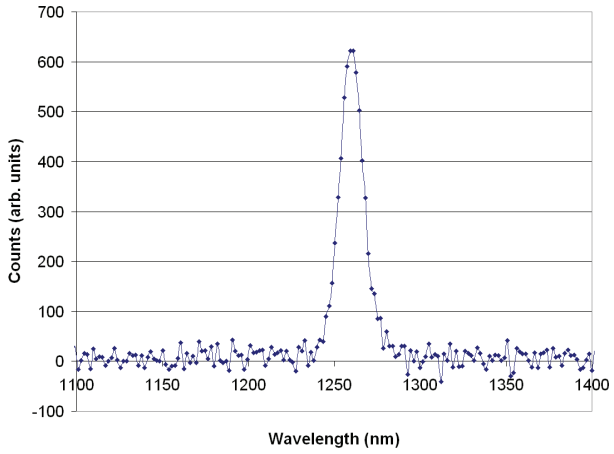
T. Hill, B. Wilhite, L. Velasquez, H. Li, A.H. Epstein, K.F. Jensen, C. Livermore
Sponsorship: DARPA, MDA

Conventional chemical oxygen iodine lasers (COIL) offer several important advantages for materials processing, including short wavelength (1.3 μm) and high power. However, COIL lasers typically employ large hardware and use reactants relatively inefficiently. This project is creating an alternative approach called microCOIL. In microCOIL, most conventional components are replaced by a set of silicon MEMS devices that offer smaller hardware and improved performance. A complete microCOIL system includes micro-chemical reactors, micro-scale supersonic nozzles, and micro-pumps. System models incorporating all of these elements predict significant performance advantages in the microCOIL approach [1].

Initial work focuses on the design, microfabrication, and demonstration of a chip-scale singlet oxygen generator (SOG), a micro-chemical reactor that generates singlet delta oxygen gas to power the laser. Given the extensive experience with micro-chemical reactors over the last decade [2-4], it is not surprising that a micro-SOG would offer a significant performance gain over large-scale systems. The gain stems from basic physical scaling; surface-to-volume ratio increases as the size scale is reduced, which enables improved mixing and heat transfer. The SOG chip demonstrated in this project, shown in Figure 1, employs an array of micro-structured packed-bed reaction channels interspersed with micro-scale cooling channels for efficient heat removal. Production of singlet oxygen has been confirmed via spontaneous emission (as shown in Figure 2) and mass spectrometry techniques. The yield (or fraction of singlet oxygen produced) is estimated at 70%, making the micro-SOG competitive with macro-scale alternatives.



▲ Figure 1: Photograph of completed microSOG device.



▲ Figure 2: The IR spectrum measured at the μSOG gas outlet. The peak at 1268 nm indicates the spontaneous decay of singlet oxygen into its triplet state.

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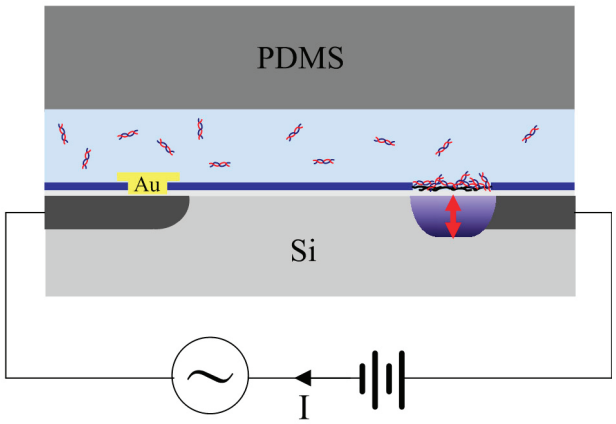
Label-free Microelectronic PCR Quantification

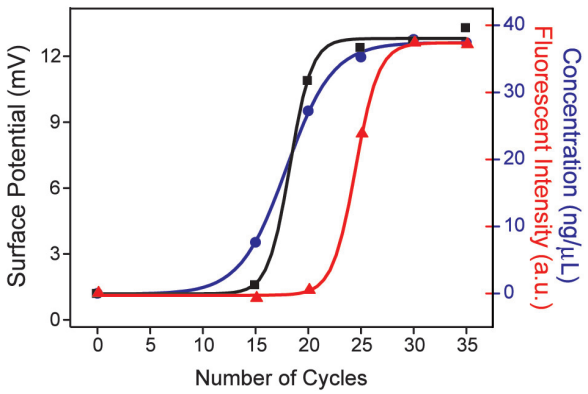
C.-S. Johnson Hou, N. Milovic, M. Godin, P. Russo, R. Chakrabarti, S.R. Manalis
Sponsorship: AFOSR, Hewlett Packard, MIT Sea Grant Program

The introduction of real-time monitoring of the polymerase chain reaction (PCR) represents a major breakthrough in specific nucleic acid quantification. This technique employs fluorescent intercalating agents or sequence-specific reporter probes to measure the concentration of amplified products after each PCR cycle. However, the need for optical components can limit the scalability and robustness of the measurement for miniaturization and field-uses. Moreover, the addition of external fluorescent reagents can induce inhibitory effects [1] and require extensive optimization [2].

We have developed a robust and simple method for direct label-free PCR product quantification using an integrated microelectronic sensor (Figure 1) [3]. The field-effect sensor can sequentially detect the intrinsic charge of multiple unprocessed PCR products and does not require sample processing or additional reagents in the PCR mixture. The sensor measures nucleic acid concentration in the PCR relevant range and specifically detects the PCR products over reagents such as Taq polymerase and nucleotide monomers. The sensor can monitor the product concentration at various stages of PCR and can generate a readout that resembles that of a real-time fluorescent measurement using an intercalating dye but without its potential inhibition artifacts (Figure 2). The device is mass-produced using standard semiconductor processes, can be reused for months, and integrates all sensing components directly on-chip. As such, our approach establishes a foundation for the direct integration of PCR-based *in vitro* biotechnologies with microelectronics.



▲ Figure 1: Cross-sectional drawing demonstrating the basis of the device measurement. Binding of charged molecules such as DNA on the sensor's surface alters the distribution of positive mobile charge carrier in silicon, results in a modulation of the depletion depth (red arrow), hence changing the capacitance. This change in capacitance is monitored by measuring the AC current between the sensor and the gold electrode.



▲ Figure 2: Comparison between steady state response of electronic measurements (black), real-time monitoring of PCR using Sybr Green I intercalating dye (red), and concentration analysis of the products using DNA Labchip kits (blue). No fluorescent labels were used for electronic detection and concentration measurements. However the discrepancy with the Sybr Green I measurement is likely due to partial inhibition of the PCR reaction by the fluorescent reagent.

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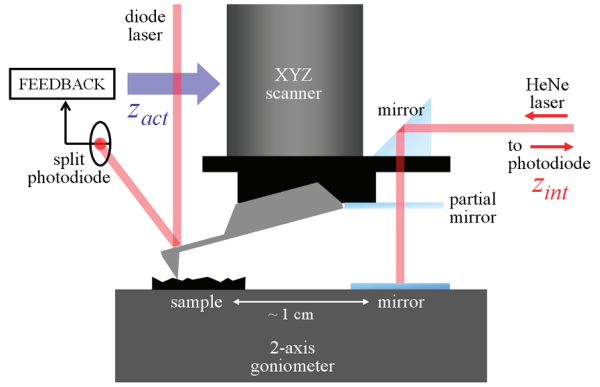
Atomic Force Microscopy with Inherent Disturbance Suppression for Nanostructure Imaging

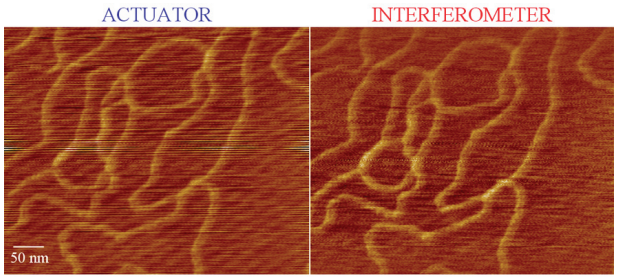
A. Sparks, S.R. Manalis
Sponsorship: AFOSR

Scanning probe imaging is often limited by disturbances, or mechanical noise, from the environment that couple into the microscope. We demonstrate on a modified commercial atomic force microscope that adding an interferometer as a secondary sensor to measure the separation between the base of the cantilever and the sample during conventional feedback scanning can result in real-time images with inherently suppressed out-of-plane disturbances (Figure 1) [1]. The modified microscope has the ability to resolve nanometer-scale features in situations where out-of-plane disturbances are comparable to or even several orders of magnitude greater than the scale of the topography. We present images of DNA in air from this microscope in tapping mode without vibration isolation, and show improved clarity using the interferometer as the imaging signal (Figure 2). The inherent disturbance suppression approach is applicable to all scanning probe imaging techniques.

We do not claim that image improvement will be comparable to these results on all SPMs and in all imaging environments. At present, this technique will be most effective in very noisy environments, such as a microfabrication facility, where Z disturbances overwhelm sample topography. However, there are two significant implications of this work: 1) vibration isolation, which is costly and consumes space, can be rendered unnecessary for noisy environments; and, 2) this technique can potentially outperform vibration isolation in any environment with further reduction of the interferometer noise floor.



▲ Figure 1: Experimental schematic. Zact (actuator) is the signal that is used for conventional scanning probe microscopy and includes a superposition of topography and mechanical disturbances. However, Zint (interferometer) reveals only topography and suppresses the mechanical disturbances.



▲ Figure 2: Due to Z disturbance effects, the actuator image appears streaked, and diagonal background stripes are present which are likely due to a resonance of the microscope. The interferometer image does not exhibit streaking and shows suppressed background noise.

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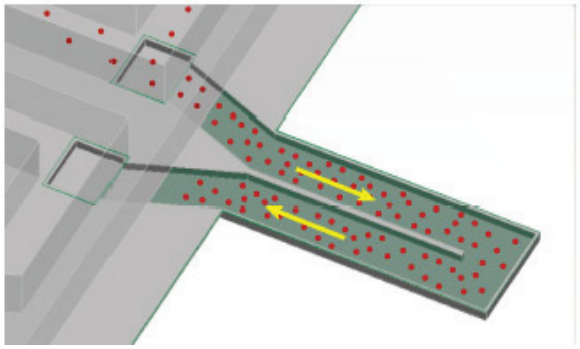
Vacuum-Packaged Suspended Microchannel Resonant Mass Sensor for Biomolecular Detection

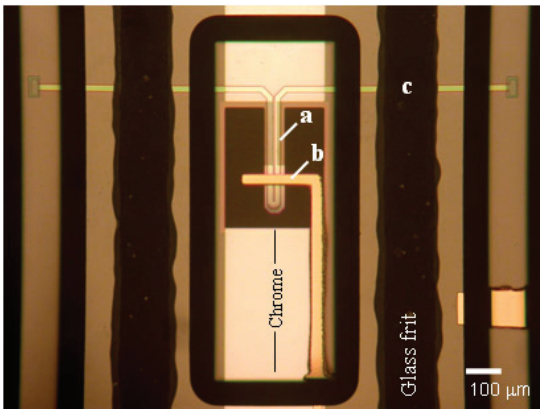
T.P. Burg, A.R. Mirza, N. Milovic, C.H. Tsau, G.A. Popescu, J.S. Foster, S.R. Manalis
Sponsorship: AFOSR, NIH

Microfabricated transducers enable the detection of biomolecules in microfluidic systems with nanoliter size sample volumes. Their integration with microfluidic sample preparation into lab-on-a-chip devices can greatly leverage experimental efforts in systems biology and pharmaceutical research by increasing analysis throughput while dramatically reducing reagent cost. Microdevices can also lead to robust and miniaturized detection systems with real-time monitoring capabilities for point-of-use applications.

We have recently fabricated, packaged, and tested a resonant mass sensor for the detection of biomolecules in a microfluidic format [1]. The transducer employs a suspended microchannel as the resonating element, thereby avoiding the problems of damping and viscous drag that normally degrade the sensitivity of resonant sensors in liquid (Figure 1). Our device differs from a vibrating tube densitometer in that the channel is very thin, which enables the detection of molecules that bind to the channel walls; this provides a path to specificity via molecular recognition by immobilized receptors. The fabrication is based on a sacrificial polysilicon process with low-stress LPCVD silicon nitride as the structural material, and the resonator is vacuum packaged on the wafer scale using glass frit bonding (Figure 2). Packaged resonators exhibit a sensitivity of 0.8 ppm/(ng•cm2) and a mechanical quality factor of up to 700. To the best of our knowledge, this quality factor is among the highest so far reported for resonant sensors with comparable surface mass sensitivity in liquid.



▲ Figure 1: Suspended microchannel resonator (SMR). In SMR detection, target molecules flow through a vibrating suspended microchannel and are captured by receptor molecules attached to the interior channel walls. What separates the SMR from existing resonant mass sensors is that the receptors, targets, and their aqueous environment are confined inside the resonator, while the resonator itself can oscillate at high Q in an external vacuum environment, thus yielding extraordinarily high sensitivity.



▲ Figure 2: Optical micrograph of a packaged cantilever resonator. The 300µm long beam contains a 1 x 20 µm microfluidic channel (a). An electrode on the glass surface above the cantilever enables electrostatic actuation (b). Glass frit conforms to the surface topography and does not collapse the thin channel in location (c) during bonding.

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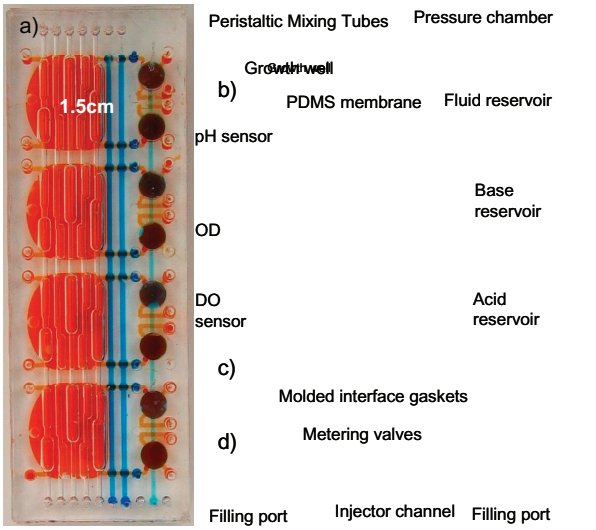
Microbial Growth in Parallel Integrated Bioreactor Arrays

H. Lee, R.J. Ram, P. Boccazzi, A. Sinskey
Sponsorship: DuPont-MIT Alliance

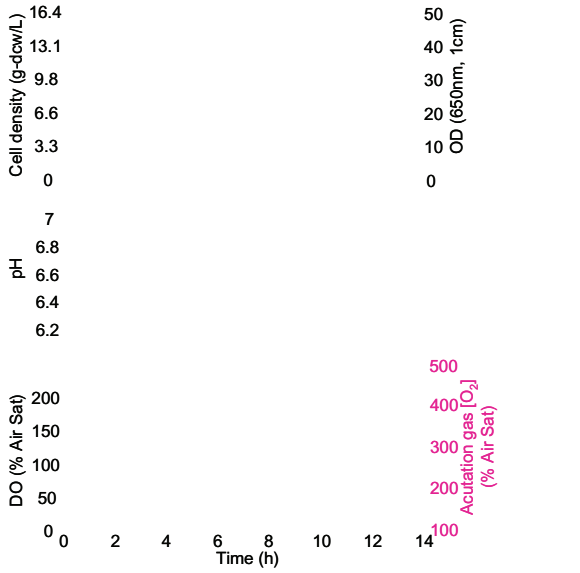
Bioprocesses with microbial cells play an important role in producing biopharmaceuticals such as human insulin and human growth hormone and other products such as amino acids and biopolymers. Because bioprocesses involve the complicated interaction between the genetics of the microorganisms and their chemical and environmental conditions, hundreds or thousands of microbial growth experiments are necessary to develop and optimize them. In addition, efforts to develop models for bioprocesses require numerous growth experiments to study phenotypes of microorganism.

We have designed and developed integrated arrays of microbioreactors that can provide the oxygen transfer and control capabilities of a stirred tank bioreactor in a high-throughput format. The devices comprise a novel peristaltic oxygenating mixer and microfluidic injectors (Figure 1), which are fabricated using a process that allows the combination of multiple scale (100 μm-1 cm) and multiple depth (100 μm-2 mm) structures in a single mold. The microbioreactors have a 100 μL working volume, a high oxygen-transfer rate ($k_La \approx 0.1s^{-1}$), and closed loop control over dissolved oxygen and pH (±0.1). Overall, the system supports eight simultaneous batch cultures in two parallel arrays with two dissolved oxygen thresholds, individual pH set points, and automated near real-time monitoring of optical density, dissolved oxygen concentration, and pH.

These capabilities allowed the demonstration of multiple *Escherichia coli* aerobic fermentations with growth to high cell densities (>12g-dcw/L, Figure 2), and individual bioreactor performance on par with bench scale stirred tank bioreactors. The successful integration of diverse microfluidic devices and optical sensors in a scalable architecture opens a new pathway for continued development of parallel bioreactor systems.



▲ Figure 1: Photograph and schematic of parallel integrated bioreactor array device. a) Photograph of four reactors integrated into a single module. b) Cross-section showing peristaltic oxygenating mixer tubes and fluid reservoir with pressure chamber. c) Top view of schematic showing optical sensors and layout of peristaltic oxygenating mixer and fluid injectors. d) Cross-section showing the fluid-injector membrane pinch valves.



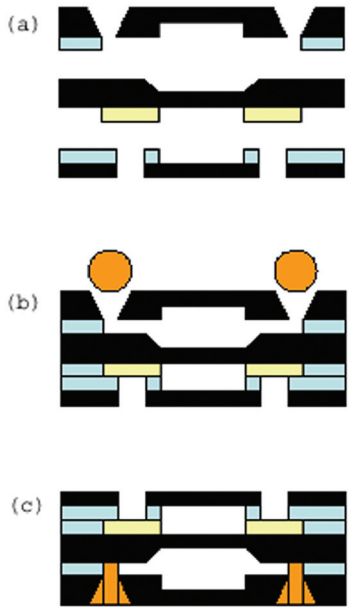
▲ Figure 2: Four *E. coli* fermentations on a defined medium performed in a single micro-bioreactor array module. The heavy black line indicates the mean of the cell density and pH replicates and the minimum of the dissolved oxygen replicates. The pH was controlled at 6.9 until the base reservoirs were depleted. Due to differences in the k_La, the oxygen concentration in three of the reactors did not remain near the set point. The oxygen concentration of the mixer actuation gas (bold magenta dashes) is shown by the orange dashed line and approximately follows the exponential growth of the cells.

Vacuum-Sealing Technologies for Micro-chemical Reactors

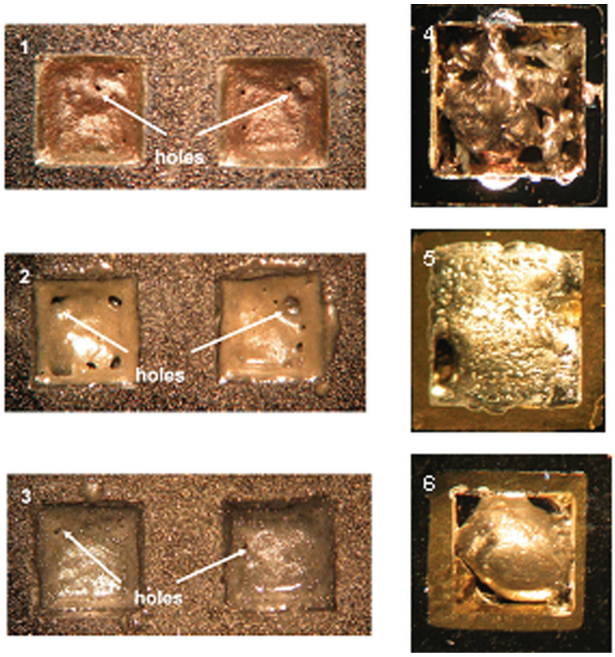
K. Cheung, K.F. Jensen, M.A. Schmidt
Sponsorship: ARO MURI

Current portable power sources may soon fail to meet the demand for increasingly larger power densities. To address this concern, our group has been developing MEMS power generation schemes that are focused around fuel cells and thermophotovoltaics. At the core of these systems is a suspended tube micro-reactor that has been designed to process chemical fuels [1]. Proper thermal management is critical for high reactor efficiency, but substantial heat loss is attributed to conduction through air. A straightforward solution is to eliminate the heat-loss pathways associated with air by means of a vacuum package. This work explores a glass-frit bonding method for vacuum sealing.

Optimization of pre-sintering and bonding parameters of the glass frit produced a repeatable and robust hermetic seal. Encounters with outgassing issues prompted an alternate two-step packaging process illustrated in Figure 1. New capping dies were fabricated, test devices were packaged, and the final seal-off was attempted with various materials [2]. Several experimental results appear in Figure 2. The glass frits are undesirable since they produce holes from material breakdown when heated in a vacuum. The gold-indium solder appears promising but holes formed due to internal outgassing. Extended heating to assist outgassing resulted in the delamination of the solder from the wetting metal. Recent work has been conducted to evaluate oxidized caps and lead-tin solder as solutions to these problems. Enhancements through the incorporation of non-evaporable getters will be assessed once a vacuum package is achieved.



▲ Figure 1: Basic concept of the two-step approach. (a) Initial bond in box furnace (blue = frit, black = silicon, yellow = metallization); (b) place solder/frit (orange) into pump-out hole; and (c) final seal-off.



▲ Figure 2: Experimental results of final seal-off attempts with various materials and conditions (1) Diemat DM2700PF (2) Semcom B-10105 (3) Semcom B-10127 (4) 82Au/18In (5) 80Au/20In (6) 80Au/20In extended outgassing.

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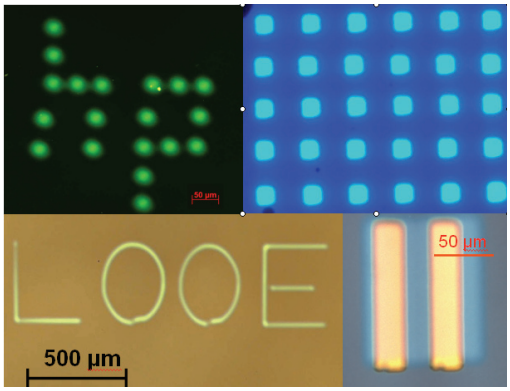
Direct Patterning of Organic Materials and Metals Using Micromachined Printheads

V. Leblanc, J. Chen, D.M. Schut, P. Mardilovich, V. Bulovic, M.A. Schmidt
Sponsorship: Hewlett-Packard

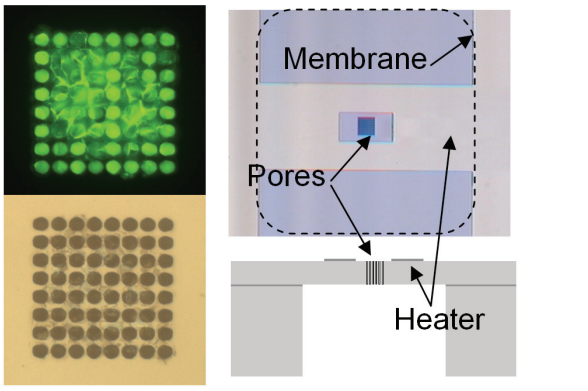
Organic optoelectronic devices are promising for many commercial applications if methods for fabricating them on large-area, low-cost substrates become available. Our project investigates the use of MEMS in the direct patterning of materials needed for such devices. By depositing the materials directly from the gas phase, without liquid phase coming in contact with the substrate, we aim to avoid the limitations of inkjet printing such materials.

In our first demonstration, we used an electrostatically actuated micromachined shutter integrated with an x-y-z manipulator to modulate the flux of evaporated organic semiconductors and metals and to generate patterns of the deposited materials. We printed arbitrary patterns of organic semiconductor Alq_3 (tris(8-hydroxyqunolinato) aluminum) and metal silver on glass substrates. We also printed pentacene/silver organic field effect transistor (OFET) and arrays of organic light emitting devices (OLED), as shown in Figure 1. This printing technique can pattern small-molecule organic light-emitting devices at high resolution (800 dpi).

The next stage of this project investigates the use of a microporous layer with integrated heaters for local evaporation of the materials. The microfabricated device is shown in Figure 2. The material to be printed is delivered to the porous region in liquid or gas phase and deposits inside the pores. An integrated heater then heats up the porous area and the material is re-evaporated from the pores onto the substrate. Compared to the first generation of printheads, the problems of crashing and stiction are avoided, since there is no moving part. Clogging is also limited since most of the material is removed during each printing cycle. Other advantages include the smaller quantity of organic material used, and the reduced substrate heating. Such a printhead would ultimately be integrated with an ink-jet printer for the delivery of liquid phase material into the porous region.



▲ Figure 1: Patterns obtained using our direct patterning method. Clockwise from top left: photoluminescence of Alq3 pixels, electroluminescence of OLED array with 30-micron pixels, and pictures of an OFET and a silver line pattern.



▲ Figure 2: Left: Pictures of the pores seen from the front of the device, top: fluorescent imaged after Alq3 was introduced from the back; bottom: optical microscope picture after the integrated heater re-evaporated the material. Right: Optical microscope image and schematic of device.

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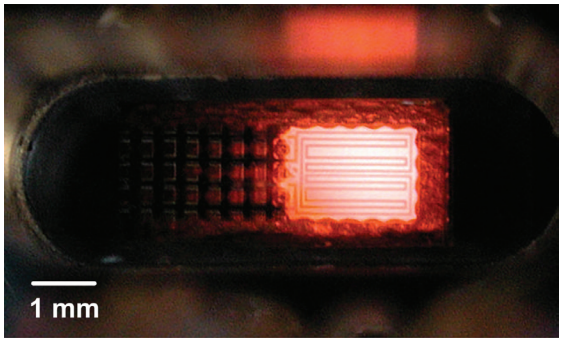
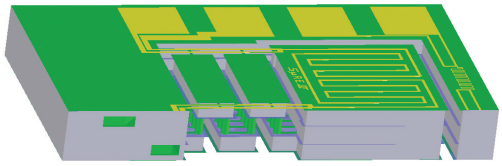
A Thermophotovoltaic (TPV) MEMS Power Generator

O.M. Nielsen, K.F. Jensen, M.A. Schmidt
Sponsorship: ARO MURI

For a number of years, batteries have not kept up with the fast development of microelectronic devices. The low energy densities of even the most advanced batteries are a major hindrance to lengthy use of portable consumer electronics such as laptops and of military equipment that most soldiers carry today. Furthermore, battery disposal constitutes an environmental problem. Hydrocarbon fuels exhibit very high energy densities in comparison, and micro-generators converting the stored chemical energy into electrical power at even modest levels are therefore interesting alternatives in many applications. This project focuses on building thermophotovoltaic (TPV) micro-generators, in which photocells convert radiation from a combustion-heated emitter into electrical power. TPV is an indirect conversion scheme that goes through the thermal domain and therefore does not exhibit very high efficiencies (10-15% max). However, because of its simple structure and because the combustor and photocell fabrication processes do not need to be integrated, the system is simpler to micro-fabricate than other generator types, e.g., thermoelectric systems and fuel cells. It is also a mechanically passive device that is virtually noiseless and less subject to wear than engines and turbines. In this TPV generator, a catalytic combustor, the suspended micro-reactor (SμRE) (Figure 1), is heated by combustion of propane and air, and the radiation emitted is converted into electrical energy by low-bandgap (GaSb) photocells. Net power production of up to 1 mW has been achieved [1], constituting a promising proof of concept. A new version of the SμRE is currently under fabrication. This new design (Figure 2) aims to address several problems existing in the earlier version, including fabrication difficulties, low burst pressure of the tubes, and low emitter surface area.



▲ Figure 1: Suspended micro-reactor (SμRE I) for fuel processing and TPV energy conversion heated to ~900°C.



▲ Figure 2: Three-dimensional model of the new suspended micro-reactor (SμRE III).

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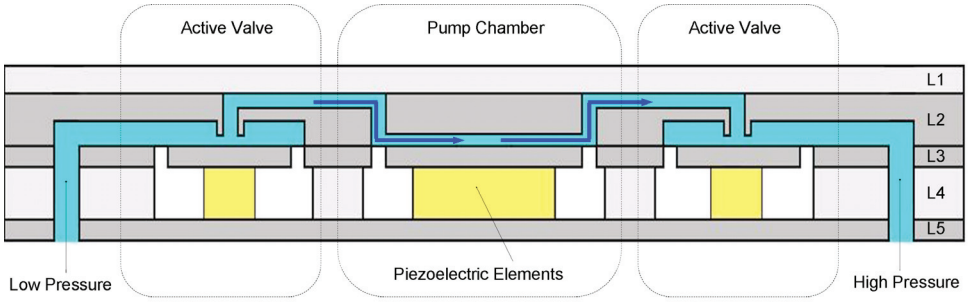
MEMS Vacuum Pump

V. Sharma, M.A. Schmidt
Sponsorship: DARPA

There are many advantages to miniaturizing systems for chemical and biological analysis. Recent interest in this area has led to the creation of several research programs, including a micro gas analyzer (MGA) project at MIT. The goal of this project is to develop an inexpensive, portable, real-time, and low-power approach for detecting chemical and biological agents. Elements entering the MGA are first ionized, then filtered by a quadrupole array, and sensed using an electrometer. A key component enabling the entire process is a MEMS vacuum pump, responsible for routing the gas through the MGA and increasing the mean free path of the ionized particles so that they can be accurately detected.

There has been a great deal of research done over the past 30 years in the area of micro pumping devices [1, 2]. We are currently developing a displacement micro-vacuum pump that uses a piezoelectrically driven pumping chamber and a pair of piezoelectrically driven active-valves; the design is conceptually similar to the MEMS pump reported by Li *et al.* [3]. We constructed accurate computer models for all aspects of the pump's operation: a compressible mass flow model of the flow rates, the pressure, the density, and the Mach number in the different parts of the pump in both the sonic and subsonic regimes [4], and a nonlinear plate deformation model of the stresses experienced by the pistons, tethers, and walls of the pump during operation [5], for any chosen dimensions and material properties.

Using these models we have defined a process flow for our first-generation MEMS vacuum pump designed to meet our first-term goals. A schematic of this pump that we started fabricating is shown in Figure 1 below. For ease in testing we have decided to fabricate only Layers 1-3 and constructed a testing platform that will drive the pistons pneumatically. This will allow for rapid characterization of pumping performance as well as chamber and valve designs for several dies at once without having to incorporate piezos in each case. The final device will be driven using low-voltage, low-loss, piezoelectric-stacks incorporated into Layer 4 and will include Layer 5 for structural support.



▲ Figure 1: Schematic of the MEMS vacuum pump. Layers 1 and 4 are glass, Layer 2 forms the chambers and channels using double-side polished silicon, Layer 3 forms the pistons and tethers being silicon-on-insulator, and Layer 5 is single-polished silicon. For testing and characterization, only Layers 1-3 are being fabricated.

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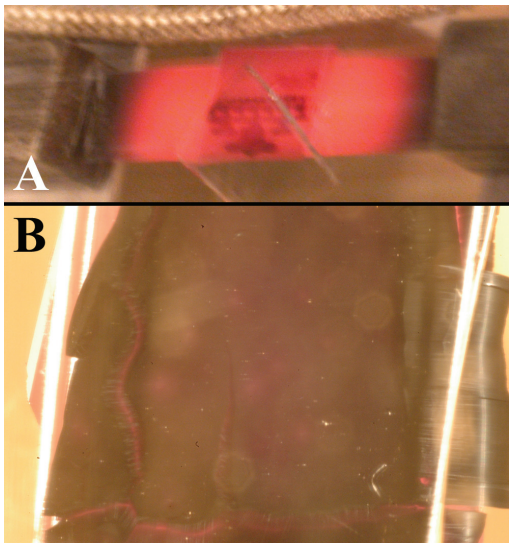
Rapid and Shape-Controlled Growth of Aligned Carbon Nanotube Structures

A.J. Hart, L.C. van Laake, A.H. Slocum
Sponsorship: Deshpande Center, NSF, Fannie and John Hertz Foundation

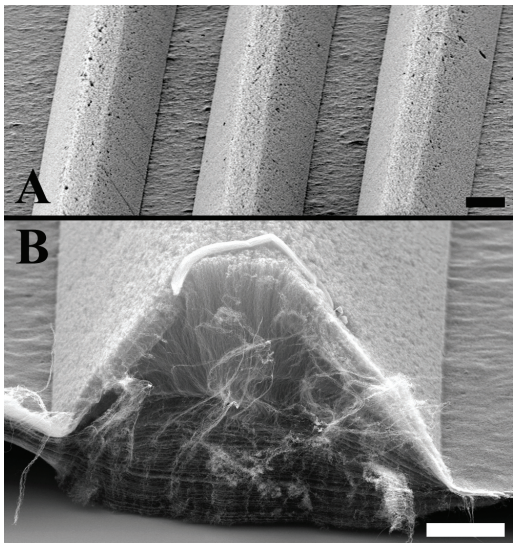
We present approaches for growth of aligned carbon nanotube (CNT) structures on silicon substrates, based on atmospheric pressure chemical vapor deposition (CVD) using a Fe/Al_2O_3 catalyst film in C_2H_4/H_2. First, vertically-aligned films of small-diameter (5-10 nm) multi-walled CNTs (MWNTs) are grown to 0.9 mm thickness in 15 minutes and 1.8 mm in 60 minutes, using a conventional 1-inch-diameter tube furnace [1]. The catalyst is patterned by photolithography, and the growth rate of CNT microstructures depends on the local areal density of catalyst, which is analogous to loading effects in plasma etching process. Further, using a novel apparatus where the silicon substrate is resistively heated, we achieve CNT film thickness of 3 mm in just 20 minutes along with rapid (100°C/s) control of the substrate temperature and optically image the film during growth (Figure 1).

By placing a weight on the catalyst-coated substrate, we measure the force which can be exerted by a growing CNT film and demonstrate that the film thickness after a fixed growth time and the alignment of CNTs within the film decrease concomitantly with increasing applied force [2]. We utilize this principle to fabricate three-dimensional structures of CNTs (Figure 2) that conform to the shape of a microfabricated template. This technique is a catalytic analogue to micromolding of polymer and metal microstructures; it enables growth of nanostructures in arbitrarily-shaped forms and does not require patterning of the catalyst.

Finally, we perform combinatorial flow studies of CNT growth using an array of parallel microchannels fabricated by KOH etching of silicon [3]. We observe transitions in CNT yield and quality along the microchannels, grow CNT structures that are aligned by gas flows in the microchannels, and fabricate CNT-filled microchannels for applications such as microfluidic filters.



▲ Figure 1: Growth of a CNT film on a resistively heated silicon substrate: (a) suspended silicon substrate at 750°C; (b) optical top-view image of CNT film during growth.



▲ Figure 2: The CNT microforms fabricated by growth under mechanical pressure: (a) Microforms fabricated using KOH-etched microchannel template. (b) Cross-section of a trapezoidal CNT microform.

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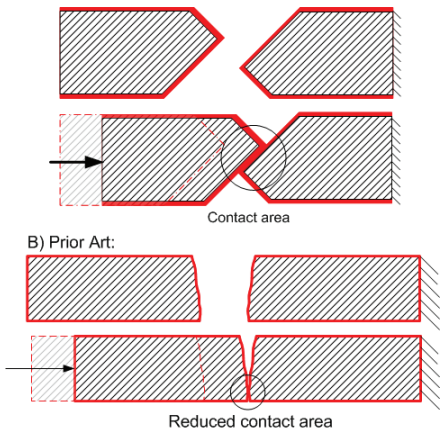
A Low Contact Resistance MEMS-Relay

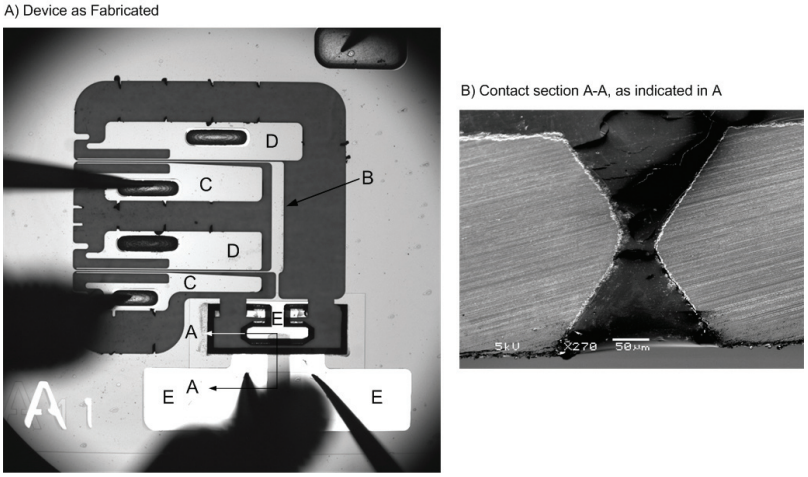
A.C. Weber, J.H. Lang, A.H. Slocum
Sponsorship: ABB Corporate Research, Baden-Daettwil

A low contact resistance MEMS-relay featuring highly parallel and planar oblique contacts has been fabricated and is currently being tested. The contacts are etched in silicon using a potassium hydroxide (KOH) solution. An offset between the wafer-top and the wafer-bottom KOH masks produces the oblique contact geometry schematically shown in Figure 1A.

In contrast, many prior art MEMS devices [1-3] have rough, non complementary contacts. As these surfaces touch, they do so in a small number of high points, as shown in Figure 1B, which significantly reduces the effective contact area and leads to a high contact resistance and a low current carrying capacity. Additionally, vertical contacts are prone to poor metallization, which further affects the device's contact resistance. Our MEMS-relay, shown in Figure 2, is composed of a compliant mechanism (B), a pair each of engaging (C) and disengaging (D) rolling-point "Zipper" actuators [4-5], and a pair of planar and parallel contacts (E).The relay is fabricated by a combination of deep reactive ion etching (DRIE) and KOH etching. Nested masks are used to pattern both wafer-through etches. Low stress silicon nitride (Si_3N_4), which will later be used as a KOH mask, is patterned initially on both sides of the device wafer. A silicon oxide film is deposited on the KOH mask. The compliant mechanism and actuators are then etched through DRIE and a second Si_3N_4 film is deposited. The second Si_3N_4 film is patterned using a "shadow" (through-etched) wafer as a mask. The oxide is selectively etched to reveal the buried nitride mask. The contacts are etched in KOH solution. Both Si_3N_4 and oxide films are stripped and a thermal oxide, which insulates both the electrostatic actuators and the relay contacts from the rest of the device, is grown. Gold is evaporated over both sides of the insulated contacts and the device wafer is anodically bonded to a Pyrex handle wafer. Experimental pull-in and drop-out voltages of 70 V and 40 V, respectively, agree with the model. Contact travel of 50 μm prevents arcing as the load circuit is switched on and off. A contact resistance of 50 mΩ was demonstrated by our group using an externally actuated structure as a proof of concept for the contact design [4]. Our group continues to develop these MEMS relays for power applications.



▲ Figure 1: Schematic cross section of oblique planar parallel contacts (A), schematic cross section of prior art (B).



▲ Figure 2: Device as fabricated (A), SEM contact cross section A-A of oblique contacts as shown in Figure 2A (B). The die saw causes the rough edge of the static contact in (B).

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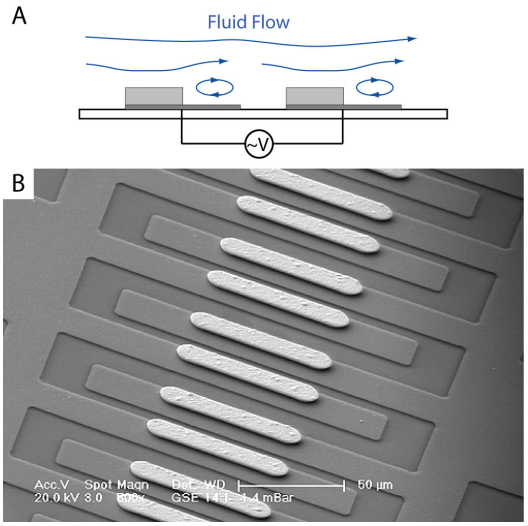
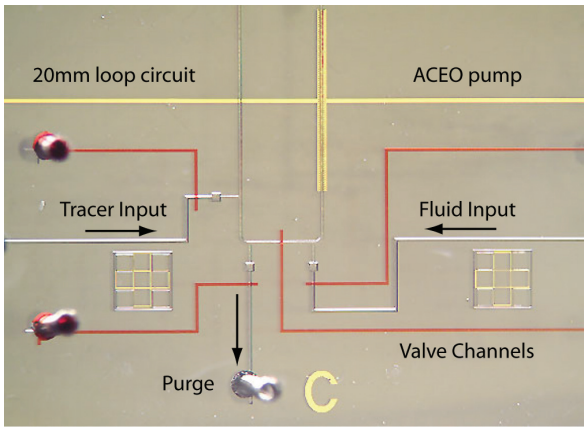
Fast Three-Dimensional Electrokinetic Pumps for Microfluidics

J.P. Urbanski, J. Levitan, M. Bazant, T. Thorsen
Sponsorship: ISN

Electrokinetic pumps are attractive for portable and flexible microfluidic analysis systems, since they operate without moving parts using low (battery-powered) alternating potentials. Since the discovery of AC electro-osmosis (ACEO) in the late 1990s, there has been much work in designing planar, periodic pumps, which exploit broken symmetry in electrode spacing and width to produce a streaming flow over a surface. Although surface-height modulation has been suggested as another means of breaking symmetry[1], it has never been numerically or experimentally pursued. Recently, Bazant and Squires described more general flows due to induced charge electro-osmosis (ICEO) around three-dimensional metal structures[2], which has since been realized experimentally in microfluidic systems[3]. Motivated by ICEO around raised electrodes, we are developing a variety of new three-dimensional AC electrokinetic pumps capable of much faster directional flows than planar ACEO pumps (for the same applied voltage and minimum feature size) by an order of magnitude according to the usual low-voltage model. This phenomena and an example microfabricated device are illustrated in Figure 1. We test and improve our theoretical designs experimentally in a microfluidic loop[4], as shown in Figure 2. Our pumps involve interdigitated planar electrodes with raised metal structures from a simple electroplating step, which leads to greatly enhanced pumping.



▲ Figure 1: (A) Schematic diagram of fluid flow that may be generated by an AC field between two electrodes located on a substrate. This "fluid conveyor belt," containing partially raised electrodes, exploits naturally occurring fluid rolls to pump fluid in microchannels with voltages < ~10 V. (B) Electroplating is used to create the raised geometry on repeated periods of planar patterned electrodes.



▲ Figure 2: A microfluidic device featuring a closed loop channel is used to test AC electrokinetic pump designs. The PDMS chip, which caps the electrodes, provides fluid inputs and outputs, and isolates the working pump from external pressure perturbations. This approach enables systematic characterization of pump performance as a function of input voltage and frequency. The scale bar indicates 1 mm.

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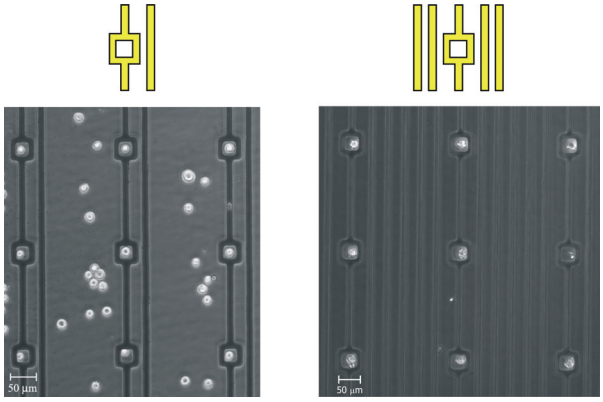
BioMEMS for Control of the Stem-cell Microenvironment

L. Kim, A. Rosenthal, S. Sampattavanich, J. Voldman
Sponsorship: NIH

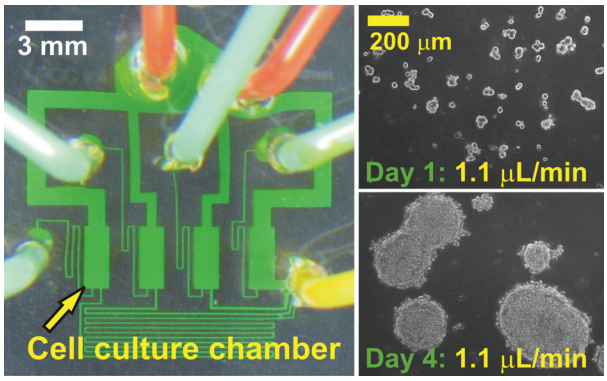
The stem-cell microenvironment is influenced by several factors including cell-media, cell-cell, and cell-matrix interactions. Although conventional cell-culture techniques have been successful, they offer poor control of the cellular microenvironment. To enhance traditional techniques, we have designed a microscale system to perform massively parallel cell culture on a chip.

To control cell-matrix and cell-cell interactions, we use dielectrophoresis (DEP), which uses non-uniform AC electric fields to position cells on or between electrodes [1]. We present a novel microfabricated DEP trap designed to pattern large arrays of single cells (Figure 1, left). We have experimentally validated the trap using polystyrene beads and cells, showing excellent agreement with our model predictions [2]. In addition, by placing interdigitated electrodes between the traps, we can prevent cells from sticking to the substrate outside the traps (Figure 1, right).

To control cell-media interactions, we have developed a microfluidic device for culturing adherent cells over a logarithmic range of flow rates (Figure 2, left) [3]. The device controls flow rates via a network of geometrically-set fluidic resistances connected to a syringe-pump drive. We use microfluidic perfusion to explore the effects of continuous flow on the soluble microenvironment. We have demonstrated logarithmically-scaled perfusion culture of mouse embryonic stem cells over 4 days, with flow rates varying > 300x across the array. Cells cultured at the slowest flow rate did not proliferate while colonies at higher flow rates demonstrated healthy round morphology (Figure 2, upper and lower right) and expressed the stem-cell marker Oct-4. These microfabricated platforms will enable precise and unique control over the cellular microenvironment, allowing novel cell biology experiments at the microscale.



▲ Figure 1: Single DEP trap (upper left). 3 × 3 array of murine fibroblast cells loaded in the DEP traps (lower left). Single DEP trap with interdigitated electrodes (upper right). 3 × 3 array of HeLa cells loaded in the DEP traps, with interdigitated electrodes between traps to prevent cell sticking (lower right).



▲ Figure 2: Microfluidic 1 × 4 array of cell culture chambers for creating a logarithmic range of flow rates (left). Mouse embryonic stem cell colonies exhibit healthy morphology as they grow from Day 1 to Day 4 (right) [4].

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Microfluidic/Dielectrophoretic Approaches to Selective Microorganism Concentration

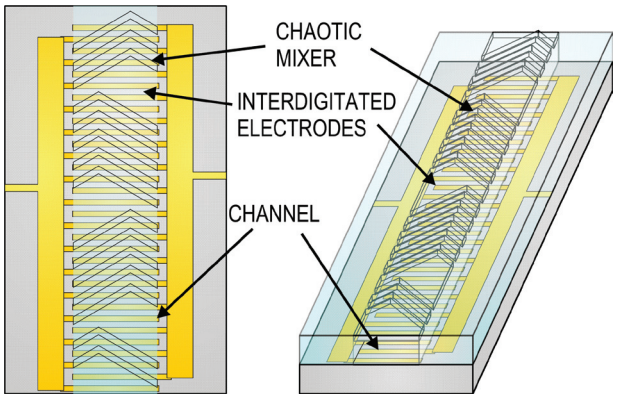
H.-Y. Lee, K.A. Puchala, J. Voldman
Sponsorship: Draper Laboratories, NASA, MIT

This project focuses on the development of microfabricated microfluidic/dielectrophoretic devices capable of concentrating micron-size particles from complex liquids, for example water containing contaminants such as dust, sand, protein or soot. The concentrated particles of interest, such as pathogenic bacteria and spores, can then be delivered in small aliquots to the appropriate sensor for identification.

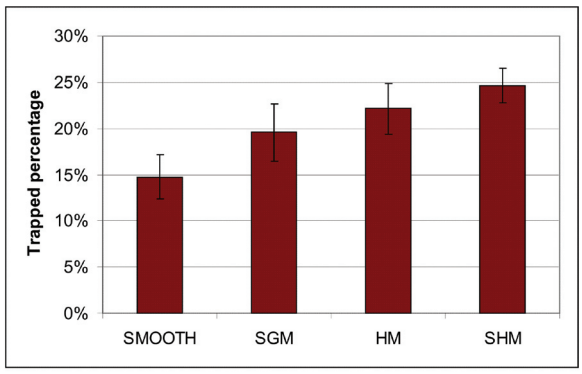
The micro-concentrator exploits the phenomenon of dielectrophoresis–the force on polarizable particles in spatially non-uniform electric field [1]–to trap the particles from the flow stream in order to subsequently concentrate them by release into a smaller volume of liquid. Dielectrophoresis does not negatively affect the liquid or the particles on which it operates. In our device the non-uniform electric field is created by interdigitated electrodes (IDE) at the bottom of the channel through which the contaminated solution is passed (Figure 1).

To maximize the exposure of particles to the DEP field, we mix the liquid using passive micro-fluidic mixers (Figure 1). Preliminary results with different fabricated micro-fluidic mixers exhibit up to 70% improvement in trapping efficiency as compared to devices without mixers (Figure 2). Although both the herringbone mixer (HM) and slanted groove mixer (SGM) show notable improvements over smooth channel configurations, the staggered herringbone mixer (SHM) provides the greatest enhancement in trapping efficiency. We believe that the chaotic mixing associated solely with the SHM exposes more particles to the concentrator's bank of IDEs, thus resulting in higher trapping efficiency when compared to other mixer types.

The magnitude and direction of the dielectrophoretic (DEP) force depends on the particle's dielectric properties (i.e., conductivity and permittivity); therefore, when the operating frequency of the field and the conductivity of the medium are chosen, the DEP force can be selectively applied to trap and concentrate some particles (bacterial spores of interest) and not others (dust, soot, sand or protein). In our device, initial banks of interdigitated electrodes are driven to maximize interferent trapping, while final stages capture spores from a purified solution. Using this mode of operation, we demonstrated selective trapping of *B. subtilis* spores while rejecting interferents such as pollen, chitin, sand and depleting interferents such as soot and dust. Future work will focus on improving purity and efficiency of trapping.



▲ Figure 1: Overhead and isometric view of the device. A channel molded in poly(dimethylsiloxane) caps a glass wafer lined with gold electrodes. Electrodes create the field that traps particles from flow when sample liquid passes through the channel.



▲ Figure 2: Experimental results of the percentage of beads trapped in the channel with different types of micromixers. By using a staggered herringbone mixer (SHM), we can trap a greater percentage of particles as compared with a plain smooth channel. Other mixers, such as the herringbone mixer (HM) and slanted groove mixer (SGM), give intermediate performance.

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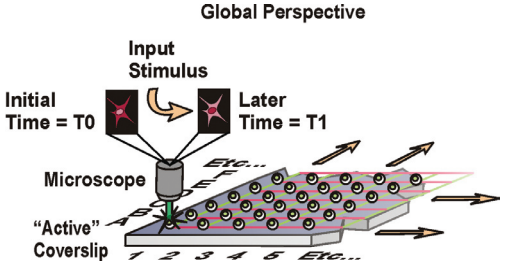
Microfabricated Approaches for Sorting Cells Using Complex Phenotypes

B. Taff, S. Desai, J. Kovac, N. Mittal, J. Voldman
Sponsors: NSF Graduate Research Fellowship, NIH NCRR, Singapore-MIT Alliance

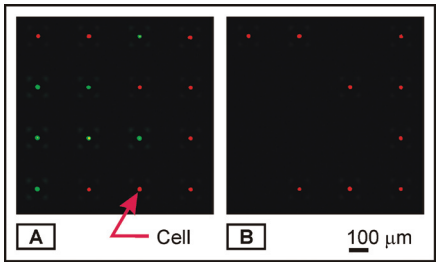
We are developing microfabricated approaches to create sorting cytometers for genetic screening of complex phenotypes in biological cells. Our goal is to create technologies that combine the ability to observe with the ability to isolate individual mutant cells from a population under study. Such cytometry merges benefits of microscopy and flow-assisted cell sorting (FACS) to offer unique capabilities on a single platform. Biologists will be able to use these technologies to isolate cells based upon dynamic and/or intracellular responses, permitting creation of new types of genetic screens.

We currently are developing optical and electrical approaches to enable image-based sorting. One of our current approaches uses an array of switchable traps (Figure 1) that rely upon the phenomena known as dielectrophoresis (DEP) [1]. The DEP-enabled traps allow for capturing and holding cells in defined spatial locations and then subsequently releasing a desired subpopulation for further study. The traps in our device are controlled using a series of row and column electrical connections. This setup avoids any need for separate connections to each of the traps in our arrays. Our chip-to-world interconnect needs thus scale only as $2\sqrt{n}$ for any $n \times n$ trap footprint. This condition enables site-specific addressing within arrays sized appropriately for bio-relevant assays (10,000 sites) using a minimal number of electrical ties (200 wires). To date, we have captured, held, and sorted small populations of individual HL60 human leukemia cells using a demonstrative 4 × 4 trap array [2]. Figure 2 shows a proof-of-concept assay where orange- and green-stained HL60 cells are first held in the 16-site array and then we sorted each of the green cells from the grid.

Developing and scaling such a platform for screening applications requires performance characteristics that are easily met only by using quantitative modeling [3]. Using such an approach, we have developed updated trap geometries and system configurations for use in larger 20 × 20 array structures. Currently we are fabricating these enhanced devices, their affiliated control and automation systems, and specific RFP-tagged cell lines for planned complex phenotype-based sorting assays. In tandem with this design cycle, we are investigating the effects of DEP trapping on cell health and the impact that it may have on our ability to assess specific phenotypic behaviors. Complementary and alternative approaches for implementing these sorting functionalities are similarly under study in an attempt to lower the threshold for acceptance and use in biological laboratories.



▲ Figure 1: A sorting cytometer for screening complex phenotypes. The cytometer consists of a two-dimensional array of traps, each of which holds a single cell. After loading the traps, the array is optically interrogated, and cells with phenotypes of interest are sorted.



▲ Figure 2: Image-based cell sorting. (A) shows an image from an assay where mixtures of orange and green CellTracker-stained HL-60 cells are loaded into a 4 × 4 array. Though the initial placement of the green and orange cells is random in nature, the addressable traps enable selective sorting for all cells of a prescribed color in (B).

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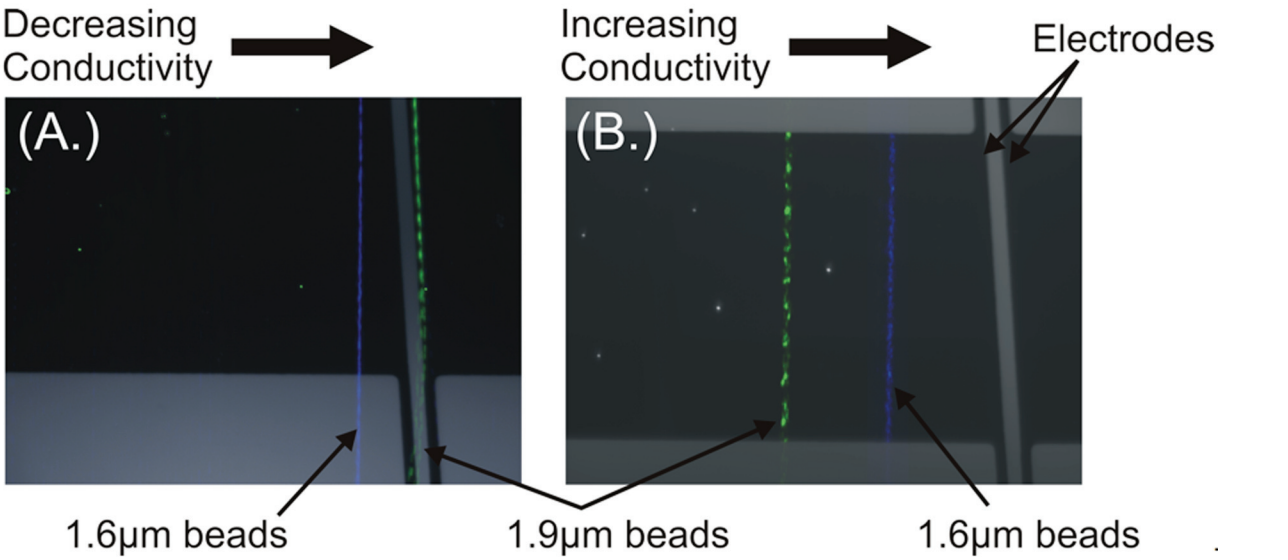
A Continuous, Conductivity-Specific Micro-organism Separator

M.D. Vahey, J. Voldman
Sponsorship: NIH NIBIB, MIT Buschbaum Fund, CSBi/Merck Graduate Fellowship

Increased throughput in the techniques used to engineer new metabolic pathways in unicellular organisms demands similarly high throughput tools for measuring the effects of these pathways on phenotype. For example, the metabolic engineer is often faced with the challenge of selecting the one genomic perturbation that produces a desired result out of tens of thousands of possibilities [1]. We propose a separation method–iso-dielectric separation, or IDS–which separates microorganisms continuously based on their dielectric properties. This technology would enable high-throughput screening of cells based upon electrically distinguishable phenotypes.

Iso-dielectric separation uses dielectrophoresis (DEP) and media with spatially-varying conductivity to separate cells by their effective conductivity. It is similar to iso-electric focusing, except that it uses DEP instead of electrophoresis, and is thus applicable to uncharged particles, such as cells [2]. We apply this method to the separation of polystyrene beads (based on surface conductance), vesicles (based on the conductivity of the internal fluid), and cells (based on viability). Current efforts are focused on the separation of *Escherichia coli* based upon the amount of the intracellular polymer poly(hydroxybutyrate) that each cell contains.



▲ Figure 1: (A) Trial separation of polystyrene beads using nDEP. The smaller, more conductive beads separate out into higher conductivity, as would be expected. The 1.9 μm particles reach their IDP in-frame, where they are seen passing over the electrodes. (B) Using pDEP, the smaller beads still separate into higher conductivity, corresponding to a further displacement (from left to right) to reach the IDP than that for the larger beads.

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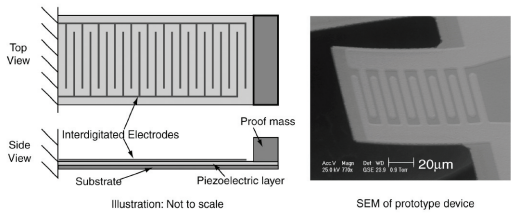
MEMS Vibration Harvesting for Wireless Sensors

A. Mracek, W.S. Kim, Y. Manioulloux, S. Tonn, H. Wong, B.L. Wardle (in collaboration with S.-G. Kim)
Sponsorship: Cambridge-MIT Institute, NSF

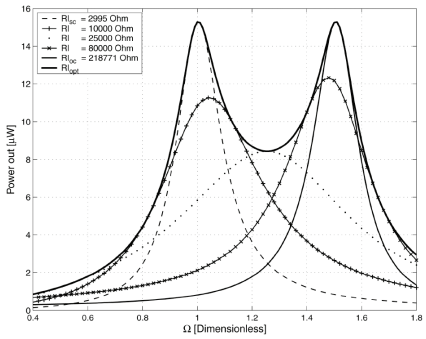
The recent development of "low power" (10's-100's of μW) sensing and data transmission devices, as well as protocols with which to connect them efficiently into large, dispersed networks of individual wireless nodes, has created a need for a new kind of power source. Embeddable, non-life-limiting power sources are being developed to harvest ambient environmental energy available as mechanical vibrations, fluid motion, radiation, or temperature gradients [1]. While potential applications range from building climate control to homeland security, the application pursued most recently has been that of structural health monitoring, particularly for aircraft.

This SHM application and the power levels required favor the piezoelectric harvesting of ambient vibration energy. Current work focuses on harvesting this energy with MEMS resonant structures of various geometries. Coupled electromechanical models for uniform beam structures have been developed to predict the electrical and mechanical performance obtainable from ambient vibration sources. The uniform models have been validated by comparison to prior published results [2] and verified by comparison to tests on a macro-scale device [5]. Models of a uniform harvester with proof mass are currently undergoing macro-scale testing and validation. A non-optimized, uni-morph beam prototype (Figure 1) has been designed and modeled to produce 30 μW/cm^3 [3]. A MEMS fabrication process for a prototype device is presented based on past work at MIT [4]. Dual optimal frequencies with equal peak powers and unequal voltages and currents are characteristic of the response of such coupled devices when operated at optimal load resistances (Figure 2). Design tools to allow device optimization for a given vibration environment have been developed for both geometries.

Future work will focus on fabrication and testing of optimized uni-morph and proof-of-concept bi-morph prototype beams. System integration and development, including modeling the power electronics, will be included.



▲ Figure 1: Illustration of MPVEH unimorph configuration (left) and SEM of a prototype device (right, courtesy of S.-G. Kim).



▲ Figure 2: Power vs. normalized frequency with varying electrical load resistance [3].

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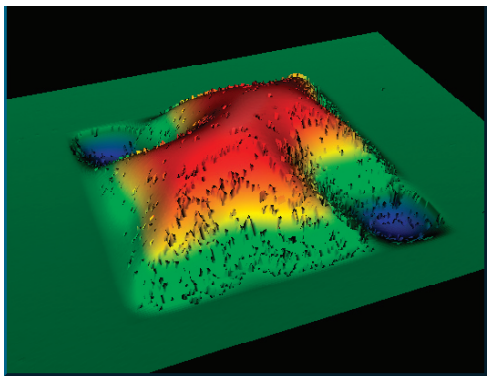
Fabrication and Structural Design of Ultra-thin MEMS Solid Oxide Fuel Cells

N. Yamamoto, D. Quinn, P. Capozzoli, N. Wicks, S. Wicks, S.M. Spearing, B.L. Wardle (in coll. with B.A. Wilhite, J. Hertz, J. Cui, K. Deshpande, K.F. Jensen, H. Tuller, M.A. Schmidt)
Sponsorship: ARO

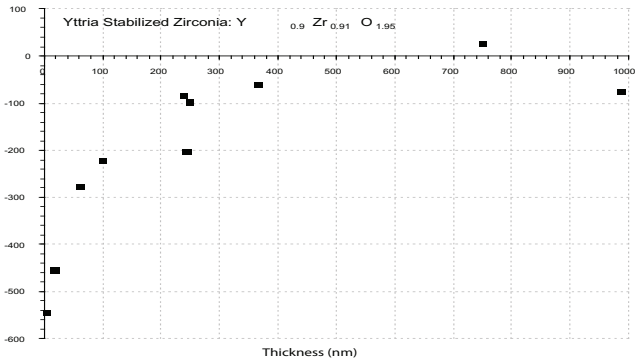
Microfabricated solid oxide fuel cells are being investigated for portable power applications requiring high energy densities [1-2]. Reducing the thickness of the fuel cell stack (anode, electrolyte, and cathode) improves the electrochemical performance over that of traditional devices. This motivation for thinner structures, combined with significant temperature excursions during processing and operation (~600-1000 °C), leads to a major challenge of thermomechanical stability of such membranes. Figure 1 shows a buckled electrolyte/SiN thin film. To predict and control structural stability and failure, the structural characterization of thin films is being investigated.

Our group has characterized the residual stress and microstructure of the electrolyte layer. Complete studies were done on residual stress in sputter-deposited yttria-stabilized zirconia (YSZ) thin films (5 nm-1000 nm thickness) as a function of substrate temperature [3]. The results indicate variations in intrinsic stress from ~-0.5GPa to ~50 MPa as in Figure 2. Changes in microstructure are characterized using x-ray diffraction of as-deposited and annealed films and correlated with relevant mechanisms/ models of residual stress evolution. Based on the design frameworks using the data above, a large-area full fuel cell stack (anode, electrolyte, and cathode) has been fabricated and tested to be thermomechanically stable at high operating temperatures. Tri-layers (Pt-YSZ/YSZ/Pt-YSZ, 50-200-μm wide, each 250-nm-thick) were sputter-deposited at high temperature (500-600C). Devices are being tested for electrochemical performance and power generation. In addition, proton-conducting electrolytes, typically capable of significant power generation at temperatures lower than YSZ are also being investigated in ultra-thin film form. Crack-free barium cerium-yttrium-oxide (BaCeYO) films with uniform thickness (300-500-nm thick) have been successfully sputter-deposited. Electrochemical and residual stress characterization for this material is currently underway.

Additional ongoing work includes bulge-testing to determine the electrolyte's elastic/thermal/fracture properties in ultra-thin membrane form, investigation of the mechanical and chemical properties of anode cathode materials, and nonlinear modeling of film postbuckling and failure.



▲ Figure 1: Postbuckled YSZ/SiN membranes on Si. Displacement contour plot.



▲ Figure 2: The YSZ electrolyte film stress as a function of film thickness.

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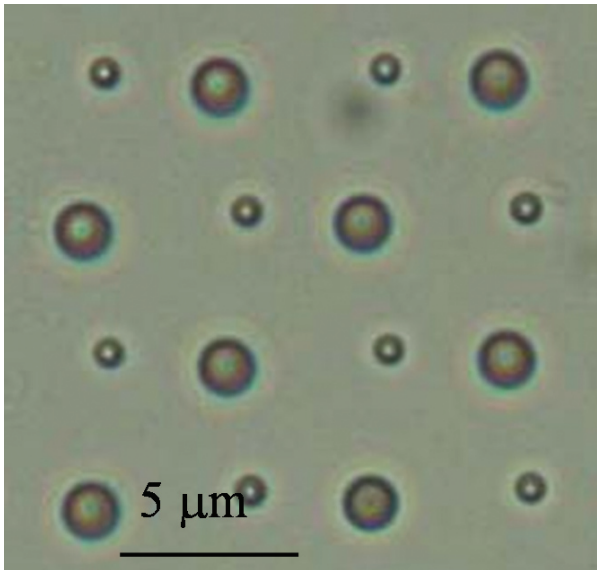
MOLECULAR & NANOTECHNOLOGY



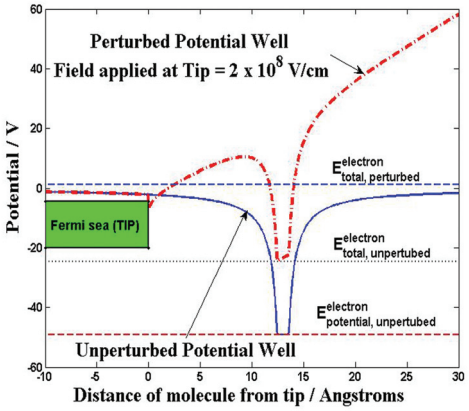
▲ Optical micrograph of 600 nm and 2 μm spheres assembled into designated sites on a surfaces (K.-J. Lee, T.S. Cho, A.P. Chandrakasan, J. Kon, p. 175).

for additional reading…

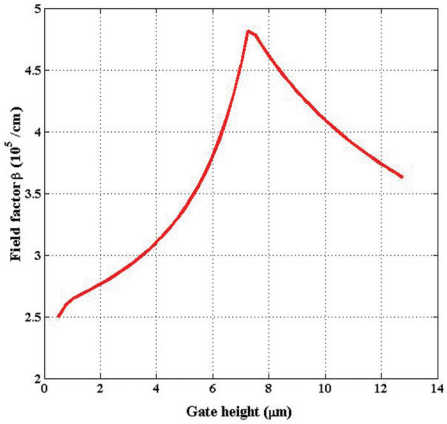
Studies of Field Ionization Using PECVD-grown CNT Tips

B. Adeoti, A.I. Akinwande
Sponsorship: DARPA

The Micro Gas Analyzer project aims to develop the technology for portable, real-time sensors intended for chemical warfare and civilian air-purity control. For the analyzer, we are developing a field ionizer array based on gated CNTs. We plan to use arrays of CNTs because their small tip radii and high aspect ratio yield high fields at low voltage. One possible configuration for the device is to bias the CNTs to the highest potential and the collecting anode to the lowest potential. The electrons in the outer shell of the molecules tunnel out due to the ambient high electric fields, which serve to lower the unperturbed potential barrier seen by the electrons (Figure 1). The tunneling effect is a purely quantum-mechanical process whose probability of occurrence is strongly dependent on the applied electric fields [1]. We optimize the electron current by varying structural parameters in our device. The most relevant parameters include the radius of curvature, height, base radius and base angle of the grown tip; height and thickness of the tip; and the gate aperture. Varying the gate (or oxide) height without updating the height of the CNT yields the derivable result that the electric field is maximized with the tip peaks at about the same height as the gate. When the tip height is varied in sync with the height of the gate (or oxide), we see that an independent optimum height exists (Figure 2). The value of this height will depend, among other variables, on the electrostatic properties of the insulating material and the actual dimensions of the rest of the structure. These simulation results are being verified by experiment.



▲ Figure 1: Representative picture of potential barrier faced by electron in a single molecule when the molecule is close to a tip biased at a high potential.



▲ Figure 2: Field factor ß for various heights of gate. Tip height was varied in sync with gate height so that the tip remained within the range of the gate width. A field ionization configuration was used. [CNT] : roc = 5.01 nm | Base: angle=85 , radius=101 nm [GATE] : Aperture=1.01 µm Thickness=0.301 µm V_{CNT} = 10 V, V_{GATE} = 0 V, V_{ANODE} = -150 V

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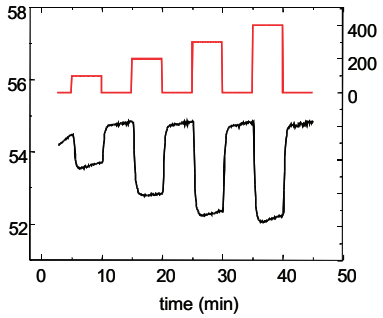
Combinatorial Sensing Arrays of Phthalocyanine-based Field-effect Transistors

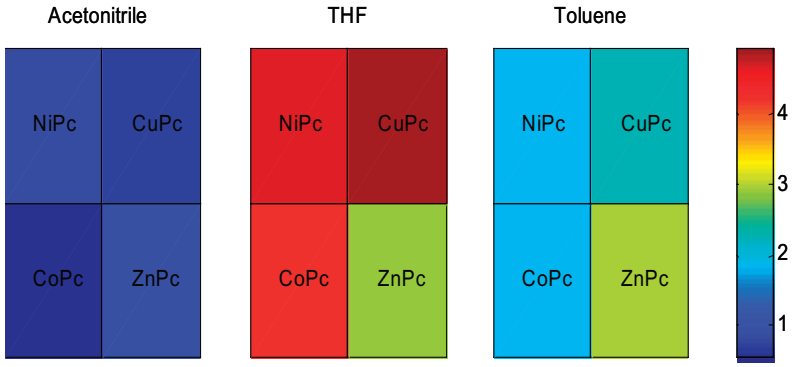
M. Bora, D. Schut (HP), M.A. Baldo

Of the millions of molecular species floating in air or dissolved in water, a substantial fraction can be smelled and uniquely discriminated[1]. Biological systems achieve this functionality with a multitude of non-specific receptors. In this project, we are developing gas sensors based on combinatorial arrays of organic transistors. The combinatorial approach reduces the need to develop specific receptors for each and every molecule of interest. Rather, our sensors are based on exploiting the wide variation in interactions between molecules and metal ions[2], an approach previously employed in colorimetric sensors[3].

We have fabricated gas-sensitive organic transistors each consisting of an approximately 10-nm-thick polycrystalline layer of a metallophthalocyanine (MPC) with gold source and drain contacts. The width and length of the channel for each transistor is 2 mm and 50 μm, respectively. The charge-carrier mobility is typically between 10^{-3} and 10^{-4} cm^2/Vs. But the transconductances of various MPC transistors (CoPC, CuPC, ZnPC, and NiPC) are observed to vary when exposed to different gases (acetonitrile, tetrahydrofuran, and toluene); channel current in MPC transistors decreases linearly with increasing solvent concentration (Figure 1). The transient response of the current modulation (Figure 2) is chemically selective and depends on the interaction between the solvent and the central metal atom in the MPC. The linear dependence of channel current on solvent concentration, the steady state current modulation, and the transient response of the MPC transistors are all consistent with the disruption of percolation pathways leading to modulation of transistor channel currents. Since the sensors can be manufactured simply by inkjet printing on a patterned substrate, they may find application as single-use diagnostic aids.



▲ Figure 1: The linearity of MPC sensors is tested by modulating the solvent concentration (V_{ds}=-20V, V_g=-20 V).



▲ Figure 2: The transient rate of channel current recovery, k_{OFF}, after removal of solvent vapor in units of min^{-1}, summarized for various MPC-solvent combinations. Transistor bias conditions are V_{ds}=-20 V, V_g=-20 V.

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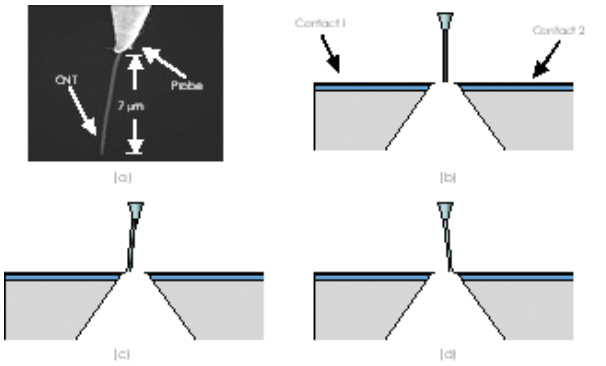
Nanoelectromechanical Switches and Memories

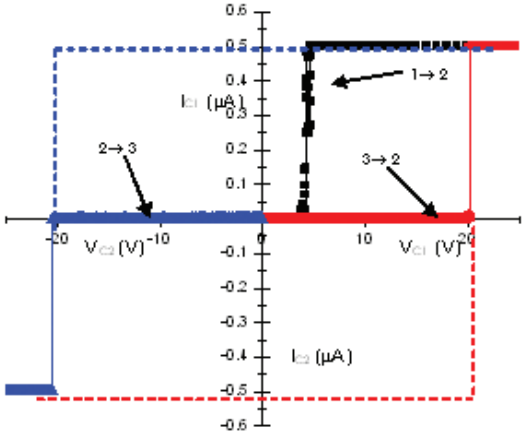
K.M. Milaninia, M.A. Baldo
Sponsorship: MARCO MSD, ISN

The ability to change shape is a compelling attraction of molecular semiconductors. Compared to rigid inorganic materials, molecules are soft and malleable, and their conformational changes are essential to the functionality of biological systems. Applications of nano-electro-mechanical (NEM) molecular devices include memories and transistors. Information can be stored in the conformation of molecules, potentially leading to very high density memories; molecular transistors that change shape under bias could exhibit sub-threshold slopes of << 60 mV/decade[1]. Indeed, as an example of the potential of NEMs, voltage gated ion channels possess subthreshold slopes of approximately 15 mV/decade [2].

Although many materials are available for NEM applications, carbon nanotubes exhibit low resistance and good mechanical properties. In this project, we are constructing a NEM testbed. The proposed design for our relay is shown in Figure 1. Nanotubes are directly grown at the bottom of an electron-beam defined trench etched in Si. This offers better control over nanotube growth and removes the need for additional steps that are required for the removal of surfactants and organics from the surface of the nanotubes. Because the nanotubes are vertically oriented, we are able to take advantage of the smallest size feature of the carbon nanotube - its diameter. This allows us to create dense arrays of relays for applications such as memory or logic devices. The vertical orientation allows NEM structures with very large aspect ratios. Theoretical results[3] have shown that increasing the aspect ratio of a carbon nanotube reduces the voltage needed to pull in the nanotube and thereby reduces the power requirement. Furthermore, because of the ability to easily functionalize the surface of nanotubes, we can functionalize the tube with charge to lower the pull-in voltage even further.



▲ Figure 1: Initial results were obtained by introducing a (a) carbon nanotube mounted to a tungsten probe between two (Au/SiO2/Si) contacts. (b),(c), and (d) are schematics of the device in state 1 (its initial state), state 2, and state 3, respectively.



▲ Figure 2: An I-V of device being switched from state 1→2 by applying a bias between Contact 1 and CNT, then switched from state 2→3 by applying a bias between Contact 2 and CNT, and finally from state 3→2 by applying a bias between Contact 1 and CNT.

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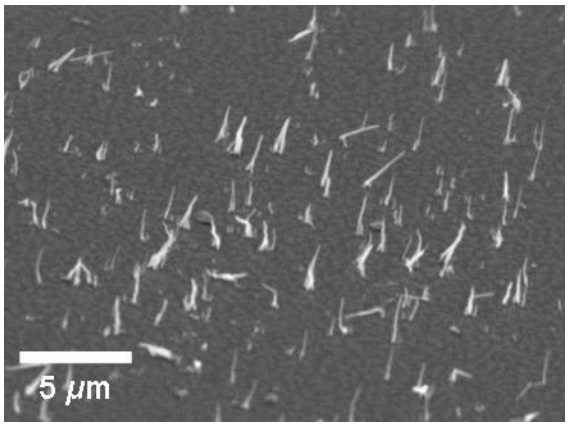
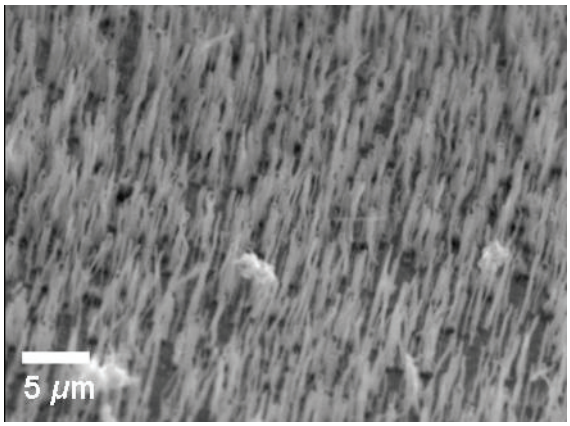
Growth of Carbon Nanotubes for Use in Origami Supercapacitors

H.J. In, S. Kumar, Y. Shao-Horn, G. Barbastathis
Sponsorship: MARCO IFC, ISN, NSF SGER

The Nanostructured Origami™ 3D fabrication and assembly process can be used to create nanostructured, three-dimensional (3D) devices exclusively through existing 2D micro- and nano-fabrication techniques. Previously, the folding method was used in fabricating an origami supercapacitor with carbon electrodes [1]. The carbon electrode material was composed of 99 wt% Super P carbon black and 1 wt% polyvinylidene fluoride binder in N-methyl-2-pyrrolidone. This mixture was highly porous with a very high specific surface area and resulted in microscale supercapacitors with a high specific capacitance. However, the material had to be deposited manually using a probe tip, and its exact properties, e.g., surface area and variations in pore size could not be determined precisely. To enable *in situ* deposition of the electrode material, multi-walled carbon nanotubes (CNTs) were grown through a plasma-enhanced chemical-vapor deposition (PECVD) method in place of the manually deposited carbon paint. Moreover, as Figures 1 and 2 partially illustrate, growth conditions of the nanotubes determine their density, length, diameter, etc. Being able to control the nanotube properties will allow us to more carefully characterize the electrochemical properties of the origami supercapacitors. All nanotubes were grown using S. Kim group's PECVD CNT deposition equipment.



▲ Figure 1: Low-density growth of carbon nanotubes. Each tube is approximately 2 microns long.



▲ Figure 2: High-density growth of carbon nanotubes.

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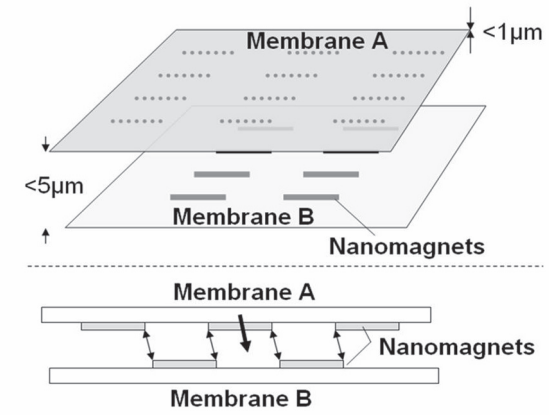
Self-Alignment of Folded, Thin-Membranes via Nanomagnet Attractive Forces

A. Nichol, W.J. Arora, F.J. Castaño, G. Barbastathis
Sponsorship: ISN, MARCO IFC

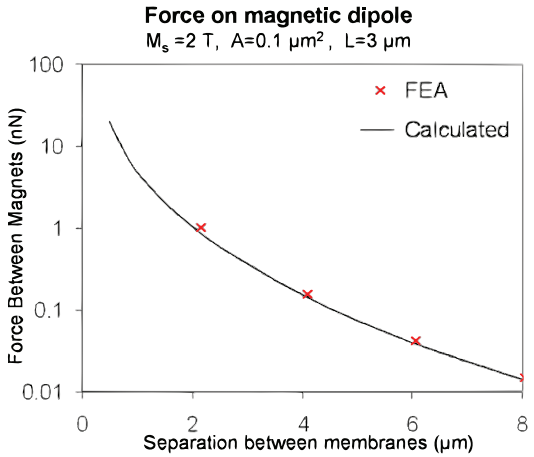
We are developing a thin-membrane self-alignment technique based on the attractive force between arrays of nano-patterned magnetic material (nanomagnets). The alignment scheme shown in Figure 1 will be applied in the Nanostructured Origami™ fabrication method [1], which involves first nano-patterning membranes using 2D lithography and then folding the membranes in a 3D configuration. We have shown that the scaling of the attractive force between magnets is favorable for this application. The research is moving towards a completely self-assembling, 3D nanofabrication method with better than 50-nm accuracy of feature placement for use in 3D photonics, 3D integrated circuits, and other 3D hybrid devices.

Nanomagnets with preferred magnetization in-plane can be patterned on thin-membranes with nano-scale precision using e-beam lithography, e-beam evaporation for the metallization steps, and liftoff processing. The alignment system uses a large array of nanomagnets to increase force and to average out the local errors in magnetic pole positions. A dynamic model of the system has shown a significant dependency on the number of magnets for the precision of the final alignment.

The magnetic alignment scheme is most effective when the folding takes place in an external magnetic field that holds a common magnetization direction for the nanomagnets. The addition of an external field allows the use of soft magnetic material operating at saturation. This reduces processing constraints because hard permanent nanomagnets at this scale are more difficult to fabricate than soft magnets. Furthermore, the torque due to the external field provides alignment about two axes of rotation. Using a dipole approximation along with finite element magnetic modeling (FEMM) [2], we have determined the alignment forces that can be achieved with this method. A plot of the forces between two 100 nm x 1 µm x 3 µm saturated iron nanomagnets appears in Figure 2. We are characterizing the alignment force experimentally using sensitive 300 nm-thick silicon nitride flexures that have been e-beam-patterned with iron nanomagnets.



▲ Figure 1: Schematic of the alignment system of nanomagnets. The two membranes are patterned with magnetic material that is magnetized in-plane by using an external magnetic field. When the coarse alignment brings them close enough, self-alignment occurs.



▲ Figure 2: The force exerted on a single 100 nm x 1 µm x 3 µm magnetically saturated iron nanomagnet by similarly-sized magnets on the other membrane. The force is highly dependent on the separation between the membranes.

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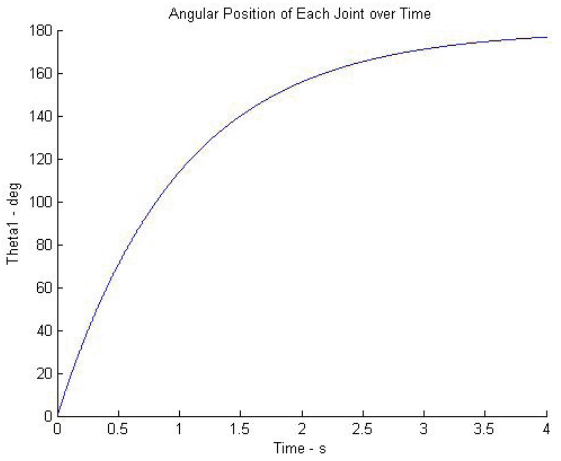
Control System Design for the Nanostructured Origami™ 3D Nanofabrication Process

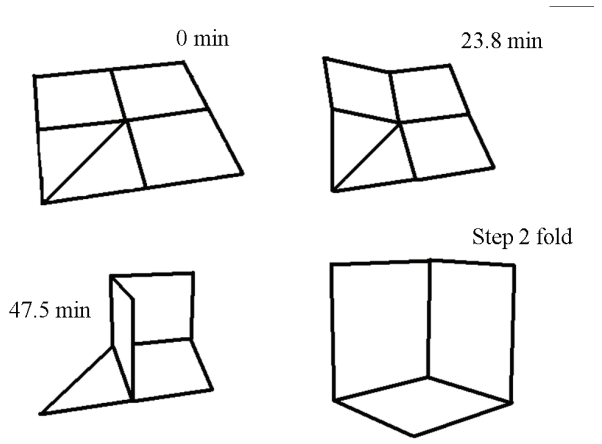
P. Stellman, G. Barbastathis
Sponsorship: NSF, MARCO IFC, ISN

Nanostructured Origami™ is the 3D nanomanufacturing process that folds patterned membranes into useful 3D structures. Since the origami segments must be accurately aligned in the 3D folded state, the actuation mechanisms for Nanostructured Origami must be both controllable and repeatable. Accurate analytical models of the actuation are therefore necessary to expedite the design of complex origamis. We borrow techniques from the robotics community to simulate the motion of the origami as it folds from 2D to its 3D shape. The dynamics of the folding process are computed using wrench calculus [1] and are used to design a control scheme for folding the segments in the laboratory. A PD position control scheme is briefly described here.

To date, we have modeled the dynamics of two classes of origamis: accordions and single-vertex origamis [2]. In this abstract, we describe the analysis of a single-vertex origami referred to as the corner cube. The creases are modeled as revolute joints, which represent the generalized coordinates of the systems. The segments of the origami are assumed to remain rigid throughout the origami's motion. This allows us to use screw calculus [1] to describe the geometry and kinematics of the corner cube. Since the corner cube has a closed chain kinematic topology, the motion of the segments is interdependent. The dependencies are manifested through holonomic equality constraints. The corner cube is then virtually cut at an unactuated joint, and the dynamics of the resulting one degree-of-freedom system are computed. The equations of motion of the system are then formed according to the principles outlined in [1]. These nonlinear equations can be integrated in time to simulate the trajectory of the origamis. The dynamic response of the corner cube subject to a PD controller is shown in Figure 1, and its trajectory is illustrated in Figure 2. The final folded state of the corner cube is also guaranteed to be stable for a stress actuation method since the stiffness matrix is positive definite.



▲ Figure 1: Dynamic response of driving joint of corner cube when subject to an input torque following the PD control law.



▲ Figure 2: Trajectory of corner cube as it folds from the flat to the folded state.

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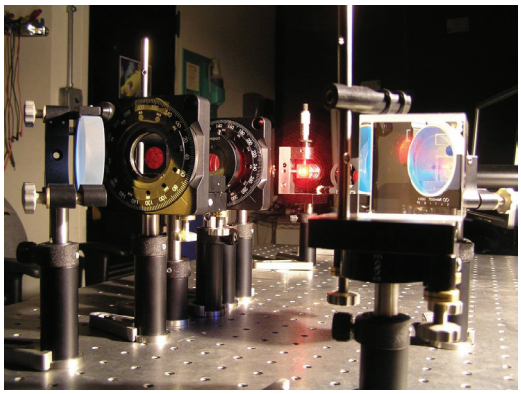
Tomographic Interferometry for Detection of Nafion® Membrane Degradation in PEM Fuel Cells

L. Waller, J. Kim, G. Barbastathis, Y. Shao-Horn
Sponsorship: DuPont-MIT Alliance

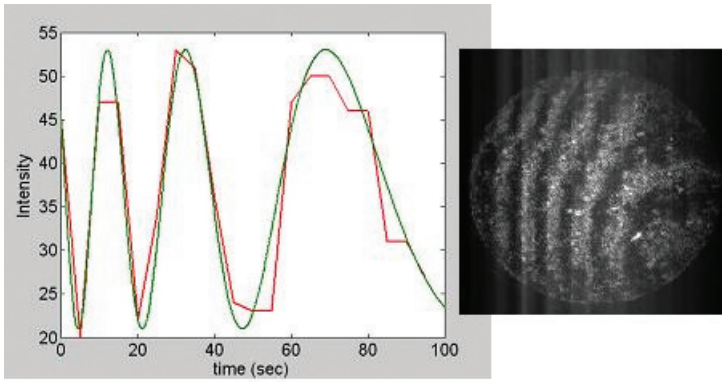
At present, membrane degradation and failure are the main limitations on the lifetime of proton exchange membrane (PEM) fuel cell systems [1]. Nafion® membranes, produced by DuPont, have excellent proton conductivity and relatively good chemical stability. However, fundamental studies of the degradation mechanisms of Nafion membranes are needed in order to optimize membrane design. Our goal is to correlate indirect and *ex-situ* measurements with *in situ* monitoring of membrane microstructural changes in order to better understand how the membrane thins or forms pinholes and voids.

We are conducting atomic force microscopy (AFM) studies of both fresh and degraded *ex-situ* Nafion samples to study the changes in the microstructure of the Nafion as it degrades. These studies will be used to guide optical characterization of the Nafion® membrane *in situ*. The goal of the *in situ* optical studies is to construct a refractive index profile of the membrane while the fuel cell is in use. We place the fuel cell system inside one leg of a Mach-Zehnder interferometer (Figure 1). The membrane, which has an average refractive index of 1.35 (room temperature, 20%RH) [2], will act as a phase object, and the phase delay at any point in the x-y plane is proportional to the refractive index at that point. Thus, a 2D map of the refractive index in the membrane can be constructed from the interference pattern, which is recorded on a CCD camera (Figure 2). The refractive index is related to membrane density at each point by the Lorentz-Lorentz relation. We focus on density changes due to temperature, pressure, and humidity, which occur on different orders of magnitude. Simulations are used to solve the forward problem through the optical system and to compute the inverse problem, which can then be used to estimate the refractive-index profile of the membrane from the measured interference pattern.

In situ profiling of the Nafion membrane will allow us to observe exactly where and how the membrane degrades. Our approach is non-invasive and provides a 2D distribution of water uptake, stresses, and micropores in the membrane. The technique can be extended to 3D with tomographic techniques. A better understanding of the mechanisms of membrane failure will give insight into membrane and fuel cell design.



▲ Figure 1: Experimental set-up of PEM fuel cell within a Mach-Zehnder interferometer. Fringe patterns yield a map of the refractive index of the fuel cell membrane.



▲ Figure 2: Measured fringe pattern (right) and the corresponding intensity vs. time plot for several specific points (left) for a Nafion® membrane as it cools. Chirped sinusoid is a result of decreasing temperature.

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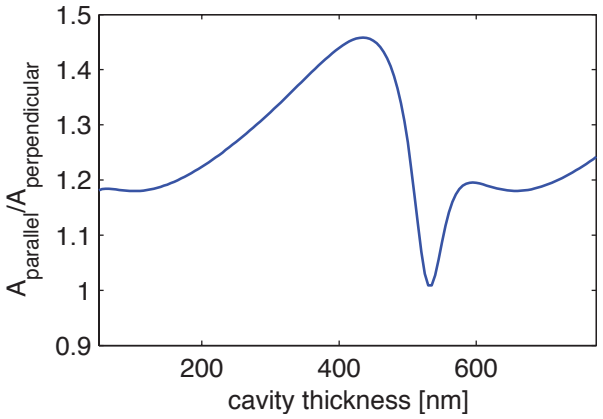
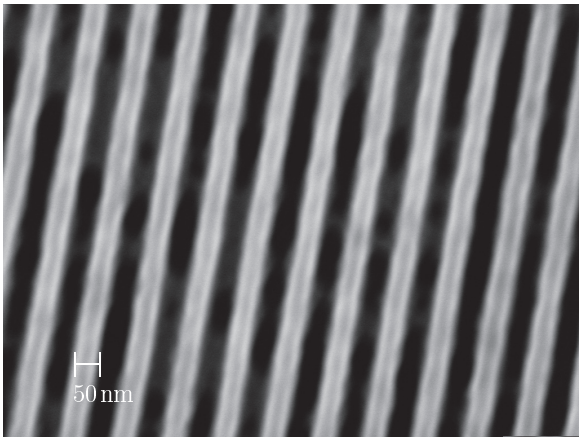
Modelling the Optical Properties of Superconducting Nanowire Single-photon Detectors

V. Anant, A.J. Kerman, J.K. Yang, E.A. Dauler, K.M. Rosfjord, K.K. Berggren
Sponsorship: United States Air Force

Polarization-sensitive single-photon detectors can be useful for high-speed optical and quantum communication where one can encode information in the polarization of the photon. We have observed that superconducting nanowire single-photon detectors (SNSPD) fabricated at MIT exhibit sensitivity to polarization. For this project, we will investigate the polarization sensitivity for devices with various geometries and conduct numerical simulations that explain the sensitivity. Our SNSPDs consist of a nanowire in a meandering pattern that acts as an optical wire-grid polarizer. In order to corroborate our model with experimental results, we approximated the meander geometry with wire arrays characterized by two parameters: pitch (periodicity) and fill-factor (the ratio of wire-width to pitch). We conducted finite-element-method (FEM) simulations of the absorptance of polarized radiation to wire grids. The simulations show that meanders with small pitch and small fill-factors will exhibit larger sensitivity to photon polarization than meanders with large pitch and fill-factors. We intend to use our results to design SNSPDs that are optimized for enhanced sensitivity to polarization. The FEM simulations also show this sensitivity of SNSPDs with integrated optical cavities that have been reported to exhibit detection efficiencies of 57% at 1550 nm wavelength and 67% at 1064 nm [1].



▲ Figure 1: Plot showing the expected ratio of absoptances for electric fields polarized parallel and perpendicular to the nanowires as a function of cavity thickness for a SNSPD with an integrated optical cavity. The nanowire detector is modelled as an array of 100-nm-wide parallel wires at a 200 nm pitch. The material set and relavent optical constants are given in [1].



▲ Figure 2: Scanning electron micrograph of a microfabricated structure on a sapphire substrate. The structure is composed of 50-nm-wide wires at a pitch of 100 nm. After the underlying NbN is etched, this structure (and others with different fill-factors and wire widths) can be used to measure the dependence of polarization on absorptance.

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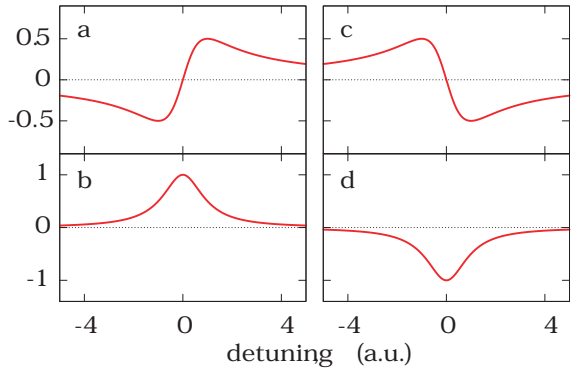
Using Optical Mixtures of Materials to Control Index, Speed of Light, and Transparency

V. Anant, A.F. Abouraddy, K.K. Berggren
Sponsorship: United States Air Force

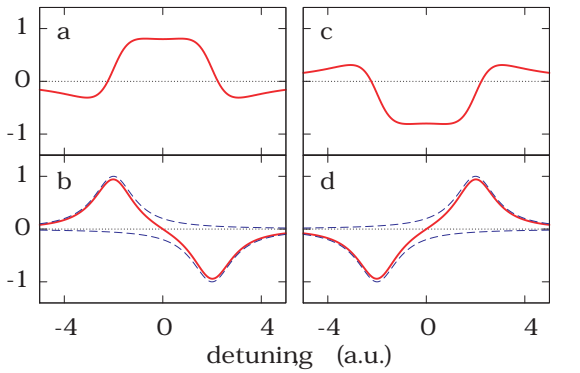
Recent achievements in optical physics have dramatically redefined the limits of attainable optical properties in materials. Novel optical phenomena, including electromagnetically induced transparency [1], slow light [2], and superluminal speed [3] have been demonstrated in diverse physical implementations. Building on our previous work [4], we have developed a unified approach to engineering optical materials that exhibit these phenomena by using mixtures of simple optical materials near resonances. In addition, this approach can be used to realize large and small (much less than 1) indices of refraction and negative permittivity ($\varepsilon < 0$), all while maintaining transparency and without relying on quantum coherence.

Previous work in this field has largely been associated with exploiting quantum-optical effects in a single carefully chosen atomic species. In many cases the complexities of this implementation has prevented further application of these effects. Additionally, the strong association with quantum-coherence has suggested that these optical effects are somehow achievable only using multi-level atomic interactions. Finally, the lack of robustness of these methods has meant that, while these effects may be interesting, they are of little practical utility to robust, real-world devices.

All of the interesting optical effects mentioned above can be produced using a simple mixture of materials composed of population-inverted ("active") and conventional ("passive") resonances. By using the fact that an incoherent mixture of materials with different optical properties exhibits an optical characteristic that is a superposition of the characteristics of its components, we propose materials that exhibit a number of optical effects, e.g., large refractive index or a large change in index with respect to frequency, without absorption or amplification. Additionally, this approach is independent of the underlying physical origin of the resonances in the system, so may be applied in a variety of atomic, optical, and nonlinear optical systems.



▲ Figure 1: Plot of real (χ') and imaginary (χ'') components of susceptibility as a function of detuning frequency, Δ for active and passive resonances. Plots (a) and (b) are spectra for a passive resonance, while (c) and (d) show an active resonance.



▲ Figure 2: Plot of real (χ') and imaginary (χ'') components of susceptibility as a function of detuning frequency for mixtures of active and passive resonances shown in Figure 1. Plots (a) and (b) depict a material with an equal mixture of passive and active resonances chosen so that one gets a positive χ', zero $d\chi'/d\omega$, accompanied with transparency ($\chi''=0$). Plots (c) and (d) depict a material where $\chi' < 0$ and $d\chi'/d\omega = 0$ at the transparency point. The dashed lines in (b) and (d) show χ'' for the constituent active and passive resonances.

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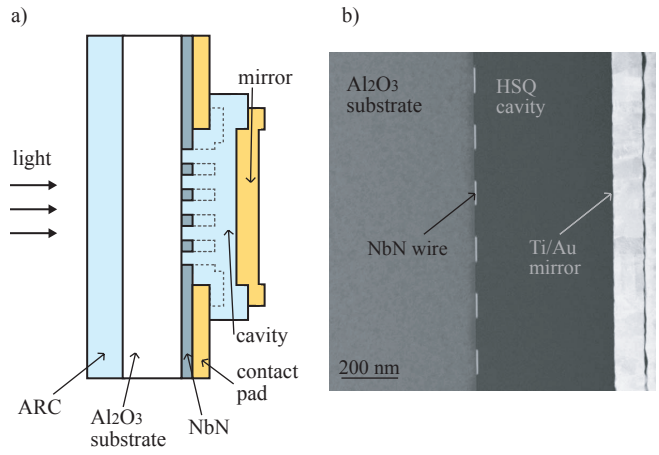
Increasing Detection Efficiency of Superconducting Nanowire Single-photon Detectors

K.M. Rosfjord, J.K.W. Yang, E.A. Dauler, A.J. Kerman, V. Anant, K.K. Berggren
Sponsorship: United States Air Force

Superconducting NbN-nanowire single-photon detectors (SNSPDs) [1] are an enabling technology for high-performance single-photon optical systems. Examples of these systems include ultra-long range communications [2], integrated circuit testing [3] and quantum cryptography [4]. These systems require the detectors to have high detection efficiency and photon-counting rates, and low dark-count rates and jitter. This work has aimed to increase the detection efficiency of SNSPDs.

The SNSPDs are limited in their efficiency of detection due to transmission through and reflection from the device. To combat these losses we integrated optical enhancements in the form of an anti-reflection coating and optical cavity. These enhancements enabled us to achieve a detection efficiency of 57% at 1550 nm wavelength [5]. This detection efficiency contrasts with previously reported detection efficiencies of 17% at 1550 nm wavelength [6]. A schematic cross-section and transmission electron micrograph of the detector integrated with an optical cavity are shown in Figure 1.

The SNSPDs are also limited in their efficiency of detection by the dimensions of the nanowire they employ. We are currently developing a process, utilizing slant evaporation, which will enable us to lower the width of the nanowire and increase the fill factor of the meander. By changing these physical properties of the meander and coupling this process with our now established optical enhancements, we aim to again increase the detection efficiency of these devices.



◀ Figure 1: a) Schematic cross-section of photodetector (not to scale) integrated with an optical cavity and anti-reflection coating to reduce loss of photons from reflection and transmission. b) Transmission electron micrograph of cross-section of fabricated device with optical cavity. The cavity shown here was fabricated for calibration purposes and was thicker than those used to increase the detection efficiency.

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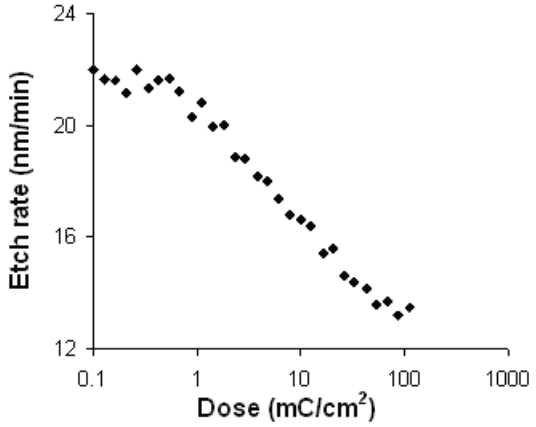
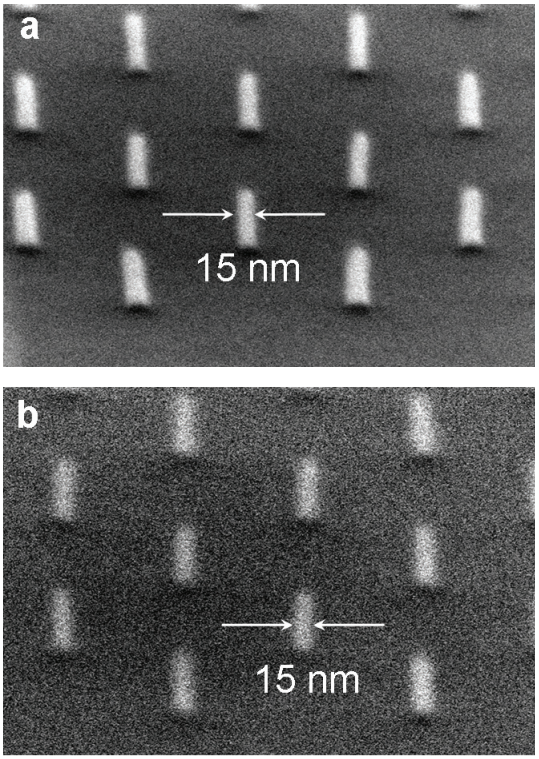
Enhancing Etch Resistance of Nanostructured Spin-on-Glass Electron Resist via Post-Develop Electron Curing

J.K.W. Yang, V. Anant, K.K. Berggren
Sponsorship: Lincoln Laboratory

Hydrogen silsesquioxane (HSQ) has been used recently as a high-resolution, negative-tone, electron-beam resist[1]. Although HSQ is a good etch mask in chlorine reactive-ion etching (RIE), its poor etch resistance in fluorine RIE makes it undesirable as a mask for etching materials that etch only in fluorine. In this work, we increased the etch-resistance of hydrogen silsesquioxane (HSQ) in CF_4 chemistry via electron-beam curing at high doses. We observed a decrease in the HSQ etch rate by as much as 40% after resist exposure to electron doses of 85 mC/cm^2 (Figure 1). This property of the resist was exploited to fabricate 15-nm-wide superconducting NbN nanowires. We achieved this result by subjecting HSQ to an exposure-develop-exposure step prior to pattern transfer into NbN. The first electron beam exposure defined the nanowires at doses of ~400 μC/cm^2. This step was followed by resist development in Shipley Microposit MF CD-26, resulting in 15-nm-wide HSQ structures. The nanostructures were then re-exposed at 50 mC/cm^2 before RIE to toughen the resist, which would otherwise not survive the etch. Electron exposures were performed at 30-kV acceleration voltage using a Raith 150 electron-beam lithography tool. We demonstrated that the second electron exposure does not decrease the resolution of the nanostructures by comparing images of 15-nm-diameter HSQ nano-pillars before and after re-exposure (Figure 2). This process will enable nanofabrication with thinner resist, therefore avoiding problems such as resist collapse and reduced resolution that are associated with thicker resist layers.



▲ Figure 1: Plot of HSQ etch rate with respect to electron exposure dose. We successfully decreased the etch rate of HSQ by exposing the resist to high doses of electrons. Reactive-ion etch (RIE) conditions were 100-W rf power, 15-V DC self-bias potential, and 15 mT with 15 sccm CF_4.



▲ Figure 2: Scanning electron micrograph (SEM) images of HSQ nano-pillars arranged in a hexagonal close-packed structure on Si substrate before (a) and after (b) curing with 50-mC/cm^2 electron dose. There was no observable degradation in the resist shape or dimension due to the second exposure at these dimensions.

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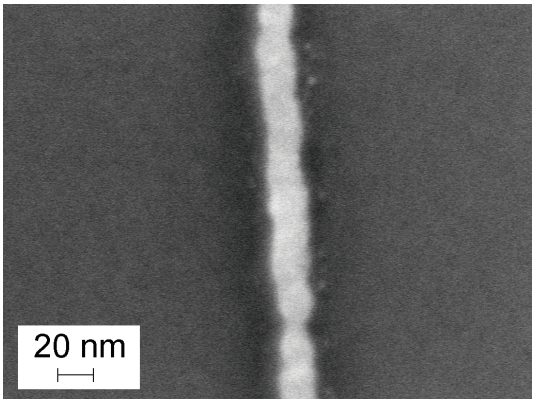
Robust Shadow-Mask Evaporation via Lithography-Controlled Undercut

B. Cord, C. Dames, J. Aumentado (NIST), K.K. Berggren
Sponsorship: QuaCGR Fellowship, AFOSR

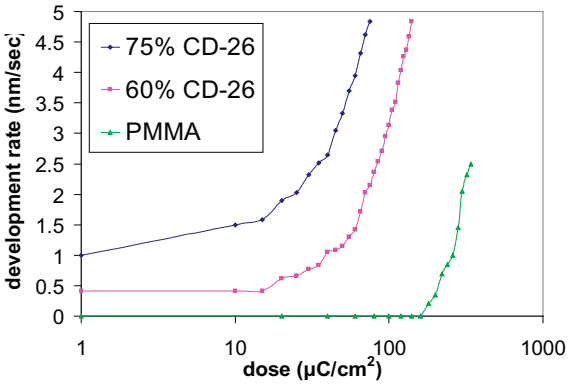
Suspended shadow-mask evaporation is a simple, robust technique for fabricating Josephson junctions using electron-beam lithography. The basic process entails the fabrication of an undercut structure in a resist bilayer to form a suspended "bridge," followed by two angle evaporations of superconducting material with a brief oxidation step in between, resulting in two overlapping wires separated by a thin oxide layer. Josephson junctions with sub-20-nm diameters are of particular interest in a variety of superconductive devices, including quantum bits. Unfortunately, standard shadow-mask fabrication techniques are unreliable at line widths below 100 nm.

While most previous processes used PMMA for the top (imaging) layer and a PMMA/MAA copolymer for the bottom (support) layer, our process uses a PMMA/PMGI bilayer. This resist system allows the two layers to be developed separately, ensuring that the imaging layer is not biased during development of the undercut and allowing the process to achieve the full resolution of the PMMA layer. Additionally, the extent of the undercut in the support layer can be precisely controlled by defining it lithographically, making it possible to repeatedly fabricate undercut regions as large as 600 nm.

Extensive modeling of both the exposure and development processes was used to verify our results. Using Monte Carlo and mass transfer simulations, we produced a model that closely matches experimental data. With the process fully characterized, it is possible to produce a wide range of line width/undercut combinations. This robustness, combined with the high resolution of PMMA, will allow the reliable fabrication of sub-20-nm Josephson junctions.



▲ Figure 1: Scanning electron micrograph of a 16-nm-wide, 10-nm-thick evaporated titanium-gold line fabricated using the PMMA/PMGI process.

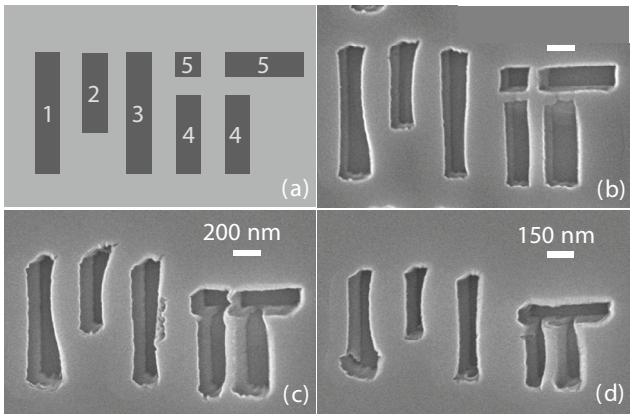


▲ Figure 2: Contrast curve plots for PMGI using two different dilutions of CD-26 developer. Contrast data for PMMA developed in a 3:1 IPA:MIBK solution is shown for reference.

Pattern Generation Using Multi-Step Room-Temperature Nanoimprint Lithography

S. Harrer (Technische Universität München, Munich, Germany), J.K.W. Yang, F. Ilievski, C.A. Ross, K.K. Berggren
Sponsorship: AFOSR, Karl Chang Innovation Fund at MIT

We have demonstrated multi-step room-temperature nanoimprint lithography (RTNIL) using polystyrene (PS, average molecular weight 97 kg/mol) as the polymer layer for imprinting complex patterns. Our motivation in pursuing multi-step RTNIL is to create a new pattern-generation method, able to create complex and arbitrary patterns without requiring a custom template for each new pattern. A variety of different forms of NIL have been demonstrated in the past: thermal NIL [1], UV-cured NIL [2], and room-temperature NIL (RTNIL) [3-6]. All of these existing techniques focus on pattern replication using one, or at most two, imprint steps. In our approach, the extent of each of the starting templates is only a fraction of the extent of the desired final pattern (i.e., each template is much smaller than the final pattern). In separate experiments, single, double, and multiple (up to 10) sequential imprint steps were performed at imprint pressures between 3 to 30 MPa. To accomplish this demonstration, we designed and built a tool that controllably and repeatedly translated and pressed a sample into a stationary mold. The demonstrated inter-step alignment accuracy of this tool was ~ 500 nm. To illustrate this capability, we imprinted the letters "MIT" by using ten sequential imprint steps, translating the sample a programmable distance along a single direction in between steps (Figure 1). The molds used in these experiments consisted of rectangular structures of varying aspect ratios, ranging from 150 to 300 nm wide. Before this technique can be used as it is ultimately intended, as a method for the generation of complex patterns across a wide variety of length scales using only a simple set of generic template structures, the imprint polymer distortion and deformation must be minimized and inter-step alignment must be optimized. However, the work suggests that RTNIL may be a useful pattern-generation tool. This development can be thought of as analogous to the development of the typewriter after the printing press. While a printing press can replicate large-scale molds (entire pages of books) at high rates, in the typewriter, the smallest mold unit was a single letter. The typewriter sacrificed throughput in return for flexibility and low cost. Similarly, by removing the difficult and slow step of custom-template manufacturing from the process, our work represents a shift in the way some nanoimprint work might be performed in the future.



◀ Figure 1: Results of a 10-step RTNIL imprint cycle for different mold dimensions: (a) graphical representation of desired final pattern to be printed out. The numbers indicate the order in which parts of the final pattern are imprinted. After the 5th imprint step the pattern is complete; steps 6-10 create further identical patterns, yielding a total number of 6 completed patterns after the 10th imprint step. We performed several 10-step RTNIL cycles using molds with different feature sizes: The linewidth of the imprinted pattern in (b) is 300nm, the linewidth in (c) is 200 nm, and (d) shows an imprint result for a pattern composing a linewidth of 150 nm. The observed vertical and horizontal misalignment was ~ 500 nm.

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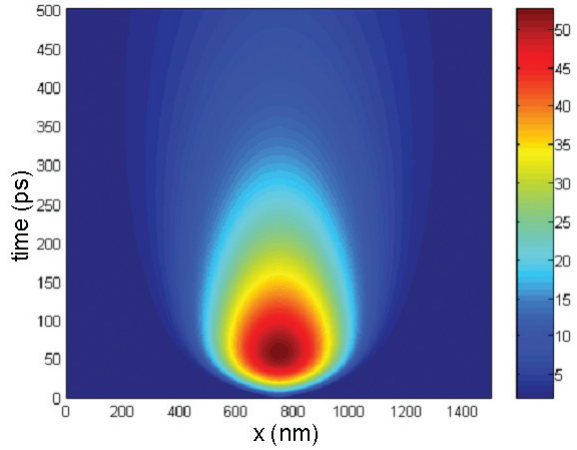
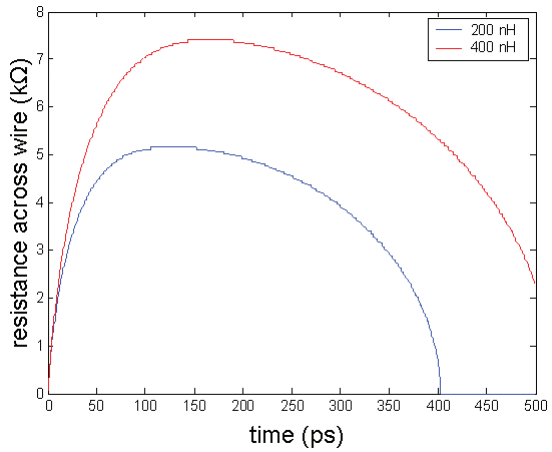
Modeling of Electrical and Thermal Response of Superconducting Nanowire Single Photon Detectors (SNSPD)

J.K. Yang, K.K. Berggren
Sponsorship: Lincoln Laboratory

The response time of superconducting nanowire single-photon detectors (SNSPD) is in the order of several nanoseconds [1-2]. This detector works by the formation of a photon-induced resistive barrier across a superconducting nanowire that is biased close to its critical current. Detected photons result in measurable voltage pulses with very fast rise times and a slower decay. We modeled the full electrical and thermal response of a NbN SNSPD to the absorption of a single photon. The thermal response was modeled by a one-dimensional, time-dependent heat equation incorporating power dissipated by Joule heating in the resistive segment of the wire and heat conduction along the wire and into a sapphire substrate. The electrical model consists of the SNSPD, modeled as an inductor in series with a time-varying resistor shunted by a 50 ohm transmission line and a current bias. This model predicts the growth of the normal region leading to the increase in the total electrical resistance with time as more of the wire heats up and switches into the normal state as shown in Figure 1. However, the resistance does not build up indefinitely since the current flowing through the wire drops as it is diverted into the transmission line once resistance develops in the wire as shown in Figure 2. The model will also enable us to predict performances of devices made of different materials.



▲ Figure 1: Plot of simulation data showing the temperature evolution in a short segment (1.5 μm) of a longer nanowire (with a total kinetic inductance of 200 nH) after a photon-induced resistive barrier forms across the nanowire at t = 0, x = 750 nm. Temperature information is depicted in the color with a corresponding color-map shown on the right in units of Kelvin. The temperature increases quickly and reaches a maximum at about ~50 ps after photon absorption.



▲ Figure 2: Plot of simulation data showing the total resistance built up across a superconducting nanowire after the formation of a resistive barrier for wires of different total kinetic inductances.

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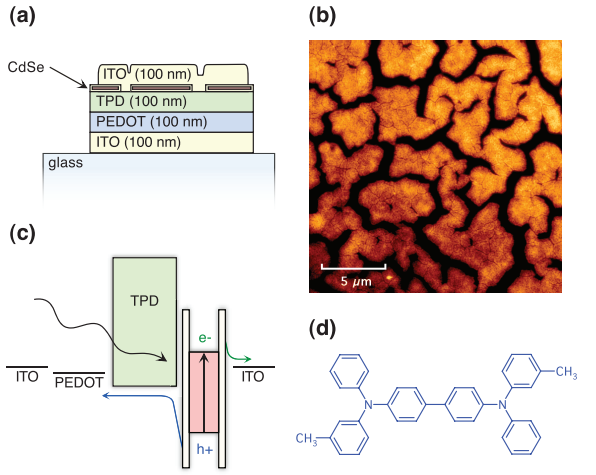
Quantum Dot Photodetectors Deposited via Microcontact Printing

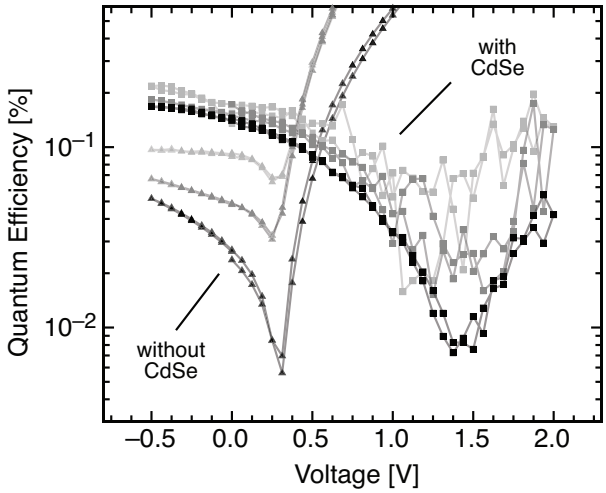
A.C. Arango, D.C. Oertel, M.G. Bawendi, V. Bulović
Sponsorship: ISN

Solution processable colloidal quantum dot systems exhibit many of the special optical and electronic properties associated with epitaxially grown quantum confined systems. Their tunable band gap and higher absorption relative to the bulk make quantum dots particularly attractive as photogeneration materials. At the same time, colloidal quantum dots offer greater material system flexibility than epitaxial quantum dots because deposition on any substrate is possible. The prevailing deposition method, however, is spin casting [1], which introduces limitations such as solvent incompatibility with underlying films and the inability to pattern side-by-side pixels for multispectral photodetector arrays. We employ a non-destructive microcontact printing method that allows for deposition of a thin (20 nm) quantum dot film onto a wide band gap organic hole transport layer, N,N'-bis-(3-methylphenyl)-N,N'-bis-(phenyl)-benzidine (TPD), thus producing an inorganic/organic heterojunction which serves to enhance charge separation in the device. The use of ITO electrodes provides the top and bottom contacts, allowing for near-transparency.

Current-voltage characteristics show low dark currents in reverse bias and good rectification. Excitation of the quantum dots yields a strong, saturated photoresponse; open circuit voltages of +0.5V; and a fill factor of 0.4. Measurement of the locked-in photocurrent under bias reveals a strong photocurrent signal extending out to +1.4V (Figure 2), in excess of the built-in acceptor-donor energy level offset of approximately 0.8V. We attribute the photocurrent voltage dependence to efficient charge extraction and low recombination rates at the heterojunction and top ITO contact. Changing the size and material properties of the quantum dots can tune the response spectrum of the device across the visible and near infrared spectrum. The present focus is on improving the device performance and optimizing the photodetection response in the 1 μm to 2 μm wavelength region by using different quantum dot film chemistries.



▲ Figure 1: Schematic of photodetector device structure (a). An AFM of the surface of the printed quantum-dot film demonstrates that the film is not continuous (b). The energy band diagram (c) illustrates the photogeneration process. The molecular structure of the hole- transport material, TPD, is shown in (d).



▲ Figure 2: Plot of the quantum efficiency versus applied bias for the photodetector and a control device without quantum dots. The CdSe device is measured with a 532-nm laser at 2, 20 and 200 uW/cm2 (light grey, grey, and black squares, respectively). The TPD control device is measured at 408 nm at 2, 20 and 200 uW/cm2 (light grey, grey, and black triangles, respectively).

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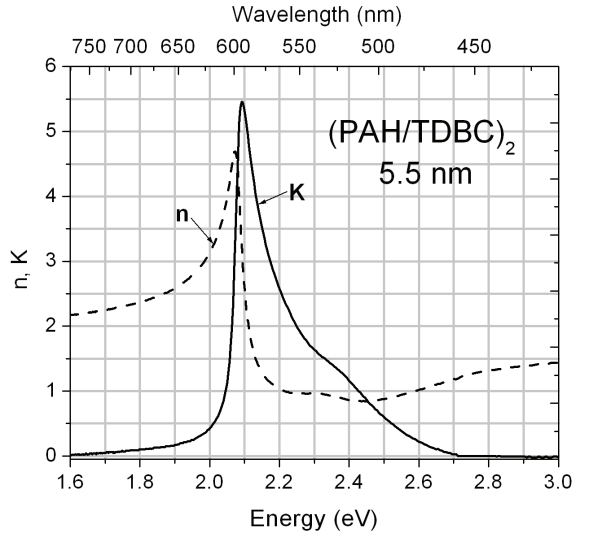
Microcontact Printing of J-Aggregate Thin Films for Photonic Devices

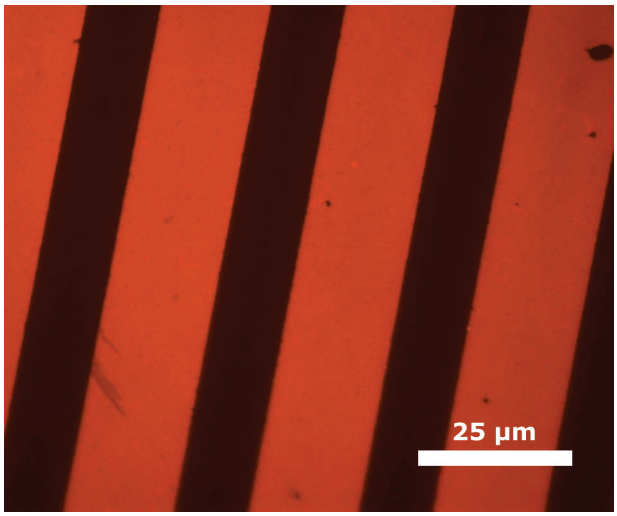
M.S. Bradley, J.R. Tischler, V. Bulović
Sponsorship: DARPA, NDSEG, MIT NSF MRSEC

Thin-film J-aggregates of cyanine dyes enable the observation of strong coupling between light and matter at room temperature, potentially allowing for the development of an entirely new class of optoelectronic devices [1]. Previously, J-aggregate deposition methods have required the exposure of a device in fabrication to the solvents of a J-aggregate solution that can potentially damage other optically or electrically active materials and restrict the steps involved in fabricating devices. In this work, we demonstrate a new stamping technique for depositing J-aggregate thin films that decouples the formation of J-aggregates from the placement of J-aggregate thin films into device structures.

Combining research in polyelectrolyte layer-by-layer deposition of J-aggregates [2] with stamping of polyelectrolyte thin films, we show how to form thin films of J-aggregates on a stamp and then stamp those films into device structures [3]. We show the optical and morphological properties of stamped J-aggregate films and calculate the optical constants of the films (Figure 1), which we use to determine the density of J-aggregated dye molecules in the final thin film. Additionally, we investigate device structures enabled by stamping of J-aggregate thin films, including J-aggregate organic light-emitting devices and patterned J-aggregate devices made via stamp pattern transfer (Figure 2). Lastly, we explore the extension of J-aggregate thin-film stamping to other methods of depositing J-aggregate thin films, including Langmuir-Blodgett-type deposition methods.



▲ Figure 1: Complex index of refraction of PAH (polyallylamine hydrochloride)/TDBC (J-aggregating cyanine dye) film formed on a PDMS (polydimethylsiloxane) stamp and deposited on glass using microcontact printing, calculated from reflectance measurements using Kramers-Kronig regression and a thin film dielectric model. The peak extinction coefficient corresponds to an absorption constant of 1.2 x 10^6 cm^{-1}.



▲ Figure 2: Photoluminescence of patterned PAH/TDBC film using green light excitation. Patterned PDMS stamps were made by curing PDMS on a silicon mold. The J-aggregate thin films were grown on patterned PDMS stamps, and in the microcontact printing process only the raised portions of the film were transferred to the glass substrate.

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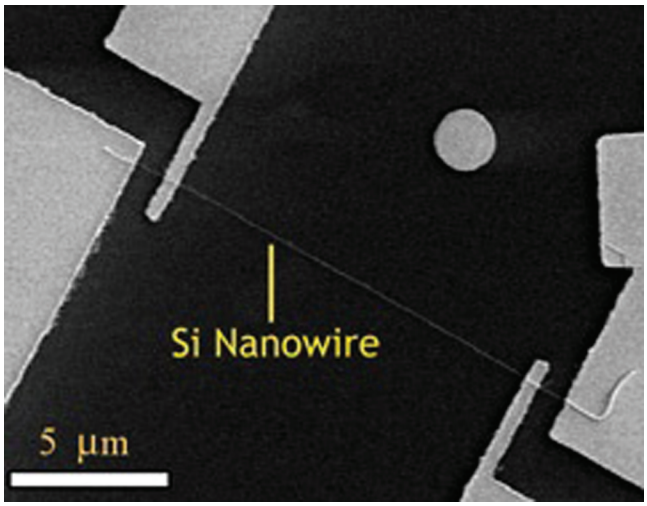
Measuring Thermal and Thermoelectric Properties of Single Nanowires and Carbon Nanotubes

C. Dames, C.T. Harris, A. Muto, G. Chen (in coll. with M.S. Dresselhaus, MIT, Z.F. Ren, Boston College)
Sponsorship: JPL, NSF

Knowledge of nanowire and carbon nanotube thermal and thermoelectric properties will be important for the thermal management of nanoscale devices that have recently been demonstrated (optoelectronic, sensing, and computing) and essential for the design of nanostructured thermoelectric materials. For nanowire diameters smaller than the bulk mean-free path of heat carriers (electrons and/or phonons), theory predicts that the thermal conductivity of these structures will be reduced when compared to similar bulk materials [1]. In order to experimentally verify these predictions, we are exploring several systems to measure the properties of single nanowires and carbon nanotubes.

Current work includes a basic platform to measure the thermal conductivity and specific heat of electrically conductive nanowires, such as the silicon nanowire shown below. Electron-beam lithography was used to pattern the leads of a four-point probe aligned to the ends of the nanowire. Joule heating of a suspended nanowire with thermally clamped ends results in a temperature rise of the nanowire due to its finite thermal resistance. This temperature rise can be measured by resistance thermometry (again using the nanowire) and used to calculate its thermal conductivity and specific heat. This technique is being adapted for an *in situ* TEM measurement, to enable high-throughput physical property measurements of many nanowires of various geometries and morphologies, and allow correlations with their atomic structure as determined by TEM.

Microfabricated metal lines can also be employed to measure electrically insulating nanowires. Using electron beam lithography, a metal heater line is fabricated such that a target nanowire crosses the center of the line. With the ends of the nanowire and heater thermally anchored, the nanowire removes a fraction of heat from the heater line, reducing the heater's temperature rise, and thus making it possible to calculate the thermal resistance of the nanowire.



▲ Figure 1: Contacts for a four-point probe measurement of a single silicon nanowire.

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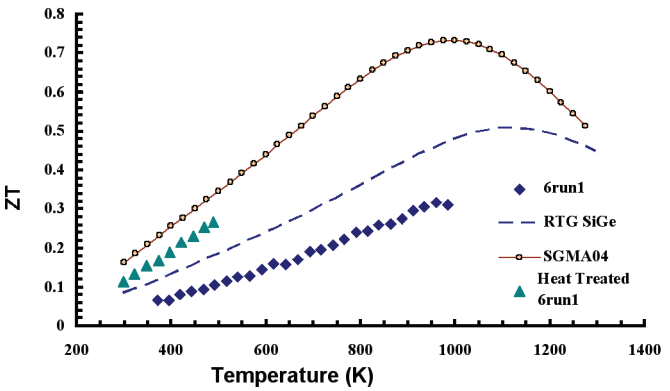
Nanocomposites as Thermoelectric Materials

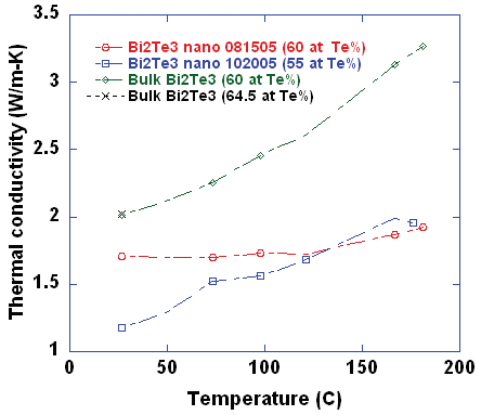
H. Lee, Q. Hao, M. Tang, M.S. Dresselhaus, G. Chen (in coll. with Z.F. Ren, Boston College, J.-P. Fluerial, JPL, P. Gogna, JPL)
Sponsorship: NASA, Intel, Nanolab SBIR

Direct energy conversion between thermal and electrical energy based on thermoelectric effects is attractive for potential applications in waste heat recovery and environmentally-friendly refrigeration [1-2]. The energy conversion efficiency depends on the dimensionless figure of merit of the thermoelectric materials, ZT, which is proportional to electrical conductivity, square of the Seebeck coefficient, inverse of the thermal conductivity, and absolute temperature. At the current stage, the low ZT values of available materials restrict the efficient applications of this technology. Recently, significant enhancements in ZT were presented through the use of nanostructures such as superlattices. Previous works done by our group show that such improvement in superlattices is mainly attributed to the increased interfacial diffuse phonon scattering [3-4]. These studies lead us to pursuing the nanocomposite approach as a cost-effective alternative in developing high ZT materials.

Previously, we reported thermal conductivity reduction in SiGe nanocomposites. Through collaboration with Boston College group and Jet Propulsion Lab, we realized significant improvement in the ZT over that of SiGe used in the past NASA flights (Figure 1). We are also working on Bi_2Te_3 and PbTe nanocomposites. Our preliminary results on Bi_2Te_3 nanocomposites also show reduced thermal conductivities. Work is in progress to optimize the structures for further improving the ZT values.



▲ Figure 1: Measurements of temperature-dependent ZT. Nanostructured sample SGMA04 shows higher ZT than typical bulk alloy, "RTG SiGe."



▲ Figure 2: Temperature-dependent thermal conductivities of Bi_2Te_3 nanocomposite samples. Data of bulk materials are plotted for comparison.

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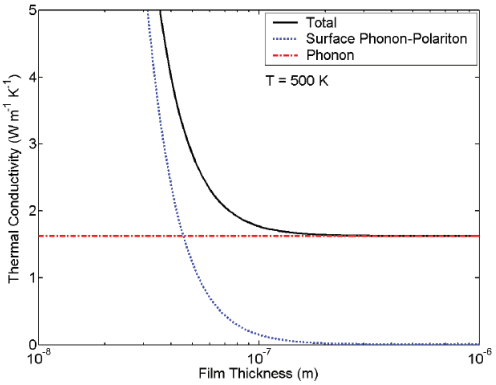
Flux and Force due to Near-field Thermal Radiation

D. Chen, L. Hu, A. Narayanaswamy, G. Chen (in coll. with J.D. Joannopoulos)
Sponsorship: ONR, MURI (through UC Berkeley)

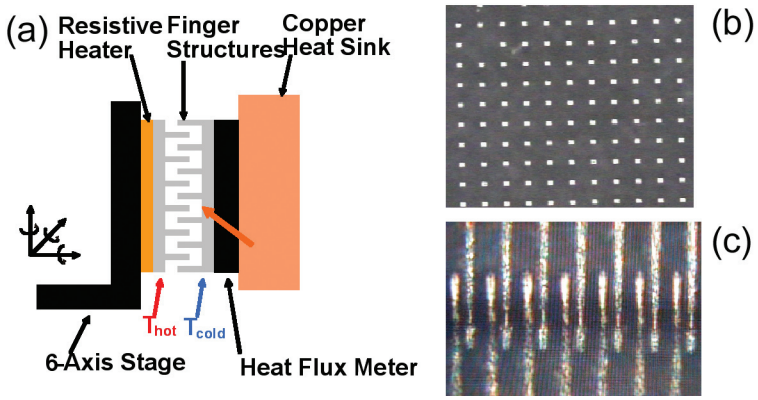
Fluctuating electromagnetic fields of thermal origin lead to surprising results in the near-field. For instance, the radiative energy transfer between bodies that can support surface polaritons can be increased by a few orders of magnitude compared to far-field thermal radiation predicted by Planck's law. These fluctuating fields, even at absolute zero temperature, also lead to the Casimir force between objects. We have previously shown that the enhancement in radiative transfer can be used to improve the performance of thermophotovoltaic (TPV) [1] as well as thermoelectric devices [2].

Surface polaritons, which are involved in enhancing out-of-plane radiative transfer, can also lead to significant increase in in-plane thermal "conductivity." We model the in-plane energy transfer due to these surface polaritons as a diffusive process in an absorbing medium. Due to the well-known very long propagation length of the anti-symmetric mode, we find that the surface polaritons can make a significant contribution to the effective thermal conductivity along thin films. In particular, for a 40 nm thick film of amorphous silicon dioxide, we calculate a total thermal conductivity of 4 W m^{-1} K^{-1} at 500 K, which is an increase of ~100% over the intrinsic phonon thermal conductivity [3], as shown in Figure 1. In addition to thermal in-plane transport, we are in the process of measuring near-field thermal radiation transfer and forces between two spherical micro-particles as well as between spheres and planar substrates.

We are developing a 2-D structure that features micro-sized interdigitized hot and cold fingers, as shown in Figure 2. The objective is to increase both power density and efficiency of TPV devices by exploiting the increased radiative surface/volume ratio, photon recycling, and photonic band gap in one compact device structure. We have fabricated the finger structures and successfully aligned the two mating structures. Thermal characterization of the device is in progress.



▲ Figure 1: Amorphous silicon dioxide (glass) thermal conductivity due to phonons and surface phonon polaritons as a function of film thickness at 500 K.



▲ Figure 2: (a) Illustration of the testing rig for the interdigitized thermophotovoltaic device structure. (b) Top-view of one set of the finger structures. (c) Aligned finger structures.

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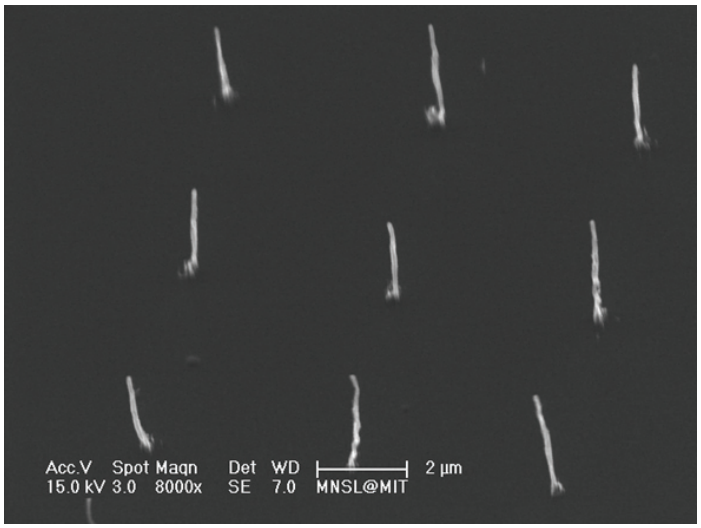
CNT Assembly by Nanopelleting

S.D. Gouda, S. Kim, S.-G. Kim
Sponsorship: Intelligent Microsystems Center

We have developed a novel method of manufacturing and assembling process termed nano-pelleting [1-2], which refers to large-scale handling and long-range order assembly of individual carbon nanotubes (CNTs). The nano-pelleting concept overcomes the limitation of very small-scale order by embedding carbon nanotubes into micro-scale pellets. This technique includes vertically growing single strand CNTs, embedding a CNT into a polymeric pellet, separating a pellet, and transplanting a CNT. The CNTs are grown vertically, both individually and in bunches, on the patterned catalytic metal using a plasma enhanced chemical vapor deposition (PECVD) machine (Figure 1) built by us at MIT. The machine's key feature is the control of the substrate temperature during the growth process. At the bottom of the ceramic heater, three thermocouples are connected to measure the temperature, which is controlled by the heater controller. Plasma is formed between anode and cathode by applying a DC voltage, which then decomposes acetylene into carbon that deposits below the Ni catalyst and leads to the formation of carbon nanotubes. The process sequence to make pellets is the following: coating PMMA on the silicon wafer, exposing the photo-resists using Raith 150 to obtain the desired patterns by varying the aperture size, dose, electric field, developing the photo-resist, depositing Ti/Ni (25nm), and lifting-off the resist to obtain Ni-catalyst nano-dots. Single stranded CNTs are grown in the PECVD machine with optimized process conditions as shown in Figure 2. On these isolated CNTs, SU-8 is spin-coated to form a thickness of 25 micro-meter. This SU-8 layer is exposed to UV light using an appropriate mask and then developed to form nano-pellets. The nano-pellets are released from the silicon substrate by manually breaking them with a spark needle. We are developing an in-plane AFM probe [3] with mechanically assembled CNT tips.

▲ Figure 1: The PECVD machine for growing CNTs at MIT.



▲ Figure 2: Single strand CNTs grown by the PECVD machine.

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Integrated Carbon Nanotube Sensors

K.-J. Lee, T.S. Cho, A.P. Chandrakasan, J. Kong
Sponsorship: Intel, MARCO IFC

Single-walled carbon nanotubes (SWNT) exhibit unique mechanical and electrical properties that make them attractive for nanoelectronic applications. In particular, the conductance of a semiconducting SWNT is known to change significantly when exposed to certain gases [1]. The high sensitivity and fast response time make carbon nanotubes (CNT) very attractive for chemical sensing applications. However, the underlying sensing mechanism of CNT sensors is quite different from Si-based chemical transistors, and fabrication methods generally yield devices with large variations. Device variations and technology integration issues must be resolved before any CNT sensor devices can become practical [2].

In this project, we grow carbon nanotubes through chemical vapor deposition (CVD) and fabricate devices for an ultra low-power wireless sensing system. This work is done in collaboration with T. S. Cho in Professor A. Chandrakasan's group from the Department of Electrical Engineering and Computer Science at MIT, whose back-end circuitry will provide an interface to our CNT sensor array. The main goals of this project are to build a CNT sensor array with high yield of semiconducting SWNTs, high sensitivity and selectivity of gases, and low variability in the performance of the device. Through statistical characterization of the device, we attempt to get a better grasp of the underlying CNT sensing mechanism and find enhanced fabrication methods to reduce performance variability. In addition, chemical functionalization of CNT sensors will allow the target application to detect different types of toxic gases for environmental and industrial applications.

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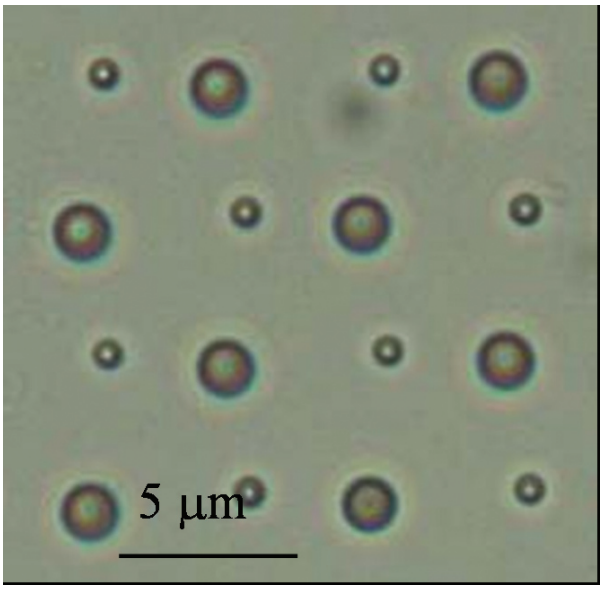
Templated Assembly by Selective Removal

S. Jung, F. Eid, C. Livermore
Sponsorship: NSF, 3M Corporation

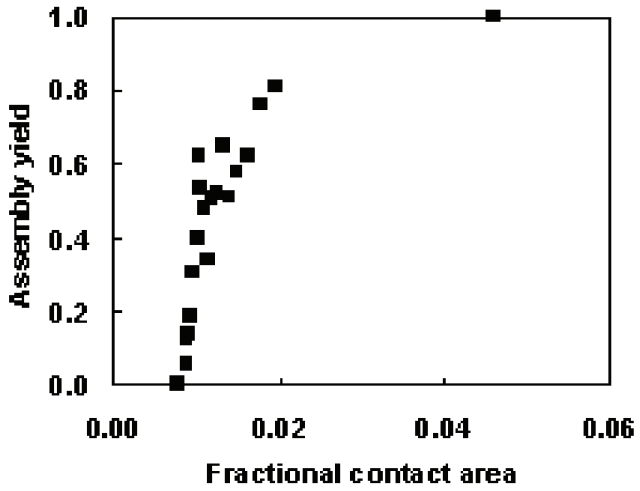
In this project, an effective technique for site-selective, multicomponent assembly at the nano- and micro-scale has been created and quantitatively modeled. This approach offers great promise for assembling arbitrary (not necessarily periodic) systems of multiple different types of nanoscale components, such as electronics (memory, logic, interconnects, displays) and sensor systems.

The key elements of the approach follow. First, the topography of the substrate is modified to match the components' 3D shapes. Then the substrate and components are coated with an adhesion promoter, such as a hydrophobic SAM for adhesion in a water-based environment. The components and substrate are placed in a fluid environment for the assembly process, and megahertz frequency ultrasound is applied to the fluid bath. Components contact the substrate randomly and adhere wherever they land; however, components that are not in shape-matched sites are removed by fluid forces initiated by the high frequency ultrasound. Components in shape-matched sites are selectively retained because their adhesive force is stronger than the removal forces. Figure 1 is an optical micrograph showing the successful assembly of 600 nm and 2 μm diameter silica microspheres into designated sites on the substrate. Figure 2 shows how measured assembly yield of spheres into holes of slightly different sizes increases with the contact area between spheres and substrate.

This approach to assembly is inherently selective; since each component will adhere only in a shape- and size-matched site, geometrically distinct components will assemble only into their designated assembly sites. This allows the organizing information to be stored in the template initially, and permits components that may not be compatible with top-down manufacturing techniques to be added to the system later, with high positional precision. Work is underway to demonstrate this approach at smaller size scales and to create practical systems using this technology.



▲ Figure 1: Optical micrograph of 600 nm and 2 μm spheres assembled into designated sites on a surfaces.

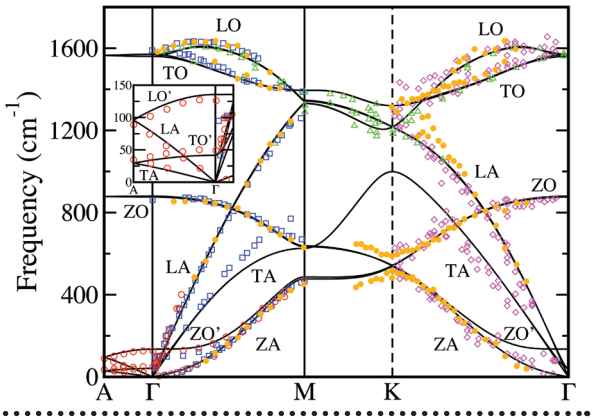


▲ Figure 2: Plot of assembly yield (number of filled holes/total number of holes) vs. contact area between sphere and hole. Assembly yield increases from 0% to 100% as quality of the shape match improves.

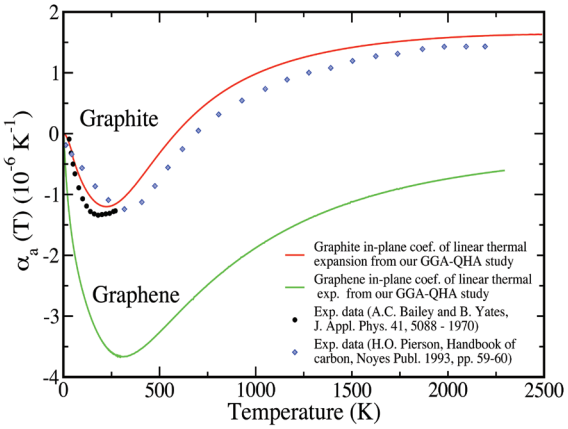
Vibrational, Thermodynamic, and Transport Properties of Carbon Nanotubes from Density-functional Perturbation Theory

N. Bonini, N. Marzari
Sponsorship: MARCO IFC, ISN

Carbon nanotubes present unique physical properties, which make them promising materials for applications in high-performance nanoscale devices. Indeed, because of their high thermal and electrical conductivities, carbon nanotubes are excellent candidates both as interconnects in integrated circuits and as heat-management materials in silicon chips. Unfortunately, due to the challenge in nanoscale experiments, the thermodynamics of these materials as well as the origin and the limits of their transport properties are still unclear. In this project we use a combination of density-functional theory and density-functional perturbation theory to study the vibrational properties of carbon nanotubes. In particular we investigate anharmonic effects, such as thermal expansion and phonon lifetimes, which are key quantities to understanding the thermodynamical and transport properties of these systems. The thermal expansion coefficients are calculated from the minimization of the vibrational free energy in the quasi-harmonic approximation. This same approach provides excellent agreement with experimental data for the case, e.g., of graphite. Our results show that carbon nanotubes contract both in the axial and radial directions at low and room temperature, while they expand at higher temperatures. Anharmonic phonon lifetimes are evaluated from the cubic terms in the interatomic potential, using density-functional perturbation theory and the 2n+1 theorem. We plan to use these quantities to predict the transport properties of carbon nanotubes using the Boltzmann transport equation– in particular how inelastic excitation of phonons further reduces the ballistic transport of electrons.



▲ Figure 1: The *ab initio* phonon dispersion of graphite (solid lines). The inset shows an enlargement of the low-frequency Γ-A region. The experimental data are also shown (color marks).



▲ Figure 2: In-plane coefficient of thermal expansion as a function of temperature for graphite and graphene.

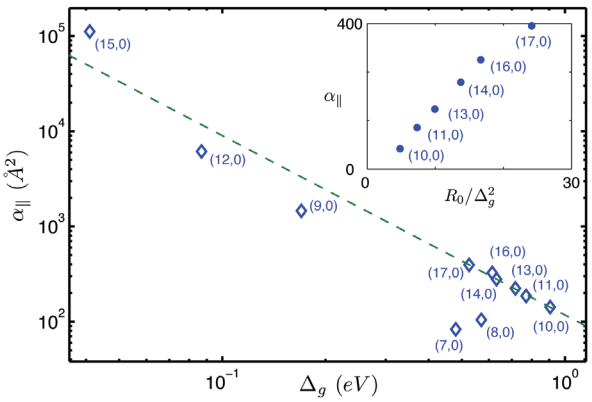
Static Dielectric Response of Single-wall and Multi-wall Carbon Nanotubes from First-principles

B. Kozinsky, N. Marzari
Sponsorship: MARCO IFC, NSF

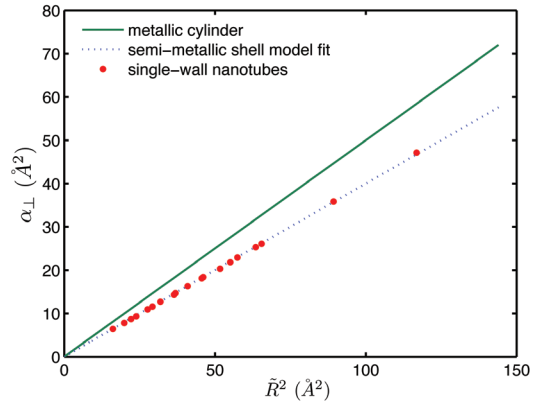
We characterize the response of isolated single-wall (SWNT) and multi-wall (MWNT) carbon nanotubes and bundles to static electric fields using first-principles calculations and density-functional theory. The longitudinal polarizability of semiconducting SWNTs scales as the inverse square of the band gap (Figure 1). Because of the absence of depolarization effects in the longitudinal direction, nearby parallel tubes have very weak dielectric interaction, so in MWNTs and bundles the longitudinal polarizability is given by the sum of polarizabilities of the constituent tubes.

The transverse polarizability of SWNTs is insensitive to band gaps and chiralities and is proportional to the square of the radius (Figure 2). The electric field applied perpendicular to a SWNT is screened by a universal factor of about 4.5, independent of the nanotube's radius. This property is inherited from the anomalous scale-invariant in-plane response of a sheet of graphene. The transverse response is thus intermediate between metallic and insulating. We construct a simple electrostatic model based on a scale-invariance relation that captures accurately the first-principles results for transverse response of SWNTs and MWNTs. Because of strong screening and radius dependence of polarizability, the outer few layers dominate the response in MWNTs.

Using the results of our calculations, we analyze the feasibility of separating semiconducting and metallic nanotubes using uniform and non-uniform static electric fields in vacuum and in solutions. We also find that the dielectric response of non-chiral SWNTs in both directions remains linear up to very high values of the applied field.



▲ Figure 1: Log scale plot of the longitudinal polarizability (per unit length) of zigzag semiconducting SWNTs as a function of the band gap. The dashed line has slope –2. The inset shows the values for large-gap zigzag SWNTs as a function of radius divided by band gap squared.



▲ Figure 2: Transverse polarizabilities (per unit length) of armchair and zigzag nanotubes as a function of radius squared. The solid line corresponds to an ideal metallic cylinder, and the dashed line is the best fit of the first-principles results. This figure shows that transverse polarizabilities of SWNTs of different band gaps and chiralities lie on the same line.

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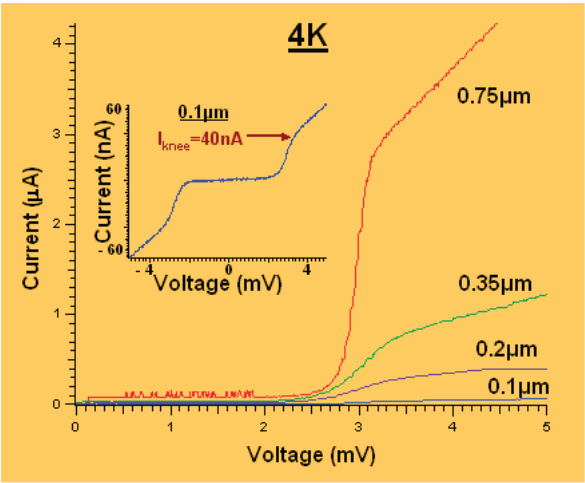
Niobium Superconducting Persistent-Current Qubits with Deep Submicron Josephson Junctions

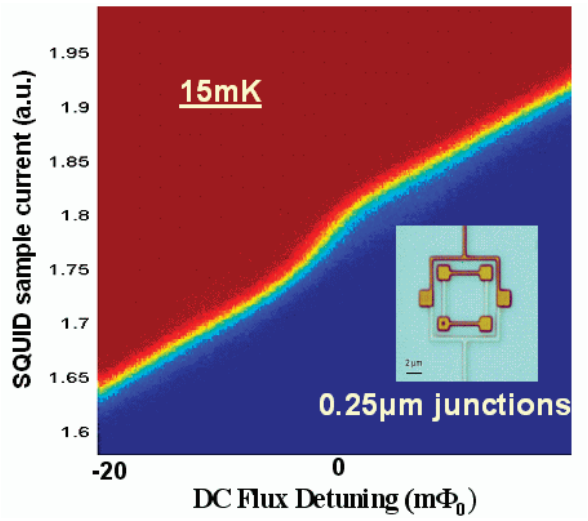
D.M. Berns, W.D. Oliver, S.O. Valenzuela, T.P. Orlando, V. Bolkhovsky, E. Macedo

Quantum computation holds the potential to solve problems currently intractable with current computers. The basic component of a quantum computer is the "qubit," the quantum analog to today's bits. Any two-level quantum system could serve as a qubit; however, the qubit must satisfy two major criteria for practical quantum computing: long coherence times and the ability to scale to thousands of qubits. Persistent-current (PC) qubits are promising candidates for realizing such a large-scale quantum computer. The PC qubit is a superconducting circuit with Josephson junction (JJ) elements that can be effectively operated as a two-level quantum system [1].

With a tri-layer process using optical lithography, we can create the deep-submicron JJs required to realize large qubit tunnel-couplings, which allow improved immunity to dielectric-induced decoherence, and there is no foreseeable barrier to large-scale integration. We have recently begun measuring and characterizing the PC qubits designed with these deep-submicron JJs fabricated with the Nb-Al/AlOx-Nb trilayers. Initital testing of the JJs shows excellent performance down to sizes necessary for long decoherence times (Figure 1), and first studies of how the ground state of the new qubits changes as the applied DC flux is swept show the large tunnel-couplings we were aiming for (Figure 2).



▲ Figure 1: IV traces taken at 4K for a few different test junctions, from 0.75 um down to 0.1um. Blown up in the inset is the 0.1 um junction IV and we see a knee current of 40 nA and a very large subgap resistance.



▲ Figure 2: Qubit step taken at dilution refrigerator temperatures with the device seen in the inset, where the larger junctions are 250 nm on a side. One can clearly see that as the applied dc magnetic flux is changed, the ground state changes from one circulating current state to the other.

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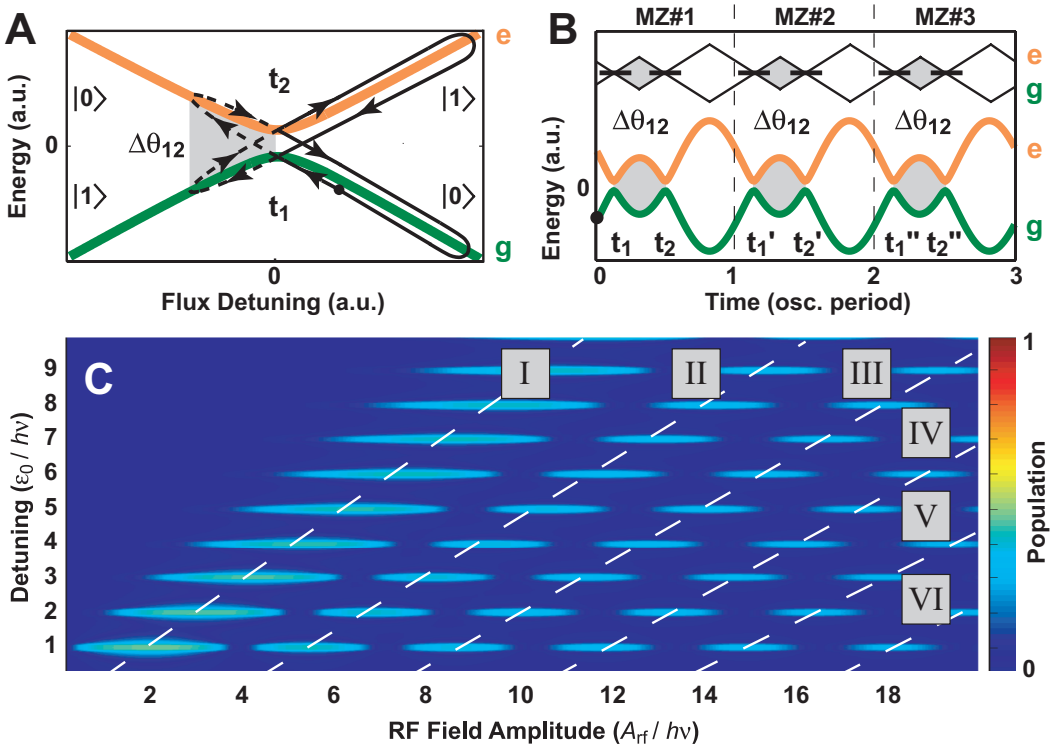
Mach-Zehnder Interferometry in a Persistent-Current Qubit

W.D. Oliver, Y. Yu, J.C. Lee, K.K. Berggren, L.S. Levitov, T.P. Orlando

We have demonstrated Mach-Zehnder (MZ)-type interferometry with a niobium superconducting persistent-current qubit. These experiments exhibit remarkable agreement with theory, and they will find application to non-adiabatic qubit control methods. The qubit is an artificial atom, the ground and first-excited states of which exhibit an avoided crossing. Driving the qubit with a large-amplitude harmonic excitation sweeps it through this avoided crossing two times per period. The induced Landau-Zener (LZ) transitions at the avoided crossing cause coherent population transfer between the eigenstates, and the accumulated phase between LZ transitions varies with the driving amplitude. This is analogous to a MZ interferometer, in which the LZ transition is the beamsplitter and the relative phase accumulated between LZ transitions is the optical path-length difference between the arms of the interferometer. Over the entire length of the microwave driving pulse, we have a sequence of MZ interferometers. We have observed MZ quantum interference fringes as a function of the driving amplitude for single- and multi-photon excitations.



▲ Figure 1: (a) Energy of the two-level system. Starting at the marker, the qubit state is swept through the avoided crossing twice, accumulating a phase between the LZ transitions that occur. (b) The corresponding energy variation over a few pulse periods. The sequence of LZ transitions and phase accumulation are analogous to a sequence of Mach-Zehnder interferometers. (c) Qubit population as a function of driving amplitude. We see the Bessel dependence to the Mach-Zehnder-like quantum interference for n-photon transitions.

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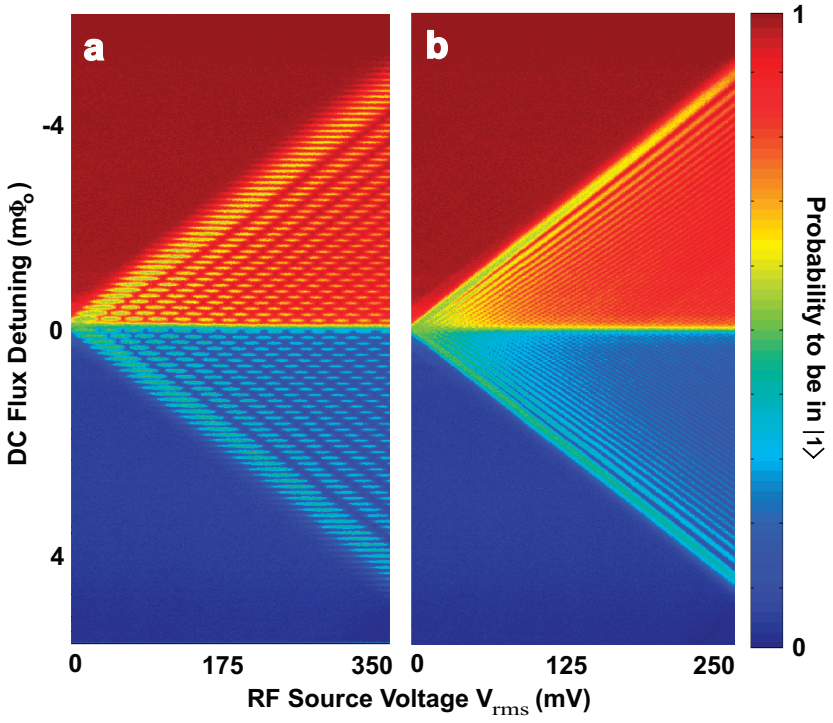
Coherent Quasi-classical Dynamics of a Niobium Persistent-Current Qubit

D.M. Berns, S.O. Valenzuela, W.D. Oliver, L.S. Levitov, T.P. Orlando

We have recently demonstrated Mach-Zehnder-type interferometry in the persistent-current qubit, in the strong driving limit [1]. We have now extended this work to much lower driving frequencies. By driving our system at frequencies smaller than our linewidth, we have observed a new regime of quasi-classical dynamics within the strong driving limit. Now a transition at a DC flux detuning resonant with n photons is assisted by neighboring resonances. In this regime we find remarkable agreement with theory by assuming the population transfer rate for the n^{th} photon resonance is the sum of rates from all other resonances.



◀ Figure 1 : Qubit population as a function of driving amplitude. (a) Driving frequency = 270 MHz. We see the Bessel dependence to the Mach-Zehnder-like quantum interference for n-photon transitions. (b) Driving frequency = 90 MHz. Individual resonances are no longer distinguishable but we still see coherent quantum interference.

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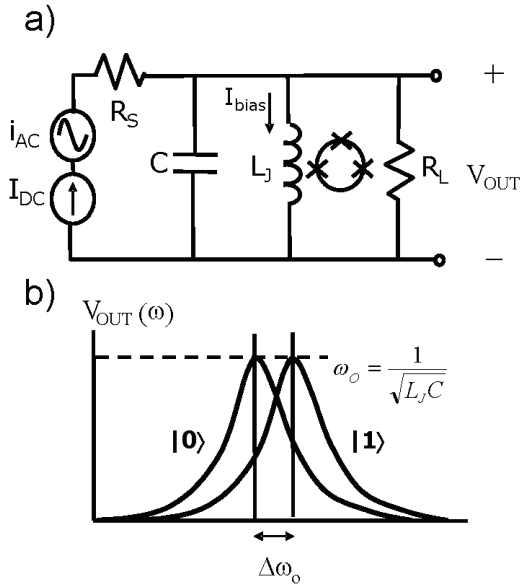
Resonant Readout of a Persistent Current Qubit

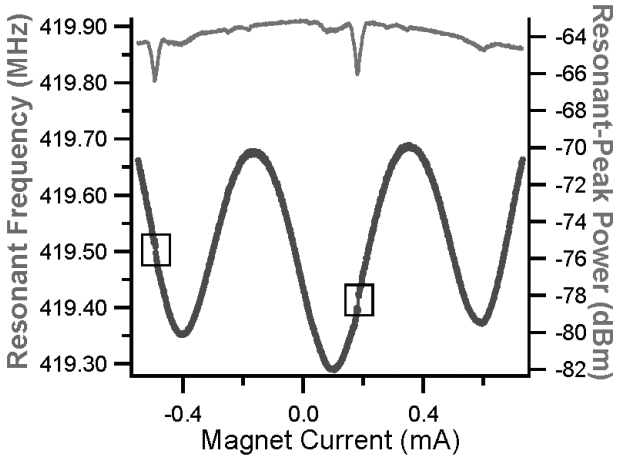
J.C. Lee, W.D. Oliver, T.P. Orlando
Sponsorship: DURINT, ARDA, NSF

The two logical states of a persistent current (PC) qubit correspond to oppositely circulating currents in the qubit loop. The induced magnetic flux associated with the current either adds to or subtracts from the background flux. The state of the qubit can thus be detected by a DC SQUID magnetometer inductively coupled to the qubit.

We have implemented a resonant technique that uses a SQUID as a flux-sensitive Josephson inductor for qubit readout. This approach keeps the readout SQUID biased at low currents along the supercurrent branch and is more desired for quantum computing applications in reducing the level of decoherence on the qubit. By incorporating the SQUID inductor in a high-Q on-chip resonant circuit, we can distinguish the two flux states of a niobium PC qubit by observing a shift in the resonant frequency of the readout circuit. The nonlinear nature of the SQUID Josephson inductance, as well as its effect on the resonant spectra of the readout circuit, was also characterized.



▲ Figure 1: a) The SQUID inductor is incorporated in a resonant readout circuit. It is inductively coupled to a PC qubit to detect its state. b) A transition of the qubit state changes the Josephson inductance of the SQUID and can be sensed as a shift in the resonant frequency of the readout circuit.



▲ Figure 2: Experimental results at 300 mK: the lower plot (left axis) shows the modulation of the resonant frequency with external magnetic field. Qubit steps corresponding to transitions between opposite flux states were observed at every 1.3 periods of the SQUID lobe. The upper plot (right axis) shows the corresponding peak amplitude of the resonant spectrum. The dip in peak power coincides with the qubit step.

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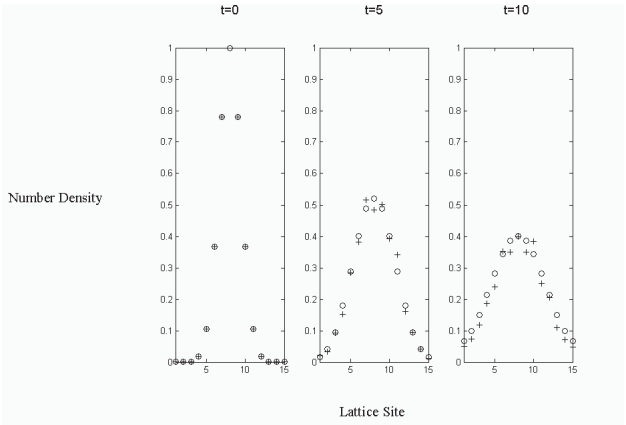
Type-II Quantum Computing Using Superconducting Qubits

D. Berns, W.M. Kaminsky, B. Cord, K.K. Berggren, W.D. Oliver, T.P. Orlando (in coll. with J. Yepez, Air Force Laboratories)
Sponsorship: AFOSR, Fannie and John Hertz Foundation

Most algorithms designed for quantum computers will not best their classical counterparts until they are implemented with thousands of qubits. For example, the factoring of binary numbers with a quantum computer is estimated to be faster than a classical computer only when the length of the number is greater than about 500 digits [1]. In contrast, the factorized quantum lattice-gas algorithm (FQLGA) [2] for fluid dynamics simulation, even when run on a quantum computer significantly smaller than the one just discussed, has significant advantages over its classical counterparts.

The FQLGA is the quantum version of classical lattice-gases (CLG) [3]. CLGs are an extension of classical cellular automata with the goal of simulating fluid dynamics without reference to specific microscopic interactions. The binary nature of the CLG lattice variables is replaced for the FQLGA by the Hilbert space of a two-level quantum system. The results of this replacement are similar to that of the lattice-Boltzmann model, but with a few significant differences [4]. The first is the exponential decrease in required memory. The second is the ability to simulate arbitrarily small viscosities.

We have recently developed two implementations of the algorithm for the 1D diffusion equation using the PC Qubit [5]. The first consists of initializing the qubits while keeping them in their ground state, and then performing the collision by quickly changing their flux bias points and then performing a single $\pi/2$ pulse (Figure 1). This initialization technique could prove quite useful, since relaxation effects are avoided, but the way we have implemented the collision is not easily generalized to other collisions. A more general collision implementation was then developed by decomposing the unitary collision matrix into a sequence of single qubit rotations and coupled free evolution. The single qubit rotations then also serve to initialize the fluid's mass density.



▲ Figure 1: Simulation of the FQLGA for 1D diffusion is pictured(o) alongside simulation of the first proposed implementation(+). The expected diffusion of a gaussian is observed.

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Scalable Superconducting Architecture for Adiabatic Quantum Computation

W.M. Kaminsky, S. Lloyd, T.P. Orlando
Sponsorship: Fannie and John Hertz Foundation

Adiabatic quantum computation (AQC) is an approach to universal quantum computation in which the entire computation is performed in the ground state of a suitably chosen Hamiltonian [1]. As such, AQC offers intrinsic protection against dephasing and dissipation [2,3]. Moreover, AQC naturally suggests a novel quantum approach to the classically intractable constrained minimization problems of the complexity class NP. Namely, by exploiting the ability of coherent quantum systems to follow adiabatically the ground state of a slowly changing Hamiltonian, AQC promises to bypass automatically the many separated local minima occurring in difficult constrained minimization problems that are responsible for the inefficiency of classical minimization algorithms. To date, most research on AQC [4-8] has focused on determining the precise extent to which it could outperform classical minimization algorithms. The tantalizing possibility remains that–at least for all practical purposes–AQC offers at least a large polynomial, and often an exponential, speedup over classical algorithms. However, it may be the case that in the same way the efficiency of many practical classical algorithms for NP problems can be established only empirically, the efficiency of AQC on large instances of classically intractable problems can be established only by building a large-scale AQC experiment.

To make feasible such a large-scale AQC experiment, we have proposed a scalable architecture for AQC based on the superconducting persistent-current (PC) qubits [9, 10] already under development here at MIT. As first proposed in [11], the architecture naturally incorporates the terms present in the PC qubit Hamiltonian by exploiting the isomorphism [12] between antiferromagnetic Ising models in applied magnetic fields and the canonical NP-complete graph theory problem Max Independent Set. Such a design notably removes any need for the interqubit couplings to be varied during the computation. Moreover, since Max Independent Set remains NP-complete even when restricted to planar graphs where each vertex is connected to no more than 3 others by edges, a scalable programmable architecture capable of posing any problem in the class NP may simply take the form of a 2D, hexagonal, square, or triangular lattice of qubits. Finally, the latest version of the architecture [13] permits interqubit couplings to be limited to nearest-neighbors and qubit measurements to be inefficient.

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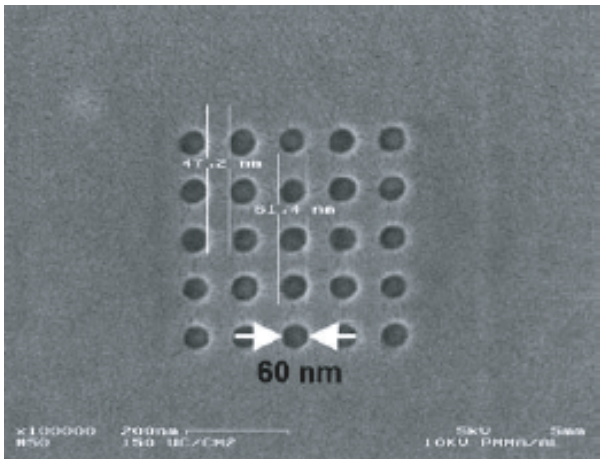
Fabrication Methods for Adiabatic Quantum Computing Devices

B. Cord, W. Kaminsky, T.P. Orlando, K.K. Berggren
Sponsorship: Quantum Computing Graduate Research Fellowship, AFOSR

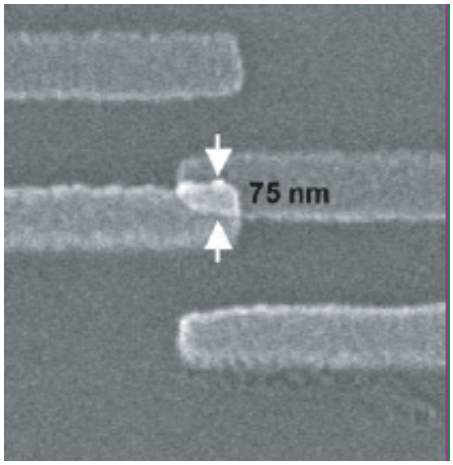
Adiabatic quantum computing devices (AQCs) have been implemented successfully in several types of systems, including ion traps, nuclear spins, and photon cavities. However, we find implementing AQCs in superconductive circuits offers several key advantages. Primarily, using standard techniques adapted from the semiconductor industry, we can fabricate very large numbers of superconductor-based qubits in CMOS-compatible materials [1]

The stringent resolution and uniformity requirements for AQC devices present an interesting fabrication challenge. In order to perform certain AQC experiments, Josephson junctions with diameters of ~50 nm are useful. While previous quantum computing experiments at MIT used devices fabricated using optical projection lithography, sub-100-nm dimensions require alternate techniques, such as electron-beam lithography and suspended shadow-mask evaporation. Additionally, the uniformity of these nanoscale junctions must be high and the areas of the Josephson junctions within a single device must exhibit very low variation.

No readily available lithographic technology meets these requirements, so research is being conducted on methods of defining arbitrary features as small as 50 nm with the precision required for adiabatic quantum computing. Current experiments have focused on improving the resolution and uniformity of the scanning electron-beam lithography (SEBL) system in the Nanostructures Laboratory, particularly in investigating the effects of different pattern geometries on the uniformity of very small features. Parallel work is also being done on a reliable, automated method of measuring the dimensions of very small structures for the purposes of determining uniformity, using scanning electron microscope (SEM) images and image-processing software.



▲ Figure 1: An SEM of an array of 60-nm-diameter features in photoresist.



▲ Figure 2: An SEM of an 0.007-μm^2 Al/AlOx/Al Josephson junction fabricated via shadow-mask evaporation.

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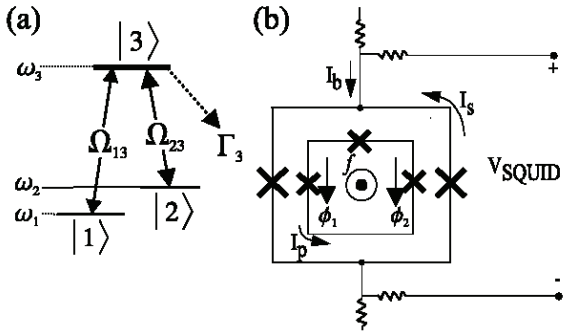
Probing Decoherence with Electromagnetically Induced Transparency in Superconductive Quantum Circuits

K. Murali, W.D. Oliver, T.P. Orlando (in coll. with Z. Dutton, Naval Research Laboratory)
Sponsorship: DURINT, ARDA

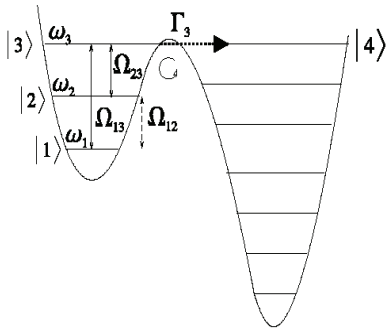
Superconductive quantum circuits (SQCs) comprising mesoscopic Josephson junctions, quantized flux, and/or charge states are analogous to the quantized internal levels of an atom [1]. This SQC-atom analogy can be extended to the quantum optical effects associated with atoms, such as electromagnetically induced transparency (EIT) [2, 6].

The three-level Λ-system for our S-EIT system (Figure 1a) is a standard energy-level structure utilized in atomic EIT. It comprises two meta-stable states $|1\rangle$ and $|2\rangle$, each of which may be coupled to a third excited state $|3\rangle$. In an atomic EIT scheme, a strong "control" laser couples the $|2\rangle \rightarrow |3\rangle$ transition, and a weak resonant "probe" laser couples the $|1\rangle \rightarrow |3\rangle$ transition. By itself, the probe laser light is readily absorbed by the atoms and thus the transmittance of the laser light through the atoms is very low. However, when the control and probe laser are applied simultaneously, destructive quantum interference between the atomic states involved in the two driven transitions causes the atom to become "transparent" to both the probe and control laser light [2-4]. Thus, the light passes through the atoms with virtually no absorption. In this work, we propose to use EIT in SQCs to sensitively probe decoherence.

The SQC (Figure 1b) can be biased to result in an asymmetric double-well potential as shown in Figure 2. The three states in the left well constitute the superconductive analog to the atomic Λ-system [5]. States $|1\rangle$ and $|2\rangle$ are "meta-stable" qubit states, with a tunneling and coherence time much longer than the excited "readout" state $|3\rangle$. State $|3\rangle$ has a strong inter-well transition when tuned on-resonance to state $|4\rangle$. Thus, a particle reaching state $|3\rangle$ will tend to tunnel quickly to state $|4\rangle$, causing the circulating current to switch to the other direction, an event that is detected with a SQUID. Knowing how long the SQC remains transparent, i.e., does not reach state $|3\rangle$, in the S-EIT experiment provides an estimate of the decoherence time.



▲ Figure 1: a. Energy level diagram of a three-level Λ system. EIT can occur in atoms possessing two long-lived states |1>, |2>, each of which is coupled via resonant laser light fields to a radiatively decaying state |3>. b. Circuit schematic of the persistent –current qubit and its readout SQUID.



▲ Figure 2: One-dimensional double-well potential and energy-level diagram for a three-level SQC.

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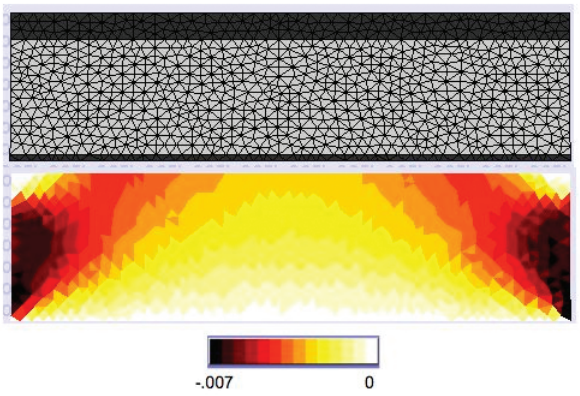
Magnetoelastic Behavior of Magnetic Nanostructures

E. Friend, C.A. Ross, R.C. O'Handley
Sponsorship: NSF

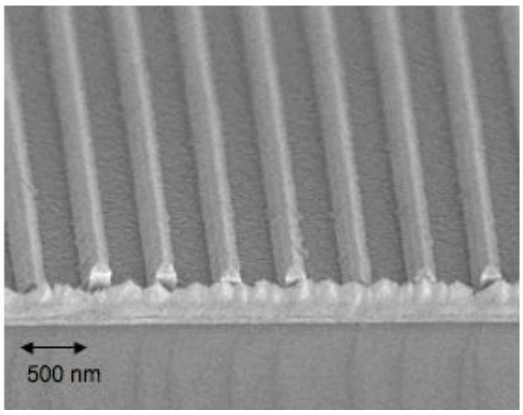
Previous researchers have investigated the magnetic properties of multilayer thin-film sandwiches of copper/ nickel/ copper epitaxially grown on silicon [1]. In this system, the magnetic properties of the nickel layer change drastically as the thickness (and therefore the amount of strain) of the nickel layer varies, and it does so over a thickness range that is uniquely broad. This effect is due to both the large magnetoelastic energy and to the surface magnetocrystalline anisotropy energy of the nickel film.

Our research focuses on understanding the effects of patterning these Cu/Ni/Cu films into nanoscale lines. Once patterned, the strained films can relax at the edges, with the strain relief being a function of line width and thickness. The ultimate aims are to elucidate the relationship between stress and magnetic properties in nanoscale features, to understand and control the effects of stress on magnetic nanostructures, and to exploit this effect to achieve desired magnetic properties. Understanding this relationship is a key part of the development of future magnetic recording technologies such as patterned recording media and read/ write heads.

Magnetic characterization of Cu/Ni/Cu nanolines (Figure 2) has shown that, contrary to the expectations from shape anisotropy, the preferred magnetization direction is transverse to the line direction in the sample plane [2]. This preference is due to strain relief in the nanoline across its width. Simulations of strain in these structures (Figure 1) have shed further light on the relation between the nanoline cross-section aspect ratio and strain relief, showing that strain is relaxed at the edges of the lines over a distance of about 1.5 times the film thickness. Therefore narrower lines show a greater magnetic anisotropy parallel to their width. Strain relief is even greater in the case of overetch into the copper substrate. Magnetic anisotropy data is being analyzed to understand how the net anisotropy of the nanolines agrees with theoretical models.



▲ Figure 1: Strain relief simulation for 100-nm-wide stripe of epitaxial Cu (50 Å)/Ni (206 Å)/Cu (20.6 Å) on Cu (~2000 Å)/Si. The top panel shows the mesh of the model while the lower panel shows the amount of strain relaxation, which is greater at the edges of the stripe.



▲ Figure 2: An SEM image of Cu (50 Å)/Ni (206 Å)/Cu (2000 Å)/Si nanolines with 500-nm-period. The facetted layer on the lines is the remains of the hard-etch mask.

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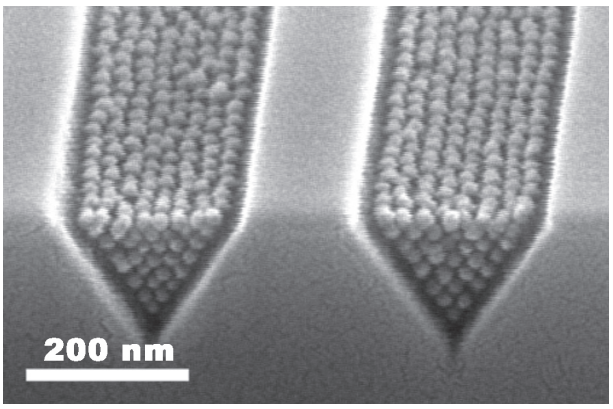
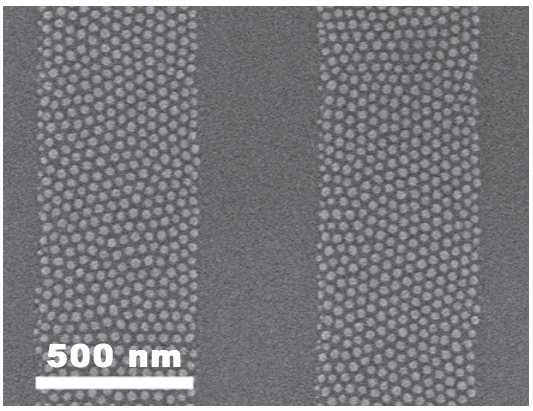
Templated Self-assembly of Block Copolymers for Nanolithography

C.A. Ross, H.I. Smith, F. Ilievski, V. Chuang, Y.S. Jung
Sponsorship: NSF, CMSE, Singapore-MIT Alliance, SRC

Large-area, periodic nanoscale structures are interesting for understanding fundamental material properties as well as for developing novel applications, such as the fabrication of magnetic media or contacts to nano-sized devices. Self-organizing systems provide a simple and low-cost method of fast fabrication of periodic nanoscale structures. One such system is the family of compounds called block-copolymers that we have been using. Block copolymers consist of two covalently bound polymer chains of chemically distinct polymer materials. The chains can self-assemble to form small-scale domains whose size and geometry depend on the molecular weights of the two types of polymer and their interaction[1]. The domains have a very uniform distribution of sizes and shapes. We have been using block copolymers as templates for the formation of structures such as magnetic particles, by selectively removing one type of domain and using the resulting template to pattern a nanostructured magnetic film. We have successfully applied this patterning process to the fabrication of magnetic dots from Co, NiFe[2] and multilayer CoFe/Cu/NiFe[2] films. One drawback of this technique is that the as-cast block copolymer forms a short-range ordered structure, whereas many applications require long-range ordered structures. It is therefore necessary to guide the microphase separation of the block copolymer by a process called templating. This can be done by using a substrate with shallow grooves as guides for a single layer of spheres[3] or cylinders that could be utilized in fabrication of nanorods and nanowires. Deep v-shaped grooves provide an interesting model for analyzing the ordering in 3 dimensions (Figure 1). Lastly, by combining this technique with nanoimprint lithography (Figure 2), we can achieve large-scale alignment and avoid additional steps for removal of the guiding template.



▲ Figure 1: Self-assembled block copolymer in a v-shaped groove. For imaging, one of the blocks was removed by oxygen plasma etching to reveal the structure of the other block. The number of rows of spheres increases in a quantized manner from the bottom up (one row of spheres, then two, etc.) Half-spheres and other transitions do not form.



▲ Figure 2: Initial results in templated block copolymers using nanoimprint lithography. A 1-μm- period mold was pressed into a thin layer of block copolymer on a flat substrate and both were annealed to induce the phase separation. The polymer was pushed out of regions where the mold was in contact with the substrate. If transferred into a magnetic layer, similar dots could be used as storage units for single bits in magnetic media. We are currently working on methods of improving the long-range order.

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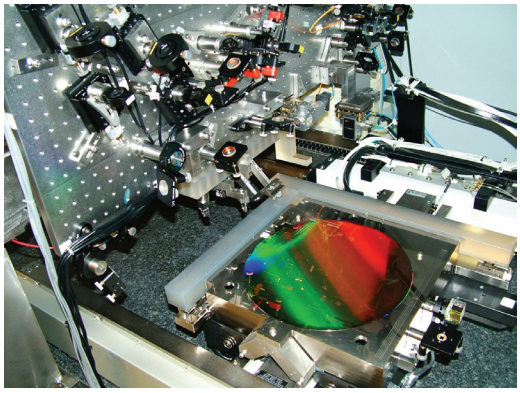
Scanning Beam Interference Lithography

M. Ahn, C.-H. Chang, R. Heilmann, J. Montoya, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA, Plymouth Grating Laboratory

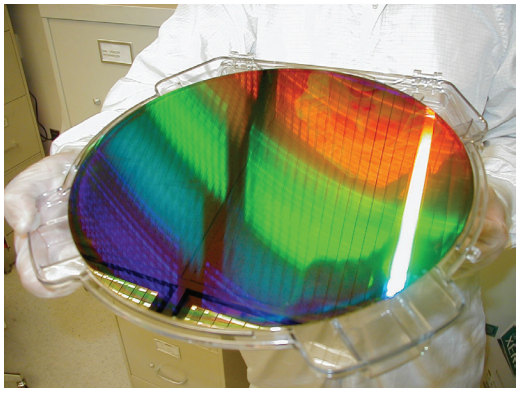
Traditional methods of fabricating gratings, such as diamond tip ruling, electron and laser beam scanning, or holography, are generally very slow and expensive and result in gratings with poor control of phase and period. More complex periodic patterns, such as gratings with chirped or curved lines, or 2D and 3D photonic patterns, are even more difficult to pattern. This research program seeks to develop advanced interference lithography tools and techniques to enable the rapid patterning of general periodic patterns with much lower cost and higher fidelity than current technology.

Interference lithography (IL) is a maskless lithography technique based on the interference of coherent beams. Interfering beams from an ultra-violet laser generates interference fringes which are captured in a photo-sensitive polymer resist. Much of the technology used in modern IL practice is borrowed from technology used to fabricate computer chips. Traditional IL methods result in gratings with large phase and period errors. We are developing new technology based on interference of phase-locked scanning beams, called scanning beam interference lithography (SBIL). The SBIL technique has been realized in a tool called the MIT Nanoruler, which recently won an R&D 100 award (Figure 1). Large gratings can be patterned in a matter of minutes with a grating phase precision of only a few nanometers and a period error in the ppb range (Figure 2).

Current research efforts seek to generalize the SBIL concept to pattern more complex periodic patterns, such as variable period (chirped) gratings, 2D metrology grids, and photonic patterns [1]. Important applications of large, high fidelity gratings are for high-resolution x-ray spectroscopes on NASA x-ray astronomy missions, high energy laser pulse compression optics, and length metrology standards. We are in the process of a major upgrade of the Nanoruler optical and mechanical system which will allow rapid variation and control of grating pitch and fringe orientation, which will enable a new mode of operation of the Nanoruler that we call variable-period SBIL.



▲ Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.



▲ Figure 2: A 300mm-diameter silicon wafer patterned with a 400-nm-period grating by the Nanoruler. The grating is diffracting light from the overhead fluorescent bulbs.

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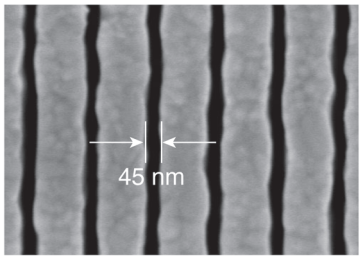
Nanofabricated Reflection and Transmission Gratings

M. Ahn, C.-H Chang, R. Heilmann, J. Montoya, Y. Zhao, M.L. Schattenburg
Sponsorship: NASA

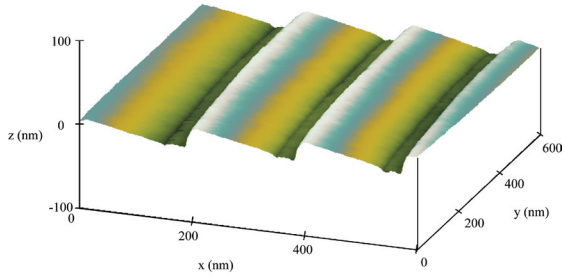
Diffraction gratings and other periodic patterns have long been important tools in research and manufacturing. Diffraction is due to the coherent superposition of waves—a phenomena with many useful properties and applications. Waves of many types can be diffracted, including visible and ultraviolet light, x-rays, electrons and even atom beams. Periodic patterns have many useful applications in fields such as optics and spectroscopy, filtering of beams and media, metrology, high-power lasers, optical communications, semiconductor manufacturing, and nanotechnology research in nanophonics, nanomagnetics and nanobiology.

The performance of a grating is critically dependant on the geometry of individual grating lines. Lines can have rectangular, triangular or other geometries, depending on the application. High efficiency requires control of the geometric parameters which define individual lines, e.g., width, height, smoothness, sidewall angle, etc., in the nanometer or even sub-nanometer range. For some applications control of grating period in the picometer to femtometer range is critical. Traditional methods of fabricating gratings, such as diamond tip ruling, electron and laser beam scanning, or holography, generally result in gratings which fall far below theoretical performance limits due to imperfections in the grating line geometry. The main goal of our research is to develop new technology for the rapid generation of general periodic patterns with control of geometry measured in the nanometer to sub-nanometer range in order to achieve near-theoretical performance and high yields.

Fabrication of gratings is generally accomplished in two main steps, (1) lithographic patterning into a photosensitive polymer resist, followed by (2) pattern transfer. A companion research program in this report entitled "Scanning Beam Interference Lithography" (previous page) describes progress in advanced grating patterning. In this abstract we report on research in pattern transfer technology. Development of a variety of grating geometries and materials is ongoing. Advanced gratings have been fabricated for 10 NASA missions, and further advances are sought for future missions [1]. Figure 1 depicts a gold wire-grid transmission grating designed for filtering deep-UV radiation for atom telescopes, while Figure 2 depicts a nano-imprinted sawtooth reflection grating for x-ray spectroscopy.



▲ Figure 1: Scanning electron micrograph of a deep-UV blocking grating used in atom telescopes on the NASA *IMAGE* and *TWINS* missions. The grating blocks deep-UV radiation while passing energetic neutral atoms.



▲ Figure 2: AFM image of 200-nm-period nano-imprint grating with 7° blaze angle developed for the NASA *Constellation X* mission. The groove surfaces are extremely smooth with a RMS surface roughness of <0.2 nm.

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Nanometrology

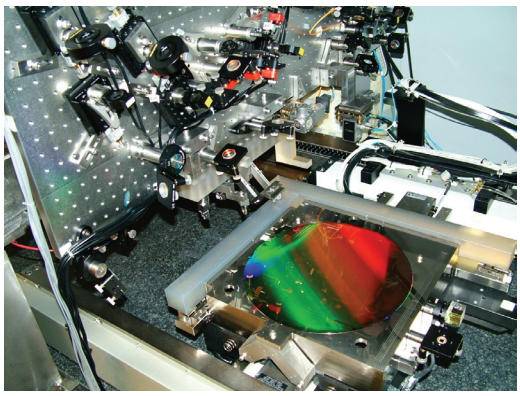
R. Heilmann, J. Montoya, Y. Zhao, D. Trumper, M.L. Schattenburg
Sponsorship: NSF

Manufacturing of future nanodevices and systems will require accurate means to pattern, assemble, image and measure nanostructures. Unfortunately, the current state-of-the-art of dimensional metrology, based on the laser interferometer, is grossly inadequate for these tasks. While it is true that when used in carefully-controlled conditions interferometers can be very precise, they typically have an accuracy measured in microns rather than nanometers. Achieving high accuracy requires extraordinarily tight control of the environment and thus high cost. Manufacturing at the nanoscale will require new technology for dimensional metrology which enables sub-1 nm precision and accuracy in realistic factory environments.

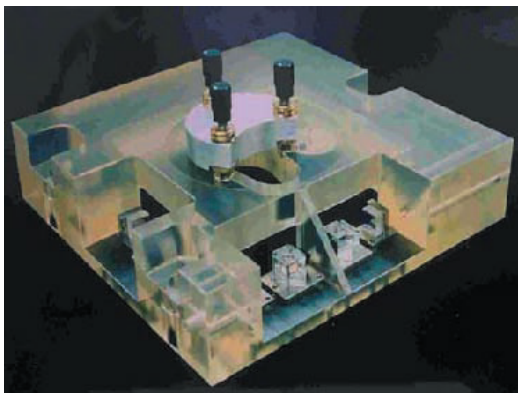
A recently formed MIT-UNC–Charlotte team is developing new metrology technology based on large-area grating patterns that have long-range spatial-phase coherence and ultra-high accuracy. Our goal is to reduce errors in gratings by 10-100 times over the best available today. These improved gratings can be used to replace interferometers with positional encoders to measure stage motion in a new nanomanufacturing tools, and to calibrate the dimensional scales of existing nanofabrication tools. This increased precision and accuracy will enable the manufacturing of nanodevices and systems that are impossible to produce today. Improved dimensional accuracy at the nano-to-picometer scale will have a large impact in many nanotechnology disciplines including semiconductor manufacturing, integrated optics, precision machine tools and space research.

As part of this effort, we will utilize a unique and powerful tool recently developed at MIT called the nanoruler that can rapidly pattern large gratings with a precision well beyond other methods. Another unique high-precision tool, the UNCC-MIT-built sub-atomic measuring machine (SAMM), is being brought to bear to research new ways to quantify and reduce errors in the gratings.

Recent work at MIT is focused on improving the thermal controls in the Nanoruler lithography enclosure and developing an improved interferometer system to reduce errors in the stage metrology frame. At UNCC the SAMM is undergoing extensive refurbishment and improvements designed to boost interferometer accuracy.



▲ Figure 1: Photograph of the Nanoruler lithography and metrology system built by MIT students. This unique tool is the most precise grating patterning and metrology system in the world.



▲ Figure 2: Photograph of reference block/sample holder for the Sub-Atomic Measuring Machine at the University of North Carolina – Charlotte.

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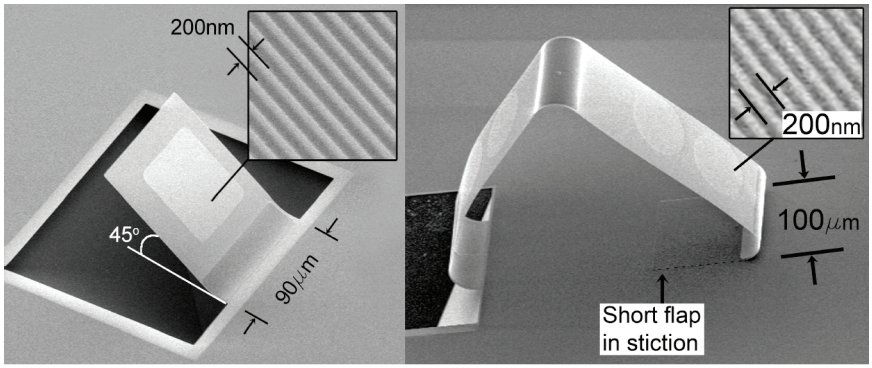
Building Three-dimensional Nanostructures via Membrane Folding

W.J. Arora, A.J. Nichol, G. Barbastathis, H.I. Smith
Sponsorship: ISN

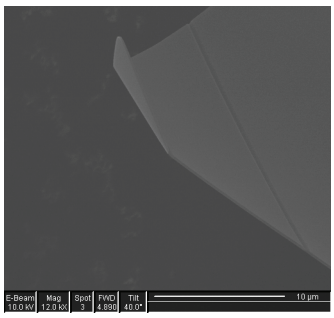
Nanostructured Origami™ describes a method of manufacturing three-dimensional (3D) nanostructures on a silicon wafer. Nanometer-scale structures are best fabricated with various two-dimensional (2D) lithography techniques. This project addresses the problem of building 3D structures using only 2D lithography. The general method of the Nanostructured Origami™ approach involves three steps: lithographically define micrometer-scale membranes and hinges; lithographically pattern nanostructures on these membranes; and release the membranes and actuate the hinges to fold into a 3D shape. Presently, we envision this technology to be well suited for fabrication of 3D photonic crystals and 3D diffractive optical devices.

We have developed a process to fold thin membranes of silicon nitride using stressed chromium hinges [1]. To date, these membranes have been patterned with gratings prior to being folded into 3D. However, arbitrary nanoscale features can be etched into or deposited onto the membranes. Experimental results are shown in Figures 1 and 2.

Current work focuses on reducing the radius of the folds. With the stressed chromium metal approach, we have demonstrated 30-μm-radius folds and by thinning the membrane at the hinge area, we predict that it is possible to achieve 5-μm-radius folds. However, it is desirable to have fold radii on the order of the membrane thickness, usually 1μm or less. We are developing a new folding approach that uses the stress gradient created by ion implantation. The maximum strain generated is proportional to the implanted ion concentration, which can be much larger than that generated by the stressed chromium. Additionally, as the ion implantation takes place, the hinge area is sputtered and can be controllably thinned. The combination of these effects results in a much smaller radius. Preliminary experimental results are shown in Figure 2.



▲ Figure 1: a) A 200-nmSiN$_x$ membrane folded to 45° with a grating etched into the center. The grating was patterned by interference lithography and the period is 200 nm. The membrane is folded near the base by a strip of chromium. The fold radius is 34 μm. b) Three identical hinges (63-μm long) each folded to 120^0 to form a triangular shape out of a long SiN$_x$ strip. The membranes are patterned with interference lithography inside the circular regions. The fold radius is 32 μm.



▲ Figure 2: Single pixel lines written with a focused ion beam source (Ga$^+$ ions, 30keV) folded a 200-nm-thick SiN membrane with a 500-nm radius. The folding strongly depends on the implanted dose; the line on the right had half the dose of the folded line on the left.

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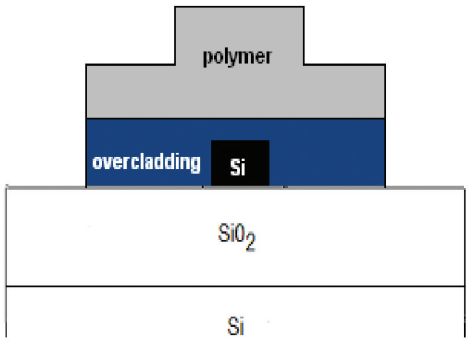
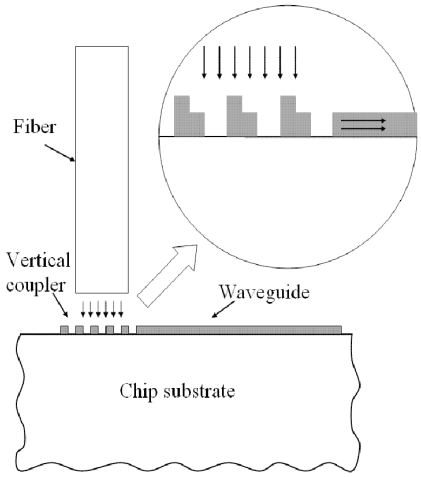
Fabrication of Nanostructured Optical Fiber-to-Chip Couplers

R. Barreto, M. Defosseux, T. Barwicz, A.M. Khilo, M. Fan, M.A. Popovic, P.T. Rakich, M. Dahlem, E.P. Ippen, F.X. Kaertner, H.I. Smith
Sponsorship: Pirelli S.p.A

Efficient fiber-to-chip coupling is a significant problem for high-index contrast micro-photonics due to the large difference in size and refractive index between the core of an optical fiber (several microns in diameter) and the core of a high-index-contrast waveguide (less than a micron wide). An efficient fiber-to-chip coupler is thus needed to match the mode of the fiber and transform it to a propagation mode inside the chip waveguide while minimizing signal loss. Our research simultaneously investigates and fabricates two different designs to accomplish the coupling. In the first design, called a horizontal coupler, a large polymer waveguide sits on a small silicon waveguide whose width tapers from 30 to 450 nm. This way, light is gradually transferred from the polymer waveguide to the silicon waveguide over the length of the tapered region. Figure 1 shows a cross-sectional area of the horizontal coupler. Fabrication is done on silicon-on-insulator wafers, so that the buried oxide functions as an under-cladding and prevents optical modes from reaching into the substrate. An over-cladding layer is also added to the structure to make the coupler compatible with other photonic devices, such as micro-ring-based reconfigurable optical add-drop filters. The second design, the vertical coupler, is based on a grating array composed of nanoscale tooth-sets that allow coupling from a vertically oriented fiber to a horizontally oriented waveguide. We are now demonstrating this concept using silicon-rich silicon nitride waveguides. Figure 2 shows a sketch of the vertical coupler design under fabrication. The minimum feature size reaches ~ 100 nm.



▲ Figure 1: Cross section of horizontal coupler.



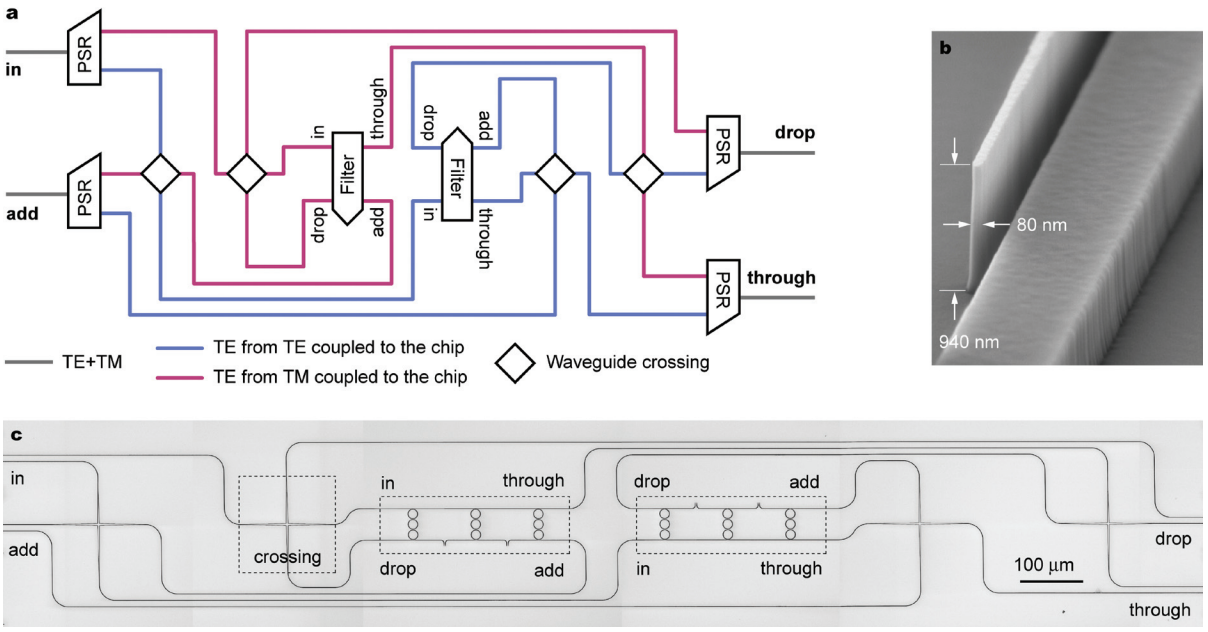
▲ Figure 2: Sketch of vertical coupler.

Polarization-insensitive Optical Add-drop Multiplexers in Silicon Nitride

T. Barwicz, M.R. Watts, M.A. Popovic, P.T. Rakich, E.P. Ippen, F.X. Kaertner, H.I. Smith
Sponsorship: Pirelli S.p.A

Microphotonics promises to revolutionize optics through miniaturization and dense integration of optical elements on planar surfaces. Of particular interest are microphotonic devices that employ high refractive-index contrast (HIC). These devices have dimensions on the order of the optical wavelength and functionality often not achievable with macro-scale devices. A long-standing criticism of HIC microphotonic devices, however, is their inherent sensitivity to polarization: they respond differently to light polarized along different axes. Since the polarization state changes randomly in optical fibers, HIC microphotonic devices are incompatible with the optical fibers necessary to connect them to the outside world.

In the Nanostructures Laboratory, we have developed nanofabrication techniques that allow the realization of microphotonic devices with unprecedented accuracy [1]. These techniques are based on scanning e-beam lithography and allow us to fabricate microring filters of unprecedented optical performance. Here, we overcome another major obstacle: sensitivity to polarization. We apply an integrated polarization-diversity scheme to render the optical response of microring filters insensitive to polarization. An optical add-drop multiplexer was realized and the polarization-dependent loss reduced to a remarkable average of 1 dB. Figure 1 presents the optical circuit diagram implemented and electron micrographs of the structure . The waveguides are based on silicon-rich silicon nitride and the critical dimensions vary from 70 to 3000 nm across the structure. The average waveguide widths of the 18 microrings forming the add-drop multiplexer are matched to 0.15 nm. The aspect ratio of the tallest and thinnest structures reaches 12 to 1.



▲ Figure 1: (a) Optical circuit required to obtain a polarization insensitive optical response from polarization sensitive components. The acronym PSR stands for polarization splitter and rotator. The two filters shown in the schematic are identical. (b) Electron micrograph of the onset of the polarization splitter and rotator. (c) Electron micrograph of the middle part of the circuit. The polarization splitters and rotators are not shown and extend to the right and the left of the micrograph. The grayscale was inverted to allow the fine lines to be readable when printed.

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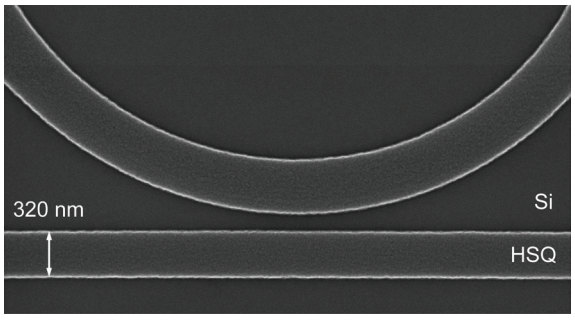
Nanofabrication of Reconfigurable Optical Add-drop Multiplexers in Silicon

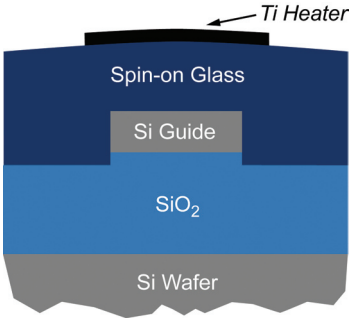
T. Barwicz, M.A. Popovic, F. Gan, P.T. Rakich, M. Dahlem, E.P. Ippen, F.X. Kaertner, H.I. Smith
Sponsorship: Pirelli S.p.A

Reconfigurable optical add-drop multiplexers (ROADMs) are key components of modern optical networks. Data in optical fibers is carried at numerous wavelengths, which are also called channels. The ROADMs allow the rerouting (drop) of a subset of the data channels traveling in an optical fiber and replacing these with new data streams (add) that will be carried in the fiber at the previously rerouted wavelengths. "Reconfigurable" in ROADM indicates that the subset of dropped channels can be changed on the fly while the ROADM is in operation.

In our previous work, we developed nanofabrication techniques of unprecedented accuracy that allowed us to demonstrate in silicon-rich silicon nitride the most advanced microring filters reported [1-2]. In this work, we employ silicon microrings to take advantage of the high thermo-optical coefficient of silicon, allowing wide tuning of the wavelengths of operation of the ROADM with integrated heaters. Figure 2 presents a cross-sectional diagram of our implementation of a silicon waveguide with an integrated heater. Line-edge roughness is of critical concern in silicon waveguides as it translates into significant optical propagation loss via scattering of the guided mode. We found that the smoothest waveguides are obtained using hydrogen silsesquioxane (HSQ) as an e-beam resist and an etch-mask. Figure 1 presents an electron micrograph of a coupling region between a microring and a bus waveguide defined in HSQ. The patterning is based on scanning electron-beam lithography.



▲ Figure 1: Top-view electron micrograph of a coupling region defined in HSQ. Line-edge smoothness is critical for Si waveguides. The patterning is based on scanning electron beam lithography. The minimum feature size required is ~100 nm and must be controlled to ~ 5 nm.



▲ Figure 2: Cross-sectional schematic of a silicon waveguide with an integrated titanium heater. Spin-on glass is used for the upper cladding of the waveguide to allow self-planarization and to avoid filling problems in narrow gaps.

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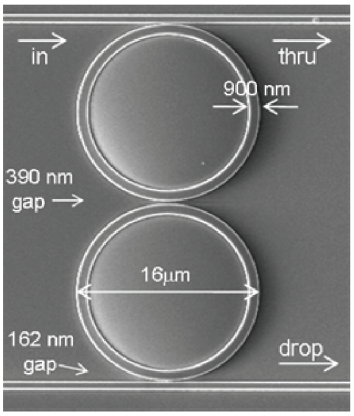
Nanofabrication of Optical Microring Filter Banks for Ultra-fast Analog-to-Digital Converters

C.W. Holzwarth, T. Barwicz, M.A. Popović, P.T. Rakich, E.P. Ippen, F.X. Kärtner, H.I. Smith
Sponsorship: DARPA

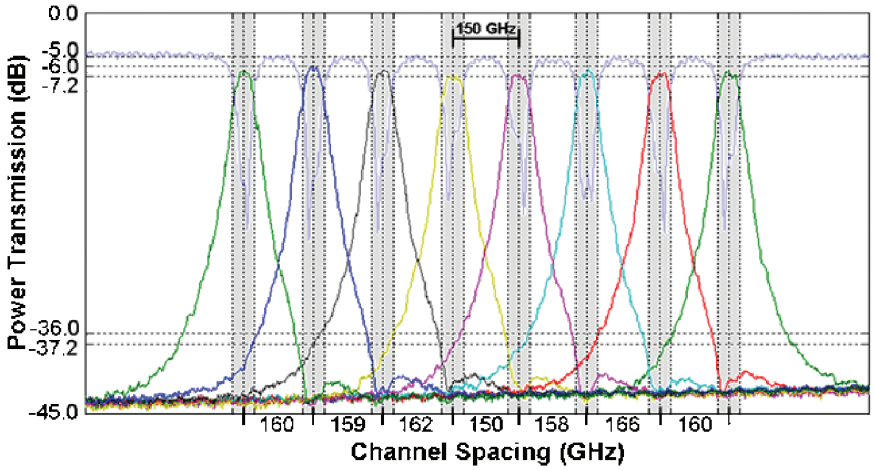
Microphotonic filter banks are an essential part of many proposed integrated photonic systems including ultra-fast analog-to-digital converters. Recent progress in designs and nanofabrication techniques for microring-resonators in high-index-contrast (HIC) materials have made possible the wide spectral spacing between resonances and low loss required for real world applications [1]. Achieving accurate resonant-frequency spacing of microring-filters is critical for these devices. In the NanoStructures Laboratory we have developed fabrication techniques based on scanning electron beam lithography (SEBL), that enables accurate control of the resonant-frequency spacing of HIC microring-resonator filter banks.

The resonant wavelength of a microring-resonator filter is given by $m*\lambda=n_{eff}*2\pi*R$, where λ is the resonant wavelength, n_{eff} is the effective index of refraction, R is the ring radius, and m is an integer. The effective index is controlled lithographically by controlling the width of the ring waveguide. Although it is simple to change both the width and the radius of the ring in the SEBL layout, this change is limited to discrete jumps corresponding to the step size of the SEBL system. In order to have 1 GHz control of the resonant frequency for the designed filters, the SEBL systems would need a step size of 30 pm. In our process this limitation of discrete step size is overcome by modulating the electron-beam dose to precisely control the width of the ring waveguide [2].

In our experiments second-order microring-resonator filters fabricated in silicon-rich silicon nitride were used in the microring filter banks (Figure 1a). Using dose modulation, eight-channel filter banks with channel spacing ranging from 90 to 180 GHz were fabricated and tested (Figure 1b). The results demonstrate that we can accurately control a 2.7 nm change in average width of the ring waveguide to 0.11 nm, despite a 6 nm step size in the SEBL system.



(a)



(b)

▲ Figure 1: a) Scanning electron micrograph of a fabricated second-order microring-resonator filter that has a 20 nm free spectral range, 50 GHz bandwidth and 1.5 ± 0.5 dB drop loss. b) Measured response of an eight-channel filter bank based on second-order microring-resonators with a target channel spacing for 150 GHz. The actual average channel spacing measured is 159 GHz (σ=5 GHz) and channel crosstalk is less than 30 dB.

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[2] T. Barwicz, M.A. Popović, P.T. Rakich, M.R. Watts, F.X. Kaertner, E.P. Ippen, H.I. Smith, "Resonance-frequency control of high-index-contrast microphotonic cavities at fabrication," *Integrated Photonics Research and Applications 2006*, invited paper JWA3.

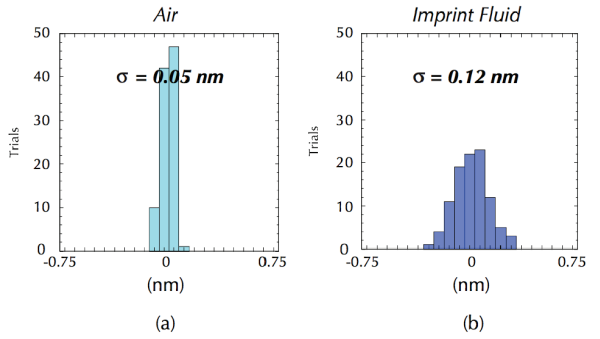
Imprint Lithography with Multilevel Alignment via Interferometric-Spatial-Phase Imaging

E.E. Moon, H.I. Smith
Sponsorship: Molecular Imprints, Inc.

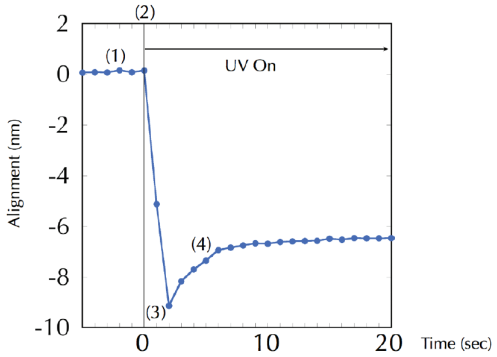
A critical obstacle to widespread industrial acceptance of imprint lithography is the lack of capability for multilevel, nanometer-scale overlay. In journal articles [1-2] we described an alignment detection scheme, called interferometric-spatial-phase imaging (ISPI), which encodes alignment in the spatial phase disparity of complementary interference fringes, observed with oblique-incidence, long-working-distance, darkfield optical microscopes. We have applied ISPI to step-and-flash imprint lithography (S-FIL), in which alignment is actively measured and corrected with imprint fluid filling the template-substrate gap.

In S-FIL, it is desirable to use a shallow phase grating as the alignment mark, which raises the issue of ISPI fringe contrast. Fringe contrast with a fused silica phase grating in an imprint fluid is reduced to 12% of the fringe contrast with air in the template-substrate gap, as predicted by two-dimensional finite-difference time-domain (FDTD) simulations and confirmed by experiment. Despite the low fringe contrast, experimental data (Figure 1) indicate the ability of ISPI to achieve sub-nanometer alignment detectivity under such conditions, the most stringent typically encountered in imprint lithography.

Figure 2 illustrates the ability of ISPI to effect dynamic alignment control throughout the S-FIL imprint process. The data shows an initial condition with alignment well below 1 nm. Alignment is disturbed by a mechanical impulse from opening of the UV shutter, but ISPI can observe and correct such disturbances, which would usually pass unnoticed. We believe these experiments, among others, indicate that ISPI is uniquely advantaged for application to S-FIL and other forms of imprint lithography.



▲ Figure 1: Alignment detectivity of ISPI with (a) air in the template-substrate gap (σ = 0.05 nm), and (b) imprint fluid in the gap (σ = 0.12 nm). Detectivity is reduced in the stringent case of phase gratings on the template, used with an imprint fluid of similar index of refraction, but remains within the sub-nanometer range. The template-substrate gap was mechanically locked during the experiment.



▲ Figure 2: Plot of ISPI alignment data (1) before exposure, (2) at the instant the shutter to the UV lamp opens, (3) during misalignment caused by a mechanical shock transmitted from the UV lamp to the template, and (4) during correction of misalignment, until crosslinking solidifies the imprint material. The experiment demonstrates the ability of ISPI to detect and identify sources of misalignment on the nanometer level, as well as a limited ability to re-align during crosslinking of the imprint material. Improvements are readily achievable with increased feedback bandwidth.

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[2] E.E. Moon, M.K. Mondol, P.N. Everett, and H.I. Smith, "Dynamic alignment control for fluid-immersion lithographies using interferometric-spatial-phase imaging," *J. Vac. Sci. Technol. B*, vol. 23, p. 2607, 2005.

Interference Lithography

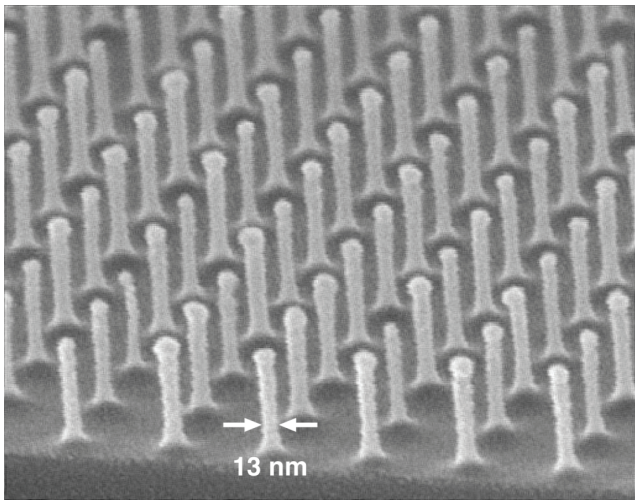
T.B. O'Reilly, T. Savas, H.I. Smith
Sponsorship: Internal funds

Interference lithography (IL) is a means to produce periodic structures using the coherent interference of light. Typically, light from a source is divided and recombined, forming a periodic intensity pattern that can be used to expose a photosensitive substrate. The NanoStructures Lab (NSL) has been developing interference lithography systems since the mid 1970s, and operates a range of tools capable of writing gratings, grids, and other periodic structures with periods as fine as 100 nm; these structures are used in a wide variety of research areas.

Two of the NSL's IL systems use 325 nm wavelength HeCd lasers. The most flexible and widely used of these systems is known as the Lloyd's mirror. This system is a half Mach-Zehnder interferometer that is easily configured to write patterns with periods from 170 nm to several microns. A second system at the same wavelength in a full Mach-Zehnder configuration can write gratings over larger areas than the Lloyd's mirror system, but is less flexible. Finally, the NSL operates an achromatic interference lithography (AIL) system. This system uses a 193 nm excimer laser and can write patterns with periods of 100 nm, as shown in Figure 1. This AIL system uses phase gratings to split and recombine the light, and can form high-contrast fringe patterns whose area is not dependent on the spatial or temporal coherence of the source.

Gratings produced by the Lloyd's mirror have been used to cut carbon nanotubes, guide the assembly of nanoparticles for templated self-assembly, study the behavior of strained-silicon wafers, fabricate templates for imprint lithography, and more. The full Mach-Zehnder system has been used to study in-plane distortion of silicon nitride membranes and to create super-prisms and super-collimators based on 2D photonic crystals. The AIL system has been used to create free-standing gratings used in atom-beam interference experiments and EUV spectroscopy.

In addition, the NSL collaborates with the Space Nanotechnology Laboratory, which operates a Mach-Zehnder IL system and the Nanoruler, an IL system that can write high-quality gratings over areas larger than 300 mm in diameter.



▲ Figure 1: Scanning electron micrograph of a 100 nm-period grid, exposed in PMMA on top of an antireflection coating and transferred into Si by reactive ion etching.

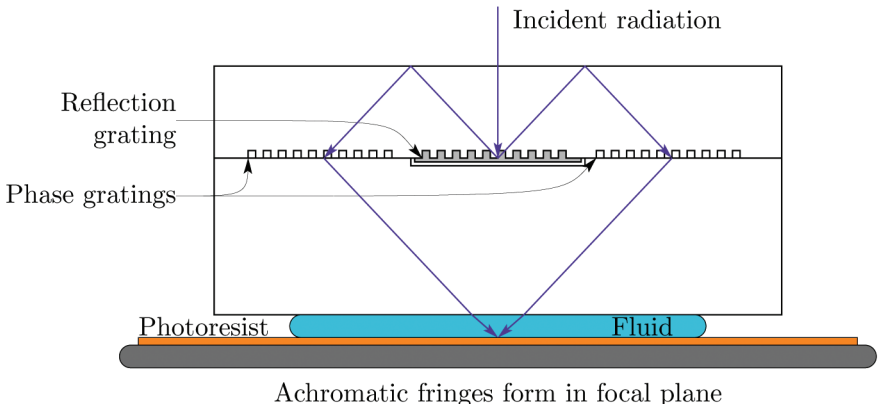
Immersion-Achromatic-Interference Lithography

T.B. O'Reilly, M. Walsh, T. Savas, H.I. Smith
Sponsorship: Singapore-MIT Alliance

Interference lithography is a means of using the coherent interference of light to create periodic structures. The period of the pattern written is determined by the interference angle, θ, and the wavelength, λ, according to the equation $P = \lambda/2n\sin(\theta)$. Since an upper limit exists for the interference angle (90°), to reduce the period below half the wavelength it is necessary to use an immersion fluid to reduce the effective wavelength of the light. The NanoStructures Lab is developing an immersion interference lithography system that will be capable of writing gratings with periods of 70 nm or even smaller.

The system under development, shown in Figure 1, is an achromatic grating interferometer similar to an existing system that is used to write 100 nm period gratings. In this system, diffraction gratings split and recombine light. The gratings are configured in such a way that contrast of the fringe pattern formed is not dependent on the spatial or temporal coherence of the source. Analysis of the proposed system has shown that it will be capable of writing gratings with periods as fine as 70 nm, over areas as large as the parent gratings, using water as the immersion fluid. Using higher-index immersion fluids, it should be possible to write patterns as fine as 60 nm.

Gratings produced by this system are likely to find application in areas such as atom interferometers and templated self-assembly. In addition, the system will be used to study the performance of photoresists and immersion fluids at very high numerical apertures.



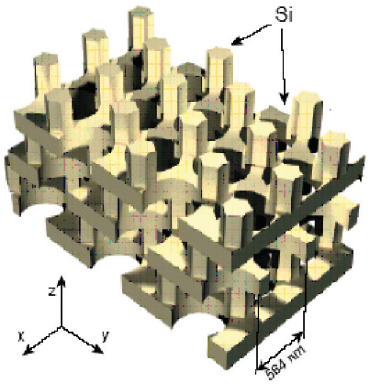
▲ Figure 1: Immersion grating-interference lithography system.

Three-dimensional Photonic Crystals by Membrane Assembly

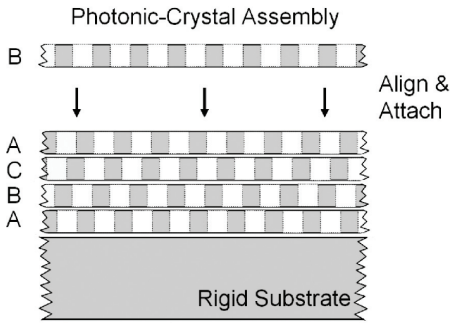
A. Patel, J.D. Joannopoulos, H.I. Smith
Sponsorship: NSF

A three-dimensional photonic crystal is a periodic structure in which back-diffraction prevents light within a given wavelength band (the bandgap) from propagating in any direction. A local deviation from perfect periodicity (a "defect") such as some missing material, i.e., a hole, or a local change in dimensions, can produce a photon trap or resonant cavity. Light cannot propagate through the photonic crystal but it can remain localized around the defect, leading to resonators of extraordinarily high Q. This phenomenon promises many practical applications, including single-photon sources and highly sensitive chemical detection. A line defect, such as a row of missing material, can serve as a lossless waveguide, leading to highly complex and functional photonic systems. Figure 1 [1] depicts a 3D photonic crystal with a very large omni-directional bandgap. In the past, we fabricated this type of structure using a layer-by-layer process composed of e-beam lithography followed by deposition and etch back [2]. We are replacing this tedious and error-prone process with layer-by-layer assembly of membranes that are pre-patterned using interference lithography, as depicted in Figure 2. Although this technique will require the development of entirely new membrane fabrication and assembly techniques, it should reduce the probability of error since the membranes are separately fabricated and inspected and assembled only at the final step.

Large area SiN membranes (1 cm x 1 cm), 350-nm thick, have been patterned with the appropriate 2D periodic structure. We are developing techniques for assembling such membranes with ~10 nm alignment accuracy. In the future Si membranes will be investigated. Ultimately we plan to assemble more than 20 layers in a 3D photonic crystal structure.



▲ Figure 1: A 3-D rendering of the photonic crystal structure to be fabricated. The picture depicts a crystal with 6 layers. Ultimately, we will assemble 20+ layers.



▲ Figure 2: Proposed membrane-assembly process for fabricating 3D photonic crystals.

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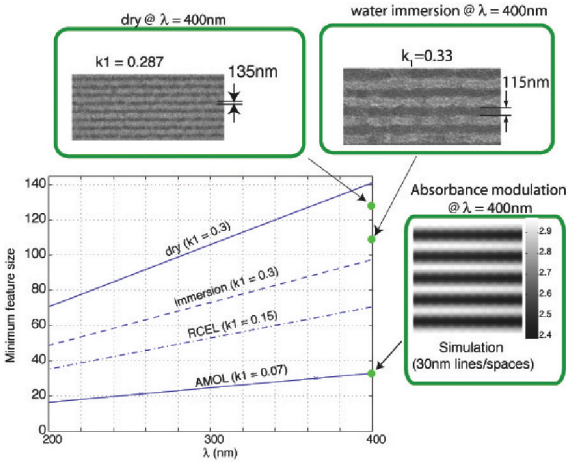
Absorbance-Modulation Optical Lithography

R. Menon, S. Tsai, H.I. Smith
Sponsorship: Internal funds

In the NanoStructures laboratory, we are developing an optical nano patterning technology that can push the resolution limits to sub-diffraction-limited regimes using photochromic molecules. Photochromic molecules are those that reversibly change their absorbance spectra upon irradiation [1]. By placing a thin photochromic layer on top of a traditional photoresist, coupled with a two-wavelength illumination, one can pattern sub-diffraction-limited features (~ $\lambda/13$) [2]. The first wavelength, λ_1, bleaches the photochromic layer, turning it transparent, while the second longer wavelength, λ_2, reverses this bleaching process. The two-wavelength scheme, which we call absorbance-modulation-optical lithography (AMOL), uses a focused beam at λ_1 and a ring-shaped beam at λ_2. As a result, the beam transmitted through the photochromic layer is compressed laterally.

Thus, AMOL has the potential to pattern 30 nm features at λ_1 = 400 nm. Compared to scanning electron beam lithography (SEBL), AMOL has the advantages of higher accuracy, higher throughput (via parallel beams [3]), non-damaging effects (for organic and other sensitive substrates), and a fundamentally simpler configuration.

Furthermore, it can be shown that if both isomers of the photochromic molecule are stable, the compression of the transmitted beam is dependent on the ratio of the intensities at λ_1 and λ_2, not on either one alone. This has the important practical implication that highly compressed beams may be created at low power densities. The scale of the compression of the transmitted beam is determined by the initial absorbance of the photochromic layer as well as the difference between the initial and final absorbances, i.e., the contrast of the absorbance modulation. Figure 1 shows the predicted resolution improvement achievable with AMOL.



◀ Figure 1: Resolution scaling with wavelength for different technologies. Note that AMOL has the potential to extend optical nano patterning to the sub-30-nm regime.

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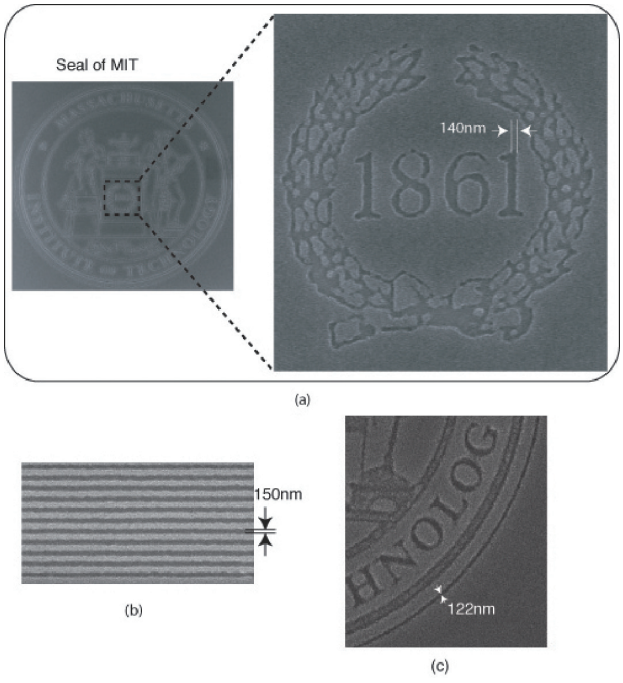
[3] R. Menon, A. Patel, D. Gil and H.I. Smith, "Maskless lithography," *Materials Today*, vol. 8, no. 2, pp. 26-33, Feb. 2005.

Zone-Plate-Array Lithography (ZPAL)

R. Menon, S. Tsai, H.I. Smith
Sponsorship: DARPA, NSF

Optical projection lithography (OPL) has been the key element in the technological progress of the semiconductor industry. In OPL, a fixed pattern on a photomask is imaged onto a photoresist-coated substrate by means of a complex and expensive optical system. Resolution-enhancement techniques used to print at the diffraction-limit often constrain the geometries of these patterns. Furthermore, OPL is inherently inflexible since the patterns once defined in the photomask cannot be changed. Obtaining a new set of photomasks is an expensive and time-consuming proposition. This requirement is a significant impediment in emerging applications, in which frequent experimentation and changes to pattern geometries are often essential to achieving the optimum design.

In order to address these issues, in the NanoStructures laboratory at MIT, we have developed an optical-maskless lithography called zone-plate-array lithography (ZPAL) [1] that uses a massively parallel array of tightly focused laser beamlets to create patterns of complex geometries in a dot-matrix fashion. The array of beamlets is created by an array of high-numerical aperture zone plates. The illumination of each zone plate is controlled by one pixel on an upstream spatial-light modulator. This technology is currently being commercialized by LumArray Inc. [2].



▲ Figure 1: Scanning electron micrographs of patterns created using ZPAL at an exposure wavelength of l = 400 nm.

REFERENCES:

[1] R. Menon, A. Patel, D. Gil, and H.I. Smith, "Maskless Lithography," *Materials Today*, pp. 26-33, Feb. 2005.
[2] LumArray [Online]. Available: http://www.lumarray.com

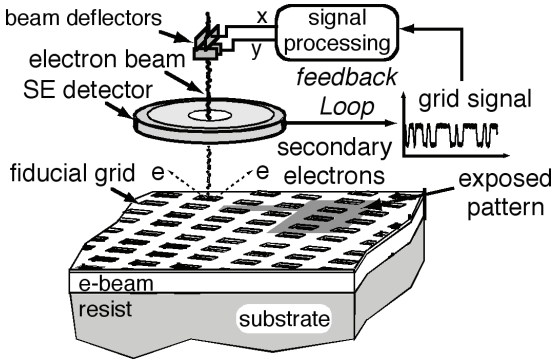
Spatial-phase-locked E-beam Lithography

H.I. Smith, F. Zhang, M. Mondol
Sponsorship: No external sponsor

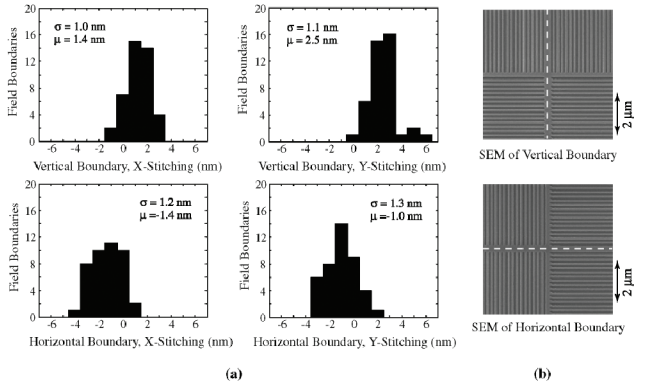
Our research in spatial-phase-locked electron-beam lithography (SPLEBL) is aimed at reducing pattern-placement errors in electron-beam-lithography systems to the 1nm level. Such high precision is essential for a variety of future lithographic applications. SPLEBL is currently the only approach capable of achieving such accuracy. As shown in Figure 1, SPLEBL uses a periodic signal, derived from the interaction of the scanning e-beam with a fiducial grid on the substrate, to continuously track the position of the beam while patterns are being written. Any deviation of the beam from its intended location on the substrate is sensed, and corrections are fed back to the beam-control electronics to cancel errors in the beam's position. In this manner, the locations of patterns are directly registered to the fiducial grid on the substrate.

The research effort focuses on developing the three critical components of SPLEBL: 1) the beam-position-detection algorithm [1], 2) a user-friendly-fabrication process for the fiducial grid [2], and 3) a beam-current-modulation scheme [3]. The last component is necessary for the SPLEBL-enabled tool to discriminate between non-exposed and exposed areas while enjoying a continuous feedback signal.

SPLEBL in its continuous-feedback mode has been implemented on a Raith150 scanning e-beam lithography system (an inexpensive system that provides sub-20-nm patterning resolution). In this implementation, a thin (<10 nm) metallic fiducial grid is placed on top of the e-beam resist. During exposure, a periodically varying secondary-electron (SE) signal is produced as a result of the interaction between the electron beam and the metal reference grid. Its limited thickness makes the grid layer essentially transparent to the primary electron-beam. The beam position is determined in real time by a detection algorithm based on Fourier technique. This implementation allowed the beam position to be monitored constantlyand corrected during exposure. Experimental results [1] shown in Figure 2 indicate that 1-nm-level placement accuracy is achievable with this technology.



▲ Figure 1: Schematic of the global-fiducial-grid mode of spatial-phase-locked electron-beam lithography. The periodic signal detected from the fiducial grid, which includes both X and Y components, is used to measure placement error, and a correction signal is fed back to the beam-deflection system.



▲ Figure 2: (a) Histograms showing x- and y-stitching measurements at all 84 field boundaries of 49 stitched fields. Spatial-phase locking has reduced the standard deviation of the stitching errors to below 1.3 nm. (b) Sample 200-nm period stitched grating patterns. The dashed line indicates the field boundary.

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[1] J.T. Hastings, F. Zhang, and H.I. Smith, "Nanometer-level stitching in raster-scanning e-beam lithography using spatial-phase locking," *J. Vac. Sci. Technol. B*, vol. 21, no. 6, pp. 2650-2656, Nov/Dec 2003.

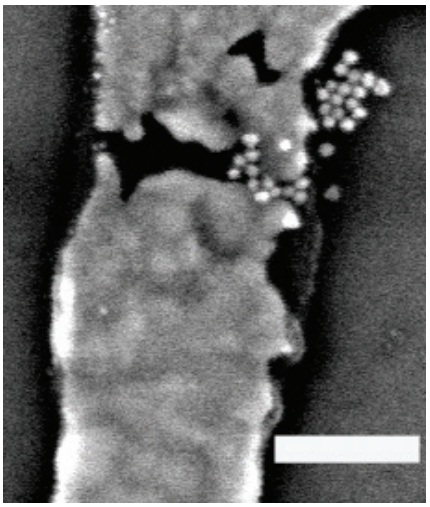
[2] F. Zhang, H.I. Smith and J.F. Dai, "Fabrication of high-secondary-electron-yield grids for spatial-phase-locked electron-beam lithography," *J. Vac. Sci. Technol. B*, vol. 23, no. 6, pp. 3061-3064, Nov/Dec 2005.

[3] F. Zhang and H.I. Smith, "Partial blanking of an electron beam using a quadrupole lens," in *J. Vac. Sci. Technol. B*, vol. 23, no. 1, pp. 133-137, Jan/Feb 2005.

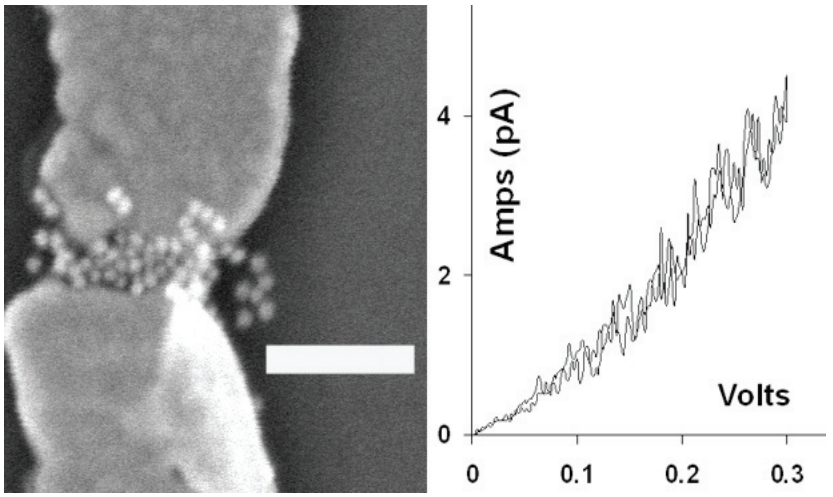
Controlled Assembly of 20-nm-diameter Gold Nanoparticles into Nanogaps using AC Dielectrophoresis

R. Barsotti, M. Vahey, R. Wartena, J. Voldman, Y. Chiang, F. Stellacci
Sponsorship: Singapore-MIT Alliance, NDSEG Fellowship

The directed assembly of nano-objects into specific locations will allow for the fabrication of electronic devices that utilize the unique properties of the nano-objects. One method to assemble nano-objects into gaps uses the dielectrophorectic (DEP) force via the application of an alternating field [1-2]. Here, we demonstrate the assembly of gold nanoparticles into nanogaps (15-100 nm in width) that are fabricated by electron beam lithography. Nanoparticle assembly is achieved by applying an AC field across the nanogaps after a drop of an aqueous solution of gold nanoparticles has been placed over the device. The assembly is characterized by SEM, AFM, and post-assembly electrical measurements. The number of nanoparticles that assemble in the gap is studied as a function of the applied AC field, the concentration of the nanoparticle solution, and assembly time with a goal of the assembly of a single particle in a gap. Pre-assembly modification of the gold surfaces using a dithiol self-assembled monolayer results in a significant increase in DEP assembly as the surface-bound thiol groups bind the gold particles to the substrate. Theoretical modeling of the dielectrophorectic force on nanoparticles in comparison to their thermal motion is used to predict the experimental conditions for the assembly of a single particle.



▲ Figure 1: An SEM image of assembly of citrate-stabilized 20-nm-diameter gold particles by the application of a 2-V_{pp}, 1-MHz alternating field across a 23-nm gap for 120 seconds. A solution concentration of 7 * 10^{10} particles/ml was used for this assembly. Scale bar=200 nm.



▲ Figure 2: An SEM image showing increased nanoparticle assembly at 3 V_{pp} for 120 seconds. Scale bar=200 nm. The IV characteristics of the assembly show a 100-fold increase in conductance after particle assembly. The electrical characteristics remain stable after 20 voltage sweeps.

REFERENCES

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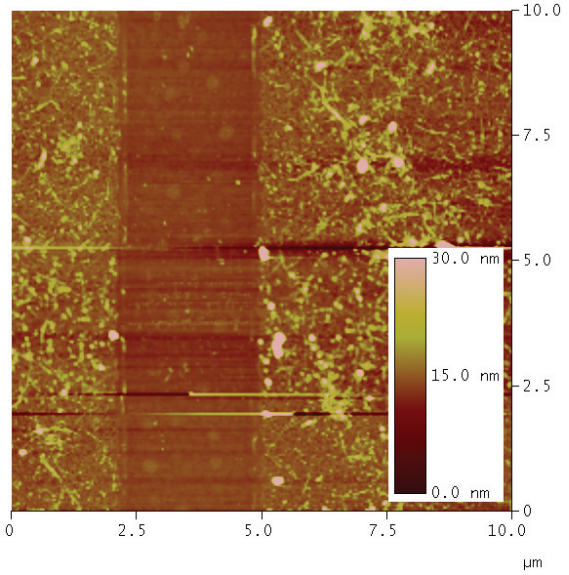
[2] S.I. Khondaker and Z. Yao, "Fabrication of nanometer-spaced electrodes using gold nanoparticles," *App. Phys. Lett.*, vol. 81, no. 24, pp. 4613-4615, 2002.

Carbon Nanotube Assembly for Interconnect and Device Applications

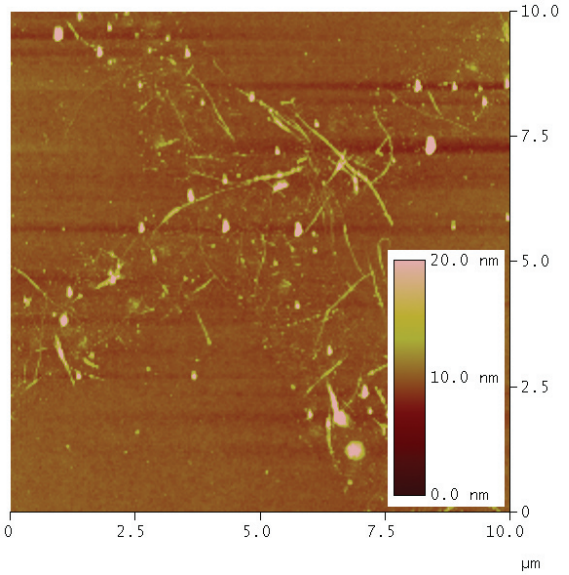
T.M. Wu, B. Long, B. Wunsch, F. Stellacci
Sponsorship: MARCO IFC

Carbon nanotubes (CNTs) are materials with potentially useful electronic, thermal, and mechanical properties. Our current work with CNTs focuses on applications in the microelectronics arena, especially use as a substitute for conventional metal interconnects. As interconnect dimensions shrink, surface scattering begins to contribute dramatically to line resistance, leading to power loss and signal delay. The CNTs, with length-independent conductivity due to ballistic transport, offer a potential solution.

We are investigating currently methods to accurately and precisely construct CNT structures on surfaces via assembly from a suspension or solution. We use a series of chemical and physical interactions to direct the assembly of CNTs onto desired locations on a substrate. In the chemical sense, we can tune the interaction between CNTs and a surface by selectively growing polar and non-polar monolayer patterns on the substrate. In the physical sense, we can pattern the growth of the monolayer and of the CNT deposition by lithographic methods such as electron-beam writing and dip-pen nanolithography. By combining these two approaches, we hope to develop an integrated system for the massively parallel and accurate assembly of CNTs on a surface.



▲ Figure 1: Chemically-directed assembly of CNTs on polar and non-polar silane monolayers. The CNTs assemble on the polar monolayers (sides) and are repelled by the nonpolar monolayer (stripe).

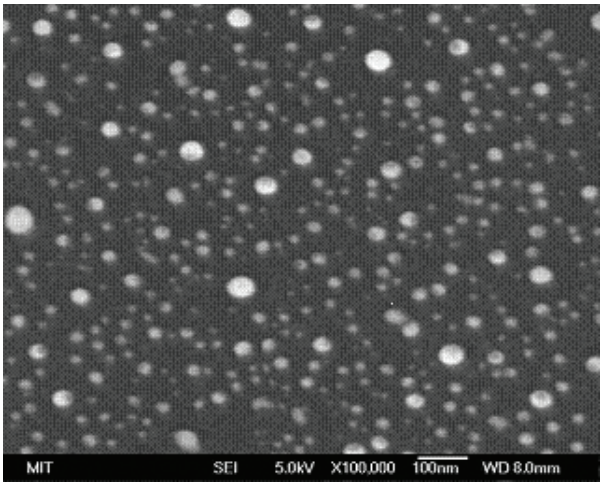


▲ Figure 2: Lithographically-directed assembly of CNTs on a polar silane monolayer. The resist was patterned with electron beam lithography and served as a liftoff mask for CNT deposition from solution.

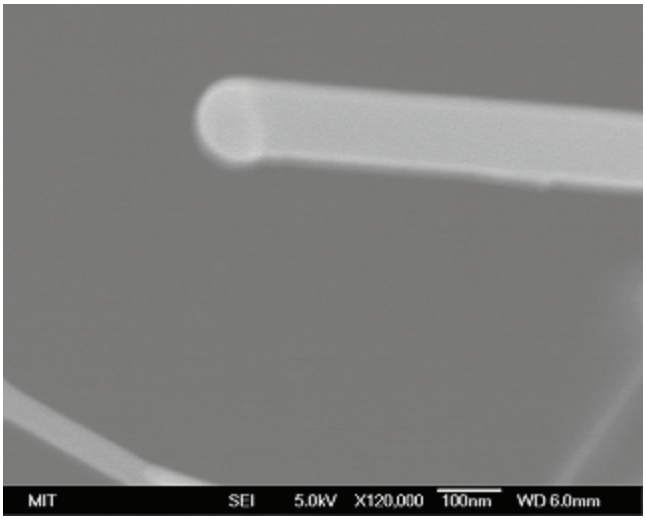
Catalyst Engineering and Nanowire Growth Mechanisms

S. Boles, O. Nayfeh, E.A. Fitzgerald, D.A. Antoniadis, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

The use of semiconductor nanowires for electronic and photonic applications has generated a great deal of interest in recent years, due to their mechanical, electronic, and photonic properties. A great deal of effort has been focused on demonstrating the unique properties of nanowires, while there has been less interest in developing techniques that allow growth of functional arrays of nanowires. Our research focuses on creating high-density nanowire arrays by controlling the metallic dots that catalyze wire growth through the vapor-liquid-solid mechanism. Our early work has focused on the development of a baseline growth process using disordered catalyst arrays, as show in Figure 1. Future work will involve growth on catalysts ordered through templated self-assembly techniques. Our ultimate goal is to grow ordered arrays that can be included in electronic and photonic device structures that will allow detailed correlations among the techniques of growth and the properties of nanowires.



▲ Figure 1: Au particles produced by dewetting of 0.3nm-thick Au film at 550 C on a <111> silicon substrate.



▲ Figure 2: Silicon nanowire grown by MOCVD using a Au catalyst on <111> Si substrate. The Au particle remains at the top of the wire and controls the diameter of the growing wire.

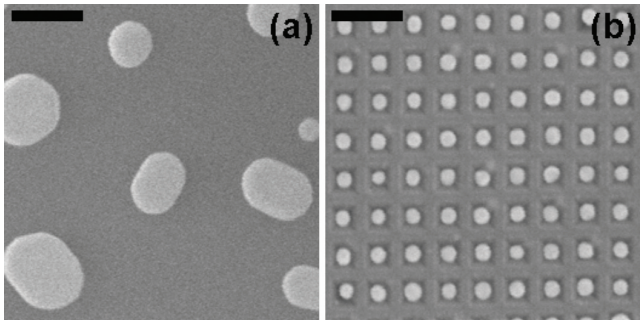
Templated Self-Assembly for Nano-particle Organization: Solid State Dewetting

A.L. Giermann, J. Ye, R. Mönig, C.V. Thompson
Sponsorship: NSF, Singapore-MIT Alliance

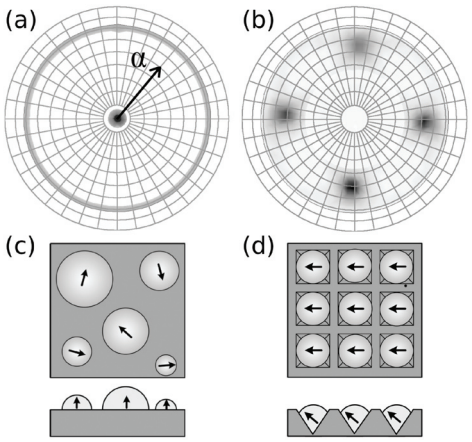
We are exploring solid-state dewetting of thin films as a tool for producing ordered arrays of metal nanodots over large areas. Such arrays may be interesting in memory or plasmonic applications and for use as catalysts for the growth of carbon nanotube or semiconductor nanowire arrays. Our current investigations focus on two topics: 1) the effects of materials anisotropies on dewetting; and 2) the effects of physical templates to control dewetting.

In the area of materials anisotropies, we seek a material system in which the islands formed by dewetting exhibit spatial order due to anisotropy in the surface energies and diffusivities. As an initial step, we observed significantly different dewetting behaviors of Ni thin films on MgO substrates, depending on the crystallographic orientation of the substrate surface. Our future work will involve investigating how micro-faceting of MgO affects the dewetting behaviors of Ni thin films.

In the area of physical templating, we use topographically patterned substrates to modulate the curvature of as-deposited films and thus influence the dewetting behavior of polycrystalline films [1]. We deposit and anneal gold films on di-periodic arrays of pits on oxidized silicon substrates to induce one-to-one self-assembly of ordered arrays of gold particles over large areas. Average particles sizes of less than 50 nm can be achieved. Compared to dewetting on flat substrates, the templates impose a significant decrease in average particle size, as well as ensure a narrow size and spatial distribution (Figure 1). This templating technique uniquely results in crystallographic ordering (i.e., graphoepitaxy) of the particles, imposing an in-plane texture and changing the out-of-plane texture (Figure 2). Particles formed in topographic features are expected to be stable with respect to agglomeration during growth of tubes or wires. Our current efforts include investigating additional techniques for imposing topographic templating on thin films; exploring the templating phenomena in other materials, including those that are known to catalyze carbon nanotubes and those with high surface mobilities; and developing numeric models of topographic dewetting in order to fully characterize the mechanism.



▲ Figure 1: The effect of topography on particle morphology. The results of dewetting a 10-nm-thick Au film on (a) a flat substrate and (b) a topographic substrate. Micrographs are displayed at the same magnification to emphasize the effect of topography on particle size. Scale bars are 200 nm in length.



▲ Figure 2: The effect of topography on particle orientation. (a) and (b) show Au <111> X-ray pole figures ($37.4^\circ < 2\theta < 38.6^\circ$), (a) for particles on a flat substrate and (b) for particles on a topographic substrate. (c) and (d) schematically illustrate the particle orientation on flat and topographic substrates, respectively. The arrows indicate the <111> projection.

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Catalyst Engineering and Carbon Nanotube Growth Mechanisms

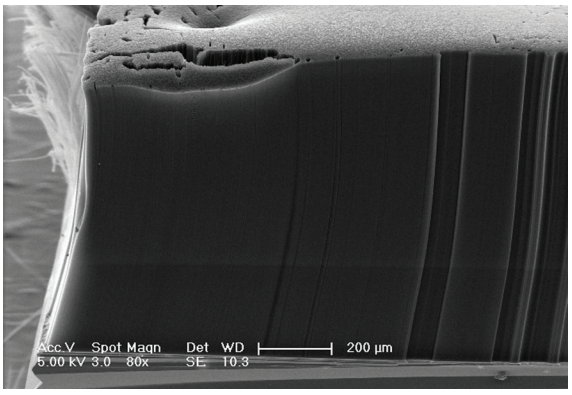
G.D. Nessim, J S. Kim, D. Acquaviva, A.J. Hart, C.V. Thompson
Sponsorship: MARCO IFC, Singapore-MIT Alliance

In addition to having many other applications in electronics and biology, carbon nanotubes (CNTs) are good substitutes for copper interconnects in integrated circuits. However, a significant challenge is the ability to control the density, type, size, and position of the nanotubes to be used as interconnects. These CNTs must also be grown on conductive substrates to achieve ohmic contact. Our approach to these challenges is to study and engineer catalysts in order to obtain CNTs with the required properties.

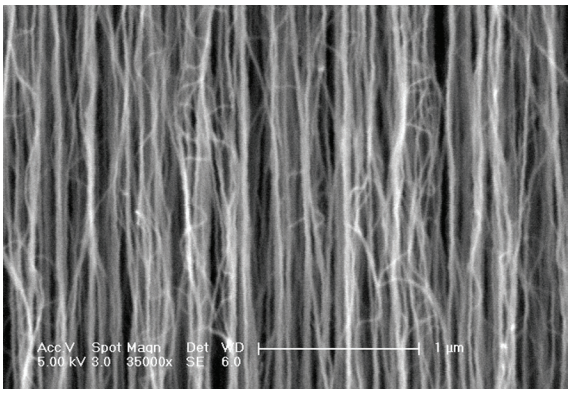
We initially studied nanotube growth with an iron catalyst on alumina underlayers using thermal chemical vapor deposition (CVD) and analyzed the influence of parameters such as catalyst size, temperature, reactant partial pressure, gas flow rate, timing of introduction of a reducing gas, pre-deposition annealing, and growth time. We have determined a range of conditions in which the growth of dense carpets of vertically aligned CNTs of different height, up to 1 mm (Figures 1 and 2), is possible. Characterization of the resulting CNTs with SEM, TEM, and AFM is underway.

We also started a series of experiments involving growth of CNTs with catalysts on conductive underlayers. This process is more challenging as evidenced by the very few successful reports of CNT growth directly on conductive substrates. With rapid heating of the samples prior to thermal CVD, we have grown CNTs as a mesh of CNTs ("spaghetti," not a regular carpet of CNTs). Preliminary measurements indicate that electrical conductivity exists between the nanotubes and the substrate.

Our next step is to grow CNTs on conductive underlayers inside a matrix of regularly spaced pores in an insulating overlayer, e.g., ordered porous alumina scaffolds developed in our group. Using this method we will measure and analyze the characteristics of regular arrays of individual multi-wall CNTs and bundles of CNTs with near-uniform dimensions.



▲ Figure 1: Dense carpet of carbon nanotubes grown using thermal chemical vapor deposition (catalyst Fe/Al_2O_3 on SiO_2).



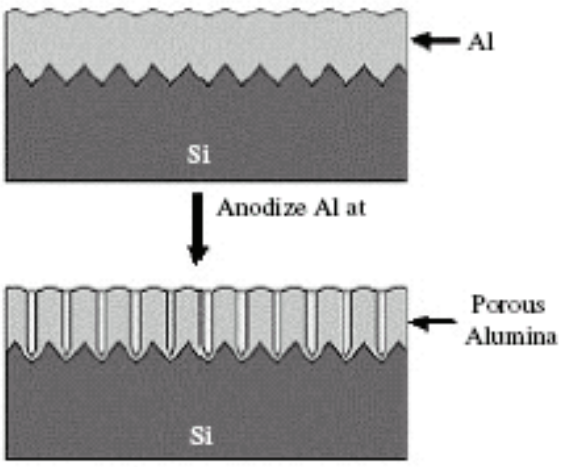
▲ Figure 2: Higher magnification image of the very dense carpet of CNTs of Figure 1.

Templated Self-Assembly for Nano-Particle Organization: Templated, Ordered Porous Alumina Templates

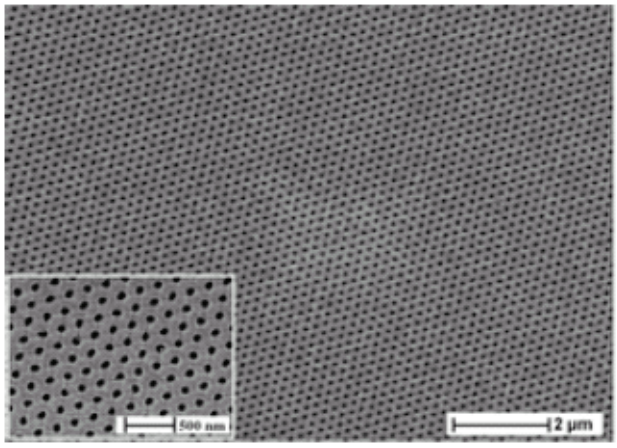
J. Oh, C.V. Thompson
Sponsorship: MARCO IFC, Singapore-MIT Alliance

Nano-sized materials are core building blocks for advanced functional systems such as electronic circuits, memories, sensors, and displays. Due to their size-sensitive electrical, optical, magnetic and chemical properties, it is desirable to fabricate nano-sized materials with controlled size and distribution on the system-applicable substrates. As a strategy, we are developing templated self-assembly methods that combine top-down (lithography) and bottom-up (self-assembly) approaches for fabricating and assembling metallic nano-wires, rods, and dots for new applications including nano-contacts for devices and interconnects for mixed-material and multifunctional micro- and nano-systems.

Anodic aluminum oxide (AAO) is a self-ordered nanostructured material that is suitable as a template in magnetic, electronic, and opto-electronic devices. Under proper anodization conditions, aluminum oxidizes as a porous structure with aligned pores that have a close-packed (hexagonal) order at short range and with pore sizes that can vary from 7 nm-300 nm. While short-range pore ordering can be achieved during anodization, domains (<5 μm) with different repeat directions occur at longer ranges. This breakdown in long-range order limits fabrication of large ordered arrays of devices using porous alumina templates. We developed perfectly ordered porous alumina scaffolds by combining interference lithography with anodization of evaporated Al thin films on silicon substrates. We have achieved regular arrays of pores with diameters of less than 30 nm and aspect ratios >50:1 in insulating alumina. Topographic templating of long-range order in anodic aluminum oxide allows independent control of the pore size, spacing, and order symmetry in ranges not achievable without templating. Using the perfectly-ordered AAO scaffolds, we have fabricated ordered metallic nanodots, nanorods, and nanotubes as well as well-aligned multi-walled carbon nanotubes (CNTs) on silicon substrates. We are currently pursuing the growth of uniform arrays of electrically contacted CNTs in templated AAO scaffolds to obtain statistical, electrical, and thermal characterizations of CNTs as a function of variations in the diameter and length of nanotubes.



▲ Figure 1: Schematics of fabrication of templated porous alumina scaffold [1].



▲ Figure 2: An SEM image of perfectly ordered porous alumina with hexagonal symmetry on silicon-over-wafer-scale areas with pore diameter of 80 nm and pore spacing of 180 nm [1].

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[1] R. Krishnan, H.Q. Nguyen, C.V. Thompson, W.K. Choi, Y.L. Foo, "Wafer-level ordered arrays of aligned carbon nanotubes with controlled size and spacing on silicon," *Nanotechnology*, vol. 16, no. 6, pp. 841-845, 2005.

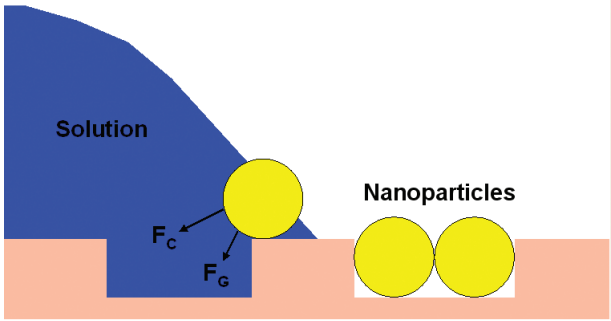
Templated Dewetting of Nano-Particle Solutions

S.-W. Chang, C.V. Thompson
Sponsorship: Singapore-MIT Alliance

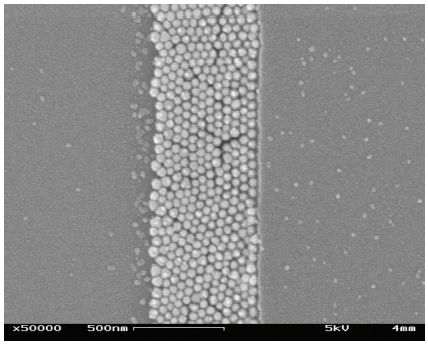
A major issue in nanotechnology is the need for versatile techniques for self-organization of nanometer-scale building blocks, such as nanoparticles, to form large-area periodic systems. Our goal is to combine physical templating and self-assembly to form nanoparticle arrays that can be used as catalysts for the growth of nanowire or nanotube arrays, and other applications such as nanoelectronics or nanophotonics.

A combination of physical templating and capillary interaction has been employed to self-organize colloidal particles into lithographically patterned templates with well-controlled sizes and structures [1]. However, the diameters of the particles studied to date are typically in the range of hundreds of nanometers. The capillary interaction strength decreases with diminishing dimensions due to random thermal fluctuations. Controlling the appropriate parameters may make it possible to overcome the randomizing effects of Brownian motion to extend the templated self-assembly (TSA) approach to sub-50-nm diameter particles.

As an initial effort, patterned substrates with gratings were fabricated using conventional contact-mode photolithography and inserted into nanoparticle solutions for evaporation. The resulting capillary interaction due to solvent evaporation was found to be sufficiently strong to force the nanoparticles into the template trenches without leaving particles on the surrounding areas. Figure 1 presents a schematic outline of the process. Current efforts include applying the templated dewetting approach to smaller nanostructures and on different topographies.



▲ Figure 1: A schematic outline of the assembly process. Forces that may be exerted on the gold particles are shown: capillary force (F_C) and gravitational force (F_G).



▲ Figure 2: Scanning electron micro-graph of ordered gold nanoparticles assembled in trenches.

REFERENCES:

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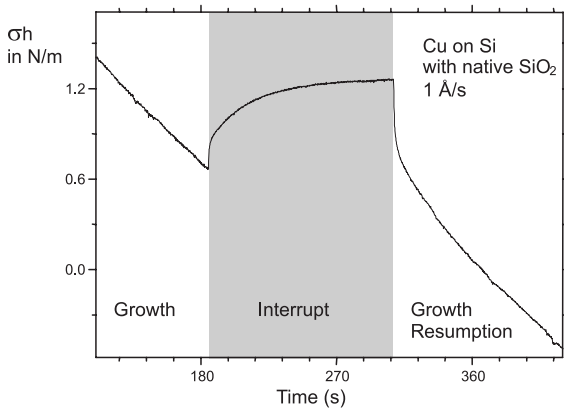
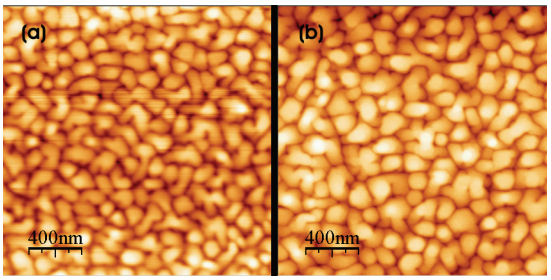
Surface Mound Formation and Stress Evolution during Growth of High-Mobility Metal Films

R. Moenig, J. Leib, A.R. Takahashi, C.V. Thompson
Sponsorship: NSF

Residual stress is an important factor affecting the performance and reliability of many micro-mechanical devices and thin-film structures. In order to control the residual stress of a thin metal film, knowledge of the active stress generation mechanisms is necessary. Our work focuses on structural changes and associated stress effects that occur during the growth of high-mobility metal films, e.g., Au, Cu, Ag, and Al, using evaporative deposition. Film stress measurements using capacitive deflection measurements of Si and SiO_2 cantilevers show tensile stress excursions after the deposition flux is interrupted and compressive changes after the deposition has been resumed [1-2]. Earlier studies using reflected high-energy electron diffraction indicate that stress changes are correlated with changes in surface roughness during growth interruptions [3]. Figure 1 shows a stress curve characteristic for growth interrupts and subsequent growth resumptions of high-mobility metal films. This reversible behavior was observed in Volmer-Weber growth of polycrystalline as well as in epitaxial films. Flash depositions of 1Å of Ta have been used to suppress surface diffusion on a film after interrupting growth in order to allow for atomic-force microscopy imaging of "frozen" films. Figure 2 shows two examples where the Ta flash was performed at different times after the growth had been interrupted. Figure 2 shows that the average mound spacing and the mound area increase during interrupts. Our observations indicate that the step-edge barrier (Ehrlich-Schwoebel-Barrier) that governs the interlayer transport of adatoms has a strong effect on film morphology. This barrier is significantly higher than the barrier for intralayer diffusion and therefore leads to mound formation and growth (roughness) even on high-mobility metal films deposited at RT.



▲ Figure 1: Stress measurement during deposition of Cu on Si with amorphous SiO_2 at RT. The film grows in Volmer-Weber mode and during the growth interrupt the stress experiences a tensile excursion.



▲ Figure 2: AFM images of a 1000Å Cu film deposited on large-grained Au. a) Ta deposition less than 2 s after Cu growth. b) Ta deposition 5 min after Cu growth was interrupted.

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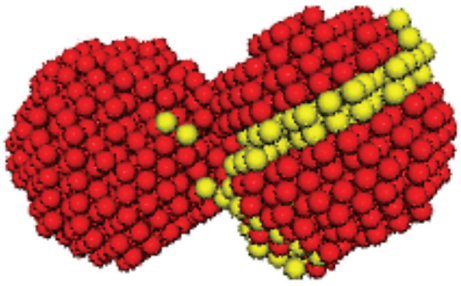
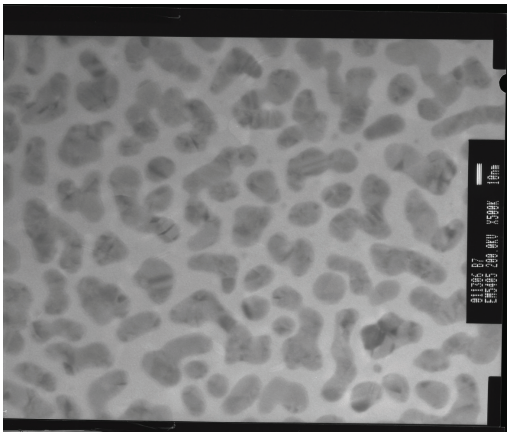
Stress and Structure Evolution Film Formation through Island Coalescence

A.R. Takahashi, J. Leib, R. Moenig, C.V. Thompson
Sponsorship: NSF

When thin films form through the Volmer-Weber mechanism, growth initiates through the nucleation and growth of isolated single-crystal nano-scale islands. As these islands impinge and coalesce to form a continuous film, dramatic evolution in the residual stress and microstructure of the film occurs. Island coalescence generates a tensile stress as islands strain towards each other to eliminate surface area [1-3]. While new models for the magnitude of the tensile stress due to coalescence [3-5] provide results that match experiments, the assumptions required to make these models tractable preclude a realistic consideration of the microstructure evolution. To complement analytic and numerical models for the magnitude of stress, we have initiated computational studies of microstructural evolution during boundary formation. The computational approach relies mainly on semi-empirical molecular dynamics (MD) calculations and some continuum finite element analysis(FEA)[6]. Using a fully atomistic approach such as MD provides direct insight into the types of boundaries formed during coalescence and their effect on continued structure evolution. An interesting preliminary result from atomistic modeling is that the boundary formation process can generate secondary defects such as stacking faults (Figure 1). For larger islands, the stress generated is insufficient to propagate defects and for smaller islands, size-strengthening inhibits formation of defects. However, in an intermediate range of island sizes, stacking faults are readily formed. Transmission electron microscopy (TEM) of late-stage coalescence films does show a high density of stacking faults and twins but the origin of these defects is still unclear (Figure 2). Future experiments will focus on controlling the size of islands at coalescence and characterizing the distribution of defect types formed for different size ranges.



▲ Figure 1: Computer calculated stacking fault resulting from boundary formation. This type of defect is observed frequently in calculations of islands in the 3-to 5-nm diameter range.



▲ Figure 2: Micrograph of later stage coalescence of Au on a thin silicon nitride membrane. Stacking faults are evident in several of the coalesced island structures.

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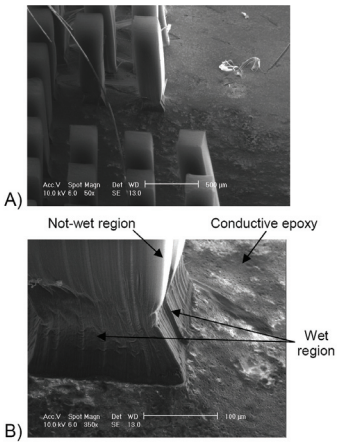
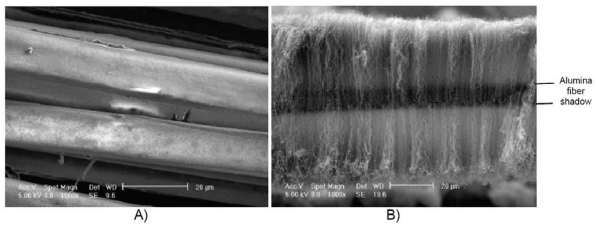
Hybrid Carbon Nanotube-Composite Architectures

E.J. García, A.J. Hart, K. Sorensen, B.L. Wardle (in coll. with A.H. Slocum)
Sponsorship: La Caixa Foundation

Hybrid composite architectures employing traditional advanced composites and carbon nanotubes (CNTs) offer significant potential mechanical and multifunctional performance benefits. Dense patterns of well-aligned carbon nanotubes (CNTs) were grown on silicon wafers using a thermal chemical vapor deposition (CVD) process [1]. Wetting of CNTs and retention of mechanical properties of the fibers after the CVD process are considered fundamental issues related to realizing novel hybrid composite architectures. Wetting of CNT forests by several commercial polymers (including a highly-viscous epoxy, as shown in Figure 1) has been demonstrated at rates conducive to creating a fully-dispersed CNT/matrix region around the fibers in hybrid architectures [2]. A new microfabrication method [3] was developed to create well-aligned, regularly contracted pillars. The basic mechanical properties (elastic modulus, strength) of the polymer and the CNT/polymer nanocomposite were obtained by means of a nanoindenter to apply a compression test to the vertically aligned circular composite pillars [3]. The elastic modulus was obtained using the Oliver-Pharr theory adapted to the flat punch used in the experiments. These intermediate architectures of aligned CNTs in a polymer matrix are being employed to create more sophisticated architectures utilizing advanced fibers and prepregs of traditional advanced composites [4-5]. The dense, aligned, high-quality forests of CNTs grown at high rates (~50 microns per minute) suggest that the process is scalable for incorporation into traditional composites. Single-fiber tension tests [6] indicate no mechanical degradation for fibers undergoing the CNT growth process, as shown in Figure 2c). Results indicate that hybrid CNT/composite architectures are feasible; future work focuses on mechanical and multifunctional property characterization of other hybrid architectures and scaling to a continuous CNT growth process.



▲ Figure 1: A) Pattern of CNT pillars wet by 20-minute-curing, high-viscosity epoxy resin; B) Close-up of the wet region at the base of the pillar.



	Tensile strength [GPa]		Young's modulus [GPa]		Strain-to-failure [%]	
	Mean	Standard deviation	Mean	Standard deviation	Mean	Standard deviation
Pure alumina fiber	2.19	0.19	135	6.38	1.63	0.13
Alumina soaked in catalyst	2.30	0.21	138	12.6	1.73	0.06
Alumina fibers with CNTs	2.28	0.09	134	11.3	1.63	0.16

C)

▲ Figure 2: A) Pure alumina fiber; B) Alumina fiber (shadow behind CNTs) with well-aligned, 30-µm-long CNTs grown on its surface; C) Experimental results for pure alumina fibers, fibers soaked with catalyst, and fibers after the CNT growth process.

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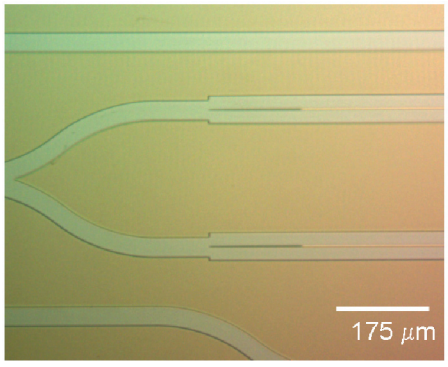
PHOTONICS



▲ A photograph of the beginning of the second- generation Mach Zehnder interferometer (R. Williams, A. Markina, G.S. Petrich, E.P. Ippen, R.J. Ram, L.A. Kolodziejski, p. 237).

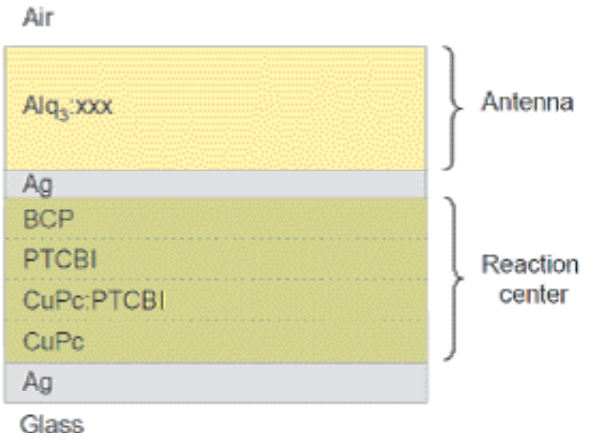
for additional reading...

Organic Photovoltaics with External Antennas

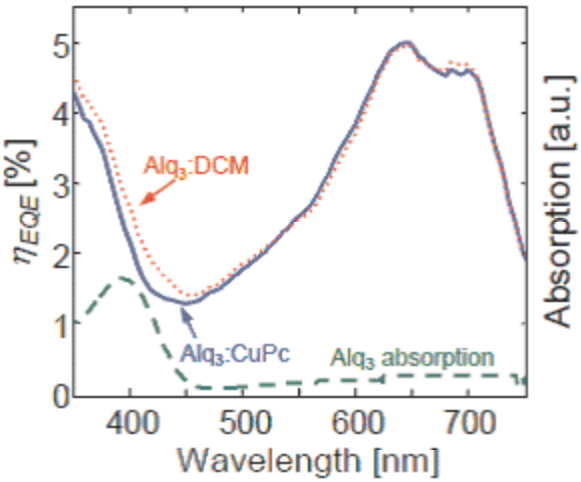
J.K. Mapel, T.D. Heidel, M.A. Baldo
Sponsorship: DARPA, NIRT

The structures and processes of photosynthesis are evolved, highly efficient, robust, and possess high power density. We attempt to leverage these characteristics by incorporating photosynthetic architectural motifs into organic semiconductor solar cells. We adapt the organization of processes in photosynthesis and introduce a synthetic light harvesting structure into an organic photovoltaic so that it couples light energy to the active device area by near field energy transfer. Light energy absorbed in an artificial antenna layer is transferred to an artificial reaction center in the interior of the solar cell. The energy transfer is of the Förster type, mediated by surface plasmons polaritons. While the introduction of the antenna necessarily adds a step to the energy transduction process, decoupling photon absorption and exciton dissociation can be exploited to increase each separately.

We have experimentally examined the efficiency of energy transfer for this process. We utilize a film of photoluminescent chromophores placed immediately adjacent to an organic solar cell with dual silver electrodes as an antenna layer. We predict and verify that energy transfer can occur in technically relevant device structures with energy transfer efficiencies of approximately 50% and demonstrate this transfer result in increased quantum efficiency.



▲ Figure 1: The device structure utilized in these studies is composed of aluminum tris(8-hydroxyquinoline), bathocuproine, copper pthalocyanine, 3,4,9,10-perylenetetracarboxylicbis-benzimidazole, 4-dicyanomethylene-2-methyl-6-(p-dimethylaminostyryl)-4*H*-pyran, and silver. To tune the emission of the Alq3 antenna it was doped with either CuPc or DCM at 1% weight ratio.

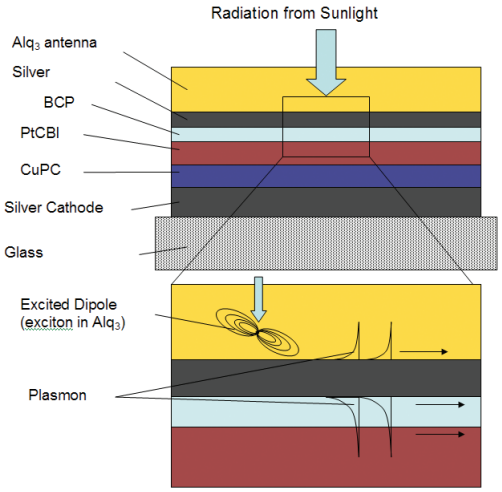


▲ Figure 2: The comparison of devices with functional (dotted line) and nonfunctional (solid line) antennas demonstrate external energy transfer. Devices with functional external Alq3 antenna layers (dotted line) exhibit an increase in external quantum efficiency over the wavelength range where Alq3 absorption occurs (dashed line). The photocurrent spectra are identical outside the spectral range where Alq3 absorbs. Functional antennas employ the laser dye, *X* = DCM, whereas nonfunctional antennas employ the quencher *X* = CuPc).

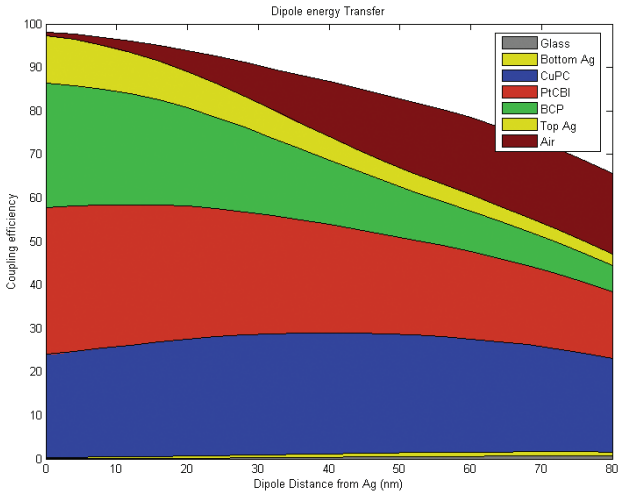
Optical Models of Organic Photovoltaic Cells

K. Celebi, M.A. Baldo
Sponsorship: DARPA

Common organic photovoltaic devices utilize a direct energy transfer from sunlight to the excitons in the active layers. However, this direct transfer results in a trade-off between the absorption and charge generation by exciton diffusion to the interface [1]. Our group has recently demonstrated a separation of these two processes by absorbing the sunlight in an external antenna and then reemitting the energy in a near-field fashion so that very large exponential fields become possible in the active layers (Figure 1). Calculating the effect of this reemission needs near-field methods since the thicknesses are on the order of the vacuum wavelength of the corresponding emission frequency. To solve this problem, we extend a previously established dyadic Green's functions model [2] to calculate the z-component of the Poynting vector, thus find the spatial absorption of the antenna reemission throughout the multilayer stack (Figure 2). Using these calculations we calculate optimum layer thicknesses for maximum efficiencies. Future work in modeling will concentrate on far-field emission for OLED outcoupling studies and collective dipole behavior.



▲ Figure 1: Working principle of the organic PVs with external antennas. Energy is first absorbed by the excitons in the antenna and then these excited excitons transfer their energy to the excitons in the active layers (PtCBI & CuPC) mainly through surface plasmon polariton modes. Structure used is Air/ 800Alq_3/ 80Ag/ 100BCP/ 180PtCBI/ 240CuPC/ 400Ag/ Glass (thicknesses are in Angstroms).



▲ Figure 2: Percentage of power transferred from the excitons in the antenna to different layers in the structure of Figure 1 as a function of exciton distance from the Alq_3-Ag interface. White space on the top shows internal damping in the Alq_3 molecules. As the exciton distance from silver film increases efficiency decreases due to the reduction in plasmon coupling.

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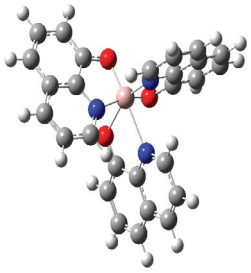
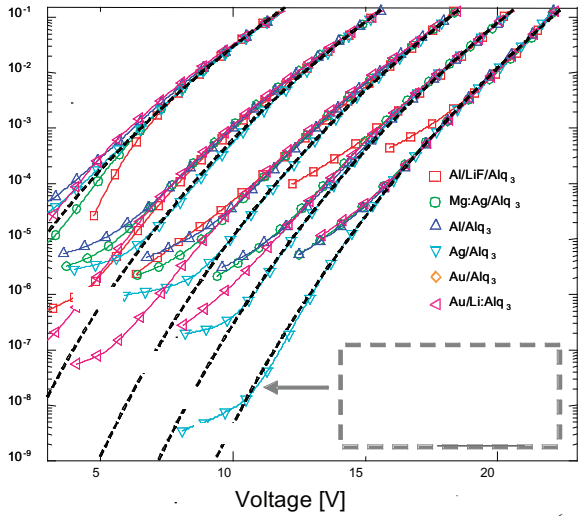
Percolation Model of Charge Transport in Organic Semiconductors

B.N Limketkai, M.A. Baldo
Sponsorship: DuPont-MIT Alliance

In this project, we study charge transport in organic semiconductors using percolation theory. A percolation model was first introduced by Ambegoakar *et al* [1] to explain the hopping conductivity in disordered systems. It was later incorporated in Vissenberg and Matters [2] for an exponential DOS to explain the field-effect mobility in amorphous organic transistors. This percolation model is further employed here, incorporating the effects of an applied electric field to the mobility and current-voltage (IV) characteristics of organic semiconductors. By modifying the percolation model to include the effect of an applied electric field, the temperature and field dependence of mobility and IV characteristics are found. A universal IV characteristic for organic semiconductors is explained. The Miller-Abrahams expression for charge hopping between exponential trap distributions gives a master equation [3]: $\tilde{J} = \tilde{J}_0(V/V_0)^m$, where $\tilde{J}_0$ and V_0 are constants and $m = 1+2\alpha kT_0/(qF+2\alpha kT)$, where α is the tunneling decay rate, is the power-law slope. Characterization of IV measurements were done with the archetypal organic semiconductor material, tris(8-hydroxyquinoline) aluminum, or Alq_3. Figure 1 shows its molecular structure. To demonstrate the universality of the model, the IV characteristics of a number of Alq_3 devices are overlapped as shown in Figure 2.



▲ Figure 1: Molecular structure of the archetypal organic semiconductor material, tris(8-hydroxyquinoline) aluminum (Alq_3).



▲ Figure 2: The temperature dependence of the universal IV characteristics of Alq_3 devices. A rigid voltage shift was applied to each IV characteristics to overlap on one another.

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Integrated Optical-wavelength-dependent Switching and Tuning by Use of Titanium Nitride (TiN) MEMS Technology

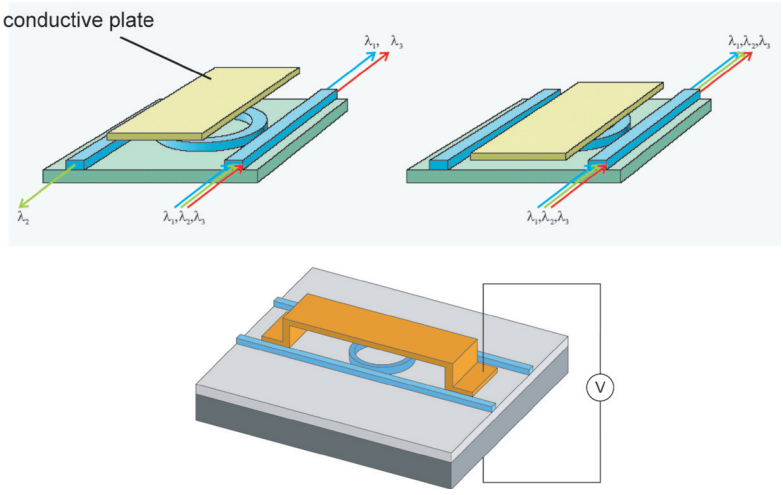
S. Takahashi, G.N. Nielson, G. Barbastathis
Sponsorship: DARPA

Ring resonators are integrated optical components that have the capabilities to filter specific bands of wavelength from a broad-band input signal. Although these devices themselves are passive components, by use of evanescent field coupling, the ring resonator can be switched or tuned by electrostaticactuation of a MEMS bridge-type structure above the ring waveguide (Figure 1). This procedure of switching and tuning will allow for a faster speed than thermal tuning and will not induce severe loss, as does carrier injection.

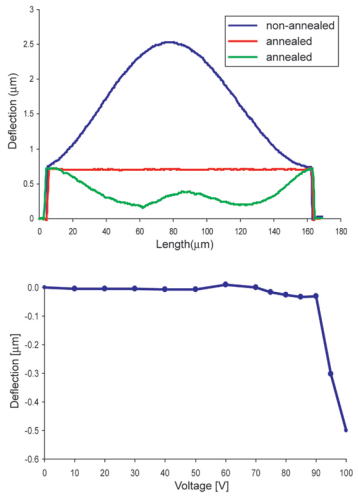
One major issue that must be faced when implementing this concept is the residual stress that the MEMS bridge structure exhibits. Precise vertical positioning of the bridge is crucial for this type of device, and hence the bridge structure must not deflect due to residual stress within the structure. Use of TiN was investigated as the structural material due to its appealing mechanical properties, high electrical conductivity as well as its ability to relax its residual stress by annealing. The TiN MEMS bridges were fabricated and tested. The MEMS structures were successfully annealed to a flat state, and the actuation voltage of the switch was 90V (Figure 2).

Recently, we have been investigating an architecture which allows for a more flexible design of the device, as well as the capabilities for implementing ultra fast-switching and feed-back control of the position of the wafer via capacitance measurement [1]. In this architecture, the ring resonator is fabricated on one wafer and the MEMS structure on another, and the wafers are flip-chip bonded by thermocompression waferbonding with gold.

Wavelength tuning of the ring resonator filter has been numerically simulated by a combination of FEM structural analysis and mode-solver electromagnetic analysis. This analysis showed that tuning of a range of 30 nm with an actuation voltage of 10V was feasible with a silicon oxynitride membrane as the dielectric material.



▲ Figure 1: Concept of ring resonator switching via evanescent field coupling (top) and the implemented MEMS-based switching device (bottom). The same concept can be used to tune the resonating wavelength of the ring resonator by using a dielectric material instead of a lossy material, in which case the dropping wavelength on the top left figure will be altered to another wavelength when the membrane is pulled down close to the ring resonator.



▲ Figure 2: The profile of the TiN MEMS bridge before and after annealing at 500˚C (top), and the voltage vs. deflection curve of the actuated MEMS bridge (bottom).

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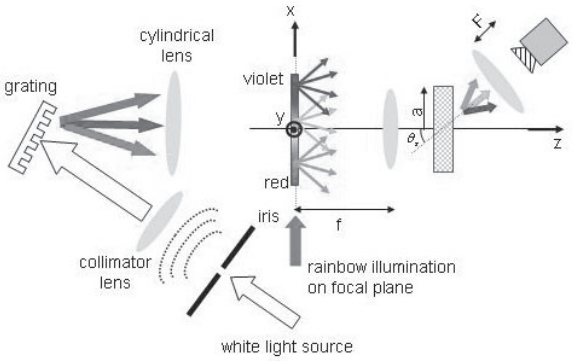
Four Dimensional Volume Holographic Imaging with Natural Illumination

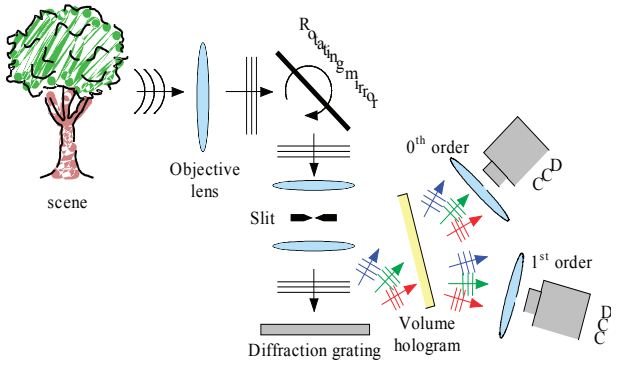
S.B. Oh, W. Sun, G. Barbastathis
Sponsorship: AFRL, DARPA

Volume holographic imaging is a 3D imaging technique that uses volume holographic lenses. We devised a rainbow volume holographic imaging (RVHI) system, shown in Figure 1. The system projects a rainbow illumination on objects by means of a diffraction grating. Collimated white light is decomposed by a diffraction grating. After passing through a cylindrical lens, the rainbow is focused to the focal plane of a volume holographic lens. All the in-focus points along the *x* dimension are Bragg- matched; in the *y* dimension they are also Bragg-matched because of degeneracy. Therefore, the entire rainbow plane is Bragg-matched, resulting in a broad field of view (FOV). When shifted out of focus, each point source in the rainbow becomes Bragg-mismatched due to defocus, much as a narrow-band source at the same wavelength would be[1].

A four-dimensional (3D + spectral) imaging system was devised recently. One unique advantage of this system is that it can be used under natural broadband light illumination on this principle [2]. The imaging process of the 4D imaging system can be understood as a combination of non-invasive optical slicing and spectral analysis. A narrow slit portion (along the *y* axis) of the object on the focal plane is sampled and its spectrum is laterally imaged on the CCD camera. To cover the entire four-dimensional object space (three spatial dimensions plus one spectral dimension), auxiliary mechanical scanning (rotational mirror as shown in Figure 2) or multiplexing holograms corresponding to different slits are necessary. Also both the 1st order and 0th order diffraction from the volume hologram are measured simultaneously to normalize the brightness of objects.



▲ Figure 1: Schematics of rainbow holographic imaging system.



▲ Figure 2: Schematic of the newly devised setup to use volume holographic imaging system under extended white light illumination.

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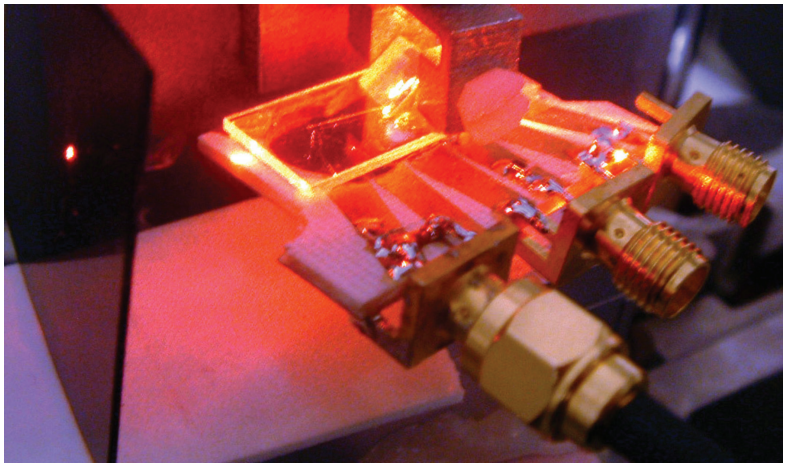
Guided-Wave Devices for Video Display Applications

D. Smalley, V.M. Bove, Jr., Q. Smithwick
Sponsorship: CELab, Digital Life, and Things That Think research consortia, MIT Media Lab

We are developing a guided-wave optical modulator[1-2] with 1 Ghz composite bandwidth surface acoustic wave (SAW) transducer arrays for use in video display. This device is designed to diffract light both vertically and horizontally by creating surface acoustic waves that interact with light trapped in waveguides on the surface of a lithium niobate substrate. To fabricate this modulator, we first mask a wafer of Z-cut lithium niobate with SiO_2 through a PECVD process and then we immerse it in heated benzoic acid to create single polarization waveguides. Finally, we pattern aluminum transducers onto the waveguides by contact lithography employing a negative resist lift-off technique.

The goal of this work is to enable the inexpensive manufacturing of Scophony-architecture video displays [3] (both 2D and holographic video [4-5]) without the need for the horizontal scanning mirrors that typically limit the scalability of this technology.



▲ Figure 1: Prototype 2-D guided-wave acousto-optic device for video display applications.

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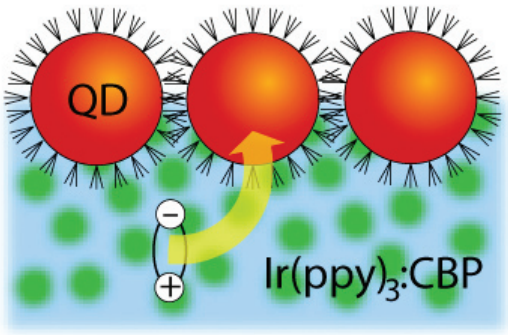
Energy Transfer from an Organic Phosphorescent Thin Film to a Monolayer of Quantum Dots

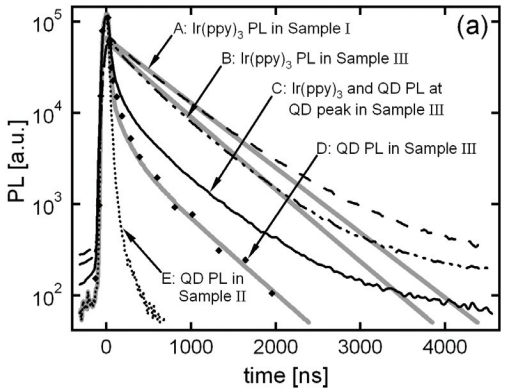
P.O. Anikeeva, C F. Madigan, S.A. Coe-Sullivan, J.S. Steckel, M.G. Bawendi, V. Bulović
Sponsorship: ISN, NSF Materials Research Science and Engineering Center at MIT, PECASE

Over the past several years the optical and electronic properties of colloidaly synthesized nanocrystals, or quantum dots (QDs), of CdSe have been extensively studied, with the aim of using QD films in solid-state opto-electronic devices. Efficient exciton generation in CdSe QDs suggests use of nanocrystal composite films in photovoltaic cells, while high luminescence quantum yields and tunability of QD emission wavelengths over the entire visible spectrum suggests QD film use in light-emitting devices (LEDs). These developments are a consequence of advances in colloidal QD synthesis that allow for increased control over the shape, size, and emission wavelength of nanocrystals and the development of methods for forming QD thin films of controlled structure and composition. We utilize these advances in the present study to demonstrate triplet exciton energy transfer (ET) from a thin film of phosphorescent molecules to a monolayer of CdSe/ZnS core/shell QDs (Figure 1). Triplet exciton harvesting and transfer to an efficient lumophore has been previously used in advancing organic light emitting device (OLED) technology and has the potential to similarly benefit the emerging field of quantum-dot-LEDs.

The efficient energy transfer is facilitated by the spectral overlap of the organic phosphor fac tris(2-phenylpyridine) iridium ($Ir(ppy)_3$) luminescence and QD absorption spectra. In time-resolved photoluminescence (PL) measurements, the energy transfer is manifested as elongation of the QD PL time constant from 40 ns to 400 ns (Figure 2) and a concomitant 55 % increase of time-integrated QD PL intensity. Numerical analysis supports the conclusion that the observed PL dynamics are dominated by exciton diffusion within the $Ir(ppy)_3$ film to the QD layer, energy transfer from $Ir(ppy)_3$ to QD film, and subsequent QD luminescence [1].



▲ Figure 1: Schematic diagram of the energy transfer form an organic film doped with a phosphorescent donor to a monolayer of colloidal CdSe/ZnS core-shell QDs.



▲ Figure 2: Time resolved PL measurements for samples I, II, and III, which respectively correspond to $Ir(ppy)_3$ film on glass, QD layer on glass, and QD layer on $Ir(ppy)_3$ film on glass . The black lines and dots represent the experimental measurements, and the thick grey lines represent numerical fits using the proposed diffusion model. Data set A represents $Ir(ppy)_3$ PL decay in purely organic sample, data set B represents $Ir(ppy)_3$ PL decay in contact with QDs, data set C represents QD and $Ir(ppy)_3$ PL decay in contact with each other at QD PL peak position, data set D represents QD dynamics in contact with $Ir(ppy)_3$, data set E represents QD dynamics in purely QD sample.

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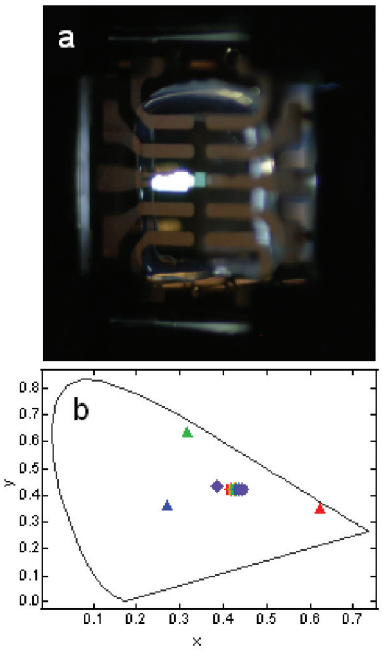
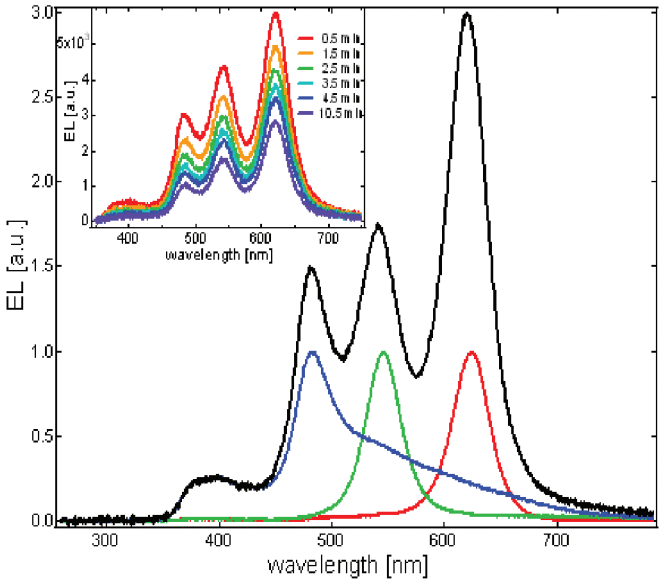
White Light QD-LEDs

P.O. Anikeeva, J.E. Halpert, M.G. Bawendi, V. Bulović
Sponsorship: ISN, NSF Materials Research Science and Engineering Center at MIT, PECASE

We are developing white-light emitting quantum dot LEDs (QD-LEDs) for use as planar white-light sources in the full-color active-matrix displays with color filters and in future solid-state lighting. Our white QD-LEDs consist of organic charge transport layers with a QD monolayer sandwiched between them. This device architecture enables independent processing of the charge transport layers and the emissive layer. The independent processing of QDs is a result of the recent development of the QD printing technique, which allows for the solvent–free deposition of QD monolayers onto various organic materials [1]. By mixing different amounts of high quantum-yield colloidal core/shell QDs (red CdSe/ZnS, green ZnCdSe/ZnS, blue CdS/ZnS), we demonstrate different QD-LED colors. Figure 1a shows electroluminescence of the white QD-LED with the CIE (Commission International de l'Eclairage) coordinates of (0.42, 0.41). Figure 1b and inset of Figure 2 also show that CIE coordinates vary only slightly under the different applied bias and different operation time [2].



▲ Figure 1: a) Photograph of a white QD-LED operated at 10 V of applied bias. b) CIE coordinates of QD-LEDs: red (red triangle), green (green triangle), blue (blue triangle), and white (purple diamond at 12 V. Change of color with operation lifetime is shown with progression from red circle to purple circle for a QD-LED operated at 9 V.



▲ Figure 2: Electroluminescence of the blue (blue line), green (green line), red (red line), and white (black line) QD-LEDs shown not to scale to demonstrate the presence of the spectral signatures of all three QD colors in the white device spectrum. Inset: We observe slight change of the spectral shape of the white QD-LED with operation time.

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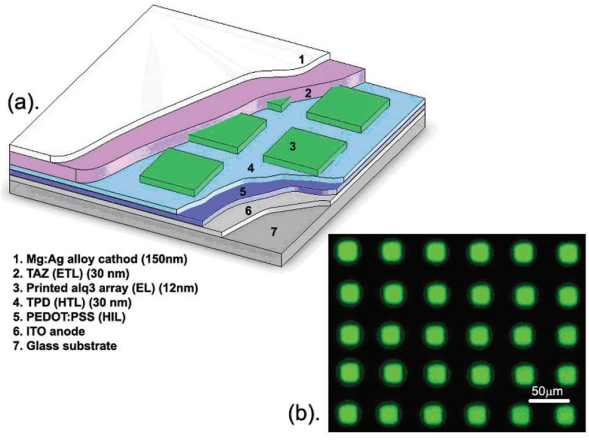
Organic Optoelectronic Devices Printed by the Molecular Jet Printer

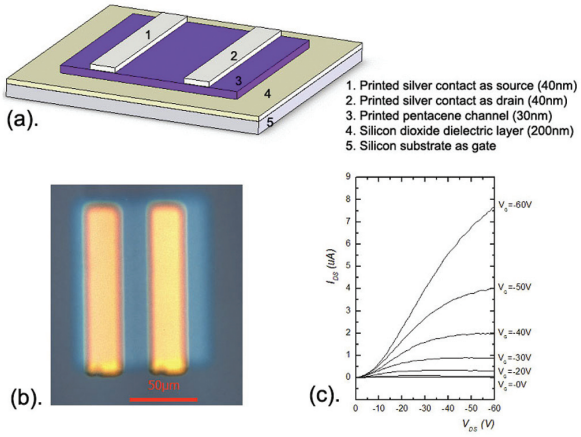
J. Chen, V. Leblanc, M.A. Baldo, M.A. Schmidt, V. Bulović
Sponsorship: Hewlett-Packard

Using a micro-fabricated silicon printhead, we developed a novel printing technique, molecular jet printing (MoJet) [1-2] that allows direct patterning of small molecular weight organics and metals by additive deposition at high resolution. Today's dominant method for patterning vacuum-deposited semiconducting molecular organics uses a thin metal stencil as a shadow mask through which material evaporates. Once the metal stencil is fabricated, it cannot be reconfigured to define arbitrary patterns or be scaled up with substrate size. In contrast, the MoJet printing technique utilizes a silicon printhead that integrates a moving micro-shutter with a micro-aperture. The shutter can be opened or closed with a DC control signal. Evaporated organic molecules can either pass through the aperture to reach the substrate when no bias is applied or be obstructed by the shutter when the control signal is above 30 V DC. This reconfigurable printhead together with a moving stage allows arbitrary patterning capability and scalability of the MoJet printer to larger substrate sizes.

We demonstrate that active organic devices such as organic LEDs and organic FETs (see graphics below) can be fabricated directly using the MoJet printer. The MoJet printing is a solvent-free process (in contrast to ink-jet printing) that combines the high quality of thermally evaporated thin films with the high precision and scalability enabled by MEMS technology. The MoJet printed organic electronic devices have the same performance characteristics as those defined by the shadow-mask patterning method, but the size of the substrate plate can now be expanded beyond GEN 2/3. As such, the MoJet printer surpasses the capability of the metal-stencil shadow mask and has the potential to become the next generation patterning tool for making organic optoelectronic devices.



▲ Figure 1: (a) Layer structure of printed OLED array. The green electroluminescent layer (EL) is directly printed with the MoJet printer. (b) EL micrograph of active OLED array at 7.5V applied voltage. The image is taken through a 470-nm low-pass filter to reveal that green pixel patterned by the MoJet. The pixel size is 30 μm, equivalent to 800 dpi resolution.



▲ Figure 2: (a) Structure of the printed Pentacene transistor. Pentacene layer is printed down first and silver contacts are printed sequentially. (b) Micrograph of a single-printed OFET on silicon oxide. (c) The I-V characteristics of one of the transistors. The gate voltage Vg is varied from 0 to –60V in 10V steps.

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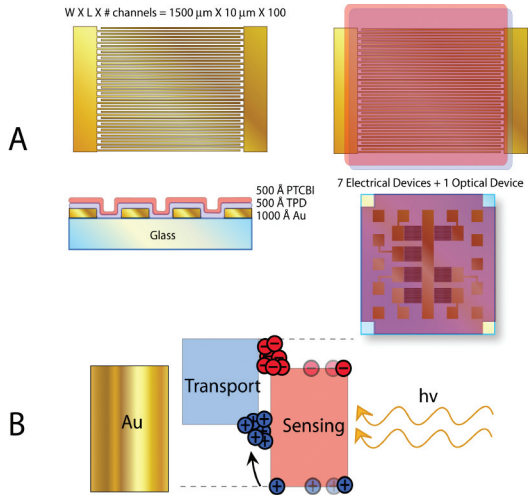
Charge Dynamics in Organic Heterojunction Lateral Photoconductors

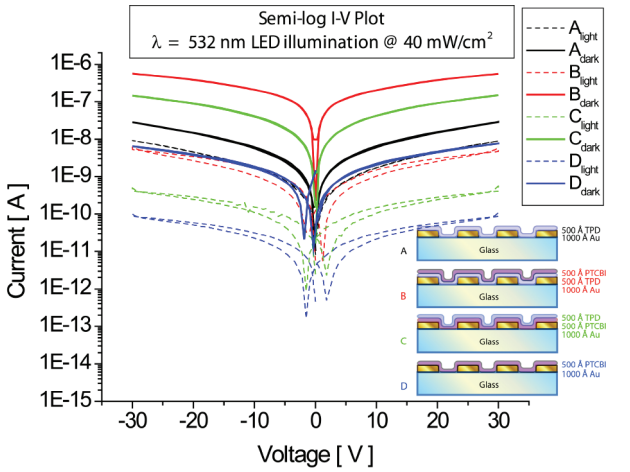
J.Ho, V. Bulović

The purpose of this project is to develop solid-state, organic device structures capable of efficiently converting analyte detection into an attenuation in electrical signal. The main advantage to using organic materials is that they are synthetically flexible and can be tailored to respond to specific analytes. Our proposed device structure is a heterostructure consisting of an optically active, chemosensing layer and a charge-transport layer arranged in a lateral photoconductor-style device (Figure 1A). The advantages to physically separating the sensing and transport functions in chemical sensors include: 1) the ability to optimize the transduction of luminescence to device current, and 2) the development of a reusable device platform for a variety of chemosensing applications.

In addition to developing a novel device platform for chemical sensing, we are using this novel structure to study charge transport and exciton dynamics in organic thin films (Figure 1B). The devices consist of a series of gold interdigitated fingers (W x L = 1500 μm x 4 μm) spaced 10 μm apart (Figure 1A). The gold electrodes are photolithographically defined on glass before the organic layers are thermally evaporated. Locked-in measurements of the photocurrent spectra suggest external quantum efficiencies ranging from 10-15%. Initial experiments indicate an enhancement in photoresponse of the heterostructure devices over devices made from bulk films of both materials (Figure 2).



▲ Figure 1: A) Schematic drawings of lateral photo conductor devices. Clockwise from upper left are photolithographically defined gold electrodes, electrodes with evaporated organic thin films, cross-section view, and top view of actual substrate. B) Mock band diagram of device showing exciton generation, exciton diffusion, and charge carrier build-up at the heterostructure interface.



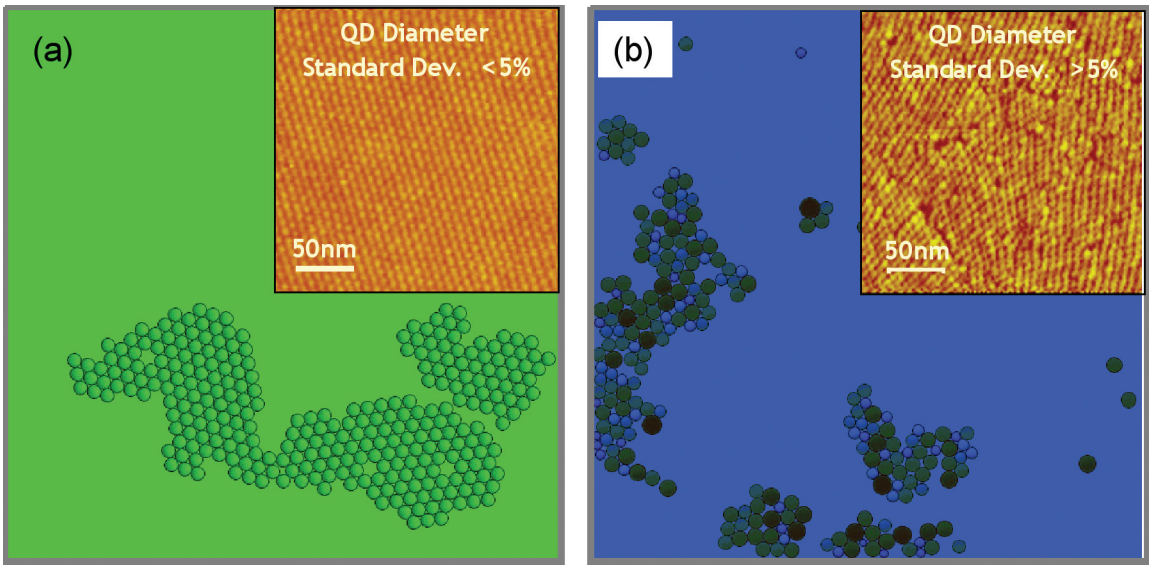
▲ Figure 2: Semi-log current-voltage characteristics of bulk and heterostructure lateral photoconductor devices. Dotted lines represent I-V curves in dark. Solid lines represent I-V curves under LED illumination centered at λ = 532 nm. Inset: Cross-sections of tested devices. Note the different photoresponse curves between the bulk and heterostructure devices.

Packing of Quantum Dot Monolayers

E. Howe, V. Bulović
Sponsorship: MARCO MSD

We developed a kinetic model for assembly of ordered quantum-dot (QD) monolayers on a 2-dimensional surface that reproduces experimental observations for a variety of QD size distributions (of Gaussian size profile). Such QD monolayers have already been utilized in a number of thin-film applications, QD-LEDs, and QD-photodetectors. However, methods of fabricating QD films are still being developed and our work focuses on developing a numerical tool to investigate methods for improving the quality of these films.

To numerically assemble a QD monolayer, we model the QDs as spheres that move on the surface with no friction but with random thermal motion added at each time-step. We apply a van der Waals attraction between QDs and hard-wall repulsion at the QD radius. When two QDs collide, their interaction is partially inelastic based on a model parameter. These conditions allow for a range of behavior encompassing many interesting phenomena. We find that a mono-disperse size distribution of QDs forms hexagonally close-packed aggregates, and the packing and aggregate stability of the QD monolayer degrades dramatically as the standard deviation of the size distribution is increased. In experimental studies [1], the instability of QD monolayers has been observed to occur for standard deviations of greater than 10% in QD diameter. We were able to reproduce these findings in our simulations (Figure 1). We have further shown that confining the same QD distributions inside a 1-dimensional hard boundary with a width of a few QD diameters can counteract this instability.



▲ Figure 1: (a) Results of simulation of packing for 300 QDs of equal size. The inset is an AFM image [1] of a monolayer of QDs with less than 5% standard deviation in diameters. In our simulation we observe the same hexagonal close-packed arrangement of QDs and stability of aggregates that allows for good monolayer formation. (b) Results of simulation for packing 300 QDs with a 15% standard deviation in diameters. The inset is an AFM image for the same method of preparation as (a) but with QDs having a greater than 5% standard deviation in diameters. For these large size distributions, our simulated dots could no longer form hexagonally close-packed arrays. In addition, aggregates readily broke up as dots were less well-bound.

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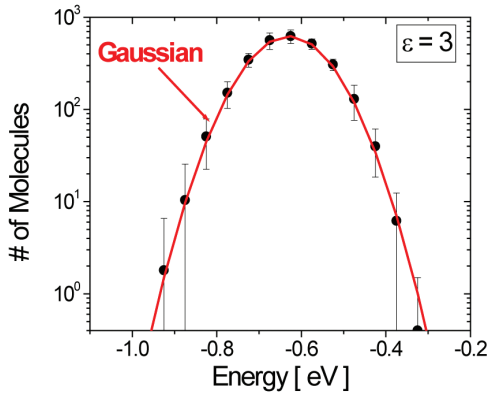
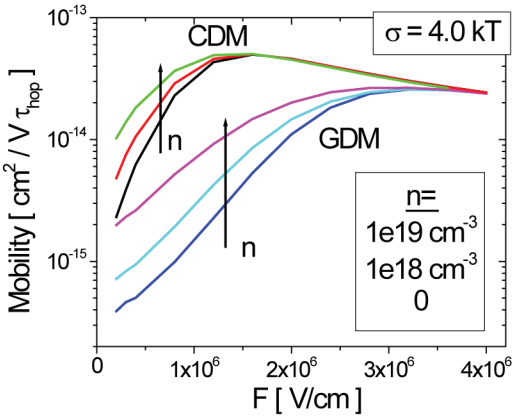
Energy Disorder and Device Performance in Organic Electronics

C.F. Madigan, V. Bulović
Sponsorship: MARCO MSD, NDSEG Fellowship

Presently many organic electronic devices employ amorphous materials, and it is well known that the molecular energy levels in such materials are subject to disorder arising from variations in local intermolecular interactions. The movement of molecular charge carriers and excitons through the constituent materials largely controls the performance of such devices, and it has been well established that energy disorder strongly influences charge carrier and exciton motion. Though accurate analytic treatments remain elusive, Monte Carlo (MC) simulations of charge carrier and exciton hopping between molecular sites subject to energy disorder have proven an effective tool for analyzing charge carrier and exciton motion in such materials [1]. Combining MC simulations with accurate models of energy disorder should make it possible to perform calculations of device behavior in realistic structures with relatively few theoretical model assumptions. This project addresses: (1) the theoretical calculation of energy disorder in amorphous organic materials; and (2) the application of MC simulations to realistic device structures and operating conditions. We have performed exact calculations of charge carrier and exciton energy disorder arising from electrostatic interactions between structurally disordered, polarizible molecular charge distributions (see Figure 1). These calculations differ from those in the literature because the molecular polarizibility is explicitly included in the calculation, avoiding the need to employ dielectric continuum approximations (DCAs). It is found that the widely used DCAs are inaccurate, and we presently are developing improved expressions for relating the magnitude of the disorder to the material properties (principally, the molecular dipole moment, the molecular density, and the dielectric constant). We have also developed an MC simulator of charge carrier and exciton motion in energetically disordered molecular materials capable of treating realistic device geometries (e.g., multilayer stacks and electrical contacts). Because organic electronic devices often operate at high carrier concentrations, we have also included basic charge-carrier interactions to treat the effects of carrier concentration on charge transport; these effects have not been previously investigated using the MC simulation technique. We are presently performing calculations of carrier mobilities as a function of field and carrier concentration (see Figure 2) for comparison with existing approximate analytic approaches. These studies support future simulations of real device structures for a rigorous comparison of experimental device performance and theory.



▲ Figure 1: Calculation of charge carrier energy disorder (in the form of the histogram of energies for a large collection of interacting molecules) for a structurally random molecular solid, composed of molecules having a dipole moment of 2 Debye, a molecule density of 1e21 cm^{-3}, and a dielectric constant, Σ, of 3. The black symbols denote the raw data, and the red line indicates a fit using a Gaussian function.



▲ Figure 2: Calculations of charge-carrier mobility as a function of field, F, and carrier concentration, n, in an energetically disordered molecular organic material. In these calculations, the standard deviation of the energy disorder, σ, is 4.0 kT, where kT is the thermal energy. Calculations for two different energy disorder models, the Gaussian disorder model (GDM) and the correlated disorder model (CDM) are shown.

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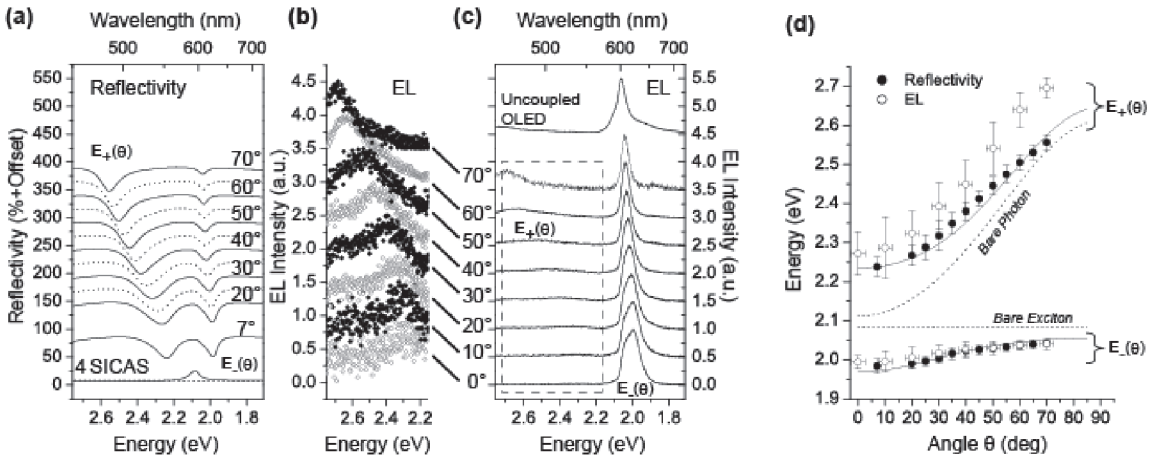
Strong Coupling of Light and Matter in a Microcavity LED

J.R. Tischler, M.S. Bradley, V. Bulović
Sponsorship: DARPA Optocenter, NDSEG, NSF-MRSEC

We have demonstrated the first microcavity light emitting device (LED) in which light emission is produced from strongly coupled states of light and matter by electrical excitation [1]. Applications of strong coupling in atomic and semiconductor systems have led to one-atom zero threshold lasers, high gain polariton parametric amplifiers, and predictions that strong coupling may play a key role in future quantum information processors. These previous experiments have all relied on optical pumping. We achieve strong coupling in the microcavity LED by electrically exciting a 6±1 nm thick film of J-aggregated dye that we embedded into a resonant cavity organic LED (RC-OLED) structure. Specifically, the film of J-aggregated dye is composed of the anionic cyanine dye TDBC. which is electrostatically adsorbed to the cationic polyelectrolyte PDAC (poly diallyldimethylammonium chloride). These films contain a high density of J-aggregated TDBC and therefore have very large peak absorption constant ($\alpha \sim 1.0 \times 10^6$ cm^{-1}). We achieved a coupling strength (Rabi-splitting) of $h\Omega$ = 265±15 meV with 6 nm thick films of active material and even larger coupling strengths should be achievable with thicker films. Figure 1 shows that the device exhibits angular dispersion in the reflectivity and electroluminescence measurements that is characteristic of the strong coupling limit.



▲ Figure 1: Angularly resolved polariton electroluminescence, reflectivity, and dispersion relations for near- resonantly tuned polariton RC-OLED. (a) TE polarized reflectivity. Data of successive measurements are offset by 50 percentage points. The reflectivity at θ = 7° of a 6 nm thick PDAC/TDBC film (4 SICAS), is shown for comparison. (b) Expanded view of higher energy portion of the EL spectra, normalized to emission of the higher energy polariton peak, $E_+(\theta)$, in the λ = 450 nm to λ = 575 nm range. (c) The EL spectra normalized to lower energy polariton peak, $E_-(\theta)$. The EL spectrum at θ = 0° of an uncoupled OLED is shown for comparison. (d) Polariton angular dispersion relation for RC-OLED of parts (a-c) with $E_{ph}(\theta = 0°)$=2.11 eV. The fit is generated from reflectivity data in (a) using the two-state model of Eq. 1 with the coupling interaction, $h\Omega$ = 265 meV.

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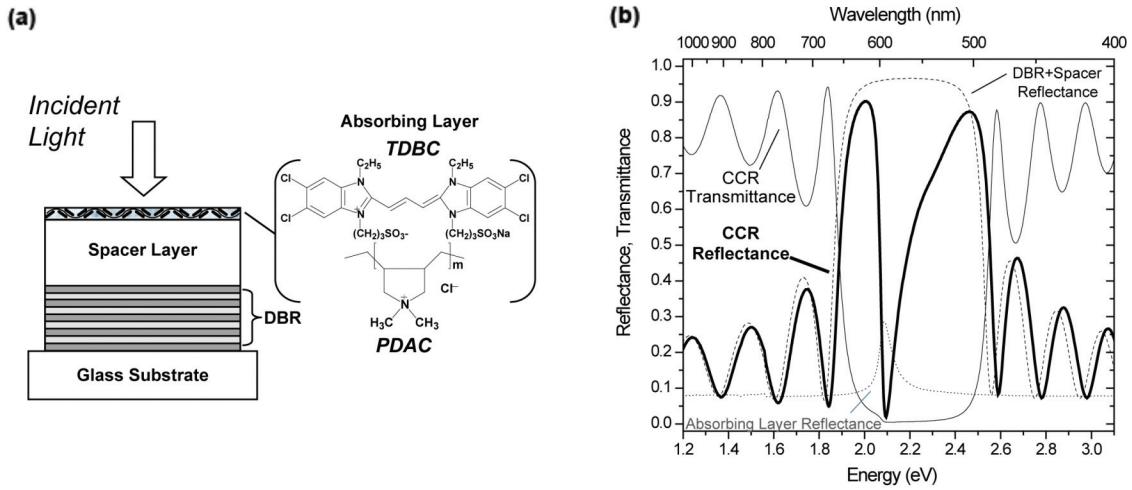
Critically Coupled Resonators in Vertical Geometry, Capable of Absorbing Nearly 100% of Incident Light in a 5 nm thick Absorber Layer

J.R. Tischler, M.S. Bradley, V. Bulović
Sponsorship: DARPA Optocenter, NDSEG, NSF-MRSEC

When light of wavelength λ_c = 584 nm is incident on the critically coupled resonator (CCR) structure illustrated in Figure 1a from the absorbing layer side of the device, the measured reflectance is R = 2%, as shown in Figure 1b [1]. In contrast, for the DBR with spacer but without the absorbing layer, the reflectivity at λ_c = 584 nm exceeds 95%, showing the dramatic change in reflectance due to critical coupling. For the same CCR, the transmittance at λ_c is T = 1%. Consequently, 97% of the incident light is absorbed within the 5.1 ± 0.5 nm thick absorber layer, yielding a maximum effective absorption coefficient of α_{eff}= 6.9x106 cm_{-1}. We developed a generalized model of the CCR phenomenon and have shown through simulation that critical coupling is achievable with a variety of material sets, providing several general conditions are satisfied. Among non-epitaxially grown materials, we can envision building CCR's with organic polymers that are used in biological assays and chemical sensors, with molecular materials that are used in photodetectors and xerographic photoresistors, and in the emerging uses of colloidally grown inorganic nanocrystal quantum-dots (QDs). Application of the CCR phenomenon can also facilitate development of single-photon optics where it is desirable to absorb a photon with 100% probability in the thinnest possible films and of colloidally grown semiconductor saturable absorber mirrors for ultra-fast optical modulators.



▲ Figure 1: a) Critically coupled resonator (CCR) structure. The device consists of a dielectric Bragg reflector (DBR), a transparent spacer layer, and a layer of J-aggregate cyanine dye. The J-aggregate layer consists of the cationic polyelectrolyte, PDAC, and the anionic cyanine dye, TDBC. Reflection and transmission measurements are made with light incident from the J-aggregate side of the device. b) Reflectance and transmittance data for the CCR with spacer layer thickness of 90 ± 1 nm, along with reflectance data for the neat PDAC/TDBC film and for the dielectric stack consisting of DBR with spacer layer. At λ_c=584 nm, the CCR absorbs 97% of incident light.

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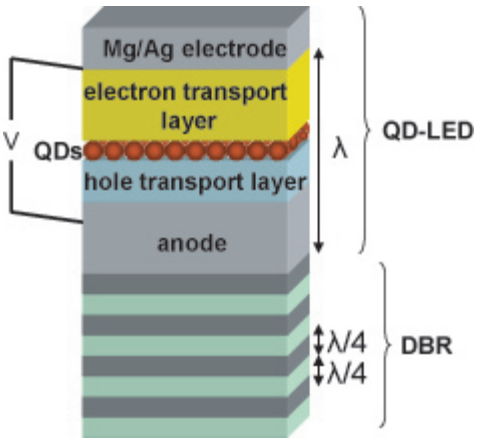
Resonant Cavity Quantum Dot LEDs

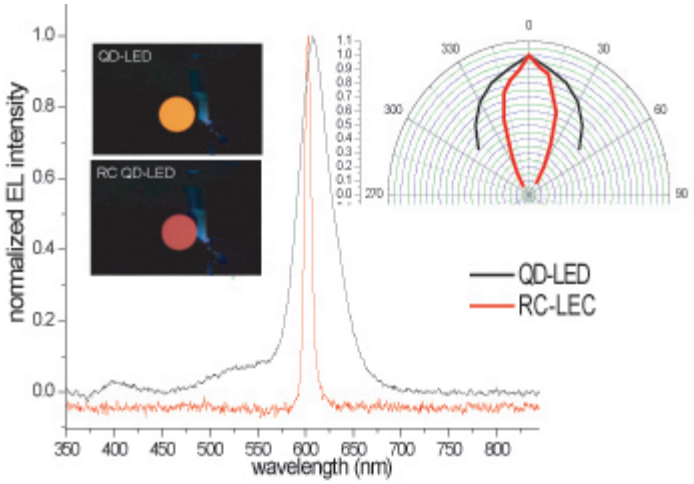
V. Wood, J.R. Tischler, V. Bulović
Sponsorship: NSF, PECASE

Quantum dot LEDs (QD-LEDs), which capitalize on the excellent color saturation and high photoluminescence efficiencies offered by quantum dots, promise to be part of future generations of display technologies [1]. The goal of our project is to integrate the already developed technology of the QD-LED into a resonant cavity (RC) and thereby achieve enhanced, directed electroluminescence (EL) that can be of use in fields as diverse as optical communications, spectroscopy, and environmental and industrial sensing.

The RC structure we are currently investigating (Figure 1) consists of a standard QD-LED [1] grown on top of a distributed Bragg reflector (DBR). A DBR is a highly reflective mirror made of $\lambda/4$ layers of alternating high and low indices of refraction. With a reflectivity of more than 98% in the wavelength region of interest, the DBR serves as one of the cavity mirrors. The other cavity mirror is the Ag doped Mg electrode of the QD-LED. With this structure, we have achieved narrowed emission, which is evident when comparing EL spectra and images of the QD-LED and the RC QD-LED (Figure 2). The QD-LED appears orange because our eyes sense the red light of the QDs as well as the shorter wavelength emission from the organics. In contrast, the RC QD-LED exhibits effectively monochromatic red light. The plot of peak emission intensity at different angles (Figure 2) shows an emission cone of less than twenty degrees. If the path-length of the cavity does not match the QD emission wavelength, EL from the RC QD-LED is off-normal. We are currently working to understand the emission enhancement capability of our RC QD-LED.



▲ Figure 1: Schematic of RC QD-LED.



▲ Figure 2: Comparison of EL spectra, images, and angular emission profiles of RC QD-LED and QD-LED. The RC QD-LED exhibits marked narrowing.

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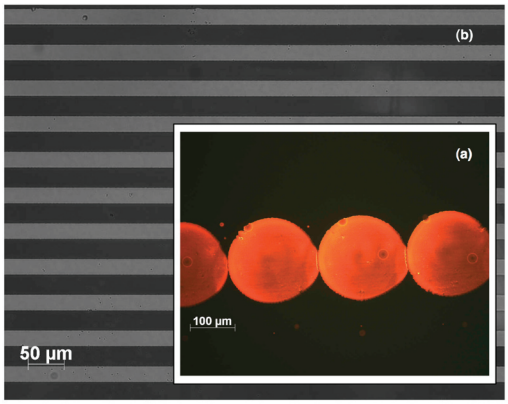
Patterning Micron-Sized Features of Quantum Dots and Metal Electrodes

J. Yu, J. Chen, V. Bulović
Sponsorship: ISN, NSF Materials Research Science and Engineering Center at MIT, PECASE

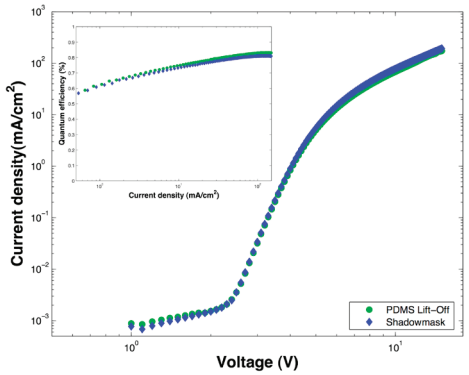
Organic LEDs (OLED) and quantum-dot LEDs (QD-LED) are promising technologies for the emissive element in flat panel displays. However, organic material in these devices is sensitive to solvent exposure and creates processing challenges in patterning a pixelated display. This project aims to develop novel fabrication processes for OLED and QD-LED displays.

In QD-LEDs, quantum dots can be patterned by spin-casting a monolayer onto a relief poly(dimethylsiloxane) (PDMS) stamp and then transferring the pattern onto an organic substrate [1]. However, the spin-cast process requires significant use of material. An alternative solution is to directly pattern the dots using thermal inkjet pico-fluidic drop dispensing system (TIPS) provided by Hewlett-Packard (Figure 1a). A process for formation of patterned monolayer using this technique is currently being developed.

Patterning of electrodes in OLED or QD-LED displays presently is done primarily by shadow masking, which is limited in resolution; or cold-welding, which requires high pressures, additional protection layers, use of gold electrode, or subsequent dry etching steps [2-3]. Recently transfer printing has been demonstrated with PDMS on various materials [4]. We are investigating subtractive pattering of silver or silver-magnesium electrodes with untreated PDMS stamp. We demonstrated 25 micron-sized features with good yield on 20 nm thick silver-magnesium films (Figure 1b). This PDMS lift-off technique applied on an OLED electrode made of 50 nm silver film on top of 50 nm silver-magnesium yields OLEDs with the same quantum efficiency and current voltage characteristics to OLEDs defined by shadow masking (Figure 2).



▲ Figure 1: a) Patterned quantum dot features using TIPs system. b) PDMS lift-off of 20-nm-thick silver-magnesium electrodes.



▲ Figure 2: Comparison of current voltage characteristics for shadow-masked and PDMS lift-off electrode for typical ITO, PEDOT, 50-nm Alq_3, 50-nm TPD, 50-nm Mg:Ag, 50-nm Ag OLED. Inset: Quantum efficiency vs. current characteristics.

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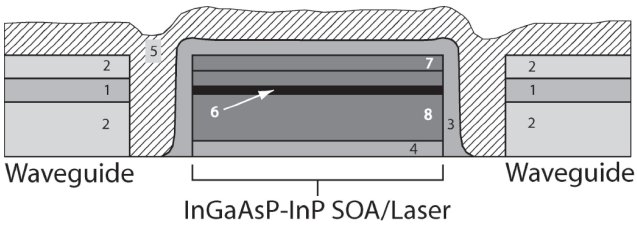
SiO_xN_y Waveguides on Si and Optical Coupling to Co-Axial RM^3 Integrated Devices

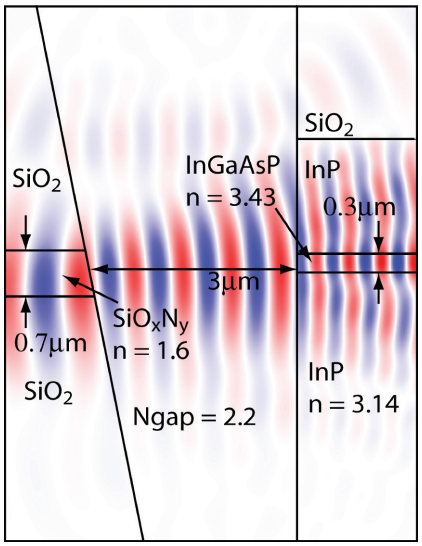
E.R. Barkley, J.J. Rumpler, J.M. Perkins, S. Famini, C.G. Fonstad, Jr.
Sponsorship: DARPA

We present research in progress on the design, fabrication, and characterization of rectangular, buried-channel silicon oxynitride waveguides. We are currently pursuing optoelectronic device integration on silicon for both in-plane and surface normal optical interconnects using the recess mounting with monolithic metallization (RM^3) technique. The waveguides associated with this work provide co-axial optical guiding and coupling for the case of in-plane optical interconnects. These single-mode waveguides have been designed to provide minimum propagation loss and maximum optical coupling to/from an RM^3 integrated InGaAsP/InP semiconductor optical amplifier (SOA) or laser. Figure 1 shows a schematic cross-section (in the wafer surface normal and propagation direction plane or y-z plane) showing an integrated SOA and a silicon oxynitride waveguide.

The optimum waveguide design is based on the optimization of a series of tradeoffs such as the tradeoff between maximized coupling and reduced sensitivity to vertical and lateral device misalignment. These design tradeoffs will be illustrated through a series of finite difference time domain (FDTD) simulation results. A typical simulation is shown in Figure 2. Fabry-Perot waveguide loss measurements showing fabricated waveguide propagation losses below 5 dB/cm will also be shown. Finally, the latest experimental results from a recently designed test chip will be included.



▲ Figure 1: An RM^3 integrated SOA/laser schematic: 1) Silicon oxynitride waveguide core, 2) SiO_2 waveguide cladding, 3) reflection control material 4) Au/Sn device bonding/contact material, 5) gap-fill material (BCB, Si_3N_4, or TiO_2), 6) InGaAsP core material, 7) SOA/laser ridge, and 8) InP cladding material.



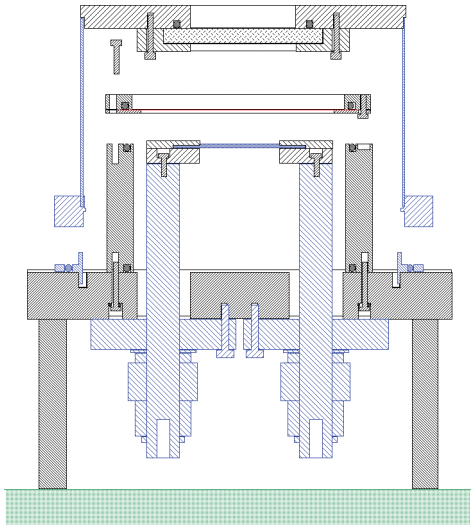
▲ Figure 2: Electric field-strength contour plot taken from a FDTD simulation. This particular simulation shows the optimum silicon oxynitride waveguide parameters for coupling from a waveguide with unintentionally angled sidewalls to an InGaAsP/InP SOA. We are currently exploring TiO_2 for use as the high refractive index gap-fill material.

A Bonding Apparatus for OptoPill Assembly

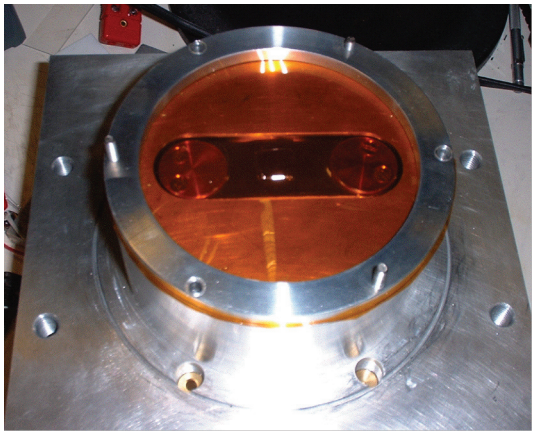
C.A. Cooper, J.M. Perkins, C.G. Fonstad, Jr.
Sponsorship: MARCO IFC, NSF

The central objective of our heterogeneous integration effort is to integrate III-V functionality, such as laser emission, with Si CMOS circuitry in a manner that retains all of the advantages of multi-wafer, batch processing that have propelled Si ICs along the Moore's Law performance timeline for so long. To this end we have developed recess mounting with monolithic integration (RM^3), in which we place III-V heterostructure pills, OptoPills, in recesses 5 to 6 microns deep and 50 microns in diameter that are formed in the inter-metal dielectric layers covering a processed Si IC. We then interconnect them monolithically with the underlying circuitry.

Once the heterostructure device pills have been placed in their recesses, whether by means of micro-scale pick and place or fluidic self-assembly (both described in other abstracts), they must be securely fastened in place. It is also often desired that a good electrical contact be made to the bottom of the pill at the same time. Two different solders have been found to be particularly suitable for this purpose: a Au-Sn eutectic to solder gold-coated pills into the recesses, and a Pd-Sn-Pd stack to bond bare pills into the recesses. In both cases it is necessary to supply pressure between the pill and substrate to reliably achieve successful bonding or soldering. To apply the required pressure to these micro-scale pills, particularly when they are in recesses, we have developed a bonding system, shown in Figure 1, in which a vacuum-bagging film and a pressure differential are used to apply a controlled, reproducible, and uniform pressure simultaneously to all the pills on a wafer. A photograph of the unit, with the outer chamber removed so the film is visible, is shown in Figure 2. Typical bonding conditions used involve a pressure of approximately 50 psi and a temperature of approximately 200˚C.



▲ Figure 1: Cross-sectional drawing of the bonding chamber showing the base plate with heater strip, the inner bonding-ambient chamber, the film holder plate, and the outer pressurized chamber.



▲ Figure 2: The film-pressure bonding system shown with the outer, pressurized chamber removed to show the film and heater strip.

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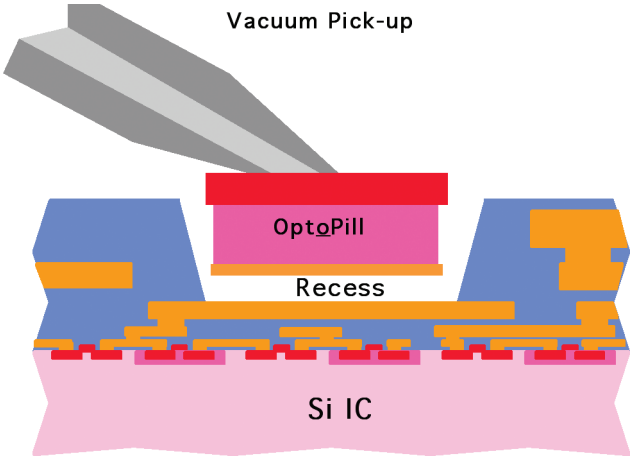
[1] M.S. Teo, "Development of pick-and-place techniques for monolithic OptoPill integration," Master's thesis, Massachusetts Institute of Technology, Cambridge, 2005.

Micro-scale Pick-and-Place Integration of III-V Devices on Silicon

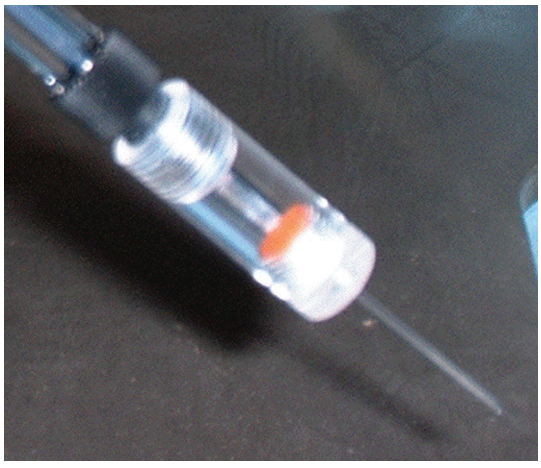
J.M. Perkins, C.A. Cooper, C.G. Fonstad, Jr.
Sponsorship: MARCO IFC, NSF

We are developing micro-scale assembly techniques for integrating III-V optoelectronic devices on silicon integrated circuits that blur the practical distinction between hybrid and monolithic integration. Our general approach, which we term Recess mounting with monolithic integration (RM^3) involves forming recesses 5 to 6 microns deep and 50 microns in diameter, in the inter-metal dielectric layers covering a processed Si IC. After all of the standard silicon processing is completed, the Si IC wafers for RM^3 integration undergo further back-end processing first to create the recesses, and to then place and bond III-V device structures in them. Wafer-level processing is then continued to complete any remaining III-V device processing and to interconnect those devices with the underlying electronic circuitry. One approach we have taken to placing the III-V devices in recesses has been to form discrete heterostructure pills the size of the recesses, and the then place them individually into the recesses using micro-scale pick-and-place assembly, as illustrated in Figure 1.

The dimensions of the pills we are assembling are much smaller than the die normally encountered in pick-and-place applications, and thus conventionally available vacuum pick-up tools are not suitable. We have found, however, that quartz micropipettes of the type used by microbiologists to study cells can be fabricated with the right dimensions and geometry for this application. In particular, we use micropipettes pulled from 1-mm-diameter, 0.25-mm-wall quartz tubing and tapered down over 7 mm to a tip diameter of 30 microns. The tip is beveled at 45˚ to complete the pick-up tool. A photomicrograph of a tool mounted in its holder is shown in Figure 2. With this tool, pills can be picked up, placed in a recess, and released without damaging the pills [1]. Our current effort is directed at both using micro-scale pick and place to do heterogeneous integration, and further developing and refining the technique.



▲ Figure 1: A cartoon illustrating the micro-scale pick and place process for locating a heterostructure device pill in a recess on a Si IC wafer surface.



▲ Figure 2: A quartz micropipette pick-up tool mounted on its holder.

REFERENCES

[1] M.S. Teo, "Development of pick-and-place techniques for monolithic OptoPill integration," Master's thesis, Massachusetts Institute of Technology, Cambridge,2005.

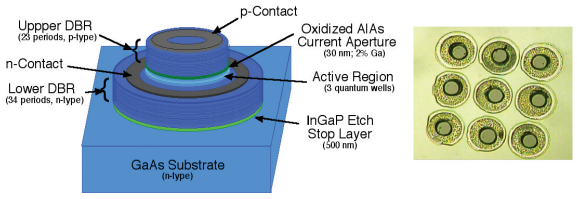
AlGaAs/GaAs VCSEL Processing and Heterogeneous Integration with Si ICs

J.M. Perkins, C.G. Fonstad, Jr.
Sponsorship: MARCO IFC

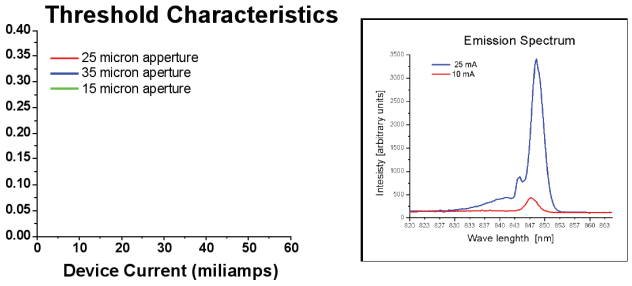
The goal of this research is to integrate AlGaAs vertical cavity surface-emitting lasers (VCSELs) onto a preprocessed Si IC, enabling creation of an intimately integrated hybrid circuit of CMOS devices and III-V laser diodes for interconnect applications. Pick-and-Place integration as well as magnetically assisted statistical assembly will be used [1-2]. These techniques will insert the III-V devices onto the target IC. These devices can then be solder-bonded in place, securing and electrically connecting them to the IC.

A technique, using AlGaAs 850 nm VCSEL heterostructure device material to produce optopills, has been developed to allow this hybrid integration. Mesa etching, ohmic metalization, current aperture formation, and selective removal have been studied. Oxide aperture growth has been performed and a non-invasive technique has been developed to characterize these oxide current apertures. Low-resistance contacts have been obtained, producing devices with 1.5-volt turn-on voltages. I-V, L-I, and spectral characteristics have been obtained and lasing is observed. A technique has been developed to metalize and pattern the backside of these devices, enabling metal-metal integration bonding, as well as enabling the inclusion of a backside magnetically susceptible Ni layer needed for MASA integration. Fully processed pill devices have been obtained. A CMOS neural network IC has been designed and fabricated [3].

Initial integration work has begun. Recesses have been made opening to an aluminum backplane and a Au/Sn stack has been patterned within the recesses to provide a bonding alloy. The VCSEL pills have been metalized with a stack that includes a Au top-bonding layer, using the backside liftoff technique. They have been placed within these recesses metal-side down. These devices can be maneuvered to center them within the wells. A modified bonding scheme has been developed and successfully used to bond these devices and anneal their contacts. A polymer film presses down on the pills at 30 psi to produce the compressive force needed in the Au/Sn bonding process. An Al film between the sample and the polymer pressure film has been used to prevent the devices from sticking to the polymer and ripping them off after bonding. The bonded devices have been shown to be connected to the aluminum backplane and to have good device characteristics. A novel post bonding passivation and metalization scheme has been developed and will be tested. Heat dissipation modeling is being developed to determine the operation temperature of these devices and how it depends on the surrounding circuitry environment.



▲ Figure 1: (left) Diagram of a VCSEL opto-pill processed until the release step. First mirror etch exposes n-type layer for metalization, while also exposing the aperture layer for wet oxidation. Top metalized contacts allow prerelease device characterization. (right) Bonded pills in Al recesses. No aperture or top metallization.



▲ Figure 2: (left) Luminescence characteristics of apertured VCSEL devices on native substrate. (right) Emission spectrum for 10 and 25 milliamps device currents for a nonapertured 35 micron device.

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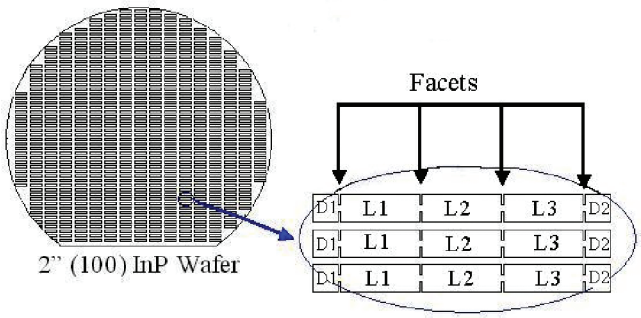
Highly Integrable In-Plane Laser Diodes for Optoelectronic Integration

J.J. Rumpler, E.R. Barkley, J.M. Perkins, C.G. Fonstad, Jr.
Sponsorship: DARPA

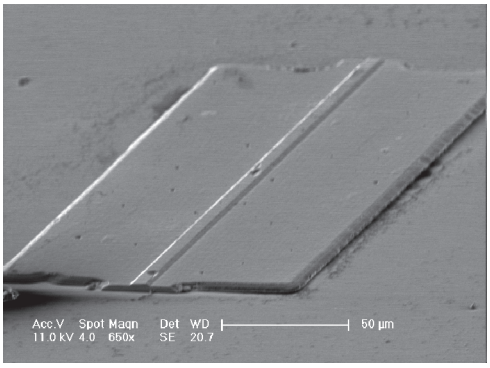
The level of integration seen in commercial active photonic devices is at most a laser monolithically integrated with a modulator or a photodetector flip-chip bonded to an optical waveguide. Our goal is to achieve much larger levels of optoelectronic integration, and our approach involves optimally fabricating building blocks, such as laser diodes or optical amplifiers, and assembling these blocks in dielectric recesses on a system substrate [1]. Our test case for demonstrating this technology is the integration of 1.55 μm InGaAsP edge-emitting laser diode blocks with planar silicon oxy-nitride waveguides on silicon.

To this end, a process has been developed to fabricate freestanding edge-emitting laser diodes by our newly developed micro-cleaving technique. This process begins with a (100)-oriented InP wafer upon which an in-plane laser heterostructure has been grown. After defining the laser ridge on the top-side of the substrate, the wafer frontside is patterned into large arrays of rectangular bars aligned with the laser ridges and wafer flat so that short and long faces of the rectangular bars are aligned with the two cleavage planes as shown in Figure 1. Notches in the rectangular bars divide each rectangular bar into three rectangular sub-bars in between two square sub-bars. The rectangular sub-bars define the active devices, L1, L2, and L3, and the square sub-bars at the ends define dummy devices D1 and D2.

Once the bar pattern is formed on the semiconductor wafer, a chemical-etch resistant layer is applied to the wafer surface and the semiconductor substrate is removed using a hydrochloric acid-based, selective wet-etch chemistry that stops on an InGaAs etch stop layer. The etch-resistant layer is then dissolved and the long bars are collected in solution. The long bars are then agitated ultrasonically in this solution at which time they preferentially cleave in the notch region forming a large quantity of active devices and dummy devices. An individual cleaved laser platelet is seen in Figure 2.



▲ Figure 1: Schematic depicting the micro-cleave enabling pattern and how it must be aligned properly to the semiconductor.



▲ Figure 2: SEM image of a micro-cleaved edge emitting laser platelet with a ridge defined.

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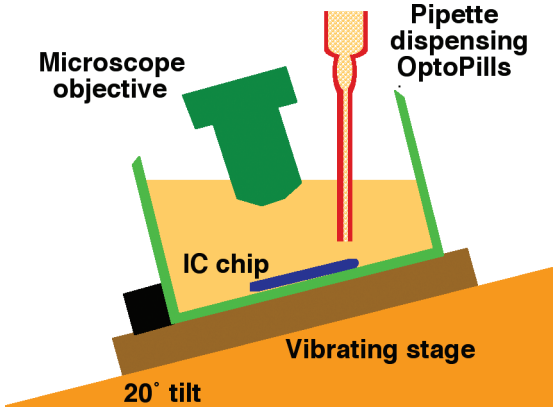
Magnetically Assisted Statistical Assembly of III-V Devices on CMOS

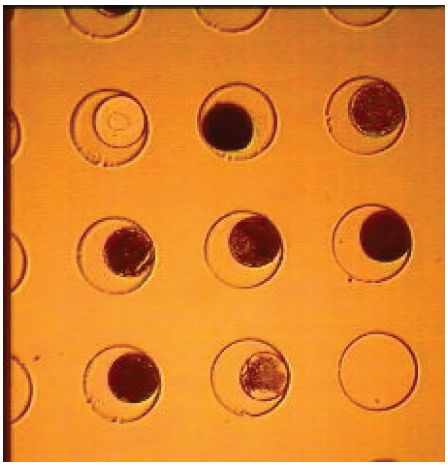
J.J. Rumpler, J.M. Perkins, C.G. Fonstad, Jr.
Sponsorship: MARCO IFC, NSF

Development of an efficient process for integrating III-V devices on silicon CMOS is key to making optical interconnects a reality on the micro-scale as well as enabling low cost and compact optoelectronic sensors for applications such as biomedicine. The III-V semiconductors typically have superior lasing properties and high electron mobilities making make them attractive for applications such as optical sources and RF electronics. Silicon is the material of choice for large-scale digital circuits because of its ability to form a high-quality, low-defect oxide, thus enabling low-power CMOS technology. Unfortunately, direct epitaxy of III-V devices on silicon is not practical due to mismatches between the lattice constant and thermal expansion coefficient of the materials. Therefore, III-V device integration on CMOS today consists of at most small arrays of devices attached by flip-chip or wire bonding. Our approach is aimed at permitting large-scale integration of these heterogeneous materials. Specifically, III-V and silicon devices are processed separately under optimal conditions on their own native substrates. On the CMOS wafer surface, dielectric recesses are formed. At the bottom of these recesses are located patterned permanent ferromagnetic films. Once fabricated, the III-V devices having a permeable ferromagnetic film are released from their substrate and flowed over the CMOS wafer where they assemble in the recesses by gravity and are retained by short-range magnetic forces. Experimentally, the III-V devices are found to stick to the permanent magnetic film due to the large magnetic adhesion force [1].

Experiments have been conducted whereby thousands of these 45-micron diameter, 6-micron thick III-V devices are flowed over a target substrate consisting of hundreds of correspondingly sized dielectric recesses as shown in Figure 1. Initial fluidic assembly experiments without magnetic retention show that a large number of successfully assembled pills, as shown in Figure 2. They are also found to readily come out of the recesses as the substrate is removed from the fluid, which verifies the need for a short-range retention force.



▲ Figure 1: Assembly setup.



▲ Figure 2: An array of silicon dioxide recesses filled by GaAs devices.

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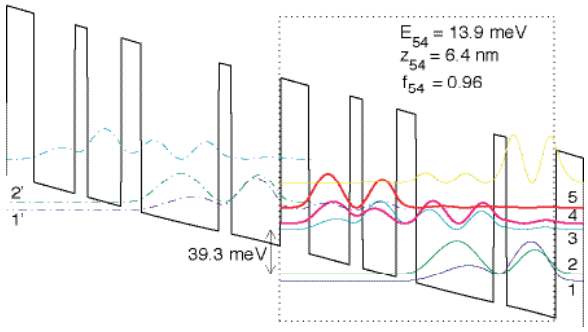
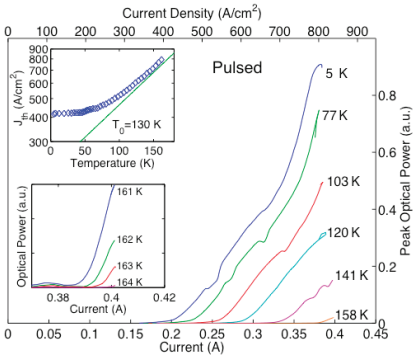
Development of Terahertz Quantum Cascade Lasers

B. Williams, H. Callebaut, S. Kumar, Q. Qin, Q. Hu (in coll. with J. Reno, Sandia National Laboratories)
Sponsorship: NSF, NASA, AFOSR

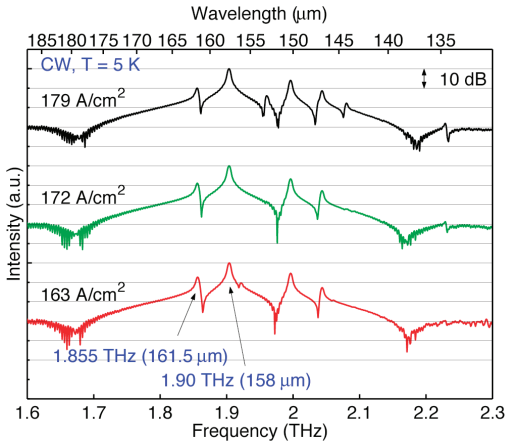
The terahertz frequency range (1-10 THz) has long remained undeveloped, mainly due to the lack of compact, coherent radiation sources. Transitions between subbands in semiconductor quantum wells were suggested as a method to generate long wavelength radiation at customizable frequencies. However, because of difficulties in achieving population inversion between narrowly separated subbands and mode confinement at long wavelengths, THz lasers based on intersubband transitions were developed only very recently. We have developed THz quantum-cascade lasers based on resonant-phonon-assisted depopulation and using metal-metal waveguides for mode confinement. Figure 1 illustrates the schematics of both features are illustrated. Using the combination of these two unique features, we have developed many THz QCLs with record performance, including a maximum pulsed operating temperature at 164 K (see Figure 2), a maximum power of ~250 mW, and the longest wavelength (~161 μm) QCL to date without the assistance of magnetic fields.



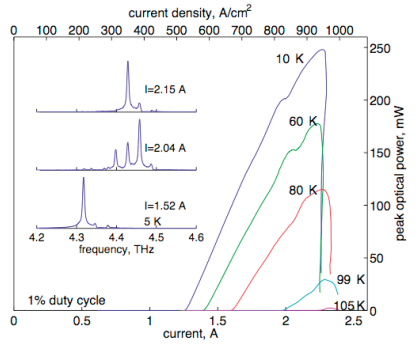
▲ Figure 1



▲ Figure 2



▲ Figure 3



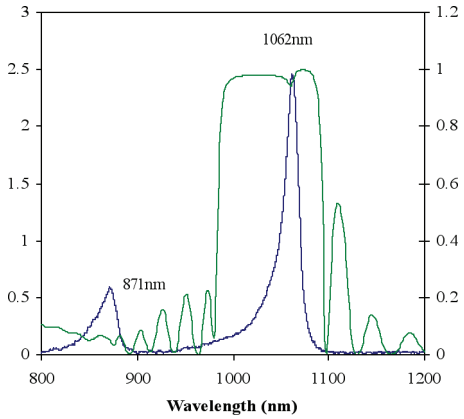
▲ Figure 4

Broadband, Saturable Bragg Reflectors for Mode-locking, Ultrafast Lasers

G. Petrich, F. Kaertner, E. Ippen, L.A. Kolodziejski
Sponsorship: NSF, ONR MURI, DARPA, Q-Peak Inc.

Self-starting, mode-locked, ultrafast lasers require broadband high reflectivity mirrors with saturable absorbers. However, AlAs/GaAs or AlAs/AlGaAs mirrors with saturable absorbers exhibit a limited bandwidth due to the low index-contrast between the individual GaAs and AlGaAs layers, but these mirrors are suitable for mode-locking 1064-nm lasers. Figure 1 shows the reflectivity, as measured using a Varian Cary 500i spectrophotometer, and the room temperature photoluminescence from a saturable Bragg reflector (SBR) consisting of 25 pairs of 88-nm-thick $Al_{0.95}Ga_{0.05}As$ layers and 74.7-nm-thick GaAs layers with two 8-nm-thick $In_{0.27}Ga_{0.73}As$ quantum wells separated by 16 nm of GaAs centered within 117 nm of GaAs. The dip in the reflectivity that is due to the InGaAs quantum wells is easily observed.

In addition, two oxidizable saturable Bragg reflectors have been grown by molecular beam epitaxy. The SBRs consist of two 8-nm-thick InGaAs quantum wells separated by GaAs with GaAs cladding layers on a 7-pair oxidizable InGaP/AlAs dielectric stack. By thermally oxidizing the AlAs layers to form Al_xO_y, broadband reflectors can be created. The photoluminescence that is measured from the as-grown SBRs exhibit emission at 1062 +/- 2 nm. The AlAs/InGaP mirror stacks have not been oxidized thus far.



▲ Figure 1: The reflectivity and photoluminescence of an InGaAs/GaAs absorber on an AlGaAs/GaAs distributed Bragg reflector.

A Nanoelectromechanically Tunable, High-Index-Contrast Interference Directional Coupler

R.E. Bryant, M.L. Povinelli, S.G. Johnson, G.S. Petrich, J.D. Joannopoulos, E.P. Ippen, L.A. Kolodziejski
Sponsorship: NSF-MRSEC

One of the most exciting and practical application of a directional coupler is the switch modulator in which the amount of optical power coupling is adjustable. A method of tuning a single mode interference high-index-contrast (HIC) directional coupler with a nanoelectromechanical (NEM) mechanism is proposed. An electomechanically tunable directional coupler has the benefit of providing large changes in effective index, of being transparent, and requiring low power. An HIC system has the added benefit of permitting a size reduction that allows machined nanostructures to optically guide light at a wavelength of 1.55 microns as well as to mechanically actuate.

Using GaAs waveguides with a ~300-nm-square cross-section, directional couplers are fabricated so that they are anchored atop of Al_xO_y as well as suspended over a trench. The anchored portions of the waveguides are adiabatically curved to a lithographically-defined coupling separation that exists suspended over the trench. The desired mechanical compliance determines the extent to which the adiabic curves are situated over the trench. The amount of optical power coupling is adjusted by the electromechanical actuation of the waveguide separation and the S-bend curvature. The selected method of electromechanical actuation utilizes a gap-closer mechanism. A gap-closer is a "spring"-suspended, parallel capacitive plate mechanism that is allowed to mechanically deflect in order to reduce its capacitance. In planar MEMS/NEMS, the "spring" is usually a mechanical compliant beam (i.e., the suspended portion of the directional coupler). Gap-closers are characterized by large mechanical force densities over small displacements, which make them well suited for this particular application.

Molecular beam epitaxy is used to define layer thickness. Traditional micromachining techniques are used to lithographically define the topology and provide optical, electrical, and mechanical isolation. After these processes, high-index-contrast is accomplished by stream oxidation that transforms crystalline high Al-content $Al_xGa_{1-x}As$ alloys to an amorphous Al_xO_y oxide. Nanostructure mechanical latches and bi-stable mechanisms are expected to aid in improving alignment accuracy. Nanostructure mechanical levers can be used to tailor the shape and angle of deflection. The device is expected to operate within the MHz regime in a speed-optimized design.

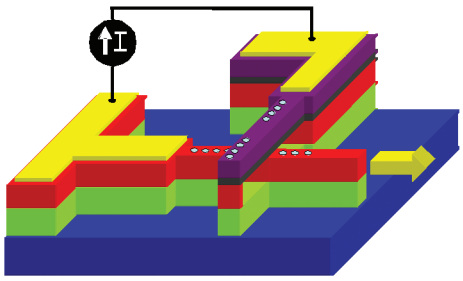
Electrically-Activated Nanocavity Laser Using One-Dimensional Photonic Crystals

A. Grine, G.S. Petrich, L.A. Kolodziejski
Sponsorship: NSF-MRSEC

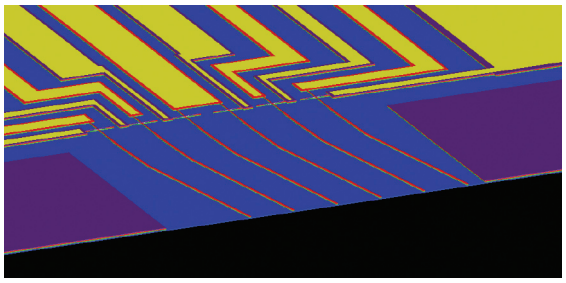
The focus of this project is the design and fabrication of a laser that is suitable as a light source for integrated optics. Four characteristics make the laser particularly advantageous for use in integrated optics. First, the laser is electrically activated and eliminates the need for a separate pump laser. Second, the laser requires only 25 μm^2 of space, which conserves chip real-estate and should lead to a relatively small threshold power. Third, the output of the laser is directly connected to the output waveguide, eliminating the need for separate couplers. Finally, the laser's output is coplanar, which eases integration with other components.

The laser design (Figure 1) incorporates one-dimensional (1-D) photonic crystals patterned on two crossing waveguides. The nanocavity, located at the two waveguide's intersection, creates a high-Q optical resonator with the 1-D photonic crystals acting as highly reflective mirrors. By removing some of the holes in one of the photonic crystals, one can control the direction of the emitted light. The top GaAs-based waveguide is doped p-type, while the bottom, InGaAlP-based waveguide, is doped n-type, so that a p-n diode exists only in the area where the waveguides overlap. The top GaAs waveguide contains a quantum dots-in-a-well structure, which serves as the active material for the laser. Optical simulations have led to the inclusion of a high-index InGaP layer in the center of the output waveguide. The inclusion of the InGaP layer allows more light to be coupled into the output waveguide and a thinner upper waveguide to be used to minimize the loss due to radiation. The output waveguide is designed to be multi-mode in order to minimize the fabrication time.

A new fabrication sequence has been developed that employs either electron-beam or focused-ion-beam lithography to define the sub-micron features and photolithography to define the larger features, allowing many lasers with varying dimensions to efficiently be processed on a single chip. A die measuring ~ ¼" x ¼" contains 280 devices, each with varying features. This method will allow the empirical determination of the optimal device. To ease the electron-beam lithography process, the mask unit cell contains an array of six devices to be processed within a 200-μm square electron-beam field (Figure 2). Current work includes the fabrication of the device in the Technology Research Laboratory. Once the device is fabricated, testing will take place in collaboration with the Ultrafast Optics and Quantum Electronics Group.



▲ Figure 1: Depiction of the electrically-activated, photonic-crystal nanocavity laser. The green arrow represents the direction and location of the emitted light.



▲ Figure 2: Schematic of an array of 6 lasers within a 200-μm field. The output waveguide is 164 μm long and is angled 11° with respect to the facet.

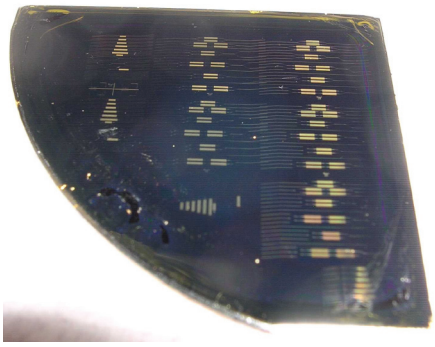
Photonic Integrated Circuits for Ultrafast Optical Logic

R. Williams, A. Markina, G.S. Petrich, E.P. Ippen, R.J. Ram, L.A. Kolodziejski
Sponsorship: DARPA

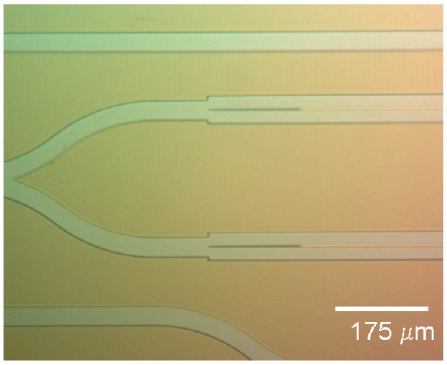
With an increasing demand for higher speed switching technologies in optical telecommunications networks, interest in both all-optical switching schemes and monolithic integration of photonic components is increasing. Reducing or eliminating optical-electronic-optical (OEO) conversions offers advantages of higher bit rates, lower power consumption, and reductions in size and weight.

The current study aims to demonstrate an optical gate consisting of semiconductor optical amplifiers (SOAs) integrated into a Mach-Zehnder interferometer on InP substrates. The optical gate is capable of basic Boolean functionality, wavelength conversion, and other important switching operations. Prior to fabrication, the design of the components such as the InGaAsP quaternary dilute waveguide, the multi-mode interferometers, and the adiabatic taper geometry has been optimized using standard optical simulation techniques.

To integrate the active SOA devices with the passive components, an asymmetric twin waveguide approach, which eliminates the need for regrowth at the expense of additional processing steps, is employed. The first-generation design contained two separate die: one consisting of basic isolated components and the other consisting of integrated components (Figure 1). Upon the completion of the processing and testing, further optimizations of the design and fabrication process were incorporated into a second-generation design that is currently undergoing fabrication on campus and in collaboration with Lincoln Laboratory. The second-generation design combines both the active and passive devices into single die suitable for a step-and-repeat mask set, allowing for sharper tapers and smoother waveguide bends. Processing improvements include depositing the base metal for the top-side contact prior to any III-V etching, minimizing the amount of InP-based etching through the use of trenches, and using a dedicated CH_4/H_2 etcher at Lincoln Laboratory. Figure 2 shows the tips of the upper active waveguide and the trench in which the passive waveguides will be centered.



▲ Figure 1: A photograph of the first-generation fabricated dies on a quarter of a 2" InP wafer.



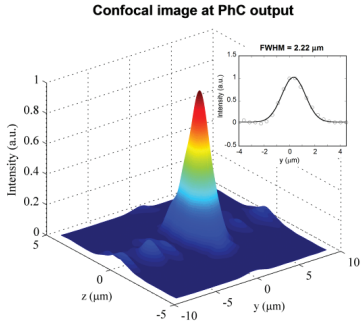
▲ Figure 2: A photograph of the beginning of the second-generation Mach Zehnder interferometer.

Super-collimation of Light in Photonic Crystal Slabs

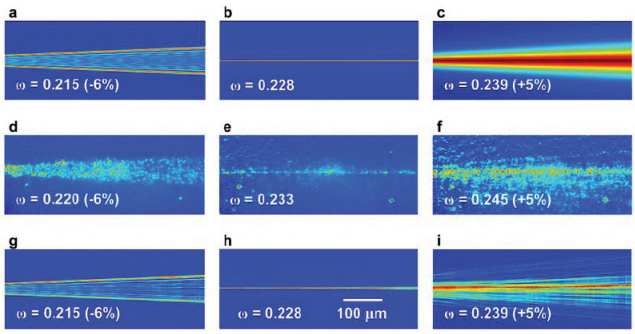
S.N. Tandon, M. Dahlem, P. Rakich, M. Ibanescu, M. Soljacic, G.S. Petrich, J.D. Joannopoulos, E.P. Ippen, L.A. Kolodziejski
Sponsorship: NSF-MRSEC, MARCO IFC

A super-collimator is a device in which light is guided by the dispersion properties of a photonic crystal slab rather than by defects or by traditional waveguiding structures. Photonic crystals (PhC) form the essence of the super-collimation effect. The super-collimator consists of a two-dimensional PhC composed of a square lattice of cylindrical air holes etched into a high-index material such as silicon. The device was fabricated using a silicon-on-insulator wafer in which the low-index oxide layer (3 μm thick) is used to minimize radiation loss into the high-index silicon substrate. The photonic crystal occupies the entire surface of the super-collimator so that the cleaved edges of the photonic crystal function as input or output facets of the device. The initial design has focused on realizing super-collimation at a wavelength of 1500 nm so that the hole lattice constant, hole radius, and Si thickness were 350 nm, 105 nm and 200 nm, respectively.

Testing of the super-collimator device has been performed in collaboration with the Ultra-fast Optics Group. Figure 1 shows the output of the propagating beam from a cleaved facet after traversing the PhC for 5 mm where the 1-μm-diameter incident optical beam exiting the device was found to be 2-μm wide. By defining the isotropic diffraction length to be the length over which the light beam spreads by root 2, super-collimation for more than 600 isotropic diffraction lengths has been observed. Using an infrared-camera to image the scattered light, the light propagating through the photonic crystal was observed at a number of different wavelengths. Figure 2a-c shows the simulated propagation of light through an ideal photonic crystal, while Figure 2d-f shows the measured scattered light as the light propagated through the super-collimator. Figure 2e shows that at a normalized frequency of ω=0.233 (λ=1510 nm), light propagates through the photonic crystal in a collimated fashion as the light path resembles a stripe of light. As the normalized frequency of the input laser is varied from ω=0.233, the beam no longer exhibits a collimated behavior and begins to diverge, with the beam width expanding as it propagates. The inclusion of short-range, fabrication-related disorder can improve the agreement between the measured light propagation and the simulated results (Figure 2g-i).



▲ Figure 1: Output measured at the facet of the device for a super-collimating beam that has propagated for 5 mm inside a photonic crystal silicon slab.



▲ Figure 2: (a-c) Theoretical beam evolution generated by the beam propagation method to be compared with experiment d-f. (d-f) Top-view experimental images of light traveling through the photonic crystal at wavelengths of 1430 nm, 1510 nm and 1610 nm that were obtained from an IR camera. g-i, Simulations of the beam evolution including the effects of short-range disorder.

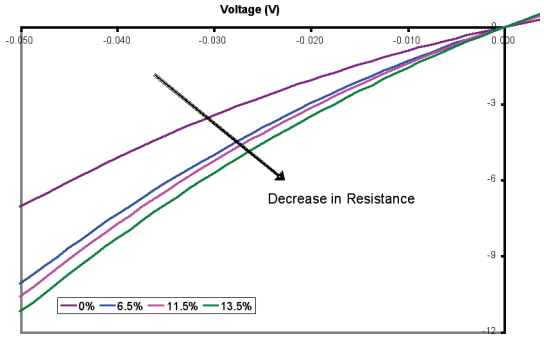
Tunnel Junction Diodes

S.Y. Young, R.D. Williams G.S. Petrich, R.J. Ram, L.A. Kolodziejski
Sponsorship: DARPA

The goal of this project is to characterize the tunneling behavior in InGaAs/GaAs tunnel junction diodes for use in tunnel-junction-coupled lasers. The reversed-bias leakage current of the tunnel junctions can be exploited to epitaxially connect more than one lasing active region in series. The tunneling of electrons from the valence band of one active region to the conduction band of a second active region can increase the external quantum efficiency of the overall device by allowing multiple photons to be emitted per injected carrier. Thus, low tunneling resistances are desired for high-efficiency lasers.

The InGaAs/GaAs tunnel junction diodes were grown with varying indium contents ranging from 6.5% to 13.5% while the diameter of the fabricated diode mesas ranged from 3.5 μm to 90 μm. Variable-angle spectroscopic ellipsometry was performed on the epiwafers to determine the InGaAs composition and the epilayer thickness. Under both forward and reverse bias, the InGaAs tunnel junction diodes matched the theoretically predicted electrical behavior. First, the tunneling resistance decreased for increasing contact size, but, more importantly, the resistance decreased with increasing indium content (Figure 1).

The results demonstrate that more electrons tunnel across the tunnel junction as the amount of indium is increased due to the decrease of the InGaAs bandgap. Additional tests also demonstrated that annealing the metal-semiconductor contact reduced the diode's overall resistance and that reducing the diode's temperature increased the tunnel junction resistance. With tunneling successfully demonstrated, the InGaAs tunnel junctions were implemented in GaAs-based, two-stage lasers. Significant increases in efficiency of the tunnel-junction-coupled lasers are anticipated in future work.



▲ Figure 1: The reverse-bias current-density response, demonstrating a decrease in resistance for increasing indium content.

Ultrabroadband Modulator Arrays

G.S. Petrich, F.X. Kaertner, E.P. Ippen, L.A. Kolodziejski
Sponsorship: DARPA

Creating an arbitrary optical waveform at wavelengths that are centered at 800 nm requires an ultrabroadband modulator array. Since these modulators operate at wavelengths around 800 nm, the material choices are limited to relatively high-Al content AlGaAs and $In_{0.5}(Ga_xAl_{1-x})_{0.5}P$ layers lattice-matched to GaAs. In addition, since GaAs absorbs light with a wavelength less than 870 nm, the lower cladding layer of the modulator must be relatively thick to isolate the modulator from the GaAs substrate. To create the largest optical mode possible and to minimize the coupling loss, the index contrast between the waveguiding layers and the cladding layers should be minimized. Hence, a dilute waveguide structure in which thin layers of high index material are embedded in a low-index material, is employed. The resulting layered structure has an effective index slightly higher than the low-index material and is determined by the layer thicknesses as well as the refractive index of the two materials that compose the dilute waveguide. Two slightly different structures were grown by molecular beam epitaxy: (i) an InAlP-based structure in which the dilute waveguide consisted of alternating layers of InAlP and $Al_{0.5}Ga_{0.5}As$ and (ii) an $Al_{0.8}Ga_{0.2}As$-based structure in which the dilute waveguide consisted of alternating layers of $Al_{0.8}Ga_{0.2}As$ and InGaP. Both structures are challenging in terms of the epitaxial growth. In the phosphide-based structure, the growth of thick, lattice-matched InAlP cladding layers is challenging due to the need to maintain the lattice-matched condition and due to possible anion ordering. In the arsenide-based structure, although the use of $Al_{0.8}Ga_{0.2}As$ for the cladding layer minimizes the lattice-mismatch problem, achieving high-quality, high-Al content AlGaAs cladding layers is difficult due to the low Al adatom mobility on the surface during growth. To minimize free carrier loss, the modulator uses a p-i-n structure in which the Si and Be dopants are graded from the contact layers to the dilute waveguide region. Photoluminescence (PL) measurements from the arsenide-based structure show a weak PL peak at ~650 nm from the InGaP layers in the dilute waveguide. The $Al_{0.8}Ga_{0.2}As$ and $Al_{0.5}Ga_{0.5}As$ layers as well as the InAlP layers have indirect band gaps and hence do not exhibit photoluminescence. Due to the high etch selectivity between the arsenide and phosphide layers, the uppermost high index layer of the dilute waveguide also acts as an etch stop.

Both structures are anticipated to have similar optical mode profiles; the structures are designed to be single mode in a 2-μm wide ridge waveguide. Using OptiBPM, the fundamental mode for the phosphide-based structure is calculated to be roughly 2 μm x 1 μm (WxH); a similar mode profile exists for the arsenide-based structure. In both structures, if the dilute waveguide is not completely etched, due to the low index contrast of the dilute waveguides, the bending radius is quite large, on the order of a millimeter.

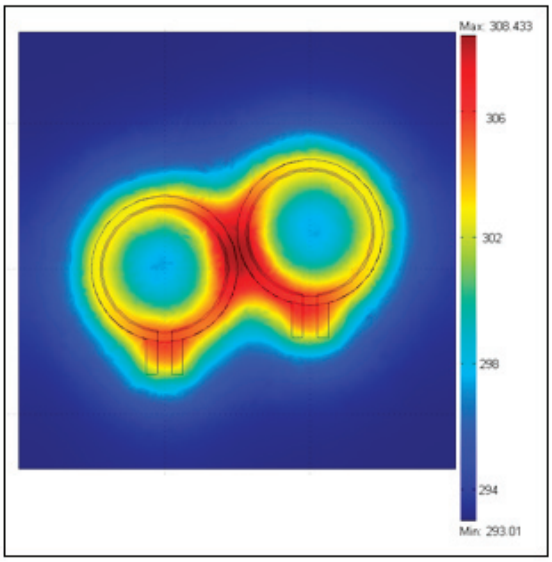
A mask set suitable for both structures has been designed and fabricated. The mask set contains Mach Zehnder interferometer modulators of various lengths with multimode interference couplers or Y-splitters. The Mach Zehnder interferometer modulators as well as conventional modulators are oriented both parallel and perpendicular to the major flat of the 2" GaAs(100) wafers. The mask set also contains a variety of passive components such as Y-splitters and multimode interference couplers as well as straight and curved waveguides. The fabrication of the phosphide-based and arsenide-based modulators will commence shortly.

Design and Measurement of Thermo-optics on Silicon

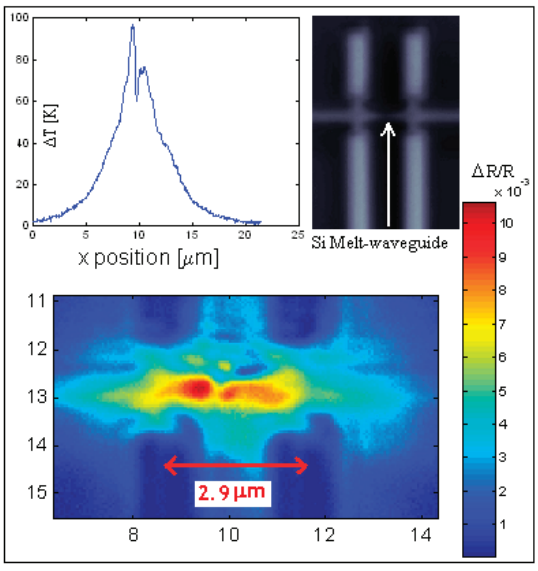
R. Amatya, R.J. Ram
Sponsorship: DARPA

The vision of optoelectronics started with the integration of optics and electronics on the same substrate. Various optical and electrical components on the same chip would have better performance and functionalities than the components taken alone. Electrical integrated circuits (IC) have been very successful on silicon substrate. Thus, silicon is one of the more desirable materials for optoelectronic devices. Silicon (Si) as well as silicon nitride (SiN) optical waveguides are becoming integral components for optical systems because of their advantages of high index contrast and compatibility with IC. Thermally tunable optical ring resonators made of SiN on silicon can be used as switches and filters. A small ring diameter (≈20 μm) allows a large free-spectral range. The temperature dependence of the refractive index (i.e., the thermo-optic effect of the core and cladding) is utilized to tune these ring resonators. Resistive heaters are designed to sit on top of the cladding for thermal tuning. One of the key aspects while designing the heaters is minimum power dissipation per GHz in terms of tuning flexibility. Figure 1 shows a thermal simulation for a heater over a two-ring filter.

Waveguides formed on silicon-on-insulator substrates can have sub-microsecond switching capabilities. These waveguides are heated by passing current through them; it is important to be able to study and measure the thermal characteristics of the device. Thermoreflectance spectroscopy is one of the many ways of measuring the temperature of the device. A temperature profile for a silicon-melt waveguide of 0.5 μm thickness is shown by measuring the reflectance changes due to modulating the current. Figure 2 shows the image of the melt waveguide along with temperature profile and the thermoreflectance image. The figure on the left inset shows the non-uniform temperature distribution within the waveguide. For the silicon melt waveguide, the measured thermo-optic coefficient (κ) was 1.1E-4/K, which is similar to the reported values for silicon for the specific wavelength (510 nm). Similar measurements can be done on SiN ring resonators to obtain the thermo-optic coefficient.



▲ Figure 1: Temperature profile for the thermal tuning of ring resonators.

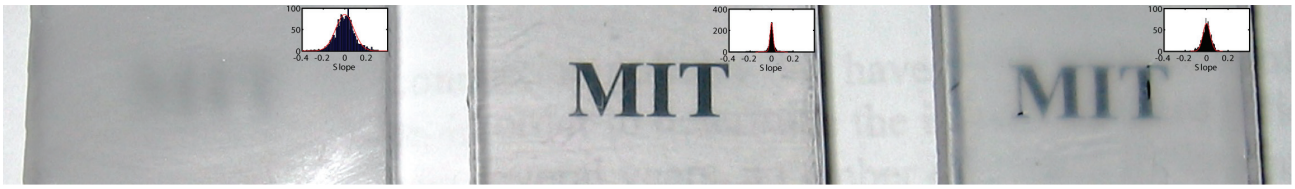


▲ Figure 2: Silicon melt waveguide-thermal profile using the thermo-reflectance technique.

Polymer Waveguides for Integrated Biosensors

K. Lee, R.J. Ram
Sponsorship: DuPont-MIT Alliance, NSF Center for Material Science and Engineering

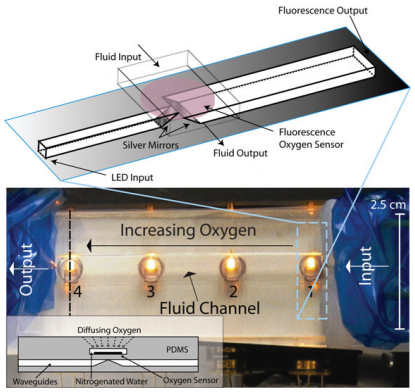
To overcome the challenge of fabricating large-dimension waveguides with optical-quality surfaces, a conventional fabrication approach using plastics is utilized over a micro-fabrication approach generally used for micro-fluidics. While conventional milling can easily create structures with dimensions of 1 mm, roughness from the fabrication process leads to diffuse surfaces and variations greater than 1 μm. To overcome the roughness due to milling and ultimately create large features with optical quality roughness, a solvent vapor polishing process is used in which a solvent vapor such as methylene chloride vapor is used to liquify the plastic surface [1]. Varying the solvent pressure and the exposure time can control the degree of polishing. Under optimal polishing conditions, the average roughness from sanded polycarbonate samples can be reduced from 1000 nm to 70 nm as shown in Figure 1. When combined with vapor polishing, CNC milling becomes a viable process for both optical and micro-fluidic fabrication of master molds.



▲ Figure 1: Polished polycarbonate samples under different polishing conditions and histograms of the slope distribution seen at the surface. (Left) 10% saturation pressure results in no polishing (Ra = 1000 nm). (Middle) 75% saturation pressure results in excellent polishing (Ra = 70 nm). (Right) 95% saturation pressure results in over-polishing (120 nm) and is seen as a developing haze.

After mold fabrication, standard soft lithography processes are used to create negative PDMS replicas of the polycarbonate molds. In addition, PDMS molds are subject to e-beam deposition of evaporated silver to provide reflective surfaces where necessary. The same fabrication process is used for both waveguides and microfluidic components of the chip and the final oxygen sensing device is shown in Figure 2. The oxygen sensors used for this experiment are created by a mixture of Platinum(II) octaethylporphine ketone (PtOEPK) [2] and polystyrene deposited on glass disks. This fluorescent dye has a maximum absorption at 592 nm and emits at 759 nm.

Fabricated waveguides exhibit a propagation loss of 0.136 dB/cm at 626 nm and a measured 50% intensity numerical aperture of 0.5. E-beam deposited silver on PDMS measured a reflectivity of 72% with a HeNe laser at 632 nm. Oxygen measurements were preformed by fiber coupling amplitude modulated LEDs into the input guides, collecting the output through a colored glass filter and photodetectors, and measuring the phase shift between the input and output signals. The sensor system achieves an SNR greater than 40 and provides a phase shift of 30 degrees with 1 degree variance from nitrogen to air.



▲ Figure 2: A schematic of the integrated fluidic and photonic device showing the device and a cross sectional view. Fluorescence based oxygen sensors at the base of the fluidic channel lie on a plane sitting above the collection and excitation optics. A picture of the fabricated optical and fluidic integrated device is shown.

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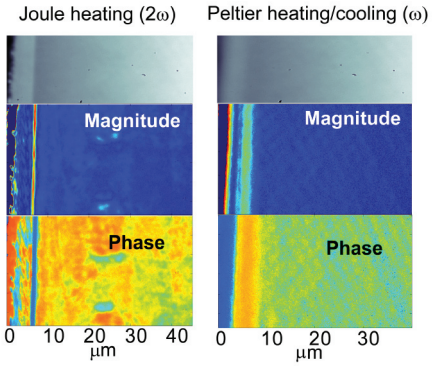
[2] D.B. Papkovsky, "Phosphorescent complexes of porphyrin ketones: Optical properties and application to oxygen sensing," *Anal. Chem.*, vol. 67, pp. 4112-4117, 1995.

Nanoscale Thermal Imaging Microscopy of Thermoelectric Devices

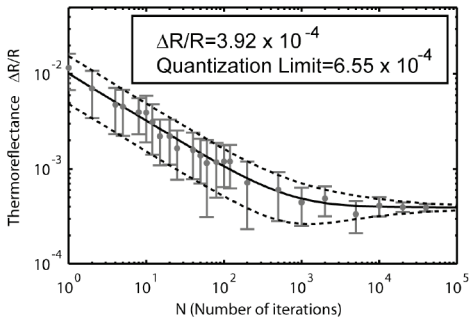
P. Mayer, R.J. Ram
Sponsorship: ONR MURI

In many solids, a change in temperature produces a small change in the dielectric response of the material, and particularly in the index of refraction. By measuring the change in reflectance from a device or material whose temperature is modulated in some way, an image of the temperature change can be obtained, after proper calibration. This approach is useful for examining heat transport in electronic/optoelectronic devices since the heating due to a changing bias current or voltage can be measured. Unlike the case with typical (infrared) thermal imaging, deep sub-micron spatial resolution is possible. Shown below in Figure 1 are (uncalibrated) thermoreflectance images of the Joule and Peltier heating and cooling in a 4.9 μm-thick InGaAs-based superlattice incorporating semimetallic self-assembled ErAs nanodots, on an InP substrate. The ErAs dots and the superlattice both scatter phonons participating in cross-plane heat transport, reducing the thermal conductivity to below the alloy limit by nearly a factor of two. The dots and the superlattice are also expected to increase the free electron concentration, the electrical conductivity, and the Seebeck coefficient.

The thermal imaging technique used here relies on a CCD camera triggered 4 times per temperature cycle and averaged over many cycles, so that each pixel of the camera functions as a lock-in detector. Because the change in reflectance is small (e.g. 1 part in 10000, per degree Kelvin) it has been suggested that the temperature resolution of the technique is limited by the least significant bit size of the quantizer of the CCD array, giving rise to a minimum temperature resolution in the singe Kelvin range. However, due to the presence of noise in the pre-quantized signal, sufficient averaging can actually improve the resolution. We have demonstrated a temperature resolution on the order of 10 mK and developed a quantitative theory describing the statistics and accuracy of the measurement, set by the noise characteristics of the camera and the measurement characteristics. Figure 2 shows the measurement of a temperature signal smaller than that corresponding to the bit size of the CCD array, as a function of the measurement duration. The theoretically predicted mean and standard deviation are close to those measured.



▲ Figure 1: Cross-plane magnitude and phase images of the Joule and Peltier contributions to the thermal response in a nanostructured thermoelectric element. Superlattice (clearly visible in the top photomicrographs) is to the left of the image.



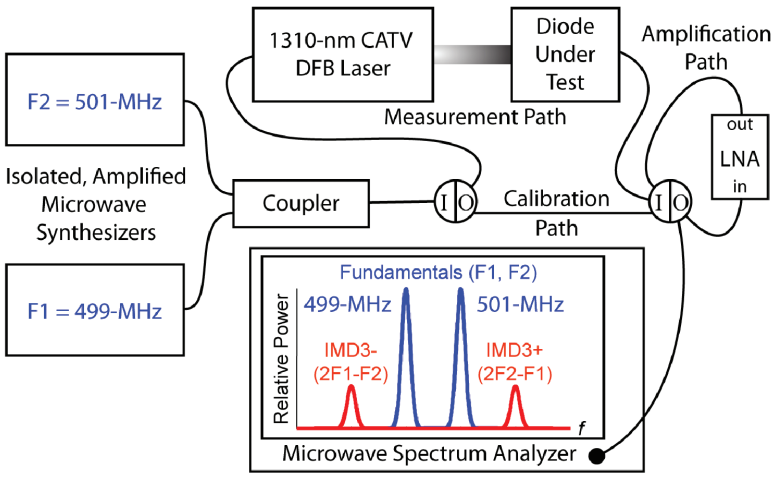
▲ Figure 2: Measurements (gray) and theoretical predictions (black) for sub-quantization thermoreflectance measurements. The measurement converges for sufficient iterations (long-enough duration).

Dynamic Range of Strained Ge-on-Silicon Photodiodes

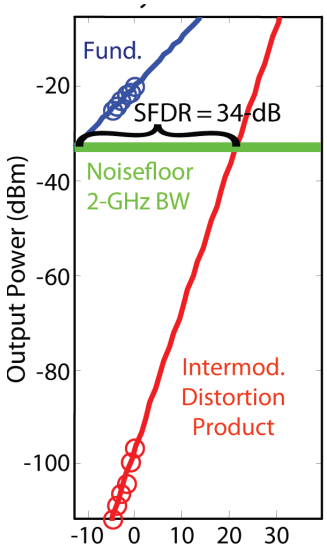
J. Orcutt, R.J. Ram, O.L. Olubuyide, J.L. Hoyt
Sponsorship: DARPA

As photonic integrated circuits gain maturity in the silicon material system, new applications that require photonic components integrated with silicon electronic circuitry become possible. One such new application is the hybrid photonic-electronic analog-to-digital converter in which the sampling front-end is achieved optically and the digital conversion back-end is achieved electronically [1]. To allow this converter to achieve a high effective number of bits (ENOBs), an important figure-of-merit for these systems, photodetector with a high dynamic range that are compatible with an integrated CMOS platform are necessary. One such photodetector under development is a germanium-on-silicon photodiode that is CMOS-compatible. To characterize the linearity, we measured the spur-free dynamic range (SFDR) of the diodes using the test setup shown in Figure 1.

To calculate the SFDR, we measured the spectrum of the photodiode response to a two-tone RF-modulated input as a function of modulation amplitude. As shown in the microwave spectrum analyzer screen inset to Figure 1, third-order nonlinearities produce in-band intermodulation distortion products (IMD3) that limit the dynamic range of the detector. To ensure that observed nonlinearities are caused by the diodes, we examined the output of the link laser by using a ligh-twave front-end to the microwave spectrum analyzer and by replacing the Ge photodiodes with industry-standard Epitaxx InGaAs p-i-n photodiodes designed for CATV applications. To complete the data required to calculate SFDR, we measured the noise floor of the link, roughly integrating it over a 2-GHz bandwidth with the microwave spectrum analyzer. This data and the calculated SFDR are shown in Figure 2. The demonstrated 34-dB SFDR of this link would currently allow for 5.6 effective bits if it were the limiting factor in the converter's performance.



▲ Figure 1: Diagram showing the SFDR measurement setup. The I/0 blocks are microwave switches that enable switching between the measurement path and the calibration path, as well as the insertion of the optional amplification path. The block labeled "LNA" in the amplification path is a Miteq low-noise amplifier.



▲ Figure 2: Spur-free dynamic range measurement on a 100 x 100 µm Ge photodiode. The diode was biased at -3 V in this measurement.

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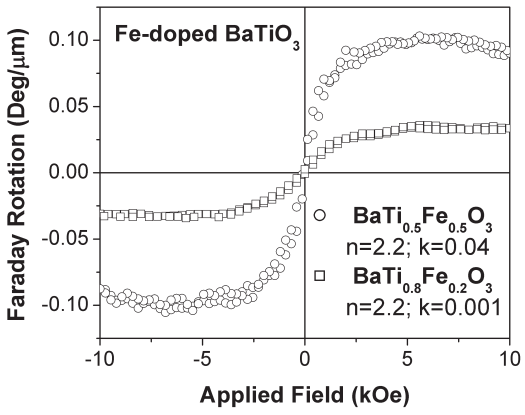
Magnetic Oxide Films for Optical Isolators and Magneto-Electronic Devices

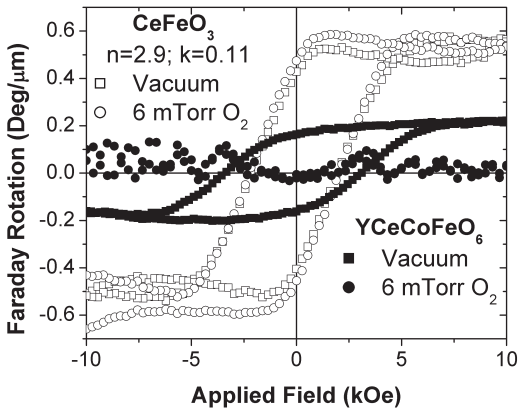
C.A. Ross, G.J. Dionne, M. Bolduc, A. Taussig, V. Sivakumar
Sponsorship: Lincoln Laboratory, ISN, MicroPhotonics Consortium

We have established a thin-film laboratory that includes a pulsed-laser deposition (PLD) system and an ultra-high vacuum sputter/analysis system. In PLD, a high-energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. The PLD is particularly useful for making complex materials such as oxides because it preserves the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magneto-optical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magneto-optical isolators in photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite) grows very well on MgO or Si, with high Faraday rotation but its optical absorption is high. Recently we have examined magnetic perovskite thin films such as Fe-doped barium titanate (Figure 1) [1] and Ce-doped orthoferrites (Figure 2). These materials show strong magneto-optical properties with weak optical absorption and the films grow with good quality onto MgO substrates. These films could be useful for waveguide isolators and other magneto-electronic devices in which optical absorption losses are critical. A second project involves the use of electrochemical methods to control the magnetization of iron oxide spinel structure films (magnetite or maghemite) grown on conducting substrates, making a chemically-switchable material. The insertion of Li ions by electrochemical discharge changes the oxidation state of the Fe(III) to Fe(II) and can reduce the magnetization of the film by about 30%, in a reversible process. Recent experiments on nanoparticles of iron oxide show much greater changes in magnetization, up to ~80%, indicating that the process is kinetically limited.



▲ Figure 1: Faraday rotation vs. applied field for 750-nm-thick $BaTi_{0.5}Fe_{0.5}O_3$ and $BaTi_{0.8}Fe_{0.2}O_3$ films grown in a vacuum on MgO substrates, with the field perpendicular to the film.



▲ Figure 2: Faraday rotation vs. applied field for 500-nm-thick $CeFeO_3$ and $YCeCoFeO_6$ films grown in a vacuum or under 6-mTorr O_2 pressure on MgO substrates, with the field perpendicular to the film.

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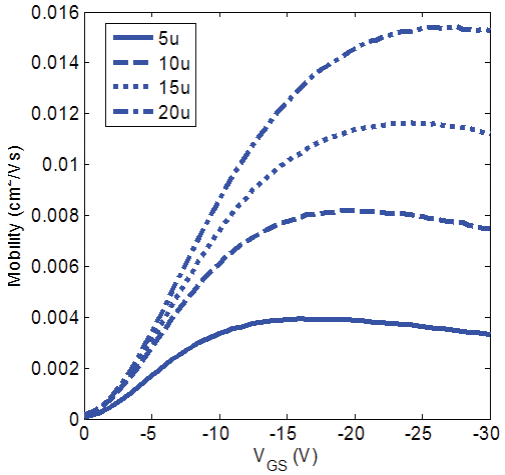
Characterization of Organic Field-effect Transistors for OLED Displays

K. Ryu, I. Kymissis, V. Bulovic, A.I. Akinwande, C.G. Sodini
Sponsorship: MARCO C2S2

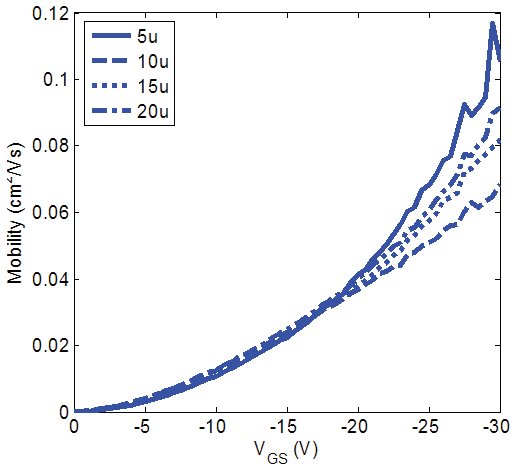
Organic field-effect transistors (OFETs) provide exciting new applications because they can be made using low-temperature processing techniques such as thermal evaporation and solution-based patterning. The low-temperature processing enables the transistors to be fabricated on durable plastic substrates, which can be both flexible and very large. The solution-based patterning enables "printing" circuits like newspapers using a roll-to-roll method and can drive down cost. In addition, the fabrication process of OFETs is compatible with that of a variety of organic optoelectronics and sensors. Various sensor arrays such as pressure sensors, light sensors, and chemical sensors have been made successfully using OFETs [1-3]. One crucial area that needs to be researched in this field is how the different charge transport mechanisms and material sets in organic transistors change the design considerations in circuit applications compared to the traditional silicon MOSFETs. In this research, an optical-feedback organic LED (OLED) display is designed and fabricated in order to investigate this problem.

The contact resistance, threshold voltage, and mobility are extracted from top-contact and bottom-contact transistors with current-voltage (I-V), and capacitance-voltage (C-V) measurements. Extraction of contact resistance is found to be crucial in characterization of bottom-contact transistors as it obscures mobility extraction. Figures 1 and 2 show mobility extracted from various length transistors without and with taking contact resistance into consideration, respectively. In addition, mobility is found to increase as gate voltage increases contrary to the mobility dependence in crystal silicon MOSFETs where mobility decreases as gate voltage increases. Currently, slow transients, a manifestation of the trap-limited hopping transport in organic semiconductors, are being characterized.

Future work will focus on modeling transistors and simulating two main OFET components in the display, which are the switch and the transconductance amplifier.



▲ Figure 1: Mobility extracted without taking contact resistance into consideration. The mobility decreases as the channel length shortens because effect of the contact resistance becomes more prevalent as the channel length shortens.



▲ Figure 2: Mobility extracted with contact resistance taken into consideration. The mobility is consistent from shorter to longer channel length.

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EDUCATIONAL ACTIVITIES

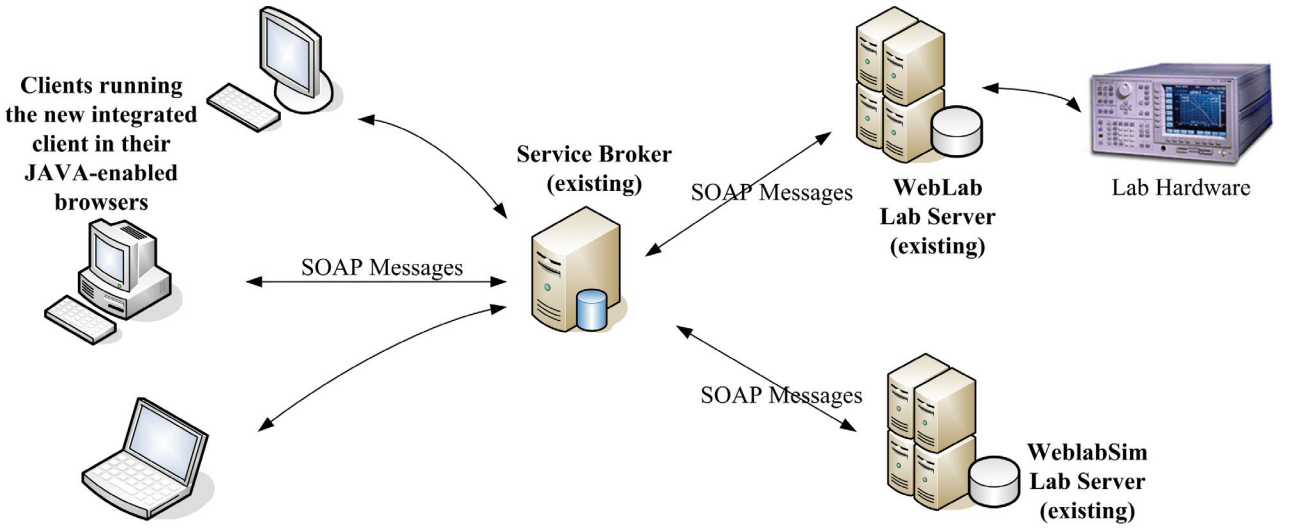
Integration of Online Microelectronic Device Characterization and Simulation

B. Cukalovic, J.A. del Alamo
Sponsorship: iCampus (MIT-Microsoft Alliance)

In this project we created a new online laboratory that combines and significantly upgrades the capabilities of our two existing online microelectronics labs: WebLab, a device characterization lab [1], and WebLabSim, a device simulation lab [2]. The new integrated tool allows users to run, simultaneously, experiments on real devices and simulations on the virtual ones, as well as to compare the results of the two. Our hope is that this tool will enrich microelectronics teaching and learning by allowing students to compare the real-life behavior of devices with theoretical expectations.

Both WebLab and WebLabSim were built based on the iLab Shared Architecture. This means that they are both three-tier systems, consisting of a client Java applet that lets users set up the experiments/simulations, a laboratory server that runs them, and a generic service broker that mediates between the two, through SOAP-based web services. The modular infrastructure and common interfaces allowed us to integrate the two labs simply by developing a new lab front-end (Figure 1). The development was a very smooth task owing to the facts that the clients of WebLab and WebLabSim share much of their codebase and that this existing software core has been gradually perfected in the eight years of operational history of WebLab.

In addition to integrating the labs, we significantly extended the capabilities of the original clients. Two of the most interesting features we added are: 1) the ability to graph the results of multiple experiments/simulations simultaneously, on top of each other, which allows for much easier comparison and 2) the ability to load and display results of experiments/simulations that ran at any point in the past. These improvements will be made part of the main client codebase and, thus, be featured in all new releases of our online microelectronics laboratories.



▲ Figure 1: Schematic diagram of the new integrated lab as implemented on top of the existing modules and architecture.

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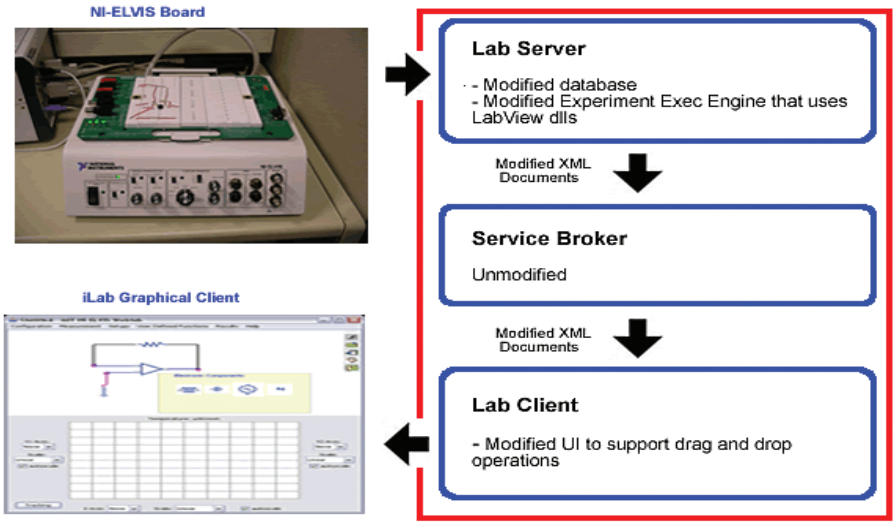
The ELVIS iLab: a Flexible Platform for Online Laboratory Experiments in Electrical Engineering

S. Gikandi, J.A. del Alamo
Sponsorship: Carnegie Corporation of New York, Microsoft

This project is part of the collaboration between MIT and universities in sub-Sahara Africa to exploit the value of iLabs in the developing world [1]. The main goal of this project is to develop software that will integrate the National Instruments Educational Laboratory Virtual Instrumentation Suite (ELVIS) into the iLabs shared architecture. The project takes into consideration the special circumstances surrounding the deployment of iLabs in Africa such as bandwidth limitations, limited access to networked computers, and lack of computer skills on the part of students. Integrating ELVIS into iLabs will facilitate the rapid deployment of new online labs to augment the physics and electrical engineering curricula in these universities.

The iLab development efforts for this project are being made in parallel with developers at the Obafemi Awolowo University (OAU) in Nigeria. One of the main goals of the new system is to fill the gap of laboratory experiences in introductory level electronics and physics classes, which are hardest hit by the lack of equipment due to their typically large enrollment. Our goal is to support the development of electronic circuit building skills by providing an environment where students can easily try different circuit configurations before submitting experiments for execution. We are therefore investigating new iLab client-user interface designs that will enable students to create and edit circuit schematics from provided electronic components.

Our ELVIS iLab design will also formalize and simplify the process of creating and administering such labs for instructors, thereby speeding up the deployment of new labs in an environment where software development skills are not at a premium. This will be achieved by recycling many of the components that currently lie behind the success of the microelectronics weblab [2]; these components have been adapted before for new iLabs [3]. Besides reusing existing software, the project aims to make a major contribution towards enhancing students' experiences with iLabs through its new interactive client design.



▲ Figure 1: This diagram shows how many of the microelectronics weblab components can be adapted to create software for developing new iLabs that communicate with the ELVIS board.

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Increasing Reliability, Reusability, and Measurement Flexibility in the MIT Microelectronics WebLab

J. Hardison, A. Haldar, J.A. del Alamo
Sponsorship: Microsoft

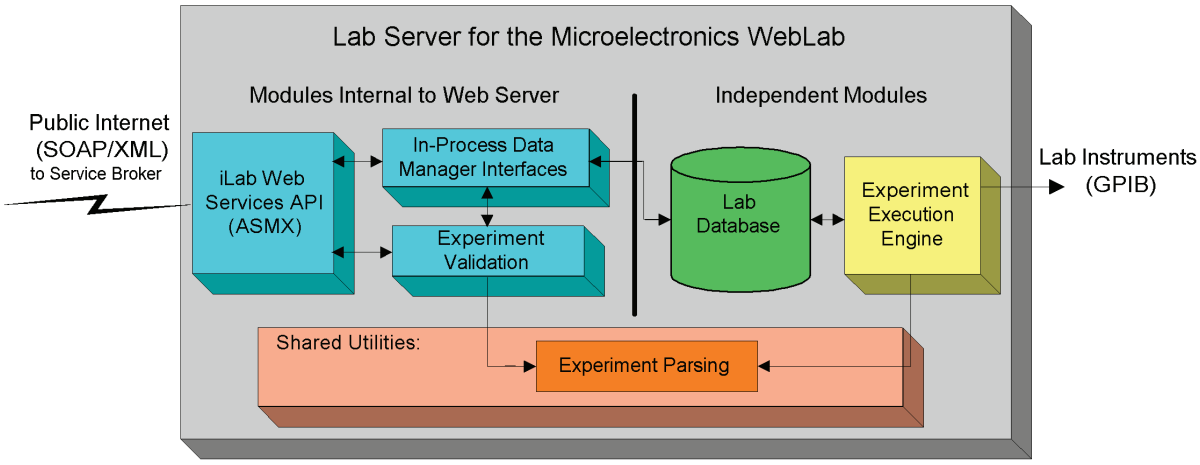
A number of updates have recently been made to the MIT Microelectronics WebLab, an online semiconductor device characterization laboratory. The most recent major release came in the Spring of 2004 with WebLab 6.0; the first lab built on the iLab Shared Architecture and an exemplar for lab development using that architecture [1]. These latest revisions focus on increasing the functionality and reliability of the lab as well as its efficacy as a reference implementation for other developers.

The functionality of WebLab has been expanded with the integration of an Agilent 41501B SMU & Pulse Generator Expander. This addition increases the measurement capacity from 100 volts and 100 milliamps to 200 volts and 1 amp, allowing the characterization of high power devices. The result is a lab with broader utility that can be used in a greater range of courses.

Revisions have also been made to the WebLab Lab Server software (Figure 1). A stand-alone utility now performs the parsing of XML-encoded experiment specification documents. Previously, this functionality was duplicated in a number of other components. The Experiment Validation module has been re-written in an effort to streamline its operation and make it easier to modify validation criteria. Finally, the WebLab Experiment Execution Engine, which governs the execution of experiments on the lab instrumentation, has been similarly streamlined and deployed as a Windows service. All of these revisions contribute to the reliability of the lab by reducing the complexity of the code base, increasing modularity, enabling easier modification, and improving the integration of the lab server software with the host server.

Additionally, these revisions benefit lab developers using WebLab as a reference. Clearly written modular components can be more easily co-opted into other labs or used as models for original components. Further, thorough documentation details the specific functionality and reusability of these revised components.

WebLab continues to be used for credited lab assignments in undergraduate and graduate level courses both at MIT and at other institutions. It is also made publicly available through MIT's OpenCourseWare initiative [2]. The WebLab source continues to be released a model for other lab developers and has been used as the basis for other online labs. The MIT Microelectronics WebLab can be accessed for in-course use at http://ilab.mit.edu or at http://openilabs.mit.edu for unrestricted guest use.



▲ Figure 1: Schematic of the Microelectronics WebLab Lab Server detailing the relationships between the revised components.

REFERENCES:

[1] J. Hardison, D. Zych, J.A. del Alamo, V.J. Harward, S.R. Lerman, et al., "The Microelectronics WebLab 6.0 – An implementation using web services and the iLab shared architecture," presented at ICEER, Tainan, Taiwan, 2005.

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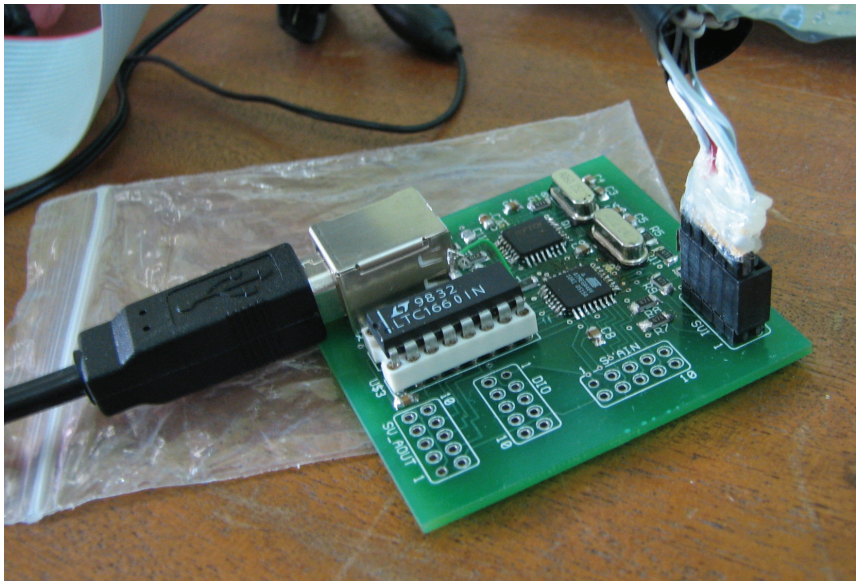
A Low-cost Platform for Online Experiments

P. Mitros, J.A. del Alamo
Sponsorship: Carnegie Corporation of New York

The goal of the iLab project is to connect laboratory instruments to the web, allowing students to perform experiments from anywhere at anytime. We are developing a low-cost platform for the development of online electronics experiments for use under the iLab architecture. With this board, instructors in the developed world will be able to quickly, cheaply, and easily deploy online laboratories relevant to specific problem sets. In addition, it will dramatically facilitate the creation of iLabs in the developing world, where students would otherwise have extremely limited practical experience, due to equipment costs.

The initial version of the platform consists of a USB-powered board with eight analog inputs, eight analog outputs, and a number of digital general purpose IO ports. This board can be used to deploy basic electronic experiments for under $30. It can be used for static and low-speed experiments, such as characterizing the input/output relationship of a logic gate or plotting the response of an integrator to a variety of waveforms. In addition, in conjunction with a daughterboard being developed, the system can function as a basic, low-precision parameter analyzer for around $40. This daughterboard can convert each set of 2 analog input ports, 1 analog output ports, and 1 digital port into one SMU port capable of outputting either a controlled voltage or a controlled current and capable of measuring both the current and the voltage (for a total of 4 SMU).

We currently have a working prototype PCB of the main board, shown in Figure 1. We have developed and tested the parameter analyzer daughterboard on a protoboard. We have manufactured, but not yet tested, a prototype PCB version of the parameter analyzer daughterboard, as well as of a candidate final version of the main board. In addition, we are working on integrating the system into the iLab Shared Architecture. We are doing a preliminary investigation of the possibility of developing similar low-cost equipment for other types of experiments, e.g., higher-speed circuits.



▲ Figure 1: The prototype iLab Mini PCB board.

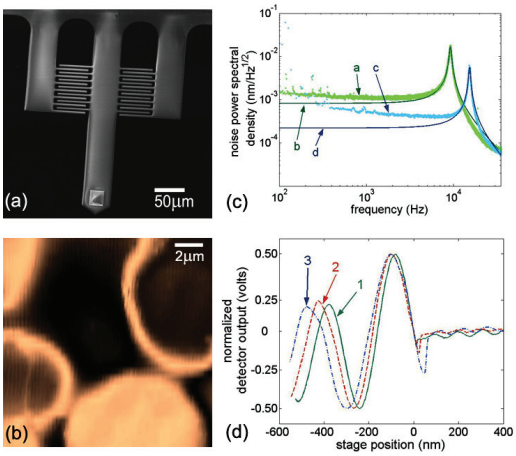
Low-cost Atomic Force Microscopy for the Bioinstrumentation Teaching Laboratory

M. Shusteff, T.P. Burg, S.R. Manalis
Sponsorship: Cambridge-MIT Institute educational grant

We present a low-cost atomic force microscopy (AFM) apparatus that we have designed and built for use in an undergraduate teaching laboratory. The tool gives students hands-on access to nano-Newton force measurements, and sub-angstrom position measurements. The apparatus relies mainly on off-the-shelf components and utilizes an interferometric position sensor known as the interdigitated (ID) cantilever to obtain high resolution. The mechanical properties of the ID readout enable a robust and open design that makes it possible for students to learn about and directly control any part of it. Its instructional advantage is that students interact with a complete measurement system, and learn measurement principles in context.

This AFM enables several experiments in biomechanics and thermodynamics. Students have used it for imaging, measuring the elastic modulus of a surface, and measuring Boltzmann's constant k_B by recording the thermo-mechanical noise of the probe cantilever and applying the equipartition theorem. Further experiments for measuring molecular forces and elastic moduli of live cells are in development. In addition to gaining an appreciation of the lower limits of position and force measurement, students learn to apply numerous classroom concepts such as digital sampling, Fourier-domain analysis, noise sources, and error propagation.

The complete design details are available online at http://web.mit.edu/be/teachAFM/ .



▲ Figure 1: (a) A scanning electron micrograph (SEM) image of the cantilever probe used for imaging. The short side-levers are used as fixed reference beams and do not contact the sample. (b) A 15 µm square image of human red blood cells taken with our AFM, imaged in air after the cells were dried on a glass substrate (32 lines of data × 250 points per line, up-sampled to 400 × 400 pixels). (c) Power spectral density data of cantilever vibrations driven by ambient thermal energy (curves "a" and "c") and corresponding fits (curves "b" and "d") for 350 µm and 275 µm long cantilevers, respectively. Fitting a second-order model harmonic oscillator function to the data yields key system parameters like quality factor Q and resonant frequency f0, which allow the calculation of kB by equipartition. (d) Normalized data collected for an experiment to measure elastic modulus. The period of the oscillating section of the force curves is larger for softer samples. Force curve 1 was taken on a hard sample (silicon nitride), whereas curves 2 and 3 were taken on PDMS of variable hardness (Dow Corning Sylgard 184 mixed in ratios of 10:1 and 25:1, respectively).

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Microfabrication Project Laboratory (6.151)

Technical Instructor, L. Wang

This laboratory course is offered in the spring semester for students that have already completed 6.152J. The course is designed to teach experimental microfabrication process design. The students of this subject are given a broad process goal, namely to build a device, and they are challenged to design and develop a process sequence. Typically, the entire class (4-6 students) works on one device, and they partition the integrated process into a set of unit process sequences. Work proceeds first, on the development of the unit processes, and then, on the integrated process. In recent years, the students have succeeded in microfabricating micromachined contactors for integrated circuit testing, flexible electrode arrays for retinal implants, and microcantilevers for AFM applications.

Micro/Nano Processing Technology (3.155J/6.152J)

Technical Instructor, L. Wang

This combination laboratory and lecture course is offered and taught jointly by the Department of Electrical Engineering and Computer Science and the Materials Science and Engineering Department. The course includes weekly lectures on all aspects of micro/nano processing technology with design problems to teach process design. Additionally, the course includes weekly laboratory sessions conducted in the MTL. During these sessions, each student fabricates a wafer of poly-silicon gate MOS devices, silicon nitride nano-mechanical devices, and a plastic microfluidic mixer. All the devices and structures are tested and laboratory reports correlating the test results with theoretical expectations culminates the education experience. The course is offered every semester, and a laboratory-only version of the course is offered 3-4 times/year.

MTL RESEARCH CENTERS

Center for Integrated Circuits and Systems

Prof. Hae-Seung Lee, Director

The Center for Integrated Circuits and Systems (CICS) at MIT, established in early 1998, is an industrial consortium created to promote new research initiatives in circuits and systems design, as well as to promote a tighter technical relationship between MIT's research and relevant industry. Seven faculty members participate in the CICS: Hae-Seung Lee (director), Anantha Chandrakasan, Joel Dawson, Michael Perrott, David Perreault, Charles Sodini, and Vladimir Stojanovic. CICS investigates a wide range of circuits and systems, including wireless and wireline communication, high-speed and RF circuits, microsensor/actuator systems, imagers, digital and analog signal processing circuits, DC-DC converters, among others.

We strongly believe in the synergistic relation between industry and academia, especially in practical research areas of integrated circuits and systems. We are convinced that CICS is the conduit for such synergy. At present, participating companies include Analog Devices, IBM, Linear Technology, Marvell Technology Group, Maxim Integrated Products, National Semiconductor, Philips, Silicon Laboratories, and Texas Instruments.

CICS's research portfolio includes all research projects that the seven participating faculty members conduct, regardless of source(s) of funding, with a few exceptions. (A very small number of projects have restrictions on information dissemination placed on them due to the nature of funding.)

Technical interaction between industry and MIT researchers occurs both on a broad and individual level. Since its inception, CICS recognized the importance of holding technical meetings to facilitate communication between MIT faculty and students and industry. We hold two informal technical meetings per year open to participating companies. Throughout each full day meeting, faculty and students present their research, often presenting early concepts, designs, and results that have not been published yet, giving early access to meeting attendees. Participating companies then offer valuable technical feedback, as well as suggestions for future research. We have held bi-annual meetings each year, and the response from industry has been overwhelmingly positive.

More intimate interaction between MIT researchers and industry takes place while working on projects of particular interest to participating companies. Companies may invite students to give on-site presentations, or they may offer students summer employment. Additionally, companies may send visiting scholars to MIT. The result is truly synergistic, and we strongly believe that it will have a lasting impact in the field of integrated circuits and systems.

MTL RESEARCH CENTERS

Intelligent Transporation Research Center

Dr. Ichiro Masaki, Director

Transportation is an important infrastructure for our society. It is time to propose a new transportation scheme for resolving the increasing transportation problems. In responding to social needs, MIT's Microsystems Technology Laboratories established the Intelligent Transportation Research Center (ITRC) in September 1998 as a contact point of industry, government, and academia for ITS research and development.

ITRC focuses on the key Intelligent Transportation Systems (ITS) technologies, including an integrated network of transportation information, automatic crash & incident detection, notification and response, advanced crash avoidance technology, advanced transportation monitoring and management, etc., in order to improve the safety, security, efficiency, mobile access, and environment. There are two emphasis for research conduced in the center:

- The integration of component technology research and system design research.
- The integration of technical possibilities and social needs.

ITRC proposes the incremental conversion and development process from current to near and far future systems and develops enabling key components in collaboration with the government, industries, and other institutions. Other necessary steps are the integration of technical, social, economical, and political aspects. The integration of the Intelligent Transportation Systems in different countries is also essential. The integration of vehicles, roads, and other modes of transportation, such as railways and public buses, are all imperative.

These integrations are fulfilled with the cooperation of researchers in various fields, including the Microsystems Technology Laboratory (MTL), the Research Laboratory of Electronics (RLE), the Artificial Intelligence Laboratory (AI), the Center for Transportation Studies (CTS), the Age Laboratory, the Department of Electrical Engineering and Computer Science, the Department of Civil and Environmental Engineering, the Department of Aeronautics and Astronautics, and the Sloan School of Management. The research center has 8 MIT faculty and several visiting professors and scientists. The director of the center is Dr. Ichiro Masaki.

MTL RESEARCH CENTERS

MEMS@MIT

Prof. Martin A. Schmidt, Director

The MEMS@MIT Center is a newly formed center intended to serve as a means to unite the wide-ranging campus activities in Micro/nano systems and MEMS with forward-looking industrial organizations. Currently, MEMS@MIT is comprised of more than 125 faculty, students, and staff working on a broad research agenda and supported by more than $10 million/year. The MEMS research efforts on campus focus on three overarching themes:

i) Biological, Chemical and Medical MEMS – includes work on manipulation and processing of biologically-relevant materials of varying size scales from tissue engineering scaffolds and cell manipulation, to devices for separation and sorting of DNA and proteins, sensing platforms for detection of biomolecules, a wide range of microfluidic devices, and microchemical systems for synthesis and characterization

ii) Power MEMS – includes work on energy scavenging by vibration harvesting, various approaches to fuel burning power generation, eg. thermo- photovoltaics, fuel cells, microturbines

iii) Enabling Technologies – includes work on MEMS processes and process modeling (eg. materials characterization, CAD tools and novel metrology methods), and micro and nano-mechanical devices, ie. switches, actuators, and self-assembled devices.

Membership benefits include:

- Insight to newest ideas in MEMS
- Early access to research results
- Early awareness of IP generated for licensing
- Access to high quality continuing education materials
- Partnering for federal or other funding opportunities
- Recruitment of leading MIT graduates

MTL RESEARCH CENTERS

MIT Center for Integrated Photonic Systems

Prof. Rajeev J. Ram, Director

The goals of the Center for Integrated Photonic Systems are:

1. To provide leadership and direction for research and development in photonics.
The core activity of CIPS is the development of a long-range vision for research and the development of integrated photonic devices & systems. CIPS will host forums and facilitate working groups with industrial consortium members to identify and discuss technology and road mapping issues:

- technology directions
- potential disruptive technologies
- technical barriers (gaps)
- actions needed to enable future-generation systems, and
- manufacturing and market issues that drive timing of technology deployment.

As an academic institution we can work openly with a variety of different organizations in developing and gathering input for our models. Whether it is performance data for new devices 'in the lab,' yield data for existing manufacturing processes, planning documents, or first-hand observations of the corporate decision making process, CIPS researchers benefit greatly from the unique relationship between MIT and industry. The level of detail and intellectual rigor of the models being developed here is complemented by the high quality of data available to us. CIPS researchers are developing models of optical and electronic devices, the packages they are wrapped inside, the manufacturing processes that assemble them, the standards that define them, the market that buys them, and the policy processes which influence their deployment.

2. To foster an Institute wide community of researchers in the field of integrated photonics & systems.
The Departments of Electrical Engineering and Computer Science, Materials Science and Engineering, Mechanical Engineering and Economics are consistently ranked as the top graduate programs in the country. Likewise, the Sloan School of Management has consistently ranked first in the nation in the areas of information technology, operations research, and supply chain management. CIPS leverages MIT's strengths, by unifying the photonics researchers in these departments and laboratories to focus on technology developments in photonics. The combined volume of research funds in the photonics area at MIT exceeds $20 million dollars annually. The faculty and staff at MIT in photonics related areas have included Claude Shannon (founder of information theory), Charles Townes (inventor of the laser), Robert Rediker (inventor of the semiconductor lasers), and Hermann Haus (inventor of the single frequency semiconductor laser & ultrafast optical switch). CIPS affiliated faculty and staff continue this tradition of excellence in areas ranging from optical network architectures to novel optical devices to novel photonic materials.

3. To integrate member companies into the MIT photonics community.
CIPS will host annual meetings and seminars in photonics. For CIPS member companies, focused visits to the Institute for individual companies will be organized with faculty and graduate students. In addition, CIPS will hold forums geared towards the creation of campus-industry teams to pursue large-scale research programs. CIPS will host poster sessions at the annual meeting so as to introduce graduate students and their research to industry. CIPS publications will include a resume book of recent graduate students in the area of photonics. Graduates of the Massachusetts Institute of Technology have founded 4,000 firms which, in 1994 alone, employed at least 1.1 million people and generated $232 billion of world sales. Photonics related companies founded by alumni include Sycamore Networks, Analog Devices, Texas Instruments, Hewlett-Packard, and 3Com as well as recent start-up such as OmniGuide.

Member companies have the opportunity to guide the research of CIPS faculty and students through the Working Groups (WGs) and individual graduate student awards.

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T. Thorsen, R.W. Roberts, F.H. Arnold, and S.R. Quake, "Dynamic pattern formation in a vesicle-generating microfluidic device," *Physical Review Letters*, vol. 86, no. 18, pp. 4163-4166, Apr. 2001.

M.A. Unger, H.-P. Chou, T. Thorsen, A. Scherer, and S.R. Quake, "Monolithic microfabricated valves and pumps by multilayer soft lithography," *Science*, vol. 288, no. 5463, pp. 113-116, Apr. 2000.

P.C. Simpson, D. Roach, A.T. Woolley, T. Thorsen, R. Johnston, G.F. Sensabaugh, and R.A. Mathies, "High-throughput genetic analysis using microfabricated 96-sample capillary array electrophoresis microplates," in *Proc. Natl. Acad. Sci.*, vol. 95, no. 5, pp. 2256-2261, Mar. 1998.

L. Calandro, T. Thorsen, L. Barcellos, J. Griggs, D. Baer, and G.F. Sensabaugh, "Mutation analysis in hereditary hemo-chromatosis (Commentary)," *Blood Cells, Molecules and Diseases*, vol. 22, no. 16, 194a-194b, Aug. 1996.

Joel Voldman
NBX Associate Professor
Department of Electrical Engineering and Computer Science

COLLABORATORS

G. Daley, Children's Hospital
K.M. Lim, NUS, Singapore
G. Stephanopoulos, MIT
F. McKeon, Harvard Med. School
G. Vunjak-Novacovic, Columbia
J. White, MIT

GRADUATE STUDENTS

S. Desai, Research Asst., EECS
H.-Y. Lee, Research. Asst., EECS
L.Y. Kim, Research Asst., HST
J.R. Kovac, Research Asst., EECS
N. Mittal, Research Asst., Physics
K. Puchala, Research Asst., EECS
A.D. Rosenthal, Res. Asst., HST
P. Sampattavanich, Res. Asst., EECS
N. Tandon, Research Asst., EECS
B. Taff, Res. Asst., EECS
M. Vahey, Research Asst., EECS

SUPPORT STAFF

S. Chafe, Admin. Asst.

PUBLICATIONS

J. Voldman, "Electrical forces for microscale cell manipulation," *Annual Review of Biomedical Engineering*, Aug. 2006, to be published.

J. Voldman, "Dielectrophoretic traps for cell manipulation," in *BioMEMS and Biomedical Nanotechnology*, A.P. Lee, J. Lee, and M. Ferrari, Eds. New York, NY: Springer, 2006.

A. Rosenthal, B.M. Taff, and M.D. Vahey, "Quantitative modeling of dielectrophoretic traps," *Lab Chip*, vol. 6, no. 4, pp. 508-515, Apr. 2006.

L. Kim, M.D. Vahey, H.-Y. Lee, and J. Voldman, "Microfluidic arrays for logarithmically perfused embryonic stem cell culture," *Lab Chip*, vol. 6, no. 3, pp. 394-406, Mar. 2006.

B.M. Taff and J. Voldman, "A scalable row/column-addressable dielectrophoretic cell-trapping array," in *Proc. Ninth International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS)*, Boston, MA, Oct. 2005, pp. 865-867.

L.Y. Kim, H.-Y. Lee, and J. Voldman, "Logarithmically perfused embryonic stem cell culture on chip," in *Proc. Ninth International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS)*, Boston, MA, Oct. 2005, pp. 530-532.

A.D. Rosenthal and J. Voldman, "Dielectrophoretic traps for single-particle patterning," *Biophysical Journal*, vol. 88, no. 3, pp. 2193-2205, Mar. 2005.

A.D. Rosenthal and J. Voldman, "Simple, strong, and size-selective dielectrophoretic trap for single-cell patterning," in *Proc. Eighth International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS)*, Malmö, Sweden, Sept. 2004, pp. 228-230.

D.S. Gray, J.L. Tan, J. Voldman, and C.S. Chen, "Dielectrophoretic registration of living cells to a microelectrode array," *Biosensors and Bioelectronics*, vol. 19, no. 12, pp. 1765-1774, July 2004.

J. Voldman, "BioMEMS - Building with cells," *Nature Materials*, vol. 2, no. 7, pp. 433-434, July 2003.

J. Voldman, M. Toner, M.L. Gray, and M.A. Schmidt, "Design and analysis of extruded quadrupolar dielectrophoretic traps," *Journal of Electrostatics*, vol. 57, no. 1, pp. 69-90, Jan. 2003.

J. Voldman, M. Toner, M.L. Gray, and M.A. Schmidt, "A microfabrication-based dynamic array cytometer," *Analytical Chemistry*, vol. 74, no. 16, pp. 3984-3990, Aug. 2002.

J. Voldman, M. Toner, M.L. Gray, and M.A. Schmidt, "A dielectrophoresis-based array cytometer," in *Proc. Transducers 2001: 11th International Conference on Solid-State Sensos & Eurosensors XV*, Munich, Germany, June 2001, pp. 322-325.

J. Voldman, R.A. Braff, M. Toner, M.L. Gray, and M.A. Schmidt, "Holding forces of single-particle dielectrophoretic traps," *Biophysical Journal*, vol. 80, no. 1, pp. 531-541, Jan. 2001.

J. Voldman, M.L. Gray, and M.A. Schmidt, "An integrated liquid mixer/valve," *Journal of Microelectromechanical Systems*, vol. 9, no. 3, pp. 295-302, Sept. 2000.

J. Voldman, R.A. Braff, M. Toner, M.L. Gray, and M.A. Schmidt, "Quantitative design and analysis of single-particle dielectrophoretic traps," in *Proc. International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS)*, Twente, The Netherlands, May 2000, pp. 431-434.

J. Voldman, M.L. Gray, and M.A. Schmidt, "Microfabrication in biology and medicine," *Annual Review of Biomedical Engineering*, vol. 1, pp. 401-425, Aug. 1999.

J. Voldman, M.L. Gray, and M.A. Schmidt, "Liquid mixing studies using an integrated mixer/valve," in *Proc. International Conference on Miniaturized Systems for Chemistry and Life Sciences (μTAS)*, Banff, Canada, Oct. 1998, pp. 181-184.

Brian L. Wardle
Boeing Assistant Professor
Department of Aeronautics and Astronautics

COLLABORATORS

K.F. Jensen, MIT
S. Kessler, Metis Design Corp.
W.-S. Kim, MIT
S.-G. Kim, MIT
D. Pafitis, Schlumberger-Doll Research Center
M. A. Schmidt, MIT
D.-J. Shim, MIT
A. H. Slocum, MIT
S.M. Spearing, Univ. Southampton
H. Tuller, MIT
N. Wicks, MIT
C.-Y. Wu, China Steel

GRADUATE STUDENTS

P. Capozzoli, Res. Asst., AA/Sloan
J. Chambers, Res. Asst., AA
N. duToit, Res. Asst., AA
E. Garcia, La Caixa Fellow, AA
A. Mracek, Res. Asst., AA
D. Quinn, NSF Fellow, ME
N. Yamamoto, Res. Asst., AA

UNDERGRADUATE STUDENTS

K. Sorensen, AA
S. Tonn, AA
S. Wicks
H. Wong, AA

SUPPORT STAFF

J. Kane, Research Specialist
P. Lee, Financial Officer
M. Prendergast, Admin. Assist. II

PUBLICATIONS

N.E. duToit, B.L. Wardle, and S.-G. Kim, "Design considerations for MEMS-scale piezoelectric vibration energy harvesters," *Integrated Ferroelectric,* vol. 71, pp. 121-160, 2005.

E.J. Garcia, J. Hart,, B.L Wardle, and A. Slocum, "Composite materials reinforced with long CNTS grown on the surface of fibers," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 1854.

N.E. duToit and B. L. Wardle, "Experimental verification of models for microfabricated piezoelectric vibration energy harvesters," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 1792.

J.T. Chambers, B.L. Wardle, and S.S. Kessler, "Durability assessment of Lamb wave-based structural health monitoring nodes," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 2263.

B.L. Wardle, "The incorrect benchmark shell buckling solution," in *Proc. 47th AIAA Structures, Dynamics, and Materials Conference*, Newport, RI, May 2006, doc. 2028.

S.S. Kessler, K. Amaratunga, and B.L. Wardle, "An assessment of durability requirements for aircraft structural health monitoring sensors," in *Proc. 5th International Worshop on Structural Health Monitoring*, Stanford, CA, Sept. 2005, p. 9.

N. Yamamoto, N. Wicks, and B.L. Wardle, "Wrapping and through-thickness poisson effects on composite plates and shell contact laws," presented at the *46th AIAA Structures, Dynamics, and Materials Conference*, 2005.

N. Wicks, B.L. Wardle, and D. Pafitis, "Horizontal cylinder-in-cylinder buckling under compression and torsion: review and considerations for oil drilling applications," presented at the *15th International Conference on Composite Materials (ICCM)*, 2005.

D. Quinn, S.M. Spearing, and B. L. Wardle, "Residual stress and microstructural evolution in thin film materials for a micro solid oxide fuel cell (SOFC)," presented at the *Materials Research Society (MRS) Annual Fall Conference,* 2004.

THESES AWARDED

Bachelor of Science
S.B.

2004

Buchner, T. (G. Barbastathis), “Kinematics of 3D Folding Structures for Nanostructured Origami™,” December 2004.

Gibbons, J.S. (T.A. Thorsen), “Mobile Power Plants: Waste Body Heat Recovery,” June 2004.

Samouhos, S.V. (T.A. Thorsen), “Mobile Power Plants: Waste Body Heat Recovery,” June 2004.

Slowe, T.J. (M.L. Culpepper), “Design of a Prototyping Press for 3D Monolithic Compliant Mechanisms,” June 2004.

Tsikata, S. (T.A. Thorsen), “Microfluidic Optical Devices,” June 2004.

2005

Barron, K. (G. Chen), “Experimental Studies of the Thermoelectric Properties Of Microstructured and Nanostructured Lead Salts,” February 2005.

Bourgeois, J. (M.L. Culpepper), “Modeling Effects of Adding a Flux Channel to a Planar Magnet–Coil Actuator,” June 2005.

Cukalovic, B. (J.A. del Alamo), “WebLabSim Administrative Interface,” May 2005.

Dibiasio, C.M. (M.L. Culpepper), “Design of Micro–scale Nanomanipulators Utilizing Digital Actuation,” June 2005.

Hopkins, J. (M.L. Culpepper), “Design and Control of a Five–axis AFM Manipulation System,” June 2005.

Hu, J. (T.A. Thorsen), “Microfluidic Microarrays,” June 2005.

Mazzeo, B. (A.I. Akinwande), “Models for Energy States in Thin Film Transistors,” May 2005.

Smith, E. (T.A. Thorsen), “Fabrication of a Picoliter Microreactor,” June 2005.

Vitr, M. (G. Barbastathis), “Image Restoration for 3D Volume-Holographic Imaging Systems,” January 2005.

2006

Allard, N. (M.L. Culpepper), “Compliant Mechanism Learning Toolkit,” June 2006.

Labuz, J. (M.L. Culpepper), “Design, Fabrication, and Testing of a Three-Dimensional Monolithic Compliant Six-Axis Nanopositioner,” June 2006.

Turner, S. (M.L. Culpepper), “Design of an Adaptable, Protective Covering for Precision Experiments,” June 2006.

THESES AWARDED

Master of Engineering
M.Eng.

2004

Akilian, M.K. (M.L. Schattenburg), "Thin Optic Surface Analysis for High Resolution X-ray Telescopes," September 2004.

Chang, C.-H. (M.L. Schattenburg), "Fabrication of Extremely Smooth Blazed Gratings," June 2004.

Das, R. (M.A. Baldo), "Photovoltaic Devices using Photosynthetic Protein Complexes," February 2004.

Mehta, A. (M.A. Schmidt, K.F. Jensen), "A Microfabricated Solid Oxide Fuel Cell," June 2004.

Peters, J. (L. Daniel), "Design of High Quality Factor Spiral Inductors in RF MCM-D," September 2004.

Quentmeyer, T. (V.M. Bove, Jr.), "Delivering Real-Time Holographic Video Content with Off-the-Shelf PC Hardware," May 2004.

Wang, Y.C. (T.A. Thorsen), "On-chip Multidimensional Biomolecule Separation Using Multilayer Microfabricated Valves," February 2004.

Wang, A.I. (A.I. Akinwande), "Threshold Voltage in Pentacene Field Effect Transistors with Parylene Dielectric," May 2004.

2005

Abrokwah, K. (D.S. Boning), "Characterization and Modeling of Plasma Etch Pattern Dependencies in Integrated Circuits," February 2005.

Ackerman, N. (A.P. Chandrakasan), "A Platform for Ultra Wideband Communication Systems," May 2005.

Arora, W.J. (G. Barbastathis, H.I. Smith), "Nanostructured Origami™: Folding Thin Films out of the Plane of a Silicon Wafer with Highly Stressed Chromium Hinges," June 2005.

Gadish, N. (J. Voldman), "A Microfabricated Dielectrophoretic Micro-organism Concentrator," August 2005.

Park, M. (M.H. Perrott), "Optical/Electrical Implementation Techniques for Continuous-Time Sigma-Delta A/D Converters," June 2005.

Selbst, A. (R. Sarpeshkar), "Clock Division as a Power Saving Strategy in a System Constrained by High Transmission Frequency and Low Data Rate," June 2005.

Tsai, J. (A.P. Chandrakasan), "Design and Implementation of an Online Laboratory for Introductory Digital Systems," August 2005.

Urbanski, J.P. (T.A. Thorsen), "Application of Microfluidic Emulsion Technology to Biochemistry, Drug Delivery and Lab-on-a-Chip Programmability," June 2005.

Vollmer, A. (T.A. Thorsen), "Development of an Integrated Microfluidic Platform for Oxygen Sensing and Delivery," June 2005.

Walker, J.Z. (A.I. Akinwande, A.P. Chandrakasan), "A Low Power Display Driver with Simultaneous Image Transformation," February 2005.

Waller, L.A. (G. Barbastathis), "Feedback Loop Design and Experimental Testing for Integrated Optics with Micro-mechanical Tuning," June 2005.

Werkmeister, J. (A.H. Slocum), "Development of Silicon Insert Molded Plastic (SIMP," June 2005.

Winter, A. (M.L. Culpepper), "Design of Fluid Film Journal Bearings Containing Continuous 3D Fluid Pathways Which are Formed by Wrapping a Sheet Containing 2D Through–cut Features," June 2005.

THESES AWARDED

Master of Engineering
M.Eng

2006

Bradley, M.S. (V. Bulović), "Highly Absorptive Thin Films for Integrated Photonic Devices," February 2006.

Kim, L. (V. Bulović), "Deposition of Colloidal Quantum Dots by Microcontact Printing for LED Display Technology," February 2006.

Lamba, K. (V. Bulović, C.G. Sodini), "An Integrated Circuit for Feedback Control & Compensation of an Organic LED Display," June 2006.

Lin, A. (V. Bulović), "A Silicon Current Sensing Amplifier and Organic Imager for an Optical Feedback OLED Display," February 2006.

Lin, K. (M.L. Culpepper), "Multi-axis Compliant Mechanism-based Nanopositioner for Multi-mode Mechanical Testing of Carbon Nanotubes," February 2006.

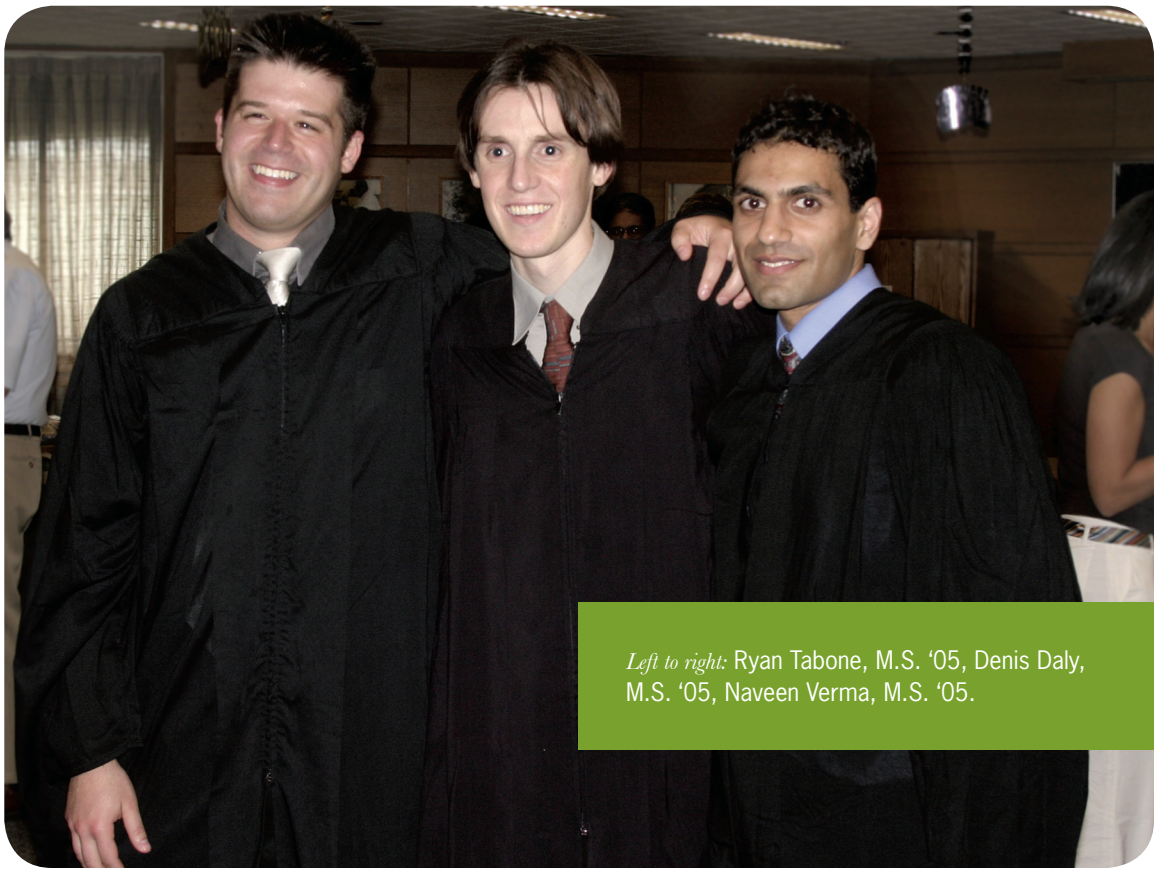
Rayanakorn, S. (H.-S. Lee), "Design of Micropower CMOS Operational Amplifiers," June 2006.

Reyes-Gonzalez, N.I. (J. Han), "AC-Electrophoresis of Biomolecules in Nanofluidic Filter Array Devices," January 2006.

Smalley, D. (V.M. Bove, Jr.), "Integrated-Optic Holovideo," September 2006.

Timm, R. (M.L. Culpepper), "Visual-based Methods in Compliant Mechanism Optimization," February 2006.

Young, S. (L.A. Kolodziejski), "Characterization of Novel III-V Semiconductor Devices," June 2006.



Left to right: Ryan Tabone, M.S. '05, Denis Daly, M.S. '05, Naveen Verma, M.S. '05.

THESES AWARDED

Master of Science
S.M.

2004

Abu Ibrahim, F. (A.H. Slocum), "Low-Cost Precision Waterjet," June 2004.

Au, S. (C. Livermore), "Solder Self-Assembly for MEMS Fabrication," September 2004.

Caramana, C. (H.I. Smith), "Pattern-Placement-Error Detection for Spatial-Phase-Locked E-Beam Lathography (SPLEBL)," June 2004.

Crain, E.A. (M.H. Perrott), "Fast Offset Compensation for a 10 Gb/s Limit Amplifier," June 2004.

Cybulski, J.S. (G. Chen), "Fabrication, Modeling, and Electrical Characterization of Self-Assembling Microscale Rollup Structures," June 2004.

Hill, S.L. (V.M. Bove, Jr.), "Scalable Multi-view Stereo Camera Array for Real World Real-Time Image Capture and Three-Dimensional Displays," May 2004.

Jia, J. (C.V. Thompson), "The Mechanism of Thin Film Si Nanomachining Using Femtosecond Laser Pulses," June 2004.

Kuo, S. (M.H. Perrott), "Linearization of a Pulse Width Modulated Power Amplifier," June 2004.

Lee, H. (M.J. Cima), "Experimental Study of the Atomization Processfor Viscous Liquids by Meniscus Perturbation and Micro Air Jet," June 2004.

Patel, A. (H.I. Smith), "The Development of a Prototype Zone-Plate Array Lithography (ZPAL) System," May 2004.

Schmidt, A.J. (G. Chen), "Photothermal Lithography," June 2004.

Thompson, K. (A.H. Slocum), "MEMS Fluid Coupling," June 2004.

Verma, H. (C.V. Thompson), "Scanned Pulsed Laser Annealing of Cu Thin Films," June 2004.

Wei, F. (C.V. Thompson), "The Electromigration Drift Velocity and the Reliability of Dual-Damascene Copper Interconnect Trees," February 2004.

Wells, B. (C.V. Thompson), "Commercial Applications of Nanostructures Created with Ordered Porous Alumina," June 2004.

2005

Arango, A. (V. Bulović), "Quantum Dot Heterojunction Photodetector," February 2005.

Cheung, K. (M.A. Schmidt), "Die Level Glass Frit Vacuum Packaging for a Micro-Fuel Processor System," May 2005.

Dahl, R.A. (C.V. Thompson), "Femtosecond Laser-Microstructured Silicon for Photodetection: Technology Transfer Analysis," June 2005.

Dalton, B. (V.M. Bove, Jr.), "Audio Based Localisation for Ubiquitous Sensor Networks," September 2005.

Daly, D. (A.P. Chandrakasan), "An Energy Efficient Transceiver for Wireless Sensor Networks," May 2005.

duToit, N.E. (B.L. Wardle), "Modeling and Design of a MEMS Piezoelectric Vibration Energy Harvester," May 2005.

Finchelstein, D. (A.P. Chandrakasan), "Low-Power Digital Processor for Wireless Sensor Networks," May 2005.

Frantzeskakis, E. (C.V. Thompson), "Analysis of Potential Applications for the Templated Dewetting of Metal Thin Films," June 2005.

Gazor, M. (D.S. Boning), "Design for Manufacturability with Regular Fabrics in Digital Integrated Circuits," May 2005.

Herrington , W. (I. Masaki), "Image Fusion for a Nighttime Driving Display," June 2005.

THESES AWARDED

Master of Science
S.M.

Ho Duc, H.L. (M.J. Cima), "Packaging for a Drug Delivery Microelectromechanical System," February 2005.

In, H.J. (G. Barbastathis), "Origami Nanofabrication of Three-dimensional Electrochemical Energy Storage Devices," June 2005.

Lajevardi, P. (A.P. Chandrakasan), "Design of a 3-Dimension FPGA," July 2005.

LeCoguic, A. (J. Han), "Gate Potential Control of Nanofluidic Devices," May 2005.

Lee, H. (G. Chen), "Thermoelectric Properties of Si-Ge Nanocomposites," January 2005.

Mao, P. (J. Han), "Fabrication and Characterization of Nanofluidic Channels for Studying Molecular Dynamics in Confined Environments," January 2005.

Matalon, N. (C.G. Sodini), "An Implementation of a 5.25 GHz Transceiver for High Data Rate Wireless Applications," December 2005.

McCaghren, N. (D.S. Boning), "Visual Indicators for Process Control," June 2005.

Nanda, G (V.M. Bove, Jr.), "Accessorizing with Networks: the Possibilities of Building with Computational Textiles," September 2005.

Pilpre, A. (V.M. Bove, Jr.), "Self-* Properties of Multi-Sensing Entities in Smart Environments," May 2005.

Rushfeldt, S. (C.V. Thompson), "Sensor Applications of Carbon Nanotubes," June 2005.

Ryu, K. (V. Bulović, C.G. Sodini), "Characterization of Organic Field Effect Transistors for OLED Displays," June 2005.

Tabone, R. (V. Bulović), "Sub-20nm Substrate Patterning Using A Self-Assembled Nanocrystal Template," June 2005.

Verma, N. (A.P. Chandrakasan), "An Ultra Low Power ADC for Wireless Micro-Sensor Applications," May 2005.

Wong, M. (J.A. del Alamo), "The Effect of Varying Gate-Drain Distance on the RF Power Performance of Pseudomorphic High Electron Mobility Transistors," August 2005.

2006

Barabas, J. (V.M. Bove, Jr.), "Sensor Planning for Novel View Generation by Camera Networks," May 2006.

Garcia, E. (B.L. Wardle), "Characterization of Composites with Aligned Carbon Nanotubes (CNTs) as Reinforcement," May 2006.

Hadiashar, A. (J.L. Dawson), "Chopper Stabilization in Analog Multipliers," June 2006.

Hirsh, D. (V.M. Bove, Jr.), "Piecing Together the Magic Mirror: Creating Responsive Spaces with Autonomous Elements," September 2006.

Mracek, A. (B.L. Wardle), "Towards and Embeddable Structural Health Monitoring Sensor: Design and Optimization of MEMS Piezoelectric Vibration Energy Harvesters," June 2006.

Quinn, D. (B.L. Wardle), "Microstructure, Residual Stress, and Mechanical Properties of Thin Film Materials for a Microfabricated Solid Oxide Fuel Cell," May 2006

Vahey, M. (J. Voldman), "A Novel Method for the Continuous Separation of Microorganisms based on Electrical Properties," January 2006.

THESES AWARDED

Doctor of Philosophy
Ph.D.

2004

Chiang, C. (C.V. Thompson), "Geometrical and Microstructural Effects on Electromigration in Advanced Cu-Based Metallization Systems," June 2004.

De Mas Valles, N. (K.F. Jensen, M.A. Schmidt), "Scalable Multiphase Microchemical Systems for Direct Fluorination," June 2004.

Freisen, C. (C.V. Thompson), "Stress Evolution During Growth and Atomic-Scale Surface Structure Effects in Transition-Metal Thin Films," June 2004.

Kershner, R.J. (M.J. Cima), "Surface Forces During Electrophoretic Assembly of Micron Scale Silica Particles," June 2004.

Li, J. (A.H. Slocum), "Electrostatic Zipping Actuators and Their Application to MEMS," January 2004.

Liu, W. (G. Chen), "In-Plane Thermoelectric Properties of Si/Ge Superlattices," July 2004.

Love, N. (I. Masaki), "Recognition of 3D Compressed Images and its traffic monitoring applications," June 2004.

Moon, E. (H.I. Smith), "Interferometric-Spatial-Phase Imaging for Sub-Nanometer Three Dimensional Positioning," September 2004.

Shawgo, R.S. (M.J. Cima), "In vivo Activation and Biocompatibility of a MEMS Microreservoir Drug Delivery Device," June 2004.

Tupper, M.M. (M.J. Cima), "Fabrication and Assembly of Micron-scale Ceramic Components," February 2004.

Walsh, M. (H.I. Smith), "On the Design of Lithographic Interferometers and their Application," September 2004.

2005

Ariel, N. (E.A. Fitzgerald), "Integrated Thin Film Batteries on Silicon," September 2005.

Barwicz, T. (H.I. Smith, H.L. Tuller), "Accurate Nanofabrication Techniques for High-Index-Contrast Microphotonic Devices," September 2005.

Calhoun, B. (A.P. Chandrakasan), "Low Energy Digital Circuit Design Using Sub-threshold Operation," December 2005.

Checka, N. (A.P. Chandrakasan, R. Reif), "Substrate Noise Analysis and Techniques for Mitigation in Mixed-Signal RF Systems," June 2005.

Choy, H.K.H. (C.G. Fonstad, Jr.), "Quantum Wells on Indium Gallium Arsenic Compositionally Graded Buffers realized by Molecular Beam Epitaxy," January 2005.

Coe-Sullivan, S. (V. Bulović), "Hybrid Organic/Quantum Dot Thin Film Structures and Devices," June 2005.

Chen, A. (A.I. Akinwande, H.-S. Lee), "CMOS Micro-Display," June 2005.

Krishnan, R. (C.V. Thompson), "Templated Self-assembly of Nanoporous Alumina: Pore Formation and Ordering Mechanisms, Methodologies, and Applications," June 2005.

Li, Y. (M.J. Cima), "Mechanical Characterization and in vivo Operation of an Implantable Drug Delivery MEMS Device," February 2005.

Lauer, I. (D.A. Antoniadis), "The Effects of Strain on Carrier Transport in Thin and Ultra-Thin SOI MOSFETs," September 2005.

Markina, A. (L.A. Kolodziejski), "Design and Simulation for the Fabrication of Integrated Semiconductor Optical Logic Gates," September 2005.

THESES AWARDED

Doctor of Philosophy
Ph.D.

Meninger, S. (M.H. Perrott), "Low Phase Noise, High Bandwidth Frequency Synthesizer Techniques," June 2005.

Pham, A. (C.G. Sodini), "Outphase Power Amplifiers in OFDM Systems," December 2005.

Pitera, A. (E.A. Fitzgerald), "Engineered Substrates for Coplanar Integration of Lattice-Mismatched Semiconductors with Silicon," January 2005.

Qi, M. (H.I. Smith), "Three Dimensional Nanofabrication of Photonic Crystals and Polarization Splitters and Rotators," April 2005.

Sprunt, A. (A.H. Slocum), "A Variable Capacitor Made from Single Crystal Silicon Fracture Surface Pairs," August 2005.

Steyn, L. (A. Epstein, M.A. Schmidt), "A Microfabricated Electrostatic Indiction Turbine-generator," May 2005.

Tandon, S. (H.I. Smith, L.A. Kolodziejski), "Engineering Light Using Large Area Photonic Crystal Devices," June 2005.

Tavakoli-Dastjerdi, M. (R. Sarpeshkar), "An Analog VLSI Front End for Pulse Oximetry," October 2005.

Wang, H.R. (M.J. Cima), "Gradient-index (GRIN) Lenses by Slurry-based Three-Dimensional Printing (S-3DP™)," February 2005.

Zanzotto, A. (K.F. Jensen), "Integrated Microbioreactors for Rapid Screening and Analysis of Bioprocesses," February 2005.

Zhang, F. (H.I. Smith), "Real-Time Spatial-Phase-Locked Electron-Beam Lithography," September 2005.

Willoughby, P. (A.H. Slocum), "Elastically Averaged Precision Alignment," June 2005.

2006

Callebaut, H. (Q. Hu), "Analysis of the Electron Transport Properties in Quantum Cascade Lasers," April 2006.

Fan, A. (A.I. Akinwande), "3-D Integration Using Copper Wafer Bonding," June 2006.

Gervais, T. (K.F. Jensen, P.K. Sorger), "Mass Transfer and Structural Analysis of Microfluidic Sensors," February 2006.

Kralj, J.G. (K.F. Jensen, M.A. Schmidt), "Continuous Flow Separation Techniques for Microchemical Synthesis," February 2006.

Lee, J.C. (T.P. Orlando), "Resonant Readout of a Superconducting Persistent Current Qubit," June 2006.

Mallett, J. (V.M. Bove, Jr.), "The Role of Groups in Smart Camera Networks," February 2006.

Montoya, J. (M.L. Schattenburg), "Towards Nano-accuracy in Scanning Beam Interference Lithography," June 2006.

Murali, K. (T.P. Orlando), "Electromagnetically Induced Transparency and Electron Spin Dynamics using Superconducting Quantum Circuits," February 2006.

Sun, W. (G. Barbastathis) "Profilometric Imaging Using Volume Holograms," March 2006.

Tian, K. (G. Barbastathis) "Three-Dimensional Optical Information Processing," March 2006.

Yang, H. (R. Sarpeshkar), "An Energy-Efficient Time-Based Analog-to-Digital Converter," January 2006.

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Limits on ADC Power Dissipation
September 20, 2005 | Boris Murmann, Stanford University

High Performance Link Challenges and Tradeoffs Above 5Gb/s
September 27, 2005 | Jared Zerbe, Rambus

Adaptive Designs for Power and Thermal Optimization
October 4, 2005 | Sam Naffziger, Intel Corporation

Analog Design: Art or Science?
October 25, 2005 | Mar del Mar Hershenson, SabioLabs

Silicon Process Directions in the Nanoelectronics Era
November 1, 2005 | Mark Pinto, Applied Materials

0-60GHz in Three Years: mm-Wave CMOS Research at BWRC
November 8, 2005 | Ali Niknejad, UC Berkeley

All-Digital RF Frequency Synthesizer and Transmitter for Cellular Phones
November 29, 2005 | Robert Bogdan Staszewski, Texas Instruments

Measurement Tools for Electronics and the Life Sciences
December 6, 2005 | Jim Hollenhorst, Agilent Technologies

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Bioelectronics
February 14, 2006 | Rahul Sarpeshkar, MIT

Transformation of CMOS Scaling: How Many "Moore" Generations?
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Microchips for Implantable Drug Delivery and Biosensing
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Integrative MEMS Materials and Processes for Bio-Micro-Systems
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Integration of Synthetic Nanomaterials for Nano- and Macro- Electronics
May 7 , 2006 | Ali Javey, UC Berkeley

FPGA Ride the Tide of Moore's Law
May 16, 2006 | Ivo Bolsens, Xilinx Inc.

ABBREVIATIONS

Massachusetts Institute of Technology

ACC .....Advanced Concepts Committee (MIT LL)
CAES .....Center for Advanced Engineering Study
ChE.....Department of Chemical Engineering
ChemE .....Department of Chemical Engineering
CICS .....Center for Integrated Circuits and Systems
CIPS.....Center for Integrated Photonic Systems
CMI .....Cambridge-MIT Institute
CMSE.....Center for Materials Science and Engineering
CSR .....Center for Space Research
DMA.....Dupont-MIT Alliance
DMSE.....Department of Materials Science and Engineering
EECS .....Department of Electrical Engineering and Computer Science
HST .....Health Sciences and Technology, Harvard-MIT
ICL.....Integrated Circuits Laboratory
ISN.....Institute for Soldier Nanotechnologies
ITRC.....Intelligent Transportation Research Center
LEES.....Laboratory for Electromagnetic and Electronic Systems
LFM.....Leaders for Manufacturing
MIG.....Microsystems Industrial Group
MIT .....Massachusetts Institute of Technology
MNSL.....Micro & Nano Systems Laboratory
MPC.....Materials Processing Center
MTL .....Microsystems Technology Laboratories
NSL .....NanoStructures Laboratory
RLE.....Research Laboratory of Electronics
SMA.....Singapore-MIT Alliance
SML .....Space Microstructures Laboratory
SOE .....School of Engineering
TRL.....Technology Research Laboratory
UROP .....Undergraduate Research Opportunities Program

Private Industry

AMD.....Advanced Micro Devices
CSDL .....Charles Stark Draper Laboratory
HP .....Hewlett-Packard
IBM .....International Business Machines Corporation
KIMM.....Korea Institute of Machinery and Materials
MARCO.....Microelectronics Advanced Research Corporation
  C2S2.....Center for Circuits and Systems Solutions
  GSRC .....Gigascale Systems Research Center
  IFC .....Interconnect Focus Center
MSD.....Center for Materials, Structures and Devices
MGH.....Massachusetts General Hospital
NTT.....Nippon Telephone and Telegraph
SIA.....Semiconductor Industry Association
SRC .....Semiconductor Research Corporation
TI.....Texas Instruments

Government

AFOSR.....U.S. Air Force Office of Scientific Research
AFRL .....Air Force Research Laboratories
ARDA .....Advanced Research and Development Activity
ARL.....Army Research Labotratories
ARO MURI.....Army Research Office M
CSE .....Consortium on Superconducting Electronic
DARPA.....Defense Advanced Research Projects Agency
DOD.....Department of Defense
DOE .....Department of Energy
DURINT .....Defense University Initiative on Nanotechnology
JPL .....Jet Propulsion Laboratories
JSEP .....Joint Services Electronics Program
LANL.....Los Alamos National Laboratory
MDA.....Missile Defense Agency
MRSEC.....Materials Research Science and Engineering Center
MURI .....Multi University Research Initiative
NASA .....National Aeronautics and Space Administration
NCIPT.....National Center for Integrated Photonics Technology
NDSEG.....National Defense Science and Engineering Graduate
NIH .....National Institutes of Health
  NCI.....National Cancer Institute
  NCRR .....National Center for Research Resources
  NIDDK .....National Institute of Diabetes and Digestive and Kidney Diseases
  NIBIB .....National Institute of Biomedical Imaging and BioEngineering
  NHLBI.....National Heart, Lung, and Blood Institute
NIST.....National Institute of Standards and Technology
NOAA .....National Atmospheric and Oceanographic Administration
NREL.....National Renewable Energy Laboratory
NRL.....Naval Research Laboratory
NSA .....National Security Administration
NSF.....National Science Foundation
  CMSE .....Center for Materials Science and Engineering
  MRSEC .....Materials Research Science and Engineering Centers
  NIRT .....Nanotechnology and Interdisciplinary Research Initiative
  SGER.....Small Grant for Exploratory Research
ONR.....Office of Naval Research

Other

CFI.....CAD Framework Initiative
CIE.....Commission International de l'Eclairage
CIM .....Computer Integrated Manufacturing
IEEE .....Institute of Electrical and Electronics Engineers
IEDM .....International Electronic Devices Meeting

IME .....Institute of Microelectronics, Singapore
IMEC .....Interuniversity MicroElectronics Center
MCNC .....Microelectronics Center of North Carolina
MRS.....Materials Research Society
NATO .....North Atlantic Treaty Organization
NTCIP.....National Transportation Communications for Intelligent Transportation
WiMAX.....Worldwide Interoperability for Microwave Access, Inc.

Technical

AAO .....Anodic aluminum oxide
ACEO .....AC electro-osmosis
ACPR.....Adjacent channe power ratio
ADC .....Analog-to-digital converter
AFM .....Atomic force microscope
ALD.....Atomic layer deposition
AMOL .....Absorbance-two-wavelength scheme
APCVD .....Atmospheric pressure chemical vapor deposition
ASIC.....Application-specific integrated circuit
BEOL.....Back-end-of-line
BER.....Bit-error-rate
BiCMOS.....Bipolar complementary metal oxide semiconductor
BPSK .....Binary phase shift keying
BPV.....Back-propagation of variance
BTBT.....Band-to-band tunneling
CAD .....Computer aided design
CATV.....Category V
CBSC .....Comparator-based switched-capacitor circuit
CCD .....Charge couple device
CCR .....Critically coupled resonator
CDR .....Clock and data recovery
CFB.....Cartesian feedback
CFT.....Clock feed-through
CML .....Current mode latch
CMOS .....Complementary metal oxide semiconductor
CMP.....Chemical mechanical planarizetion
CNT .....Carbon nanotube
COC.....Cyclic olefin copolymer
COIL.....Chemical oxygen iodine laser
CV.....Capacitance voltage
CVD .....Chemical vapor deposition
DAC .....Digital-to-analog converter
DBR .....Dielectric Bragg reflector
DCA .....Dielectric continuum approximation
DCP .....Dielectrophoretic cell patterning
D-CAP.....Digitally-configurable analog processor
DEM.....Dynamic element matching
DEP .....Dielectrophoresis
DHI .....Digital holographic imaging
DIBL.....Drain-induced barrier lowering
DPD .....Digital predistortion
DRIE.....Deep reactive-ion etching
DSP .....Digital signal processing
DUT .....Devices-under-test
ECG .....Electrocardiogram
EEG .....Electroencephalogram
EEPROM.....Electrically erasable programmable read only memory
EL.....Electroluminescence
EM.....Electromagnetic
ENOB.....Effective number of bits
EPD .....Endpoint detection
FACS.....Flow-assisted Cell Sorting
FDTD.....Finite difference time domain
FEOL.....Front-end-of-line
FET .....Field-effect transistor
FFT .....Fast Fourier transform
FIR .....Finite impulse response
FOM .....Figure of merit
FOV.....Field of view
FPGA.....Field programmable gate array
GeOI.....Germanium-on-insulator
GMR.....Giant magnetoresistance
GOI .....Germanium-on-insulator
GP .....Geometric programming
HD .....Harmonic distortion
HDQ .....Harmonic Differential Quadrature
HEMT .....High-electron mobility
HIC.....High-index-contrast
HM.....Herringbone mixer
HOI .....Heterostructure on insulator
HSQ .....Hydrogen silsesquioxane
ICEO .....Induced charge electro-osmosis
IDE.....Interdigitated electrodes
IMD .....Inter-modulation distortion
INL.....Integral nonlinearity
ISI .....Inter symbol interference
ISM .....Industrial, scientific, medical
ITO.....Indium-tin-oxide
IV.....Current voltage
KOH .....Potassium hydroxide
LED.....Light-emitting device
LINC.....Laboratory instrument computer
LNA.....Low noise amplifier
LPCVD.....Low pressure chemical vapor deposition
LSB.....Lower sideband
MAA .....methacrylic acid
MDLL .....Multiplying delay-locked loops
MEM .....Micro-electro-mechanical
M-HEMT.....Metamorphic high-electron-mobility transistor
MEMS .....Micro-electro-mechanical systems
MGA.....Micro gas analyzer
MMA .....Methylmethacrylate
MMSE .....Minimum mean square error
MMW.....Millimeter-wave
MOCVD.....Metallorganic chemical vapor deposition
MOR.....Model-order-reduction
MOS.....Metal-oxide-semiconductor
MOSFET .....Metal-oxide-semiconductor field-effect transistor
MPIE .....Mixed-potential-integral-equation
MRAM .....Magnetic-random-access memory

NEM.....Nano-electro-mechanical
NIL.....Nanoimprint lithography
NMOS .....Negative-channel metal-oxide semicondutor
OEO .....Optical-electronic-optical
OFDM.....Orthogonal frequency division multiplexing
OFET.....Organic field-effect transistor
OFF .....Off
OHC .....Outer hair cells
OLED .....Organic light-emitting diode
OPL.....Optical projection lithography
PA.....Power amplifier
PAE .....Power-added efficiency
PCR .....Polymerase chain reaction
PDAC .....poly diallyldimethylammonium chloride
PDMS.....Polydimethylsiloxane
PECVD .....Plama enhanced chemical vapor deposition
PEM .....Proton exchange membrane; polymer electrolyte membrane
PFM .....Pulse frequency modulation
PHEMT .....Pseudomorphic high-electron mobility transistor
PHY.....Physical layer
PIV .....Particle image velocimetry
PL.....Photoluminescence
PLL .....Phase-locked loops
PMGI .....Polymethylglutarimide
PMMA.....Polymethylmethacrylate
PMOR.....Parameterized model reduction
PMOS.....Postive channel metal oxide semicondutor
PPM .....Pulse-position modulated
PRF .....Pulse-repetition frequency
PROM.....Parameterized reduced-order models
PSV.....Pseudo-spin-valve
PTM .....Predictive technology models
QCL .....Quantum-cascade laser
QD .....Quantum dot
RC .....Resonant cavity
RFID .....Radio frequency identification
RIE .....Reactive-ion etching
ROI.....Regions of interest
RSM .....Response surface model
RTNIL .....Room-temperature nanoimprint lithography
RVHI .....Rainbow volume holographic imaging
SAR.....Successive approximation register
SAW.....Surface acoustic wave
SBR .....Saturable Bragg reflector
SCE .....Short-channel Effects
SEBL.....Scanning-electron-beam lithography
SEM .....Scanning-electron microscope
SFDR.....Spur-free dynamic range
SGM.....slanted groove mixer
SHM.....Staggered herringbone mixer
SIMS .....Secondary ion-mass spectrometry
SiNW.....Silicon nano-wire
SiNWT .....Silicon nanowire transistors
SMR .....Suspended microchannel resonator
SMU.....Sense-Measurement Unit
SNR .....Signal-to-noise ratio
SOA .....Semiconductor optical amplifier
SoC .....System-on-chip
SOG.....Singlet oxygen generator
SOI.....Silicon on insulator
SOLES .....Silicon on lattice-engineered substrate
SPLEBL .....Spatial-phase-locked electron-beam lithography
SPM.....Scanning probe micrograph
SRAM .....Static random access memory
SSDSOI .....Strained-silicon directly on insulator
STI.....Shallow trench isolation
TAT .....Trap-assisted tunneling
TDC .....Time-to-digital
TDD .....Threading dislocation density
TERS.....Tip enhanced Raman spectroscopy
TIPS.....Thermal inkjet pico-fluidic drop dispensing system
TPV.....Thermophotovoltaic
TTTDD.....Time-temperature threading dislocation density
UHVCVD .....Ultra high vacuum chemical vapor deposition
ULSI.....Ultra Large Scale Integration
UWB.....Ultra-wideband
VCO .....Voltage Controlled Oscillators
VCSEL.....Vertical-cavity Surface-emitting Laser
VDG .....Voltage from Drain to Gate
VLS.....Vapor-liquid-solid
VLSI .....Very Large Scale Integration
VPR.....Versatile Place and Route
VSCEL.....Vertical cavity surface-emitting laser
WiGLAN .....Wireless gigabit local area network
WLAN.....Wireless local area network
WSP.....Water soluble particles
YSZ.....Yttria-stabalized zirconia oxide
ZPAL .....Zone-plate-array lithography

index

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