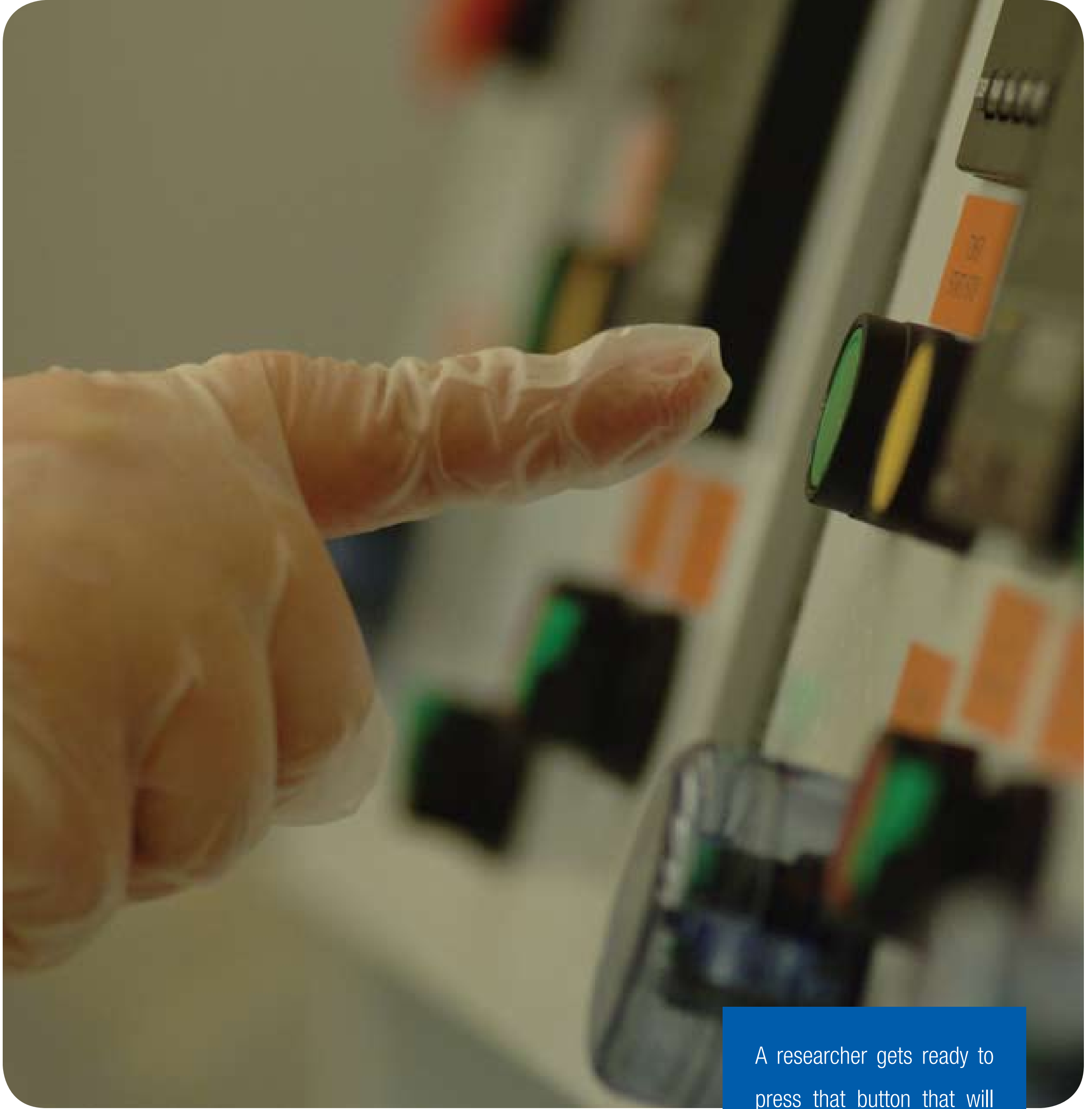


A researcher gets ready to press that button that will begin a new process in ICL.

FACILITIES

FACILITIES

Process research and device fabrication at MTL are primarily conducted in three laboratories; the Integrated Circuits Laboratory (ICL), the Technology Research Laboratory (TRL) and the Exploratory Materials Laboratory (EML). The ICL is designed, equipped and staffed to serve as a highly advanced silicon integrated circuit, device, structures, and process research facility. The laboratory houses a complete six-inch silicon IC fabrication line. Cassette-to-cassette transfer techniques are employed extensively, and VLSI discipline is maintained throughout the facility.

The TRL supports the development of novel process technologies and provides facilities for the fabrication of novel micro and nanostructures

The EML is a highly flexible microfabrication resource with all the basic fabrication capabilities and few limitations, beyond those called for by safety protocols, on substrate and source materials

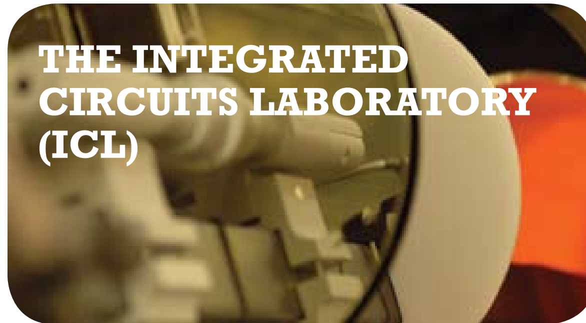
The TRL and ICL are complementary laboratories. Since the ICL is designed to permit fabrication of complex integrated circuits and devices, by necessity it must be operated under the strict discipline that is required for state-of-the-art silicon device and circuit research. The TRL is designed to make up for any loss of flexibility that this discipline imposes. Similarly, fabrication of devices in the ICL can readily take advantage of new technologies that have been developed in the TRL. Examples of such technologies include deep reactive ion etching and wafer bonding. The Class 100 clean room environment and clean room procedures employed in the TRL assure that wafers can move between the ICL and TRL without compromising either the wafers or the facilities.

EML provides an additional degree of flexibility for samples that do not require strict cleanliness or contamination control. Samples that have been in EML cannot be transferred into ICL or TRL.

In addition to these MTL facilities, the Research Laboratory of Electronics (RLE) maintains a shared Scanning Electron Beam Facility (SEBL) with access to direct-write e-beam capabilities

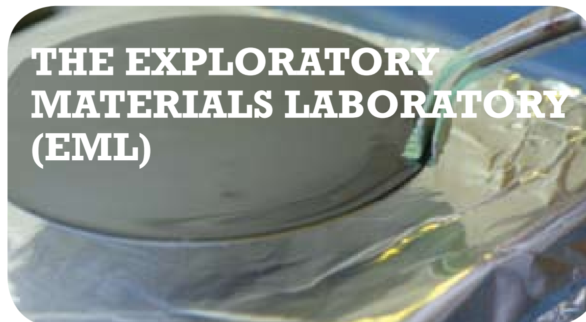
MTL has continued to serve the microfabrication needs of the MIT community, working on projects from an ever-larger variety of academic departments (e.g., Biology, Chemical Engineering, Mechanical Engineering, Physics). Recently, the Scanning Electron Beam Facility (SEBL) was qualified to be compatible with TRL processes, adding nanometer-size capability to our lithography tool set. The Process Technology Committee reviews all new processes in ICL/TRL to ensure the integrity of all processes.

A detailed list of equipment and use protocols for MTL can be found on the MTL web site (http://mtlweb.mit.edu).



7,910 sq-ft integrated circuit fabrication facility comprised of:
- 2,800 sq.-ft Class 10 clean space
- 4,000 sq.-ft support space
- 460 sq.-ft characterization space

3,600 sq-ft of laboratory space comprised of:
- 2,200 sq.-ft class 100 clean space
- 1,400 sq.-ft support space



This is a flexible thin film deposition lab, with photolithography, etching and metrology capabilities.
- 2,100 sq.-ft class 10,000 clean space

PERSONNEL AND COMMITTEES

Director's Office

M. Schmidt, Director
A. Chandrakasan, Faculty Associate Director
J. del Alamo, Faculty Associate Director
J. Hoyt, Faculty Associate Director
S. Crooks, Associate Director
V. Diadiuk, Associate Director

MTL Faculty Policy Board

D. Antoniadis, Professor, EECS
D. Boning, Assoc Dept. Head, EECS and Professor, EECS
A. Chandrakasan, Professor, EECS
J. del Alamo, Professor, EECS
J. Hoyt, Associate Professor, EECS
M.A. Schmidt, MTL Director and Professor, EECS (Chair)
C.G. Sodini, Professor, EECS
S. Crooks, Associate Director (ex-officio)
V. Diadiuk, Associate Director (ex-officio)

Administrative Services

S. Crooks, Associate Director and Administrative Officer
D. Hodges-Pabon, Personnel Officer
A. Adams-Heath, Fiscal Officer
M. Karapetian, Media Specialist
T. Santiago, Account Assistant (Billing)
D. Moore, Accounts Payable

Account assistant Tatia Santiago.

Fabrication Services

V. Diadiuk, Associate Director and Principal Research Engineer
P. Varley, Clerical Assistant

Fabrication
D. Adams, Research Specialist, Techn. Supervisor
D. Terry, Project Technician
T. Turner, Technician A
M. Klotz, Technician C

Diffusion and Device Characterization
B. Alamariu, Research Engineer

Vacuum Etching
R. Bicchieri, Research Specialist
D. Jameson, Research Specialist
E. Lim, Research Specialist

Vacuum Deposition
P. Zamora, Research Specialist

EML Processes
K. Broderick, Research Associate

Facilities
P. McGrath, Research Specialist

Equipment Maintenance
B. McKenna, Research Specialist

CORAL and Web Applications
I. Lin, Research Specialist

Photolithography
P. Tierney, Research Specialist

Project Processing
S. Poesse, Research Specialist

Computational Services

J. del Alamo, Professor and Associate Director
T. Lohman, Research Specialist, System/CIM Manager
M. Hobbs, Research Specialist, System Manager
W. Maloney, Research Specialist, System Manager

CAD Services

A. Chandrakasan, Professor and Associate Director
M. McIlrath, Research Specialist, System/CAD Manager

Process Technology Committee (PTC)

A. Akinwande, Associate Professor, EECS
V. Diadiuk, MTL Associate Director, Operations (Chair)
J. Lang, Professor, EECS
C. Livermore, Assistant Professor, MechE
J. Hoyt, Associate Professor, EECS
D. Isaacson, MSE
A. Khakifirooz, EECS
O. Nielson, ChemE
N. Waldron, EECS

PTC meeting in progress, from left to right: Ali Khakifrooz, David Isaacson, Niamh Waldron, Jifeng Liu, Judy Hoyt, Vicky Diadiuk.