A research specialist examines his work on a wafer in the Hoyt lab.

# EMERGING TECHNOLOGIES

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# Microelectronically Fabricated $LiCoO_2/SiO_2$/Polysilicon Power Cells

N. Ariel, G. Ceder, D.R. Sadoway, E.A. Fitzgerald
Sponsorship: CMSE-NSF MRSEC Program, Partial support from ARO

Monolithic on-chip integration was successfully demonstrated in Si CMOS technology. The enhanced development in electronics and optoelectronics technologies has increased the need for an integrative power unit that will also decrease conduction leaks, power losses, and cross talking [1]. We present a rechargeable, all-solid-state thin-film battery compatible with microelectronics technology in its materials, fabrication method, and applications.

Our cells consist of $LiCoO_2$ and polysilicon electrodes and an ultra-thin $SiO_2$ electrolyte. Solid-state battery electrolytes typically contain lithium and are 1-2-$\mu$m-thick. The only lithium-free electrolyte reported was a 0.5-2-$\mu$m-thick, porous $SiO_2$-15 at % $P_2O_5$ in a Li-battery [2]. Our cells contain an electrolyte of 7-50-nm-thick, silicon technology-compatible $SiO_2$.

The high-quality, ultra-thin oxide allows fast lithium ion transport and thereby, compensates for the film's higher resistance compared to that of common electrolytes. The cells were fabricated using microelectronics technology as described schematically in Figure 1. Utilizing CMP, we have succeeded in creating highly planar interfaces, enabling the use of an ultra-thin electronically insulating electrolyte. The polysilicon electrode is doped to improve electronic conductivity, and the $SiO_2$ is thermally grown from a 10-20-nm-thick, undoped polysilicon layer for better oxide quality. Figure 2 is a XTEM image of a cell consisting of 7-nm-thick, lithium-free $SiO_2$ electrolyte thermally grown from a 20-nm, undoped polysilicon layer. We were able to successfully charge and discharge such cells.

We have demonstrated the utilization of microelectronics processing in fabricating a $LiCoO_2/SiO_2$/poly-Si cell consisting of an ultra-thin $SiO_2$ layer as a novel lithium-free thin solid electrolyte.

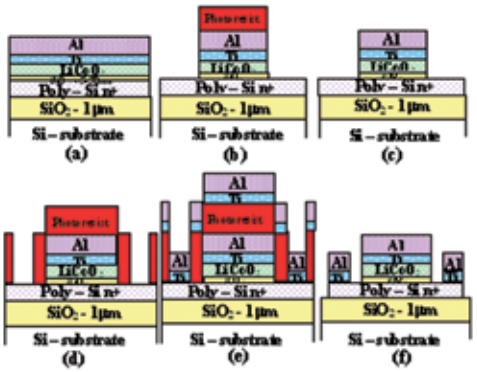


Figure 1: Cell fabrication: (a) poly deposition, CMP and oxidation, $LiCoO_2$ and cathode contact deposition; (b) photolithography and etching to poly level; (c) structure after etching; (d) photolithography to define anode contact; (e) e-beam deposition of anode contact and lift-off; and (f) photolithography and poly etch for isolation of cells.

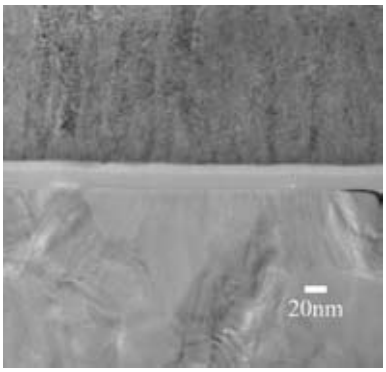


Figure 2: TEM picture showing a $LiCoO_2/SiO_2$/Poly-Si cell, which consists of a 7-nm-thick $SiO_2$ electrolyte.

## REFERENCES:

[1] Balkanski, M., *Solar Energy Materials and Solar Cells*, 62, 21 (2000).
[2] Kushida, K., Kuriyama, K. Nozaki, T., *Applied Physics Letters*, 81, 5066 (2002).

# RF Power Potential of 90 nm CMOS

J. Scholvin, J.A. del Alamo, in collaboration with D. Greenberg (IBM)
Sponsorship: IBM Faculty Award, IBM PhD Fellowship

Our research presents the first detailed comparative study of the RF power potential of the various device options offered in a state-of-the-art 90-nm CMOS foundry technology. The roadmap for integration of the RF and digital functions on a chip inevitably goes through the 90-nm node, which offers clear advantages for digital CMOS. However, implementing RF functions, particularly RF power amplification, on deeply scaled CMOS brings unique concerns about performance and reliability. The problem is the low operating voltage that this technology can support. In a modern foundry process, in addition to the nominal digital devices, it is common to offer devices with thicker gate oxides and longer gate lengths for analog and input/output (I/O) functions. This comes at the cost of increased process complexity. When considering the RF power potential of a deeply scaled CMOS technology generation, it is essential to evaluate the suitability of the entire set of devices from a performance as well as a reliability point of view.

Scaling trends of CMOS devices used for power amplifiers have traditionally followed the CMOS roadmap with a delay of 1 or 2 generations (Figure 1). Aggressive technology scaling has recently resulted in power CMOS devices with gate lengths that are shorter than the most advanced III-V RF power FETs. The benefits of scaling for power amplifiers are primarily an increase in gain that can be exploited to increase the power added efficiency (PAE).

We have characterized CMOS devices of different gate lengths and gate oxide thicknesses in a 90nm foundry process, and demonstrated excellent power performance of the nominal (thin gate oxide) 90-nm device [1]. A comparison between the nominal 90-nm device and a thick-oxide 250-nm I/O device integrated on the same wafer is shown in Figure 2. We can see that at a constant voltage of 1 V, the nominal 90-nm thin gate-oxide logic devices offer the best performance, showing a power density of 34 mW/mm and 59% PAE. Operating at 1 V might be required if the system is constrained to have a single voltage supply, which will be determined by the digital portion of the chip. However, if multiple design voltages are available to the designer, and the operating voltage can be selected, the 250-nm long thick gate-oxide I/O devices offer the highest power density and efficiency at 2.5 V.

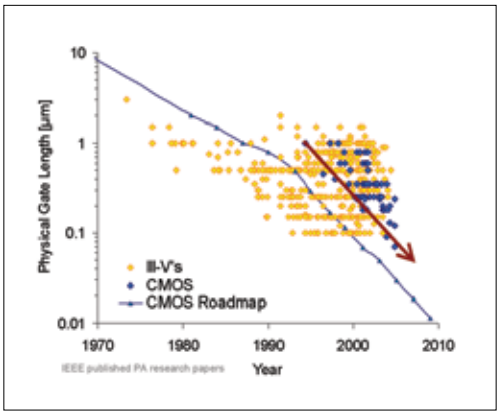


Figure 1: Physical gate length as a function of year showing the scaling trend of CMOS devices and III-V FETs used in RF power amplifiers.

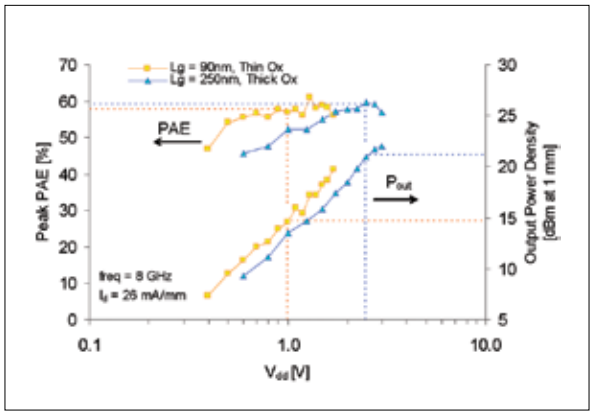


Figure 2: Power performance at 8 GHz for the nominal (thin-oxide) 90-nm device, and the thick-oxide, 250-nm I/O device, as a function of drain bias.

## REFERENCES:

[1] Scholvin, J., D.R. Greenberg, and J.A. del Alamo, "RF Power Potential of 90 nm CMOS: Device Options, Performance, and Reliability", *IEEE International Electron Devices Meeting*, 2004, pp. 455-458.

# Electron Transport in Ultra-Thin Body SOI MOSFETs

I. Lauer, D.A. Antoniadis
Sponsorship: SRC

Thin-body MOSFET geometries such as double-gate, finFET, and tri-gate devices are attractive because they can offer superior scaling properties compared to bulk and thick-body SOI devices. The electrostatics of a MOSFET limit how short a gate length can be achieved without the gate losing control over the channel. In bulk-like devices, the device designer keeps the gate in control with gate oxide scaling and doping profile design. In thin-body geometries, silicon thickness is a new, powerful scaling parameter. Much like with gate oxide scaling, the electrostatics improve (the gate has more control of the channel) with thinner films. This relationship means that the limits of scaling thin-body devices are closely tied to the limit of scaling silicon film thickness.

The limit of scaling silicon thickness, at least from a theoretical perspective, is determined by the properties of carrier transport. As the silicon film thickness is reduced into the ultra-thin regime, where the film is thinner than the bulk inversion layer thickness, quantum confinement of carriers begins to be observed. For the most part, these effects act to degrade mobility, reducing performance and making further scaling less rewarding.

This project focuses on what can be done to maintain good mobility in ultra-thin silicon films. We are examining uniaxial and biaxial strain in thin and ultra-thin films as a solution to reduced mobility caused by silicon film scaling. By building ultra-thin SOI and SSDOI (Strained Silicon Directly on Insulator) MOSFETs and measuring mobility while applying uniaxial strain, it is possible to examine the transport mechanisms of ultra-thin strained films. We find that strain does enhance mobility in SSDOI and ultra-thin films. Further work is being done to add quantitative physical insight to this observation.

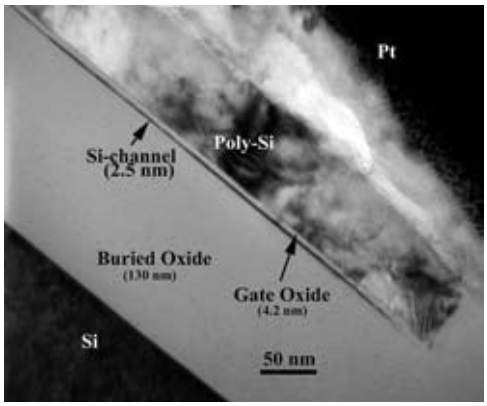


Figure 1: XTEM image of an ultra-thin silicon MOSFET. Uniform single-crystal silicon films of <5 nm can successfully be fabricated.

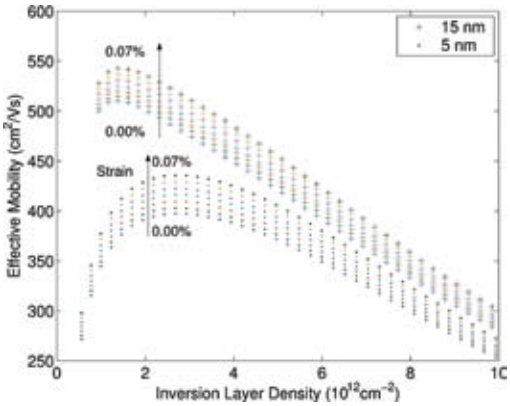


Figure 2: Electron mobility vs. inversion layer density for a thick (15 nm) and ultra-thin (5 nm) SOI film under various levels of strain. More enhancement from strain is observed in the ultra-thin film.

# Raised Source/Drain Technology for Ultra-Thin Fully Depleted SOI

L. Gomez, J.L. Hoyt, J.A. Burns, C. Chen
Sponsorship: MIT Lincoln Laboratory

Ultra-thin fully depleted (FD) SOI is an attractive alternative to bulk CMOS because of benefits that include excellent latch-up immunity, higher achievable device density, reduced junction capacitance, and suppressed short channel effects [1]. However, process integration issues (e.g. silicide formation on ultra-thin Si) and high series resistance can hamper this technology. These issues can be addressed by the selective epitaxial growth (SEG) of raised source/drain structures. The focus of the present work is to develop a process to selectively grow raised source/drain structures on FD SOI MOSFETs, and to assess the associated device performance benefits. Future work may include the use of heteroepitaxial SiGe and $Si_{1-y}C_y$ source/drain structures, which can modify channel strain (and thus enhance mobility) and may offer higher dopant solubility and hence lower series resistance.

The incorporation of high quality raised source/drains requires an effective *in-situ* cleaning procedure that rids the active surface of C and O prior to epitaxial growth, while minimizing the thermal budget. In this work, the pre-bake was optimized by varying the process parameters and using Secondary Ion Mass Spectrometry (SIMS) to determine which settings produce minimal amounts of O and C at the epi/substrate interface. An *in-situ* cleaning procedure of 2 minutes at 825ºC in hydrogen ambient was found to be an effective surface preparation prior to selective Si growth (Figure 1). Selective growth is achieved using a dichlorosilane and hydrogen chloride chemistry. Figure 2 shows the successful integration of 30 nm-thick raised source drains on a 0.1um gate-length SOI MOSFET.

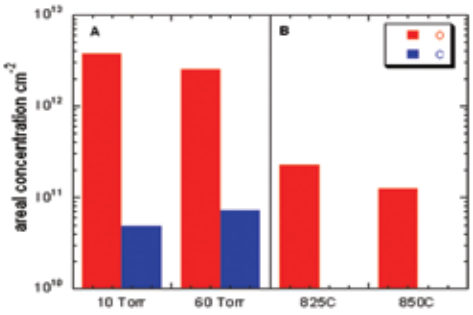


Figure 1: O and C areal density of peaks observed by SIMS at the epi/substrate interface, as a function of (A) bake pressure, and (B) bake temperature. The C content at the interface in part B remained below the SIMS detection limit at both 825ºC and 850ºC.

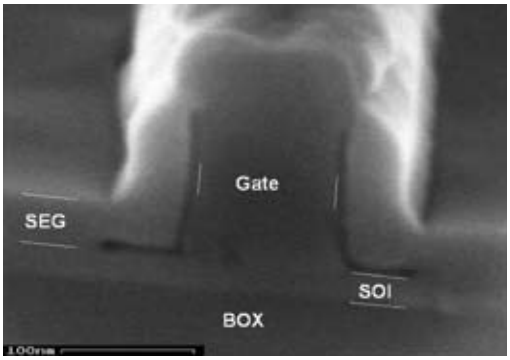


Figure 2: Cross-sectional SEM of 0.1um nFET (25nm SOI) with 30nm raised source/drain structures. Dual nitride/LTO spacers are used to isolate the source/drain SEG from the gate poly-Si.

## REFERENCES:

[1] Kuo, J.B., K. Su, CMOS VLSI Engineering Silicon-on-Insular (SOI). Norwell, Ma: Kluwer, 1998, pp. 2–9.

# Improved Hole Mobilities and Thermal Stability in a Strained-Si/Strained-$Si_{1-Y}Ge_y$/Strained-Si Heterostructure Grown on a Relaxed $Si_{1-x}Ge_x$ Buffer

S. Gupta, M.L. Lee, D.M. Isaacson, E.A. Fitzgerald
Sponsorship: MARCO MSD

A dual channel heterostructure consisting of strained-Si/strained-$Si_{1-y}Ge_y$ on a relaxed $Si_{1-x}Ge_x$ buffer ($y>x$), provides a platform with high hole mobilities ($\mu_{eff}$) that depend directly on Ge concentration in the $Si_{1-y}Ge_y$ layer. Ge out-diffusion from the strained-$Si_{1-y}Ge_y$ layer into the relaxed $Si_{1-x}Ge_x$ buffer, which occurs during high temperature processing, reduces the peak Ge concentration in the strained-$Si_{1-y}Ge_y$ layer and degrades hole $\mu_{eff}$ in these dual-channel heterostructures.

We present a tri-layer heterostructure of strained-Si/strained-$Si_{1-y}Ge_y$/strained-Si grown on a relaxed $Si_{1-x}Ge_x$ buffer. The Ge diffusion coefficient in tensilely strained Si is very low, leading to much reduced Ge out-diffusion from the strained-$Si_{1-y}Ge_y$ layer in the tri-layer heterostructure. Numerical simulations were undertaken in order to investigate the diffusion characteristics of the dual channel. A diffusion coefficient of Ge that matches well with the existing literature values over an entire range of Ge concentration was used for the diffusion simulation. A new finite difference scheme, which has much improved accuracy over the ones described in literature, has also been used for the simulations.

Numerical investigations and SIMS results establish that tri-layer heterostructures retain a higher peak Ge concentration in the strained-$Si_{1-y}Ge_y$ layer than corresponding dual-channel heterostructures after identical thermal treatment. Ring-shaped MOSFETs were fabricated on both platforms and subjected to varying processing temperatures in order to compare the extent of $\mu_{eff}$ reduction with thermal budget. Hole $\mu_{eff}$ enhancements are retained to a much greater extent in a tri-layer heterostructure after high temperature processing as compared to a dual channel heterostructure. The improved thermal stability of a tri-layer heterostructure combined with improved hole $\mu_{eff}$ provides a platform for fabricating high $\mu_{eff}$ p-MOSFETs that can be processed over higher temperatures without significant losses in hole $\mu_{eff}$.

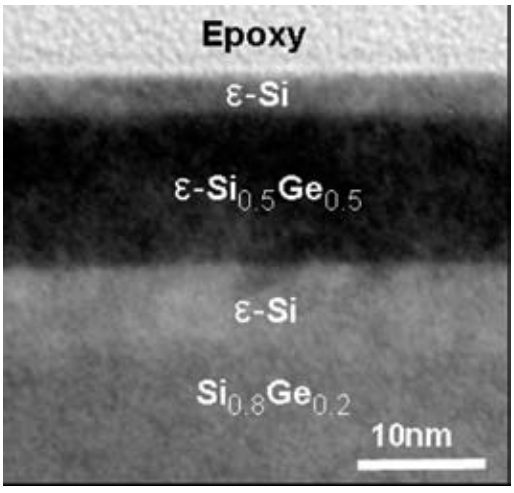


Figure 1: XTEM of a tri-layer heterostructure.

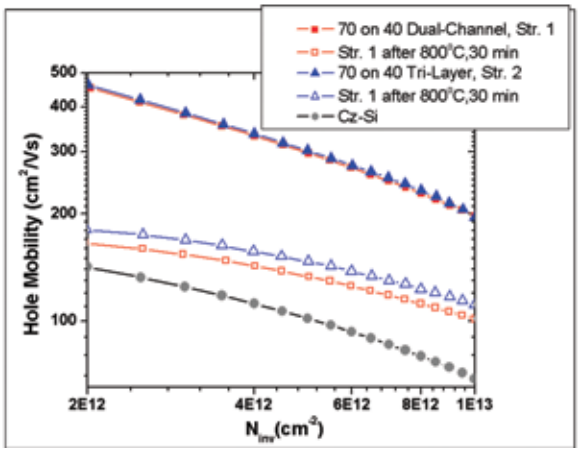


Figure 2: Mobility plot showing that higher enhancements are retained in a tri-layer heterostructure as compared to a dual -channel heterostructure, after similar high temperature processing.

# Novel High Thermal Conductivity CMOS Platforms by Wafer Bonding and Layer Transfer from Relaxed SiGe Buffer

D.M. Isaacson, A.J. Pitera, N. Ariel, S. Gupta, E.A. Fitzgerald
Sponsorship: SMA, ARO

Over the past decade, the relaxed graded SiGe buffer has enabled the development of a multitude of novel CMOS-compatible strained-Si, -SiGe, and -Ge heterostructure platforms with enhanced carrier transport properties relative to bulk Si. However, one significant drawback to the relaxed graded SiGe buffer platform is the low thermal conductance of such a structure. This results in a local temperature increase near the device channel, a condition known as the self-heating effect. This self-heating effect is especially pronounced in high-power devices and can lead to significant reductions in both mobility and drain current.

As possible solutions to this self-heating problem, we report the creation of two CMOS-compatible platforms for high-power applications: strained-silicon on silicon (SSOS) and strained-silicon on silicon-germanium on silicon (SGOS). SSOS substrate has an epitaxially-defined, strained silicon layer directly on bulk silicon wafer without an intermediate SiGe or oxide layer. SSOS is a homochemical heterojunction, i.e. a heterojunction defined by strain state only and not by an accompanying compositional change, and therefore in principle SSOS may ease metal-oxide-semiconductor (MOS) strained Si fabrication as SiGe is absent from the structure. SGOS has an epitaxially-defined SiGe layer between the strained silicon channel and the Si substrate, which is necessary to prevent excessive off-state leakage in MOS devices due to overlap of the source-drain contacts and the interfacial misfit array. Plan-view transmission electron microscopy revealed edge-type interfacial misfit dislocation arrays with an average dislocation spacing of approximately 40 nm for both structures. This spacing indicates that the strained Si layer of SSOS is fully strained and that the SiGe layer of SGOS is fully relaxed. Complete relaxation of the intermediate SiGe layer in SGOS was confirmed by Raman spectroscopy, and since this layer is thin (<100nm), its inclusion is not expected to detrimentally affect the overall thermal conductivity of the structure.

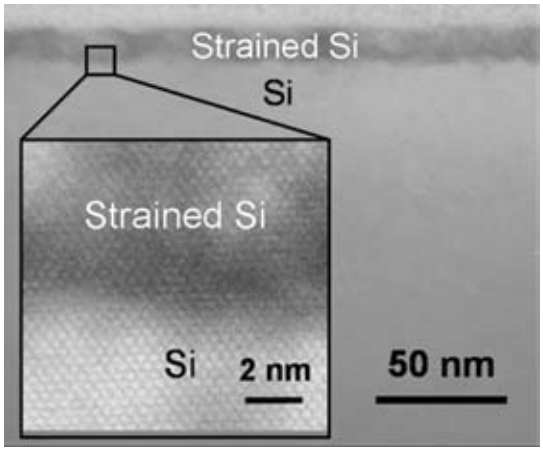


Figure 1: Cross-sectional transmission electron microscopy image of the strained-Si on Si (SSOS) heterostructure.

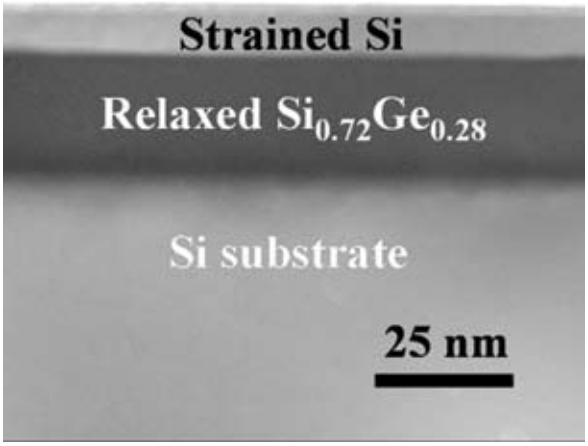


Figure 2: Cross-sectional transmission electron microscopy image of the strained-Si on SiGe on Si (SGOS) heterostructure .

# Epitaxial Growth of SiGe Buffers on Si (111) and (110)

M.L. Lee, E.A. Fitzgerald, D.A. Antoniadis
Sponsorship: MARCO MSD

The band structure that a carrier experiences in a MOSFET inversion layer depends strongly on the crystallographic orientation of the substrate surface. Surface orientation also influences the relaxation and dislocation morphology of mismatched epitaxial semiconductor films. Recently, the emergence of local and global strain techniques to enhance VLSI circuit performance has brought about renewed interest in the influence of surface orientation on $\mu_{eff}$, particularly Si(110) surfaces for *p*-FETs, and Ge(111) and (110) surfaces for ultra-scaled *n*-FETs [1]. The ability to control defect densities in SiGe buffers grown on arbitrary substrate orientations would allow the coupled effects of surface orientation and strain on $\mu_{eff}$ to be studied in greater detail.

Most dislocations in diamond cubic semiconductors are 60° a/2[101] total dislocations that are slightly dissociated into 90° and 30° Shockley partials. For compressive films on (111) and (110) substrates, the 90° a/6[211] dislocation leads the 30° partial and also experiences a larger resolved shear stress. Therefore, 60° dislocations in compressive films grown on (111) and (110) substrates can dissociate, resulting in stacking fault growth.

In PVTEM, we have observed high densities of dislocation pileups in SiGe layers grown on both (111) (Figure 1) and (110) substrate orientations. Cross-sectional TEM images and diffraction patterns indicate that these pileups consist of 90° a/6[211] partial dislocations that nucleate at the surface and glide to the hetero-interface on neighboring (111) glide planes, resulting in the formation of microtwins (Figure 2).

In general, low-mismatch SiGe layers grown on Si (111) and (110) exhibit dislocation densities several orders of magnitude greater than those grown on (001). Since relaxation processes on these substrate orientations tend to involve the glide of partial dislocations and the formation of stacking faults, achieving high quality SiGe buffer layers on Si (111) and (110) is intrinsically more challenging than on (001).

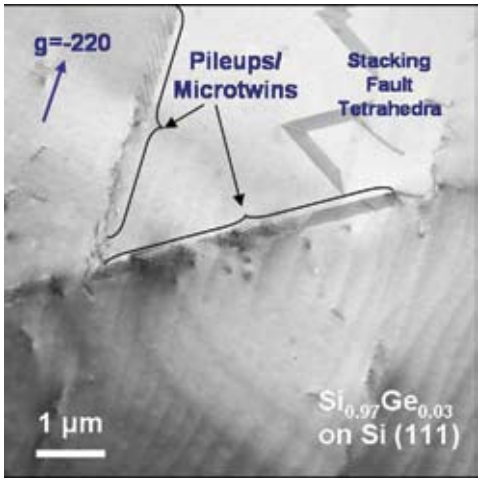


Figure 1: PVTEM of 1 µm thick $Si_{0.97}Ge_{0.03}$ film on Si (111) showing dislocation pileups and stacking fault tetrahedra.

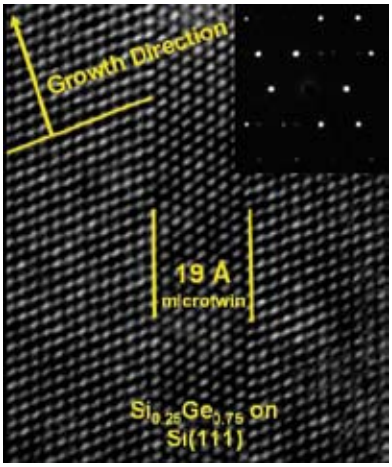


Figure 2: XVTEM of microtwin in $Si_{0.75}Ge_{0.25}$ grown on Si (111). *Inset*- Selected area diffraction pattern showing twin spots.

## REFERENCES:

[1] Takagi, S., "Re-examination of Subband Structure Engineering in Ultra-Short Channel MOSFETs under Ballistic Carrier Transport," presented at Symposium on VLSI Technology Digest of Technical Papers, 2003.

# Interdiffusion in Strained Si/Strained SiGe Heterostructure Devices

G. Xia, J.L. Hoyt

In the past decade, SiGe-based strain and bandgap engineering have received increasing attention for CMOS applications. Carrier transport is enhanced by applying strain in the Si channel, or by the use of strained SiGe as the p-MOSFET channel material, as in dual-channel and heterostructure-on-insulator (HOI) MOSFETs. One issue for these structures is interdiffusion at the strained Si/strained SiGe interface during processing, which degrades device performance by reducing strain and carrier confinement and increasing alloy scattering. To date, research on Ge diffusion has been focused on Ge self-diffusion in $Si_{1-x}Ge_x$ [1] and interdiffusion in compressively strained SiGe superlattices with low Ge fractions ($x < 0.25$) grown on Si [2]. Basic understanding of interdiffusion, such as Ge fraction, strain, and temperature dependence, and the influence of point defects generated during oxidation, nitridation, and other processes is inadequate. In addition, little data is available for SiGe interdiffusion in device structures, such as Strained Si/Strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ with Ge content $y>0.3$.

In this work, interdiffusion is studied in Strained Si/Strained $Si_{1-y}Ge_y$/relaxed $Si_{1-x}Ge_x$ structures under various point defect injection conditions. In one experiment, Boltzmann-Matano analysis is used to obtain SiGe interdiffusivity experimentally. With transient diffusion taken into account, a TSuprem4 interdiffusion model is set up based on the interdiffusivity obtained. This model will be tested by application to various annealing conditions, especially to rapid thermal processing (RTP) of dual channel and HOI structures. Figure 1 shows examples of Ge profiles used for Boltzmann-Matano analysis, for Ge fraction up to 0.4. The interdiffusivity model is based on the interdiffusion coefficients obtained from Boltzmann-Matano analysis (Figure 2), which has a similar form to the model used in [2] for compressive SiGe at lower Ge fractions.

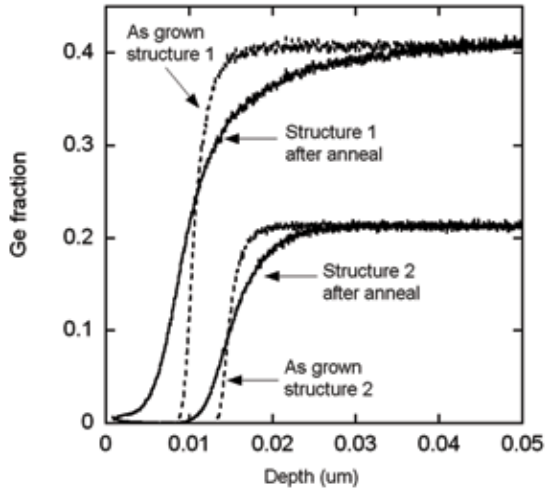


Figure 1: Ge profiles measured by SIMS for Boltzmann-Matano analysis. Both samples are annealed at 920C for 60min in nitrogen.

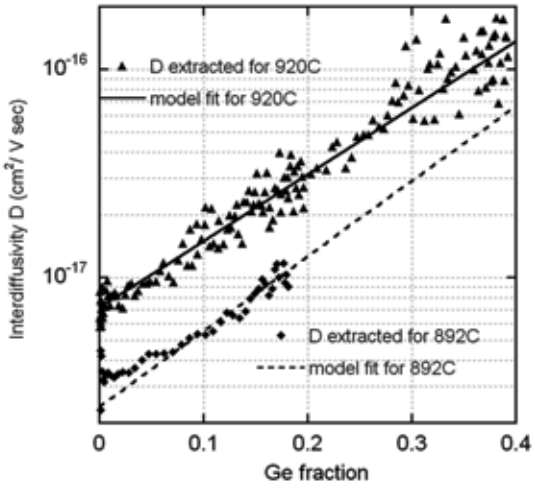


Figure 2: SiGe interdiffusivity (D) extracted from Ge profiles similar to those in Figure 1 (symbols), and model fit (lines) at two different temperatures.

## REFERENCES:

[1] Aubertine, D.B., P. C. McIntyre, "Influence of Ge Concentration and Compressive Biaxial Stress on Interdiffusion in Si-Rich SiGe Alloy Heterostructures," *J. Appl. Phys.,* vol 97, n 1, pp. 013531-1-013531-10, January 2005.

[2] Zangenberg, N.R., J. L. Hansen, J. Fage-Pedersen, A. N. Larsen, "Ge Self-Diffusion in Epitaxial $Si_{1-x}Ge_x$ Layers," *Physical Review Letters*, v 87, pp. 125901-1-125901-4, September 2001.

# Extraction of Band Offsets in Strained Si/Strained $Si_{1-Y}Ge_y$ on Relaxed $Si_{1-X}Ge_x$ Dual-Channel Enhanced Mobility Structures

C. Ní Chléirigh, C. Jungemann, J. Jung, O. Olubuyide, J.L. Hoyt
Sponsorship: MARCO MSD, SRC, Applied Materials

In this work, for the first time, the valence band offset, $\Delta E_V$, between strained Si and strained $Si_{1-y}Ge_y$ on relaxed $Si_{1-x}Ge_x$, has been measured using a combination of experimentation and modeling. Such structures have been shown to offer large mobility enhancements for both electrons and holes, and knowledge of the band parameters is critical in order to optimize and predict device behavior [1-3]. The positions of the conduction band edge in the strained Si and the valence band edge in the strained $Si_{1-y}Ge_y$ significantly affect the effective bandgap of the structure and can be used to tune the threshold voltage of both n- and p-MOSFETs for use with a single workfunction metal gate [4]. Theoretical predictions of these band parameters are uncertain by ±100 meV [5]. P-type metal-oxide-semiconductor (MOS) capacitors were fabricated on epitaxial structures containing strained $Si_{1-y}Ge_y$ layers ($0.4 < y < 0.8$) grown on relaxed $Si_{1-x}Ge_x$ layers ($0.2 < x < 0.4$). DEV was extracted by fitting simulated results to the experimental capacitance-voltage (C-V) characteristics of the MOS capacitors (Figures 1 and 2). The impact of the valence band edge density of states, $N_V$, on the extraction of $\Delta E_V$ is investigated. The effect of these band parameters on threshold voltage and subthreshold slope of a dual channel p-MOSFET is demonstrated using simulations.

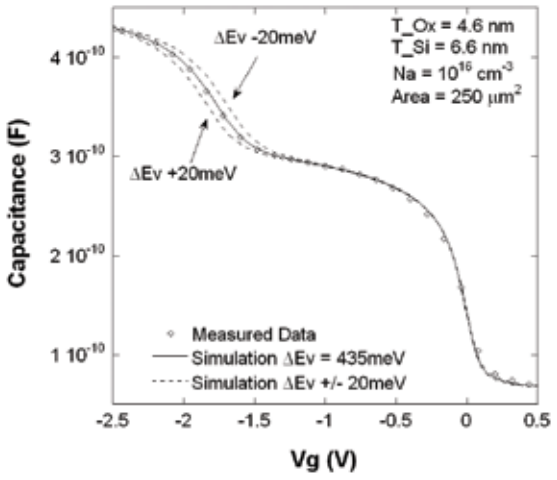


Figure 1: $\Delta E_V$ extraction and sensitivity for strained Si, strained $Si_{0.4}Ge_{0.6}$ on a relaxed $Si_{0.7}Ge_{0.3}$ substrate. Measured data with simulation of $\Delta E_V = 435$meV ± 20meV.

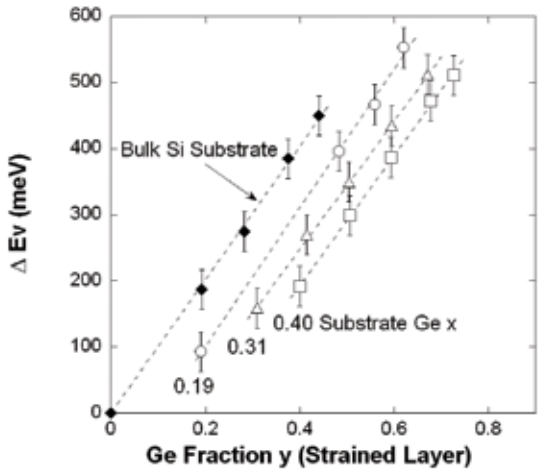


Figure 2: Extracted $\Delta E_V$ for strained Si on strained $Si_{1-y}Ge_y$ on various relaxed $Si_{1-x}Ge_x$ substrates.

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# Electron and Hole Mobility in Thin-Body Strained Si/Strained SiGe/Strained Si Heterostructures on Insulator

I. Åberg, J.L. Hoyt
Sponsorship: MARCO MSD, SRC, Applied Materials

Geometric scaling of MOSFETs can no longer provide all the current drive enhancements necessary to maintain historic performance gains. Channel strain and novel materials may provide additional transport improvements. At the same time, fully depleted or double gate technologies may be required to maintain electrostatic integrity in deeply scaled MOSFETs. To address these issues, fully depleted MOSFETs were fabricated on strained Si/strained SiGe (46% Ge)/strained Si heterostructures on insulator (HOI), demonstrating both high electron and hole mobility enhancements while maintaining excellent subthreshold swing of 66-70 mV/dec. Subthreshold characteristics are improved compared to bulk dual-channel MOSFETs [1]. The total thickness of the heterostructure on insulator is less than 25 nm. At an inversion charge density of $1.5x10^{13}$ $cm^{-2}$, mobility enhancements of 90% and 107% are obtained for electrons and holes respectively. The tri-layer heterostructure on insulator was fabricated by using a bond and etch-back technique [2]. Electron mobilities are enhanced by a factor of 1.8-2X over regular SOI (Figure 1) as in the case of strained Si directly on insulator, while hole mobilities are enhanced by ~2X even at high inversion charge densities depending on the Ge concentration of the buried layer, strain level, and cap thickness design (Figure 2) [2]. For example, for a cap thickness of 4 nm, hole mobility improves when the Ge concentration of the buried SiGe channel increases from 35% to 46%.

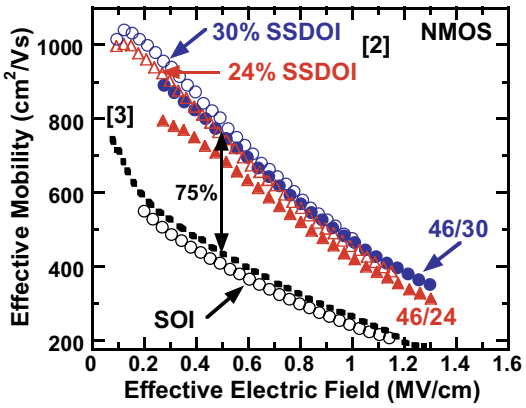


Figure 1: NMOS effective mobility as a function of Eeff. $\mu_{eff}=L/W*I_D/(Q_{inv}V_{DS})$ was extracted by integration of $C_{GC}$, measuring $I_D$ at an applied $V_{DS}$=50mV. The universal mobility is indicated [3].

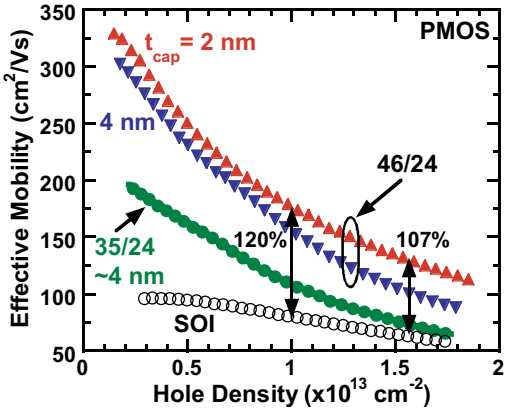


Figure 2: PMOS effective mobility as a function of $N_{inv}$. The enhancement compared to the SOI control at $N_{inv}$= $1x10^{13}$ $cm^{-2}$ is 120%. As the Ge content of the buried channel is increased (keeping the cap thickness constant), the mobility is increased.

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# Germanium-on-Insulator Fabrication by Hydrogen-Induced Layer Transfer

J. Hennessy, D.A. Antoniadis
Sponsorship: MARCO MSD

Germanium is considered a promising material for high performance CMOS devices because it possesses higher bulk electron and hole mobility than Si. Similarly, the on-insulator structure is also a good candidate for improved device performance due to the electrostatic benefits it holds over bulk technologies. This project is meant to combine both advantages in the fabrication of Germanium-on-Insulator (GeOI) substrates.

The initial goal of this work is to develop a process to transfer a high quality Ge layer to a less expensive and more readily available Si handle wafer. This goal is accomplished by first implanting a bulk Ge transfer wafer with a high dose of hydrogen, and then direct-bonding the Ge wafer to an oxidized Si handle wafer. As the bonded wafer pair is annealed, the activation of the implanted hydrogen leads to the formation of micro-cracks near the peak of the implant and the eventual exfoliation of a thin Ge layer from the transfer wafer (Figure 1). By incorporating an epitaxial etch-stop layer in the transfer wafer, the implant-damaged Ge can be selectively removed by wet etching. This technique also allows for arbitrarily thin GeOI because the device layer is defined epitaxially and not by a polishing or etching step.

The most challenging aspect of this approach is the mismatch of the thermal coefficients of expansion between Ge and Si. A typical hydrogen activation anneal is performed at 300-400°C for Si applications. At this temperature, the Ge/Si bonded pair will break due to the great increase in thermal stress. For the fabrication of GeOI, it is necessary to reduce the temperature at which layer transfer will occur. One approach being investigated is the use of a second SiGe epitaxial layer as a gettering layer for the implanted hydrogen (Figure 2). This gettering layer is seen to reduce the time required for layer exfoliation at a given annealing temperature. Future work on this project will include device fabrication and analysis on partially depleted and fully depleted GeOI substrates.

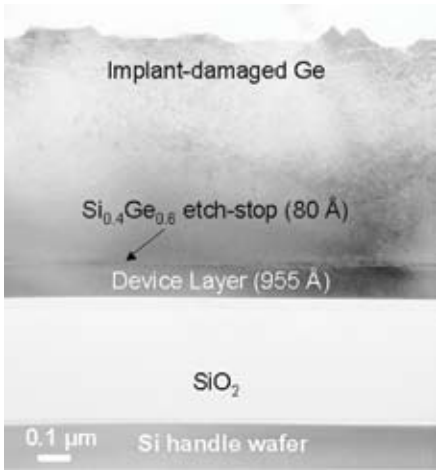


Figure 1: Cross-sectional TEM of GeOI structure immediately after layer transfer.

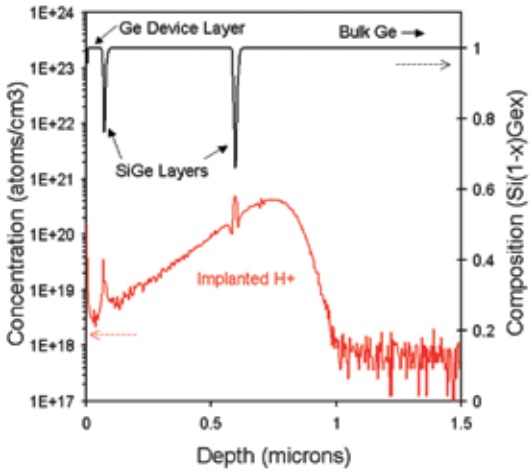


Figure 2: SIMS analysis of a hydrogen-implanted transfer wafer with a double etch-stop structure.

# RTP Growth of Germanium Oxynitride for MOSFET Fabrication

A. Khakifirooz, A. Ritenour, D.A. Antoniadis
Sponsorship: MARCO MSD

Germanium channel MOSFETs are considered one of the promising options for high performance CMOS technology because of the high electron and hole mobility, as well as high ballistic carrier injection velocity in germanium. One of the most important challenges in integrating the Ge MOSFETs is the formation of high quality gate dielectrics on the Ge surface. Several attempts have been made in recent years to deposit high-k dielectrics on Ge [1, 2]. However, by far the highest mobility reported for Ge MOSFETs is obtained using a thermally grown germanium oxynitride [3]. A rapid thermal processing (RTP) version of such processes is of interest for providing realistic EOT values for futuristic devices, while offering the possibility of obtaining high carrier mobility values similar to those reported earlier for Ge MOSFETs with an oxynitride dielectric grown in a furnace. Germanium oxynitride gate dielectrics are grown on 6" (100) n-type germanium wafers as well as relaxed p-type Ge layers epitaxially grown on silicon. A special "RCA-equivalent" cleaning process has been developed to minimize Ge loss during the cleaning step and to give reasonably smooth surface ($R_a$ ~ 0.25 nm). Oxidation is performed in an RTP chamber at 550°C for 30-60 s and in oxygen, followed by a nitridation step at 600°C for 60-300 s in ammonia. From spectroscopic ellipsometry the thickness of the oxynitride layer is determined to be 50±5 Å. Upon nitridation, the refraction index of the film measured at 600 nm is increased from 1.3 to 1.7, indicating the oxynitride formation. From CV measurements the effective electrical oxide thickness is about 30 Å, corresponding to a dielectric constant of about 6.5. MOS capacitors made by depositing Al gates on as grown oxynitride dielectrics show a kink in the CV characteristics measured at lower frequencies. A forming gas annealing step at 400°C effectively removes this kink and reduces the density of surface states. The midgap $D_{it}$ extracted from the conductance method is roughly $8\times10^{11}$ $cm^{-2}$. PMOS transistors were fabricated with a TiN metal gate and show a peak effective mobility of 280 $cm^2$/V.s which corresponds to 40% enhancement over p-channel Si MOSFETs.

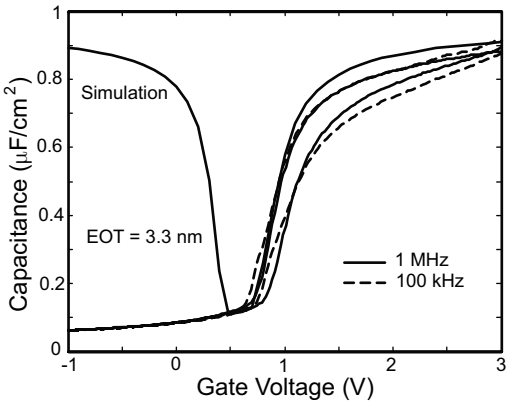


Figure 1: CV characteristics of the MOS capacitor fabricated using RTP Ge oxynitride and after a post-metal annealing in forming gas.

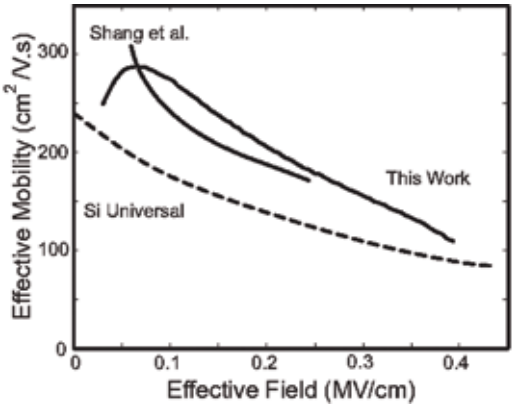


Figure 2: Effective hole mobility in the Ge MOSFETs. An enhancement of about 40% is observed compared to silicon.

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# Bulk Germanium MOSFETs Using High-K Gate Dielectrics

A. Ritenour, R.Z. Lei, D.A. Antoniadis
Sponsorship: MARCO MSD

The advent of high-k gate dielectrics provides a new opportunity to consider semiconductors other than silicon for future ultra-scaled MOSFETs. Germanium has started to receive attention because it simultaneously offers significant enhancements in bulk carrier mobility relative to silicon; however, the inherent instability of germanium oxide makes interface engineering particularly challenging. Advanced techniques such as molecular beam deposition (MBD) and atomic layer deposition (ALD) are being explored as options for gate stack deposition. Figure 1 shows the transfer characteristics for a germanium p-MOSFET with an MBD GeON-HfO2-TaN gate stack. Figure 2 shows the extracted hole mobility for this device. MBD gate stack deposition was performed by A. Dimoulas at the NCSR in Greece.

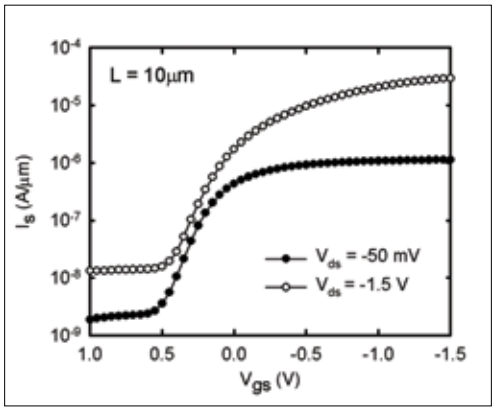


Figure 1: Typical as-measured $I_s$-$V_g$ characteristics for bulk Ge p-MOSFETs with MBD GeON-HfO2-TaN gate stack.

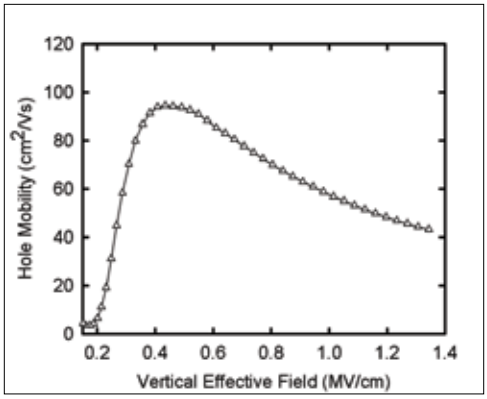


Figure 2: Extracted hole mobility for Ge MBD p-MOSFET.

# Modeling and Simulation of Advanced Transistors with Novel Channel Materials

O.M. Nayfeh, D.A. Antoniadis
Sponsorship: MARCO MSD, SRC

Recent experimental results [1] have demonstrated significant mobility enhancement in transistors such as the dual channel heterostructure-on-insulator (HOI). Germanium is optimally incorporated in the channel to provide increase in mobility. The increase in mobility in an HOI structure is due to Germanium's bulk nature, and also from strain effects due to the lattice mismatch between silicon and germanium. In this work, we examine by modeling and simulation, electrostatics and transport of such devices, in order to understand the physical mechanisms that contribute to enhanced mobility as compared to Silicon-On-Insulator counterparts. Moreover, we determine the performance limits of such channel materials for integration in deep sub 45 nm transistors.

Modeling of such advanced devices requires the determination of key electrostatic parameters; either theoretically, or from measurements of experimental structures. These parameters are affected by strain, quantum-mechanical, and high-field effects. Figure 1 shows the Hole density in an HOI structure at a cut through the center of the channel. The silicon cap thickness is 7 nm and the SiGe layer is ~12.5nm. The gate potential is –1.7 V. Shown is the solution from a Schrödinger/Poisson calculation, and also from the calibration of the Density-Gradient quantum mechanical correction model. Figure 2 shows the respective Gate-Capacitance vs. Gate-Voltage curves. Both plots show good agreement between the two models after calibration.

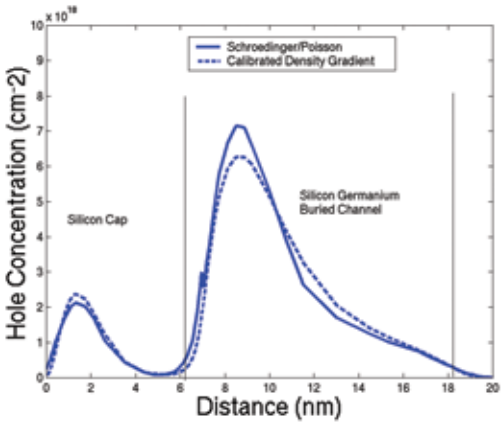


Figure 1: Cut of simulated Hole density through the center of the channel of an HOI device. Shown are the Schrödinger/Poisson calculation, and also the result from the calibration of the Density Gradient quantum mechanical correction model. The gate potential is –1.7 V.

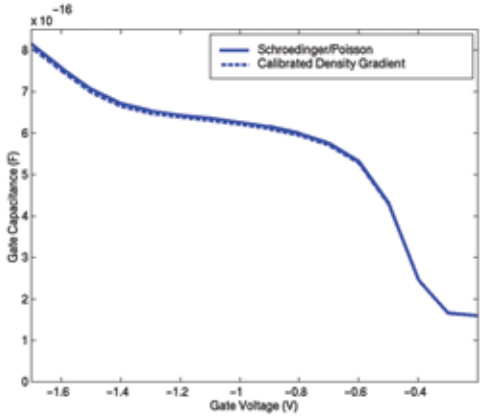


Figure 2: Respective Capacitance-Voltage curves of the device in Figure-1. Notice the hump in the curves due to population of the Silicon cap at high gate fields. Calibration of the DG provides good agreement with the Schrödinger/Poisson calculation.

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# An Equivalent Circuit Model of a Faraday Cage for Substrate Noise Isolation

J.H. Wu, J.A. del Alamo
Sponsorship: Applied Materials Fellowship

Substrate crosstalk between digital, analog, and RF blocks is a major problem for System-on-Chip applications. A promising approach that is both compact and effective up to millimeter-wave frequencies is a Faraday cage embedded in the substrate that surrounds a noisy or sensitive circuit. This Faraday cage uses through-wafer vias with solid copper cores that are shorted at the top and to the backside ground plane (Figure1a) [1]. These Faraday cages significantly improved isolation by 41 dB at 1 GHz, 30 dB at 10 GHz, and 16 dB at 50 GHz with respect to a reference at a distance of 100 μm [1]. In order to better understand the exceptional performance of this Faraday cage, we have developed a physics-based equivalent circuit model [2].

We developed a model for the Faraday cage (Figure 1b) starting from the simple substrate model in [3]. The lumped elements $R_1$ and $C_1$ represent the substrate between the transmitter and receiver pads. $R_3$ and $C_3$ represent the substrate from the surface to the backside of the wafer. We modified the substrate model in [3] to include the effect of the Faraday cage by exposing a node that corresponds to the center of the substrate between the transmitter and receiver pads and shunting this center node to ground. The entire effect of the Faraday cage is captured by lumped elements $R_v$ and $L_v$. The smaller $R_v$ and $L_v$ are, the more effective the shunting of the substrate between the transmitter and receiver, resulting in a reduction in crosstalk.

The equivalent circuit model was simulated using Agilent ADS. Figure 2 shows $S_{21}$ measured and simulation data for the reference and Faraday cage structures. The simulation data matches the experimental data well into the millimeter-wave regime. This model will be useful in evaluating the effectiveness of Faraday cages in circuits.

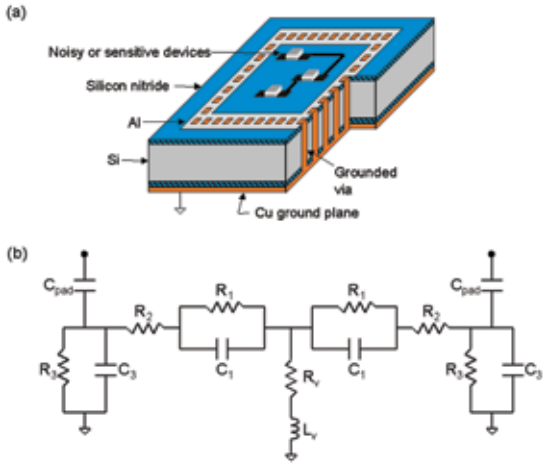


Figure 1: (a) Schematic diagram of a Faraday cage constructed using through-wafer vias. (b) Equivalent circuit model of the Faraday cage.

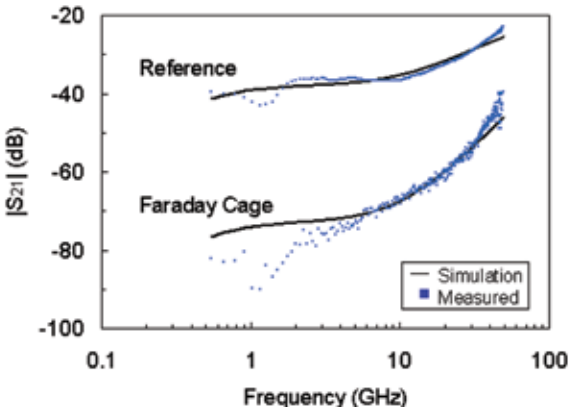


Figure 2: $S_{21}$ of the reference and Faraday cage at 100-μm pad separation distance.

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# Approaching the InP Lattice Constant on GaAs

N.J. Quitoriano, E.A. Fitzgerald
Sponsorship: Walsin Lihwa

Integrating different materials onto a Si platform brings new functionality to Si. InP on Si could allow the integration of optical and electronic (e.g. CMOS) devices. By growing high-quality GaAs on Si, our group has been able to demonstrate a GaAs laser grown on Si. Our research goal is to expand the lattice constant beyond GaAs and grow high-quality InP on GaAs. Having explored many materials systems and methods (e.g. InGaAs, InGaP, and InGaAlAs), to date, we have grown low dislocation-density $In_{(0.43)}Al_{(0.57)}As$ on GaAs with a dislocation-density of 1.4E6/cm$^2$, more than an order-of-magnitude less dislocations than typical commercial metamorphic buffers. After achieving high-quality InP on GaAs, we will work to grow InP on Si. Bringing low-defect density InP onto Si may bring high-speed InP based devices into new markets because the processing and material cost for a given area will be drastically reduced and allow for high-frequency and/or low-power operation.

Figure 1: Plan-view TEM of $In_{(0.43)}Al_{(0.57)}As$ on GaAs with a dislocation density of 1.4E6/cm$^2$.

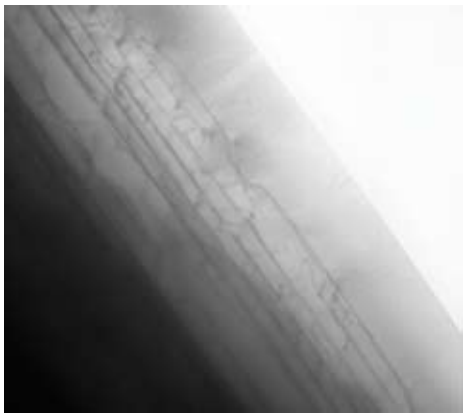

Figure 2: Cross section of $In_{(0.43)}Al_{(0.57)}As$ on GaAs.

# The Impact of Recess Length on the RF Power Performance of GaAs PHEMTs

M.F. Wong, J.A. del Alamo, A. Inoue, T. Hisaka, K. Hayashi
Sponsorship: Mitsubishi Electric

Due to their excellent performance, reasonable cost, and relative technological maturity, AlGaAs/InGaAs Pseudomorphic High Electron Mobility Transistors (PHEMTs) constitute an attractive choice for RF power applications. Theoretically, increasing the gate-to-drain recess length ($L_{RD}$) should lead to an increase in breakdown voltage, which ought to allow the selection of a higher drain voltage bias point and subsequently yield higher output power. However, we have experimentally found that not to be the case. In fact, beyond a certain value, we have observed that further increasing $L_{RD}$ results in a decrease in saturated output power and peak power-added efficiency (PAE), (Figure 1). In addition, we have observed a decrease in output power and peak PAE with increasing frequency that cannot be accounted for by existing large signal models.

In our investigation into the origins of this anomalous behavior, we have identified two contributing explanations. First, a comparison of the output characteristics reveals an increase in $V_{DS,SAT}$ when $L_{RD}$ is increased; this trend reduces the peak-to-peak voltage swing possible during RF operation and adversely affects the output power that can be delivered from the device.

Secondly, we have observed a reduction in both gain and short-circuit current-gain frequency ($f_T$) with increasing $L_{RD}$. To gain further insight into the reduction of $f_T$, we have performed a delay time analysis and extracted the drain delay, which is associated with the electron drift through the depletion region on the drain side of the device [1]. Figure 2 shows a plot of the intrinsic delay versus drain voltage, where the minimum intrinsic delay is the same for all four devices with different $L_{RD}$ and represents the transit of electrons in the gate region. As the drain voltage is increased, the depletion region widens toward the drain, contributing an additional delay associated with the electron drift through this region and hence, increasing the intrinsic delay. This drain delay becomes longer as $L_{RD}$ is increased and appears to be a significant limitation at high frequency, large drain voltage operation.

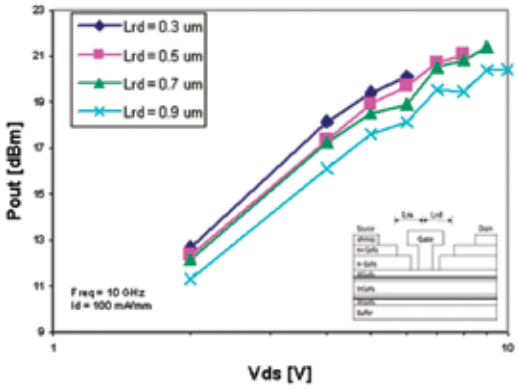


Figure 1: Saturated output power versus drain voltage for different $L_{rd}$ devices. Inset: Schematic cross-section of the GaAs PHEMT under study.

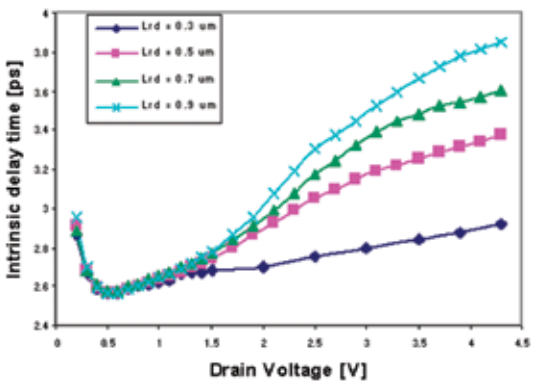


Figure 2: Intrinsic delay time of GaAs PHEMTs versus drain voltage for different $L_{rd}$ devices. Vgs was chosen to correspond with the value with the lowest intrinsic delay time.

## REFERENCES:

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# Electrically-Induced Changes in Threshold Voltage and Source Resistance in RF Power GaAs PHEMTs

A.A. Villanueva, J.A. del Alamo
Sponsorship: Mitsubishi Electric

GaAs Pseudomorphic High-Electron Mobility Transistors (PHEMTs) have great potential for RF power applications. A major issue with these devices is electrical reliability–the gradual degradation of certain electrical characteristics that occur under prolonged high-voltage biasing. The degradation of the extrinsic drain (observed via an increase in the drain resistance $R_D$ and a decrease in the maximum drain current $I_{max}$) is usually of primary concern; however, under high-bias stress, significant shifts in the threshold voltage $V_T$ and in the source resistance $R_S$ are also observed. Since such changes affect the long-term electrical performance of the device, it is important to understand the underlying mechanisms behind these changes.

In our study, experimental RF power PHEMTs were electrically stressed using a bias-stressing scheme that kept the impact-ionization rate constant [1]. During stressing, the devices were characterized at frequent intervals. In our experiments, we observed negative shifts in $V_T$ (Figure 1) and decreases in $R_S$ (Figure 2), which were both accelerated with increasing temperature. Both the changes in $V_T$ and $R_S$ tended to saturate with stressing and could be modeled well by an exponential fit. Additional tests showed that the $V_T$ shift was recoverable with unbiased storage at room temperature. This all makes $\Delta V_T$ consistent with a trapped electron recombination mechanism occurring under the gate, as previously identified in [2]. In this mechanism, the trapped electrons recombine with holes generated from impact ionization on the drain side of the device. As for $R_S$, through additional experiments on simple test structures, we were able to attribute the decrease in $R_S$ to an increase in sheet carrier concentration ($n_s$) on the source. This suggests the presence of a similar electron-trapping and recombination mechanism on the source side. All these findings provide a better understanding of the cause for these device instabilities and thus, should be instrumental in developing effective solutions to this problem.

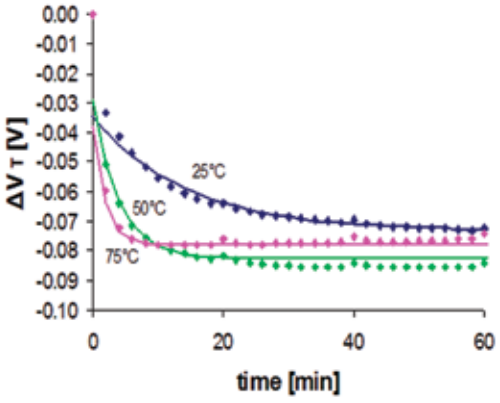


Figure 1: Time evolution of the threshold voltage shift of GaAs PHEMTs stressed at $I_D$=400 mA/mm, and $V_{DG0}+V_T$ = 6.0 V, at 25, 50, and 75°C in $N_2$. Solid lines show exponential fits to data.

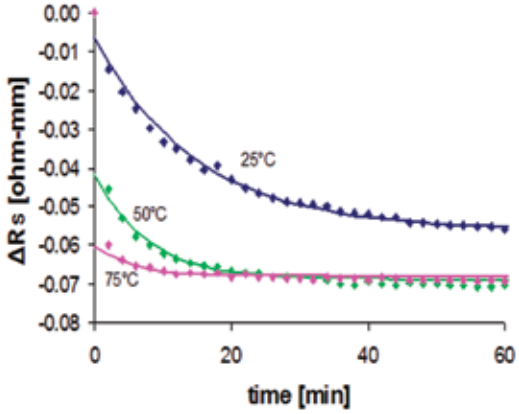


Figure 2: Time evolution of the source resistance decrease of GaAs PHEMTs stressed at $I_D$=400 mA/mm, and $V_{DG0}+V_T$ = 6.0 V, at 25, 50, and 75°C in $N_2$. Solid lines show exponential fits to data.

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# InP-Based HEMTs for Large Scale Logic Applications

N. Waldron, J.A. del Alamo
Sponsorship: MARCO MSD

InP High Electron Mobility Transistors (HEMTs) have been shown to have the best intrinsic frequency performance of all the families of semiconductor devices (Figure 1). However, this superior intrinsic performance has not translated into the best circuit or system performance. Much of the reason for this is that these devices have been developed for millimeter wave rather than digital applications, resulting in a large extrinsic footprint and high parasitics. In contrast Si CMOS, which dominates the digital IC market, has benefited from aggressive gate scaling coupled with close attention to extrinsics and packing density. However, CMOS even now is approaching the end of the scaling roadmap, and more and more radical changes in the design of logic technology can be expected. Considering the current trend towards heterogeneous integration of various material systems, e.g. SiGe on Si, InAlAs on GaAs, the time perhaps has come to investigate III-V FETs as a post-CMOS logic technology. Of all III-V systems, the InAlAs system closely lattice-matched to InP is the most promising, and that is the one we are investigating in this project.

In order to realize the potential of InP-based HEMTs in large scale digital circuits, it is necessary to address the problems of the extrinsic resistances and capacitances that the non self-aligned design and large footprint bring about. To this end, we have designed a device architecture that incorporates a novel shallow trench isolation and self-aligned gate scheme (Figure 2). The BCB shallow trench design provides a low capacitive isolation scheme while maintaining a planar surface. The self-aligned gate process reduces the parasitic source and drain resistances with the added benefit of reducing the device footprint. The non-alloyed tungsten ohmic contacts allow for well-defined contact geometries. The process architecture offers the promise of a reliable, highly manufacturable process needed to realize the complex circuits required for large scale digital applications.

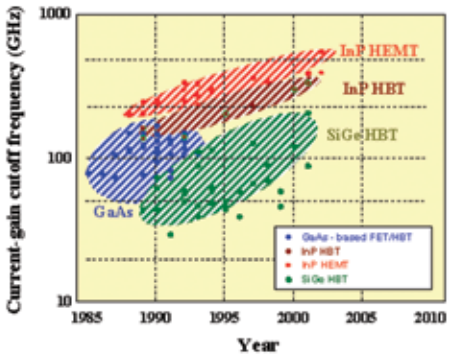


Figure 1: $f_T$ of InP HEMTs compared to other III-V devices and SiGe HBTs. InP HEMTs have the best intrinsic performance. [Courtesy of T.Enoki, NTT].

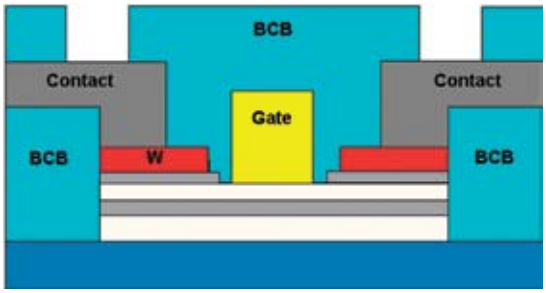


Figure 2: Cross section of the proposed new device architecture. Features include: BCB planar isolation, a self-aligned gate, and non-alloyed ohmic contacts. The architecture has the flexibility of being compatible with a wide variety of heterostructure designs.

# Concepts and Devices for Micro-Scale Thermo-Photovoltaic Energy Conversion

H.K.H. Choy, C.G. Fonstad, Jr., in collaboration with R. Dimatteo (Charles Stark Draper Laboratory)
Sponsorship: Charles Stark Draper Laboratory

The first order proximity enhancement of thermo-photovoltaic (TPV) energy conversion that we and the C. S. Draper Laboratory (CSDL) demonstrated for the first time several years ago [1, 2] leads to a dramatic and important increase in energy conversion rate, but only a modest increase in the efficiency of the conversion process. The present challenge is to use the micro-scale geometry (in which the hot and cold surfaces are in extreme proximity) to increase the efficiency of TPV as significantly as we have increased the conversion rate.

Our work supports the CSDL effort on micro-scale thermo-photovoltaic (MTPV) electrical power sources. We have provided InAs-based MTPV cells to the CSDL effort, we have analyzed the impact of the enhancement effect on TPV cell performance, and we have evaluated more sophisticated, quantum-effect-based phenomenon that can be used to enhance significantly the energy selectivity of the energy transfer, and thereby dramatically increase the efficiency of the thermal to electrical energy conversion. We have most recently also begun work on dot-junction, back-side illuminated solar cells, and in the past year we designed an original InGaAlAs-on-InP heterostructure, shown in Figure 1, suitable for fabricating high performance dot-junction, back-side illuminated solar cells. The final n+ InGaAs layer is the n-side of the junction and a low resistance contact layer. The InGaAlAs layers shield the minority carriers created in the wide, p-type InGaAs light absorbing layer from surface recombination; the Al composition is graded to eliminate any barrier to electron flow from the absorbing layer to the n-side of the junction. The lowest p+ InGaAs layer reduces resistance as carriers flow laterally to ohmic contacts made to the p-side of the junction. The first sample of this heterostructure has been grown and has been given to CSDL researchers for device fabrication and testing.

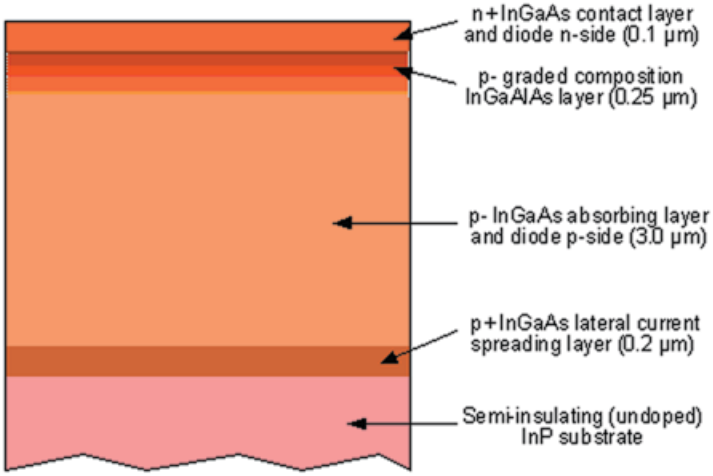


Figure 1: The layer structure for dot-junction, back-illuminated TPV and MTPV cells

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# Temporal and Spatial Current Stability of the Smart Field Emission Arrays

C.-Y. Hong, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

Field emission can be described as two sequential processes—the flux of electrons to the emitter surface followed by the transmission of electrons through the surface barrier. Either of these processes could be the determinant of the emission current. Emission current instability and current non-uniformity could be explained by the variation in the electron transmission process. Unstable emission current is due to absorption/desorption of gas molecules on the emitter surface (barrier height variation), and non-uniform emission is usually due to spatial variation of tip radius (barrier width change). These problems could be solved if the emission current is determined by the electron supply to the emitter surface instead of the electron transmission through the surface barrier. In this work, we use the inversion layer of a MOSFET to control the electron supply. It moves the current controlling barrier from the tip emitter surface (semiconductor/vacuum interface), which is susceptible to adsorption/desorption processes and spatial variation, to the source/channel interface (pn junction barrier), which is immune to adsorption/desorption and spatial variation.

Emission current stability and the spatial uniformity of field emission devices are improved when a lightly doped drain-MOSFET (LD-MOSFET) is integrated with a field emission array (FEA). At comparable current levels, the emission noise (ΔI/I) decreased from 16.9 % to 1.8%. Emission current fluctuation was reduced in the integrated device compared to the FEA device even in the presence of gasses (Figure 1). Spatial current uniformity was achieved in the integrated MOSFET/FEA devices at different wafer positions (Figure 2) and for different array sizes. The results are explained by a two-step field emission process, which consists of an electron supply step determined by the MOSFET inversion layer and an electron transmission step determined by the field emission barrier width. The device structure also results in low voltage control of emission current.

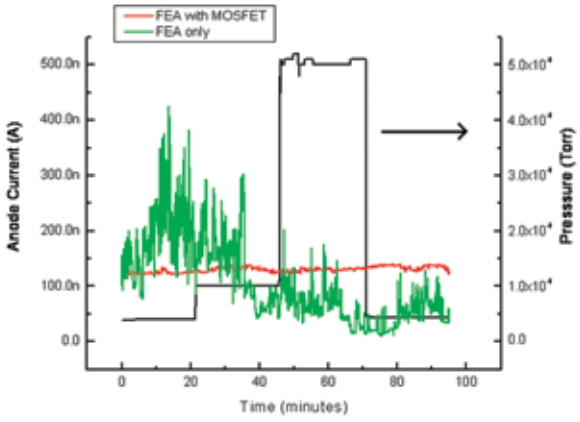


Figure 1: Emission current stability in an integrated LD-MOSFET/FEA device with and without MOSFET control in nitrogen.

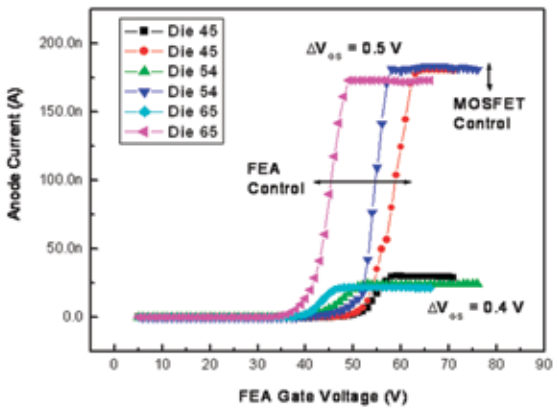


Figure 2: Spatial emission current uniformity in the integrated devices on different positions of the wafer. ΔV is 0.5 V (anode current is 170 nA) and 0.4 V (anode current is 25 nA).

# Double-Gated Silicon Field Emission Arrays

L-Y. Chen, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

There is a need for massively parallel, individually addressed and focused electron sources for applications such as flat panel displays, mass storage, and multi-beam electron beam lithography. Because of this need, double-gated FEAs have drawn much attention in the past decade for their effective beam collimation ability. Among the approaches, Dvorson, Tang, Itoh, and Py discussed and showed that a local and out-of plane (L/OP) focal electrode provides the best focusing albeit at a slightly higher gate voltage [1-4]. This project fabricates and characterizes L/OP double-gated field emission devices with high aspect ratio. One of the gates extracts the electrons while the second gate focuses the electrons into small spots. High aspect ratio silicon field emitters were defined by reactive ion etching of silicon followed by multiple depositions of polycrystalline oxide insulators and silicon gates. The layers were defined by a combination of lithography, chemical mechanical polishing, and micromachining. We obtained devices with 0.4μm gate aperture and 1.2μm focus aperture. The anode current has very little dependence on the focus voltage, and the ratio of the focus field factor to the gate field factor $\beta_F / \beta_G$ is 0.015. Scanning electron micrographs (SEM) of the devices, numerical simulation, and spot size measurements on a phosphor screen confirmed these results. Figure 1 and Figure 2 prove that the gate has a stronger effect on the initial beam spread than the focus gate. An e-beam resist, PMMA, was successfully exposed using the FEA device as an electron source.

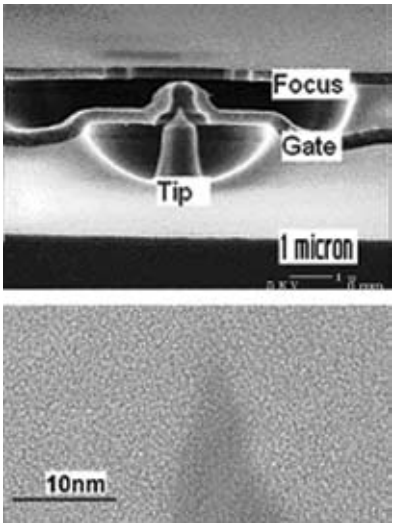


Figure 1: (Top) SEM picture of the cross section of the completed device. (Bottom) Transmission Electron Microscopy (TEM) picture of the sharp tip. According to the TEM, the tip has about 3nm tip radius.

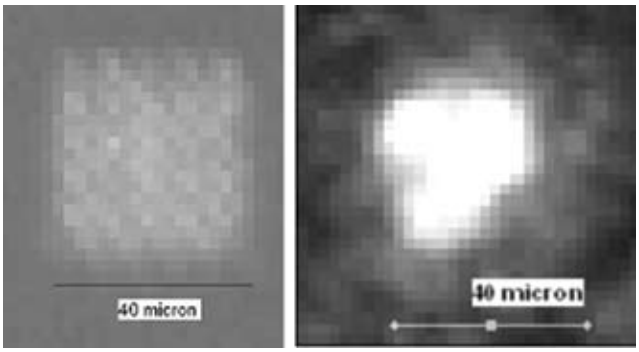


Figure 2: (Left) An optical microscope photo of an original 5x5 array, which has a 40x40μm array size. (Right) A 5x5 array generated a spot, whose diameter is about 40μm, at $V_G$=70V and $V_F$=20v on the phosphor screen.

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# Three-Dimensional Oxidation of Shaped Silicon Surfaces

C.-Y. Hong, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

As silicon device dimension decreases, a three-dimensional silicon oxidation mechanism becomes more important. The device can no longer be assumed to have one or two dimensions, but all three dimensions have to be taken into account. The objective of this work is to study the three-dimensional silicon thermal oxidation behavior by examining the oxidation sharpening process for forming silicon field emission tips. Field emission arrays (FEAs) have been studied as potential electron sources for a number of vacuum microelectronic device applications. A field emitter is usually a high aspect ratio microstructure (tip height >> tip diameter). It results in a high electrostatic field at the apex when a voltage is applied to a proximate annular electrode.

Three-dimensional thermal oxidation behavior on silicon is examined by studying the oxidation process for forming silicon field emitters. Oxide growth rate on the convex surface of a silicon feature is retarded due to stress. The sidewalls of the silicon features have a slightly higher oxidation rate because the sidewalls have more atomic steps due to their curvature increasing the reaction surface area. The oxidation rate of the top of the silicon post depends on the stress relief from the convex edges and the influx of excess oxidants from the convex edge. Figures 1 and 2 show the transmission electron microscope (TEM) images of the silicon features with different original oxide cap size.

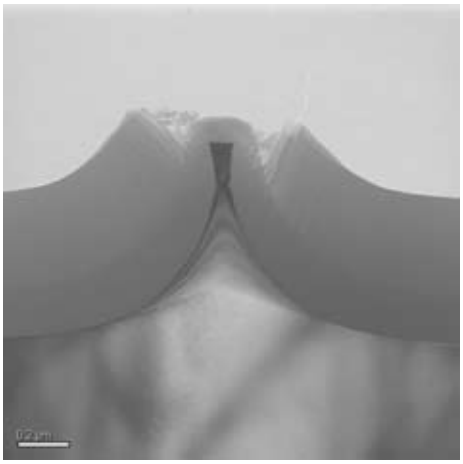

Figure 1: Transmission electron microscope (TEM) image of the silicon feature (original oxide cap size is 1.1 $\mu$m) oxidized at 950 $^{o}$C for 15 hours.

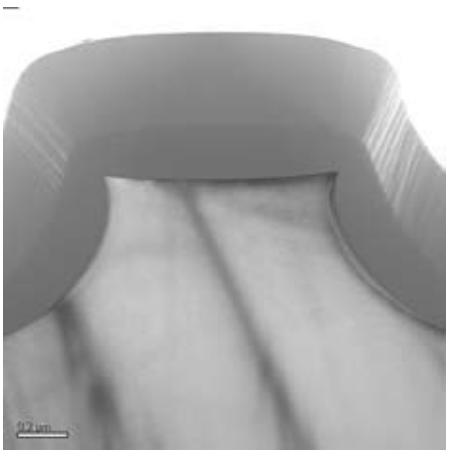

Figure 2: TEM image of the silicon feature (original oxide cap size is 1.8 $\mu$m) oxidized at 950 $^{o}$C for 15 hours.

# Oxidation Sharpening Mechanism for Silicon Tip Formation

C.-Y. Hong, A.I. Akinwande
Sponsorship: CreaTV Micro Tech, NIH, DARPA

Sharp silicon tips have a number of device applications such as (a) silicon field emission arrays, (b) atom probes, (c) atomic force microcopy probes, and (d) field ionization probes for biological and electric propulsion. The radii of the silicon tips for most of these applications are required to be as small as several nanometers. Sharp silicon tips are usually fabricated by isotropic silicon etch followed by oxidation sharpening. Oxidation sharpening is feasible for the silicon tip formation process mainly due to the much slower oxide growth rate on the curved silicon surface. The objective of this work is to study the thermal oxidation mechanism in the oxidation sharpening step for forming sharp silicon tips.

A new silicon tip formation mechanism is proposed. A neck fracture stage precedes the formation of the sharp silicon tip rather than the continuous oxidation of hyperbolic shaped silicon neck as was previously believed to be the case. Stress from the volume difference between silicon and silicon dioxide is the main reason for the silicon neck fracture. Micro-cracks form around the neck at high temperature due to stress from $Si/SiO_2$ volume difference. It is followed by oxide growth into the cracks after crack formation (Figure 1) and a sharp silicon tip is then formed by further oxidation (Figure 2). After the sharp silicon tip is formed, extensive over-oxidation will shorten and blunt the tips, but a short over-oxidation will only shorten the tip without altering the small tip radius.

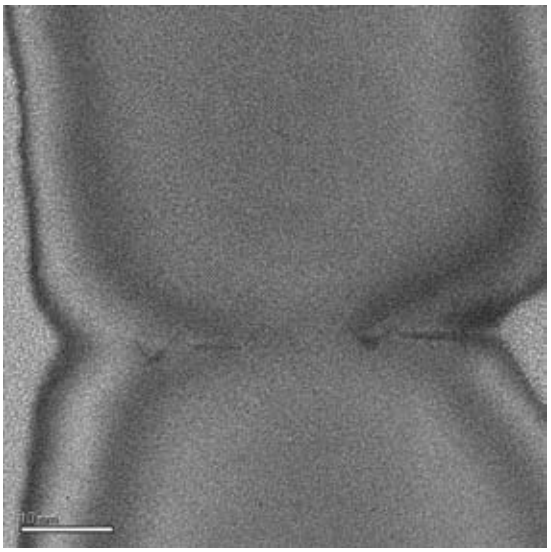

Figure 1: High-resolution transmission electron microscope (TEM) image of the neck region in the silicon feature.

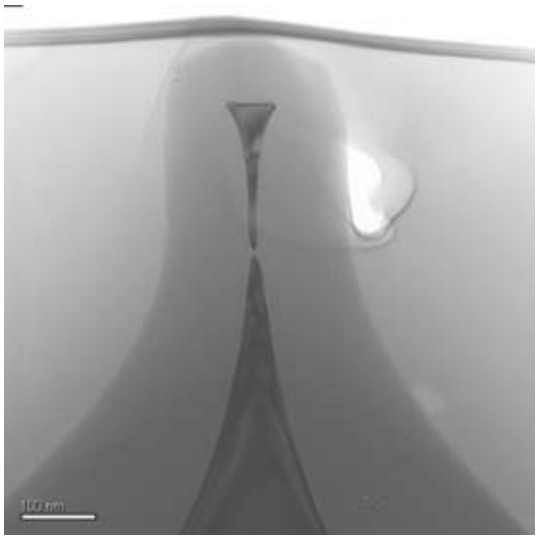

Figure 2: TEM image of the silicon neck region. Silicon was consumed to form a very sharp tip.

# Magnetic and Magnetooptical Films Made by Pulsed Laser Deposition

V. Sivakumar, A. Rajamani, C.A. Ross
Sponsorship: Pirelli, Ferry Fund, MicroPhotonics Center Consortium, ISN

We have established a thin film laboratory that includes a pulsed laser deposition (PLD) system, and a ultrahigh vacuum sputter/analysis system. In PLD, a high energy excimer laser is used to ablate a target, releasing a plume of material that deposits on a substrate to form a thin film. PLD is particularly useful for making complex materials such as oxides because it preserves the stoichiometry of the target material.

We have been using PLD to deposit a variety of oxide films for magnetooptical devices such as isolators. These materials include iron oxide, which can adopt one of four different ferrimagnetic or antiferromagnetic structures depending on deposition conditions, and bismuth iron garnet (BIG, $Bi_3Fe_5O_{12}$), which is useful for magnetooptical isolators in photonic devices. The ideal material for an isolator combines high Faraday rotation with high optical transparency. Garnets have excellent properties, but do not grow well on silicon substrates, making it difficult to integrate these materials. In contrast, iron oxide (maghemite) grows very well on MgO or Si, with high Faraday rotation, but its optical absorption is high. Recently we have examined magnetic perovskites such as Fe-doped barium titanate (Figure 1). These materials show weak magnetic properties, but absorption is low, and the films grow with good quality onto MgO substrates. The magnetization versus temperature behavior for these materials is shown in Figure 2. In another set of experiments, we have started to examine how the magnetization of oxide films can be influenced electrochemically, making a chemically-switchable material. Thin films of iron oxide (maghemite and magnetite) are grown on conducting substrates like copper and are subjected to lithium insertion by electrochemical discharge in a coin cell. It is observed that the magnetization of the film decreases upon electrochemical discharge accompanying the insertion of lithium into the interstices in the inverse spinel structure.

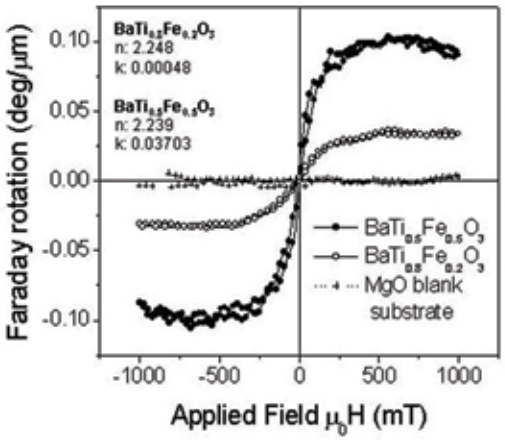


Figure 1: Faraday rotation vs. applied field for 750 nm-thick $BaTi_{0.5}Fe_{0.5}O_3$ and $BaTi_{0.8}Fe_{0.2}O_3$ films on MgO substrates, with the field perpendicular to the film. Inset: optical properties of the two films at 1.55 μm wavelength.

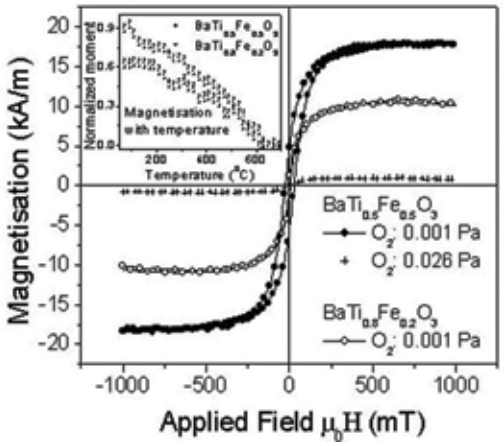


Figure 2: VSM results measured in plane for 750 nm-thick $BaTi_{0.5}Fe_{0.5}O3$ and $BaTi_{0.8}Fe_{0.2}O_3$ films on MgO substrates. Inset: their magnetization vs. temperature behavior.

# Modeling of Pattern Dependencies in the Fabrication of Multilevel Copper Metallization

H. Cai, D. Boning

Sponsorship: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, MagnaChip

This research is to understand, model, and optimize the interaction between copper electroplating and chemical mechanical polishing (CMP) processes. Currently, this research focuses on the coupling that exists due to pattern-dependent topography, which propagates from the electroplated surface into CMP dishing and erosion. A semi-physics plating model is proposed to deal with random layout in real ICs with better predictive accuracy. Compared to the previous electroplating model developed in our group, the new model has much improved root-mean-square (RMS) error (less than 300 Å). It predicts the topography more realistically and with higher resolution. In particular, the submicron structures clearly show corner and edge effects in the specially designed high-resolution profiler scans. Furthermore, the successful electroplating model is extended to the second-level metallization case by considering the underlying uneven topography form of the first-level metallization. Figures 1 and 2 show the prediction results for the second-level electroplating with grid size 10×10 μm. An improved and coherent chip-scale model framework for copper bulk polishing, copper over-polishing, and barrier layer polishing is developed. The integration of contact wear and density-step-height models is more seamlessly implemented and addresses inherent shortcomings of the previous model. In the new model, a local density instead of the effective density computed by using a planarization length is used, and only a contact wear coefficient is used to characterize the long-range planarization capability. Results obtained with the new model show a significant improvement in the modeling accuracy to less than 100 Å of root-mean square error. Furthermore, the new model framework can be adapted for the modeling of multi-level metallization processes when combined with the electroplating pattern dependence model.

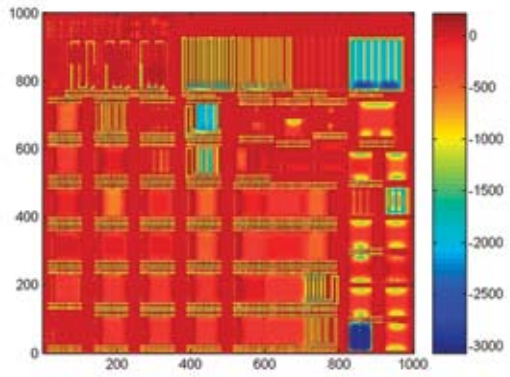


Figure 1: Pre-electroplating envelope map for the second-level metallization (unit: Å).

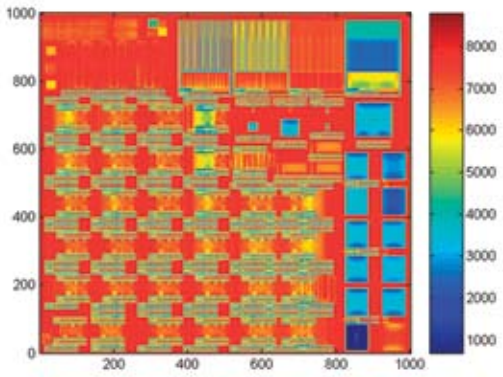


Figure 2: Post-electroplating envelope map for the second-level metallization (unit: Å).

## REFERENCES:

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# PFC Alternatives

A. Somani, R. Reif

Sponsorship: NSF/SRC Engineering Research Center for Environmentally Benign Semiconductor Manufacturing, Applied Materials

The goal of this project is to identify possible alternatives for perfluorocompound chemistries for wafer patterning that do not pose long-term environmental problems and that can also sustain ever increasing demands from the process viewpoint. The etch viability of a variety of alternatives has been determined, and so far the most promising candidates according to experiments conducted, chemistry A, was compared with the new chemistry B. This series of experiments can be considered as a preliminary evaluation for the new gas. These novel chemistries were tested on conventional silicon dioxide films. The effluents of these processes will be identified with Fourier Transform Infrared Spectroscopy (FTIR), optical emission spectroscopy (OES), and Residual Gas Analyzer (RGA) at both the chamber and exhaust levels.

This work was carried out at Applied Materials, Santa Clara. An Applied Materials 8" etch system, Enabler, has been used for all experiments. In Figure 1, the experimental set up for this work is depicted. Low pressure RGA was employed at the chamber level for *in-situ* measurements of neutral species. The low pressure RGA was an Inficon Transpector II with a 300 mass range operating at about 1e-6 torr. An Inficon Transpector CIS 2 gas system has the capability to measure a minimum detectable composition change of 200 ppb. The ionizer energy for all measurements were fixed to 70 eV electron beam, and the electron multiplier gain value was 1300. The Fourier Transform Infrared Spectrometer was a Nicolet model 470 with a 6.5 meter CIC Photonics gas cell. It was connected to look for stable species in exhaust. There is also an MKS high pressure RGA connected to the exhaust. Figure 2 summarizes the preliminary FTIR results for blanket oxide etching with all high potential global warming gases that were observed in the exhaust.

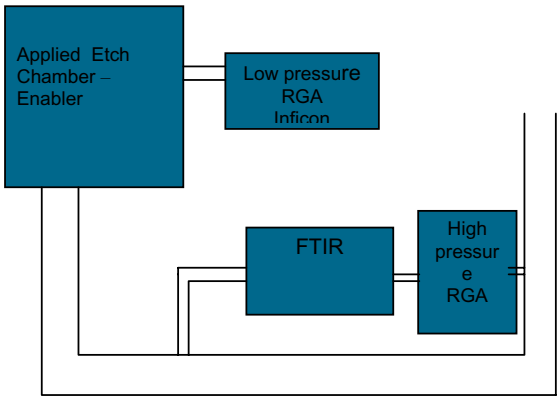


Figure 1: Experimental Set up

| Etch recipe | Data presented in standard cubic centimeter | | | | | | |
|---|---|---|---|---|---|---|---|
| Gases ratio | C2F6 | CO | CHF3 | HF | COF2 | A | B |
| Chemistry A/O2 (65/60) | 30.57 | 125.67 | 0.72 | 0.75 | 20.75 | 1.45 | 0.00 |
| Chemistry A/O2 (75/60) | 46.84 | 135.33 | 1.17 | 1.14 | 20.65 | 1.74 | 0.00 |
| Chemistry B/O2 (65/60) | 3.20 | 169.17 | 3.92 | 44.70 | 38.20 | 0.00 | 7.40 |
| Chemistry B/O2 (75/60) | 5.92 | 174.00 | 3.75 | 45.02 | 41.30 | 0.00 | 7.96 |

Figure 2: Amount of gases in exhaust for each blanket oxide etch experiment

# Characterization and Modeling of Plasma Etch Nonuniformities

K.O. Abrokwah, D. Boning
Sponsorship: Texas Instruments, Praesagus, Inc., SRC Masters Scholarship

We present work characterizing spatial variations in Integrated Circuits (IC) etching. Our work modeling non-uniformities in IC metallization encompasses plasma etching of trenches in an oxide film stack. We study non-uniformity induced by features that are being etched. These non-uniformities manifest themselves in the form of microloading and aspect ratio dependent etching.

Microloading causes spatial non-uniformity at the chip or die scale and results from design-dependent diffusion of reactant species across the wafer surface. This design-dependent diffusion describes the effect of loading on the overall concentration of reactant species. The loading is greatest in the area of high pattern density because that is where there are the most exposed surface and thus the highest loading of reagents. We characterize etch variations by etching a wafer with dies containing structures of different pattern density (i.e. structures with differing amounts of unmasked oxide). A pattern density model is fitted to the etch depth data, and the model can then predict etch variation for arbitrary amounts of exposed oxide. The model accounts for the decrease in reactant concentration in areas of high loading caused by high pattern density (Figure 1).

Aspect ratio dependent etching occurs at the length scale of individual features and structures. At this length scale, the transport of etchant species from the top of the wafer surface down to the bottom of the trench or hole being etched determines the overall etch rate of the feature. Knudsen transport, a model of how reactants traverse the etched feature, assumes a probability of transmission of reagents that depends on the aspect ratio of the feature. Neutral and ion shadowing model the line of sight transport of reactant species from the plasma down to the bottom of a feature. The Knudsen transport kinetics has been used by Coburn and Winters in their model. We have augmented the Coburn and Winters model to include a sidewall sticking coefficient and compared our experimental depth data to simulated data from the augmented model (Figure 2).

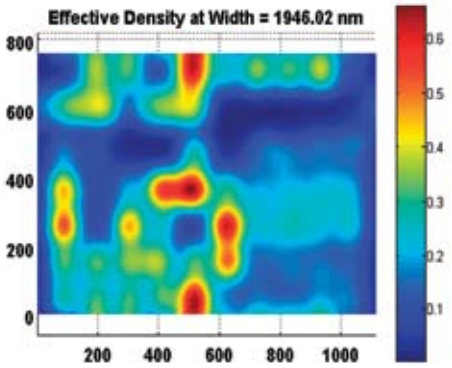


Figure 1: The figure shows the effective pattern density for the test chip containing structures with varying density (loading). The effective pattern density models the effect of neighboring densities.

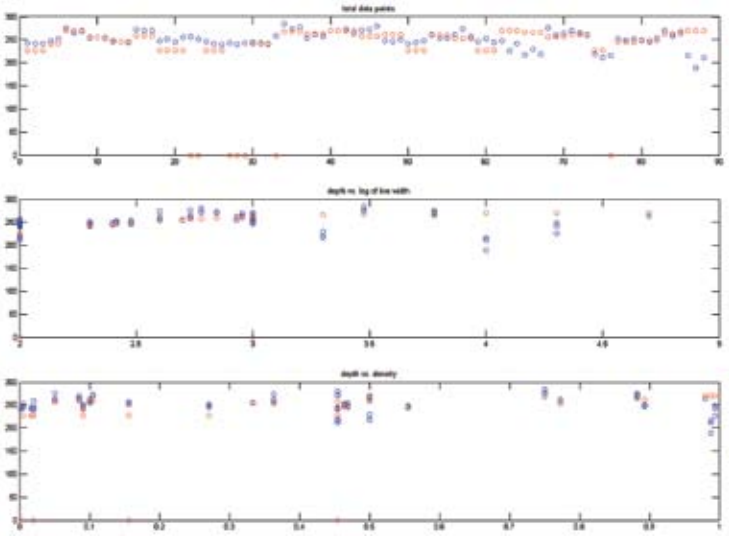

Figure 2: The figure compares the empirical (blue) depth and the simulated depth versus individual features (top), versus linewidth, and versus density.

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# Three-Dimensional Integration: Analysis and Technology Development

K.N. Chen, C.S. Tan, A. Fan, R. Reif
Sponsorship: DARPA, MARCO IFC

The main objective of this research project is to demonstrate functional three-dimensional (3-D) integrated circuits based on the stacking of silicon active layers. The bulk of the work focuses on process technology development for silicon active layers stacking using low temperature wafer bonding and wafer thinning. Two types of low temperature wafer bonding are investigated; one is the thermo-compression Cu wafer bonding and the other is direct oxide wafer bonding. Cu wafer bonding is used as a permanent bond between active device layers, while oxide wafer bonding is used as a temporary bond between donor wafers and handle wafers. Two types of stacking orientation are explored; either face-to-face or back-to-face. Bi-layer and four-layer stacks are demonstrated on blanket wafers.

A novel test structure for contact resistance measurement of bonded Cu interconnects in three-dimensional integration technology is proposed and fabricated. This test structure requires a simple fabrication process and eliminates the possibility of measurement errors due to misalignment during bonding. Specific contact resistances of bonding interfaces with different interconnect sizes of approximately $10^{-8}$ Ω-cm$^2$ are measured. A reduction in specific contact resistance is obtained by a longer anneal time. The specific contact resistance of bonded interconnects with a longer anneal time does not change with interconnect sizes [1].

The morphology and bond strength of copper-bonded wafer pairs prepared under different bonding/annealing temperatures and durations are presented. The interfacial morphology was examined while the bond strength was examined from a dicing test. Physical mechanisms explaining the different roles of post-bonding anneals at temperatures above and below 300°C are discussed. A map summarizing these results provides a useful reference for process conditions suitable for actual microelectronics fabrication and three-dimensional integrated circuits based on Cu wafer bonding [2].

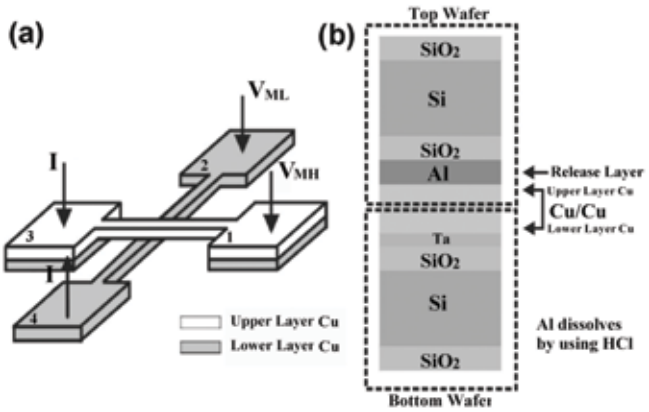


Figure 1: Schematic diagram of the contact resistance test structure [1].

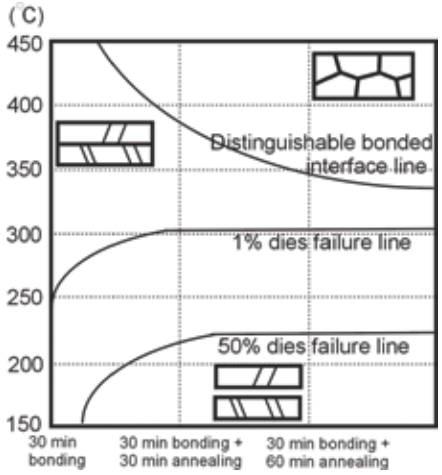


Figure 2: Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [2].

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# Interfacial Electromigration in Cu-Based IC Metallization

Z.S. Choi, F. Wei, C.C. Wai, C.L. Gan, K.L. Pey, W.K. Choi, C.V. Thompson
Sponsorship: SRC, SMA

Electromigration, the diffusion of atoms caused by a momentum transfer from conducting electrons, is one of the main causes of failures in interconnects [1]. It has been shown that the dominant diffusion path in copper interconnect technology is along the interface between dielectric capping layers and copper [2]. It is critical to minimize the diffusion at this interface in order to increase the reliability of copper interconnects. We are carrying out two sets of experiments to investigate interface and surface electromigration in copper interconnects.

In the first set of experiments, the fabrication of test structures is terminated after chemical mechanical polishing of the second metallization layer, which means that the $Si_3N_4$ capping layer is not deposited on top of second metallization, therefore the top copper surface of the second metallization is exposed (Figure 1). Samples are heated in reducing gas to remove copper oxide, and then tested at pressures of less than $10^{-6}$ torr, both in specially designed test systems in which the ambient can be used to modify the structure and chemistry of the Cu surface, and for *in-situ* testing in an SEM (Figure 2).

Through these experiments, we are obtaining fundamental constants such as surface diffusivity, drift velocity, and activation energy for diffusion.

In a second set of experiments, the copper surface is treated using various techniques before deposition of an $Si_3N_4$ dielectric capping layer. Various surface treatments will provide information on the effects of both the surface treatments and the mechanical constraints due to capping layers. Treatments that improve the lifetime of the interconnect test structure will be investigated to understand the mechanism that leads to the improvement.

Data from these basic studies are used in models and simulations. Models and simulations are utilized to predict the reliability of more complex interconnect structures. Simulations are compared with tests on complex structures manufactured at Sematech in the US and the Institute for Microelectronics in Singapore.

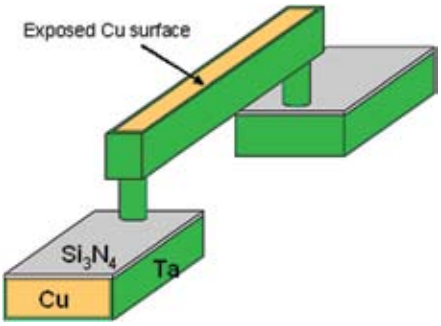


Figure 1: A test structure for which fabrication was terminated before deposition of a dielectric capping layer on top of the test segment in the second level of metallization (lead lines are in the first level).

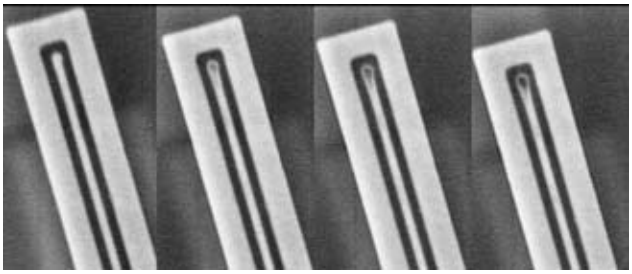

Figure 2: *In-situ* SEM images of the cathode of a test structure, showing surface electromigration damage. The test line is surrounded by a Cu extrusion monitor.

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# Effects of Mechanical Properties on the Reliability of Cu/Low-K Metallization Systems

F.L. Wei, Z-S. Choi, C.C. Wai, C.L. Gan, K.L. Pey, W.K. Choi, C.V. Thompson
Sponsorship: SRC

Electromigration-induced failure remains a critical concern for evolving Cu/low-k metallization technologies. Low elastic moduli, characteristic of low-k dielectrics, and decreasing liner/diffusion barrier thicknesses, with decreased elastic stiffness, lead to significant reliability degradation [1,2]. Thus, achieving future reliability requirements, as current densities increase and interconnect dimensions decrease, will become increasingly challenging. We have undertaken a comprehensive study involving both the experimental characterization of metallization materials and reliability testing of fully processed test structures, as well as simulation and analyses of mechanical responses and electromigration-induced stress evolution.

Electromigration is current-induced atomic diffusion that leads to an evolution in the stress state within interconnect segments. As Cu atoms are forced toward a via, where the liner at the base blocks atomic diffusion, a compressive stress develops and can eventually lead to the mechanical failure of the surrounding material system, and to extrusions of Cu.

The compressive stress that results from electromigration depends on the effective elastic modulus, B, of the interconnect system: the liner, interlevel dielectric (ILD), and cap/etch-stop layers (Figure 1). In order to accurately characterize the mechanical properties of low-k ILD materials, some of which are extremely sensitive to environmental effects, we have employed a suite of experimental techniques, including nanoindentation, cantilever deflection, pressured membrane deflection for characterization of materials deformation, and 4-point bending and double-cantilever pull structures for adhesion measurements. Experimentally measured mechanical properties of individual materials can be used to calculate B, using finite element modeling (FEM) analyses for complex geometries and stress states.

Comparisons between model expectations and lifetime testing are being carried out using test structures manufactured by Sematech.

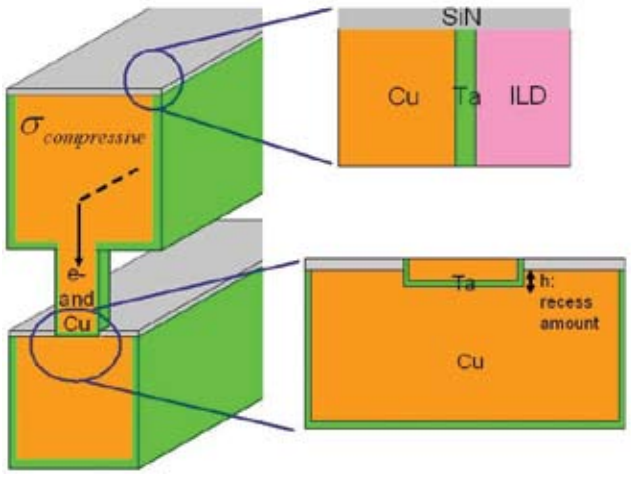


Figure 1: Schematic view of the Cu/low-k interconnect system under compressive stress due to electromigration of Cu atoms.

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# Cu Bonding Technology for Three-Dimensional Integrated Circuits

R. Tadepalli, H.L. Leong, C.L. Gan, K.L. Pey, D.E. Troxel, C.V. Thompson
Sponsorship: DARPA (3D Integrated Circuits), SMA, IME

The characterization of Cu wafer bonding is critical to the successful implementation of a three-dimensional (3D) integrated circuit (IC) technology (Figure 1). Previously, we have studied the toughness of bonded Cu interconnects using a mixed-mode fracture test [1]. We have shown that high toughness Cu bonds can be created at a bonding temperature of 300°C using the EV501 bonding tool in MTL [1].

Our present work investigates Cu bond toughness under Mode I (tensile) loading. A novel test methodology has been developed to analyze the toughness of wafer/die-level thermocompression Cu bonds. The effect of lift-off patterned Cu pad size/density on the bond toughness will be studied. Additionally, Mode I bond toughness values are useful metrics for the characterization of Cu-sealed microchannels for heatsinking (Figure 1). A theoretical study of the microchannel *heat removal-bond strength* trade-off has been performed to obtain optimum channel dimensions.

The fundamental limit of the toughness of a Cu bond will be probed using an UHV-AFM/deposition system. Pristine Cu films will be deposited on a substrate and a cantilever tip, and the tip-substrate adhesion will be measured, under UHV conditions, thereby maintaining oxide-free Cu surfaces. Such measurements cannot be performed on a wafer-scale due to the lack of a commercial UHV-bonding tool.

We are also investigating the quality of bonded ECP damascene-patterned Cu interconnects (NTU, Singapore). The bond toughness is evaluated using a four-point bend test. The effects of Cu film texture, Cu pattern density, and the CMP (chemical mechanical polishing) process on the bond quality are being studied. Under thermo-compression, the wafers overcome the effects of polishing non-uniformity and the dishing effect, to bond with varying degrees of success. Moreover, we have designed novel test structures to assess the reliability of bonded Cu interconnect structures.

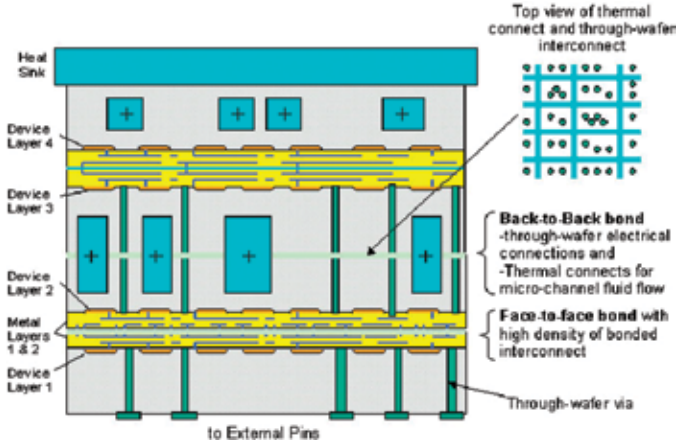


Figure 1: 3D IC technology with thermal management. Wafers are stacked using alternate face-to-face and back-to-back bonds.

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# Numerical Techniques in Biomolecule Design and Systems Biology

D. Vasilyev, J. Bardhan, M. Altman, S. Kuo, P. Ramirez, P. Barton, B. Tidor, J. White
Sponsorship: NIH, SMA, NSF

To design an effective drug or a biochemically-based sensor, it is necessary to develop ligand molecules that bind readily and selectively to receptors of interest. Electrostatic forces play an important role in the design of ligands, but the complicated three-dimensional geometry of the problem makes it difficult to assess the electrostatic fields and then optimize the ligand. We have been developing fast methods for electrostatic analysis, and have been focussed on three aspects.

First, we have developed a fast analysis program based on using discretized integral equation formulations plus sparsification-accelerated iterative techniques. Second, we have coupled electrostatic analysis with the ligand charge optimization problem using a Hession-implicit approach [1]. Finally, we have been developing improved discretizations of the molecular surface geometry using curved panels, and have developed approaches for computing integrals over curved panels [2].

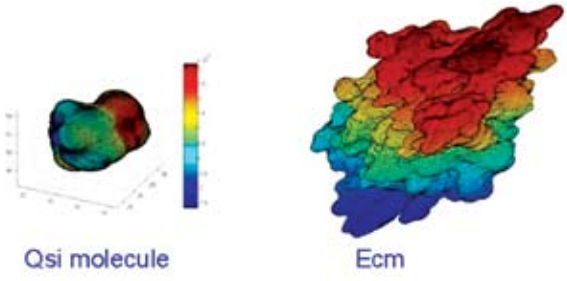


Figure 1: Electrostatic design problem

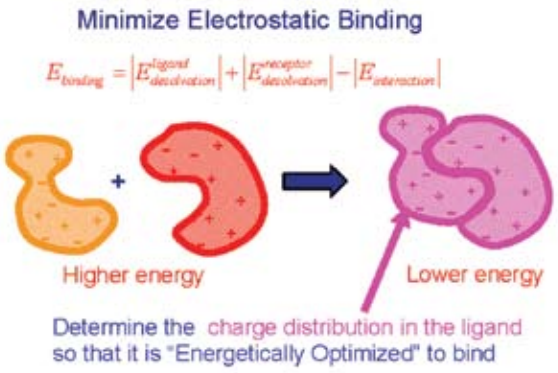


Figure 2: Molecular Surfaces for two proteins

## REFERENCES:

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# Field Emission from Organic Materials

I. Kymissis, A.I. Akinwande
Sponsorship: NSF

Field emission devices have shown tremendous potential in a wide variety of applications. Displays, high intensity lighting, RF amplifiers, chemical analysis systems, and space propulsion schemes have all been proposed using field emitters. Field emission displays (FEDs) are perhaps one of the most interesting potential applications because of the high energy efficiency of cathodoluminescence, demonstrated long lifetime of available phosphors, wide color gamut, and angle-independent viewing characteristics.

Despite this promise, FEDs have failed to penetrate the consumer market and many companies have abandoned FED development. The manufacturing processes pursued so far have capital and production costs that are too high for commercialization. In this work, we have developed a new field emission architecture that allows the use of low cost materials while simultaneously offering the possibility of a uniform, low-noise display controlled with low voltages. These goals are achieved by integrating an organic field effect transistor (OFET) with an organic field emitter (OFED). In our demonstration device, both the OFED and OFET are created at room temperature using a non-lithographic process. By moving the barrier that controls emission from the field emitter surface to the transistor source-channel junction and eliminating the need for a micromachined gate, high performance and uniformity can be achieved in a potentially low cost process. We have demonstrated a reduction in current noise, immunity to residual gas exposure, and low voltage control of the electron flux control using this FED architecture.

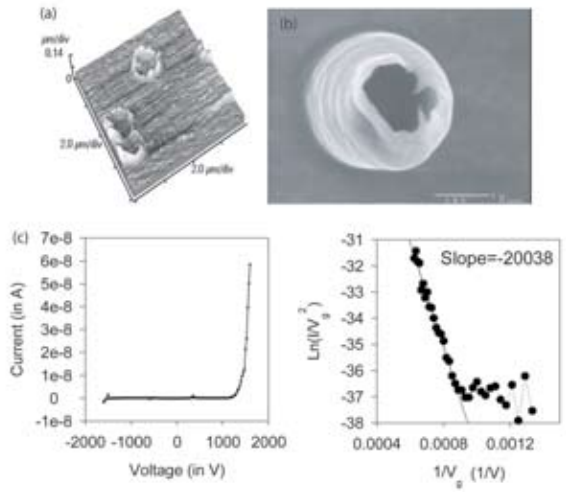


Figure 1: Figure (a) shows an atomic force micrograph of the organic field emitter, (b) shows a scanning electron micrograph, and (c) shows typical emission characteristics for the devices.

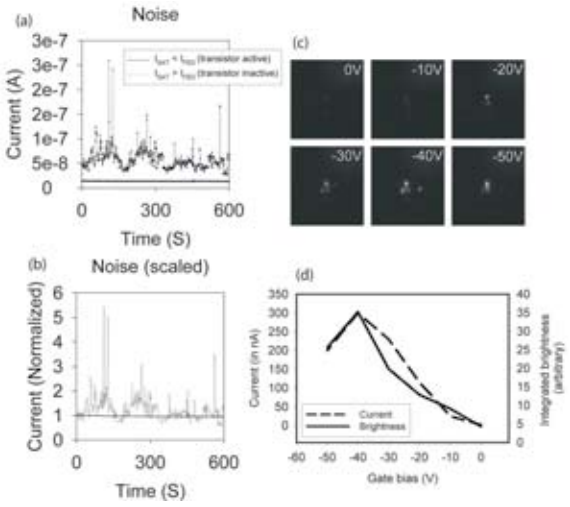


Figure 2: Figures (a) and (b) show the reduction in current noise achieved by the control technique developed; –(c) and (d) demonstrate that over 100:1 brightness switching can be achieved with 30V applied to the transistor (controlling a 1100V electrons).

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[2] Kymissis, I., A.I. Akinwande, "Field Emission from Organic Composites," International Vacuum Microelectronics Conference 2002, Lyon, France, July 2002.

[3] Kymissis, I., A.I. Akinwande, "Organic Field Emission Device Integrated with Organic Transistor," Accepted, *IEEE Transactions on Electron Devices.*

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# Integrated Organic Electronics

I. Kymissis, K. Ryu, A.I. Akinwande, C.G. Sodini, V. Bulovic
Sponsorship: MARCO MSD, NSF

Organic electronics hold promise for a wide range of applications. Using organic materials it is possible to fabricate transistors, organic light-emitting devices (OLEDs), and photodetector elements; all at low process temperatures (<90º C). While many of these individual devices have been extensively studied and optimized, technologies that are able to produce a large number of devices as well as different types of devices together in integrated circuits are not well developed.

The goal of this project is to make a fully lithographic modular platform for organic electronics that is capable of supporting organic field effect transistors (OFETs) or other related amorphous thin film transistors together with organic photodetectors and OLEDs. Because these systems can be fabricated at low temperatures, they are compatible with a wide range of substrates, including flexible polymeric foils.

To date, the project has achieved several milestones, including: the development of a fully lithographic OFET backplane process, a self-aligned OFET process (Figure 1), and the demonstration of an active matrix organic integrated photodetector array (Figure 2). Work continues on the refinement of these modular elements and their integration with organic light-emitting devices (OLEDs) to create a full-feedback controlled OLED display system that compensates for degradation in OLED devices as well as nonlinearities in the driving circuitry.

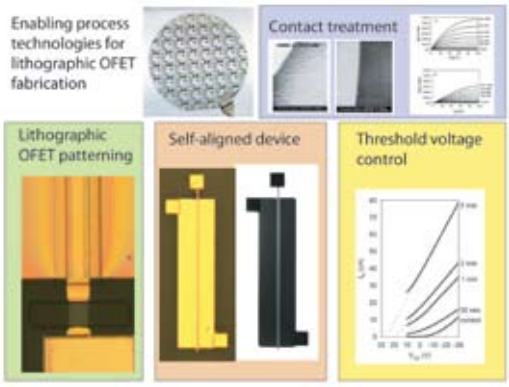


Figure 1: A summary of the technologies that we have developed to enable the lithographic fabrication of OFET backplanes and control their characteristics. The wafer shown is a typical 100mm wafer processed using our lithographic process.

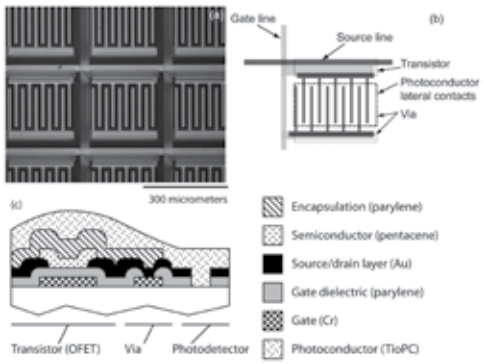


Figure 2: (a) Shows a micrograph of the low temperature active matrix photodetector presented in [1] (b) details the structure of the photodetector, and (c) schematically shows the device cross section. The transistor backplane is fabricated first; it is isolated using a layer of parylene, and a vias cut into parylene allow the photoconductor access to the interdigitated electrode structure.

## REFERENCES:

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# Charge Trapping in Layered Nanostructured Films

J. Yu, C. Madigan, S.H. Kang, I. Kymissis, V. Bulovic
Sponsorship: MARCO MSD, MIT, NSF, MRSEC

Structural disorder in amorphous organic thin films can result in localized electronic states that trap and store charges in equilibrium. These trapped charges can dominate the current-voltage (I-V) characteristics of organic devices due to the relatively low charge carrier density in organic solids.

Our recent experiments on organic devices with deliberately-inserted metal or organic traps demonstrated that charge trapping can significantly alter I-V characteristics of an operating device [1]. Predictions of energy band structure indicate that an ITO anode / 50 nm Alq3/ 10 nm trap / 50 nm Alq3 / 50 nm Mg:Ag / 50 nm Ag cathode structure with a trap layer of organic DCM2 or silver metal can be effective at trapping charge. This monopolar device transports only electrons. When a forward bias is applied on the device, electrons begin to fill the trap layer (Figure 1). With increased trap filling, the number of traps decreases, resulting in an increase in the effective charge mobility. Additionally, as the deep metal traps are filled, the effective trap level within the charged metal nanoclusters decreases. With decreasing trap depth, the probability of finding a trapped electron outside the trap boundaries increases, and the trapped carrier density can exceed the intrinsic carrier density in the vicinity of the trap (Figure 2). The trapped charges effectively dope the surrounding organic semiconductor which is manifested as an increased conduction through the device and results in a sharp conductance turn-on in the device I-V characteristics. Applying reverse bias on the device depletes the trap layer of electrons and eventually, switches the device to a low conduction state. The device demonstrates on/off current ratio of fifty for the DCM2 trap and ten million for a silver trap. Metals have higher trap density and deeper trap energy, and therefore, have a larger impact on the on/off current ratio.

We are presently modeling the charge trapping mechanism in these structures in order to generate a generalized description of the process. Space charge limited conduction for a uniform trap density and spatially non-uniform charge traps are both considered in our model.

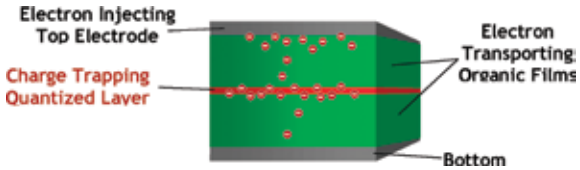


Figure 1: Charge Trapping in a trap layer embedded inside a layered semiconducting structure.

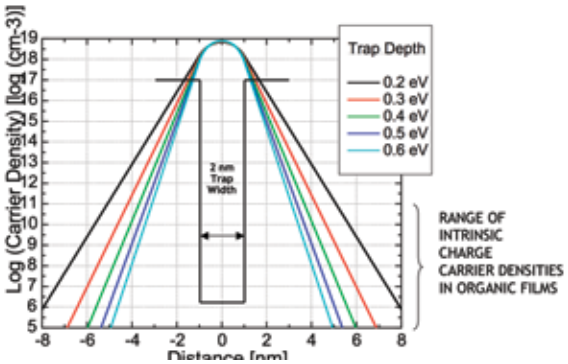


Figure 2: Due to the extent of the wavefunction, spreading charge carrier trapped in a potential well is not confined to the trap. The plot shows the charge carrier density as a function of distance away from the trap for several different trap depths. The magnitude of the trapped carrier density in the vicinity of the trap can greatly exceed the intrinsic charge carrier density in an organic film.

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# Threshold Voltage Modification of Organic Thin-Film Transistors

A. Wang, I. Kymissis, V. Bulovic, A.I. Akinwande
Sponsorship: U.S. Army Natick Center, MARCO MSD

Threshold voltage control of organic field effect transistors (OFETs) is critical to the further development of integrated circuits containing OFETs [1,2]. We report results from a process-level method for modifying the threshold voltage, $V_T$, of pentacene FETs with parylene, an organic polymer, as the gate dielectric. In this approach, treatment of the parylene surface with oxygen plasma or UV-ozone prior to pentacene deposition introduces fixed charged states at the semiconductor-dielectric interface. These states shift the flatband voltage, $V_{FB}$, and, consequently, shift the $V_T$.

Typical I-V characteristics for control and $O_2$ plasma-treated FETs are shown in Figure 1. We can model the effects of trap-introduced charges on $I_D$ in the FET linear region as (a) fixed charges, $Q_{fixed}$, that shift the threshold voltage and (b) mobile charges, $Q_{mobile}$, that increase parasitic bulk conductivity. $Q_{mobile}$, determined from the I-V characteristics, in the $O_2$ plasma-treated FETs is on the same order of magnitude as $\Delta Q_{fixed}$ ($2.0x10^{-6}C/cm^2$) and is an order of magnitude larger than in the control.

Since the 15-second $O_2$ plasma treatment resulted in $V_{FB}$ and $V_T$ shifts greater than +100V, UV ozone treatment was performed instead as a more controllable method of adjusting $V_T$. Quasistatic capacitance-voltage measurements and current-voltage characteristics demonstrate that the flatband and threshold voltages can be shifted gradually with increasing lengths of UV-ozone exposure. Figure 2a and 2b show the monotonic increase in $V_{FB}$ and $V_T$ with ozone exposure time. These results confirm that careful control of interface state densities at the semiconductor-dielectric interface is essential to threshold voltage control in organic FETs.

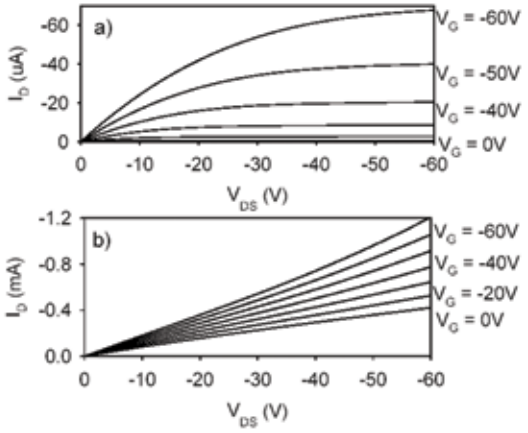


Figure 1: I-V characteristics for (a) control and (b) $O_2$ plasma-treated FETs. The $O_2$-treated device shows much higher drain current, which can be attributed to a more positive threshold voltage and increased bulk conductivity.

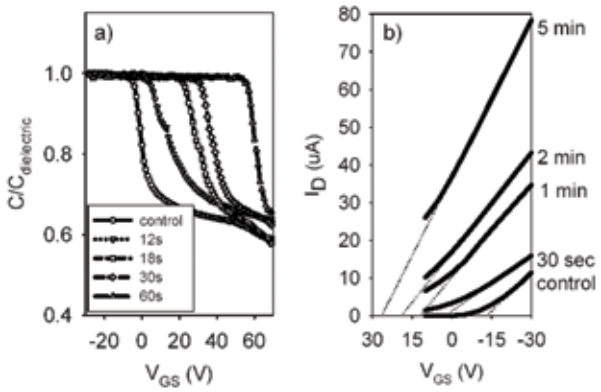


Figure 2: (a) Quasi-static C-V measurement of control and UV-ozone-treated devices. (b) $V_{GS}$ sweep and $V_T$ extrapolation for UV-ozone-treated devices in the FET linear region, $V_{DS}$ = -4V. Both flatband and threshold voltages increase monotonically with ozone exposure time.

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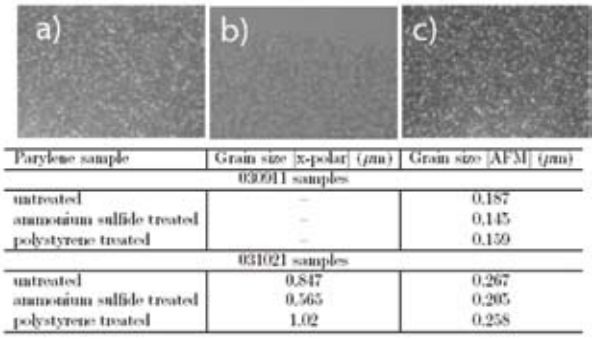
# Effect of Surface Treatments on Pentacene Organic Thin-Film Transistor Performance

A. Wang, I. Kymissis, A.I. Akinwande
Sponsorship: U.S. Army Natick Center

Pentacene TFT performance is strongly dependent on the morphology of the pentacene semiconductor. Larger grain sizes and hence, fewer grain boundaries, have been linked to improved mobility and on/off ratios [1,2]. By modifying the condition of the pentacene growth surface, i.e. the surface of the gate dielectric, pentacene crystallinity and TFT performance may be improved. A more hydrophobic surface is expected to result in better packing of pentacene molecules; Yasuda, et al. reported improved mobility and on/off ratios in pentacene TFTs using more hydrophobic dielectrics [3]. In our work, pentacene TFTs were fabricated using parylene, an organic polymer, as gate dielectric. We examined the effects of an ammonium sulfide treatment and a spin-on polystyrene treatment of the parylene prior to pentacene deposition, and compared the performance of TFTs using (a) untreated parylene, (b) ammonium sulfide-treated parylene, and (c) polystyrene-treated parylene.

Contact angle measurements confirmed an increase in surface hydrophobicity after both treatments. Atomic force microscopy (AFM) and optical microscopy using crossed polarizers showed comparable pentacene grain sizes in the untreated and polystyrene-treated samples. Because of increased average surface roughness, pentacene grain size in the ammonium sulfide-treated sample was smallest (Figure 1). Electrical characterization confirms the trend seen in the physical characterization. Field effect mobility, calculated from conventional saturation region FET equations at $V_{GS} = V_{DS} = -100V$, is significantly poorer in the ammonium-treated device and comparable in the polystyrene and untreated devices (Figure 2). After gate voltage was scaled (to account for different dielectric thicknesses) to obtain the same electric field in each device, the polystyrene-treated device shows the highest mobility. These physical and electrical characterization results demonstrate the importance of the quality of the pentacene growth surface.




| Parylene sample | Grain size x-polar (μm) | Grain size AFM (μm) |
|---|---|---|
| 030911 samples | | |
| untreated | – | 0.187 |
| ammonium sulfide treated | – | 0.145 |
| polystyrene treated | – | 0.159 |
| 031021 samples | | |
| untreated | 0.847 | 0.267 |
| ammonium sulfide treated | 0.565 | 0.205 |
| polystyrene treated | 1.02 | 0.258 |

Figure 1: Optical micrographs using crossed-polarizers of pentacene on (a) untreated, (b) ammonium sulfide-treated, and (c) polystyrene-treated parylene. Each image covers a 36.6μm x 25.6μm area. Measured grain sizes are summarized in the table.

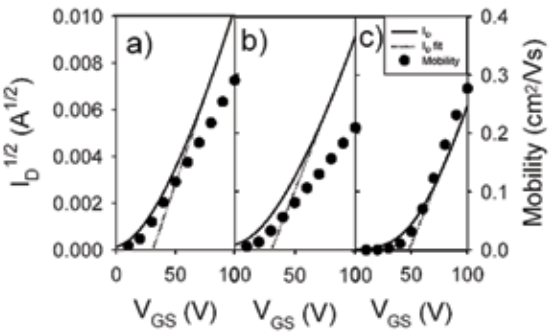



Figure 2: I-V characteristics for (a) control, (b) ammonium sulfide- treated, and (c) polystyrene-treated transistors. The circles plot mobility vs. gate voltage (right axis). The lines show the extraction of threshold voltage from the saturation region, VDS = -100V (left axis).

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# Logic Gates on Fiber: Building Blocks for Electronic Textiles

Y.W. Choi, A.I. Akinwande
Sponsorship: DARPA

Electrotextiles denote the class of fabric structures that integrate electronic elements with textiles. One of the outstanding features of electrotextiles is the ability to personalize. Each system can be tailored by choosing the type of fibers that are included in the design. Another outstanding feature is that electronics can be distributed and made invisible in electrotextiles. It makes the technology invisible, embedded in our natural surroundings, present wherever we need it, enabled by simple and effortless interactions, attuned to all our senses, adaptive to users and context, and autonomously acting [1]. Research on the integration of electronic devices on fibers, which are woven into fabric is being conducted by various groups [2,3]. Thin film transistors were fabricated on polyimide sheets and cut into fibers. The transistors on the fibers were interconnected using conductor fibers, by weaving the fibers using spacer fibers, and a woven inverter circuit has been demonstrated [2]. The amorphous Si thin film transistors (TFTs) were fabricated at 150 °C on polymer substrates [3].

Our approach fabricates logic gates instead of the individual transistors on fibers. In this approach, the "fabric primitives" are fibers consisting of rows or columns of logic gates. There are several advantages to our approach. The first advantage is that fiber-to-fiber signal transmission is digital. This increases noise immunity and improves fault tolerance. The second major advantage of this approach is that systems are configured using an FPGA (Field-Programmable Gate Array) paradigm. The fibers are in essence arrays of logic gates that are personalized through programmable contact vias / interconnects. The third major advantage is that each system could be personalized by choosing the type of "fiber" that is included in the design. For example, if there were a desire for a self-powered system, then we could add a solar cell or battery "fiber." If there were a desire for a large area micro-electro-mechanical system (MEMS), we need to add a piezoelectric-actuated "fiber" for example. We fabricated logic gates, such as inverter, NAND and NOR, using low-temperature (<150 °C) a-Si TFTs technology on polyimide sheets, which were cut into fibers and woven into fabric. These logic gates on fiber may be essential building blocks for electrotextiles.

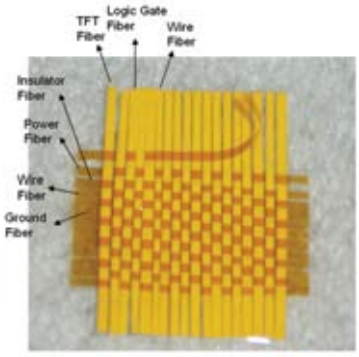


Figure 1: Photograph of the schematic electrotextiles woven polyimide fibers, which can have active devices such as inverters, NAND, and NOR.

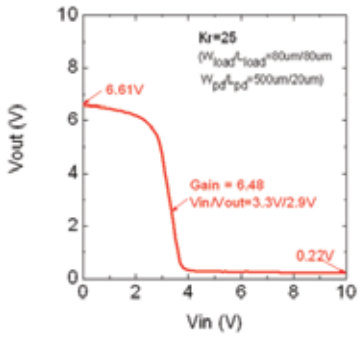


Figure 2: Transfer characteristics of the inverter fabricated with the a-Si TFTs.

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# Low-Voltage Organic Thin Film Transistors with High-K $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ Pyrochlore Gate Insulator

Y.W. Choi, I.-D. Kim, H.L. Tuller, A.I. Akinwande
Sponsorship: DARPA

Thin film transistor circuits using organic semiconductors (oTFT) have received intense interest for applications requiring structural flexibility, large area coverage, low temperature processing, and low-cost [1]. Pentacene TFTs have demonstrated the highest performance among TFTs with an organic semiconductor channel. A major limitation, however, has been unusually high operating voltages (20~100 V), a concern for portable, battery-powered device applications [2]. The high-operating voltage stems from poor capacitive coupling between the gate electrode and channel region. A combination of higher permittivity gate dielectric and reduced dielectric thickness leads to lower voltage operation. Recently, M. Hallk et al. reported low-voltage pentacene OTFTs with very thin (2.5 nm) amorphous molecular gate dielectric [3]. Flexible polymer substrates, characterized by rough surfaces, benefit from the use of high K dielectrics given the ability to accommodate thicker films without the need to increase operating voltage, which leads to the suppression of pinholes and minimizes problems associated with step coverage.

We successfully fabricated low voltage (< 3V) organic transistors using a 200 nm thick pyrochlore gate dielectric, $Bi_{1.5}Zn_{1.0}Nb_{1.5}O_7$ (BZN), with the highest reported dielectric constant ($3_r$ =50) prepared at a room temperature. The introduction of an extremely thin parylene film between the BZN dielectric and the pentacene semiconductor markedly shifted the threshold voltage, making it possible to fabricate both enhancement (E) and depletion (D) TFTs. Positive threshold voltage and the threshold voltage change caused by parylene may be due to dangling bonds at the BZN surface and the passivation of the dangling bonds. The inverters with depletion load were operated at less than 4V and had an excellent noise margin. The inverter and its performance were the best among the inverters made with OTFTs, with similar gate dielectric thicknesses reported previously in the literature.

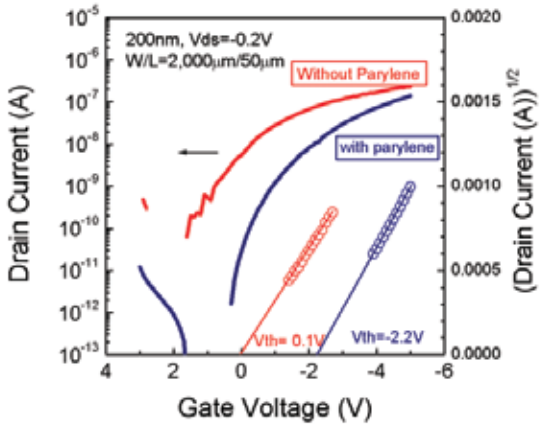


Figure 1: Transfer characteristics of pentacene OTFs with high-k BZN gate dielectric. The OTFTs with parylene and without parylene operated at enhancement and depletion modes, respectively.

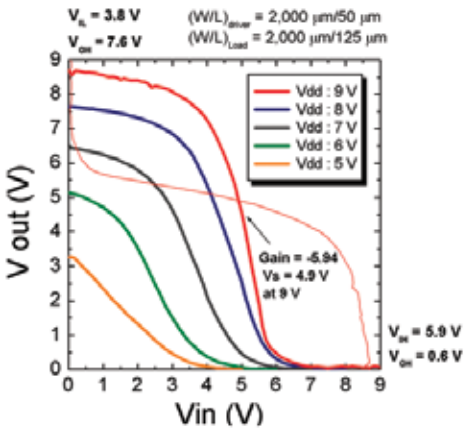


Figure 2: Transfer characteristics of the fabricated inverter with depletion load at various operating voltages.

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# Hybrid Nanocomposite Architectures Using CNTs

E.J. Garcia, D.-J. Shim, B.L. Wardle, in collaboration with S.-G. Kim
Sponsorship: La Caixa Foundation

The world has been promised the widespread use of advanced composite materials for decades. Extremely stiff and strong fibers in a matrix binder (*e.g.,* graphite fibers in an epoxy matrix like that used on the Stealth bomber) provide higher performance relative to metals, and their use is widespread in the military/defense sector, with penetration into other sectors. However, advanced composites have relatively poor performance when loaded in directions off the fiber axis. The objective of the current work is to explore hybrid architectures combining both traditional composite materials and carbon nanotubes (CNTs). Several architectures have been identified for property improvement of traditional composites, and a second theme being considered is to create tough junctures between MEMS devices and macro-scale composite structures.

Key to realizing the hybrid architectures are the nanopelleting technologies and processes developed at MIT by Prof. Sang-Gook Kim [1,2]. The unique nanopelleting process allows single- or multi-wall carbon nanotubes (S/MWNTs) to be grown in a pelletized form suitable for arrangement in various architectures to realize various mechanical, electrical, and other property improvements. Volume fraction of CNTs in the pellets is very high relative to those achieved by other groups. A SEM image of a released aligned CNT pellet is given in Figure 1.

Current work focuses on a specific architecture to create ultra-tough composites [3]. The released CNT pellets (see Figure 1) serve as the starting point for the creation of this architecture. Toughening improvements for a typical composite system have been predicted showing a nanoscale effect on toughness (Figure 2). The manufacture and testing of hybrid composites is ongoing.

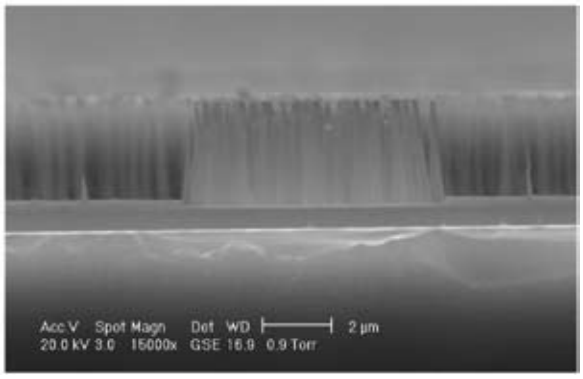


Figure 1: SEM of aligned CNT pellet (courtesy of Prof. Sang-Gook Kim, MIT ME).

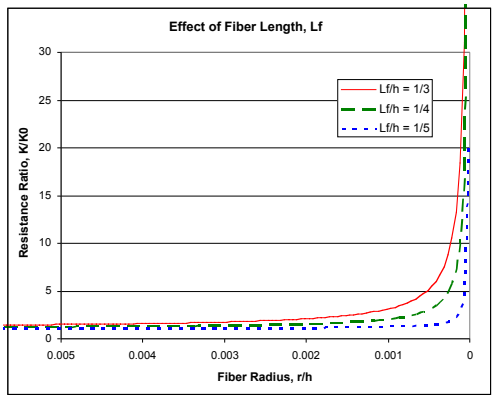


Figure 2: Relative toughness scaling results. E is the composite effective in-plane modulus and $K_0$ is 1.6 MPa$\sqrt{m}$.

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